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Citation	IEEE Transactions on Device and Materials Reliability, 2012, v. 12 n. 1, p. 58-62
Issued Date	2012
URL	http://hdl.handle.net/10722/155740
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Bias-Stress-Induced Instability of Polymer Thin-Film Transistor Based on Poly(3-Hexylthiophene)

Y. R. Liu, R. Liao, P. T. Lai, *Senior Member, IEEE*, and R. H. Yao

***Abstract*—A polymer thin-film transistor (PTFT) based on poly(3-hexylthiophene) (P3HT) is fabricated by a spin-coating process and characterized. Its bias-stress-induced instability during operation is investigated as a function of time and temperature. For negative gate-bias stress, the carrier mobility remains unchanged, the OFF-state current decreases, and the threshold voltage shifts toward the negative direction. On the other hand, for negative drain-bias stress, the carrier mobility decreases slightly, the OFF-state current increases, and the threshold voltage shifts toward the positive direction. The threshold shifts under gate- and drain-bias stresses are observed to be logarithmically dependent on time, and the decay rate of the threshold-voltage shift is independent of temperature. The results suggest that the origin of the threshold-voltage shift upon negative gate-bias stress is predominantly associated with holes trapped within the SiO_2 gate dielectric or at the P3HT/SiO_2 interface, while time-dependent charge trapping in the deep trap states and creation of defect states in the channel region are responsible for the drain-bias stress effect on the PTFT.**

***Index Terms*—Bias stress effect, polymer thin-film transistor (PTFT), stability, threshold-voltage shift.**

I. Introduction

In RECENT years, conjugated polymers have gained increasing interest as the active material in organic thin-film transistors (TFTs) due to their good performance proven with low-temperature processing on a flexible substrate. Among these materials, poly(3-hexylthiophene) (P3HT) has received considerable attention due to its relatively high carrier mobility for low-cost low-power large-area electronic systems such as organic displays [1], sensors [2], and complementary circuits [3]. Great progress has been made to develop high-performance polymer TFTs (PTFTs) over the past decade [4], [5]. However, the environmental stability, reproducibility, and reliability of PTFTs remain significant issues. In particular, the threshold-voltage (V_T) shift of the transistor with time under prolonged bias is critical for practical applications, as it limits the useful range of the transistor and also generates uncertainties in the extraction of device parameters from the PTFT characteristics.

The gate-bias stress effect was universally observed in TFTs based on organic or inorganic amorphous semiconductors, such as pentacene [6], [7], P3HT [8], a-sexithiophene [9], and amorphous silicon [10]. It was also found that the gate-bias stress effect was reversible after removal of the bias. In the literature, several mechanisms have been presented to explain the bias-stress effect. In any particular situation, the origin might be trapping in defect states within the gate dielectric, at the semiconductor/dielectric interface, or in the semiconductor itself; mobile-ion migration; charged-state creation; or bipolaron formation.

So far, many research works have focused on the gate-bias stress effect and its mechanism. However, for analog applications, the PTFT is required to withstand prolonged biasing at both the drain and gate terminals. Thus, in this work, PTFTs are fabricated on a silicon substrate with SiO_2 as the gate insulator and P3HT as the semiconducting active layer. The electrical instabilities of the P3HT PTFT are investigated under gate- or drain-bias stress as a function of time and temperature. The results are useful for deeper understanding of the bias stress effect and the development of PTFTs in organic electronics.

II. Experimental Details

An n/n^+-type (111) silicon wafer with a resistivity of 0.9–1.1 $\Omega \cdot$ cm was used as the substrate material for fabricating the device. A thin layer of gate oxide was grown by thermal dry oxidation at 1000 °C for 1.5×10^4 s. The oxide film on the back side of the silicon substrate was removed to form the gate contact of the PTFT device. Solid P3HT polymer was dissolved in chlorobenzene at a concentration of 10 mg/mL and was spin coated as the semiconducting active layer on the gate oxide at 2000 r/min for 60 s in air; then, the wafer was annealed at 90 °C in air for 600 s. Finally, gold was vacuum evaporated through a shadow mask to form source/drain (S/D) electrodes with a comb-shaped structure. In order to avoid performance degradation of the polymer semiconductor during bias stress measurement due to exposure in air, a thin solid paraffin was dissolved to form a thin passivation layer at 80 °C [11]. The device channel width and length were defined as 10 mm and 100 μm, respectively. The schematic cross section of the PTFT

Manuscript received October 24, 2010; revised April 6, 2011; accepted July 21, 2011. Date of publication August 1, 2011; date of current version March 7, 2012. This work was supported in part by the National Natural Science Foundation of China under Project 61076113, by the Natural Science Foundation of Guangdong Province under Project 8451064101000257, by RGC of Hong Kong under Project HKU 7133/07E, and by the URC for Seed Fund for Strategic Research Theme of HKU on Molecular Materials.

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Digital Object Identifier 10.1109/TDMR.2011.2163408

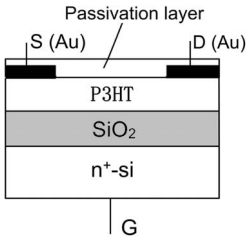

Fig. 1. Schematic cross section of the PTFT.

with top S/D contact configuration after fabrication is shown in Fig. 1.

The thickness of the silicon oxide was measured to be 220 nm by ellipsometry. The thickness of the polymer thin film was determined to be 80 nm by surface profilometry. The output and transfer characteristics of the PTFTs were measured in the dark and air by using an Agilent 4156C semiconductor parameter analyzer and a probe station with temperature control. Two series of bias-stress measurements were performed: one with zero drain bias and various gate biases and the other with zero gate bias and different drain biases. To evaluate the effects of the gate- and drain-bias stresses on the electrical characteristics of the device, the transfer characteristics need to be measured periodically during the stress experiments, and fast measurements and a small number of measured points per transfer curve were required to minimize the influence of the measurement process on the overall bias stress experiments. Since the bias stress effect was reversible after the removal of the bias for a relatively long time, to avoid the variations among different devices, all the bias stress measurements were performed on the same device.

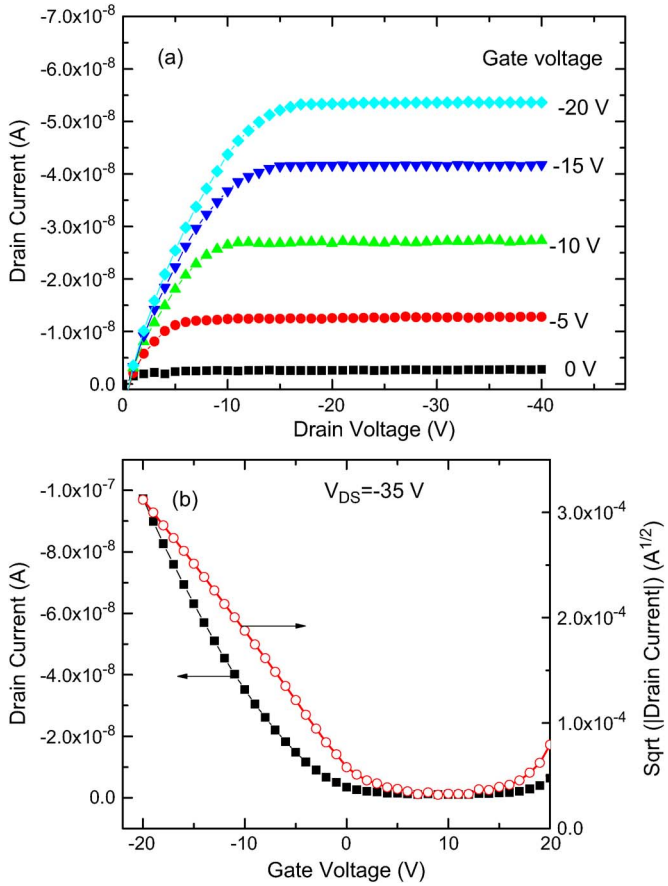

Fig. 2. Typical characteristics of the PTFT measured under dark condition. (a) Output characteristics for various gate voltages. (b) Transfer characteristics for various drain voltages.

III. Results and Discussions

The typical output and transfer characteristics of the PTFT are shown in Fig. 2. It can be seen from Fig. 2(a) that the PTFT shows a good saturation behavior, and a drain current of up to 55 nA can be achieved in the saturation region for a gate voltage of -20 V. For a PTFT operating in the saturation regime ($|V_{\rm DS}| > |V_{\rm GS} - V_T|$), the drain current $I_{\rm Dsat}$ can be described by

$$I_{\rm Dsat} = \frac{W}{2L}\mu_{\rm eff}C_{\rm ox}(V_{\rm GS} - V_T)^2 \qquad (1)$$

where W is the channel width, L is the channel length, $\mu_{\rm eff}$ is the field-effect mobility, $C_{\rm ox}$ is the gate-oxide capacitance per unit area, and V_T is the threshold voltage. According to (1), the field-effect mobility calculated from Fig. 2(b) is 2.1×10^{-4} cm^2/V $\cdot$ s in the saturation region for a drain voltage of -35 V. From the transfer characteristics of the PTFT [Fig. 2(b)], the on/off current ratio is determined to be 100, and a V_T of 4.5 V is extracted for a drain voltage of -35 V.

For the gate-bias stress experiment, with the source and drain connected to ground ($V_{\rm DS} = 0$ V), various gate biases are used as the stress conditions. Fig. 3 shows the evolution of the typical transfer characteristics of the PTFT after subjecting to a negative gate-bias voltage of -20 V for different stress times. It can be observed that there is a parallel shift for the transfer characteristics with increasing stress time under the negative bias stress. A similar parallel shift toward more positive gate voltages under the positive bias stress is also observed. V_T shifts toward the negative direction from rapid to slow with increasing stress time, changing from 6.8 to -1.5 V after a gate-bias stress for a stress time of 600 s. The OFF-state current decreases slightly with increasing stress time, while the subthreshold swing and carrier mobility remain essentially unchanged even after long periods of bias stress, indicating that the gate-bias stress is not related to charge trapping and defect-state creation in the semiconductor channel. The negative shift of V_T upon negative gate-bias stress can be explained as follows. Holes, induced in the channel during the prolonged application of the negative bias stress, are trapped in the defect states located at the P3HT/SiO_2 interface and in the gate dielectric close to the interface under the electric field of the stress. The trapped holes which do not emit immediately may screen the gate electric field when the transfer characteristics of the PTFT are measured and thus cause a negative shift of the threshold voltage. On the other hand, the trapped holes at the P3HT/SiO_2 interface or in the gate dielectric can reduce the leakage current due to the reduction of the effective defect states and thus result in a decrease of the OFF-state current.

The variation of the threshold-voltage shift with the stress time for different gate biases ($V_{\rm GS} = -5$, -10, and -20 V) and a fixed drain bias of 0 V is shown in Fig. 4. It is clear that,

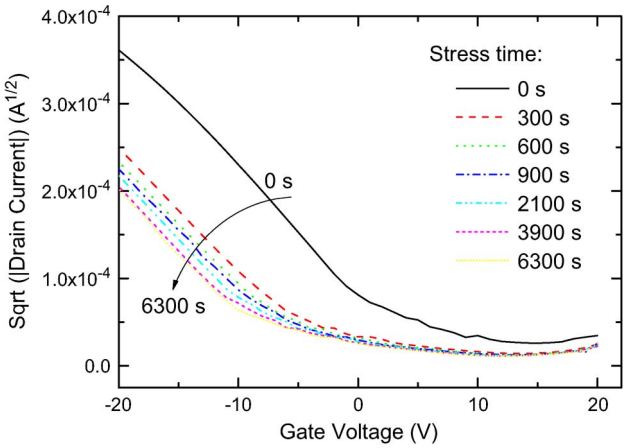

Fig. 3. Transfer characteristics of the PTFT for variable stress times. The stress condition is $V_{\rm GS} = -20$ V and $V_{\rm DS} = 0$ V.

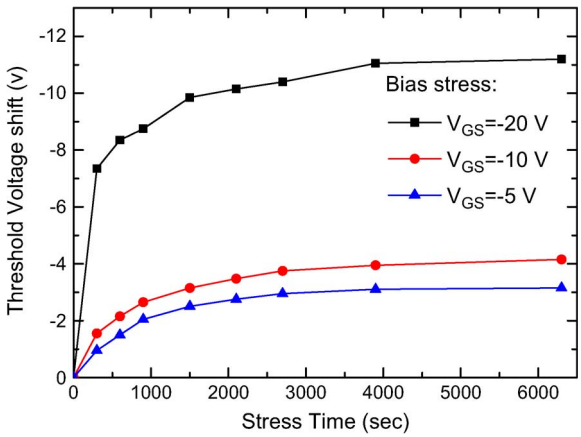

Fig. 4. Shift of the threshold voltage as a function of stress time for different gate-bias stresses and a fixed drain bias of 0 V.

for various gate-bias stresses, V_T rapidly shifts and then quickly saturates, but the shift is not significant below $V_{\rm GS} = -20$ V, indicating that the origin of the V_T shift upon negative gate-bias stress is mainly due to charges (holes) trapped in the deep defect states not too far from the semiconductor/dielectric interface. This is because, for lower stress electric fields, carriers hop or inject directly into the lower energy states located at the P3HT/SiO_2 interface, while for higher stress electric fields, carriers can be trapped in the deeper energy states located in the gate dielectric near the interface, as well as at the P3HT/SiO_2 interface. Moreover, the deep trapping in the gate dielectric close to the interface can occur by means of the Fowler–Nordheim tunneling [12], which depends on the charge density in the channel and/or applied field. Therefore, the higher the applied gate bias, the larger is the V_T shift for the same stress time. In addition, it is found that the time dependence of V_T upon the gate-bias stress follows a logarithmic law for stress at higher gate bias ($V_{\rm GS} = -20$ V), which is different from the power-law stress-time dependence described for amorphous silicon TFTs [13]. The result indicates again that the shift of the threshold voltage is mainly caused by charge trapping because a power law is generally attributed to defect-state creation [14].

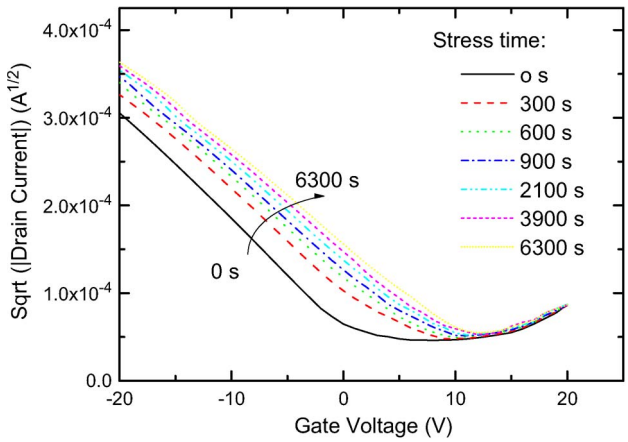

Fig. 5. Transfer characteristics of the PTFT for different stress times. The stress condition is $V_{\rm DS} = -25$ V and $V_{\rm GS} = 0$ V.

For the drain-bias stress experiment, with the source and gate connected to ground ($V_{\rm GS} = 0$ V), various drain biases are used as the stress condition. Fig. 5 shows the transfer characteristics of the PTFT after subjecting to a negative drain-bias voltage of -25 V for different times. With the increase of the stress time, the OFF-state current and the subthreshold swing increase, and the carrier mobility decreases slightly. Moreover, V_T shifts toward the positive direction from rapid to slow, increasing from 4.6 to 10.4 V for a stress time of 600 s. The results indicate that the mechanism of the drain-bias stress effect is different from that of the gate-bias stress effect. The drain-bias stress effect can be explained as follows. Under the negative drain-bias stress, on the one hand, charge carriers (holes) injected from the source electrode are partly trapped in the defect states within the channel, and on the other hand, new defect states are created within the channel by the electric field along the channel for a long period of the applied stress. Therefore, the reduction of the carrier mobility should be due to the Coulomb scattering by the trapped holes and the increase of defect states in the channel. The positive shift of V_T is also attributed to the hole trapping and defect-state creation in the channel. The increases of the OFF-state current and subthreshold swing are related to the release of the trapped holes and defect-state creation in the channel.

Fig. 6 shows the shift of V_T as a function of stress time for three drain biases ($V_{\rm DS} = -10$, -20, and -25 V) and a fixed gate bias of 0 V. Obviously, the time dependence of the V_T shift follows a logarithmic law for all the drain-bias stresses, which is given by [15]

$$\Delta V_T = r_d \cdot \log\left(\frac{t}{t_0} + 1\right) \tag{2}$$

where r_d and t_0 are the model parameters. The decay rate (r_d) of ΔV_T increases with the increase of the drain bias. The reason should be that the concentration and drift velocity of the carriers in the channel increase for higher drain bias, which causes a higher probability of being captured for injected carriers [16] and thus results in an increase of the decay rate and the threshold-voltage shift. The time constant (t_0) of charge trapping decreases with the increase of the drain bias, which is

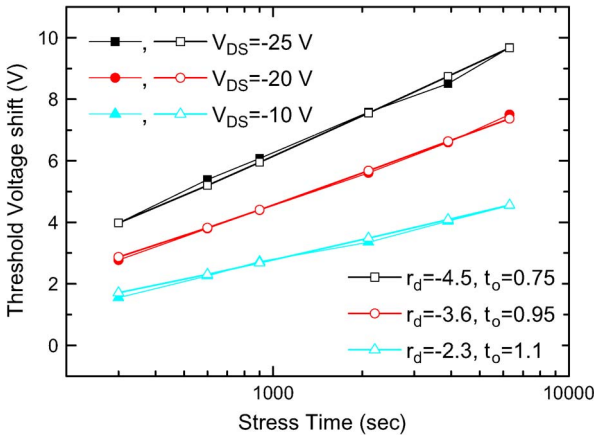

Fig. 6. Shift of the threshold voltage as a function of stress time under different drain biases ($V_{\rm DS} = -10$, -20, and -25 V) and a fixed gate-bias stress of 0 V. The solid symbols represent the measured data, and the open symbols represent the fits to (2), with the parameter values used listed in this figure.

due to having a capturing probability for deeper trap states in the channel region with the increase of the drain bias.

Fig. 7 shows the threshold-voltage shift of the P3HT PTFT as a function of time for different operating temperatures. For both the gate- and drain-bias stresses, all curves show the familiar linear relation, and the decay rate of the threshold-voltage shift is basically independent of the temperature. A possible reason is that the charge-trapping process occurs by carrier tunneling, which is, in principle, temperature independent. In addition, the shift of the threshold voltage increases with increasing temperature for both kinds of stresses. This is because carriers are only trapped in the low-energy states at low temperature, but at higher temperatures, a larger fraction of the defect states can be filled, giving rise to a larger shift of the threshold voltage.

It is worth noting that the gate- and drain-bias effects are related to the original properties of the P3HT PTFT, such as the uniformity of the polymer thin film and the interface characteristics between the P3HT film and the gate dielectric, which are greatly affected by the reproducibility of the fabrication process. All these result in a large variation among devices for the instability of the threshold voltage under the gate- or drain-bias stress. Since, so far, the distributions of defect states in the polymer and the gate dielectric are not known, the exact nature of the instability induced by bias stress needs to be further studied by new methods in the future, e.g., detecting the changes of defect-state distribution in the polymer and gate dielectric during the bias stress measurement.

IV. Conclusion

The electrical instability of a PTFT based on P3HT under gate- or drain-bias stress has been investigated as a function of stress time, stress voltage, and stress temperature. The electrical instability of the PTFT under negative gate-bias stress, such as slight decrease of the OFF-state current and threshold-voltage shift toward the negative direction, is predominantly associated with holes trapped in the deep defect states at the P3HT/SiO_2 interface or in the SiO_2 gate dielectric close to the interface. However, the electrical instability of the PTFT under negative

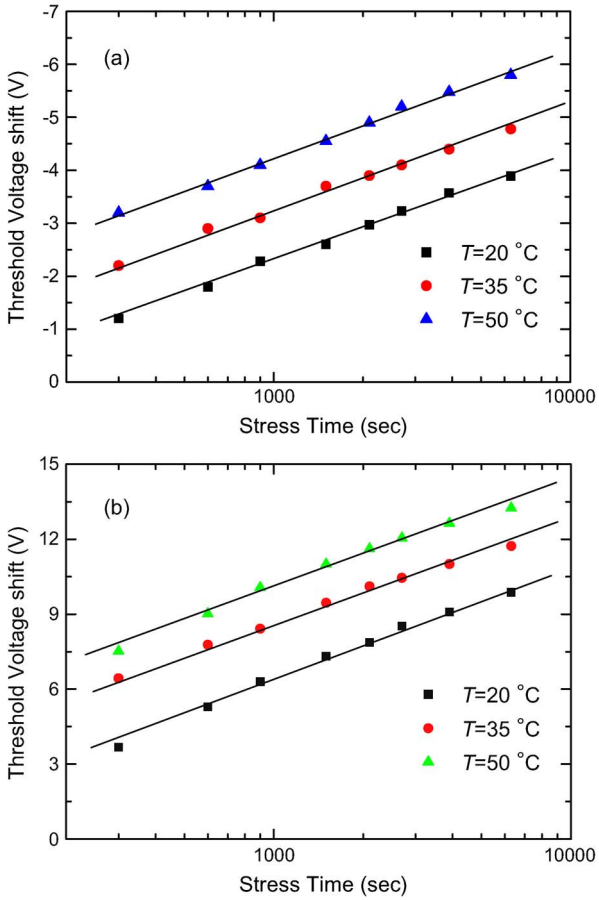

Fig. 7. Shift of the threshold voltage as a function of stress time at various temperatures. (a) Gate-bias stress with a $V_{\rm GS}$ of -10 V and a $V_{\rm DS}$ of 0 V. (b) Drain-bias stress with a $V_{\rm DS}$ of -25 V and a $V_{\rm GS}$ of 0 V.

drain-bias stress, such as increase of the OFF-state current, threshold-voltage shift toward the positive direction, and slight decrease in carrier mobility, is due to charge trapping into deep trap states and creation of defect states in the channel region. For both the gate- and drain-bias stresses, a longer stress time, a larger stress voltage, or a higher stress temperature can cause a larger shift of the threshold voltage because charges are trapped in a larger fraction of defect states with wider energy range.

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