Using Self-Driven AC–DC Synchronous Rectifier as a Direct Replacement for Traditional Power Diode Rectifier

W. X. Zhong, S. Y. Hui, *Fellow, IEEE*, W. C. Ho, *Member, IEEE*, and Xun Liu, *Member, IEEE*

***Abstract*—Synchronous rectification has previously been adopted in switched-mode circuits for reducing the conduction losses particularly in high-frequency, low-voltage, and high-current applications. This paper presents a generalized "self-driven" ac–dc synchronous rectification technique that can be used even at mains frequency to develop an ac–dc synchronous rectifier that behaves like a diode bridge but with much reduced conduction losses and without control integrated circuits. This generalized concept can be extended from single-phase to multiphase systems. Experiments based on 1- and 2-kW single-phase systems have been successfully conducted for capacitive, inductive, and resistive loads. Very significant power loss reduction (over 50%) has been achieved in the rectification stage at both 110- and 220-V ac mains operations. This patent-pending circuit can be regarded as a direct replacement of a general-purpose diode rectifier. Due to the reduction of power loss, further reduction in the size and cost of the heat sink or thermal management for the power circuit becomes possible.**

***Index Terms*—Energy saving, mains-frequency synchronous rectifiers (SRs), self-driven SRs (SDSRs).**

I. Introduction

As early as 1990 [1], synchronous rectifiers (SRs) based on the use of power MOSFETs to replace diodes for reducing the conduction losses have been widely used in low-voltage high-current applications [1]–[16]. SR techniques are primarily applied to various versions of dc–dc converters such as buck converters [2], [3], flyback and buck–boost converters [4], [5], half-bridge converters [6], [7], and LCC resonant converters [8], [9]. To reduce the cost of gate-drive circuits, self-driven techniques have been an active research topic in SRs [2], [7], [9], [10], although gate control integrated circuits for driving SRs are also commercially available [11]. Other research aspects include the use of soft-switching techniques [6], [9], [12]. Aside from dc–dc converters, synchronous rectification techniques have been applied to three-phase full-bridge ac–dc converters based on a three-phase fully controlled bridge [13] and even to five-level converters [14]. While the self-driven technique uses the changing voltage polarity of the coupled windings to control the switching of the power MOSFETs, other techniques tend to use control integrated circuits to provide the gating signals. The first attempt to replace a general-purpose diode bridge with an SR for low-power and low-voltage (3–5-V) applications appears in [15] in which the synchronous rectification technique is applied to a center-tap rectifier topology. A customized charge pump circuit is however needed in the proposal in [15] in order to provide a suitable dc power supply for the gate drive. As such proposal aims at low-voltage applications, it is not suitable for mains-voltage operations. An SR technique for high-power and mains-frequency operation has been proposed previously [17]. It is based on the detection of the phase–phase voltage. Sophisticated logic and timing circuits are needed to provide the gating signals if the ac source has significant source inductance. However, the gating signals for SRs based on voltage detection are not adequate because the diodes of a traditional bridge rectifier only turn off after their current reverse-recovery processes. Therefore, a switch with only voltage detection in an SR may suffer a short-circuit situation during current commutation, particularly when the high dc voltage output of the rectifier is connected across a large smoothing capacitor. It has been pointed out in [18] and [19] that it is more appropriate to use at least one current-sensed gate drive in each current loop of the SR for general power applications.

In this paper, a new ac–dc SR circuit, including a self-driven control circuit, for high-voltage power applications is presented. This new self-driven SR (SDSR) circuit is designed to behave like a traditional diode bridge except that its conduction loss is much smaller than that of a diode bridge. The objective is to develop a low-loss diode rectifier replacement for energy-saving purposes because a diode rectifier is a fundamental circuit component in many power electronic circuits and electronic drive systems. Unlike the concept in [17] which relies on pure voltage detection and complicated logic and timing circuits to differentiate the nature of the loads, the principle proposed here is to design the switching control of the SDSR in such a way that each conducting current loop contains at least one current-controlled MOSFET so that the MOSFET

Manuscript received March 12, 2010; revised July 20, 2010, September 24, 2010, and February 1, 2011; accepted March 14, 2011. Date of publication March 28, 2011; date of current version October 4, 2011. This work was supported by the Centre for Power Electronics, Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong.

W. X. Zhong and W. C. Ho are with the Centre for Power Electronics, Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong (e-mail: wzhong3@student.cityu.edu.hk; wing.ho@convenientpower.com).

S. Y. Hui is with the Department of Electrical and Electronic Engineering, Imperial College London, SW7 2AZ London, U.K. and also with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong (e-mail: r.hui@imperial.ac.uk; ronhui@eee.hku.hk).

X. Liu is with ConvenientPower HK, Ltd., Shatin, Hong Kong (e-mail: xun.liu@convenientpower.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2011.2134052

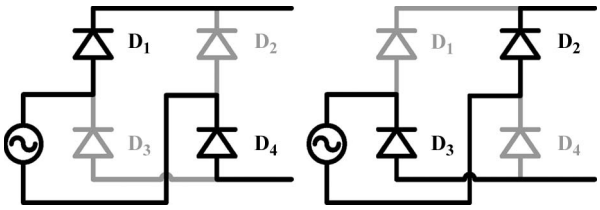


Fig. 1. Conducting paths of a diode bridge.

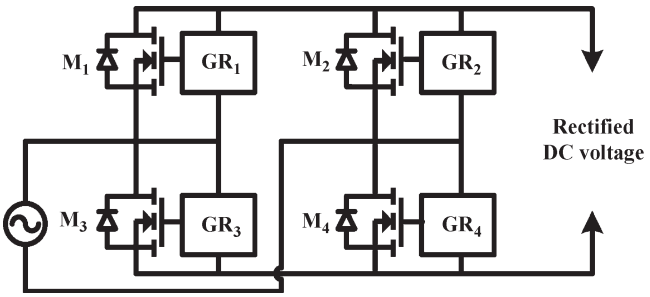


Fig. 2. Concept of the proposed ac–dc SR.

can turn off when the forward current is lower than a preset value (for example, < 0.5 A for 10-A applications). Then, the body diode of the MOSFET will conduct until its current is reversed and its current reverse-recovery process is completed (i.e., like a normal diode). In this way, the "combined actions of the MOSFET and its body diode" provide the normal functions of a power diode. Therefore, the SDSR is able to operate like a diode rectifier regardless of the nature of the loads. Since the body diode only conducts when the current is very small and during the reverse-recovery time, its conduction loss is minimized. This principle has been successfully demonstrated in two single-phase SRs of power up to 2 kW for capacitive, inductive, and resistive loads with significant loss reduction exceeding 50% when compared with a diode bridge at both 110- and 220-V mains. Consequently, the thermal management and heat sink requirements can be reduced, and a more compact rectifier can be achieved for general-purpose mains-frequency ac–dc applications. As an extended version of [22], this paper includes a power loss analysis and a practical comparison of waveforms and efficiency on the SDSR and a diode bridge. The results confirm that the SDSR and diode rectifier operate with identical waveforms but with improved efficiency.

II. Single-Phase SR for Mains-Voltage Operations

A. SDSR Circuit

Fig. 1 shows a traditional single-phase diode bridge with the two conducting paths highlighted. Since a diode will only turn off after the current reverse-recovery process, there should be at least one current-controlled MOSFET in each current path of the equivalent diode-bridge circuit. This diode circuit in Fig. 1 is to be replaced by the proposed circuit concept in Fig. 2. This self-driven ac–dc SR is expected to be a single circuit that can directly replace a traditional power diode bridge in 110-V/60-Hz and 220-V/50-Hz mains. In Fig. 2, M_1 and M_4 form a pair of switches of one conducting path, while M_2 and M_3 are for the other pair in this single-phase system. It should be noted that M_1 to M_4 could be any kind of controlled switches, such as MOSFET and insulated-gate bipolar transistor (IGBT). For IGBT, an antiparallel diode is needed. So long as the combined actions of the IGBT and its antiparallel diode follow the proposed operating principles, the SDSR will behave like a diode rectifier.

The actual circuit implementation of the concept in Fig. 2 is shown in Fig. 3. It should be noted that only four MOSFETs M_1 to M_4 are power devices. The self-driven gate-drive circuits for the four MOSFETs, highlighted in the shaded boxes, are of very low power and can, in principle, be integrated. The whole circuit can be divided into two parts: high- and low-side circuits. Both high- and low-side parts are symmetrical. It is important to note that the four body diodes of power MOSFETs M_1 to M_4 form a standard diode bridge. This means that, even if the gate-drive circuits are not ready for operation immediately at the start-up of the circuit, a standard diode bridge is inherent in the proposed circuit in Fig. 3.

B. Operating Principle—Initial Gate-Drive Start-Up

In this circuit, the power diodes D_1 and D_2 in Fig. 1 are replaced by n-type enhancement power MOSFETs (Fig. 3) which are controlled by sensing the input ac voltage. They are known as "voltage-controlled self-driven" (VCSD) switches and will be turned on alternately according to the polarity of the input voltage. The diodes D_3 and D_4 in Fig. 1 are replaced by power MOSFETs which are controlled by sensing the current through the power MOSFETs. These are called current-controlled self-driven (CCSD) switches. The self-driven gate-drive circuits for M_3 and M_4 are grounded with the power circuits, and their power supplies can thus be derived from the dc voltage of the SR.

As shown in Fig. 3, there are three capacitors in each of the two high-side driving circuits (C_1, C_2, and C_3 for M_1; C_4, C_5, and C_6 for M_2). Each upper gate drive has three driving stages. Taking M_1 as an example, Q_2 and Q_3, M_5 and M_6, and Q_4 and Q_5 form the three driving stages. Q_2 and Q_3 are for a signal amplifying and providing a charging path for the power supplies of the driving circuit of M_2, M_5 and M_6 form an inverter, and Q_4 and Q_5 are for fast driving of the power MOSFET M_1. C_1 and C_4 will be charged up as the power supplies of the first-stage driving pair. Before C_1 and C_4 have been charged up to a certain threshold voltage, for example, 10 V, the driving logic in the circuit will not be ready. C_3 and C_6 are to be charged as the power supplies for driving M_1 and M_2, respectively. In the start-up stage, C_2 and C_5 are designed to be charged up faster than C_1 and C_4 until they reach a certain voltage which is decided by the Zener diodes D_{Z1} and D_{Z2}. Bipolar transistors Q_1 and Q_6 are used to ensure that C_3 and C_6 will not be *charged* before C_1 and C_4 have been charged up to a voltage higher than the voltage of C_2 and C_5. Therefore, the MOSFETs M_1 and M_2 will not switch before the driving logic has been set up.

C. Operation Principle of the High-Side Gate Drives

C_1 and C_4 will be charged and discharged at line frequency. Assume that C_1 and C_4 will be charged up to V_1, for example,

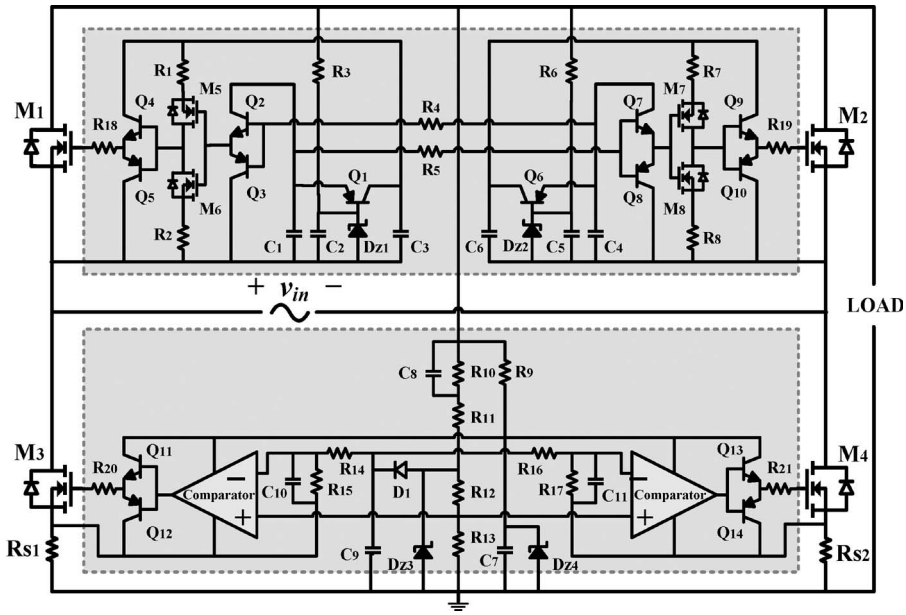


Fig. 3. Proposed SDSR.

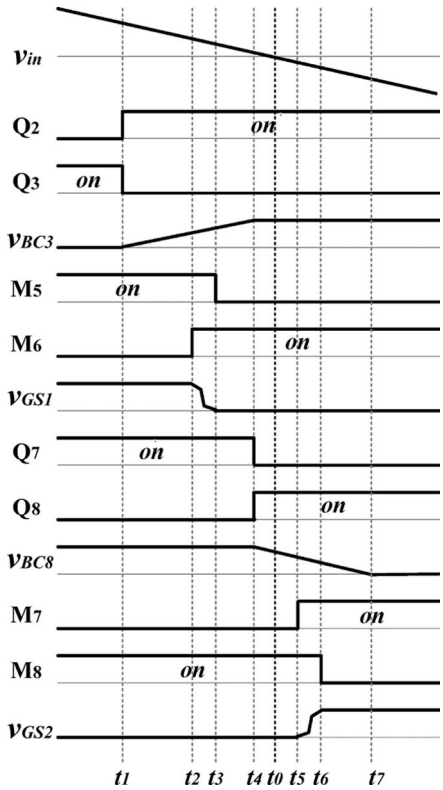


Fig. 4. Timing diagram for the high-side gate-drive circuits.

13 V, in every charging period and will be discharged to V_2, for example, 12 V, which is a little lower than V_1 after every discharging period. Here, we use $v_{\rm BC3}$ and $v_{\rm BC8}$ to represent the base–collector voltages of bipolar junction transistors $\rm Q_3$ and $\rm Q_8$, respectively. With the aid of the timing diagram in Fig. 4, the operation of the high-side gate drives can be explained as follows.

(a) Before t_1: $v_{\rm in}$ is higher than V_1. Both the current directions in R_4 and R_5 are from left to right as shown in Fig. 5(a). $v_{\rm BC3}$ is clamped to zero by the p-n junction between the collector and base of $\rm Q_3$. Therefore, the p-channel MOSFET $\rm M_5$ is turned on, and the n-channel MOSFET $\rm M_6$ is turned off; such condition keeps the gate–source voltage of $\rm M_1$ high and thus turns $\rm M_1$ on. Meanwhile, the current in R_5 flows through the p-n junction between the base and collector of $\rm Q_7$, which clamps $v_{\rm BC8}$ to V_1. Therefore, $\rm M_7$ is turned off and $\rm M_8$ is turned on to keep the gate–source voltage of $\rm M_2$ low.

(b) t_1–t_2: As shown in Fig. 5(b), when $v_{\rm in}$ becomes lower than V_1 after t_1, the current in R_4 changes its direction. $\rm Q_2$ is turned on, and $\rm Q_3$ becomes off. $v_{\rm BC3}$ starts to increase from zero. At the end of this interval, $v_{\rm BC3}$ reaches the gate threshold voltage of $\rm M_6$.

(c) t_2–t_3: $\rm M_6$ begins to conduct at t_2. $v_{\rm GS1}$ starts to decrease from high. $v_{\rm BC3}$ continues increasing. Before it reaches the threshold voltage for $\rm M_5$ to switch off at t_3, $\rm M_5$ and $\rm M_6$ will conduct simultaneously as shown in Fig. 5(c). Within this interval, $v_{\rm GS1}$ will fall down to the gate threshold voltage of $\rm M_1$, the time of which can be slightly controlled by the ratio of R_1 to R_2. The interval ends when $v_{\rm GS1}$ falls to zero and $\rm M_1$ is turned off.

(d) t_3–t_4: As shown in Fig. 5(d), $\rm M_5$ is turned off at t_3, and $\rm M_6$ keeps on to keep $\rm M_1$ off. Current flows through the source–drain diode of $\rm M_1$.

(e) t_4–t_0: As shown in Fig. 5(e), when $v_{\rm in}$ becomes lower than $V_1 - V_2$ after t_4, the current in R_5 changes its direction. $v_{\rm BC8}$ begins to decrease from V_1, indicating that $\rm Q_7$ is turned off and $\rm Q_8$ is turned on. While at t_4, $v_{\rm BC3}$ reaches V_2 and will be clamped to the voltage of $\rm C_3$ by the p-n junction between the base and collector of $\rm Q_2$.

(f) t_0–t_5: Because $V_1 - V_2$ is a positive value, $v_{\rm in}$ commutates at t_0 which is after t_4. At t_0, the source–drain diode of $\rm M_1$ begins to turn off, and the source–drain diode of

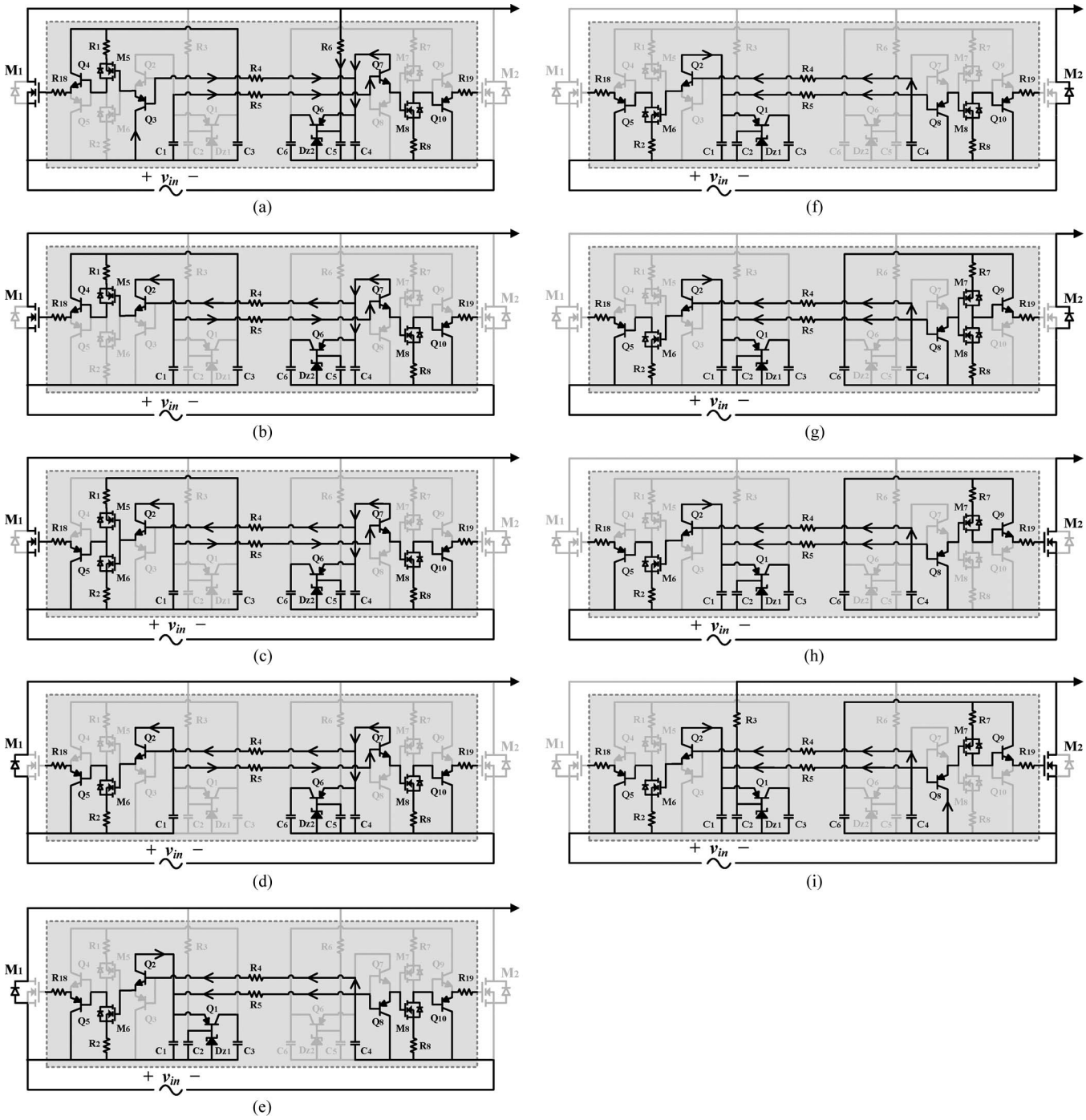


Fig. 5. Operation intervals of the proposed high-side driver. (a) Before t_1; (b) t_1-t_2; (c) t_2-t_3; (d) t_3-t_4; (e) t_4-t_0; (f) t_0-t_5; (g) t_5-t_6; (h) t_6-t_7; and (i) after t_7.

M_2 begins to conduct naturally, as shown in Fig. 5(f). The interval ends when $v_{\rm BC8}$ falls down to the threshold voltage for M_7 to switch on.

(g) t_5-t_6: As shown in Fig. 5(g), M_7 begins to conduct at t_5, and $v_{\rm BC8}$ continues decreasing. Before $v_{\rm BC8}$ falls down to the gate threshold voltage of M_8 at t_6, M_7 and M_8 conduct simultaneously. At the end of the interval, $v_{\rm GS2}$ reaches high, and M_2 is turned on.

(h) t_6-t_7: At t_6, M_8 is turned off, and $v_{\rm BC8}$ continues decreasing, as shown in Fig. 5(h). The interval ends when $v_{\rm BC8}$ reaches zero.

(i) After t_7: $v_{\rm in}$ is lower than $-V_2$. $v_{\rm BC8}$ is clamped to zero by the p-n junction between the collector and base of Q_8 as shown in Fig. 5(i).

D. Operation Principle of the Low-Side Gate Drives

The low-side MOSFETs are controlled by "current-controlled" gate-drive circuits. Current-sensing resistors $R_{\rm S1}$ and $R_{\rm S2}$ and comparators are used to detect the MOSFET currents and drive the MOSFETs. In principle, the ON-state resistances of the MOSFETs can also be used to replace the

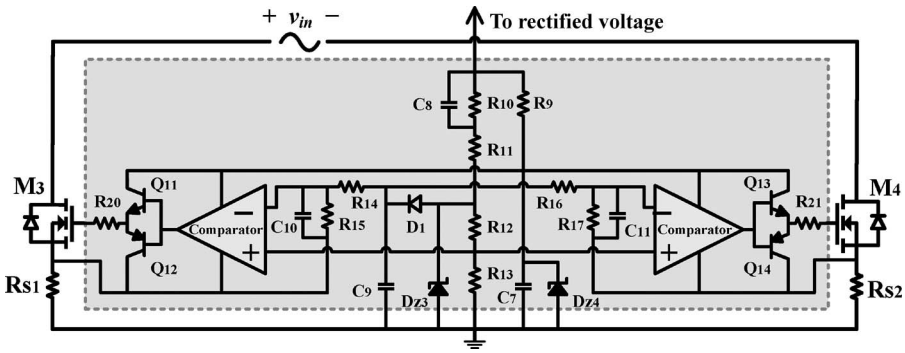


Fig. 6. Low-side circuit of the proposed SR.

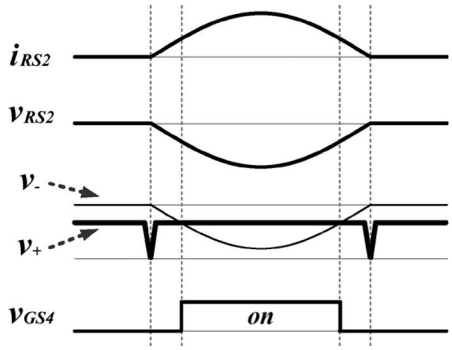


Fig. 7. Timing diagram for the low-side gate-drive circuits.

sensing resistors if desired. As shown in Fig. 6, C_9 is used to give a positive voltage for the inverting inputs of the comparators which can provide a safe margin set by the potential divider comprising resistors R_{14} to R_{17}. The voltage of C_7, stabilized by the Zener diode D_{Z4}, is the power supply for the comparators. C_9 will be charged up to the designated voltage before the voltage of C_7 reaches a voltage high enough for the comparators to work. This arrangement ensures the low-side MOSFETs M_3 and M_4 to be switched only when the proper logic control is ready.

Fig. 7 shows the timing diagram for the gate drive of M_4 as an example to demonstrate the operation principles of the low-side circuits. The source voltage of M_4 (with respect to ground) and the voltage at the inverting input of the comparator will be pulled down when there is a current flowing through R_{S2}. The voltage at the noninverting input of the comparator will be like a rectangular waveform as discussed in the next section. Therefore, when v_- is lower than v_+, the comparator output voltage will turn M_4 on.

E. Additional Circuit to Ensure Turning Off at Zero-Crossing Points

The SDSR is designed to cope with resistive, capacitive, and inductive loads. Typical driving waveforms of the low-side circuits are shown in Fig. 8, in which i_{in} is the input current having the same polarity of $v_{\rm in}$.

When the SDSR is connected to an inductive load, the input current will commutate very quickly after every half cycle. The comparators may not respond quickly enough to turn off

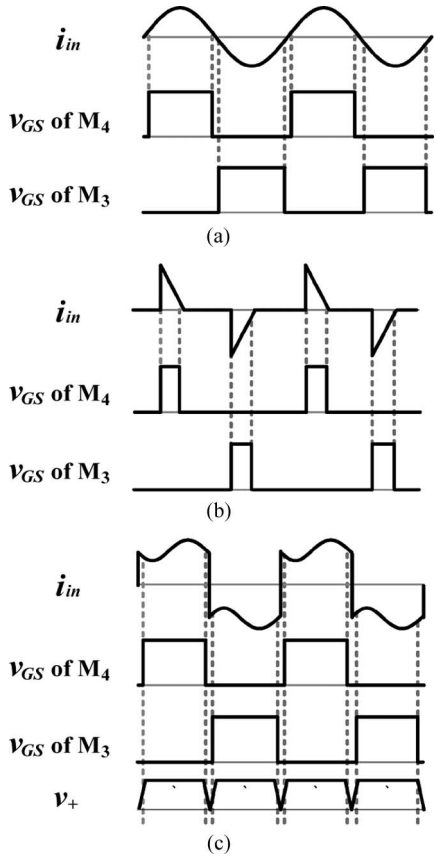


Fig. 8. Driving waveforms of the low-side circuit. (a) Resistive load; (b) capacitive load; and (c) inductive load.

MOSFETs M_3 and M_4 under such a fast current change, which may cause a fatal short-circuit situation. Therefore, an extra circuit (Fig. 9) is added to provide a small positive signal to the noninverting inputs of the two comparators. The signal is generated from the rectified voltage as shown in Fig. 1, and it can guarantee the comparators to turn off the MOSFETs in time. In Fig. 9, D_{Z3} is a Zener diode of about 10 V. When the rectified voltage begins to rise from zero, the voltage of D_{Z3} will rise until it reaches its rating voltage, and then, it will keep at this voltage with very small fluctuation. Moreover, R_{12} and R_{13} here form a voltage divider for scaling down a voltage signal with reduced fluctuation. The rising and falling periods of the signal can be slightly shaped by the value of C_8 and the ratio of R_{10} to R_{11}.

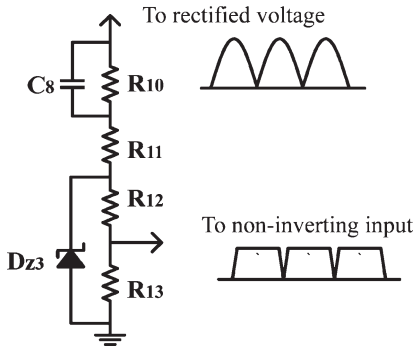


Fig. 9. Additional circuit to guarantee the comparators to turn off.

F. Power Loss Analysis of Diode Bridge and SDSR

The power loss of the SR circuit can be expressed as

$$P_{\mathrm{SR}} = P_{\mathrm{Driver}} + P_S + P_{\mathrm{SW}} \tag{1}$$

where P_{Driver} is the power loss of the driver of the SR circuit (not including current-sensing loss), P_S is the power loss of the current-sensing resistors, and P_{SW} is the power loss of the switches used in the SDSR circuit which, in this paper, are MOSFETs. P_{Driver} is low enough to be neglected; however, it mainly consists of the losses produced by R_4, R_5, and R_9. Therefore

$$P_{\mathrm{Driver}} \approx \left(\frac{V_{\mathrm{in}}^2}{R_4} + \frac{V_{\mathrm{in}}^2}{R_5}\right) + \frac{V_{\mathrm{out}}^2}{R_9} \tag{2}$$

$$P_S = I^2 R_s \tag{3}$$

where R_s is the current-sensing resistance.

$$P_{\mathrm{SW}} = 2I^2 R_{\mathrm{DS(on)}} \tag{4}$$

where $R_{\mathrm{DS(on)}}$ is the ON-state resistance of the MOSFETs.

For the power loss of the diode bridge

$$P_{\mathrm{DB}} = 2V_F I \tag{5}$$

where V_F is the forward voltage of the diode and can be considered as a constant in a rough estimation.

From (1)–(5), we can find out the current range, within which the power loss of the SR can be lower than that of a diode bridge

$$\frac{V_F - \sqrt{V_F^2 - \left(R_s + 2R_{\mathrm{DS(on)}}\right) P_{\mathrm{Driver}}}}{R_s + 2R_{\mathrm{DS(on)}}} < I < \frac{V_F + \sqrt{V_F^2 - \left(R_s + 2R_{\mathrm{DS(on)}}\right) P_{\mathrm{Driver}}}}{R_s + 2R_{\mathrm{DS(on)}}}. \tag{6}$$

In the prototype, $R_4 = R_5 = 1.3$ MΩ, $R_9 = 1$ MΩ, $R_s = 0.002$ Ω, $R_{\mathrm{DS(on)}} = 0.045$ Ω, and $V_F < 1.1$ V at 30 A ($V_F = 1$ V is assumed for the calculation).

When $V_{\mathrm{out}} = V_{\mathrm{in}} = 110$ V, $P_{\mathrm{Driver}} \approx 31$ mW, and the current range is $0.016 < I < 21.724$ A.

When $V_{\mathrm{out}} = V_{\mathrm{in}} = 220$ V, $P_{\mathrm{Driver}} \approx 124$ mW, and the current range is $0.062 < I < 21.677$ A.

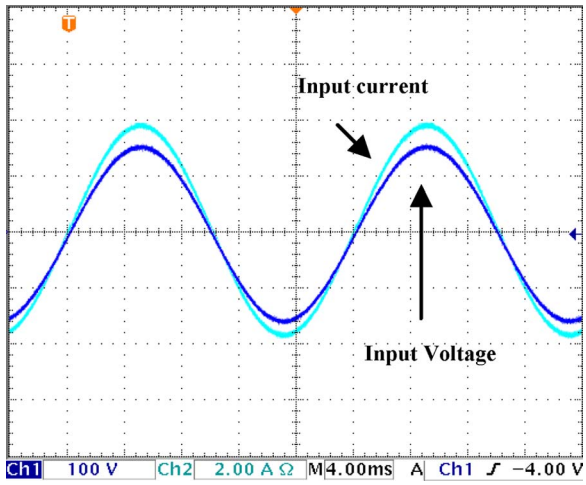


Fig. 10. (Ch1) Input voltage and (Ch2) input current of the diode bridge.

Since the body diodes of the MOSFETs are used during the start-up phase of the system (before the dc output is ready to power the control electronic circuit of the SDSR) and after the corresponding MOSFETs have turned off at near-zero current (about 0.5 A), the conduction loss of the body diodes of the MOSFETs is negligible. In general, the power losses of the diode rectifier and the SDSR for the capacitive load and inductive load can be analyzed in the same way as the resistive load. The major power loss reduction component comes from the difference between the conduction losses of the diodes in the diode bridge and the ON-state resistance of the MOSFETs in the SDSR. For a current of 10 A, for example, a diode has a conduction loss of about 10 W, while a MOSFET (with an ON-state resistance of 45 mΩ) only dissipates 4.5 W.

III. Experimental Verification Based on a Single-Phase SR

A diode bridge comprising diodes 60EPF06PbF with a forward voltage drop of about 0.85 V is used to compare with the SDSR in Fig. 3 based on MOSFETs IPW60R045CP with an ON-state resistance of 45 mΩ. Resistive, capacitive, and inductive loads are used for the evaluation of the proposed SDSR.

A. Resistive Load

Fig. 10 shows the input voltage and input current of the diode bridge for a resistive load. Fig. 11 shows the gate–source voltages (V_{GS}) of the high-side (VCSD) MOSFETs of the SDSR with respect to the input voltage waveform for a resistive load. Fig. 12 shows the corresponding gate signals for the low-side (CCSD) MOSFETs and the input current of the SDSR. It can be seen that the input voltage and input current waveforms of a diode rectifier fed with a resistive load in Fig. 10 are identical to the input voltage waveform (Fig. 11) and input current waveform (Fig. 12) obtained from the proposed SDSR for the same resistive load.

B. Capacitive–Resistive Load

The measured input voltage and input current waveforms of the diode bridge for a capacitive–resistive load are shown

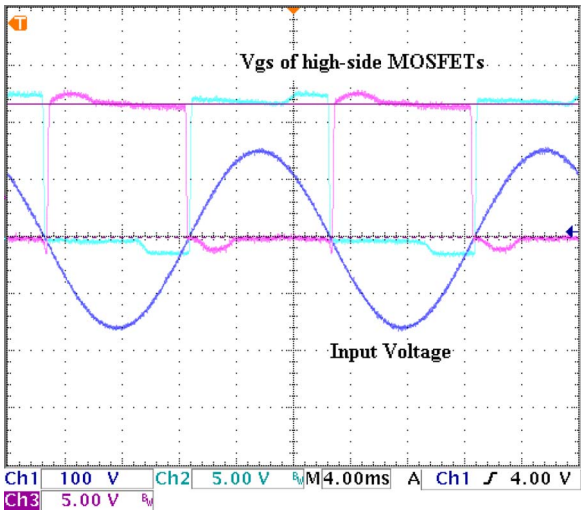


Fig. 11. (Ch1) Input voltage and (Ch2 and Ch3) gate–source voltages of the high-side (VCSD) MOSFETs of the SDSR.

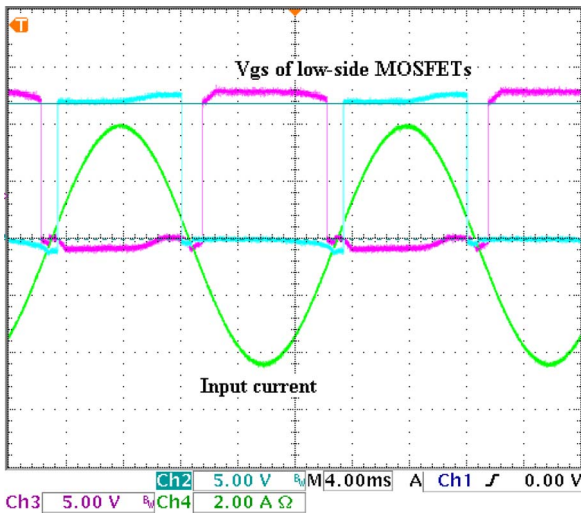


Fig. 12. (Ch4) Input current and (Ch2 and Ch3) gate–source voltages of the low-side (CCSD) MOSFETs of the SDSR.

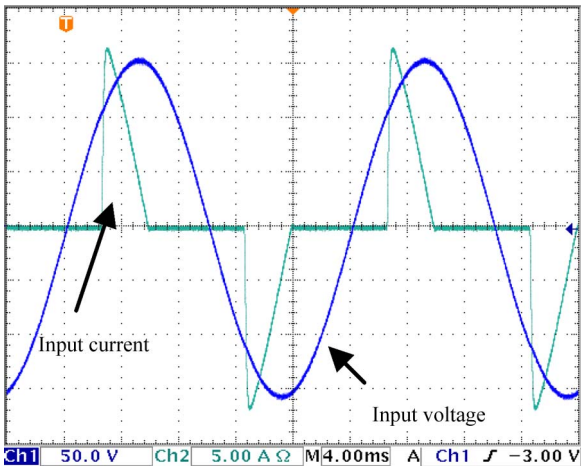


Fig. 13. (Ch1) Input voltage and (Ch2) input current of the diode bridge.

in Fig. 13. Input current pulses are observed as expected for a capacitive–resistive load. The SDSR is used to drive the same capacitive–resistive load. The input voltage and the gate signals

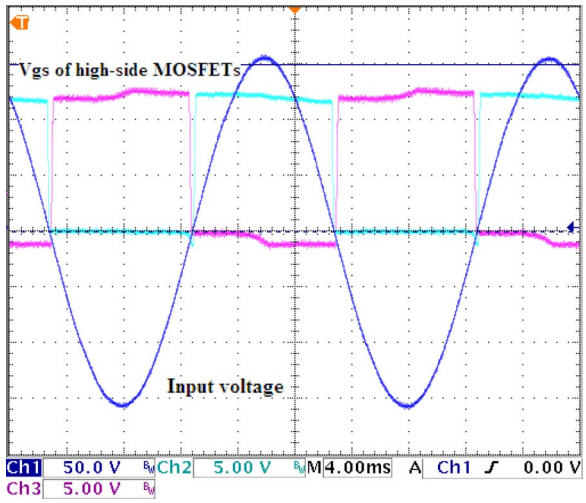


Fig. 14. (Ch1) Input voltage and (Ch2 and Ch3) gate–source voltages of the high-side (VCSD) MOSFETs of the SDSR.

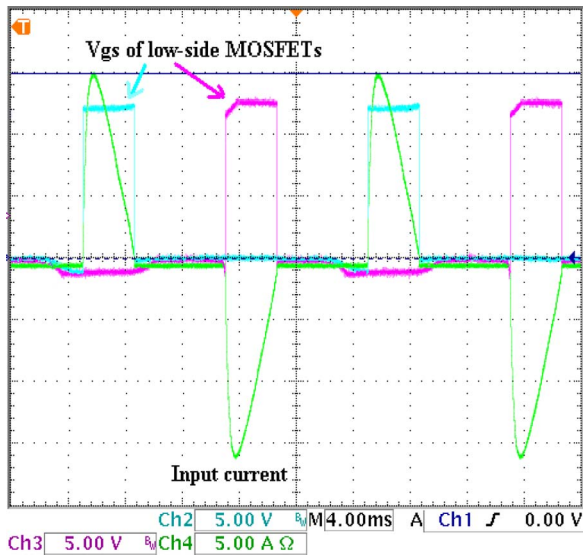


Fig. 15. (Ch4) Input current and (Ch2 and Ch3) gate–source voltages of the low-side (CCSD) MOSFETs of the SDSR.

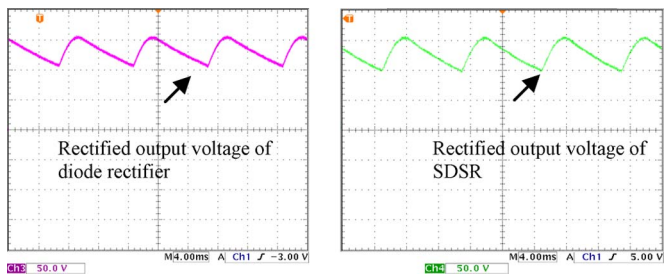


Fig. 16. Output capacitor voltage of (left) the diode bridge and (right) the SDSR.

for the high-side (VCSD) MOSFETs are shown in Fig. 14, and the input current and the gate signals for the low-side (CCSD) MOSFETs are shown in Fig. 15. The rectified dc output voltage waveforms of the diode bridge and the SDSR are shown in Fig. 16. It is noted that the input current and output voltage

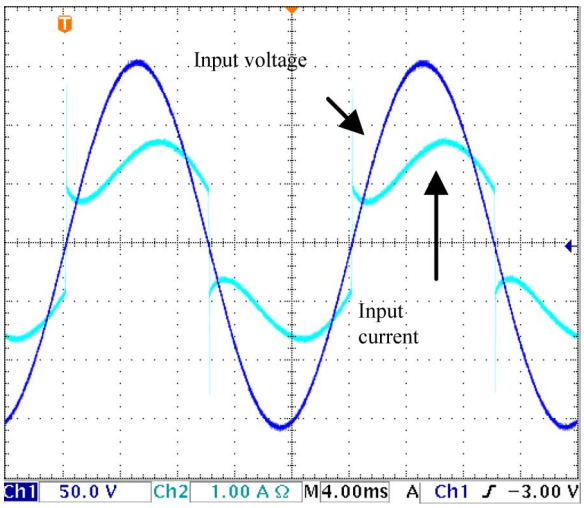


Fig. 17. (Ch1) Input voltage and (Ch2) input current of the diode bridge.

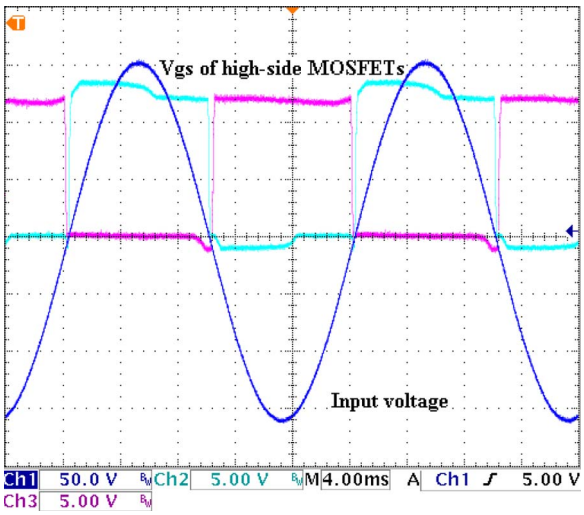


Fig. 18. (Ch1) Input voltage and (Ch2 and Ch3) gate–source voltages of the high-side (VCSD) MOSFETs of the SDSR.

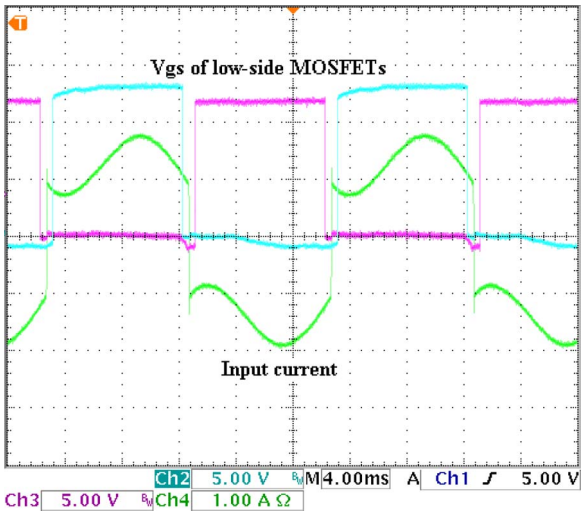


Fig. 19. (Ch4) Input current and (Ch2 and Ch3) gate–source voltages of the low-side (CCSD) MOSFETs of the SDSR.

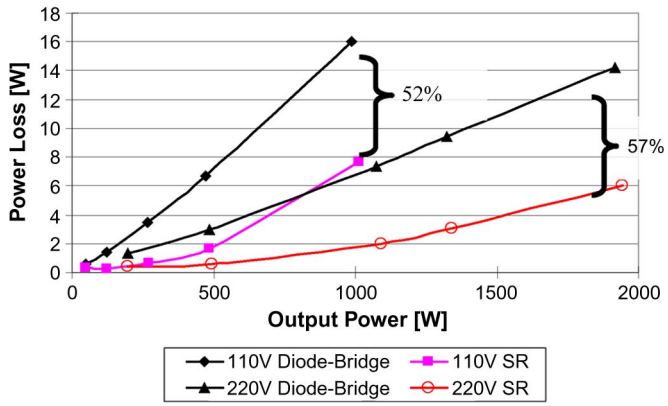


Fig. 20. Power loss versus system power comparison of the diode rectifier and the self-driven rectifier with a resistive load.

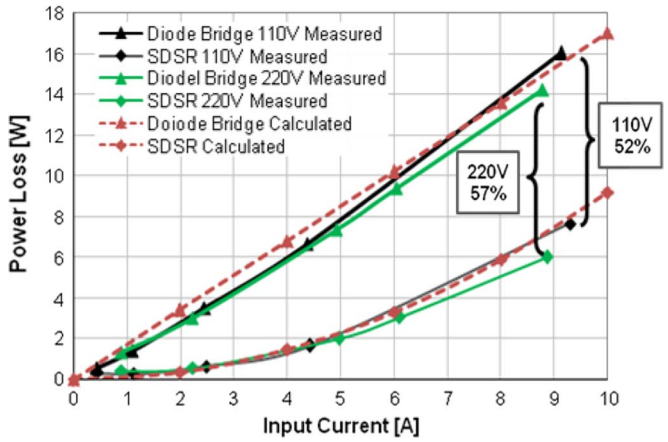


Fig. 21. Measured and calculated power losses versus input current.

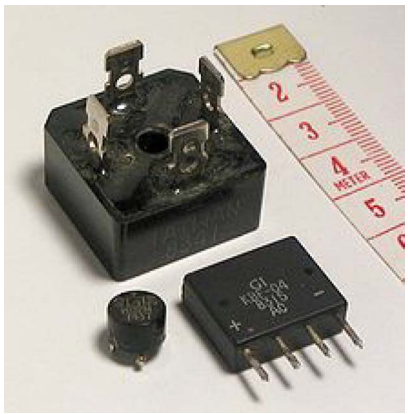


Fig. 22. Photograph of single-phase diode rectifier products.

waveforms of the SDSR are essentially the same as those of a diode bridge for the same capacitive–resistive load.

C. Inductive–Resistive Load

Tests are repeated with an inductive–resistive load for the diode bridge and the SDSR. The measured input voltage and input current waveforms of the diode bridge are shown in Fig. 17. The input voltage and the high-side (VCSD) gate signals are shown in Fig. 18. The input current and the low-side (CCSD)

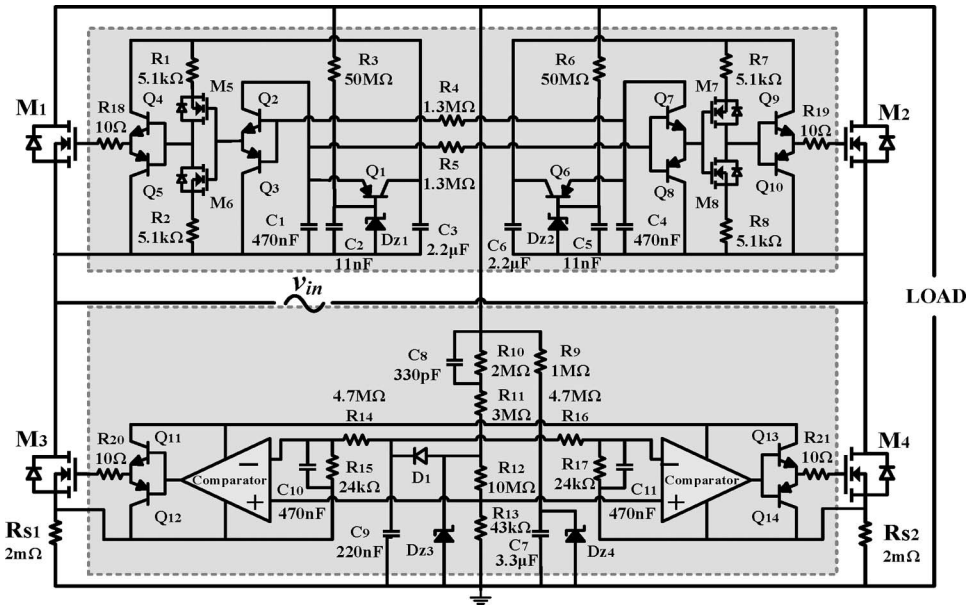


Fig. 23. Single-phase SDSR with practical component values.

gate signals are shown in Fig. 19. Again, the input current waveforms of the diode bridge and the SDSR are essentially the same. These practical measurements confirm that the proposed SDSR behaves like a diode bridge for different types of loads.

D. Power Loss Comparison of the Diode Bridge and the Proposed SDSR

The forward voltage drop of diode 60EPF06PbF is found out to be about 0.85 V in the experiments. The power loss of the diode bridge is $P_{\rm DB} = 2V_F I$. For MOSFET IPW60R045CP, $R_{\rm DS(on)} = 0.045\ \Omega$. The power loss of the SDSR is approximately $P_{\rm SR} = I^2(2R_{\rm DS(on)} + R_S)$ when the power losses of the gate drives are ignored.

Fig. 20 shows the measured power loss versus system output power of the SR and the diode-bridge rectifier under the mains operation of 110 V (up to 1 kW of output power) and 220 V (up to 2 kW of output power). At 1-kW and 110-V operation, a 52% power loss reduction has been achieved. At 2-kW and 220-V operation, the power loss reduction is 57%.

Based on the power loss analysis described in the previous section, the measured and calculated power losses versus the input current are also shown in Fig. 21. It can be seen that the calculated power loss curves agree quite well with measurements.

Fig. 22 shows a photograph of several single-phase diode rectifiers. A power loss of reduction of 8 W within such a small area can certainly reduce the thermal stress on the device and also on the size of the heat sink.

Fig. 23 shows a typical circuit implementation with the component values that are used in this project. The control circuit can, in principle, be built in the same module block with the MOSFETs so that the module can be a replacement of the diode rectifier module.

IV. Conclusion

This paper has presented a self-driven ac–dc SR that can replace a diode bridge as a general-purpose ac–dc rectifier. The proposal relies on simple circuits and can provide the normal rectification functions for resistive, capacitive, and inductive loads as a traditional diode rectifier does, except that the power loss of the proposed SDSR is at least 50% less than that of a diode bridge. This circuit has been practically and successfully demonstrated in a 1-kW system under 110-V mains operation (with 50% power loss reduction) and a 2-kW system under 220-V mains operation (with 57% power loss reduction). The identical measured waveforms of the proposed circuit and a diode bridge confirm that a diode bridge can be replaced by the proposed circuit. Cost reduction in the size of the heat sink and the energy saving can compensate for the minor increase in the component counts of the inexpensive and low-power components. High system compactness due to reduced heat dissipation can also be achieved. This proposal can, in principle, be extended to multiphase rectification systems [20], [21]. The control circuit takes advantage of the output dc voltage for its power supply. Since the body diodes of the MOSFETs provide the normal rectification function in the initial start-up stage, there is no initial start-up issue for the control circuit, which can be incorporated in the same block of the SR product.

References

[1] W. A. Tabisz, F. C. Lee, and D. Y. Chen, "A MOSFET resonant synchronous rectifier for high-frequency DC/DC converters," in *Proc. 21st Annu. IEEE Power Electron. Spec. Conf. Rec.*, Jun. 11–14, 1990, pp. 769–779.

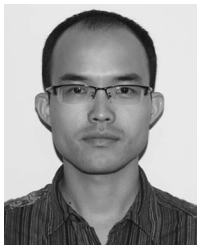
[2] K. Fukushima, T. Hashimoto, T. Ninomiya, and T. Segawa, "Analysis of abnormal phenomenon in common-source-type forward converter with self-driven synchronous rectifier," in *Proc. CES/IEEE 5th IPEMC*, Aug. 14–16, 2006, vol. 2, pp. 1–5.

[3] K. Murata, K. Harada, and T. Harimoto, "Self turn-on loss of MOSFET as synchronous rectifier in DC/DC buck converter—In case of a low driving impedance," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19, 2008, pp. 3348–3353.

[4] B.-S. Kim, H.-S. Ryu, M.-S. Shin, J.-H. Lee, and I.-H. Lim, "Design of flyback converter with voltage driven synchronous rectifier," in *Proc. 12th Int. EPE-PEMC*, Aug. 2006, pp. 631–635.

[5] R. Jaschke, "Conduction losses in DC/DC-converters as buckboost/boostbuck synchronous rectifier types," in *Proc. CPE*, May 29–Jun. 1, 2007, pp. 1–10.

[6] O. Garcia, J. A. Cobos, J. Uceda, and J. Sebastian, "Zero voltage switching in the PWM half bridge topology with complementary control and synchronous rectification," in *Proc. 26th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 18–22, 1995, vol. 1, pp. 286–291.
[7] G.-Y. Jeong, "High efficiency asymmetrical half-bridge converter using a self-driven synchronous rectifier," *IET Power Electron.*, vol. 1, no. 1, pp. 62–71, Mar. 2008.
[8] Y. Ma, X. Xie, and Z. Qian, "Frequency-controlled LCC resonant converter with synchronous rectifier," in *Proc. 7th Int. Conf. PEDS*, Nov. 27–30, 2007, pp. 1442–1445.
[9] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.
[10] J. A. Cobos, P. Alou, O. Garcia, J. Uceda, and M. Rascon, "New driving scheme for self driven synchronous rectifiers," in *Proc. 14th Annu. IEEE APEC*, Mar. 14–18, 1999, vol. 2, pp. 840–846.
[11] E. Janssen, "GreenChip SR: Synchronous rectifier controller IC," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 4–7, 2007, pp. 2319–2325.
[12] H. Mao, O. Abdel Rahman, and I. Batarseh, "Zero-voltage-switching DC–DC converters with synchronous rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 369–378, Jan. 2008.
[13] B.-H. Kwon, J.-H. Youm, and J.-W. Lim, "A line-voltage-sensorless synchronous rectifier," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 966–972, Sep. 1999.
[14] R. Portillo, J. M. Carrasco, J. I. Leon, E. Galvan, and M. M. Prats, "Modeling of five-level converter used in a synchronous rectifier application," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 16, 2005, pp. 1396–1401.
[15] M. I. Mihaiu, "Toward the "ideal diode" using power MOSFET in full wave synchronous rectifiers for low voltage power supplies," in *Proc. Int. SPEEDAM*, Jun. 11–13, 2008, pp. 1384–1387.
[16] P.-Y. Chen, M. Jinno, and Y.-M. Shie, "Research on the reverse conduction of synchronous rectifiers," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1570–1575, Apr. 2008.
[17] B. Vaysse, "Mosgate device driver for synchronous rectification of a 3-phase sinusoidal source," U.S. Patent 6 765 425, Jul. 20, 2004.
[18] W. C. Ho, S. Y. R. Hui, and X. Liu, "Single-phase self-driven full-bridge synchronous rectification," U.S. Patent Application: US12/194,921, Aug. 20, 2008.
[19] W. C. Ho, S. Y. R. Hui, X. Liu, and W. P. Choi, "Generalized AC–DC synchronous rectification techniques for single- and multi-phase systems," U.S. Patent Application: US 12/274,469, Nov. 20, 2008.
[20] S. Y. R. Hui, W. X. Zhong, and W. C. Ho, "Control circuits for self-driven synchronous rectifier as energy-efficient replacement for diode rectifier," U.S. Provisional Patent Application 61/304,09, Dec. 2, 2010.
[21] W. X. Zhong, W. C. Ho, and R. S. Y. Hui, "Generalized self-driven ac–dc synchronous rectification techniques for single- and multi-phase systems," *IEEE Trans. Ind. Electron.*, to be published.
[22] W. X. Zhong, W. C. Ho, X. Liu, and S. Y. R. Hui, "Self-driven AC–DC synchronous rectifier for power applications: A direct energy-efficient replacement for traditional diode rectifier," in *Proc. IEEE APEC*, 2010, pp. 994–1001.



W. X. Zhong was born in China in 1984. He received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2007. He is currently working toward the Ph.D. degree in the Centre for Power Electronics, Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong.

His current research interests include synchronous rectification and wireless power transfer.

S. Y. (Ron) Hui (F'03) received the B.Sc.Eng. (Hons.) degree from the University of Birmingham, Birmingham, U.K., in 1984 and the D.I.C. and Ph.D. degrees from Imperial College of Science and Technology, London, U.K., in 1987.

In 1987–1990, he was a Lecturer with The University of Nottingham, Nottingham, U.K. In 1990, he joined the University of Technology, Sydney, Australia. In 1992, he was appointed Senior Lecturer at The University of Sydney, Sydney, where he became a Reader in 1995. He joined the City University of Hong Kong (CityU), Kowloon, Hong Kong, as a Professor in 1996 and was promoted to Chair Professor in 1998. In 2001–2004, he served as an Associate Dean of the Faculty of Science and Engineering, CityU. Since July 2011, he has been a Chair Professor with the University of Hong Kong and Imperial College London. He has published over 200 technical papers, including more than 150 refereed journal publications and book chapters. Over 50 of his patents have been adopted by the industry.

Dr. Hui is a Fellow of the Institution of Engineering and Technology (IET). He has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 2007. He was appointed twice as an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2004 and 2006. He served as one of the 18 Administrative Committee members of the IEEE Power Electronics Society and was the Chairman of its Constitution and Bylaws Committee from 2002 to 2010. He was the recipient of the Teaching Excellence Award at CityU in 1998 and the Earth Champion Award in 2008. He was also the recipient of an IEEE Best Paper Award from the IEEE Industry Applications Society Committee on Production and Applications of Light in 2002 and two IEEE Power Electronics Transactions Prize Paper Awards for his publication in wireless battery charging platform technology in 2009 and for his paper on LED system theory in 2010. His inventions underpin the key dimensions of the world's first wireless power standard "Qi" with free-positioning and localized charging features. In November 2010, he received the IEEE Rudolf Chope R&D Award from the IEEE Industrial Electronics Society and the IET Achievement Medal (The Crompton Medal) and was elected to the Fellowship of the Australian Academy of Technological Sciences and Engineering.

W. C. Ho (M'86) received the B.E.Sc. degree in electrical engineering and the B.Sc. degree in applied mathematics from The University of Western Ontario, London, ON, Canada, in 1986, the Ph.D. degree in electrical engineering from The University of Hong Kong, Pokfulam, Hong Kong, in 1997, and the M.B.A. degree from The University of Newcastle, Callaghan, Australia, in 2003.

He is currently a Technical Staff member with Traxon Technologies Ltd., Shatin, Hong Kong.

Xun Liu (M'07) was born in China in 1978. He received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2001 and 2003, respectively, and the Ph.D. degree from the City University of Hong Kong, Kowloon, Hong Kong, in 2007.

He is currently the Chief Technology Officer of ConvenientPower HK Ltd., Shatin, Hong Kong, and responsible for the R&D of a new generation of universal wireless charging platforms for a wide range of consumer electronic products. He is the coholder of several patents on wireless power transfer. His main research interests include planar integration in power electronics, applied superconductivity, and electromagnetic compatibility/electromagnetic interference.