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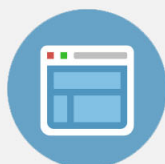
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Nitrided SrTiO₃ as charge-trapping layer for nonvolatile memory applications

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Charge-trapping characteristics of SrTiO₃ with and without nitrogen incorporation were investigated based on Al/Al₂O₃/SrTiO₃/SiO₂/Si (MONOS) capacitors. A Ti-silicate interlayer at the SrTiO₃/SiO₂ interface was confirmed by x-ray photoelectron spectroscopy and transmission electron microscopy. Compared with the MONOS capacitor with SrTiO₃ as charge-trapping layer (CTL), the one with nitrided SrTiO₃ showed a larger memory window (8.4 V at ± 10 V sweeping voltage), higher P/E speeds (1.8 V at 1 ms +8 V) and better retention properties (charge loss of 38% after 10⁴ s), due to the nitrided SrTiO₃ film exhibiting higher dielectric constant, higher deep-level traps induced by nitrogen incorporation, and suppressed formation of Ti silicate between the CTL and SiO₂ by nitrogen passivation. © 2011 American Institute of Physics. [doi:10.1063/1.3601473]

Charge-trapping nonvolatile (CTN) memories with discrete traps in dielectric for charge storage are regarded as a promising candidate for next-generation nonvolatile memories, due to their lower power consumption, higher reliability, and stronger scaling ability than their floating-gate counterparts. Si₃N₄ is the first dielectric used as the charge-trapping layer (CTL). Recently, extensive researches have been performed to study high-*k* dielectrics instead of Si₃N₄ as CTL for further scaling down of the memory dimensions and improving its charge-trapping efficiency, e.g., Y₂O₃ (*k* ~ 18),¹ HfON (*k* ~ 22),² Pr₂O₃ (*k* ~ 15),³ Nd₂O₃ (*k* ~ 16),³ Er₂O₃ (*k* ~ 13),³ ZrO₂ (*k* ~ 37),⁴ and Ta₂O₅ (*k* ~ 22).^{5,6} Unfortunately, few dielectrics proposed as CTL show a dielectric constant beyond 30. Moreover, an unavoidable low-*k* interlayer (e.g., silicate) formed between the high-*k* dielectric and SiO₂ may further reduce the *k* value. Among various high-*k* dielectrics, SrTiO₃ is well-known for its high dielectric constant (*k* > 140) and zero band-offset (ΔE_c) with respect to silicon, both of which are desirable as CTL for CTN memories to improve the program/erase (P/E) speeds and retention property.⁶⁻⁸ However, there have been few reports focusing on SrTiO₃ as CTL for nonvolatile memory applications. Furthermore, nitrogen incorporation also plays an important role in the characteristics of SrTiO₃ because it may induce more traps in the band gap through substitution of oxygen by nitrogen.^{9,10} In addition, the nitrogen incorporation can improve thermal stability and suppress elemental interdiffusion.⁶ Therefore, based on MONOS capacitors, this work aims to study the charge-trapping characteristics of nitrided SrTiO₃ by comparison with SrTiO₃.

MONOS capacitors with Al/Al₂O₃/SrTiO₃/SiO₂/Si were fabricated on p-type silicon substrate. After a standard RCA cleaning, 2 nm SiO₂ was grown on the wafers by thermal dry oxidation. Then, 3 nm SrTiO₃ was deposited on the SiO₂ by reactive sputtering using a SrTiO₃ target in a mixed Ar/N₂ (4/1) or Ar/O₂ (4/1) ambient, and the corresponding MONOS capacitors were denoted as NSTO-1 and STO-1,

respectively. Following that, 10 nm Al₂O₃ was deposited by *in situ* sputtering using an Al₂O₃ target as the blocking layer. Finally, Al was evaporated and patterned as gate electrode, followed by forming-gas annealing at 300 °C for 20 min. Al/SrTiO₃/SiO₂/Si (MNOS) capacitors with and without nitrogen incorporation were also fabricated with the same process, denoted as NSTO-2 and STO-2, respectively. The thickness of the dielectrics was determined by transmission electron microscopy (TEM). The film composition and chemical bonding states were analyzed by x-ray photoelectron spectroscopy (XPS). The electrical characteristics were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

The atomic content of nitrogen in the NSTO-2 sample is determined to be 8.0% from the XPS analysis shown in the inset of Fig. 1(a). Figure 1(a) shows the Ti 2*p* spectrum and the curve-fitting lines of the NSTO-2 and STO-2 samples. Both of the two samples possess similar spectrum. For the STO-2 sample, The Ti 2*p* spectrum shows two strong peaks located at 465.3 eV (Ti 2*p*_{1/2}) and 459.5 eV (Ti 2*p*_{3/2}), re-

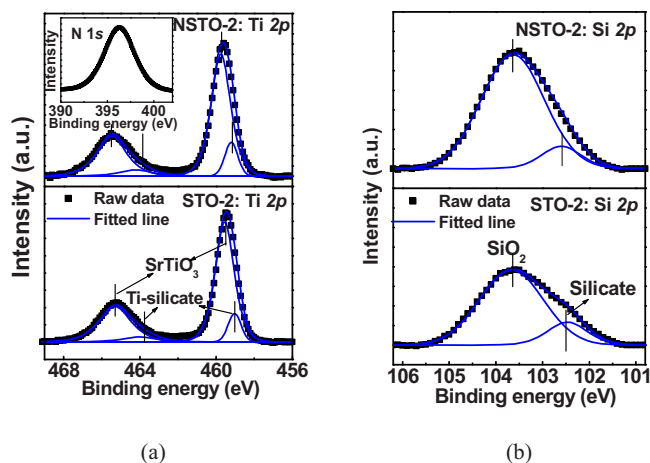


FIG. 1. (Color online) XPS spectra of the NSTO-2 and STO-2 samples: (a) Ti 2*p* and (b) Si 2*p*. The inset of (a) shows the N 1*s* spectrum of the NSTO-2 sample.

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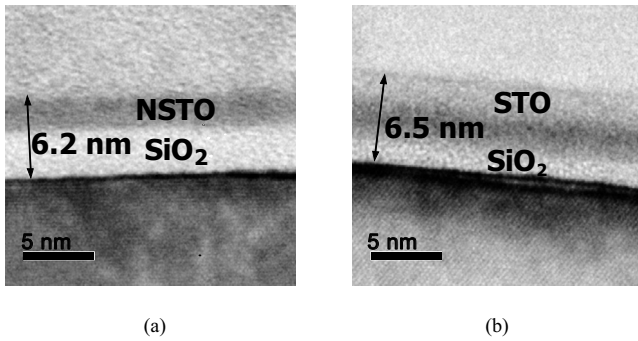


FIG. 2. TEM cross-sectional image of (a) the NSTO-2 sample and (b) the STO-2 sample.

spectively. These two peaks are in accordance with the Ti component in SrTiO₃ (465.4 eV for Ti 2p_{1/2}, 459.5 eV for Ti 2p_{3/2}).¹⁰ Furthermore, two extra peaks are also observed at 464 eV (Ti 2p_{1/2}) and 459 eV (Ti 2p_{3/2}), which agree with the values for Ti silicate (464 eV for Ti 2p_{1/2}, 458.8 eV for Ti 2p_{3/2}).¹¹ The presence of Ti silicate can further be confirmed by the Si 2p spectrum shown in Fig. 1(b), where the Si 2p spectrum in the STO-2 sample exhibits two peaks, corresponding to Ti silicate (102.3 eV) and SiO₂ (103.6 eV), respectively.^{11,12} Compared with the STO-2 sample, the Ti spectrum of the NSTO-2 sample displays a chemical shift of 0.2 eV to higher binding energy due to nitrogen incorporation. It is noted that the area ratio of Si component corresponding to SiO₂ and silicate is 8 for the NSTO-2 sample, which is larger than the value (~5) for the STO-2 one, indicating the formation of thinner Ti silicate in the NSTO-2 sample. Figure 2 shows the cross-sectional TEM image for the NSTO-2 and STO-2 samples. Compared with the NSTO-2 sample, an obvious interlayer is observed in the STO-2 sample. Including the quantum mechanical effect, the equivalent oxide thickness is calculated to be 3.34 and 3.45 nm for the NSTO-2 and STO-2 samples. The dielectric constant of SrTiO₃ with and without nitrogen incorporation is evaluated to be 36.7 and 30.3, respectively. Both of the *k* values are far below the reported value of SrTiO₃ (*k* > 140), mainly due to the formation of low-*k* Ti silicate between CTL and SiO₂.¹² The nitrated SrTiO₃ film shows higher dielectric constant than the SrTiO₃ film due to its thinner interlayer resulting from the nitrogen passivation.

Figure 3 exhibits the 1 MHz C-V hysteresis characteristics of the NSTO-1 and STO-1 samples under various sweeping voltages. As the sweeping voltage increases from ±6 to ±10 V, the memory window increases from 4.6 V/3.6 V to 8.4 V/6.0 V for the NSTO-1 and STO-1 samples, respectively. Compared with the STO-1 sample, the NSTO-1 one

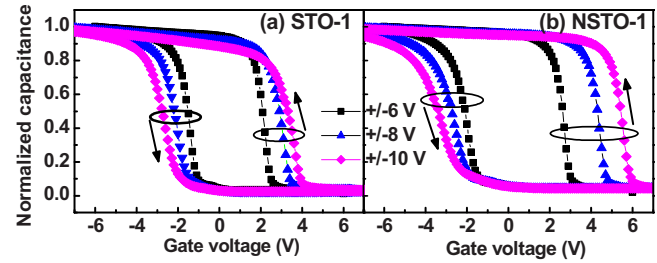


FIG. 3. (Color online) C-V hysteresis curve of the MONOS capacitors under various sweeping voltages: (a) without and (b) with nitrogen incorporation.

shows a larger memory window, which is attributed to its higher dielectric constant and higher trap density resulted from nitrogen incorporation.

Figure 4 shows the P/E transient characteristics of the NSTO-1 and STO-1 samples at various voltages. For the STO-1 sample, it shows a V_{FB} shift of 0.91 V and 1.60 V at +8 V for 1 ms and 1 s, respectively. For comparison, a larger V_{FB} shift of 1.82 and 3.04 V can be obtained for the NSTO-1 sample under the same operating conditions. Moreover, the NSTO-1 sample still shows a V_{FB} shift of 1.48 V even at a small gate voltage of +6 V for 1 ms, further supporting its higher P/E speeds, due to its high trap density induced by nitrogen incorporation as well as high dielectric constant. The NSTO-1 sample with a thinner interlayer shows higher trap density than the STO-1 one, indicating the traps are mainly distributed in the charge-trapping film rather than the interlayer.

Figure 5(a) shows the endurance characteristics of the MONOS capacitors with ±8 V 1 ms pulse stress. For the NSTO-1 and STO-1 samples, the memory window after 10⁵ cycles is 2.13 V and 1.20 V, compared with the initial value of 2.07 V and 1.12 V, respectively, thus only a slight narrowing of memory window after stress for both samples. However, both P/E V_{FB} levels decrease with cycling, which is especially severe for the STO-1 sample. This suggests electron detrapping and/or hole trapping induced by repetitive P/E stress. The P/E transient characteristics of the STO sample before and after 10⁴-cycle P/E stress are also shown in Fig. 5(b). The erase characteristics with and without stress coincide well, indicating no extra hole trapping during endurance test. In contrast, the V_{FB} shift after stress is much smaller than that without stress under the program state, demonstrating electron detrapping due to stress-induced defects, which should be responsible for the degradation of the V_{FB} shift shown in Fig. 5(a). Furthermore, the I-V characteristics before and after a 10⁵-cycle P/E stress are studied. The STO-1 sample shows larger leakage (6.2 nA/cm² and

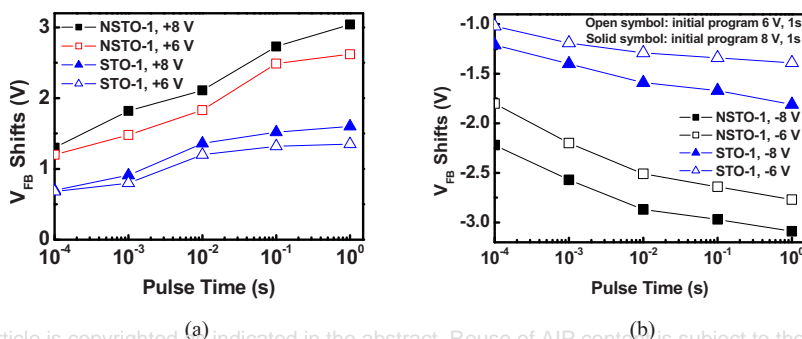


FIG. 4. (Color online) (a) Program and (b) erase transient characteristics of the MONOS capacitors. The erase characteristics are measured under an initial program state.

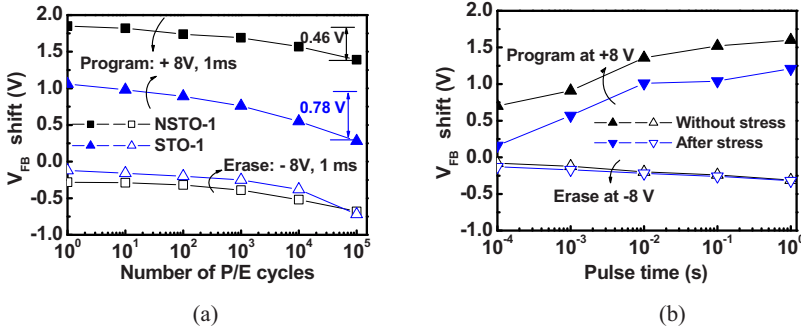


FIG. 5. (Color online) (a) Endurance characteristics of the MONOS capacitors under ± 8 V 1 ms pulse stress. (b) P/E transient characteristics of the STO-1 sample with and without P/E stress.

9.6 nA/cm² at $V_g=1.5$ V before and after stress, respectively) than the NSTO-1 one (6.0 nA/cm² and 6.4 nA/cm² correspondingly). Larger increase in current for the STO-1 sample indicates more stress-induced defects, which result in more severe degradation of the V_{FB} shift in Fig. 5(a). In addition, a slight over-erase phenomenon can also be observed in Fig. 5(b), which can be explained by some holelike traps existing in the CTL.

Figure 6(a) shows the retention characteristics tested at room temperature with an initial 1 s +8 V program state. The memory window after 10^4 s remains 62% and 49% for the NSTO-1 and STO-1 samples, respectively. The retained charge after 10 years is evaluated to be 27% for the NSTO-1 sample while that of the STO-1 sample is fully closed after 2×10^7 s (0.6 year). The charge loss through the tunneling layer and blocking layer is responsible for the degradation of the memory window during retention period. The formation of the interlayer consumes SiO₂. Furthermore, the Ti-rich silicate shows much smaller barrier height ($E_g \sim 3.5$ eV) than SiO₂ ($E_g \sim 9.0$ eV), which can enhance charge loss during the retention period.^{6,13} The charge-loss mechanism due to the interlayer can further be illustrated by the band diagram shown in Fig. 6(b). The electron-tunneling path from

SrTiO₃ to Si is reduced due to the Ti silicate, thus leading to severer charge loss. Consequently, a thinner Ti silicate between the CTL and SiO₂ in the NSTO-1 sample contributes to the better retention property as mentioned above. Moreover, the deep traps induced by nitrogen incorporation should be also desirable for the better retention property.²

In summary, the charge-trapping characteristics of SrTiO₃ with and without nitrogen incorporation are investigated based on MONOS capacitors. The MONOS capacitor with nitrided SrTiO₃ as CTL shows larger memory window, higher P/E speeds and better retention properties than the sample with SrTiO₃ as CTL because the nitrided SrTiO₃ film exhibits high dielectric constant, large quantity of traps induced by nitrogen incorporation, and suppressed interlayer by nitrogen passivation. Therefore, the nitrided SrTiO₃ film is demonstrated to be a promising CTL for high-density non-volatile memory applications.

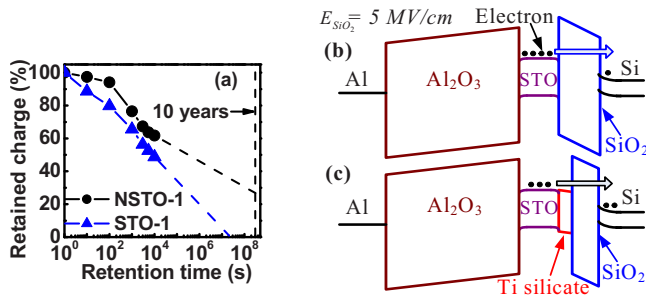


FIG. 6. (Color online) (a) Retention characteristics of the MONOS capacitors measured at room temperature. (b) Band diagram of the MONOS capacitor with no interlayer between SrTiO₃ and SiO₂ (Al₂O₃/SrTiO₃/SiO₂=10 nm/3 nm/3 nm). (c) Band diagram with an interlayer between SrTiO₃ and SiO₂ (Al₂O₃/SrTiO₃/Ti silicate/SiO₂=10 nm/3 nm/1 nm/2 nm).

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