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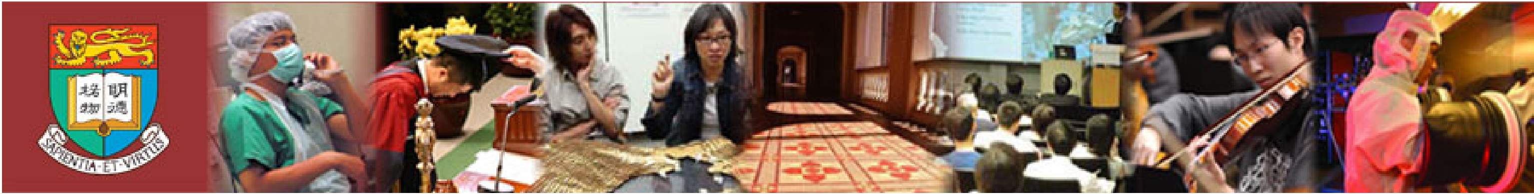

Title	A novel MONOS memory with high-κ HfLaON as charge-storage layer
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A Novel MONOS Memory With High-κ HfLaON as Charge-Storage Layer

L. Liu, J. P. Xu, F. Ji, X. D. Huang, and P. T. Lai

***Abstract*—MIS capacitors with a high-κ HfLaON or HfLaO gate dielectric are fabricated by using a reactive sputtering method to investigate the applicability of the films as a novel charge-storage layer in a metal–oxide–nitride–oxide–silicon nonvolatile memory device. Experimental results indicate that the MIS capacitor with a HfLaON gate dielectric exhibits a large memory window, high program/erase speed, excellent endurance property, and reasonable retention. The involved mechanisms for these promising characteristics with HfLaON are thought to be in part from nitrogen incorporation leading to higher density of traps with deeper levels and, thus, higher trapping efficiency, stronger Hf–N and La–N bonds, and more stable atomic structure and HfLaON–SiO_2 interface, as compared to the HfLaO dielectric.**

***Index Terms*—Charge-storage layer (CSL), endurance, HfLaON, metal–oxide–nitride–oxide–silicon (MONOS) memory, program/erase (P/E) characteristics.**

I. Introduction

According to the International Technology Roadmap for Semiconductors, the metal–oxide–nitride–oxide–silicon (MONOS) memory devices with the mechanism of charge trapping have been proposed as a potential candidate for replacing the conventional floating-gate nonvolatile memory devices, which will face serious challenges upon further scaling down [1]. In order to achieve a large memory window, fast program/erase (P/E) at low operating voltage, and good data retention simultaneously, extensive researches have been performed, involving the gate electrode [2], blocking layer [3], and tunneling layer [4] as well as the charge-storage layer (CSL) [5]–[7] of the device. Among them, the CSL is believed to be a critically important part of MONOS nonvolatile memory and has become a hot research topic. Some high-κ dielectric materials, e.g., HfO_2 [5], HfAlO [6], and La_2O_3 [7], have been proposed to replace Si_3N_4 as the CSL of the SONOS (MONOS)-type flash memories for better charge-storage capability. The larger conduction-band offset of HfO_2 [8] is expected to result in better retention compared to smaller offset dielectrics [5]. However, preexisting traps in HfO_2-based dielectrics not only contribute to P/E functions but also are the cause of VT instability, mobility, and reliability degradations [9]. The high hygroscopy of La_2O_3 is a challenge for its integration with the CMOS technology and also is a likely cause of reliability degradation. It was reported that some high-κ dielectrics (e.g., HfO_2 and HfSiO) that incorporated La could be used for high-performance CMOS technology to enhance digital and analog performances as well as reliability characteristics [9]. On the other hand, it is generally accepted that heavy nitridation induces a high density of electron traps with large capture cross section [10], and N incorporation in HfO_2 results in beneficial characteristics, including excellent resistance to interdiffusion of elements between different layers, higher dielectric strength [11], and enhanced immunity to damages induced by high-field stress [12]. In view of the aforementioned two points, it is hoped that better charge-trapping properties and dielectric performances could be achieved by simultaneously incorporating La and N into the HfO2 thin film. Therefore, in this paper, a capacitor with a HfLaON gate dielectric is fabricated, and its memory characteristics are carefully examined through comparison with another MIS capacitor with a HfLaO gate dielectric. It is found that a large memory window, high P/E speed, and reasonable retention characteristics can be obtained when HfLaON is used as the CSL.

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II. Experiment Details

MIS capacitors with a HfLaON or HfLaO high-κ dielectric were fabricated on a (100)-oriented p-type Si wafer with a resistivity of $5-10\ \Omega \cdot \mathrm{cm}$. After RCA cleaning, the wafers were put in diluted HF for 1 min to remove the native SiO_2. First, 3-nm SiO_2 was thermally grown at 900 °C in dry O_2, and then, the wafers were immediately transferred to the high-κ deposition vacuum chamber (Vacuum Discovery Deposition System made by DENTON Corporation). A nominal 15-nm HfLaON film was deposited by the reactive sputtering of a HfLa target (at a power of 24 W) in an $Ar : O_2 : N_2$ (24 : 3 : 6) ambient at room temperature. A postdeposition annealing was carried out in N_2 at 400 °C for 120 s. Al was evaporated to form the gate electrode by lithography with an area of $7.85 \times 10^{-5}\ \mathrm{cm}^{-2}$ and also evaporated on the wafer back side for the bottom electrode. Finally, metal annealing was completed in H_2/N_2 forming gas (5% H_2) at 300 °C for 20 min. For comparison, a nominal 15-nm HfLaO film was prepared by the reactive sputtering of a HfLa target in an $Ar : O_2$ (24 : 6) ambient, with other processing conditions being the same.

For evaluating the P/E characteristics and memory window of the devices, high-frequency (1-MHz) C–V curves were

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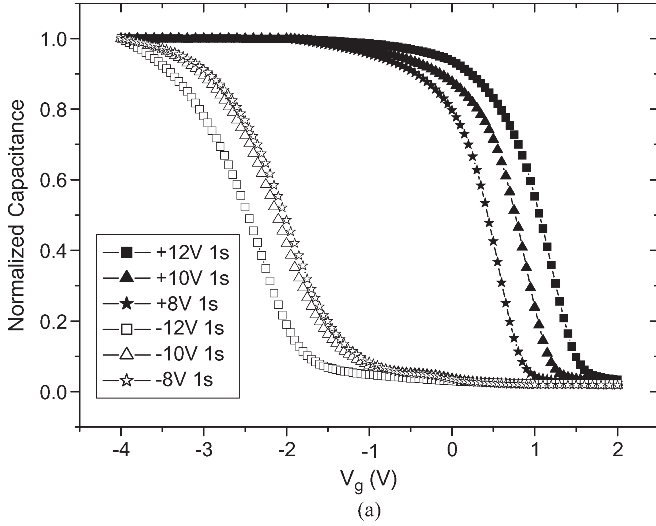
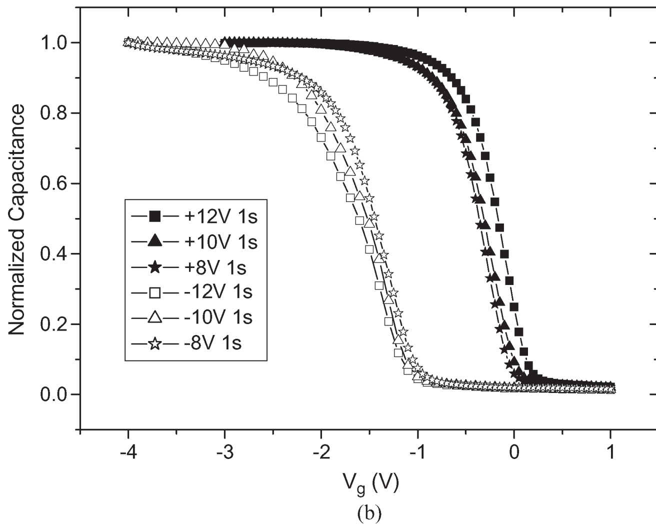
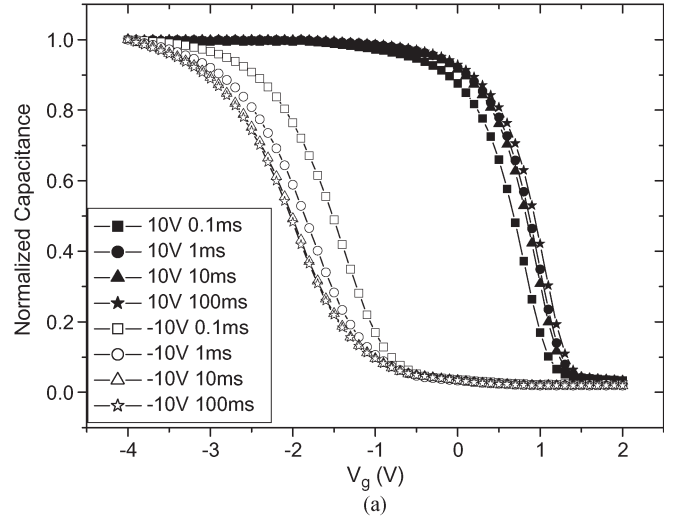


(a)

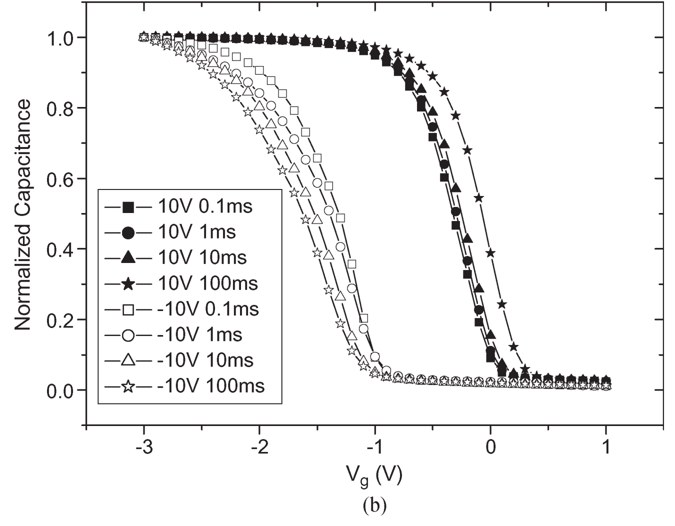


(b)

Fig. 1. C–V curves of the (a) HfLaON capacitor and (b) HfLaO capacitor at different P/E voltages for 1 ms. A similar P/E function to nonvolatile memory is demonstrated in the two devices.



(a)



(b)

Fig. 2. C–V characteristics of (a) HfLaON capacitor and (b) HfLaO capacitor after applying $+/-10$ V voltages for different times. For HfLaON capacitor, the close V_{fb} change for different P/E times indicates the fast switching time.

measured at room temperature using an HP4284A precision LCR meter, from which the flat-band voltage was extracted by assuming $C_{\mathrm{fb}}/C_{\mathrm{ox}} = 0.5$ (C_{fb} and C_{ox} are the flat-band and oxide (or accumulation) capacitances, respectively). Operating voltages were supplied by an HP4156A precision semiconductor parameter analyzer. All measurements were carried out under a light-tight and electrically shielded condition.

III. Results and Discussion

For determining the shift of the flat-band voltage, the normalized C–V curves are measured. The capacitance in accumulation is 43 and 36 pF for the HfLaON and HfLaO MIS devices, respectively.

Fig. 1(a) and (b) shows the C–V characteristics of the HfLaON and HfLaO high-κ gate-dielectric MIS capacitors, respectively, after applying different P/E voltages for 1 s by an HP4156A analyzer. The shift of the flat-band voltage (ΔV_{fb}) is extracted from the measured C–V curves under different P/E voltages, and the memory window is determined from the positive and negative shifts of the flat-band voltage. As can be seen from Fig. 1, the memory window of the HfLaON capacitor at P/E voltages of ± 8 V, ± 10 V, and ± 12 V is 2.50, 3.15, and 3.25 V, respectively, and becomes 1.05, 1.30, and 1.40 V under the same P/E voltages for the HfLaO capacitor. The larger memory window for HfLaON compared to HfLaO, even at lower P/E voltages for the HfLaON, indicates that HfLaON has a higher trapping capability as a CSL and can be more effectively programmed and erased. This could be ascribed to nitridation-induced trap generation [10] so that total trap density in HfLaON is higher than that in HfLaO, which is supported by a large C–V hysteresis (0.50 V) when measuring the HF C–V curve of the fresh HfLaON sample under dark conditions, swept in both directions (the hysteresis is only 0.20 V for the HfLaO sample), implying a large quantity of deep-level traps in HfLaON.

The P/E performances are evaluated in terms of the flat-band-voltage change (ΔV_{fb}) by applying a P/E voltage of $+/-$ 10 V for 0.1 to 100 ms. As shown in Fig. 2(a), for the HfLaON capacitor, a large $+\Delta V_{\mathrm{fb}}/-\Delta V_{\mathrm{fb}}$ is observed when the P/E time reaches 0.1 ms/1 ms, and then, $+\Delta V_{\mathrm{fb}}/-\Delta V_{\mathrm{fb}}$ gradually saturates from 0.1 ms/1 ms to 100 ms, respectively, suggesting

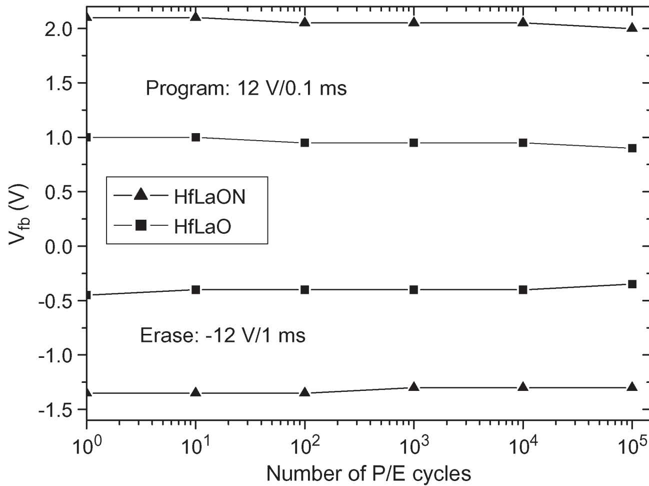


Fig. 3. Endurance of the two capacitors. The P/E of each cycle is performed at $+/-12$ V for 100 μs/1 ms, respectively.

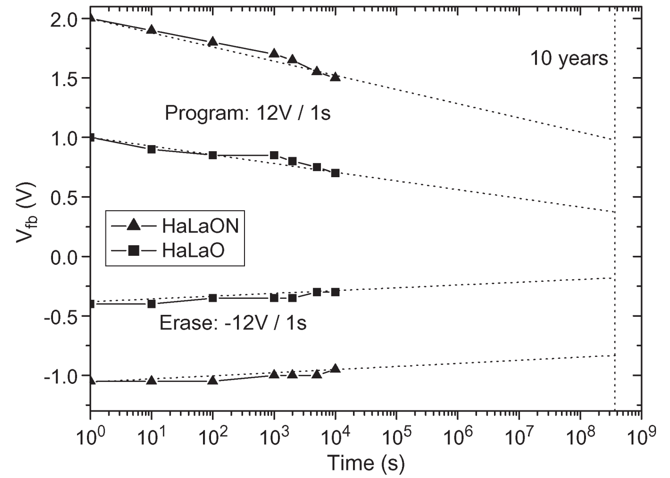


Fig. 4. Retention characteristics of the two capacitors after removing 1-ms P/E voltages at $+/-12$ V.

a P/E time of $\sim$0.1 ms/1 ms at an operating voltage of $\pm$10 V. The rapid saturation of ΔV_{fb} in short P/E time indicates faster switching for the HfLaON sample than the HfLaO sample. This is because the incorporation of N atoms can effectively increase the permittivity of the dielectric, as calculated to be 17.6 and 12.9 for HfLaON and HfLaO, respectively, from the formula of $\varepsilon_{\mathrm{ox}} = \varepsilon_{\mathrm{SiO2}} \times t_{\mathrm{ox}}/CET = t_{\mathrm{ox}}/(t_{\mathrm{SiO2}}/\varepsilon_{\mathrm{SiO2}} + t_{\mathrm{die}}/\varepsilon_{\mathrm{die}})$, where CET is the capacitance equivalent thickness; t_{SiO2}, $\varepsilon_{\mathrm{SiO2}}$, t_{die}, and $\varepsilon_{\mathrm{die}}$ are the physical thickness and relative permittivity of the SiO_2 and high-κ dielectric layers. The high permittivity can decrease the equivalent oxide thickness [13] ($CET =$ 6.3 and 7.5 nm for HfLaON and HfLaO, respectively). When the gate voltage is applied, a higher electric field (E) will be built across the SiO_2 ($E \propto$ permittivity^{-1} for the plate capacitor), leading to a larger energy-band bending and thus enhancing carrier injection from the substrate to the HfLaON film (CSL) or from the HfLaON film to the substrate. Also, the high operating speed is associated with the high trapping efficiency of HfLaON.

Fig. 3 shows the endurance properties of the two capacitors. The memory window remains almost unchanged for both capacitors after 10^5 cycles, and no closing or overprogramming phenomenon is observed. The incorporation of La into HfO_2 has been shown to improve the electrical and reliability performances through modifying its interface and bulk dielectric characteristics [14], and this, in part, may be why both the HfLaON and HfLaO capacitors exhibit good endurance characteristics. In addition, since the incorporation of N atoms into HfLaO can improve its memory window, the high-κ HfLaON dielectric is preferred over HfLaO as the CSL in the memory devices of the charge-trapping type.

Data retention is one of the most important characteristics for nonvolatile memory applications. Here, the room-temperature retention characteristic is examined by measuring the C–V curves and extracting the V_{fb} change after removing the P/E voltage at successive times from 1 to 10 000 s. Fig. 4 shows the V_{fb} variation with time after programming or erasing at $+12$ V or -12 V, respectively, for 1 ms. An extrapolated ten-year memory window of 2.00 or 0.60 V is obtained for the HfLaON capacitor (initial memory window of 3.05 V) or the HfLaO capacitor (initial memory window of 1.40 V), respectively. The loss of the memory window after ten years is 34% for the former and 57% for the latter. The improved retention characteristic of the HfLaON film could be due to the formation of strong La–N and Hf–N bonds. Also, an expected high density of traps with deeper energy levels in HfLaON may be responsible for the improved retention. In addition, the N incorporation near the HfLaON–SiO_2 interface could effectively block the diffusion of Si and O atoms [15] and give a stable HfLaON–SiO_2 interface, thus reducing the leakage current and enhancing the retention property. It is expected that, if suitable blocking and tunneling layers are prepared, a better retention property could be obtained for the case of HfLaON as the CSL.

IV. Conclusion

Experimental results indicate that high-κ HfLaON has potential for use as a CSL for MONOS devices. The MIS capacitor with a HfLaON gate dielectric exhibits programmable and erasable characteristics with a large memory window, high P/E speed, excellent endurance property, and reasonable data retention. The improved memory characteristics for HfLaON compared to HfLaO are attributed to an expected higher density of traps with deeper levels due to nitrogen addition and, thus, to higher trapping efficiency, stronger Hf–N and La–N bonds, and a more stable HfLaON–SiO_2 interface. Also, the HfLaON film has higher crystallization temperature and improved structural stability for integration with the current CMOS technology. Therefore, it is a potential candidate as the CSL of MONOS nonvolatile memory devices.

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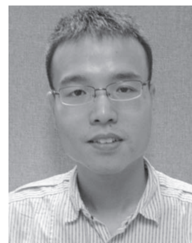

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