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Vertically Mounted InGaN-on-Sapphire Light-Emitting Diodes

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***Abstract*—An InGaN/GaN light-emitting diode (LED) chip mounted in a vertical configuration (vmLED) is demonstrated, exhibiting significant enhancement to light extraction, compared with a LED mounted in a conventional planar geometry. By flipping the chip orthogonally, two large illumination surfaces of the device are exposed for direct light extraction. Comparisons, through ray-trace modeling and experiment data with conventional surface-mounted LEDs, indicate that the vmLEDs achieve superior light extraction efficiency. A sapphire-prism-mounted vmLED is further proposed to improve heat sinking, which is well suited for higher current operations.**

***Index Terms*—Light extraction, light-emitting diodes (LEDs), vertically mounted.**

I. Introduction

ALTHOUGH there are different ways of packaging GaN-based light-emitting diodes (LEDs), including surface, flip-chip [1], and chip-on-board mounting [2] among others, the chips are invariably mounted in a planar configuration, whereby one of the largest surfaces is adhered to the package. However, the typical cuboid LED chip possesses six surfaces for light extraction, including the large-area GaN and sapphire top and bottom surfaces, together with four smaller area sidewall facets. With the planar mounting configuration, either the large-area GaN or sapphire surface is bonded to the package. Although a mirror is typically coated onto this bonding surface, the reflected light has to pass through the multiquantum wells (MQWs) before reaching the opposite surface, suffering severe absorption losses along the optical path. To fully make use of the two large surfaces for light extraction, an alternative packaging strategy should be developed.

In this paper, a design involving vertical mounting of LED chips is proposed and demonstrated. Such vertically mounted LEDs (vmLEDs) can be realized by adhering one of four chip facets to the package, as illustrated in the schematic diagram of Fig. 1(a). As a result, two large parallel surfaces are exposed for direct light extraction, together with three other sidewall facets. With enlarged exposed surface areas, this design is expected to offer higher light extraction efficiency than a conventionally mounted planar LED, together with modified emission characteristics. Through optical ray-trace simulations and experimental verifications, the optical performances of the vmLEDs have been thoroughly evaluated.

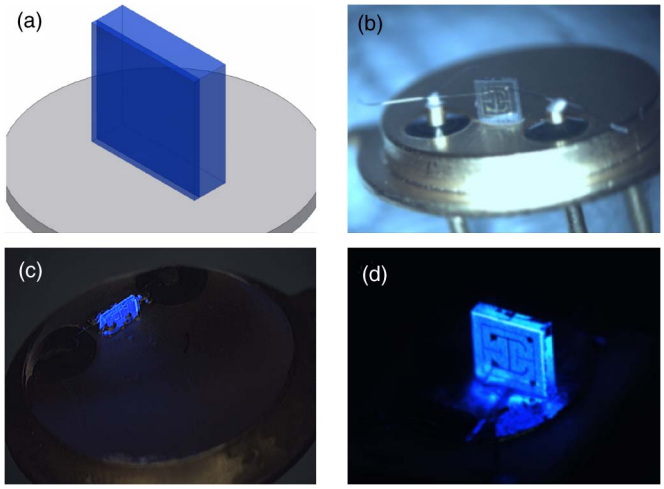

Fig. 1. (a) Schematic diagram of a vmLED. (b) Assembled vmLED on TO-package before encapsulation. (c) and (d) Two different views of an encapsulated vmLED biased at 10 mA.

Nevertheless, with a reduced contact area with the package, heat sinking of the vertically mounted chip might be compromised. Thermal dissipation of this bonding strategy is investigated through both thermal simulations and experimentally; an improved design involving a prism-mounted version of the vmLED is further proposed.

II. Experimental Details

The LED chips used in this work are fabricated on GaN-on-sapphire LED wafers with InGaN/GaN MQWs emitting with a center wavelength of about 470 nm. The devices are of square geometries (1 mm by 1 mm) fabricated by standard microfabrication processes, the details of which can be found in references such as [3]. The chips are diced and separated via ultraviolet laser micromachining [4]. The die and wire bonding steps differ from the packaging of conventional planar LEDs. With the LED chip temporarily mounted horizontally, Al bonding wires (50 μm diameter) are attached to the n- and p-bonding pads with an ultrasonic wedge wire bonder (ASM AB520). After bonding of the two wires, the chip was vertically mounted onto a TO-can package by attaching one of the sapphire sidewalls using thermally conductive epoxy. Subsequently, the loose ends of the two Al bonding wires are connected to the pins of the TO-package using silver epoxy to establish electrical conductivity, as illustrated in the microphotograph of Fig. 1(b). The device is subsequently encapsulated with a silicon resin

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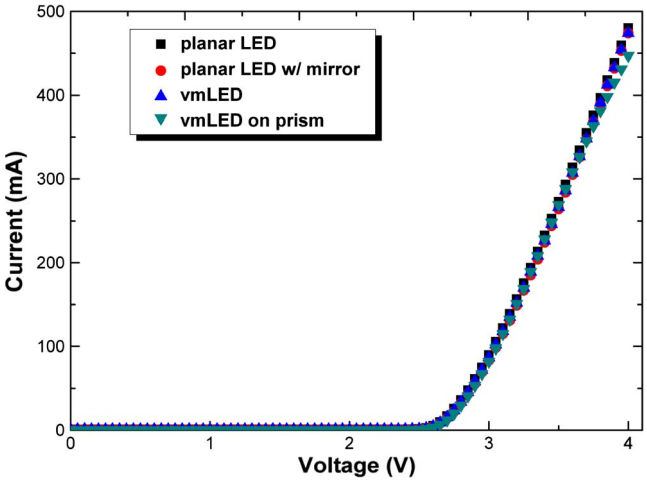

Fig. 2. Measured I–V characteristics of the devices.

(Dow Corning OE-6630), completing the vertical-mounting arrangement. The encapsulated vmLED biased at a low current is shown in Fig. 1(c) and (d). For reference, two conventional planar LEDs are prepared: one with an Al mirror-coated sapphire surface and the other without. The measured I–V characteristics of the devices are plotted in Fig. 2, which indicates that the vertically mounted configuration has negligible influence on the electric properties of the device.

III. Results and Discussions

A. Optical Characterization of the vmLED

The optical properties of the vmLEDs were evaluated comprehensively and compared with the two planar LEDs. The angular emission patterns of the devices (biased at 20 mA) were obtained by rotating a fiber coupled to an optical spectrometer about the central axis of the chips from -90° to 90°, in steps of 1°. The integrated intensity at each individual angle was plotted to form a polar diagram, as shown in Fig. 3(a). The simulated emission profiles obtained by ray tracing are plotted in Fig. 3(b) for comparison. In the simulation, the LED was modeled to consist of four layers: p-GaN, MQW, n-GaN, and sapphire substrate; the metal pads were not included to simplify the model. 50 000 light rays were set to emit from the MQWs with uniform angular distribution, traveling through the optical materials and across interfaces obeying Snell's law. The extracted light rays were detected by a spherical collection plane surrounding the LED chip. As observed in Fig. 3(a) and (b), the simulated plot is highly consistent with the experimental data. Chips mounted in a planar configuration emit with a near-Lambertian distribution as expected. In contrast, the radiation pattern of vmLED is split into two distinct emission cones on either side of the vertical axis. The enhancement of light emission occurs mainly at angles between 15° and 45° with respect to the normal, corresponding to emission from the two large vertical illumination surfaces of the vmLED. The slight nonsymmetrical pattern can be attributed to the dissimilar material (and thus refractive index) on either side of the chip (GaN and sapphire). The vmLED emits with a wide divergence,

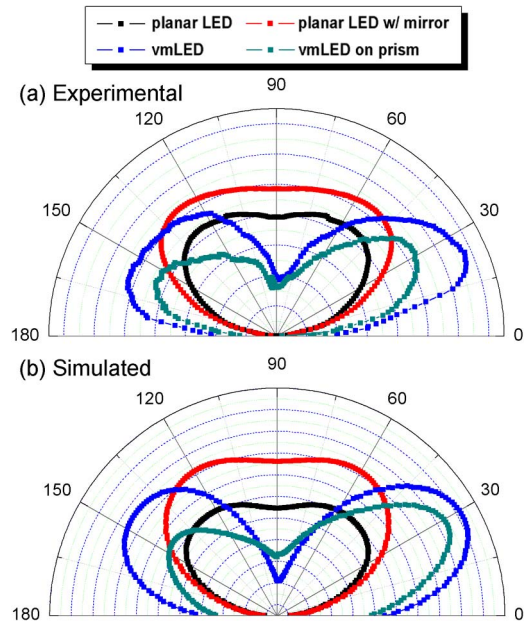

Fig. 3. (a) Experimentally measured radiation patterns of the devices. (b) Ray-trace-simulated radiation patterns of the devices.

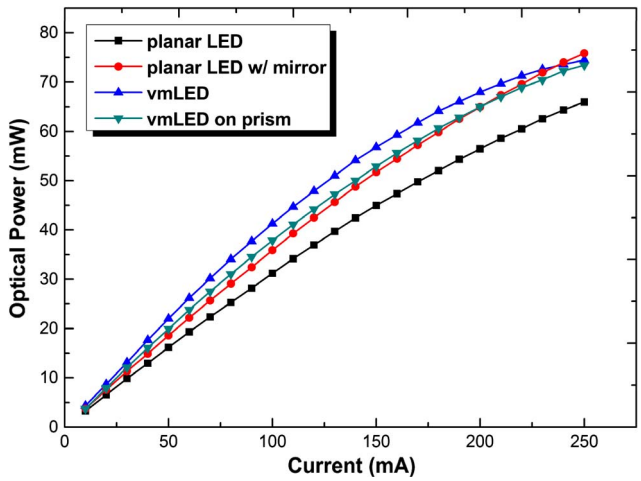

Fig. 4. L–I curve comparing the performances of the devices.

making it suitable for general lighting applications, whereby diffused light sources are generally desirable, as opposed to a directional source [5].

In addition, the light extraction efficiencies as determined by ray-trace simulations of the vmLED, mirror-coated planar LED mirror, and planar LED are 16.9%, 14.5%, and 11.9%, respectively. Based on this simulation result, the vmLED offers an overall increase in light extraction efficiency of 16.55% and 42%, compared with the other two planar LEDs.

The total output powers of the devices were measured by placing the devices within a 2-in integrating sphere, which is fiber coupled to a calibrated optical spectrometer. Fig. 4 shows the light output-current (L–I) plots for the LEDs. At lower currents ($<$150 mA), the average light enhancement factors are 14% and 23% over the planar LEDs with and without a reflector, respectively. Such significant enhancements to light

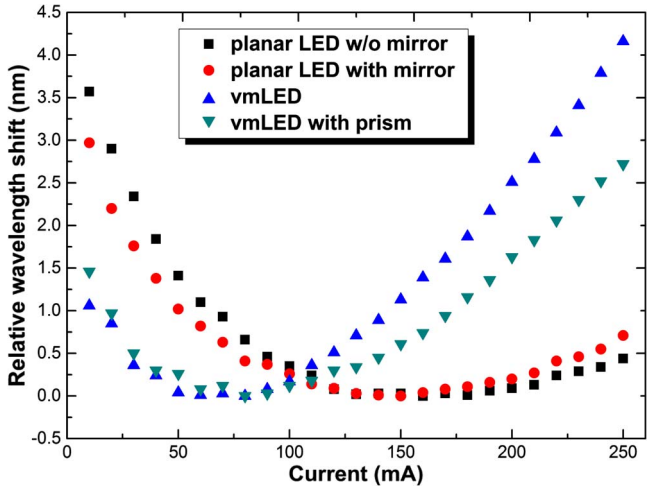

Fig. 5. Plot of peak wavelength shifts as a function of forward current of the devices.

TABLE I
MATERIAL PROPERTIES ADOPTED FOR THE THERMAL MODELING

	Material	Thermal conductivity (W/mK)
Die	Sapphire	40
Epoxy	Acrylic	5
TO-header	Copper	385

extraction highlight the effectiveness of erecting the chip onto the package, providing two large illumination surfaces. On the other hand, it is noted that the output powers begin to drop when the driving current exceeds 150 mA, which is attributed to joule heating. Among the three LEDs, the vmLED suffers the most severe drop in optical power. Setting the chip upright with a sapphire sidewall attached to the package reduces the contact area at the same time. Heat is dissipated from the chip to the package via this interface; a reduced thermal conductive area limits heat transfer, thereby increasing the junction temperature and suppressing the internal quantum efficiency, accounting for the nonlinearity of the output power at higher currents.

The thermal effect is further evaluated by measuring the emission central wavelength of the chips as a function of forward current (λ-I), as plotted in Fig. 5. It is known that, as the junction temperature increases, the emission wavelength of the device would be red-shifted [6]. From the plot, significant spectral red shift from the vmLED is observed at currents above 100 mA, with a maximum shift of 4.16 nm at 250 mA. On the other hand, although red shifts are also observed from the planar LEDs, the onset of spectral shift occurs at 150 nm with a maximum shift of 0.5 nm at 250 mA. The observations indicate that the vmLEDs are suitable for operation up to $\sim$150 mA to maintain efficiency.

The thermal performance of the devices was evaluated by Computational Fluid Dynamics simulation with specific material parameters listed in Table I. The ambient temperature was initially set to 30 °C, whereas a heat transfer coefficient of 5 W/m^{2}K was used for natural convection. The model involves a LED die with a dimension of 1 mm $\times$ 1 mm $\times$ 0.25 mm, which was set to dissipate generated heat of 0.25 W, mounted on a TO-header via a thin layer (0.01 mm) of thermally conductive epoxy. The volumetric heat generation within the active layer of a die is represented by an equivalent planar source located uniformly on the top surface of the die. In the simulation, the optical elements and the ambient were separated by coarse grids with local and dynamic rectangular mesh refinement. The heat distribution of the system, considering both conduction and convection, was evaluated using the finite volume method.

Fig. 6(a) and (b) illustrates the simulated temperature distributions across the die for the planar LED and vmLED, respectively. It is predicted that the maximum temperature attained by the vmLED (about 152 °C) is much higher than that of the planar LED (about 121 °C) because of the much reduced contact area for the vmLED. Therefore, without proper thermal design, the overheating issue can degrade the optical performance at higher currents, as shown in Fig. 4, eventually causing catastrophic failure [7].

B. Sapphire-Prism-Mounted vmLED

To improve heat sinking in the vmLED, a vmLED integrated with a block of sapphire microprism (acquired from Miller Optics), as shown in the 3-D schematic diagram of Fig. 7(a), is proposed. Sapphire is chosen as it is optically transparent with appreciable thermal conductivity. Based on dimensions of the sapphire prism, the contact area with the package of the modified device is 1.7 mm^2, which is almost six times that of the original vmLED. The enlarged thermally conductive area is expected to transmit heat more efficiently.

Initially, the chip was wire bonded as before. This is followed by liquid-capillary bonding of the chip to the sapphire prism [8], [9]. Due to surface tension of the solvent, intimate contact between the two sapphire surfaces can be achieved, eliminating the need for epoxy, which induces optical losses and thermal resistance. From our previous work, the minute gap of hundreds of nanometers between two bonding surfaces contribute to excellent optical coupling (assisted by optical tunneling via evanescent waves) [10], [11] and thermal conduction. Subsequently, the base of the prism was adhered to the package, as shown in the schematic diagram and the wires attached to the pins of package. The final packaged and illuminated device is shown in Fig. 7(b).

The performance of this modified device is evaluated and compared with that of the previous devices. Both the experimental and simulated emission patterns of the modified device plotted in Fig. 3(a) and (b) are similar as before, albeit with consistently reduced intensities. The simulated light extraction efficiency of the modified device decreases from 16.9% to 14.7% after integration with a prism. The light rays originally extracted from the vertical sapphire surface encounter additional total internal reflections at the inclined sapphire–air interface. Despite the shortcomings, the light extraction is still superior to the planar LEDs.

From the new set of L–I curves in Fig. 4, although the output power of the prism-mounted vmLED is reduced by $\sim$14%, compared with that of the original vmLED (but still higher than those of the planar LEDs), no apparent drop at higher currents

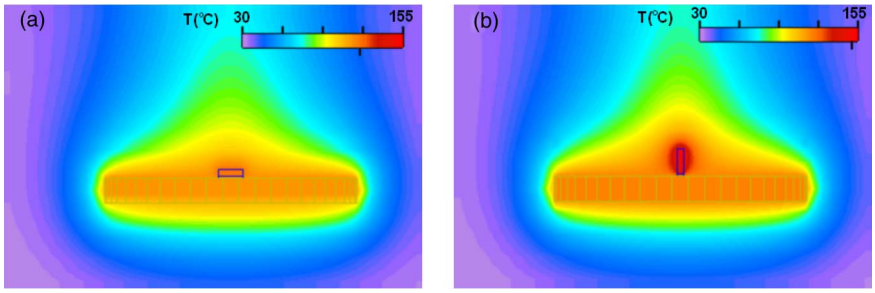

Fig. 6. Simulated heat distribution patterns across the (a) planar LED and (b) vmLED.

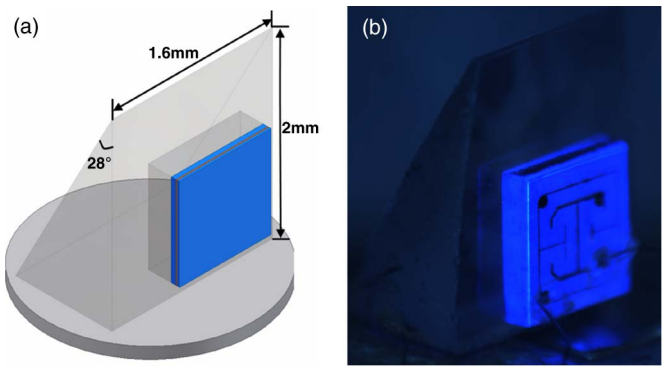

Fig. 7. (a) 3-D schematic diagram of the proposed sapphire-prism mounted vmLED and (b) illuminated device.

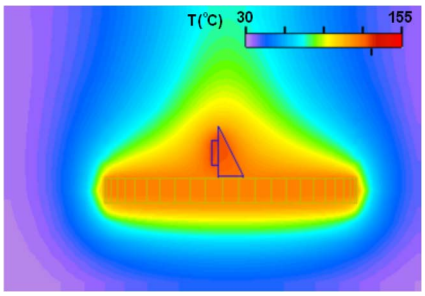

Fig. 8. Simulated heat distribution patterns of the prism-mounted vmLED.

is observed, testifying to improved heat sinking of the modified mounting configuration. Further evidence is provided by the new set λ-I plot in Fig. 5, whereby the rate of red shift of the modified device is reduced, compared to the original vmLED.

Thermal simulation was conducted for the modified mounting geometry shown in Fig. 8. The maximum temperature attained by the prism-mounted vmLED is much lower than that of the original configuration (129 °C versus 152 °C) and is similar to those of the planar LEDs. One can conclude that, by integration with a sapphire prism, the issue of thermal dissipation is alleviated, making the devices suitable for higher current operation.

IV. Conclusion

Employing a smart modification to the chip packaging scheme, our vmLEDs have been demonstrated to offer superior light extraction than conventionally packaged planar LEDs. By mounting the LED chip in a vertical configuration, two large illumination surfaces are exposed for light extraction. Reduced contact area with the package raises thermal concerns at higher driving currents. This can be alleviated through a modified mounting scheme, whereby the chip is vertically mounted onto a sapphire prism. Optical and thermal evaluations indicate desirable light extraction efficiency and improved thermal dissipation, providing a well-compromised solution for vertically mounting of LEDs.

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