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LaTiON/LaON as band-engineered charge-trapping layer for nonvolatile memory applications

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Abstract Charge-trapping characteristics of stacked LaTiON/LaON film were investigated based on Al/Al_2O_3/LaTiON-LaON/SiO_2/Si (band-engineered MONOS) capacitors. The physical properties of the high-k films were analyzed by X-ray diffraction, transmission electron microscopy and X-ray photoelectron spectroscopy. The band profile of this band-engineered MONOS device was characterized by investigating the current-conduction mechanism. By adopting stacked LaTiON/LaON film instead of LaON film as charge-trapping layer, improved electrical properties can be achieved in terms of larger memory window (5.4 V at ±10-V sweeping voltage), higher program speed with lower operating gate voltage (2.1 V at 100-μs +6 V), and smaller charge loss rate at 125 °C, mainly due to the variable tunneling path of charge carriers under program/erase and retention modes (realized by the band-engineered charge-trapping layer), high trap density of LaTiON, and large barrier height at LaTiON/SiO_2 (2.3 eV).

1 Introduction

Floating-gate nonvolatile memory devices are rapidly approaching the scaling limit mainly due to their difficulty in maintaining high gate coupling ratio and suppressing cross talk between neighboring cells. As a promising candidate, metal-oxide-nitride-oxide-silicon (MONOS)-type flash memories with discrete traps in the dielectrics for charge storage have attracted increasing interest because of their localized charge-storage and coupling-free properties. Si_3N_4 ($k \sim 7$) was the first dielectric used as the charge-trapping layer (CTL). Recently, extensive researches have been carried out to study high-k dielectrics instead of Si_3N_4 for further scaling down the device dimensions and improving its charge-trapping efficiency. Among various high-k dielectrics, rare-earth metal oxides, such as La_2O_3 ($k \sim 25$) [1], Gd_2O_3 ($k \sim 14$) [2, 3], Pr_2O_3 ($k \sim 15$) [4], Nd_2O_3 ($k \sim 16$) [4], Er_2O_3 ($k \sim 13$) [4], have received much interest as charge-trapping layer, mainly due to their relatively high dielectric constants, appropriate conduction-band offsets with respect to Si and good electrical properties [4, 5]. Moreover, nitrogen incorporated into the charge-trapping dielectrics has also been widely investigated to induce deep-level traps and enhance the reliability of the memory devices [6–8]. For a conventional MONOS memory device, it tends to have thinner tunneling oxide for higher program/erase (P/E) speeds and lower operating voltages, whereas a thinner tunneling oxide may deteriorate its retention property. Therefore, there is a trade-off between high P/E speeds and good retention property. A novel MONOS structure with band-engineered CTL (BE-MONOS) has been demonstrated to be an effective solution, which can enhance the tunneling of carriers during P/E operation, and suppress the charge loss under retention mode by modulating the tunneling path of carriers [9, 10]. In this work, we propose a novel BE-MONOS structure with stacked LaTiON/LaON film as CTL as shown in Fig. 1(a). It is worth mentioning that the Ti incorporation into the LaON film plays a key role in the formation of this kind of band-

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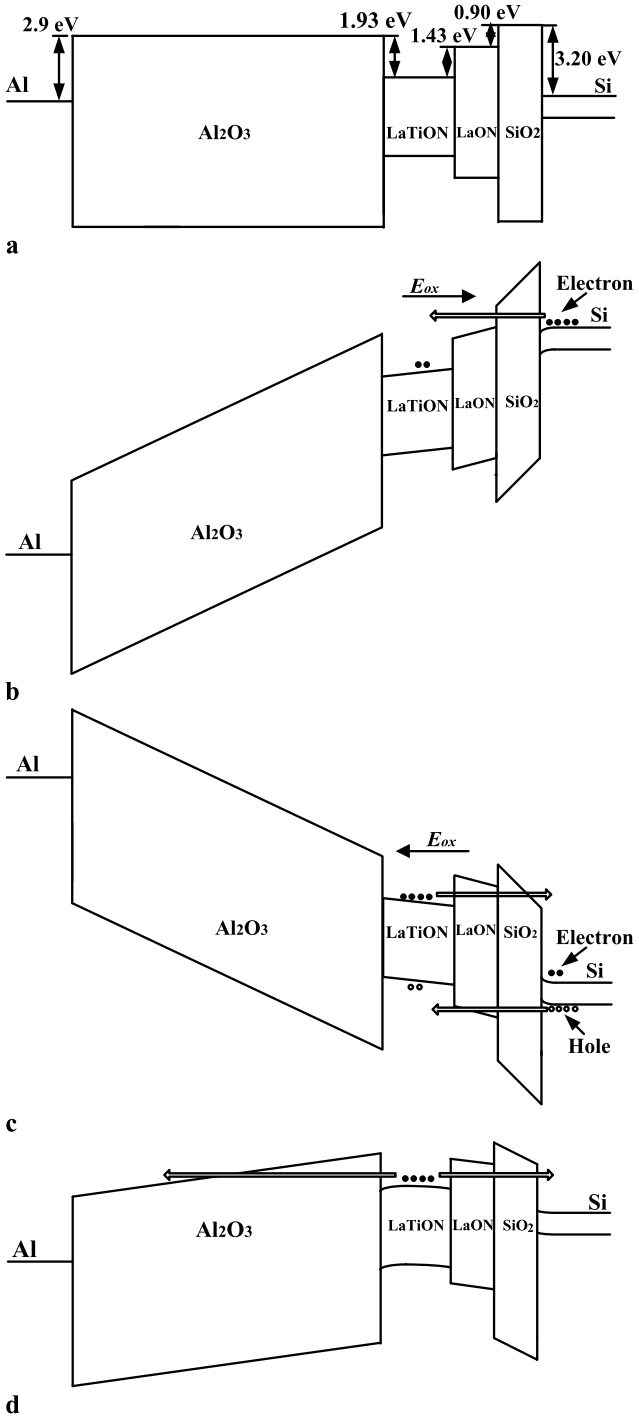

Fig. 1 Energy band diagram of the BE-MONOS capacitor: (**a**) under flat-band state; (**b**) under program state with an electric field across the tunneling oxide (E_{ox}) of 10 MV/cm; (**c**) under erase state with $E_{ox} = -10$ MV/cm; and (**d**) under retention state with $E_{ox} = 4$ MV/cm

engineered charge-trapping layer, which not only can increase the dielectric constant, but also shrink the band gap of the LaON film, thus resulting in a large band offset at the LaTiON/LaON interface [11, 12]. Compared with the BE-MONOS structure with Si_3N_4/HfON [9], this proposed structure with LaTiON/LaON has a higher dielectric constant, leading to higher P/E speeds. Furthermore, the stacked film can be formed by in-situ co-sputtering method, which simplifies the fabrication process [10].

2 Experiment

MONOS capacitor with an Al/Al_2O_3/LaTiON-LaON/SiO_2/Si structure was fabricated on p-type silicon substrate. After a standard RCA (Radio Corporation of America) cleaning [13], 2-nm SiO_2 was grown on the wafer by thermal dry oxidation. Then 2-nm LaON was deposited on the SiO_2 by reactive sputtering using a La_2O_3 target in a mixed Ar and N_2 ambient. Following that, 3-nm LaTiON was deposited in-situ by co-sputtering La_2O_3 and Ti targets in a mixed Ar and N_2 ambient, and the atomic ratio of Ti and La in the LaTiON film was determined to be 1.7 by XPS analysis. This chosen Ti/La ratio was to suppress the diffusion of Ti into the SiO_2 tunneling layer (which could deteriorate the data retention property), while maintaining the high dielectric constant and small band gap of the LaTiON film [14]. In addition, the nitrogen content in the LaTiON and LaON films was determined to be 3.3 % and 2.7 %, respectively, by XPS analysis. Then 14-nm Al_2O_3 as blocking layer was deposited by means of atomic layer deposition using trimethylaluminum ($Al(CH_3)_3$) and H_2O as precursors at 300 °C. Next, the samples went through a post-deposition annealing (PDA) in N_2 ambient at 850 °C for 30 s. Finally, Al was evaporated and patterned as gate electrode, followed by a forming-gas annealing at 300 °C for 20 min. A conventional MONOS capacitor with Al/Al_2O_3/LaON/SiO_2/Si was also fabricated for comparison. To investigate the physical and electrical characteristics of the high-*k* films, Al/(LaON, or LaTiON, or LaTiON/LaON)/SiO_2/Si(MNOS)-type capacitors were also fabricated by the same process mentioned above. The physical characteristics of the high-*k* dielectric films were characterized by X-ray diffraction (XRD), transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the memory capacitors were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

3 Results and discussion

Figure 2 shows the XRD patterns of the LaON and LaTiON/LaON films. For the stacked LaTiON/LaON film, no diffraction peaks are observed from the XRD spectrum, indicating the amorphous state of the stacked film. On the contrary, there is a peak located at $2\theta = 33.1°$ for the LaON film, suggesting its crystalline structure. This peak is in accordance with the (411) reflection of the cubic La_2O_3 phase

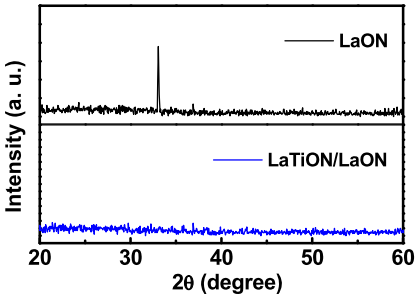

Fig. 2 XRD pattern of the LaON/SiO_2 and LaTiON/LaON/SiO_2 films on Si substrate

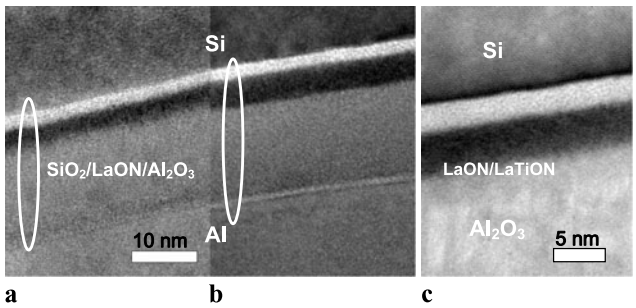

Fig. 3 (**a**) The conventional MONOS TEM cross-sectional image. (**b**) The BE-MONOS TEM cross-sectional image. (**c**) The BE-MONOS TEM cross-sectional image with a larger scale

($2\theta = 33.3°$). Ti incorporated into the LaON film can act as a network modifier and stabilize the amorphous state of the LaTiON film [15]. In addition, the thinner LaON film in the LaTiON/LaON stack (2 nm versus 4 nm for the sample with single LaON layer) usually needs a higher crystallization temperature for grain growth along the thickness dimension [8]. Both of the reasons lead to the amorphous state of the stacked LaTiON/LaON film. It should be noted that a charge-trapping dielectric with an amorphous structure is favorable for achieving excellent retention property, because charge loss via grain boundaries can be avoided.

Figure 3 shows the TEM cross-sectional images of the conventional MONOS and BE-MONOS capacitors. The thickness of each layer for the MONOS and BE-MONOS capacitors is determined to be 2.0 nm/4.3 nm/14.1 nm (SiO_2/LaON/Al_2O_3) and 2.0 nm/5.0 nm/14.5 nm (SiO_2/LaON-LaTiON/Al_2O_3), respectively. Also, an abrupt interface at SiO_2/LaON is observed from Fig. 3(c). To gain deeper insight into the physical structure of the stacked film, the depth profiling of the stacked LaTiON/LaON film with sputtering time is also performed by XPS as shown in Fig. 4, where each layer can be easily distinguished based on the distribution of the elements. Moreover, the Ti content decreases linearly with sputtering time, suggesting its homogeneous distribution in the LaTiON film.

Figure 5 shows the J–V (gate current density versus gate voltage) characteristics of the MNOS capacitors with different high-k dielectric film under negative gate voltage corresponding to gate injection. The gate leakage at $V_G - V_{FB} = -2$ V (V_G is defined as gate voltage and V_{FB} represents flat-band voltage) is 3.6×10^{-3} A/cm^2, 1.2×10^{-4} A/cm^2, and 1.1×10^{-7} A/cm^2 for the MNOS capacitors with LaTiON, LaTiON/LaON and LaON, respectively. It is obvious that the MNOS capacitor with LaTiON displays much larger leakage than the one with LaON, which should be due to its lower barrier height (see below) between Al and LaTiON because the leakage normally changes inverse-exponentially with the barrier height. Moreover, the barrier height can be extracted by studying the current-conduction mechanism. It is found that the leakage current (J) of the MNOS capacitor with LaON is well consistent with the Fowler–Nordheim (F-N) tunneling under high electric field (E) as shown in Fig. 6, where $\ln(J/E^2)$ varies linearly with E^{-1}. For the F-N tunneling, the current density can be expressed as [16]

$$J_{FN} = \frac{q^2}{8\pi h}\frac{E^2}{\phi_{FN}}\exp\left(-\frac{8\pi\sqrt{2m^*}(q\phi_{FN})^{3/2}}{3qhE}\right) \quad (1)$$

where q is the electron charge; h is Planck's constant; m^* is the effective electron mass; and ϕ_{FN} is the Al/LaON barrier height, which can be extracted from the slope of the fitted line shown in Fig. 6(a). The extracted ϕ_{FN} is 2.38 eV, and is very close to the reported value (2.40 eV) [5], given that the

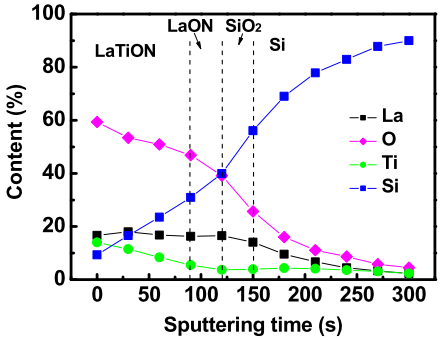

Fig. 4 XPS depth profile of the LaTiON/LaON/SiO_2 film on Si substrate

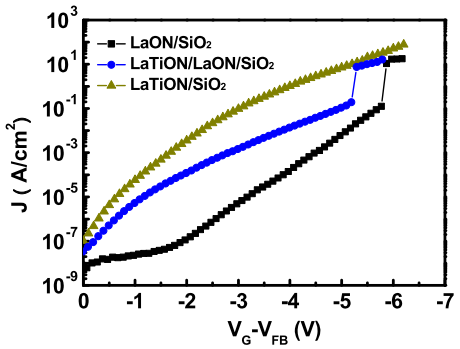

Fig. 5 J–V characteristics of the MNOS capacitors with LaON, LaTiON/LaON, and LaTiON

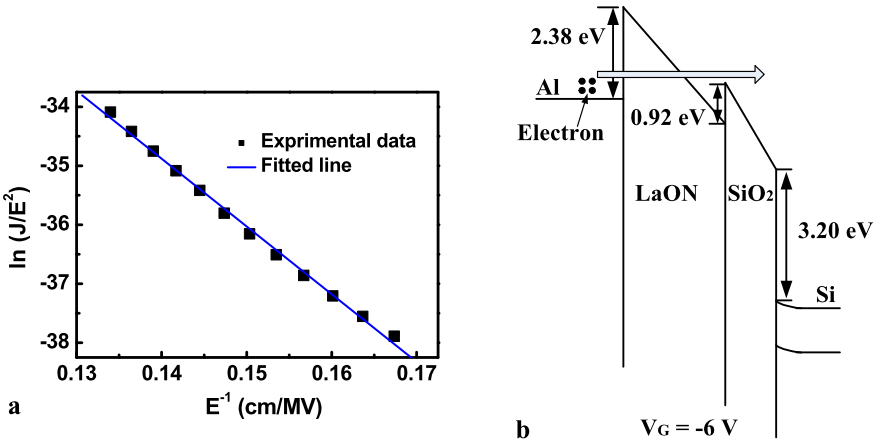

Fig. 6 (**a**) Fowler–Nordheim plot for the MNOS capacitor with LaON in the high-field region. (**b**) Conduction-band diagram of the MNOS capacitor with LaON under $V_G = -6$ V

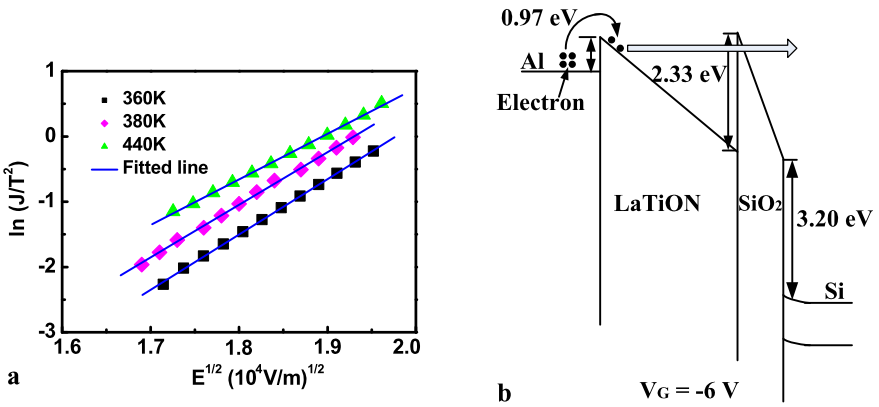

Fig. 7 (**a**) Schottky plot for the MNOS capacitor with LaTiON in the high-field region. (**b**) Conduction-band diagram of the MNOS capacitor with LaTiON under $V_G = -6$ V

electron affinity of Si is 4.05 eV and the work function of Al is 4.15 eV [5, 17]. On the other hand, the leakage current of the MNOS capacitor with LaTiON is found to obey Schottky emission, where $\ln(J/T^2)$ varies linearly with $E^{1/2}$ as shown in Fig. 7. For Schottky emission, the current density can be expressed as [16]

$$J_{SE} = AT^2 \exp\left(\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r})}{kT}\right) \quad (2)$$

where A is the Richardson constant; T is the Kelvin temperature; ε_0 is the permittivity of vacuum; ε_r is the dynamic dielectric constant of the dielectric film; k is Boltzmann's constant; and ϕ_B is the Al/LaTiON barrier height, which can be determined by the y-intercept of the fitted line in Fig. 7(a). The extracted ϕ_B is 0.97 ± 0.04 eV, which is intermediate between the Al/TiO_2 barrier height (0.10 eV) and Al/La_2O_3 barrier height (2.40 eV) [5]. For LaTiON, due to the smaller atomic radius of Ti (1.40 Å) than that of La (1.95 Å), Ti d states (instead of La d states) act as the conduction-band edge of LaTiON, thus leading to a smaller barrier height at Al/LaTiON (0.97 eV) than that at Al/LaON (2.38 eV) [11, 12]. According to the above analysis, the energy band diagram for the BE-MONOS capacitor under P/E and retention modes can be illustrated in Fig. 1, where the band gap of the Al_2O_3, LaTiON, LaON and SiO_2 layers is about 8.8 eV,

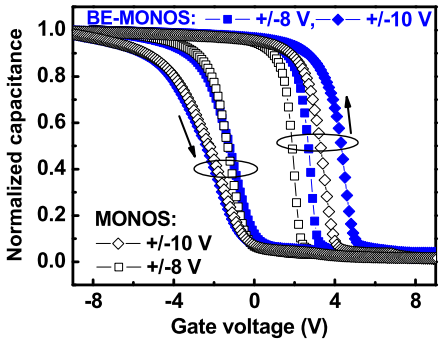

Fig. 8 C–V hysteresis curve of the conventional MONOS and BE–MONOS capacitors

3.5 eV, 6.0 eV, and 9.0 eV, respectively [5, 18]. In addition, the dielectric constant of the LaTiON and LaON is evaluated by C–V (capacitance versus gate voltage) measurements to be 33 and 15, respectively. Ti incorporated into the LaON film can induce softening of phonon modes which is responsible for the increase in dielectric constant of the LaTiON film [11, 12]. It is believed that the formation of silicate at the LaON/SiO_2 interface leads to a lower dielectric constant than that of pure La_2O_3(25) [1, 19].

Figure 8 exhibits the 1-MHz C–V hysteresis loops of the conventional MONOS and BE-MONOS capacitors. Sweep-

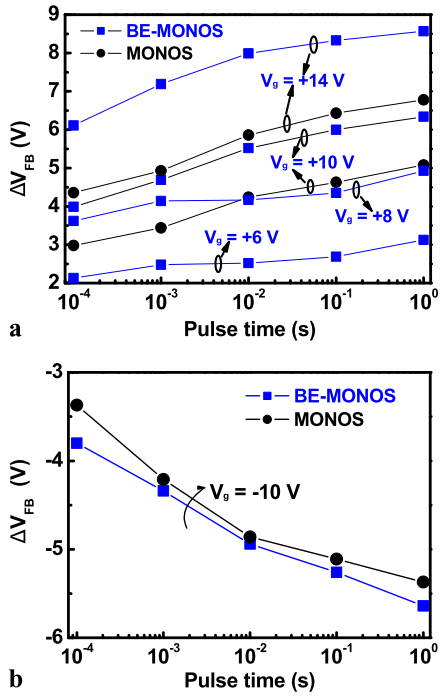

Fig. 9 (**a**) Program and (**b**) erase transient characteristics for the conventional MONOS and BE-MONOS capacitors. The devices are programmed to $V_{FB} = 6.0$ V before erase

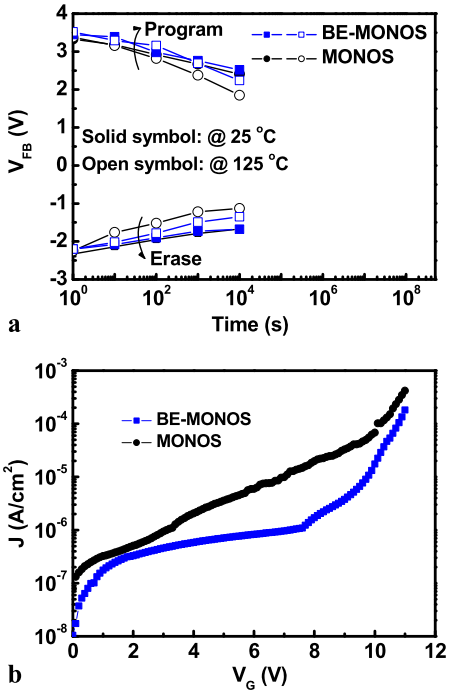

Fig. 10 (**a**) Retention characteristics of the conventional MONOS and BE-MONOS capacitors measured at 25 °C and 125 °C. (**b**) J–V characteristics of the conventional MONOS and BE-MONOS capacitors measured at 25 °C

ing starts from inversion region to accumulation region, and back to inversion region again. As the sweeping voltage increases from ±8 V to ±10 V, the memory window increases from 3.5 V/2.9 V to 5.4 V/4.9 V for the BE-MONOS and MONOS devices, respectively. It is obvious that the BE-MONOS capacitor possesses a larger memory window than the MONOS one, indicating higher trap density in the stacked LaTiON/LaON film.

Figure 9 depicts the P/E transient characteristics of the conventional MONOS and BE-MONOS capacitors under various gate voltages, with the BE-MONOS sample displaying higher P/E speeds than the latter under the same operating conditions. For the BE-MONOS and MONOS capacitors, the programmed V_{FB} shift (ΔV_{FB}, defined as the change of V_{FB} due to stress) at +14 V for 1 ms is 7.2 V and 4.9 V, respectively. Moreover, the BE-MONOS capacitor even shows a memory window of 4.7 V under a lower program voltage of +10 V for 1 ms, which is close to the value at +14 V for 1 ms for the conventional MONOS one, further supporting its higher program speed. For the BE-MONOS sample, a ΔV_{FB} of 2.1 V can still be obtained even under a lower gate voltage of +6 V for 100 μs, suggesting its potential for low-voltage high-performance memory applications. As illustrated by the energy band diagram in Fig. 1(b), this higher program speed of the BE-MONOS sample should be mainly ascribed to the shortened tunneling path of electrons from the substrate into CTL. Moreover, the higher trap density and higher dielectric constant of the stacked LaTiON/LaON film can also contribute to the higher program speed. However, different from the program phenomenon shown in Fig. 9(a), only a slight improvement of the erase speed is observed for the BE-MONOS sample shown in Fig. 9(b). In the erase mode, the stored electrons in CTL will tunnel back into the Si substrate, or recombine with holes from the substrate. The higher erase speed for the BE-MONOS sample should be ascribed to its higher hole-trapping efficiency resulting from its higher trap density. Due to the different valence of the Ti and La atoms, Ti incorporated into the LaON film can induce considerable oxygen vacancies which will give rise to large quantities of traps in the band gap of the LaTiON film [12]. On the other hand, as shown in Fig. 1(c), it is more difficult for the trapped electrons tunneling back to the substrate because of the larger barrier height (2.33 eV) between LaTiON and SiO_2 as compared with that of LaON/SiO_2 (0.90 eV) in the MONOS sample. Subsequently, only a slight improvement of the erase speed is observed for the BE-MONOS sample compared with the MONOS one.

Figure 10(a) shows the retention characteristics of the conventional MONOS and BE-MONOS capacitors measured at 25 °C and 125 °C. Both of the samples are operated to achieve a similar P/E memory window (5.7 V) at first for the measurement. For the BE-MONOS and MONOS capacitors, the retained P/E memory window after 10^4-s baking time degrades to be 3.6 V and 3.0 V, corresponding

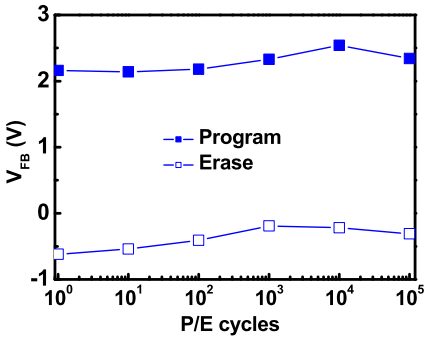

Fig. 11 Endurance characteristics of the BE-MONOS capacitor under a ±8-V 100-μs stress pulse measured at room temperature

to a charge loss of 37.2 % and 47.1 %, respectively. For the BE-MONOS sample, two main reasons are responsible for the improvement of its retention characteristics, and can be illustrated by the energy band diagram shown in Fig. 1(d). One is the large barrier height between LaTiON and SiO_2 which suppresses the escaping of charges from the CTL because the tunneling probability changes inverse-exponentially with the barrier height. Another reason lies in the lengthened tunneling path for the trapped charges de-trapping under the retention mode. The retention property can further be investigated by the J–V curves shown in Fig. 10(b), where the BE-MONOS sample displays smaller gate leakage than the MONOS one at low gate voltage, thus smaller charge loss. The smaller gate leakage of the BE-MONOS sample suggests its lower power consumption, which should be due to its lengthened tunneling path at low gate voltage (retention mode) and higher charge-trapping efficiency at high gate voltage (program mode), thus fewer electrons passing through the CTL into the gate.

Figure 11 shows the endurance characteristics of the BE-MONOS capacitor under a ±8-V 100-μs stress pulse. The P/E memory window before and after 10^5-cycle P/E stressing is 2.78 V and 2.65 V, respectively, corresponding to a slight degradation of 4.7 %. Such a good endurance property should be mainly due to its high P/E speeds at low gate voltages.

4 Conclusion

In conclusion, the charge-trapping characteristics of stacked LaTiON/LaON film are investigated by using MONOS-type memory capacitors. The band profile of the BE-MONOS structure is built by investigating its current-conduction mechanism. Compared with the conventional MONOS capacitor with LaON as CTL, the BE-MONOS one with stacked LaTiON/LaON as CTL shows better electrical characteristics in terms of larger memory window, higher P/E speeds and smaller charge loss at high temperature. Therefore, the stacked LaTiON/LaON film is promising as charge-trapping layer for high-performance nonvolatile memory applications.

References

1. H.J. Kim, S.Y. Cha, D.J. Choi, Mater. Sci. Semicond. Process. **13**, 9 (2010)
2. J.C. Wang, C.T. Lin, J. Appl. Phys. **109**, 064506 (2011)
3. J. Kwo, M. Hong, A.R. Kortan, K.L. Queeney, Y.J. Chabal, R.L. Opila, D.A. Muller, S.N.G. Chu, B.J. Sapjeta, T.S. Lay, J.P. Mannaerts, T. Boone, H.W. Krautter, J.J. Krajewski, A.M. Sergnt, J.M. Rosamilia, J. Appl. Phys. **89**, 3920 (2001)
4. T.M. Pan, T.Y. Yu, Semicond. Sci. Technol. **24**, 095022 (2009)
5. J. Robertson, Rep. Prog. Phys. **69**, 327 (2006)
6. Y.H. Wu, L.L. Chen, Y.S. Lin, M.Y. Li, H.C. Wu, IEEE Electron Device Lett. **30**, 1290 (2009)
7. H.J. Yang, C.F. Cheng, W.B. Chen, S.H. Lin, F.S. Yeh, S.P. McAlister, A. Chin, IEEE Trans. Electron Devices **55**, 1417 (2008)
8. J.Y. Wu, Y.T. Chen, M.H. Lin, T.B. Wu, IEEE Electron Device Lett. **31**, 993 (2010)
9. S.H. Lin, A. Chin, F.S. Yeh, S.P. McAlister, in *Tech. Dig. Int. Electron Device Meet* (2008), p. 843
10. G. Zhang, C.H. Ra, H.M. Li, T.Z. Shen, B.K. Cheong, W.J. Yoo, IEEE Trans. Electron Devices **57**, 2794 (2010)
11. G. Dutta, K.P.S.S. Hembram, G.M. Rao, U.V. Waghmare, J. Appl. Phys. **103**, 016102 (2008)
12. D.M. Ramo, A.L. Shluger, G. Bersuker, Phys. Rev. B **79**, 035306 (2009)
13. F.Y. Tian, D. Yang, R.L. Opila, A.V. Teplyakov, Appl. Surf. Sci. **258**, 3019 (2012)
14. X.D. Huang, P.T. Lai, ECS Trans. (2012) will be published
15. X.P. Wang, M.F. Li, A. Chin, C.X. Zhu, J. Shao, W. Lu, X.C. Shen, X.F. Yu, R. Chi, C. Shen, A.C.H. Huan, J.S. Pan, A.Y. Du, P. Lo, D.S.H. Chan, D.L. Kwong, Solid-State Electron. **50**, 986 (2006)
16. Y. Kim, S.I. Ohmi, K. Tsutsui, H. Iwai, Jpn. J. Appl. Phys. **44**, 4032 (2005)
17. W.J. Zhu, T.P. Ma, T. Tamagawa, J. Kim, Y. Di, IEEE Electron Device Lett. **23**, 97 (2002)
18. A. Ziani, C. Le Paven-Thivet, L. Le Gendre, D. Fasquelle, J.C. Carru, F. Tessier, J. Pinel, Thin Solid Films **517**, 544 (2008)
19. D. Eom, S.Y. No, C.S. Hwang, H.J. Kim, J. Electrochem. Soc. **154**, G49 (2007)