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Preface

Welcome to the first issue of the International Journal of Design, Analysis and Tools for Integrated Circuits and Systems (IJDATICS). This issue comprises of enhanced and extended version of research papers from the International DATICS Workshops in 2009.

DATICS Workshops were created by a network of researchers and engineers both from academia and industry in the areas of i) Design, Analysis and Tools for Integrated Circuits and Systems and ii) Communication, Computer Science, Software Engineering and Information Technology. The main target of DATICS Workshops is to bring together software/hardware engineering researchers, computer scientists, practitioners and people from industry to exchange theories, ideas, techniques and experiences.

This IJDATICS issue presents eight high quality research articles from eight different countries. This mix provides a comprehensive snapshot of state of the art research in the field and provides a springboard for driving future work and discussion. There are three key themes evident in these papers:

- *Analog and Digital Circuits:* Three papers address issues of circuit modeling and analysis. Boolchandani presents a Vector Machine based feasibility macromodel for analog circuit synthesis. Mahmoud looks at the impact of power supply noise on the performance of CMOS clock and data recovery circuits. Al-Hertani talks about the pattern dependent static power estimation of logic blocks in a library-free design environment.
- *VLSI Digital Systems:* Three papers introduce new analysis and design methodologies for VLSI digital system architectures. Lotfi-Kamran proposes a design methodology for pipelined processors to minimize unnecessary transitions in a NOP instruction. Yin introduces a hierarchical agent based Network-on-Chip (NoC) architecture with a real-time autonomous re-configuration. Benhamamouch presents an analysis approach to compute an upper estimation of the worst case execution time (WCET) of current complex hardware architectures.
- *Power Electronic Circuits:* Two papers talk about the application of electronics for the conversion of electric power. Chen illustrates a differential Class E power amplifier design with load mismatch protection and power control features. Huang describes a charge pump circuit topology which uses a voltage doubler as the clock scheme.

We are beholden to all of the authors for their contributions to DATICS Workshops in 2009. We would also like to thank the IJDATICS editorial team.

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