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Author(s)	Ng, DCW; Kwong, DKK; Wong, N
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Transactions Briefs

A Sub-1 V, 26 μW, Low-Output-Impedance CMOS Bandgap Reference With a Low Dropout or Source Follower Mode

David C. W. Ng, David K. K. Kwong, and Ngai Wong

***Abstract*—We present a low-power bandgap reference (BGR), functional from sub-1 V to 5 V supply voltage with either a low dropout (LDO) regulator or source follower (SF) output stage, denoted as the LDO or SF mode, in a 0.5-μm standard digital CMOS process with $V_{tn} \approx 0.6$ V and $|V_{tp}| \approx 0.7$ V at 27 °C. Both modes operate at sub-1 V under zero load with a power consumption of around 26 μW. At 1 V (1.1 V) supply, the LDO (SF) mode provides an output current up to 1.1 mA (0.35 mA), a load regulation of ±8.5 mV/mA (±33 mV/mA) with approximately 10 μs transient, a line regulation of ±4.2 mV/V (±50 μV/V), and a temperature compensated reference voltage of 0.228 V (0.235 V) with a temperature coefficient around 34 ppm/°C from −20 °C to 120 °C. At 1.5 V supply, the LDO (SF) mode can further drive up to 9.6 mA (3.2 mA) before the reference voltage falls to 90% of its nominal value. Such low-supply-voltage and high-current-driving BGR in standard digital CMOS processes is highly useful in portable and switching applications.**

***Index Terms*—CMOS bandgap, low dropout, source follower, sub-1V.**

I. Introduction

Low-voltage pure CMOS bandgap references (BGRs) [1]–[11] are of increasing importance with the widespread use of battery-operated mobile devices. Existing CMOS BGRs are mostly derivatives of the schemes in [2]–[5], utilizing the parasitic vertical substrate pnp or npn inherent to digital CMOS processes. However, when current is sunk or sourced directly from the BGR, even in the order of 10 μA, the reference voltage collapses due to its high output impedance, making it unsuitable for noisy applications such as high-speed analog-to-digital converters (ADCs) or switched-mode power supplies (SMPSs) [12], [13]. On the other hand, though some BGRs can operate at sub-1 V supplies [1], [4]–[10], they are again incapable of driving a current in the order of 10 μA. Consequently, sub-1 V CMOS BGRs having a low output impedance and high current driving capability are of high practical value.

Sub-1 V CMOS BGRs are relatively difficult to design due to: 1) the bandgap voltage of silicon is around 1.25 V and 2) the input common-mode voltage of the error amplifier forms a barrier in developing the ΔV_{EB} loop [depicted in Fig. 1(a)] at sub-1 V, no matter whether an nMOS or a pMOS input stage is used [2], [4], [6]. Though these problems can be overcome by using DTMOST devices [9], resistive subdivision method [4], [7] or sub-threshold voltage devices [5], these solutions cannot output load currents (from the reference voltage node) that are typically required in practice, or require extra masks or additional cost. Alternatively, a unity-gain opamp can buffer the output of a low-voltage high-output-impedance BGR. To achieve a low output impedance, the opamp is usually a high-gain operational transconductance (g_m) amplifier (OTA) whose output impedance in feedback is approximately $1/g_m$. However, achieving such a high transconductance gain at a low voltage involves high power consumption, complicated compensation techniques, and is generally infeasible with a sub-1 V supply (e.g., at least 2 V in [14]).

To this end, we present sub-1 V BGRs implemented in a 0.5-μm standard digital CMOS process with either a low dropout (LDO) regulator or source follower (SF) output stage/mode, denoted respectively as the LDO BGR or SF BGR. The LDO (SF) architecture starts operating at 0.93 V (0.95 V) under zero load, and exhibits a current driving capability of 1.1 mA (0.35 mA) at 1 V (1.1 V) supply, and even up to 9.6 mA (3.2 mA) at 1.5 V supply before the reference voltage falls to 90% of its nominal value. A parallel proportional-to-absolute-temperature (PTAT) resistor connection [10] is then coupled to an nMOS differential pair to form the LDO/SF loop with high current drive. Also, the SF BGR employs an nMOS output stage, not reported in existing sub-1 V BGR designs to our knowledge, that benefits from inherent feedback and low output impedance (thereby good line regulation). Lab measurements then confirm the excellence of the proposed LDO and SF BGRs against existing designs.

II. Proposed LDO and SF BGRs

Fig. 1(a)–(c) show the schematics of the proposed CMOS BGRs whose operations are described in the following.

A. Temperature-Independent Voltage Reference

On the one hand, the low-voltage complementary-to-absolute-temperature (CTAT) current circuit, for generating I_{CTAT}, is formed by p01, p02, opamp2 (Q4, Q5, p03–p11, n01–n07), Q3, R_c, R_d, and R_a. The opamp2 circuit operates at sub-1 V, whereas Q4 and Q5 are parasitic vertical BJTs forming into a dc level-shifting current mirror to overcome the problem of common-mode input voltage [4]. From Fig. 1(a), the current $I_{\mathrm{CTAT}} = I_{\mathrm{sd},p107}$ mirrors $I_{\mathrm{sd},p02}$ (here $I_{\mathrm{sd},p107}$ denotes the source-to-drain current of p107 and similar notation applies to other transistors). Subsequently

$$I_{\mathrm{CTAT}} = \frac{V_{EB3}}{R_a}\left(\frac{R_d}{R_c + R_d}\right) = \frac{V_{EB3}}{R'} \tag{1}$$

where $R' = R_a(R_c + R_d)/R_d$ and V_{EB3} is the forward-biased voltage of Q3 which decreases roughly linearly with temperature and hence constitutes a CTAT behavior [13]. On the other hand, the low-voltage PTAT current circuit, for generating I_{PTAT}, is formed by Q1 and Q2 (biased by current sources from p100 and p101), R_1, opamp1 (p102–p106 and n101–n107), and p107. Denoting the current through R_1 as I_{PTAT}, we then have

$$V_{EB1} + I_{\mathrm{PTAT}}R_1 = V_{EB2} \Rightarrow I_{\mathrm{PTAT}} = \frac{V_T \ln(n)}{R_1} \tag{2}$$

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N. Wong is with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong (e-mail: nwong@eee.hku.hk).

D. C. W. Ng and D. K. K. Kwong are with the Portable AMS Designs, IC Designs Group of the Hong Kong Applied Science and Technology Research Institute (ASTRI), Hong Kong (e-mail: davidng@astri.org).

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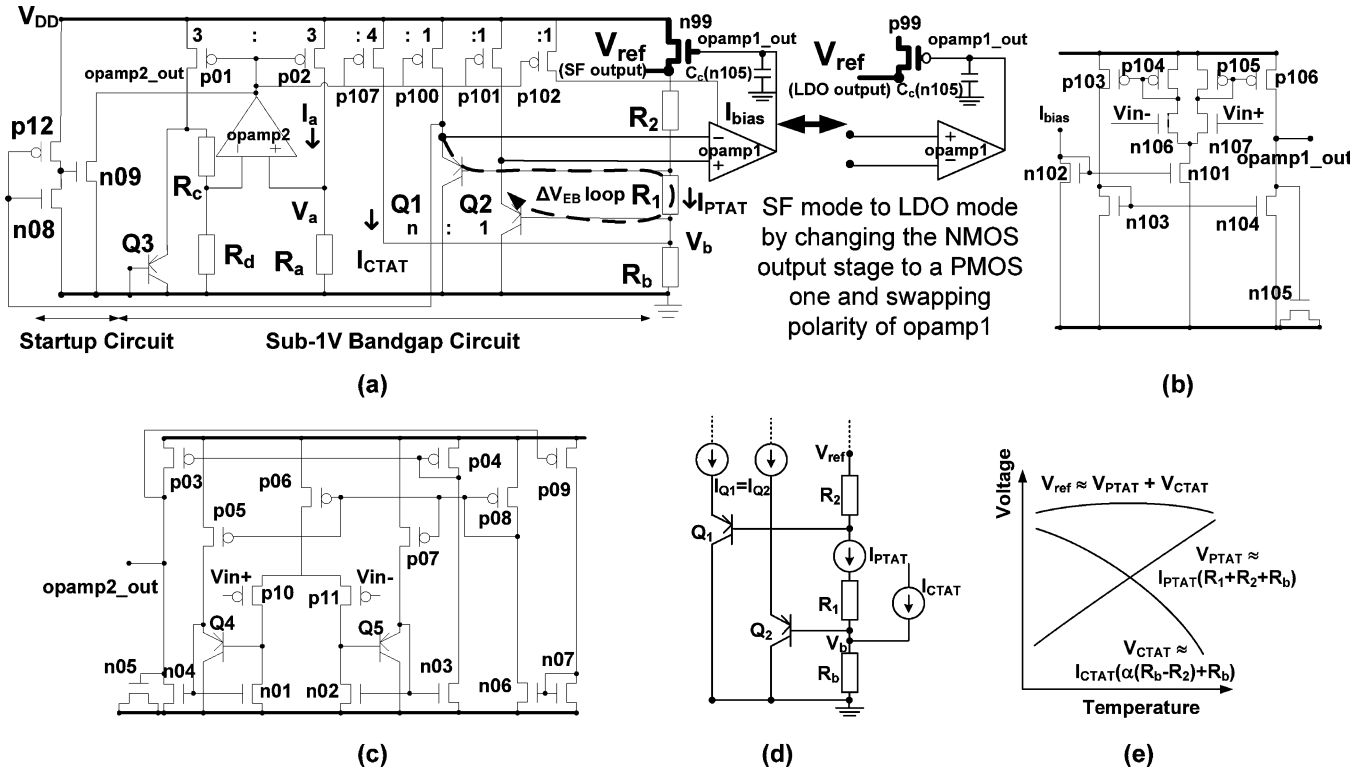

Fig. 1. (a) Proposed SF/LDO mode BGR. (b) Schematics of opamp1. (c) Schematics of opamp2. (d) $I_{\rm CTAT}$ and $I_{\rm PTAT}$ current sources. (e) Temperature behavior of $V_{\rm ref}$.

where n is the emitter area ratio of Q1 to Q2 and V_T is the thermal voltage. Also, $I_{\rm CTAT} = mI_{Q1} = mI_{Q2}$ where m is the ratio of p107 to p100 or p101, and I_{Q1} and I_{Q2} are the emitter currents of Q1 and Q2, respectively. Consequently, in contrast to $I_{\rm CTAT}$, $I_{\rm PTAT}$ has a positive temperature coefficient. The base currents of Q1 and Q2, denoted, respectively, as I_{B1} and I_{B2}, satisfy $I_{B1} = I_{B2} = I_{Q1}/(\beta+1) = I_{Q2}/(\beta+1)$, where β is the collector-base current amplification which is usually low for a parasitic BJT. Therefore, $I_{B1} = I_{B2} = \alpha I_{\rm CTAT}$, where $\alpha = 1/(m(\beta+1))$. A first-order approximation of V_b is

$$V_b \approx (I_{B2} + I_{\rm CTAT} + I_{\rm PTAT})R_b. \tag{3}$$

Noting that the voltage across R_1 is $V_T \ln(n)$ and that across R_2 is $(I_{\rm PTAT} - I_{B1})R_2$, we subsequently have

$$V_{\rm ref} \approx \left(\frac{\alpha(R_b - R_2) + R_b}{R'}\right) \times \left(\frac{(R_1 + R_2 + R_b)R'}{R_1(\alpha(R_b - R_2) + R_b)} V_T \ln(n) + V_{EB3}\right). \tag{4}$$

By designing the resistors in (4) such that the coefficient of V_T is around 22, an approximately temperature-independent voltage reference is obtained [15], as depicted in Fig. 1(d) and (e), where $V_{\rm PTAT} \approx I_{\rm PTAT}(R_1 + R_2 + R_b)$ and $V_{\rm CTAT} \approx I_{\rm CTAT}(\alpha(R_b - R_2) + R_b)$. Fig. 1(d) also shows that $I_{\rm CTAT}$ and $I_{\rm PTAT}$ can be regarded as two current sources below the $V_{\rm ref}$ node fixing the amount of current flowing from the $V_{\rm ref}$ node to ground. This configuration defines the reference voltage well even when there are changes in current loading, which gets the output current from $V_{\rm DD}$ through the output-stage (p/n)MOS. In our design, $R_a : R_b : R_c : R_d : R_1 : R_2 \approx 2.75 : 2.25 : 35.1 : 7 : 15(16.68) : 1$ in the LDO (SF) mode. The resistor ratios are designed according to the terms in the first bracket in (4) such that a $V_{\rm ref}$ of 0.228 V (0.235 V) is produced in the LDO (SF) mode.

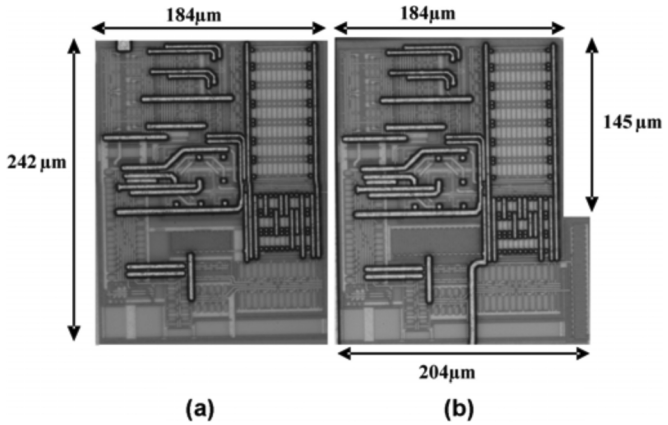

Fig. 2. Die photos: (a) SF BGR and (b) LDO BGR.

B. Stability and Load/Line Regulation

Both the LDO and SF BGRs form positive and negative loops inside the circuit under zero load condition. Referring to the SF mode in Fig. 1(a), the negative loop gain magnitude is $|A_{Q1}A_{\rm opamp1}A_{n99}|((R_1+R_b)/(R_1+R_2+R_b))$, whereas that of the positive loop is $|A_{Q2}A_{\rm opamp1}A_{n99}|((R_b)/(R_1+R_2+R_b))$, where $A_{Q1}, A_{Q2}, A_{\rm opamp1}$, and A_{n99} are the gains of Q1, Q2, opamp1, and n99, respectively, and $A_{Q1} \approx A_{Q2} \approx 1$ due to their unity-gain configurations. In the LDO mode, A_{n99} is simply replaced by A_{p99}. In both modes, the negative loop gain magnitude is larger than that of the positive loop due to an additional R_1 term in the numerator. To ensure a positive phase margin for the negative loop and thereby overall stability for either mode, we employ dominant pole compensation with n105 acting as the capacitor C_c as in Fig. 1(a) for

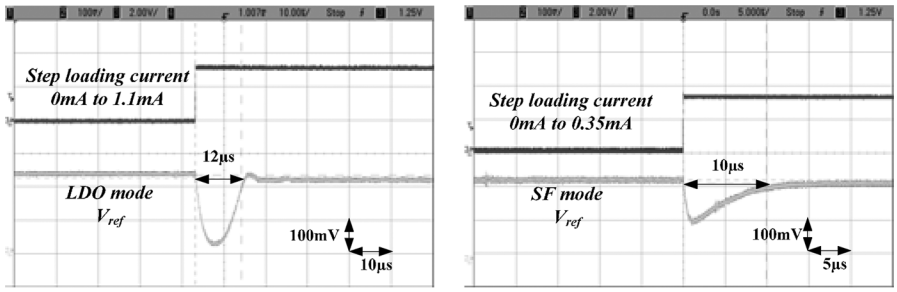

Fig. 3. (a) Measured LDO BGR load regulation with dominant pole compensation: (upper) 1.1 mA step loading under 1 V supply; (lower) output voltage settled to $<$ 18 mV in $<$ 12 μs. (b) Measured SF BGR load regulation with dominant pole compensation: (upper) 0.35 mA step loading under 1.1 V supply; (lower) output voltage settled to $<$ 20 mV in $<$ 10 μs.

simplicity and verification of concept, though various compensation schemes can also be used (e.g., [16]). The design constitutes an excellent current-driving capability (see Section III) which is in great contrast to prior works that are incapable of driving an output current even in the order of 10 μA [2], [4], [6], [7].

C. Low Supply Voltage and Power

To find the minimum supply $V_{\rm DD,min}$, the critical path for the LDO mode gives $V_{\rm DD,min} \approx |V_{{\rm dsat},p100}| + V_{EB1} + I_{\rm PTAT}R_1 + V_b \approx 0.92$ V (here the voltage across R_b is $V_b \approx 0.18$ V), whereas for the SF mode $V_{\rm DD,min} \approx |V_{{\rm dsat},p106}| + V_{gs,n99} + V_{\rm ref} \approx 0.94$ V. Lab measurements show that the $V_{\rm DD,min}$ in the LDO and SF modes are 0.93 and 0.95 V, respectively, with a zero-load power as low as 26 μW at these voltages or around 28 μW at a 1 V supply. We remark that the biasing current is formed by the $I_{\rm CTAT}$ loop and is relatively independent of the supply voltage.

Moreover, by adjusting the resistors in (4), the output voltage $V_{\rm ref}$ can be made as large as 3.3 V or even higher. For example, to obtain a $V_{\rm ref}$ of 3.3 V, the minimum supply is $V_{\rm DD} \approx \min(|V_{{\rm dsat},p100}| + V_{EB1} + I_{\rm PTAT}R_1 + V_b, V_{\rm ref} + |V_{{\rm dsat},p99}|) \approx 3.35$ V for the LDO mode, and $V_{\rm DD} \approx V_{\rm ref} + V_{gs,n99} + |V_{{\rm dsat},p106}| \approx 4.0$ V for the SF mode. In that case, the output current driving capability would also be raised due to the larger headroom for $|V_{gs,p99}|$ or $V_{gs,n99}$.

D. Minimum Input Commode-Mode Voltage and Offset Effect

The minimum input common-mode voltage for the normal operation of the differential pair in opamp1 is approximately $V_{gs,n106/107} + V_{dsat,n101} \approx V_{tn} + V_{dsat,n106/107} + V_{dsat,n101} \approx 0.6 + 0.05 + 0.05 = 0.7$ V. The minimum voltage at the emitters of Q1 and Q2 is $\min(V_{EB1} + V_b + I_{\rm PTAT}R_1, V_{EB2} + V_b) = V_{EB2} + V_b \approx 0.6V + 0.18V = 0.78V > 0.7$ V, so the input differential pair is always on where V_{EB1} and V_{EB2} are around 0.6 V. As V_{EB1}, V_{EB2}, and V_{tn} all decrease with increasing temperature, for $V_{EB2} + V_b > V_{gs,n106/107} + V_{\rm dsat,n101}$, we have to choose an appropriate value of V_b and W/L ratios of n106, n107, and n101 such that the inequality always holds. We remark that unlike the conventional approach that uses a pMOS differential pair and two extra current branches for level shifting in opamp1 for a sub-1 V BGR [4] (like what opamp2 does in Fig. 1(c)), our architecture permits an nMOS differential pair as shown in Fig. 1(b) for which the level shifting is provided by the emitters of Q1 and Q2 through the voltage drop across R_b [10]. In other words, the proposed LDO or SF BGR consumes less power than other BGRs with current drive (such as [17]) and the $V_{\rm ref}$ node is kept inside the current regulation loop, making the self-regulated nature of this BGR core attractive.

The offset voltages of opamp1 and opamp2, denoted by V_{os1} and V_{os2}, respectively, can be taken into account by replacing the terms $V_T \ln(n)$ and V_{EB3} in (4) with $(V_T \ln(n) + V_{os1})$ and $(V_{EB3} + V_{os2}R'/R_a)$, respectively. Nonetheless, this offset effect can be reduced by increasing the emitter area ratio (n) of Q1 to Q2 and decreasing the ratio R_c/R_d (and therefore R'/R_a), while keeping the coefficient of V_T to be around 22 (see Section II-A). Subsequently, the sizes of $((R_1+R_2+R_b)R')/(R_1(\alpha(R_b-R_2)+R_b))$ and R'/R_a are decreased, which in turn suppresses the influence of offset voltages. Also, systematic and random offsets can be reduced by appropriate transistor sizing, bias current ratio, symmetrical and compact layout techniques [4], [18], etc.

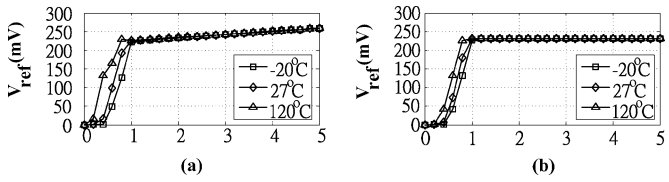

Fig. 4. $V_{\rm ref}$ versus $V_{\rm DD}$: (a) LDO BGR and (b) SF BGR.

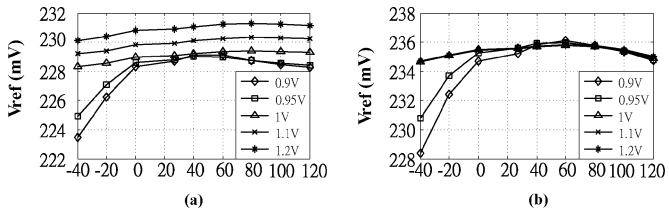

Fig. 5. $V_{\rm ref}$ versus temperature: (a) LDO BGR and (b) SF BGR.

III. Lab Measurements and Discussions

Die photos for the proposed LDO and SF BGRs are shown in Fig. 2. The lab measurements show, for the LDO or SF mode, the BGR starts up at around 0.9 V without load and operates with current driving capability from approximately 1 V onwards. With a supply of $V_{\rm DD} = 1$ V, the LDO $V_{\rm ref} = 0.228$ V and SF $V_{\rm ref} = 0.235$ V and both architectures have a temperature coefficient of around 34 ppm/°C without trimming. The transient responses are captured in Fig. 3 which shows that the proposed BGRs are able to settle to within 90% of their nominal outputs in a relatively short time. Figs. 4 and 5 further show the $V_{\rm ref}$ behavior against $V_{\rm DD}$ and temperature.

We note that the LDO mode can source current at sub-1 V supply while the SF can only do so beyond 1 V. Moreover, for $V_{\rm DD} > 1$ V, the SF mode outputs only about $1/3$ of the current available through the LDO configuration. At $V_{\rm DD} = 1.5$ V, the maximum output currents are 1 mA in the SF mode and 1.3 mA in the LDO mode with reference voltages within 98% of their nominal values, and are respectively 3.2

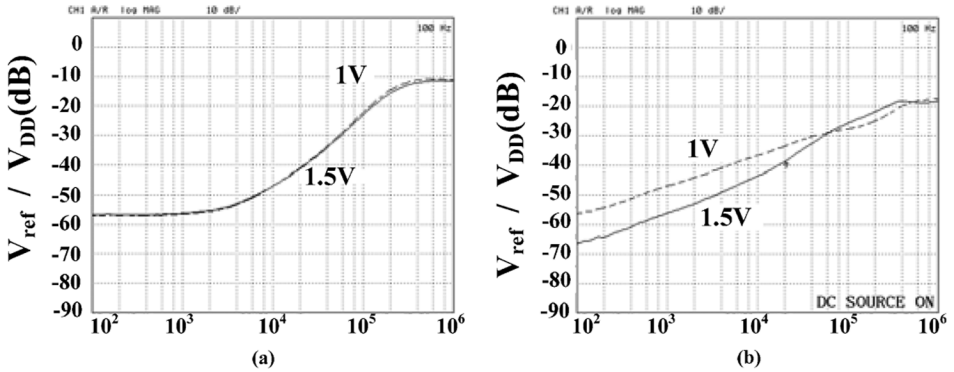

Fig. 6. PSRRs of (a) LDO BGR and (b) SF BGR at different $V_{\rm DD}$ values.

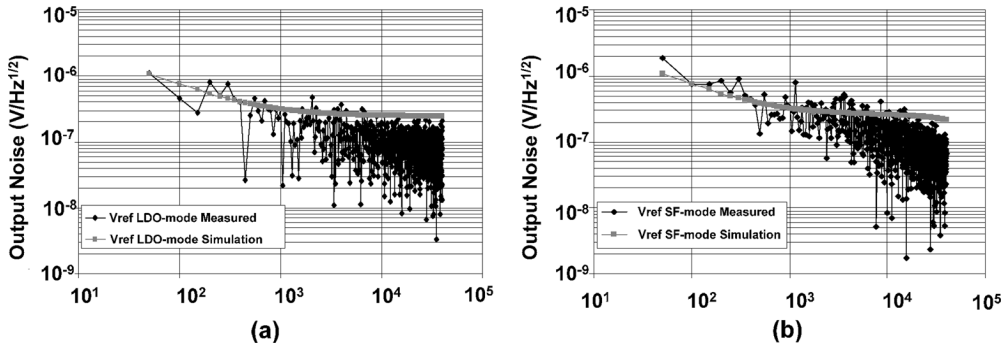

Fig. 7. Noise spectral densities at $V_{\rm DD} = 1$ V: (a) LDO BGR and (b) SF BGR.

TABLE I
COMPARISON OF THE PROPOSED BANDGAP REFERENCES (FIRST TWO COLUMNS) AGAINST EXISTING DESIGNS

	LDO	SF	[6]#2	[7]	[4]	[17]	[10]	[20]	[1]	[19]#5
Tech-nology	0.5μm CMOS	0.5μm CMOS	0.25μm CMOS	0.5μm BiCMOS	0.6μm CMOS	0.6μm BiCMOS#7	0.6μm CMOS	0.35μm CMOS	0.35μm CMOS	BiCMOS#8
V_{DD} range /V	0.93∼5	0.95∼5	0.9∼1.2	1∼5	0.98∼1.5	0.9	0.8∼2	0.9∼4	0.9-3.5	0.9-10
V_{ref}/ mV	228	235	536	190.9	603	890	356	670	635	200
Tempco /ppm/^{o}C	34	34	19.5	11	15	34.7	20	10	∼142#4	∼41.9#6
Line reg. /±μV/V	4200	50	18333	24	4231	N/A	8333	904	1750	198#6
Load reg. /mV/mA	±14.6 @V_{DD}=0.96V ±1.2 @V_{DD}=1.5V	±33 @V_{DD}=1.1V ±3.6 @V_{DD}=1.5V	N/A	N/A	N/A	N/A	N/A	N/A	N/A	±3.6 @V_{DD}=1.5V
PSRR	-58dB @100Hz -12dB @1MHz	-58dB @100Hz#1 -18dB @1MHz	-25dB @10kHz	N/A	-44dB @10kHz	N/A	N/A	-53dB @100Hz#3 -42dB @1MHz #3	-46.7dB @100Hz -4dB @30kHz	-64dB @120Hz#9 -22dB @1MHz#9
Supply current /μA	28	28	50	20	18	49	2.5	0.04	16.6	120
$I_{out-max}$ /mA	9.6 @V_{DD}=1.5V	3.2 @V_{DD}=1.5V	N/A	N/A	N/A	5	N/A	N/A	1	100
Die area /mm^2	0.0464	0.0445	0.1085	0.4	0.24	N/A	0.04	0.045	0.059	N/A

Remarks: #1: PSRR= -68dB @V_{DD}=1.5V; #2: requires both parasitic npn and pnp; #3: @V_{DD}=2V; #4:24.6$ppm/^oC$@V_{DD} =1.5V; #5: More precisely a BGR coupled to an error amplifier and a power pMOS; #6: @V_{ref} of the LDO; #7: BiCMOS or special CMOS process; #8: BiCMOS or Bipolar process; #9:@V_{DD}=1.5V

and 9.6 mA before the reference voltages fall to 90%. This is not surprising as $|V_{gs,p99}|$ has a larger voltage headroom than $V_{gs,n99}$ under the same $V_{\rm DD}$, and a larger dc gain due to the common source configuration. Consequently, the LDO mode has a better load regulation.

The line regulation of the SF mode is ± 50 μV/V whereas that of the LDO mode is ± 4.2 mV/V. When $V_{\rm DD}$ rises from sub-1 to 5 V in the LDO mode, the gate of p99 and therefore the output of opamp1 [cf. Fig. 1(a)] has to be raised by the same amount for a constant output current. Due to the finite gain of opamp1, an error voltage appears across its inverting and non-inverting inputs. This results in inaccuracy in the $I_{\rm PTAT}$ generation and thereby drift in the output reference voltage, which can be overcome by increasing the gain of opamp1. For the SF mode, the source of n99 is connected to the $V_{\rm ref}$ node instead of $V_{\rm DD}$, so the effect of line changes is less significant. To summarize, the LDO architecture should be chosen if the BGR is to be operated at a low supply voltage or when a low output impedance is desired. The SF structure, due to its excellent line regulation and inherent feedback [18], is a better choice when the supply line fluctuates a lot or when a faster and smaller-swing transient response is required.

Table I contrasts the proposed BGRs with various sub-1 V or near-1 V BGRs in the literature. Although the BGR in [17] can source current, it requires high-current-amplification ($\beta \approx 100$) and collector-free lat-

eral pnp devices available only in special CMOS or BiCMOS processes with extra masks and thereby additional cost. In terms of power consumption, the proposed LDO and SF BGRs are much better than that in [17], and comparable to or better than other BGRs. Reference [1] can source current at around 1 V supply, but it suffers from a large temperature coefficient of about 142 ppm/°C at 1 V supply without load. Also, its power supply rejection ratio (PSRR) is around -4 dB at around 30–40 kHz, which is too close to unity and is not suitable for BGR application in switching environments. The PSRRs of the proposed BGRs are shown in Fig. 6. At low frequencies, the PSRR of the LDO mode is about -58 dB for $V_{\rm DD}$ around 1–1.5 V, and converges to -12 dB near 1 MHz. For the SF mode, the low-frequency PSRR is around -58 dB at $V_{\rm DD} = 1$ V which further drops to -68 dB at $V_{\rm DD} = 1.5$ V, with both curves converging to around -18 dB near 1 MHz. Such improvement in PSRR in the SF mode with an increasing $V_{\rm DD}$ is due to the increase of impedance from the $V_{\rm DD}$ node to the $V_{\rm ref}$ node, which matches its excellent line regulation property. Indeed, the PSRR of the SF mode is among the best and its line regulation is better than others except that in [7]. Fig. 7 shows that the simulated and measured noise spectra of the LDO and SF BGRs at room temperature under a 1 V supply are in good agreement. For both modes, the measured root-mean-square (rms) noise spectral densities are around 300 nV/$\sqrt{\rm Hz}$ at 1 kHz (the $1/{\rm f}$ noise corner frequency) and 70 nV/$\sqrt{\rm Hz}$ at 20 kHz, while the flat-band noise is about 220 nV/$\sqrt{\rm Hz}$. With a 0.1 μF capacitor inserted at the $V_{\rm ref}$ node, the noise densities at the two frequencies are reduced to 290 nV/$\sqrt{\rm Hz}$ and 10 nV/$\sqrt{\rm Hz}$, respectively, whereas the integrated total rms noise value is about 23 μV. The noise spectral density can further be improved by increasing the biasing current or adding a larger output capacitor [4], [7], [18], [19]. Furthermore, the LDO and SF BGRs have small die areas in a 0.5 μm process and have the largest operating supply voltage ranges (viz. sub-1V–5V) among all. They exhibit high current drives wherein the highest is 9.6 mA at $V_{\rm DD} = 1.5$ V for the LDO mode (excluding the part in [19] since it is in fact a BGR coupled to an error amplifier and a power pMOS), and therefore constitute the most cost-effective solutions.

IV. Conclusion

This paper has presented a novel BGR, with either a LDO or SF output stage, implementable in standard digital CMOS processes. With a low supply current around 26 μA at no load, the LDO and SF BGRs start up at sub-1 V supply voltages, and are capable to drive currents in the order of mA starting from $\sim$ 1 V supply and all the way up to 5 V. The excellent line regulation in the SF mode can resist line fluctuations, whereas the excellent load regulation in the LDO mode can effectively suppress load dumping. Both BGRs exhibit excellent PSRRs and noise properties, and are highly cost-effective with their small die areas. All these features make them favorable in noisy or switching applications like SMPSs or ADCs. Lab measurements have confirmed the performance of the proposed architectures over existing designs. The proposed BGRs can alternatively be viewed as an area-efficient temperature-compensated reference embedded in a LDO or SF regulator, allowing great design flexibilities especially for low-power on-chip applications.

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