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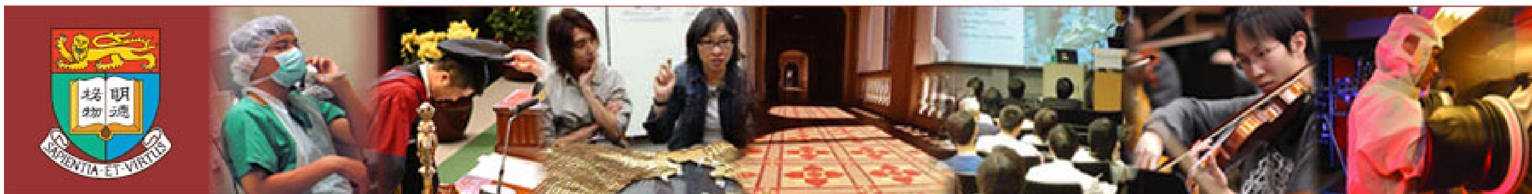

Title	Two-terminal write-once-read-many-times memory device based on charging-controlled current modulation in Al/Al-Rich Al 2O 3/p-Si diode
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Two-Terminal Write-Once-Read-Many-Times Memory Device Based on Charging-Controlled Current Modulation in Al/Al-Rich Al_2O_3/p-Si Diode

Wei Zhu, T. P. Chen, Yang Liu, Ming Yang, *Student Member, IEEE*, and S. Fung

***Abstract*—A write-once-read-many-times (WORM) memory device was realized based on the charging-controlled modulation in the current conduction of Al/Al-rich Al_2O_3/p-type Si diode. A large increase in the reverse current of the diode could be achieved with a negative charging voltage, e.g., charging at −25 V for 1 ms results in a current increase by about four orders. Memory states of the WORM device could be altered by changing the current conduction with charge trapping in the Al-rich Al_2O_3 layer. The memory exhibited good reading endurance and retention characteristics.**

***Index Terms*—Aluminum oxide, charging effect, current transport, metal-insulator-semiconductor (MIS) diode, metal nanoparticles, nanocrystals, non-volatile memory, WORM device.**

I. Introduction

WRITE-once-read-many-times (WORM) memories have widespread uses in all kinds of permanent archival storage applications, such as wireless identification tags and smart cards, rapid archival storage of video images where the vulnerability to breakage associated with slow and power-hungry magnetic or optical disk drives are not acceptable, etc. WORM memory devices based on organic small molecules and polymers have been reported in the recent years [1]–[6]. WORM memory devices based on all-inorganic materials such as aluminum nitride thin film containing Al nanocrystals (nc-Al) [7] and ZrO_2 [8] have been also reported recently. In this paper, a WORM device is realized based on the charging-controlled modulation in the current conduction of the Al/Al-rich Al_2O_3/p-type Si (p-Si) diode. It has been reported in previous studies that both electrons and holes can be trapped in the Al-rich Al_2O_3 thin films and the charge trapping greatly affects the current conduction across the thin films [9], [10]. In this paper, it is observed that a large increase in the reverse current of the Al/Al-rich Al_2O_3/p-Si diode could be achieved by applying a negative charging voltage to the diode. Memory states of the WORM device based on the diode structure could be manipulated with the charging effect. The WORM memory exhibits good reading endurance and retention characteristics.

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II. Experiment

An Al-rich Al_2O_3 thin film was synthesized with a reactive sputtering process [9], [10]. A 60-nm Al-rich Al_2O_3 thin film was deposited on a p-Si substrate by the radio-frequency magnetron sputtering of an Al target in the presence of a small amount of O_2 with a flow rate of $\sim$1 sccm. A rapid thermal annealing was then conducted at 550 °C for various durations ranging from 30 to 300 s in a N_2 ambient. For an aluminum oxide film synthesized with the reactive sputtering process, it is Al rich as confirmed by the X-ray photoelectron spectroscopy analysis, and the excess Al forms nc-Al in the Al_2O_3 matrix as revealed by the cross-sectional transmission electron microscopy measurement [10]. An aluminum film of 200 nm was deposited on the surface of the Al-rich Al_2O_3 thin film to form an Al/Al-rich Al_2O_3/p-Si diode, as shown in Fig. 1(a). The area of the diode is $\sim 3 \times 10^{-4}$ cm^2. The diode structure actually serves as a two-terminal WORM memory device in this paper. As the WORM device has a diode structure, its ON- and OFF-state currents (i.e., the reverse currents of the diode after and before a charging operation as discussed later) are proportional to the diode area, and thus, the currents can be scaled with the device area. Electrical measurements, including current–voltage (I–V) and capacitance–voltage (C–V) measurements, and the charging operations were carried out with a Keithley 4200 semiconductor characterization system in air at room temperature.

III. Result and Discussion

The diode structure exhibits forward and reverse I–V characteristics under negative and positive gate voltages, respectively. It has been observed that the reverse I–V characteristic can be seriously affected by applying a charging voltage to the device, but there is no significant impact of the charging voltage on

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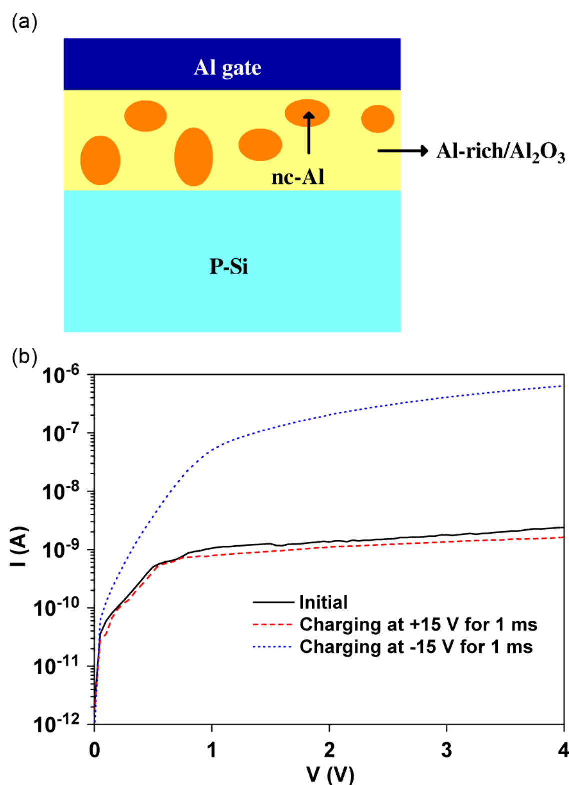

Fig. 1. (a) Schematic illustration of the WORM device based on the Al/Al-rich Al_2O_3/p-Si diode. (b) Reverse I–V characteristics of the diode before and after charging at ± 15 V for 1 ms.

the forward I–V characteristic. As an example, Fig. 1(b) shows the reverse I–V characteristics of the diode before and after charging at ± 15 V for 1 ms. As shown in the figure, the negative charging voltage leads to a large increase in the reverse current, whereas the positive charging voltage causes a small reduction in the reverse current. The influence of a charging voltage on the I–V characteristic is related to the influence of the charge trapping in the Al-rich Al_2O_3 layer caused by a charging voltage on the carrier transport in a current measurement [9], as discussed below.

For both the charging experiment and the current measurement, under the forward-bias condition (i.e., a negative voltage is applied to the Al gate), both the electron injection from the Al gate and the hole injection from the p-Si substrate simultaneously occur; under the reverse-bias condition (i.e., a positive voltage is applied to the Al gate), only the electron injection from the Si substrate occurs. The injected carriers can be transported along the tunneling paths formed by the nc-Al distributed in the aluminum oxide thin film [9], [10]. The oxide thin film should have a large amount of defects due to the imperfection of the Al_2O_3 matrix embedded with nc-Al, which can act as the effective charge trap centers. Some of the transported carriers are trapped in either the nc-Al or the defects in the oxide layer [9], [10], and at the same time, the charge trapping also occurs at the interfaces (either the gate/oxide or oxide/Si-substrate interfaces) where the carriers are injected. The situation should be similar to the charge trapping in the gate oxide and at the oxide/Si interface in a metal–oxide–semiconductor (MOS) structure when carriers are injected at the interface from the Si substrate to the gate oxide [11]. The charge trapping in the interface region due to the carrier injection will cause a change in the electric field at the interface, which will, in turn, affect the carrier injection [12], [13].

In a charging experiment, under the bias of a positive charging voltage, there is electron trapping in the oxide layer as only electrons are injected from the Si substrate. However, under the bias of a negative charging voltage, there could be both electron trapping and hole trapping in the oxide layer as both the electron injection from the gate and the hole injection from the Si substrate simultaneously occur. The net charge trapping in the oxide layer detected by the C–V measurement, which is sensitive to the charge trapping near the interface of the oxide/Si substrate, could be either negative or positive, depending on the magnitude of the charging voltage and the charging duration. The net charge trapping tends to be positive for a larger magnitude of negative charging voltage as a result of the strong hole injection from the p-Si substrate (note that holes are the majority carriers in the substrate). In the charging experiment of this paper, a net negative or positive charge trapping was observed from the C–V measurement for a positive or negative charging voltage, respectively. Fig. 2(a) shows the shifts in the C–V characteristic after the application of the charging voltage of $+15$ or -15 V for 1 ms. As shown in the figure, charging at $+15$ V leads to an increase in the flat-band voltage V_{FB} (i.e., $\Delta V_{\mathrm{FB}} > 0$), indicating the net electron trapping at the oxide/Si interface; in contrast, charging at -15 V leads to a decrease in the flat-band voltage (i.e., $\Delta V_{\mathrm{FB}} < 0$), indicating the net hole trapping at the oxide/Si interface. Fig. 2(b) shows the energy-band diagrams of the device under a positive gate bias (i.e., $V_G > 0$; e.g., in the reverse-current measurement) for the situations without charge trapping, with the positive charge trapping near the oxide/p-Si interface and with the negative charge trapping near the interface, respectively.

The charge trapping produced by the charging experiment could affect the carrier transport during the current measurement. The charge trapping (either electron or hole trapping) does not cause a large change in the forward I–V characteristics because both the electron injection from the gate and the hole injection from the Si substrate are involved in the forward I–V measurement [9]. However, the charge trapping has a significant impact on the reverse I–V characteristics, as shown in Fig. 1(b).

As shown in Fig. 1(b), the application of the positive charging voltage of 15 V for 1 ms, which causes only the electron trapping in the oxide, leads to a small reduction in the reverse current. As revealed in Fig. 2(a), the application of the positive charging voltage of 15 V for 1 ms leads to a net electron trapping in the oxide near the oxide/Si substrate interface. As shown in the energy-band diagram for the situation with the negative charge trapping near the interface presented in Fig. 2(b), the electron trapping reduces the electric field in the interface region under a positive gate voltage (i.e., the reverse-bias condition), thus decreasing the electron injection from the Si substrate during the reverse I–V measurement. In addition, the electron trapping can also suppress the electron transport across the oxide layer under the reverse-bias condition because

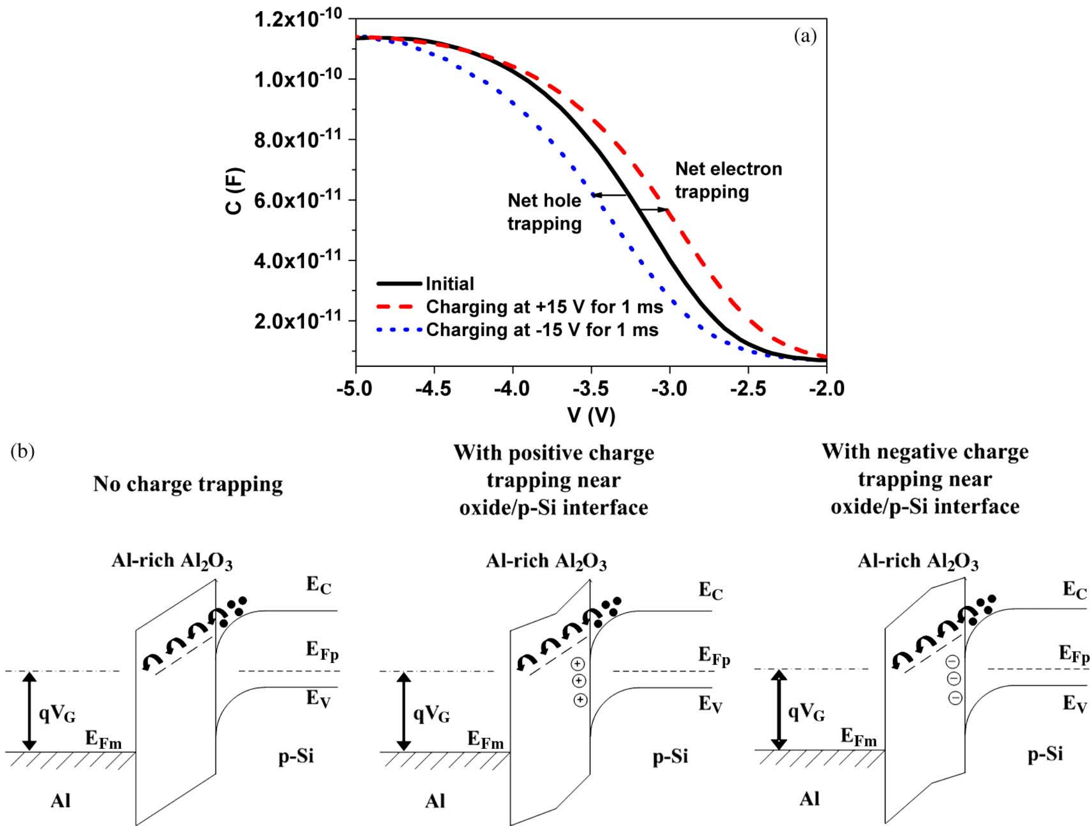

Fig. 2. (a) C–V characteristics before and after the application of ± 15 V for 1 ms. (b) Energy-band diagrams of the device under a positive gate bias (e.g., in the reverse-current measurement) for the situations without charge trapping, with the positive charge trapping near the oxide/p-Si interface and with the negative charge trapping near the interface, respectively.

of the electrostatic interaction of the transported electrons with the trapped electrons during the reverse-current measurement [9]. Therefore, the application of the positive charging voltage leads to a reduction in the reverse current.

In contrast, the application of the negative charging voltage of -15 V for 1 ms leads to a large increase in the reverse current (e.g., the current measured at $+2$ V is increased by approximately two orders), as shown in Fig. 1(b). Fig. 2(a) clearly shows that the application of -15 V for 1 ms leads to a significant equivalent amount of the hole trapping in the oxide near the oxide/substrate interface. As shown in the energy-band diagram for the situation with the positive charge trapping near the interface presented in Fig. 2(b), in the reverse-current measurement under a positive voltage, the hole trapping causes an increase in the electric field at the oxide/substrate interface, enhancing the electron injection at the interface during the reverse-current measurement. Therefore, a negative charging voltage leads to a large increase in the reverse current. The increase ΔE in the electric field in the oxide region near the oxide/substrate interface due to the hole trapping could be estimated from the C–V measurement (note that the C–V measurement is only sensitive to the charge trapping near the oxide/Si substrate interface) by using $\Delta E \approx \Delta V_{\mathrm{FB}}/d$, where d is the oxide thickness. ΔE is estimated to be 3.7×10^4 and 1.1×10^5 V/cm for the charging times of 1 ms and 1 s, respectively, at the charging voltage of -15 V.

As a negative charging voltage can produce a large increase in the reverse current, a two-terminal WORM memory device can be realized based on the change in the reverse current of the Al/Al-rich Al_2O_3/p-Si diode caused by a negative charging voltage. In other words, the memory states are represented by the currents measured at a small reverse bias that will not cause any significant charging in the oxide layer, and the memory states can be altered by using a large magnitude of negative charging voltage (i.e., the writing voltage in the WORM operation). For example, the reverse currents measured at $+2$ V before and after charging at -15 V for 1 ms represent two well-distinguished states (the current ratio of the state after writing to the state before writing is about 200). Note that, as shown in Fig. 1(b), the reverse current depends on the reverse bias. Therefore, the current ratio of the state after writing to the state before writing also depends on the detection voltage (i.e., the reverse bias). Thus, a suitable detection voltage should be chosen to achieve a large current ratio but not to change the charging state. It is also worthy to mention that the charging voltage can be scaled down by using a thinner Al-rich Al_2O_3 layer. For example, if the constant electric-field scaling law is used, the voltage can be reduced from 15 to $\sim$10 V when the oxide thickness decreases from 60 to 40 nm. To demonstrate the feasibility of the WORM application, a study on the memory performance and reliability has been conducted, as discussed below.

Fig. 3(a) shows the reverse current measured at $+2$ V as a function of the writing voltage for the fixed writing time of 1 s. The current is $\sim$1 nA before writing, and it increases to $\sim$3 nA after writing at -5 V. The current drastically increases to $\sim$200 nA after writing at -10 V, and it keeps increasing further

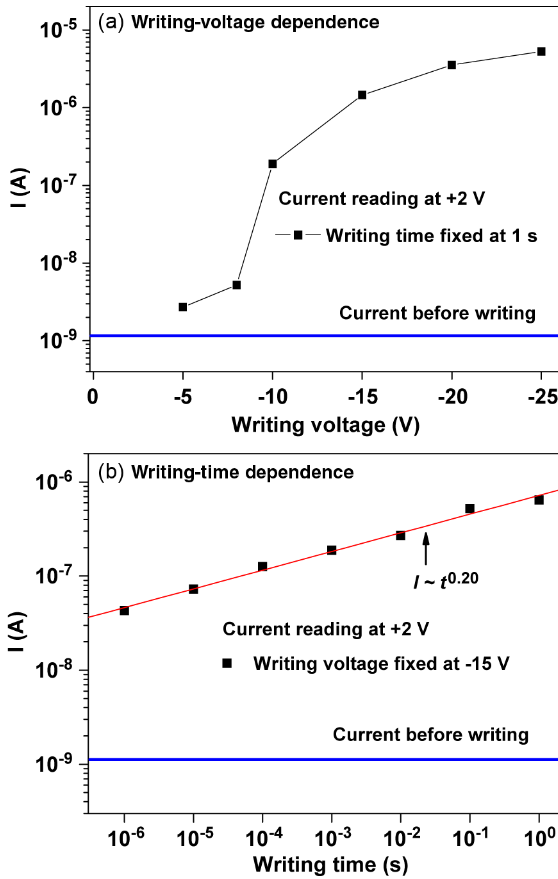

Fig. 3. Reverse current measured at +2 V as a function of either (a) the writing voltage for the fixed writing time of 1 s or (b) the writing time for the fixed writing voltage of −15 V.

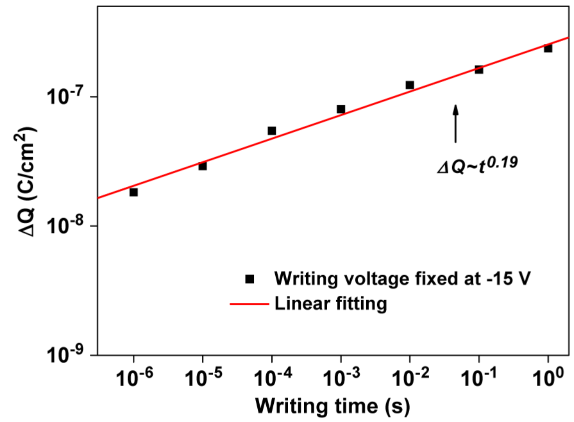

Fig. 4. Equivalent trapped charge per unit area at the oxide/Si interface as a function of the writing time.

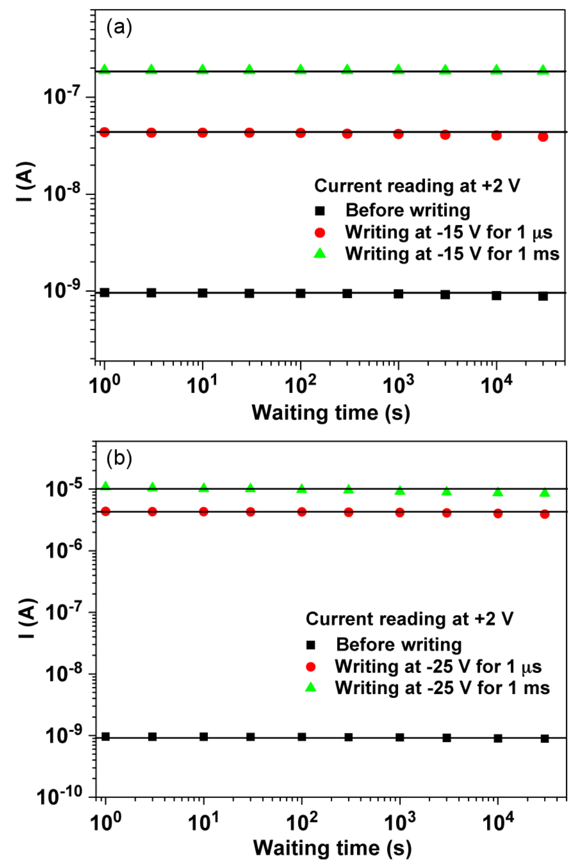

Fig. 5. Retention characteristics of different memory states. (a) Writing at −15 V for 1 μs or 1 ms. (b) Writing at −25 V for 1 μs or 1 ms.

with the magnitude of the writing voltage. Fig. 3(b) shows the current as a function of the writing time for the fixed writing voltage of −15 V. It should be pointed out that the experiments shown in Fig. 3 were carried out on different devices to avoid an accumulated charging effect. There may be a variation in the currents for different devices. However, such a variation does not affect the conclusion drawn from this paper. As shown in Fig. 3(b), the current ratio of the state after writing to the state before writing is ~50 and ~200 for the writing time of 1 μs and 1 ms, respectively. This indicates that even a short writing pulse of 1 μs can produce a memory state well distinct from the state before writing. As can be observed from Fig. 3(b), the current has a power-law dependence on the writing time t, i.e., $I \sim t^{0.20}$. The power-law behavior is due to the power-law dependence of the charge trapping on the charge injection time. A power-law dependence of the charge trapping on the charge injection time has been experimentally observed. Fig. 4 shows the equivalent trapped charge per unit area ΔQ at the oxide/Si interface determined from the flat-band voltage shifts in the C–V measurements as a function of the writing time (i.e., the charge injection time). The trapped charge density has a power-law dependence on the writing time, i.e., $\Delta Q \sim t^{0.19}$, which is similar to the power-law dependence of the reverse current on the writing time. It is worthy to mention that a power-law dependence of the charge trapping on the charge injection time is usually observed in the gate oxide of a MOS structure [12], [13].

Fig. 5 shows the retention characteristics of the WORM devices. The reading operation (i.e., the reverse-current measurement) is carried out at +2 V. Within the time limit of 3×10^4 s in our experiment, the state before writing and the state after writhing at different writing voltages (−15 V and −25 V) for different writing time (1 μs and 1 ms) do not show a significant degradation with time. This indicates that there is no significant loss of the trapped charges and the reading operation at +2 V itself does not cause a significant change in the charge trapping within the time limit also.

In the discussion in Fig. 1(b), it has been pointed out that the negative charging voltage of −15 V produces a large increase

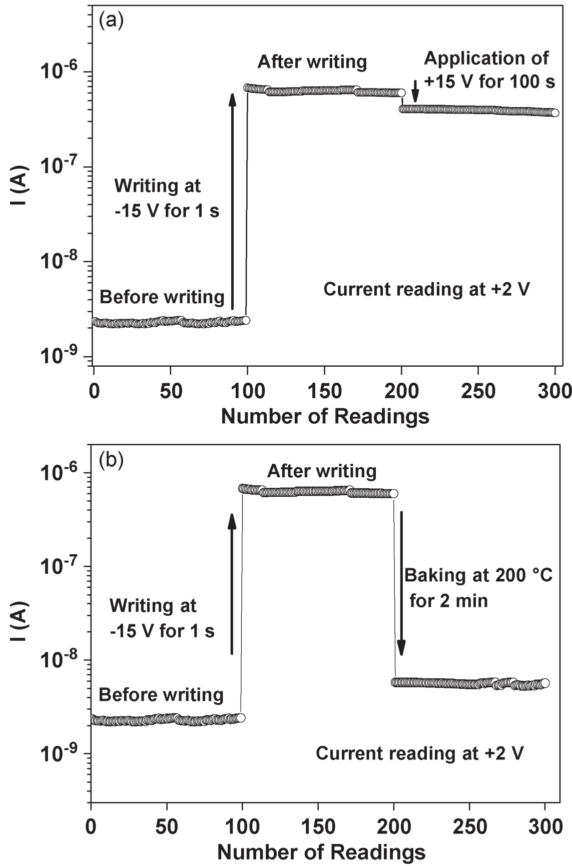

Fig. 6. Changes of a written state by (a) the application of +15 V for 100 s or (b) baking at 200 °C for 2 min.

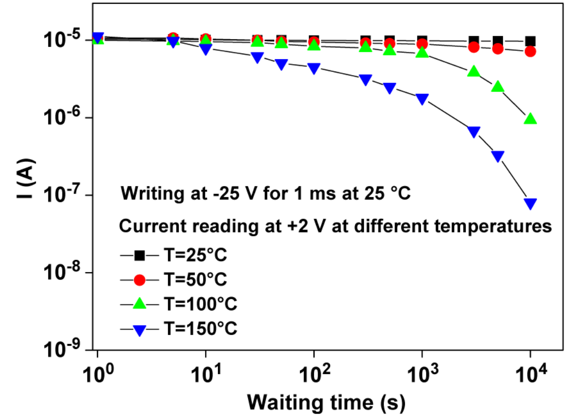

Fig. 7. Retention behaviors at various temperatures.

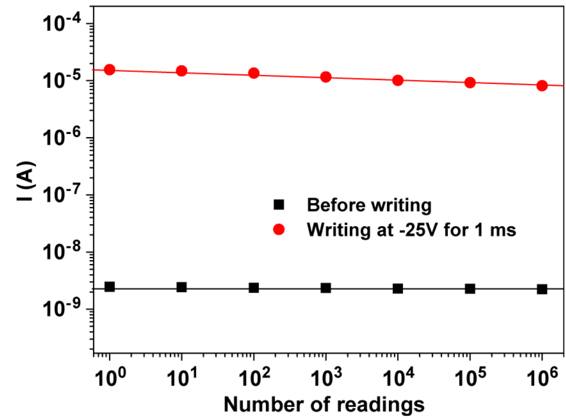

Fig. 8. Measurement of the READ endurance at room temperature. Two-volt READ pulses with a 1-ms pulsewidth are used in the measurement.

in the reverse current but the positive charging voltage of +15 V causes only a small reduction in the current. This means that a written state cannot be easily reverted by a positive charging voltage. This is confirmed by experiment. As shown in Fig. 6(a), the state written at −15 V for 1 ms does not revert to the state before writing after the application of +15 V for 100 s. This also explains why the reading operation at +2 V does not significantly change the memory states as discussed above. However, the baking of the charged device at 200 °C for 2 min leads to a reversion of the written state to the state before writing, as shown in Fig. 6(b). This indicates that most of the trapped charges associated with the writing process are released from the trap centers after baking. Note that the memory cell can be written again after baking. The release of the trapped charges at an elevated temperature will of course affect the retention performance of the WORM device. Fig. 7 shows the retention behaviors at various baking temperatures for the memory state written at −25 V for 1 ms. As shown in the figure, the retention performance is excellent at room temperature. It is still good at 50 °C for practical application, e.g., the current ratio of the state after writing to the state before writing is still larger than 5×10^3 after a waiting time of 10^4 s. However, the retention performance significantly degrades at a higher temperature. This means that the WORM device is not suitable for those applications at high temperatures (e.g., > 50 °C), which is the limitation of the device. As the memory states are determined by the charge trapping in the oxide layer, their retention performance could be highly sensitive to the temperature, depending on the trap depth. The thermal detrapping process is enhanced when the temperature is increased, leading to a more-significant loss of the trapped charges [14]. This explains the significant degradation of the retention performance at an elevated temperature. On the other hand, the release of trapped charges at a high temperature suggests that the WORM device can be erased by baking at a sufficiently high temperature for reprogramming. This has been confirmed by experiment. The reversion of the written state to the state before writing by baking at 200 °C for 2 min, as shown in Fig. 6(b), indicates that most of the trapped charges associated with the written state have been released by the thermal detrapping process during baking. In addition to the retention performance, the READ endurance of the WORM device has been also examined, and the result is shown in Fig. 8. As shown in the figure, after 10^6 readings, there is no significant degradation in the state before writing, and there is only a small decrease in the current of the state after writing, showing a good READ endurance. The current decrease in the state after writing is due to the charge release during the waiting period of the endurance experiment and/or is caused by the reading operations.

IV. Summary

In summary, the reverse current of the Al/Al-rich Al_2O_3/p-Si diode can be modulated by the charge trapping

in the oxide layer, and this effect can be used to realize the WORM memory. A written state can be achieved by applying a negative charging voltage to the gate of the diode, and memory states can be distinguished by detecting the reverse diode current at a small positive voltage. The memory exhibits good reading endurance and retention characteristics.

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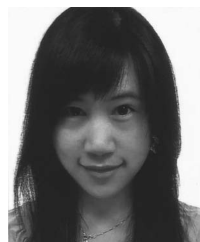

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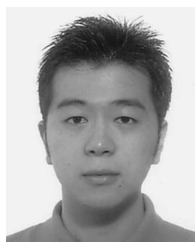
Dr. Liu was a recipient of the prestigious two-year Singapore Millennium Foundation Fellowship in 2006.



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