Impacts of Ti Content and Annealing Temperature on Electrical Properties of Si MOS Capacitors with HfTiON Gate Dielectric

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Abstract - HfTiON gate dielectric is fabricated by reactive co-sputtering method followed by annealing in N_2 ambient. The effects of Ti content and annealing temperature on the performances of HfTiON gate-dielectric Si MOS devices are investigated. Experimental results indicate that gate capacitance is increased with increasing Ti content. However, when the Ti/Hf ratio exceeds ~1.75, increase of the gate capacitance becomes small. Surface roughness of the samples annealed at different temperatures is analyzed by AFM, and results show that high annealing temperature (e.g. 700 ℃ for 30 s) can produce smooth surface, thus resulting in low gate leakage current.
Keywords: MOS capacitor, high-k dielectric, HfTiON

I. INTRODUCTION

High-k gate dielectrics, such as HfO_2 [1, 2], ZrO_2 [3, 4], and LaO [5, 6], have been widely investigated as the potential replacement of SiO_2 for the forthcoming CMOS technology. Among various high-k candidates, HfO_2 receive more and more attention due to acceptable thermodynamic stability on Si surface [7] and relatively large bandgap (5.68 eV). However, its low crystallization temperature (~520℃ [8]) restricts the post-deposition annealing which is important for avoiding high gate leakage current. It has been reported that the crystallization temperature can be increased through incorporating N into high-k films [9]. In addition, the reported relative permittivity of HfO_2 and HfON is below 24, which limits further scaling of equivalent oxide thickness (EOT). Incorporation of Ti, whose oxide has a high k of 50 ~ 80 due to strong contribution from soft phonons [10, 11], is a possible approach to further increase the permittivity of hafnium-based oxides. However, as Ti content increases, the interface quality gradually deteriorates, resulting in an increase of gate leakage current due to the reaction between Ti and Si substrate [12]. In this work, influences of Ti content in HfTiON film and post-deposition annealing (PDA) temperature on the electrical properties of MOS capacitor with HfTiON as gate dielectric are investigated, and suitable Ti content and annealing temperature are obtained by considering the interface quality and gate leakage properties.

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II. EXEREMENTS

MOS capacitors were fabricated on (100)-oriented n-type Si wafers. After the wafers were cleaned, they were dipped in diluted hydrofluoric for 60 s to remove natural oxide. Then, the Si wafers were immediately transferred to the vacuum chamber of a sputtering system. The HfTiN films with approximately same thickness were first deposited at room temperature by co-sputtering of Hf target at a RF power of 25 W and Ti target at different DC powers of 16.5 W, 26.4 W, 33 W and 39.6 W (corresponding monitoring DC power is 13W, 22W, 28.5 W and 35.5 W respectively) in an Ar/N_2 = 24/6 ambient (denoted as P1, P2, P3 and P4 samples respectively). The ratio of Ti/Hf was calculated according to the deposition rates of TiN and HfN films, and listed in Table I. The PDA was performed in N_2 (500 ml/min) at 700 ℃ for 60 s to oxidize the HfTiN films by consuming the residual oxygen in the N_2 ambient and annealing system. Then, Al was thermally evaporated and patterned using lithography technology as the gate electrode. Also, Al was evaporated as the back electrode of the MOS capacitors to decrease contact resistance. Finally, a forming-gas annealing was carried out at 400 ℃ for 25 min in N_2/H_2 = 95/5. After analyzing the accumulation capacitances and leakage current of the samples, Ti target power of 33 W was determined to be suitable since both reasonable k value and acceptable gate leakage current can be obtained. Furthermore, influences of annealing temperature on the electrical properties of the sample prepared using Ti target DC power of 33 W were investigated, and a suitable annealing temperature of 700℃ for 30 s was found.

TABLE I
PREPARATION CONDITIONS FOR SAMPLES WITH DIFFERENT Ti CONTENTS

Sample	P1	P2	P3	P4
Ti-target power / W	16.5	26.4	33	39.6
Ti/Hf	0.43	0.85	1.75	2.83

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High-frequency accumulation capacitance (HF, 1 MHz) and gate leakage current were measured at room temperature, and under light-tight and electrically shielded conditions. High-resolution transmission electron microscopy (TEM) was used to observe the cross section of the HfTiON/Si system, thus getting the physical thickness of the film and calculating equivalent oxide thickness (EOT). Surface roughness was evaluated using atomic force microscope (AFM).

III. RESULTS AND DISCUSSION

The HF accumulation capacitance C_{ox} of the samples is shown in Fig. 1. As can be seen, as Ti target power increases, C_{ox} is increased, which should be ascribed to the increase of k value due to Ti incorporation. Also, it can be noted that the C_{ox} difference between the P3 and P4 samples is smaller than that between P2 and P3, indicating a gradual saturation trend of k-value increase with Ti content, because the dielectric is closer to Ti-based oxide (TiO_2: k = ~50) for high Ti content. A small difference of C_{ox} between the P1 and P2 samples is also observed because the dielectric with low Ti content behaves more like Hf-based oxide (k = 18 ~ 20) [12].

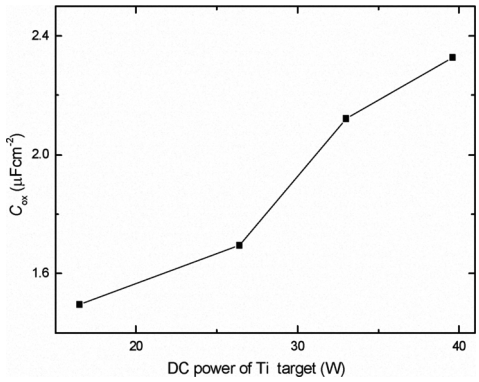

Fig.1 Dependence of C_{ox} on Ti content

Gate leakage current density of the samples is shown in Fig. 2. Obviously, the higher the Ti content, the larger is the gate leakage current. This is because with more Ti incorporation, more reaction between Ti and Si could happen during PDA, resulting in rougher interface [12].

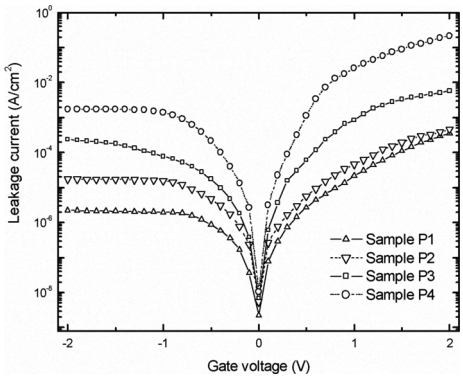

Fig. 2 Gate leakage current density versus gate voltage for MOS capacitors with different Ti contents

From Fig. 2, it can be seen that gate leakage current density of the P3 sample at V_g = 1 V is ≤ 10^{-3} Acm^2.

Based on the above discussion, a Ti/Hf ratio of 1.75 (Ti-target DC power of 33 W) could be considered as a suitable option.

Furthermore, the electrical properties of the P3 sample are investigated by annealing it at different temperatures of 650 ℃, 700 ℃, 750 ℃, and 800 ℃ respectively (denoted as T1, T2, T3 and T4 samples respectively). The extracted C_{ox}'s are shown in Fig 3. It is found that the higher the annealing temperature, the smaller the C_{ox} is. This is probably resulted from the growth of a HfTiSiON interlayer with smaller k value than HfTiON due to interdiffusions between the layers [12] during PDA, as shown by the TEM image of the T2 sample in Fig.4, with a ~1.2-nm interlayer.

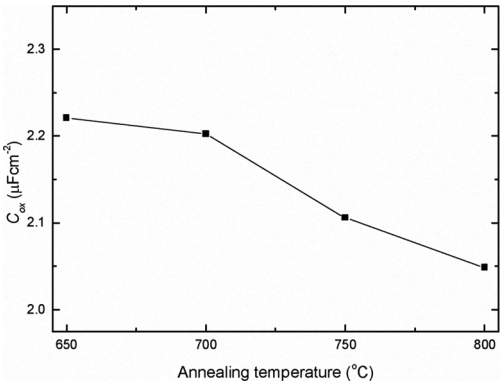

Fig. 3 C_{ox} of the samples as a function of PDA temperature

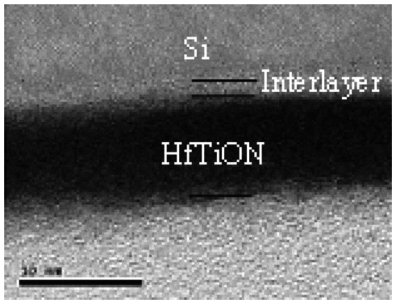

Fig.4 TEM image of the T2 sample annealed at 700 ^{0}C for 30 s

On the other hand, the gate leakage current is impacted by the roughness of the dielectric/gate interface [13] and denseness of the films. The surface roughness of the HfTiON films with different PDA temperatures is evaluated by means of AFM, as shown in Fig. 5, and extracted surface roughness is shown in Fig. 6. It can be seen that the surface roughness is decreased as PDA temperature increases, because higher PDA temperature could result in denser HfTiON film. Also, reduction of the roughness is large from 650 ^{0}C to 700 ^{0}C, and becomes small from 700 ^{0}C to 800 ^{0}C, implying that 700 ^{0}C should be high enough for densifying the film. The gate leakage current density of MOS capacitors with different PDA temperatures is shown in Fig. 7. Low gate

leakage current is observed for the samples with high PDA temperatures, in good correlations with their small surface roughness, high denseness of the HfTiON film and small interlayer thickness. Therefore, by considering both C_{ox} value and gate leakage current, the suitable annealing condition is 700 ^{0}C for 30 s.

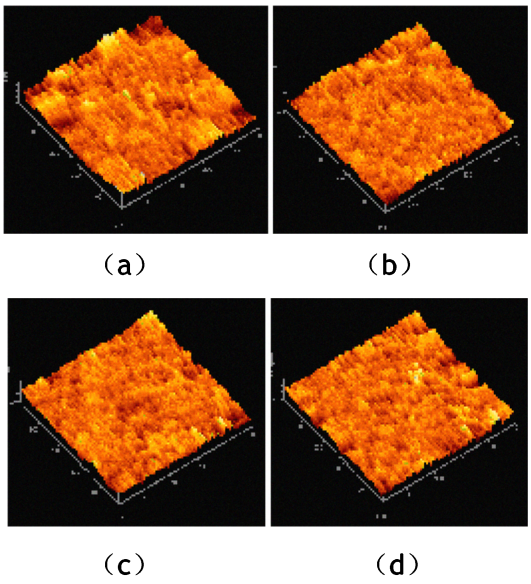

Fig.5 AFM images (0.5 × 0.5 μm^2) of the samples prepared using Ti target power of 33 W with different PDA temperatures of 650 ℃ (a), 700 ℃ (b), 750 ℃ (c), and 800 ℃ (d) respectively.

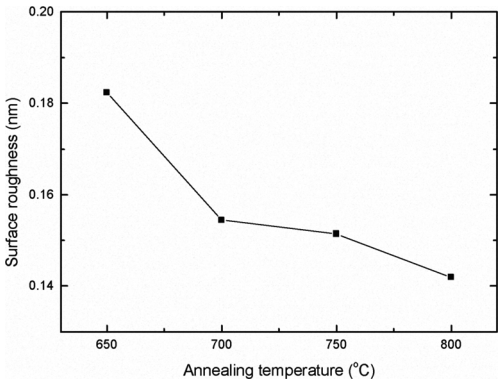

Fig.6 Surface roughness of the samples with different PDA temperatures

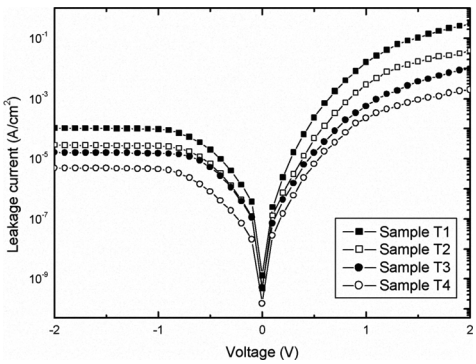

Fig. 7 Gate leakage current density of MOS capacitors with different PDA temperatures

IV. Conclusion

HfTiON films with different Ti contents and PDA temperatures have been prepared by reactive co-sputtering of Hf and Ti targets. Experimental results show that high Ti content contributes to large gate capacitance due to increased k value of the HfTiON film, but however, the interface properties become poor with increase of Ti content. As a trade-off between k value and interface-state density, a Ti/Hf ratio of 1.75 is suitable in our study. On the other hand, the effects of the PDA temperature on the interlayer growth, surface roughness and thus gate leakage properties have been investigated. It is found that as the annealing temperature increases, k value is reduced due to thicker interlayer, and gate leakage current is decreased due to enhanced denseness of the film with smaller surface roughness. In order to obtain large gate capacitance and simultaneously maintain low gate leakage, the suitable PDA condition is 700℃ for 30 s in N_2 ambient for Si MOS devices with HfTiON as gate dielectric.

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