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Author(s)	Liu, YR; Deng, LF; Yao, RH; Lai, PT
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Low-Operating-Voltage Polymer Thin-Film Transistors Based on Poly(3-Hexylthiophene) With Hafnium Oxide as the Gate Dielectric

Y. R. Liu, L. F. Deng, R. H. Yao, and P. T. Lai, *Senior Member, IEEE*

***Abstract*—The effects of hafnium oxide (HfO_2) gate dielectric annealing treatment in oxygen (O_2) and ammonia (NH_3) ambient on the electrical performance of polymer thin-film transistors (PTFTs) based on poly(3-hexylthiophene) are investigated. The PTFTs with HfO_2 gate dielectric and also octadecyltrichlorosilane surface modification, prepared by spin-coating process, exhibit good performance, such as a small threshold voltage of -0.5 V and an operating voltage as low as -4 V. Results indicate that the PTFT with NH_3-annealed HfO_2 shows higher carrier mobility, larger ON/OFF current ratio, smaller subthreshold swing, and lower threshold voltage than the PTFT with O_2-annealed HfO_2. Capacitance–voltage analysis for metal-polymer-oxide-silicon structures indicates that the better electrical performance of the PTFT with NH_3-annealed HfO_2 is attributed to improved dielectric/polymer interface and reduced series resistance in the transistor.**

***Index Terms*—Capacitance–voltage characteristics, high-k, poly(3-hexylthiophene) (P3HT), polymer thin-film transistor (PTFT).**

I. Introduction

In THE last two decades, solution-processed polymer thin-film transistors (PTFTs) have attracted much attention due to their potential applications in a variety of large-area electronic applications, such as flat-panel display, low-cost flexible integrated circuits, and sensors [1]–[3]. Among various solution-processed polymer semiconductors that are currently in use, poly(3-hexylthiophene) (P3HT) has been the most extensively studied p-type polymer material due to its relative high carrier mobility [4], [5]. So far, many researches of P3HT PTFTs have been focusing on the enhancement of field-effect mobility and the improvement of air stability by material and device engineering [6], [7]. Moreover, most of the studies on P3HT PTFTs were done by using silicon dioxide (SiO_2) as gate dielectric [8]–[10]. However, conventional PTFTs require a high operating voltage and show a large threshold voltage and a poor subthreshold swing (SS), which limit their suitability in integrated-circuit applications. In addition, high operating voltage usually leads to high power consumption and causes inconvenience to the development of portable equipment. In order to address these issues, high-k gate dielectrics [e.g., tantalum pentoxide (Ta_2O_5)] have been applied in PTFTs to obtain a higher drive current at lower voltage operation [11], [12]. Hafnium-based oxides [e.g., HfO_2 and hafnium oxynitride (HfON)] are being actively investigated to act as the gate dielectric of inorganic transistors due to their better interface quality with the silicon semiconductor [13], [14] as well as higher dielectric constant. The performance of PTFTs depends particularly on the quality of the interface between the gate dielectric and polymer semiconductor, as well as the electrical properties of the polymer semiconductor thin film. In order to decrease the gate-oxide leakage and acquire high-quality interface, one common method is performing a proper passivation treatment on the gate dielectric prior to spin-coating the polymer semiconductor layer. In this paper, in order to realize a low operating voltage and a small threshold voltage, HfO_2 dielectric layer prepared by sputtering method and then annealing in O_2 or NH_3 is applied to form the gate dielectric of the P3HT PTFT. I–V characteristic measurements are performed to characterize the electrical performance of the devices, such as field-effect carrier mobility, threshold voltage, SS, and ON/OFF current ratio. Capacitance–voltage analysis for a metal-polymer-oxide-silicon (MPOS) structure is presented to explain the difference in the electrical properties of the P3HT PTFTs with O_2-annealed or NH_3-annealed HfO_2 gate dielectric.

II. Experimental Details

The PTFTs based on P3HT were fabricated using a bottom-gate top-contact configuration. The cross sections of the PTFT and MPOS structure are shown in Fig. 1. N-type $\langle 100 \rangle$ silicon wafers with a resistivity of 0.2–0.5 $\Omega \cdot$ cm acted as substrate and gate electrode. They were first cleaned according to the standard RCA method, and then, 10% hydrofluoric acid was used to remove the native SiO_2 layer. After cleaning, HfO_2 gate dielectric was deposited onto the wafers by radio frequency (RF) sputtering (Denton Vacuum LLC Discovery 635) at room temperature. RF power and Ar gas flow rate were kept at 30 W and 24 sccm, respectively, at a deposition pressure of 3.5 mbar. Before the deposition, the vacuum in the chamber was

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Y. R. Liu and R. H. Yao are with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510640, China (e-mail: phlyr@scut.edu.cn; phrhyao@scut.edu.cn).

L. F. Deng and P. T. Lai are with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong (e-mail: lfdeng@eee.hku.hk; laip@eee.hku.hk).

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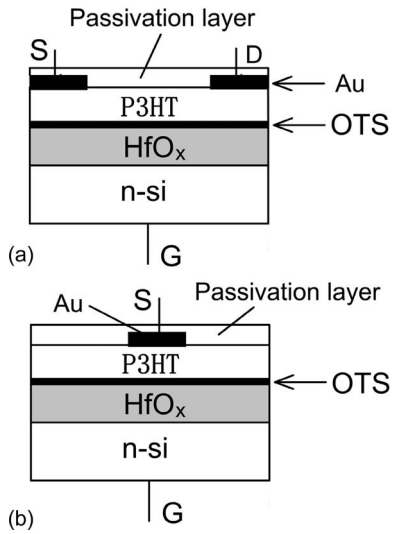

Fig. 1. Schematic diagrams of the (a) PTFT and (b) MPOS structure.

kept below 2×10^{-6} torr. The material of the target was HfO_2. Subsequently, the samples were divided into two groups, each annealed in O_2 and NH_3, respectively, at 400 °C for 20 min. Hydrofluoric acid with 20% concentration was used to remove the back oxide of the silicon substrate. To improve the interfacial characteristics, all samples were pretreated with a 0.1-ml/ml octadecyltrichlorosilane (OTS) solution in toluene to grow a self-assembling monolayer of OTS by spin coating, and then, the samples were baked in the oven at 90 °C for 10 min. Subsequently, a 10-mg/ml solution of P3HT in chloroform was spin-coated as the semiconducting active layer on the HfO_2 layer at a spin speed of 2000 r/min for 60 s in air. The P3HT obtained from Aldrich was 95% head-to-tail regioregular and 99.995% trace metal basis and used without any additional purification. The molecular weight of P3HT was about 25 000. The P3HT film was then annealed at 90 °C in air for 5 min. Finally, gold was evaporated on the P3HT layer through a shadow mask to form the drain and source electrodes. In order to avoid the performance degradation of the polymer semiconductor due to air exposure, a thin solid paraffin was dissolved to form a thin passivation layer at 80 °C. The shadow mask defined the channel lengths (L) and widths (W) as 30 and 800 μm, respectively.

The thickness of the HfO_2 layer was measured to be 20 nm by ellipsometry. The thickness of the polymer thin film was determined to be 85 nm by surface profilometry. The electrical characteristics of the PTFT devices and MPOS structures were measured in a light-shielded box without gas protection at room temperature by using an Agilent 4156C semiconductor parameter analyzer and a conventional LCR meter (Agilent 4284A), respectively, combined with a probe station. The conventional field-effect transistor model in the saturation regime was used to extract the field-effect mobility (μ) and threshold voltage $(V_{\rm th})$ of the devices, i.e., using the following equation:

$$I_{D,\rm sat} = \frac{W}{2L}\mu C_i (V_{\rm GS} - V_{\rm th})^2 \tag{1}$$

where $I_{D,\rm Sat}$ is the saturation current, C_i is the capacitance of the gate dielectric per unit area, and $V_{\rm GS}$ is the applied gate voltage. The ON/OFF current ratio and the SS were also extracted from the transfer characteristic curves.

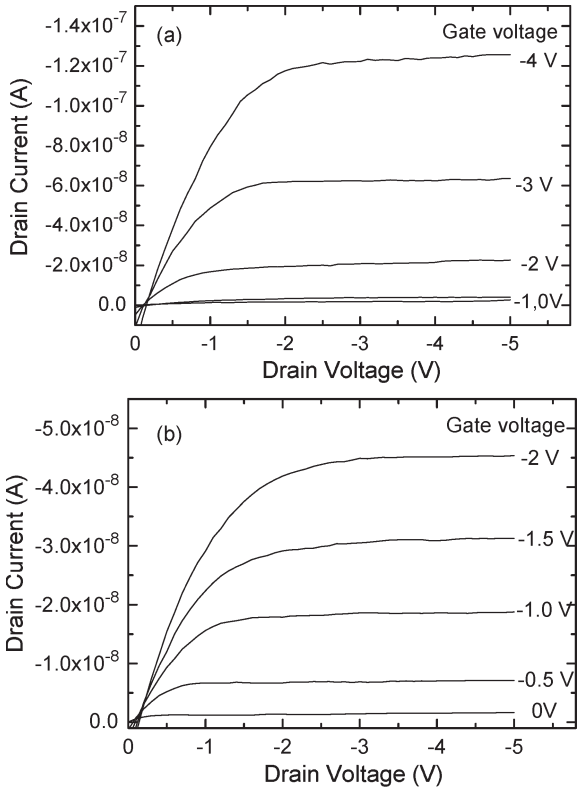

Fig. 2. Output characteristic curves of PTFTs with HfO_2 gate dielectric annealed in (a) O_2 and (b) NH_3 for variable gate voltages.

III. Results and Discussion

Fig. 2 shows the output characteristics of the PTFTs with O_2-annealed and NH_3-annealed HfO_2 as gate dielectric. The two devices show good saturation behavior at low operating voltages ($V_{\rm GS} = 0$ to -5 V). For the O_2-annealed device, a drain current of 20 nA can be achieved in the saturation region for a gate voltage of -2 V, while for the NH_3-annealed device, a larger drain current of 45 nA can be achieved in the saturation region for the same gate-bias voltage. Fig. 3 shows the transfer characteristics of the two PTFTs. By utilizing (1), the field-effect mobility of the PTFTs can be deduced from the plot of $I_D^{1/2}$ versus $V_{\rm GS}$ according to the following equation:

$$\mu = \frac{2LB^2}{WC_i} \tag{2}$$

where $B = \partial(I_D)^{1/2}/\partial V_{\rm GS}$ is the slope of the $I_D^{1/2}$ versus $V_{\rm GS}$ plot. According to (2), for the O_2-annealed device, the field-effect mobility calculated from Fig. 3 is 4.3×10^{-3} cm^2/V $\cdot$ s in the saturation region for a drain voltage of -4 V, while for the NH_3-annealed one, the field-effect mobility calculated from Fig. 3 is 6.2×10^{-3} cm^2/V $\cdot$ s in the saturation region for the same drain voltage. From Fig. 3, the threshold voltage is deduced to be -1.0 and -0.5 V for the O_2- and NH_3-annealed devices, respectively. The parameters of the two devices extracted from their transfer characteristics are summarized in

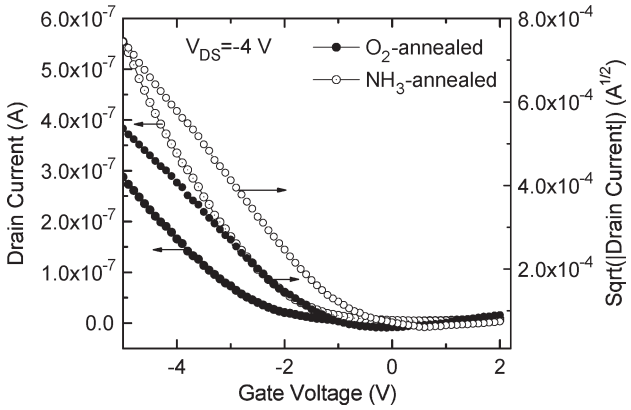

Fig. 3. Transfer characteristic curves of PTFTs with HfO_2 gate dielectric annealed in O_2 and NH_3 at a drain voltage of -4 V.

TABLE I
SUMMARIZED DEVICE PARAMETERS OF THE P3HT PFETS WITH O_2-ANNEALED HfO_2 AND NH_3-ANNEALED HfO_2. t_{ox}, ε_i, μ, V_{th}, SS, AND I_{on}/I_{off} REPRESENT THE DIELECTRIC THICKNESS, RELATIVE DIELECTRIC CONSTANT, FIELD EFFECT MOBILITY, THRESHOLD VOLTAGE, SUBTHRESHOLD SWING, AND THE ON/OFF CURRENT RATIO, RESPECTIVELY

Treatment condition	O_2-annealed	NH_3-annealed
t_{ox} (nm)	20	19.5
C_i (nF/cm^2)	280	332
ε_i	6.3	7.3
μ ($\times 10^{-3}$ cm^2/V s)	4.3	6.2
V_{th} (V)	-1.0	-0.5
SS (V/decade)	1.8	1.7
I_{on}/I_{off}	80	150

Table I. Compared with the O_2-annealed device, the NH_3-annealed device presents better electrical performance, such as higher field-effect mobility, larger ON/OFF current ratio, reduced threshold voltage, and smaller SS.

To identify the origin of the differences in the electrical properties of the two P3HT PTFTs, capacitance–voltage measurements are made to analyze the properties of the MPOS structures with O_2-annealed HfO_2 and NH_3-annealed HfO_2, particularly the difference of trapped charges in the bulk semiconductor and at the insulator/semiconductor interface. Fig. 4 shows the capacitance and equivalent parallel conductance measured at 1 MHz as a function of gate bias for the MPOS structures with O_2-annealed HfO_2 and NH_3-annealed HfO_2. For the O_2-annealed device, the absence of a peak in the conductance–voltage $(G-V)$ curve [Fig. 4(a)] means that series resistance (R_s) produces the dominant loss, completely masking the interface-trap loss. On the other hand, a clear peak in the $G-V$ curve is shown in Fig. 4(b) for the NH_3-annealed device, indicating that there is a small series resistance in the MPOS structure. The series resistance can be expressed as [15]

$$R_s = \frac{G_{\rm ma}}{G_{\rm ma}^2 + \omega^2 C_{\rm ma}^2} \tag{3}$$

where $G_{\rm ma}$ and $C_{\rm ma}$ are the equivalent parallel conductance and the capacitance when the MPOS structure is biased into strong accumulation. According to (3), the series resistances

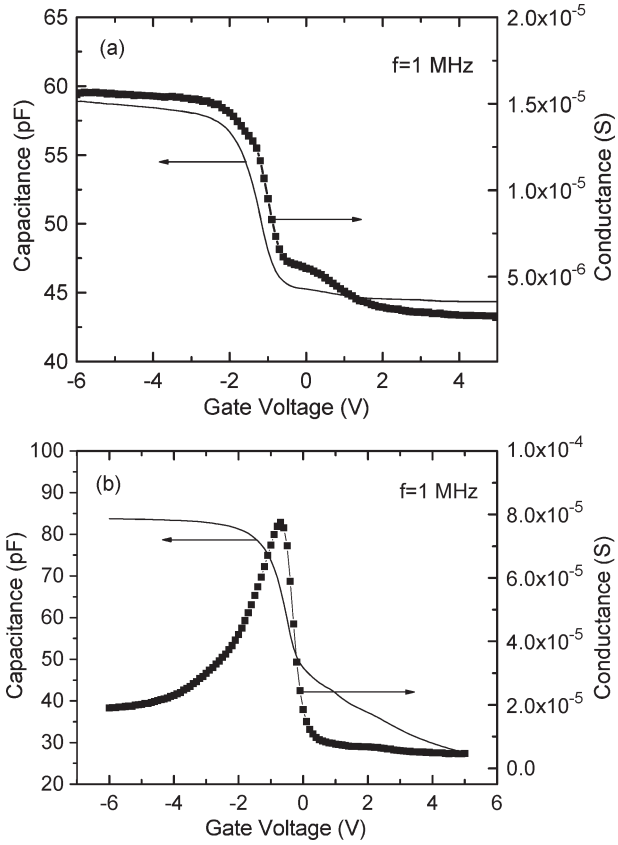

Fig. 4. Capacitance and equivalent parallel conductance measured at 1 MHz as a function of gate bias for the MPOS structures with (a) O_2-annealed HfO_2 and (b) NH_3-annealed HfO_2. Gate area is 2.5×10^{-4} cm^{-2}.

extracted from the $G-V$ and C–V curves in Fig. 4(a) and (b) are 210.1 and 68.6 Ω, respectively. Here, the smaller series resistance in the MPOS structure with NH_3-annealed HfO_2 is mainly attributed to the smaller contact resistance between metal and polymer or smaller bulk resistance between the back contact to the polymer and the depletion layer edge underneath the gate, because a larger current can be obtained between source and drain electrodes when the gate electrode is open.

Fig. 5 shows the C–V hysteresis curves of the MPOS structures with O_2-annealed HfO_2 and NH_3-annealed HfO_2 for two test frequencies. For the O_2-annealed sample, the frequency dependence of the capacitance is observed obviously, i.e., the capacitance decreasing with increasing test frequency in the accumulation region, which is due to long relaxation time for the polymer semiconductor bulk [16] or charge trapping in the states at the polymer/dielectric interface [17]. In addition, the C–V curve in Fig. 5(a) shows a clear kink in the depletion region for the sweep direction from accumulation to depletion, and the kink effect becomes more obvious as the test frequency decreases. However, the kink effect disappears for the opposite sweep direction from depletion to accumulation, indicating that the kink effect originates from the trap effect of majority carriers (holes) at the dielectric/polymer interface or within the polymer bulk. However, for the NH_3-annealed sample, the capacitance of the MPOS structure in accumulation region does not depend on the test frequency, indicating that the trap

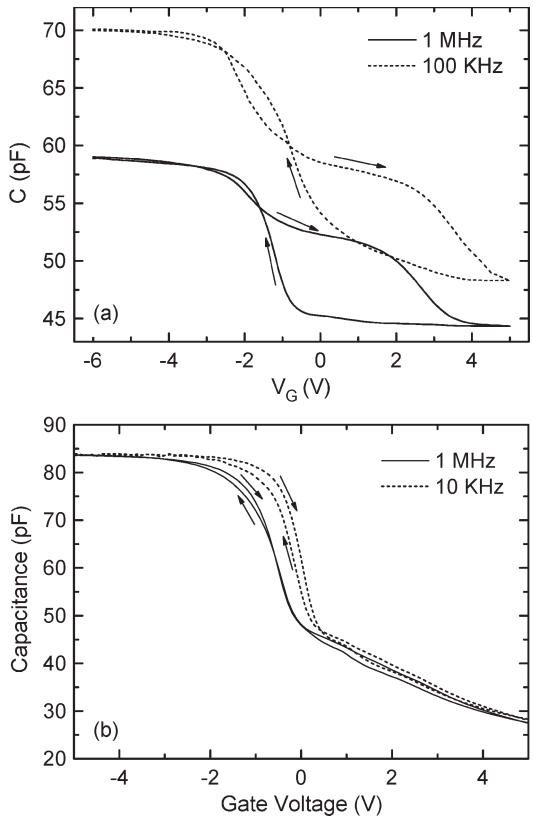

Fig. 5. C–V hysteresis curves of the MPOS structures with (a) O_2-annealed HfO_2 and (b) NH_3-annealed HfO_2 for various frequencies. The arrows indicate the sweep direction of the gate-bias voltage.

states at the interface or in the bulk of the polymer in the MPOS structure with NH_3-annealed HfO_2 are less than those in the O_2-annealed counterpart. Moreover, a slight hysteresis can be observed, and the hysteresis effect becomes larger with the decrease of the test frequency. Normally, the hysteresis is mainly associated with charge trapping at the P3HT/HfO_2 interface. The interface trap state density can be estimated by

$$N_t = \frac{C_i \Delta V}{q} \tag{4}$$

where q is the electronic charge, C_i is the capacitance per unit area of the dielectric layer, and ΔV is the flatband voltage shift in the C–V hysteresis curves. According to (4), the interface trap state density can be estimated as 7.0×10^{12} cm^{-2} at a frequency of 100 kHz for the O_2-annealed sample, while the value is 4.2×10^{11} cm^{-2} at a frequency of 10 kHz for the NH_3-annealed sample. Based on the aforementioned analysis of the electrical characteristics for the two MPOS structures, it can be deduced that the better electrical performance of the PTFT with NH_3-annealed HfO_2 should be due to lower trap states at the interface or in the bulk of the polymer and smaller series resistance in the transistor.

IV. Conclusion

We have investigated P3HT PTFTs with HfO_2 as gate dielectric, which is deposited by RF sputtering and then annealed at 400 °C in O_2 and NH_3, respectively. Both PTFTs show a small threshold voltage and a low operating voltage, arising from the high gate capacitance per unit area of the HfO_2 gate dielectric. Compared with the PTFT with O_2-annealed HfO_2, the PTFT with NH_3-annealed HfO_2 displays higher carrier mobility, larger ON/OFF current ratio, lower threshold voltage, and smaller SS due to reductions of interface trap states and series resistance in the transistor. The results suggest that the PTFT is suitable for low-voltage and low-power applications in organic electronics.

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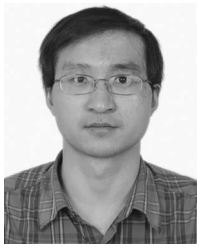
Y. R. Liu received the B.S. degree in semiconductor physics from Jiangxi University, Ganzhou, China, in 1991, the M.Sc. degree in condensed physics from Sichuan University, Sichuan, China, in 1996, and the Ph.D. degrees in microelectronics and solid state electronics from South China University of Technology, Guangzhou, China, in 2007.

He is currently an Associate Professor with the School of Electronic and Information Engineering, South China University of Technology. His current research interests include inorganic/organic thin-film transistors, solar cells, and microsensors.



L. F. Deng received the B.S. degree in applied physics from Hefei University of Technology, Hefei, China, in 2003 and the M.Sc. degree in microelectronics from Huazhong University of Science and Technology, Wuhan, China, in 2007. He is currently working toward the Ph.D. degree in the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong.

His current research concentrates on organic thin-film transistors.

R. H. Yao received the B.S. degree in sciences from Sun Yat-Sen University, Kaohsiung, Taiwan, in 1982 and the Ph.D. degree from the Chinese Academy of Sciences, Beijing, China, in 2004.

He was previously a Professor with the Department of Physics and the Dean of the School of Sciences, Shantou University, Shantou, China. Since 2002, he has been a Professor with the Institute of Microelectronics, South China University of Technology, Guangzhou, China, where he is currently the Vice-Dean of the School of Electronic and Information Engineering. He has published well over 100 papers to journals and international conferences and is the holder of four patents. His current research interests include semiconductor device and microelectronics techniques.

P. T. Lai (M'90–SM'04) received the B.Sc.(Eng.) and Ph.D. degrees from The University of Hong Kong, Hong Kong. His Ph.D. research was on the design of small-sized MOS transistor with emphasis on narrow-channel effects. The work involved the development of both analytical and numerical models, the study of this effect in relation to different isolation structures, and the development of efficient numerical algorithms for device simulation.

He was a Postdoctoral Fellow with the University of Toronto, Toronto, ON, Canada. He has proposed and implemented a novel self-aligned structure for bipolar transistor and designed and implemented an advanced polyemitter bipolar process with emphasis on self-alignment and trench isolation. He is currently a Professor with the Department of Electrical and Electronic Engineering, The University of Hong Kong. His current research interests are on thin gate dielectrics for FET devices based on Si, SiC, GaN, Ge, and organics and on microsensors for detecting gases, heat, light, and flow.