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Wide-bandgap high-*k* Y₂O₃ as passivating interlayer for enhancing the electrical properties and high-field reliability of *n*-Ge metal-oxide-semiconductor capacitors with high-*k* HfTiO gate dielectric

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High-*k* and wide-bandgap Y_2O_3 was proposed as an interlayer in *n*-Ge metal-oxide-semiconductor (MOS) capacitor with HfTiO gate dielectric for passivating its dielectric/Ge interface, and thus improving its electrical properties and high-field reliability. Results showed that as compared to the Ge MOS capacitor with HfTiO dielectric, the sample with HfTiO/Y_2O_3 dielectric had better electrical properties such as higher dielectric constant ($k=24.4$), lower interface-state density, and less frequency-dependent *C-V* dispersion, and also better reliability with less increases in gate leakage and interface states after high-field stressing. This should be attributed to the excellent interfacial quality of Y_2O_3/Ge with no appreciable growth of unstable GeO_x at the interface as confirmed by transmission electron microscopy. Moreover, Y_2O_3 can also act as a barrier against the diffusions of Ge, Hf, and Ti, thus further improving the interface quality. *© 2009 American Institute of Physics*. [DOI: 10.1063/1.3182741]

High-mobility semiconductor materials such as Ge and SiGe were studied to keep scaling down the size and increase the operating speed of metal-oxide-semiconductor field-effect transistors (MOSFETs). Although Ge MOSFETs with high-*k* gate dielectrics have been successfully demonstrated,[1–3] the quality of high-*k* dielectric/Ge interface is worse than that of the SiO_2/Si interface, mainly attributed to the parasitically grown unstable Ge oxide (GeO_x) interfacial layer. In order to achieve high-quality Ge MOS devices, different surface passivation methods were researched by using dielectrics such as GeO_xN_y,[1–3] AlO_xN_y,[4] CeO_2,[5] La_2O_3,[6] and TaO_xN_y.[7] Although GeO_xN_y and AlO_xN_y interlayers were reported to improve device quality,[1–3] they might not sufficiently passivate the Ge surface,[4] and also had a low *k* value (~6 for GeO_xN_y and ~9 for AlO_xN_y), which limits further scaling possibility. TaO_xN_y[7] was also demonstrated as an efficient interlayer for Ge MOS devices, but with a small bandgap of 4.4 eV, it suffered from large leakage current. More recently, rare-earth oxides as CeO_2 and La_2O_3 were studied as the interlayer for Ge MOS capacitors. However, CeO_2 had a small bandgap of 3.3 eV, which produced large gate leakage.[5] Also, La_2O_3 absorbed moisture,[8] which caused reliability problems. On the other hand, Y_2O_3 was a suitable candidate for the gate dielectric of Si MOS devices due to its relatively high dielectric constant (~14–18), high crystallization temperature (~2325 °C) and wide bandgap (~5.5 eV).[9,10] In this work, Y_2O_3 was proposed as the interlayer between high-*k* HfTiO gate dielectric and Ge substrate to fabricate *n*-Ge MOS devices with a stacked gate dielectric of HfTiO/Y_2O_3 for the purposes of both larger *k* value and better interface properties. Due to lack of reports on the reliability issues of Ge MOS capacitors, high-field reliability was also measured for the *n*-Ge MOS capacitors in this work.

Germanium MOS capacitors were fabricated on (100) *n*-type substrate with a resistivity of 0.040–0.047 Ω cm. The wafers were cleaned in organic solvent followed by a rinse in 2% HF and de-ionized water for several times.[7] After N_2 blow dry, the wafers were transferred immediately to the sputtering system chamber. A thin layer (~1 nm) of Y_2O_3 was deposited by sputtering of Y_2O_3 target on the clean Ge substrate, followed by the deposition of 9 nm HfTiO by cosputtering of Hf and Ti targets (denoted as stacked sample) as described in Ref. 11. For comparison, a control sample with a 10 nm HfTiO but without the Y_2O_3 interlayer deposited on Ge wafer was also made (denoted as non-stacked sample). For the purpose of analyzing the interface between Y_2O_3 and Ge, 5 nm Y_2O_3 was deposited on another Ge wafer (denoted as N2 sample). Then, the samples received postdeposition annealing (PDA) at 500 °C for 5 min in N_2. Al was evaporated and patterned as gate electrode with an area of 7.85×10^{-5} cm^{-2}. Finally, a forming-gas annealing was performed at 300 °C for 20 min to achieve better electrical contacts.

After fabrication of the samples, transmission electron microscopy (TEM) was used to observe the interface of dielectric/Ge. High-frequency (HF, 1 MHz) capacitance-voltage (*C-V*) characteristics were measured at room temperature using HP4284A precision *LCR* meter. Gate-leakage current was measured by HP4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectrics was determined by a multiwavelength ellipsometer. High-field stress (at 10 MV/cm for 3600 s) with the capacitors biased in accumulation by HP 4156A precision semiconductor parameter analyzer was used to examine device reliability in terms of gate-leakage (J_g) increase and flat-voltage (V_{fb}) shift after the stress. All electrical measurements were carried out under a light-tight and electrically shielded condition.

Figure 1(a) shows the cross-sectional TEM picture of the Y_2O_3/Ge MOS capacitor annealed in N_2 ambient. It is

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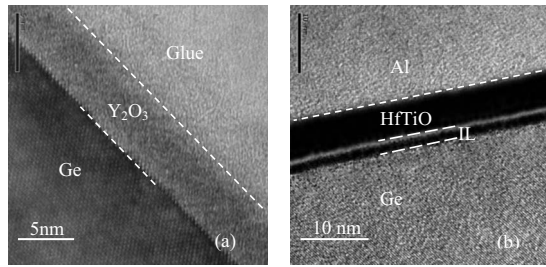
FIG. 1. TEM picture for the interface of (a) Y_2O_3/Ge and (b) HfTiO/Ge. IL in (b) indicates a layer (consisting of GeO_x or GeTiO) grown at the HfTiO/Ge interface during the postdeposition annealing.

FIG. 3. High-frequency *C-V* curves for the stacked and non-stacked samples. The inset shows their gate-leakage current vs gate voltage.

clearly shown that the Y_2O_3/Ge interface is abrupt, smooth, and GeO_x-free, similar to the Y_2O_3/Ge interface in Ref. 11. The absence of GeO_x should be attributed to the stability of the Y_2O_3 interlayer in contact with the Ge substrate. However for the HfTiO/Ge MOS capacitor annealed in N_2 ambient in Fig. 1(b), there is an obvious layer grown at the HfTiO/Ge interface, which consists of GeO_x or GeTiO compound.[12] Figure 2 shows the *C-V* and *I-V* curves of the N2 sample and also its counterpart without PDA (denoted as as-deposit sample). The distortion and hysteresis of the *C-V* curve for the as-deposited sample indicate interface and border traps, respectively. Clearly for the N2 sample, both are reduced due to reduction of border and interface traps after PDA. Moreover, the *C-V* curve of the N2 sample is shifted to the right and closer to the ideal *CV* curve, which is associated with the reduction of interfacial defects after PDA. The gate leakage current is also greatly reduced after PDA, as shown in the inset of Fig. 2, implying enhanced interface quality as well as improved bulk quality after the PDA.

Figure 3 shows the *C-V* curves for the non-stacked (HfTiO) and stacked ($HfTiO/Y_2O_3$) samples. There is a small bump in the depletion region for the non-stacked sample, indicating some interfacial defects, while no such distortion occurs for the stacked sample. This could be explained by the fact that Y_2O_3 has good interface properties with Ge, as mentioned above. Furthermore, Y_2O_3 can act as a barrier layer, which prevents Ge out-diffusion or Ti/Hf in-diffusion,[11] thus suppressing the interfacial defects. The values of capacitance equivalent thickness (CET), flat-band voltage (V_{fb}), oxide-charge density (Q_{ox}), and interface-state density near midgap (D_{it}) estimated from the HF *C-V* curve by the Terman's method[13] are listed in Table I. The CET of the stacked sample is smaller than that of the non-stacked
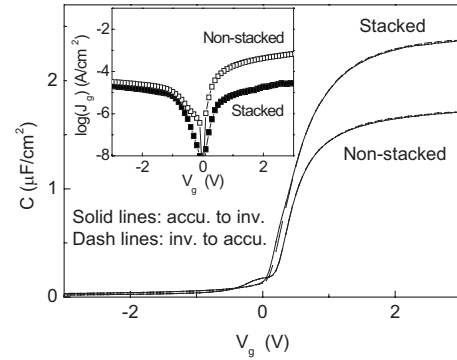
sample, which should be due to suppressed growth of GeO_x, as shown in Fig. 1(a). However, for the non-stacked sample shown in Fig. 1(b), there is an interlayer at the HfTiO/Ge interface, made of GeO_x or Ge–Ti–O compound. As a result, the stacked sample has lower D_{it} than the non-stacked sample, ascribed to suppressed growth of GeO_x and thus improved interface quality. Another reason for the smaller D_{it} is the passivation effects of the Y_2O_3 interlayer, which could function as a barrier layer for suppressing the Ge, Hf, and Ti diffusions.[11] Q_{ox} is negative for the two samples and is possibly due to the negative charges resulted from the breaking of the Hf–O bonds in the HfTiO dielectric.[14] The dielectric constant can be calculated by $k_{die} = \varepsilon_{SiO_2} \times t_{die}/CET$, where ε_{SiO_2} is the relative permittivity of SiO_2 and t_{die} is the physical thickness of the dielectric. The stacked sample is found to have a larger dielectric constant than the non-stacked sample (24.4 versus 19.5) due to the suppressed growth of low-k GeO_x.

The inset of Fig. 3 shows the gate leakage properties of the two samples. It is seen that the stacked sample has smaller gate leakage than the non-stacked sample (8.4×10^{-6} A/cm^2 versus 2.54×10^{-4} A/cm^2 at $V_g = V_{fb}+1$ V). This should be due to reduced interface traps and thus reduced trap-assisted gate leakage, as mentioned above. Figure 4 shows the *C-V* curves of the two samples under different frequencies. At low frequency, some of the traps could follow the change of the applied voltage (V_g), and thus generate additional capacitance.[15] There is a big ledge in the depletion region for the non-stacked sample, which should be due to a large quantity of interface states. However for the stacked sample, the *C-V* curve has no such ledge in the depletion region and also less frequency dispersion, implying less interface states.

A high-field stress (10 MV/cm) is imposed on the capacitors biased in the accumulation region for 3600 s to examine the reliability of the samples. The leakage current and *C-V* curves are measured for the samples before and after the stress. The changes of gate leakage (at $V_g = V_{fb}+1$ V) and
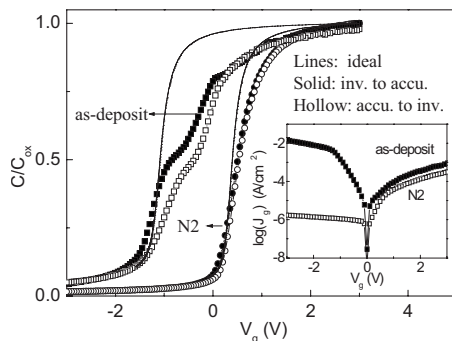

FIG. 2. High-frequency *C-V* curves for the N2 and the as-deposit samples (C_{ox} is the capacitance in the accumulation region). The inset shows their gate-leakage current vs gate voltage.

TABLE I. Parameters of the Ge MOS capacitors. t_{die} is the physical thickness of gate dielectric measured by ellipsometry.

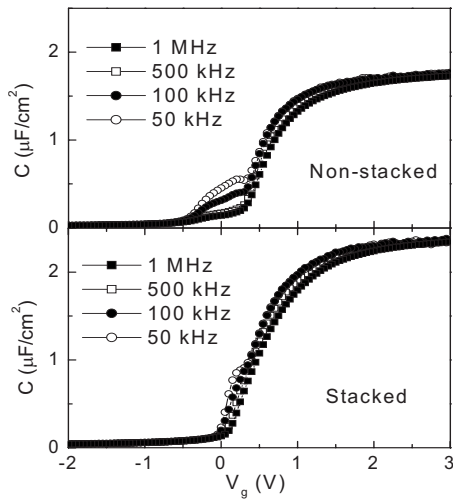| Sample	CET (nm)	V_{fb} (V)	D_{it} at midgap (cm^{-2} eV^{-1})	Q_{ox} (cm^{-2})	t_{die} (nm)	k
Non-stacked	2.0	0.27	4.3×10^{12}	-2.2×10^{12}	10.02	19.5
Stacked	1.6	0.14	7.1×10^{11}	-1.3×10^{12}	9.96	24.4

FIG. 4. *C-V* curves measured under different frequencies for the non-stacked sample and stacked sample.

flatband voltage are 4.5×10^{-5} A/cm^2 and 0.16 V, respectively, for the non-stacked sample, and 6.1×10^{-6} A/cm^2 and 0.06 V, respectively, for the stacked sample. Clearly, the nonstacked sample has larger changes of J_g and V_{fb}, indicating more defect generation during the stress. This could be explained by the GeO$_x$ interlayer grown at the HfTiO/Ge interface, which is unstable and easy to be damaged by high-field stress, thus generating new defects. However for the stacked sample, the insertion of a Y$_2$O$_3$ interlayer can effectively suppress the GeO$_x$ growth, thus resulting in less weak Ge–O bonds and a hardened interface. Consequently, the stacked sample with a Y$_2$O$_3$ interlayer has excellent reliability under high-field condition.

In summary, rare-earth oxide Y$_2$O$_3$ is investigated as a passivation layer in *n*-Ge MOS capacitors with high-*k* HfTiO gate dielectric. The Y$_2$O$_3$ interlayer can improve the electrical characteristics in terms of less *C-V* frequency dispersion, smaller gate leakage, and less interface states. The involved mechanism lies in the barrier role of the Y$_2$O$_3$ interlayer, which effectively blocks the interdiffusions of Ge, Hf, and Ti, thus suppressing the growth of unstable GeO$_x$ and improving the interface quality. In addition, the reliability of Ge

MOS capacitors with a Y$_2$O$_3$ interlayer is also improved, i.e., smaller flatband-voltage shift and less gate-leakage increase after high-field stressing. The possible reason is that the Y$_2$O$_3$ interlayer has good interface quality with Ge, thus increasing the resistance of the interface against high-field stressing. In a word, Y$_2$O$_3$ should be a promising interlayer material for passivating the Ge surface of Ge MOS devices.

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