Title	All-optical half-adder by using a single-stage optical parametric amplifier
Author(s)	Lai, DMF; Lin, EN; Wong, KKY
Citation	33rd European Conference and Exhibition on Optical Communication Proceedings, 2007, v. 4, p. 1024-1025
Issued Date	2007
URL	http://hdl.handle.net/10722/98793
Rights	European Conference on Optical Communication Proceedings. Copyright © IEEE.

All-Optical Half-Adder by Using a Single-Stage Optical Parametric Amplifier

David M. F. Lai, Edmond N. Lin, Kenneth K. Y. Wong
Department of Electrical and Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong. Email: mflai@eee.hku.hk

Abstract *An all-optical half-adder has been successfully demonstrated using cross gain modulation (XGM) and four-wave mixing (FWM) in an optical parametric amplifier (OPA) on a highly-nonlinear dispersion-shifted fiber. Power penalty of less than 2dB was achieved.*

Introduction

All-optical logic is of increasing importance for future optical networks to perform optical signal processing functions due to its speed advantage over electronic methods. Multiple logic gates can form elements for optical signal processing. One of them is the half-adder, which is a device capable of simultaneously producing XOR and AND outputs. Several implementations of half-adders using multiple semiconductor optical amplifiers (SOA) have been proposed, such as Ref.[1-4]. Here, we demonstrate a half-adder using an optical parametric amplifier (OPA) in a single highly-nonlinear dispersion-shifted fiber (HNL-DSF). The bit rate of the current setup is 10Gb/s. Since OPA is based on four wave mixing (FWM), which has ultra-fast response time; the sole use of OPA effects in our setup makes it a possibility for higher speed operation.

Theory

A summary of our half-adder's operation on all four possible input combinations is illustrated in fig. 1.

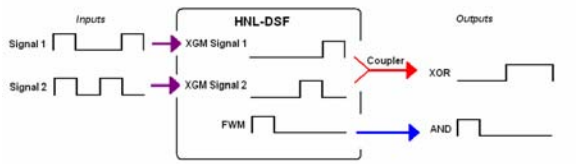

Fig. 1. The operating principle of the all-optical half-adder.

A half-adder is capable of producing AND and XOR operations of two bit streams simultaneously. In our design, two signals are launched slightly into the anomalous dispersion region of the HNL-DSF. This will allow phase matching conditions required for OPA. Only when both of the input signals are ON, FWM will cause the two signals to distribute its power to the newly generated idler frequencies. These idlers can serve as an AND operation on the input signals. However, the two signals will be depleted when they are both ON, due to cross gain modulation (XGM) from OPA. Hence, the signals at the output will be OFF only when both of the inputs are ON, or when both inputs are OFF. When either one of the input signals is ON; it will emerge at the output without much loss of power. Therefore, by coupling the two signals at the output, we can achieve an XOR gate.

Experimental Setup

The experimental setup is shown in fig. 2 below.

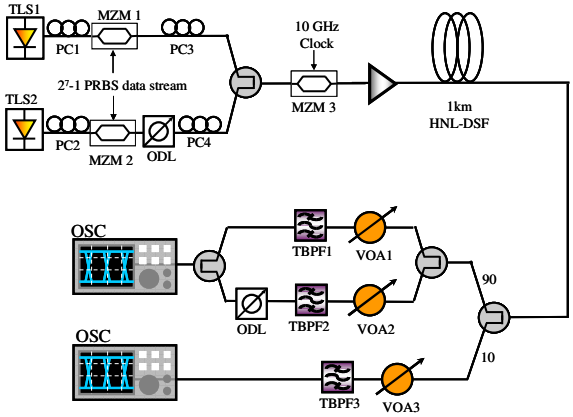

Fig. 2. Experimental Setup. ODL: Optical delay line. VOA: Variable optical attenuator. MZM: Mach-Zehnder modulator. PC: Polarization controller. OSC: Oscilloscope. All couplers are 50/50 couplers unless otherwise stated.

The nonlinear element was a spool of 1km highly-nonlinear dispersion-shifted fiber (HNL-DSF), with a zero dispersion wavelength at 1559nm and nonlinearity coefficient of $14W^{-1}km^{-1}$. The two input signals were at 1561.4nm and 1565.4nm. They were amplitude modulated with 2^7-1 pseudo-random bit sequence (PRBS) signals using Mach-Zehnder modulators. The choice of this sequence was due to the manual entry of the output bit stream to the error detector for BER measurements, since the device modified the data from input to output. The optical delay line after MZM2 was used to ensure that the two signals were detuned from each other for an integer number of bits. The input signals were then coupled and fed into MZM3. MZM3 was driven by a 10GHz clock synchronized with the input bit streams and it effectively converted the two NRZ signals into RZ signals. The result was then amplified by an EDFA to a total output power of 21dBm before being input into the HNL-DSF. At the output of the HNL-DSF, the power was split into two branches using a 90/10 coupler. At the "90%" branch, a 3dB coupler was used to further split the power into two branches. On these two branches, tunable band pass filters

TBPF1 and TBPF2 filtered out each of the two signal wavelengths. VOA1 and VOA2 were used to attenuate the two signals to prevent damage to TBPF1 and TBPF2 respectively. They were also used to allow both signals 1 and 2 to attain the same amplitude for a '1' bit. The optical delay line after TBPF2 was used to synchronize the two branches. The two branches were then recombined together using a 3dB coupler to achieve a XOR output. At the "10%" output of the 90/10 coupler, a FWM component at 1569.5nm was filtered using TBPF3 and VOA3 was used to prevent damage to TBPF3. This FWM component served as the AND operator on the two input signals.

Results and Discussion

Figure 3 below showed bit patterns of both the input and output. The bit '1's and bit '0's had been labeled accordingly. The fluctuations at bit '0's at the XOR output were due to finite rise and fall times of the inputs, since during the bit transitions, there was insufficient power to deplete the signals by XGM. This was confirmed with the eye diagram, where the fluctuations were inhibited at the pulse edges. The AND output had a slightly narrower pulse shape, which was also a consequence of finite rise and fall times [5].

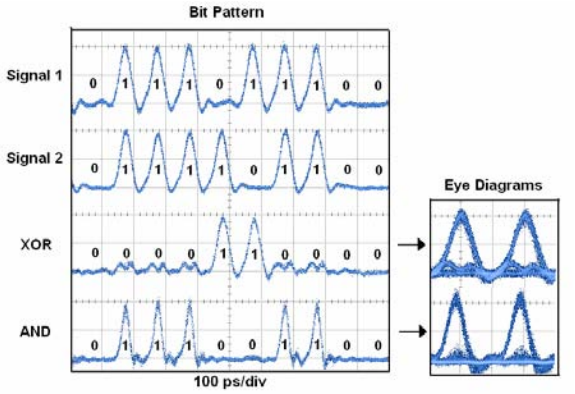

Fig.3. Bit patterns for the inputs and outputs and eye diagrams for the outputs

To quantify the non-idealities at the output, a bit error rate test was performed on the half-adder. Figure 4 showed the bit error rate curve for the XOR, AND, and input signals. At an error rate of 10^{-9}, the power penalty for the AND output is 0.35dB, but for the XOR output, the power penalty is 1.92dB. The higher power penalty at the XOR output was believed to be caused by the residues at the rising and falling edges of the input signals described earlier. Amplified spontaneous emission (ASE) noise from the EDFA had also contributed to the power penalty. The Q factors of the AND output and XOR output were 9.79 and 10.22 respectively. The lower Q factor at the AND output was primarily attributed to ASE noise.

It is possible to improve the power penalty of the XOR output by reducing the magnitude of the ripples at the edges that occurred at bit '0'. This can be achieved by increasing the input power to the HNL-DSF of the two signals. However, suppression of stimulated Brillouin scattering (SBS) will be required by using phase dithering [6] or by other means. Additionally, the OPA gain will increase, leading to stronger FWM effects amongst the generated idlers, which will deplete or amplify each other. ASE noise power from the EDFA will increase with increasing EDFA output power, leading to increase in the noise taken by the AND output. Therefore, the XOR output quality will improve by increasing the input power to the HNL-DSF, while the AND output quality may improve or degrade depending on the ASE noise.

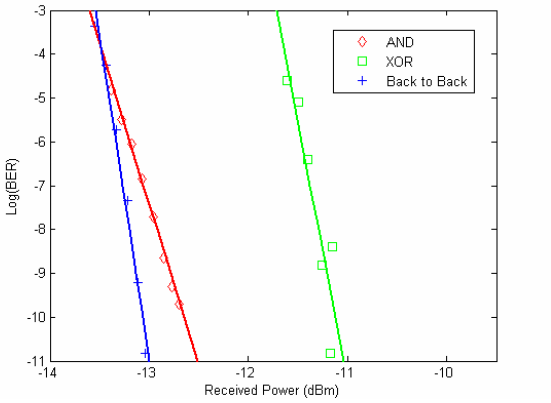

Fig. 4. BER curves for XOR, AND, and Back-to-Back

Conclusion

We have successfully demonstrated an all-optical half-adder using a single OPA in a HNL-DSF. The power penalty of the XOR gate is less then 2dB, and that of the AND gate is only 0.35dB. The minimal distortions reveal a possibility for much higher speed of operation, and this has been predicted by theory.

Acknowledgements

The work described in this paper was partially support by a grant from the Research Grants Council of the Hong Kong Special Administrative Region, China (Project No. HKU 7179/06E). The authors would also like to acknowledge Sumitomo Electric Industries for providing the HNL-DSF.

References

1 A. J. Poustie et al, *Opt. Commun.*, 156(1998), 22-26
2 D. Tsiokos et al, *IEEE PTL*, 16 (2004), 284-286
3 S. Kumar et al, *Opt. Fiber Commun. Conf*, 1(2004), 23-27
4 S. H. Kim et al, *Opt. Express*, 14(2006), 10693-10698
5 T. Yamato et al, *IEEE PTL*, 9(1997), 1595-1597
6 K. K. Y. Wong et al, *IEEE PTL*, 150(2003), 33-35