



<b>Title</b>	<b>Charging-induced changes in reverse current-voltage characteristics of Al/Al-Rich Al<sub>2</sub>O<sub>3</sub>/p-Si Diodes</b>
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# Charging-Induced Changes in Reverse Current–Voltage Characteristics of Al/Al-Rich Al<sub>2</sub>O<sub>3</sub>/p-Si Diodes

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**Abstract**—An Al-rich Al<sub>2</sub>O<sub>3</sub> thin film was deposited on a p-type silicon substrate by radio frequency sputtering to form Al/Al-rich Al<sub>2</sub>O<sub>3</sub>/p-Si diodes. The current–voltage ( $I$ – $V$ ) characteristics of the diodes were determined by carrier injection from either the Si substrate or the Al gate and by carrier transport along the tunneling paths formed by Al nanocrystals distributed in the oxide layer. The reverse  $I$ – $V$  characteristics were greatly affected by the charge trapping in the oxide layer, i.e., the electron trapping significantly reduced the reverse current while the hole trapping enhanced the current significantly. However, the charge trapping did not produce a large change in the forward  $I$ – $V$  characteristic.

**Index Terms**—Aluminum-rich aluminum oxide, charge trapping, current transport, current–voltage characteristics, metal–insulator–semiconductor (MIS) diodes, memory effect, nanocrystals.

## I. INTRODUCTION

ALUMINUM oxide (Al<sub>2</sub>O<sub>3</sub>) which has a high dielectric constant ( $k = \sim 8 - 10$ ) and also a similar band gap and band alignment as silicon oxide has been proposed to be used in nonvolatile memory devices as a blocking layer or a charge storage layer [1]–[4]. Recently, Al-rich Al<sub>2</sub>O<sub>3</sub> thin film synthesized with electron-cyclotron-resonance sputtering at a reduced oxygen gas flow rate was shown to be a promising candidate for the charge storage layer [3]. In our previous work [5], we also observed that the Al-rich Al<sub>2</sub>O<sub>3</sub> thin film synthesized by reactive radio frequency (RF) sputtering had a good charge storage capability, and the charge storage behaviors were similar to that of Al-rich AlN thin films [6]. In this paper, we show that the charge trapping in the Al-rich Al<sub>2</sub>O<sub>3</sub> thin films

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significantly changes the reverse current–voltage ( $I$ – $V$ ) characteristics of the Al/Al-rich Al<sub>2</sub>O<sub>3</sub>/p-Si diodes while there is no significant change in the forward  $I$ – $V$  characteristics. Such charging effect could be used for two-terminal charging-controlled resistive memory.

## II. EXPERIMENT

Al-rich Al<sub>2</sub>O<sub>3</sub> thin film with thickness of 60 nm was deposited on a p-type, (100)-oriented Si wafer with a resistivity of 9–12  $\Omega \cdot \text{cm}$ , which was precleaned using standard RCA process. The deposition was carried out by RF magnetron sputtering of an Al target with the purity of 99.99% in a mixed Ar/O<sub>2</sub> atmosphere at a controlled flow rate. During deposition, the RF power was 300 W and the sputtering pressure was 0.93 Pa. The argon and oxygen flow rates were 60 and 1 sccm, respectively. No additional heating was applied during deposition; but the substrate temperature was slightly higher than the room temperature due to ion bombardment. A rapid thermal annealing was conducted at 550 °C for 30 s in N<sub>2</sub> ambient. To fabricate the metal–insulator–semiconductor (MIS) diode structure, an ohmic contact on the Si wafer backside was formed by the deposition of a 200-nm aluminum layer, and an aluminum film of 100 nm was deposited on the surface of the Al-rich Al<sub>2</sub>O<sub>3</sub> thin film to form the gate electrode. Cross-sectional transmission electron microscopy (TEM) and X-ray photoemission spectroscopy (XPS) were used to investigate the structural and chemical properties of the Al-rich Al<sub>2</sub>O<sub>3</sub> thin film, respectively. The XPS result indicates that the as-fabricated thin film was indeed Al rich with an Al-to-Al<sub>2</sub>O<sub>3</sub> atomic ratio of 1.24, and the TEM images shows that Al nanocrystals (nc-Al) were formed in the Al<sub>2</sub>O<sub>3</sub> matrix. The details of the TEM and XPS experiments have been reported elsewhere [5]. The  $I$ – $V$  measurement was carried out with a Keithley 4200 semiconductor characterization system, and capacitance–voltage ( $C$ – $V$ ) measurement was performed with an HP 4284A LCR meter at the frequency of 1 MHz. Both measurements were conducted at room temperature.

## III. RESULTS AND DISCUSSION

Fig. 1 shows the  $I$ – $V$  characteristics of the MIS diode. As shown in the figure, the diode structure exhibited a “rectifying” behavior, namely, the current under the forward bias condition (i.e., the gate voltage was negative) was larger than that under

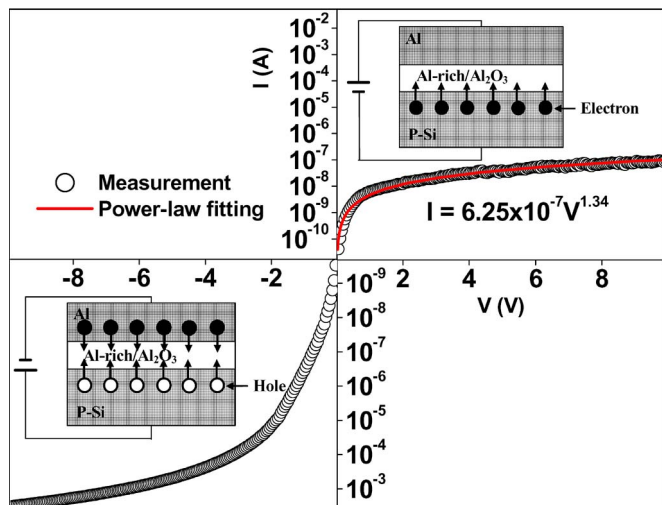


Fig. 1.  $I$ - $V$  characteristic of the MIS diode structure. The insets in the upper right and lower left panes show the carrier injection under a reverse bias (i.e., a positive voltage is applied to the Al gate) and a forward bias (i.e., a negative voltage is applied to the gate), respectively.

the reverse bias condition (i.e., the gate voltage was positive). This behavior can be explained as follows. Both the electron injection from the Al gate and the hole (the majority carrier in the Si substrate) injection from the p-type Si substrate occurred simultaneously under a negative gate voltage; in contrast, only electron (the minority carrier in the Si substrate) injection from the Si substrate occurred under a positive gate voltage.

Fig. 1 also shows that the reverse  $I$ - $V$  characteristic followed a power law, i.e.,  $I = I_0 V^\zeta$ , where the parameters  $\zeta$  and  $I_0$  were determined by both the structural properties of the oxide thin film and the charge trapping in the thin film [7]. The power law behavior suggests that the current transport was controlled by the Al-rich  $Al_2O_3$  layer rather than the electron injection from the Si substrate in the case of reverse bias. The power-law transport could be explained by a model similar to the one of collective charge transport in arrays of normal-metal quantum dots [8], [9]. The injected electrons can be transported along the tunneling paths formed by the nc-Al distributed in the aluminum oxide thin film [5], [7]. This mechanism is used to explain the observed charging-induced changes in the reversed  $I$ - $V$  characteristics, as discussed later. On the other hand, the forward  $I$ - $V$  characteristic cannot be described with the above power law, because the situation was more complicated as both the electrons injected from the gate electrode and the holes injected from the Si substrate were to be transported across the aluminum oxide layer.

As previously mentioned, under a positive gate voltage, only electrons were injected from the Si substrate to the Al-rich  $Al_2O_3$  layer. Some of the injected electrons were trapped in the oxide layer, which caused a positive flatband voltage shift ( $\Delta V_{FB}$ ) of the MIS structure. As shown in Fig. 2, the application of +15 V to the gate for 100 s shifted the  $C$ - $V$  characteristic to the positive with a positive flatband voltage shift of 0.15 V ( $\Delta V_{FB} = +0.15$  V), indicating that electron trapping occurred in the Al-rich  $Al_2O_3$  layer, with the possibility that the electrons could have been trapped in the nc-Al. On the other hand, as revealed by the TEM images, the interfaces between

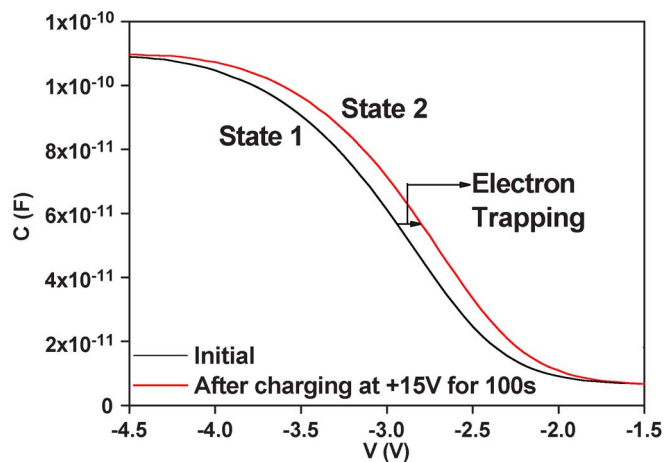


Fig. 2. Shift in  $C$ - $V$  characteristic after the application of +15 V for 100 s showing electron trapping in the oxide layer.

nc-Al and  $Al_2O_3$  were imperfect. Due to the imperfection of the  $Al_2O_3$  matrix with the embedded nc-Al, it is reasonable to assume that there was a large amount of defects at the interfacial regions between the embedded nc-Al and the  $Al_2O_3$  matrix. Therefore, the electrons could also be trapped in these defects. Nevertheless, the electron trapping was associated with the existence of the excess Al (i.e., nc-Al) distributed in the oxide layer. The electron trapping in either the nc-Al or the defects occurred when the injected electrons were transported along the tunneling paths formed by the nc-Al. The electron trapping, in turn, affected the carrier transport across the oxide layer, as discussed below.

Fig. 3 shows the  $I$ - $V$  characteristics before and after the electron trapping. The electron trapping was achieved under the same bias conditions with the same charging duration as those in Fig. 2. As shown in Fig. 3(a) for the reverse  $I$ - $V$  characteristics, the electron trapping led to a significant reduction in the current. The reverse  $I$ - $V$  characteristic after the electron trapping also followed a power law, but with smaller values of power-law parameters,  $I_0$  and  $\zeta$ , as compared to those before the electron trapping. The influence of electron trapping on the current conduction is explained as follows. Electron trapping in an nc-Al or a defect increased the resistance of the tunneling paths involving the nc-Al or the defect because of the electrostatic interaction of the transported electrons with the trapped electrons, and the tunneling paths could also be broken due to the Coulomb blockade effect [7]. Therefore, the electron trapping suppressed the electron transport across the oxide layer. On the other hand, the electron trapping reduced the electric field in the region of the oxide/Si interface, thus decreased the electron injection from the Si substrate during the reverse  $I$ - $V$  measurement. In contrast to the reverse  $I$ - $V$  characteristic, the electron trapping did not have a large impact on the forward  $I$ - $V$  characteristic, as shown in Fig. 3(b). This situation was due to the fact that both electron injection from the gate and the hole injection from the Si substrate occurred during the forward  $I$ - $V$  measurement. The electron trapping suppressed the transport of the injected electrons but enhanced the transport of the injected holes. In addition, the electron injection was reduced while the hole injection was enhanced due to the

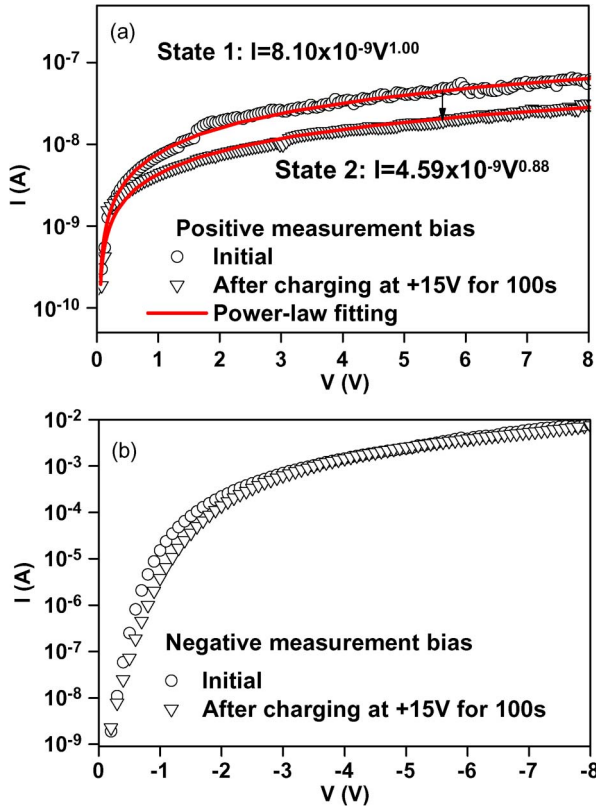


Fig. 3.  $I$ - $V$  characteristics before and after the application of +15 V for 100 s. (a) Reverse  $I$ - $V$  characteristics. (b) Forward  $I$ - $V$  characteristics.

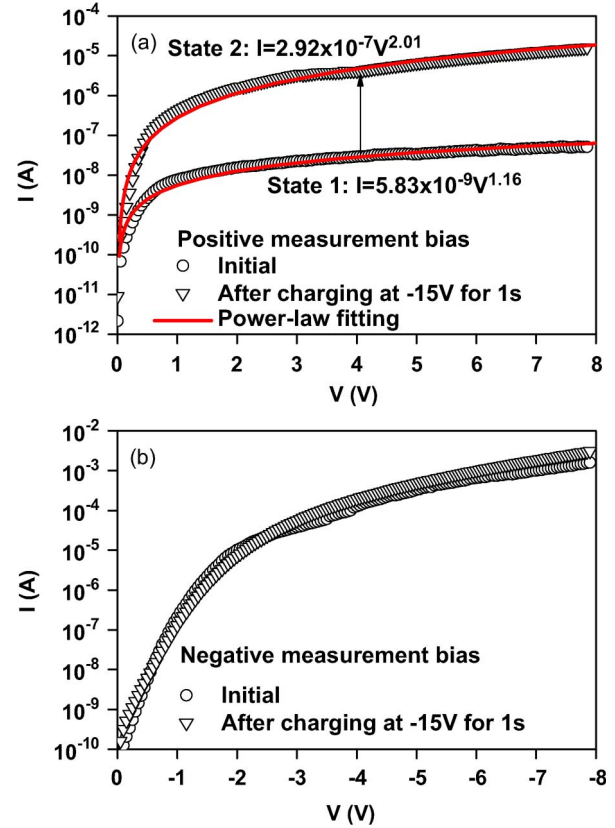


Fig. 5.  $I$ - $V$  characteristics before and after the application of -15 V for 1 s. (a) Reverse  $I$ - $V$  characteristics. (b) Forward  $I$ - $V$  characteristics.

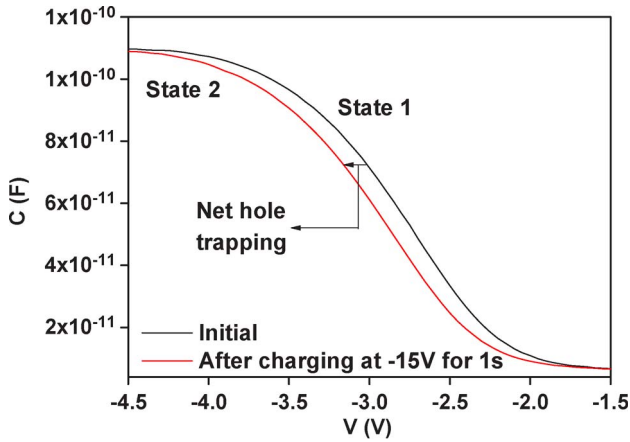


Fig. 4. Shift in  $C$ - $V$  characteristic after the application of -15 V for 1 s showing net positive charge trapping in the oxide layer.

electron trapping. Therefore, the forward  $I$ - $V$  characteristic was not significantly affected by the electron trapping.

Under a negative gate voltage, both the electron injection from the gate and the hole injection from the Si substrate occurred simultaneously, but the net charge trapping in the oxide layer could be either negative or positive, depending on the magnitude of the voltage and the charging duration. The net charge trapping tended to be positive for a larger voltage magnitude and a longer charging duration. As shown in Fig. 4, the application of -15 V for 1 s shifted the  $C$ - $V$  characteristic to the negative with a negative flatband voltage shift of 0.15 V ( $\Delta V_{FB} = -0.15$  V), indicating a net positive charge trapping

in the Al-rich  $Al_2O_3$  layer (i.e., the hole trapping was dominant). The positive charge trapping had a strong impact on the reverse  $I$ - $V$  characteristic. As shown in Fig. 5(a), the reverse current was increased by about two orders after the positive charge trapping. The increase in the reverse current was due to the enhancements in both the electron injection from the Si substrate and the transport of the injected electrons along the nc-Al tunneling paths during the reverse  $I$ - $V$  measurement by the net positive charge trapping in the oxide layer. Being similar to the situation of the electron trapping discussed earlier, the positive charge trapping did not cause a large change in the forward  $I$ - $V$  characteristics, as shown in Fig. 5(b), because both the electron injection from the gate and the hole injection from the Si substrate were involved in the forward  $I$ - $V$  measurement.

The charging effect on the reverse  $I$ - $V$  characteristic could be used to realize a two-terminal charging-controlled resistive memory based on the MIS structure. The reverse resistance of the MIS diode can be changed by the charge trapping in the Al-rich aluminum oxide layer, i.e., the resistance is switched to a high- or low-resistance state by the electron trapping or the hole trapping, respectively. The memory states represented by the resistance states can be changed by a large voltage, and they can be distinguished by measuring the resistance (or current) at a small reverse bias. The two-terminal charging-controlled resistive memory offers a higher memory density and a lower fabrication cost. Fig. 6 shows a preliminary result of the retention performance of the memory device. The current measurement was conducted at a low bias of +2 V while the charging operation was carried out at -15 V for 1 s. As shown



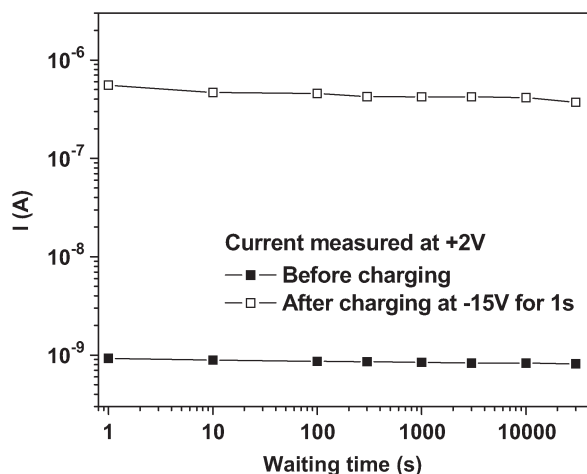


Fig. 6. Currents of the two memory states (i.e., the states before and after the charging at  $-15\text{ V}$  for  $1\text{ s}$ ) measured at  $+2\text{ V}$  as a function of waiting time.

from the figure, the current ratio of the two memory states (i.e., the states before and after the charging) was large enough for distinguishing the two memory states. In addition, the currents of the two memory states had no significant changes after a waiting time of  $30\,000\text{ s}$ .

#### IV. CONCLUSION

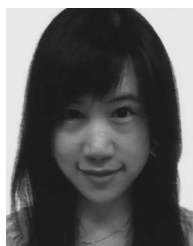
In summary, an Al-rich  $\text{Al}_2\text{O}_3$  thin film was deposited on a p-type silicon substrate by RF sputtering to form an Al/Al-rich  $\text{Al}_2\text{O}_3$ /p-Si MIS diode. Under a positive bias applied to the Al gate (i.e., reverse bias), electrons were injected from the Si substrate and some of them were trapped in the Al-rich  $\text{Al}_2\text{O}_3$  layer. In contrast, both the electron injection from the Al gate and the hole injection from the Si substrate occurred under a negative bias (i.e., forward bias), leading to both electron and hole trapping in the Al-rich  $\text{Al}_2\text{O}_3$  layer, and a positive charge trapping could be achieved with a large voltage magnitude and/or a longer charge duration. The electron trapping and hole trapping caused a significant reduction and a large increase in the reverse current, respectively. However, the charge trapping (either electron or hole trapping) did not produce a large change in the forward  $I$ - $V$  characteristic. The charging effect on the reverse current could be used to realize a two-terminal charging-controlled resistive memory based on the MIS structure.

#### REFERENCES

- [1] Y. Zhao, X. Wang, H. Shang, and M. H. White, "A low voltage SANOS nonvolatile semiconductor memory (NVSM) device," *Solid State Electron.*, vol. 50, no. 9/10, pp. 1667–1669, Sep./Oct. 2006.
- [2] M. Specht, H. Reisinger, F. Hofmann, T. Schulz, E. Landgraf, R. J. Luyken, W. Rösner, M. Grieb, and L. Risch, "Charge trapping memory structures with  $\text{Al}_2\text{O}_3$  trapping dielectric for high-temperature applications," *Solid State Electron.*, vol. 49, no. 5, pp. 716–720, May 2005.
- [3] S. Nakata, K. Saito, and M. Shimada, "Nonvolatile memory using  $\text{Al}_2\text{O}_3$  film with an embedded Al-rich layer," *Appl. Phys. Lett.*, vol. 87, no. 22, p. 223 110, Nov. 28, 2005.
- [4] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, "A novel SONOS structure of  $\text{SiO}_2/\text{SiN}/\text{Al}_2\text{O}_3$  with TaN metal gate for multi-giga bit flash memories," in *IEDM Tech. Dig.*, 2003, pp. 26.5.1–26.5.4.
- [5] Y. Liu, T. P. Chen, W. Zhu, M. Yang, Z. H. Cen, J. I. Wong, Y. B. Li, S. Zhang, X. B. Chen, and S. Fung, "Charging effect of  $\text{Al}_2\text{O}_3$  thin films

containing Al nanocrystals," *Appl. Phys. Lett.*, vol. 93, no. 14, p. 142 106, Oct. 6, 2008.

- [6] Y. Liu, T. P. Chen, P. Zhao, S. Zhang, S. Fung, and Y. Q. Fu, "Memory effect of Al-rich AlN films synthesized with rf magnetron sputtering," *Appl. Phys. Lett.*, vol. 87, no. 3, p. 033 112, Jul. 18, 2005.
- [7] Y. Liu, T. P. Chen, H. W. Lau, J. I. Wong, L. Ding, S. Zhang, and S. Fung, "Charging effect on current conduction in aluminum nitride thin films containing Al nanocrystals," *Appl. Phys. Lett.*, vol. 89, no. 12, p. 123 101, Sep. 18, 2006.
- [8] A. A. Middleton and N. S. Wingreen, "Collective transport in arrays of small metallic dots," *Phys. Rev. Lett.*, vol. 71, no. 19, pp. 3198–3201, Nov. 8, 1993.
- [9] H. E. Romero and M. Drndic, "Coulomb blockade and hopping conduction in PbSe quantum dots," *Phys. Rev. Lett.*, vol. 95, no. 15, p. 156 801, Oct. 3, 2005.



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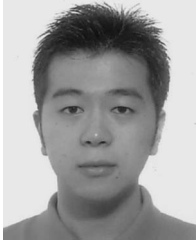
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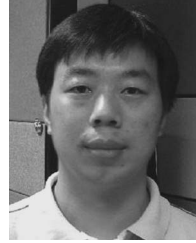
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