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Threshold-voltage instability of polymer thin-film transistor under gate-bias and drain-bias stresses

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Abstract - Polymer thin-film transistors (PTFTs) based on MEH-PPV semiconductor are fabricated by spin-coating process and characterized. Gate-bias and drain-bias stress effects at room temperature are observed in the devices. The saturation current decreases and the threshold voltage shifts toward negative direction upon the gate-bias stress. However, the saturation current increases and the threshold voltage shifts toward positive direction upon the drain-bias stress. For variable bias stress conditions, carrier mobility is almost unchanged. The results suggest that the origin of threshold-voltage shift upon negative gate-bias stress is predominantly associated with holes trapped within the SiO₂ gate dielectric or at the SiO₂/Si interface due to hot-carrier emission under high gate-bias stress, while time-dependent charge trapping into the deep trap states in the channel region is responsible for the drain-bias stress effect in the PTFTs.

Keywords: Polymer thin-film transistors; Stress effect; Threshold-voltage shift; Stability

I. INTRODUCTION

Great progress has been made to develop high-performance polymer thin-film transistors (PTFTs) over the past decade [1-2]. However, the reliability of PTFTs remains a significant issue. Even when devices are encapsulated or operate in vacuum or inert environment, the threshold voltage (V_T) shifts with stress time under a gate-bias stress. The gate-bias stress effect was universally observed in thin-film transistors based on organic or polymer materials, such as pentacene [3], [4], poly(3-hexylthiophene) [5], polythienylene vinylene [6], a-sexithiophene [7], and poly-9,9-dioctyl-fluorene-cobithiophene [8]. It was also found that the gate-bias stress effect was reversible after removal of the bias. In the literature, several mechanisms have been presented to explain the bias-stress effect. In any particular situation, the origin might be trapping in states within the gate dielectric, at the semiconductor/dielectric interface or in the semiconductor itself, or mobile ion migration, charged-state creation or formation of bipolaron.

So far, many researches have focused on the gate-bias stress effect and its mechanism. However, for analog applications, the PTFT is required to withstand

prolonged biasing at both the drain and gate terminals. Thus, in this work, PTFTs are fabricated on silicon substrate with SiO₂ as gate insulator and poly(2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene) (MEH-PPV) as semiconducting active layer because of its better stability against the oxidative doping of air [9]. The gate-bias and drain-bias stress effects are researched to gain deeper understanding of bias stress effect on the PTFTs devices. The results are useful for the development of PTFTs in organic electronics.

I. EXPERIMENTS

N/n+ type (111) silicon wafer with a resistivity of 0.9 ~ 1.1 Ωcm was used as the substrate material for fabricating the devices. A thin layer of gate oxide was grown by thermal dry oxidation at 1000 °C for 180 min. The oxide film on the backside of the silicon substrate was removed and aluminum was deposited to form the gate contact for the PTFT devices. Solid MEH-PPV polymer was dissolved in toluene at a concentration of 5 mg/ml and was spin-coated as the semiconducting active layer on the gate oxide at 2000 rpm for 60 s in air, and then the wafer was annealed at 90 °C in air for 30 min. Finally, gold was vacuum evaporated through a shadow mask to form source/drain (S/D) electrodes with a comb-shaped structure. The device channel width and length were defined as 10 μm and 100 nm, respectively. The PTFT with top-S/D-contact configuration after fabrication is shown in Fig. 1.

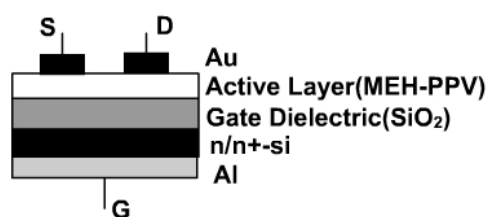


Fig. 1. Schematic cross-section of the PTFT.

The thickness of the silicon oxide was measured to be 150 nm by ellipsometry. The thickness of the polymer thin film was determined to be 50 ~ 60 nm by surface profilometry. The output and transfer characteristics of the PTFTs were measured in the dark and air by using an Agilent 4156C semiconductor parameter analyzer. Two series of bias-stress measurements were performed: one with zero drain bias and various gate biases, and the other with a fixed drain bias and different gate biases. To evaluate the effects of gate-bias and drain-bias stresses on PTFT electrical characteristics, the transfer characteristics curves needed to be measured periodically during the stress experiment, and the drain

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voltage was -20 V for all transfer characteristics measurements. Since the PTFT was sensitive to bias stress during the transfer characteristics measurements, fast measurements and a small number of measured points per transfer characteristics curve were required to minimize the influence of monitoring PTFT transfer characteristics on the overall bias stress experiment.

II. RESULTS AND DISCUSSION

Typical output and transfer characteristics of the PTFTs are shown in Fig. 2. It can be seen from Fig. 2(a) that the PTFT shows better saturation behavior than the PTFT based on P3HT polymer [10], and a drain current of up to 20 nA can be achieved in the saturation region for a gate voltage of -30 V. Since MEH-PPV is a p-type semiconductor, negative gate voltage V_{GS} and drain voltage V_{DS} are applied to induce charge carriers for operation in the accumulation mode. For PTFTs operating in saturation regime ($|V_{DS}| > |V_{GS} - V_T|$), drain current I_{Dsat} can be described by:

$$I_{Dsat} = \frac{W}{2L} \mu_{eff} C_{ox} (V_{GS} - V_T)^2 \quad (1)$$

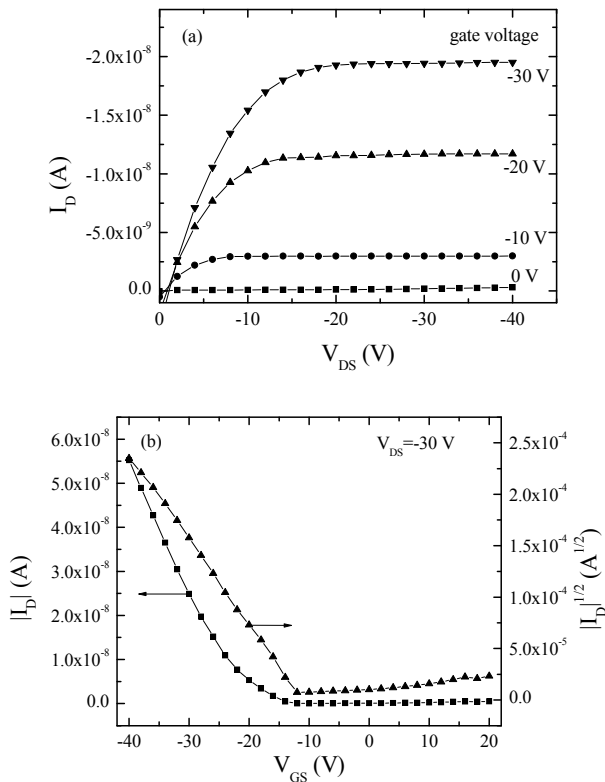


Fig. 2. Typical characteristics of the PTFT measured under dark condition. (a) output characteristics for various gate voltages; (b) transfer characteristics for various drain voltages.

where W is channel width and L is channel length; μ_{eff} is field-effect mobility; C_{ox} is gate-oxide capacitance

per unit area; V_T is threshold voltage. According to Eq. (1), the field-effect mobility calculated from Fig. 2(b) is 5.4×10^{-5} cm²/Vs in the saturation region for a drain voltage of -30 V. From the transfer characteristics of the PTFT (Fig. 2(b)), the on/off current ratio is determined to be 10^3 and a V_T of -8.1 V is extracted for a drain voltage of -30 V.

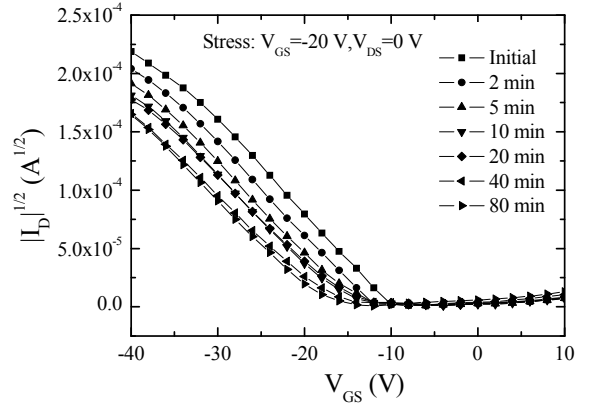


Fig.3. Transfer characteristics of the PTFT for variable stress times. The stress condition has a V_{GS} of -20 V and a V_{DS} of 0 V.

For the gate-bias stress experiment, with source and drain connected to ground, various gate biases are used as the stress conditions ($V_{DS} = 0$ V, $V_{GS} = -5$, -20 , and -30 V). Fig. 3 presents the transfer characteristics of the PTFT after subject to a negative gate bias voltage of -20 V for different times. The on-state current decreases with increasing stress time in the saturation region. With the increase of stress time, the V_T shifts towards negative direction from rapidly to slowly, and after a gate-bias stress for 10 min, the V_T shifts from -6.9 V to -12.2 V, while the off-state current, the subthreshold swing and carrier mobility remain essentially constant, indicating that the gate-bias stress does not cause charge trapping and defect-state creation in the channel. The origin of V_T shift upon negative gate-bias stress is predominantly associated with holes trapped within the SiO₂ gate dielectric or at the SiO₂/Si interface due to hot-carrier emission under high gate-bias stress [11]. Like other studies [12], [13], V_T can recover to its original value after the removal of gate bias for a relatively long time, and the reverse process can be enhanced by applying an opposite polarity gate bias. Fig.4 depicts the shift of V_T as a function of stress time for variable gate-bias and a fixed drain bias of 0 V. Obviously, V_T is drastically changed, and the direction and rapidity of V_T shift depend on the size of the gate-bias. When the gate bias ($V_{GS} = -5$ V) is lower than the initial V_T (-8.1 V), V_T shifts towards positive direction slowly. A possible explanation is that when the gate bias is smaller than the initial V_T , the gate field is low enough not to induce the channel charges (holes) and result in holes trapped within the SiO₂ gate dielectric or at the SiO₂/Si interface by hot-carrier emission. In this case, the positive V_T shift is originated from the positive mobile charges in the gate dielectric drifting from the interface to the gate electrode.

On the contrary, when the gate bias is high enough to cause channel charges (holes) trapped within the SiO₂ gate dielectric or at the SiO₂/Si interface by hot-carrier emission under strong electric field, the higher the gate bias applied, the larger is the shift of V_T for the same stress time. In addition, it is found that the time dependence of V_T upon gate-bias stress follows a logarithmic law as shown in Fig. 4 and is similar to phenomenological description developed in the studies of electrical stability in a-Si TFTs, where the V_T shift is primarily due to charge trapping in the insulator and creation of defect states under constant-bias stress [14].

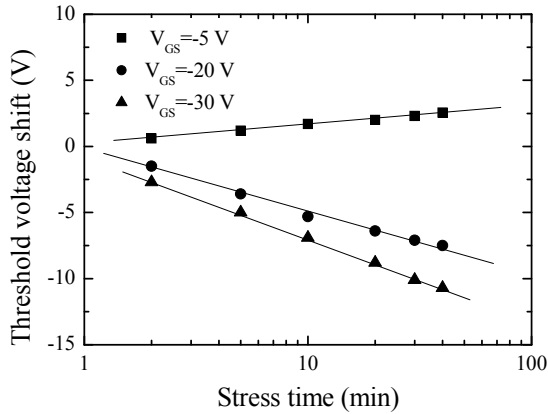


Fig.4. Shift of threshold voltage as a function of stress time for different gate-bias stresses and a fixed drain bias of 0 V.

For the drain-bias stress experiment, with a fixed drain bias ($V_{DS} = -20$ V), various gate biases are used as the stress conditions (the gate electrode is open, and $V_{GS} = 0$ and -20 V). Fig. 5 describes the transfer characteristics of the PTFT after subject to a negative drain bias voltage of -20 V for different times when the gate electrode is open. With the increase of stress time, the off-state current and the subthreshold swing increase, and mobility keeps almost unchanged, while V_T shifts towards positive direction from rapidly to slowly, and after a drain-bias stress for 10 min, V_T shifts from -5.6 V to 4.0 V. The results indicate that the mechanism of the drain-bias stress effect is different from that of the gate-bias stress effect. Under the drain-bias stress, the shift of V_T can be explained as follows. Charge carriers (holes) injected from the source electrode are partly trapped by deep defect states within the channel, while the increases of the off-state current and subthreshold swing are related to defect creation within the channel which is caused by electric field along the channel. Furthermore, the drastic effect of the gate-bias stress on the shift of V_T under drain-bias stress is observed as shown in Fig. 6. When the gate electrode is open, the shift of V_T is largest for the same stress time, and the shift of V_T decreases with the increase of the negative gate bias. When the gate bias and the drain bias are -20 V, the shift of V_T is not obvious, and a continued increase of gate bias can cause a negative V_T shift. This is because the drain-bias stress effect is suppressed by the gate-bias stress effect when the gate bias becomes more negative, and even the

gate-bias stress effect becomes dominant. In addition, it can be found from Fig. 6 that the time dependence of V_T upon the drain-bias stress is not a logarithmic law. For a longer stress time (> 20 min), the shift of V_T tends to saturate. A possible reason is that when the stress time is much longer than the effective trapping time, charge trapping is close to an equilibrium state.

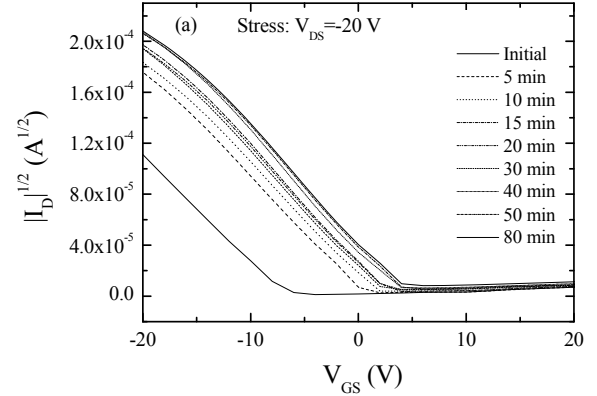


Fig.5. Transfer characteristics of the PTFT for different stress times. The stress condition is: $V_{DS} = -20$ V and the gate electrode is open.

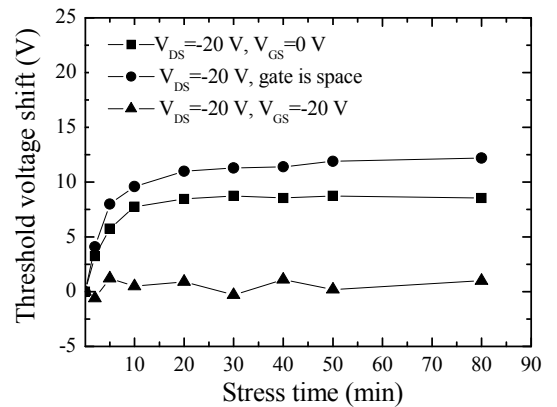


Fig.6. Shift of threshold voltage as a function of stress time under a fixed drain-bias stress of -20 V and different gate biases (the gate electrode is open, and $V_{GS} = 0$ and -20 V).

III. CONCLUSION

Gate-bias and drain-bias stress effects of PTFTs based on MEH-PPV at room temperature are investigated. The threshold voltage shifts toward negative direction upon the gate-bias stress, but the threshold voltage shifts toward positive direction upon the drain-bias stress. When dc voltages are simultaneously applied to the drain and gate terminals of the PTFT, the shift of threshold voltage depends on the dominant one between the gate-bias and drain-bias stresses. Results suggest that the origin of threshold voltage shift upon negative gate-bias stress is predominantly associated with holes trapped within the SiO₂ gate dielectric or at the SiO₂/Si interface due to hot-carrier emission under high gate-bias stress, while the

time-dependent charge trapping into the deep trap states in the channel region is responsible for the drain-bias stress effect of the PTFTs. However, a quantitative analysis should be developed for the detailed design of PTFT circuits in the future.

ACKNOWLEDGEMENT

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