Title	Enhanced performance of Si MOS capacitors with HfTaOxNy gate dielectric by using AlOxNy or TaOxNy interlayer
Author(s)	Li, CX; Zhang, XF; Xu, JP; Lai, PT
Citation	The 2008 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, China, 8-10 December 2008. In Conference Proceedings, 2008, p. 1-4
Issued Date	2008
URL	http://hdl.handle.net/10722/62041
Rights	IEEE Conference on Electron Devices and Solid-State Circuits Proceedings. Copyright © IEEE.

Enhanced performance of Si MOS capacitors with $HfTaO_xN_y$ gate dielectric by using AlO_xN_y or TaO_xN_y interlayer

C.X. Li[1], X.F. Zhang[2], J. P. Xu[2], and P. T. Lai[1]

1 Department of Electrical & Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong
2 Department of Electronic Science & Technology, Huazhong University of Science and Technology, Wuhan, 430074, P. R. China

Abstract – **Si MOS capacitors with HfTa oxide and oxynitride as gate dielectric were fabricated. Moreover, AlO_xN_y or TaO_xN_y was used as the interlayer between HfTa oxynitride and Si substrate to improve the electrical quality of the capacitors. Experimental results showed that the $HfTaO_xN_y$ capacitor with TaO_xN_y interlayer achieved better performance with larger capacitance and smaller leakage current than its counterpart with AlO_xN_y interlayer.**

I. INTRODUCTION

High-k dielectric materials have been extensively researched as the replacement of conventional gate dielectric SiO_2 for future complementary metal-oxide-semiconductor (CMOS) devices. Among them, HfO_2 [1-4] is the most favorable due to its relatively high dielectric constant (~25) and suitable band-gap offset (~6 eV) with Si. However, HfO_2 suffers from low crystallization temperature of ~500 ^oC [5]. And the grain boundaries of crystallized HfO_2 would provide oxygen diffusion path, causing undesirable low-k interfacial layer growth, defect generation, threshold-voltage instability and large leakage current. Previous reports showed that adding Ta [5] or Al [6-10] can increase the thermal stability and threshold-voltage stability [5-6]. Also, N and Ta incorporations can significantly increase the crystallization temperature [11]. In this work, the electrical properties of Si MOS capacitors with HfTa-based oxide or oxynitride as gate dielectric are investigated. Moreover, TaO_xN_y or AlO_xN_y is used as the interlayer between HfTa oxynitride and Si substrate to further enhance the electrical properties.

II. EXPERIMENTS

Si MOS capacitors with stacked and non-stacked gate dielectrics were fabricated on (100)-oriented n-type Si wafers with a resistivity of 0.2 ~ 0.5 Ωcm. First, the Si wafers were cleaned by the RCA method. Then, the wafers were put in diluted HF (5%) for 1 min to remove the native SiO_2. After drying the wafers by nitrogen flow, the wafers were immediately transferred into the vacuum chamber of Vacuum Discovery Deposition System made by DENTON Corporation. For the non-stacked dielectrics, HfTa or HfTaN was directly deposited on the clean Si wafers. For the stacked dielectrics, 1-nm layer of TaN_x or AlN_x was first deposited on the Si surface by DC sputtering of Ta target or Al target in an Ar +N_2 ambient at 0.03 A and 0.25 A respectively. Then, 5-nm HfTa or HfTaN was deposited at the room temperature by co-sputtering of a Hf target at 25-W RF power and a Ta target at 60-W DC power in an Ar or Ar+N_2 ambient respectively. Then, all samples received a post-deposition annealing (PDA) in N_2 (500 ml/min) at 700 ^oC for 30 s, converting HfTa into HfTaO and HfTaN into $HfTaO_xN_y$ by the residual oxygen in the N_2 ambient. Al was thermally evaporated and patterned as the gate electrode with an area of 7.85×10^{-5} cm^2. Finally, all samples were annealed at 400℃ in forming gas (N_2/H_2 = 95/5) for 25 min.

High-frequency 1-MHz capacitance-voltage (C-V) characteristics were measured at room temperature using HP4284A precision LCR meter. The gate leakage current was measured by HP 4156A precision semiconductor parameter analyzer. High-field stress (at 10 MV/cm), with the capacitors biased in accumulation by HP 4156A precision semiconductor parameter analyzer, was used to examine device reliability in terms of changes of C-V and I-V curves. All measurements were carried out under a light-tight and electrically-shielded condition.

III. RESULTS AND DISCUSSION

Fig. 1 shows the C-V curve for Si MOS capacitors with HfTa oxide (HfTaO) or oxynitride ($HfTaO_xN_y$). It is observed that the $HfTaO_xN_y$ sample has larger capacitance, indicating thinner SiO_x interfacial layer. Also, the nitrogen incorporated in $HfTaO_xN_y$ can increase the dielectric constant of the gate dielectric, thus resulting in larger capacitance [10]. Table 1 lists the extracted parameters from the 1-MHz C-V curve. The mid-gap interface density

978-1-4244-2540-2/08/$25.00 ©2008 IEEE

is determined by the Terman's method [12].The oxide charge density Q_{ox} is calculated by $V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$, where ϕ_{ms} is the work-function difference between Al and Si; V_{fb} is the flat-band voltage and C_{ox} is the accumulation capacitance. The V_{fb} of the HfTaO sample is positive, indicating negative charges in the dielectric which should be due to large quantity of O vacancy-related negative traps. On the other hand, the $HfTaO_xN_y$ sample has positive Q_{ox} and negative $V_{fb.}$ Nitrogen coupled and ionized at the O vacancies can remove the electron traps associated with the O vacancies [13]. Comparing with the HfTaO sample, the $HfTaO_xN_y$ sample has smaller D_{it}, because nitrogen in the dielectric can passivate the dangling bonds at the interface between the gate dielectric and the Si substrate, thus reducing D_{it}.

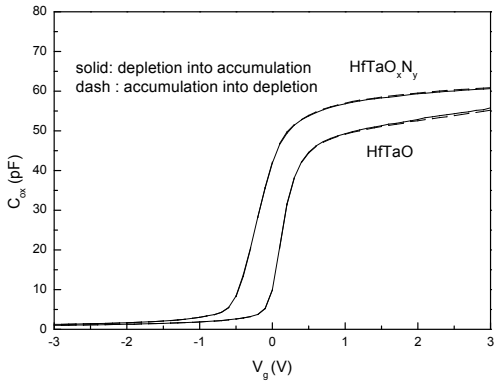


Fig. 1 C-V curve for HfTaO and $HfTaO_xN_y$ samples

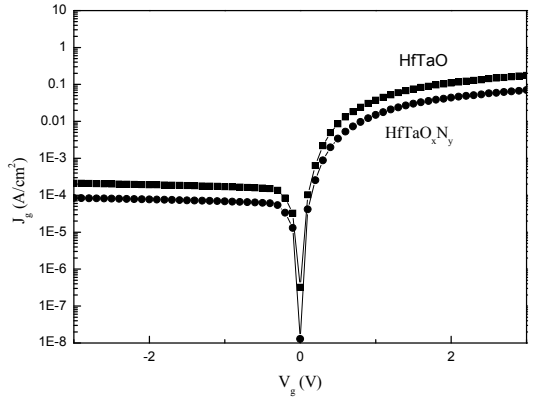


Fig.2 Leakage current for HfTaO and $HfTaO_xN_y$ samples.

Fig. 2 presents the gate leakage current of the $HfTaO_xN_y$ and HfTaO samples. Obviously the $HfTaO_xN_y$ sample has smaller leakage current than the HfTaO sample due to reduced interface states, thus reduced trap-assisted tunneling current.

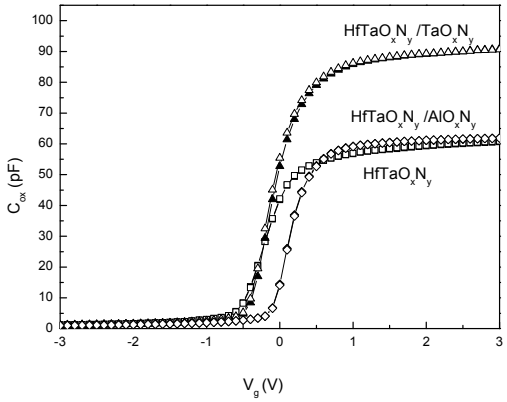


Fig. 3 C-V curves (swept in 2 directions: solid for depletion to accumulation; open for accumulation to depletion) for Al/$HfTaO_xN_y$/Si capacitors with different interlayers.

Fig. 3 shows the C-V curve of stacked $HfTaO_xN_y/TaO_xN_y$ and $HfTaO_xN_y/AlO_xN_y$ samples. Compared with $HfTaO_xN_y$ sample, the capacitances of the $HfTaO_xN_y/AlO_xN_y$ and $HfTaO_xN_y/TaO_xN_y$ samples in the accumulation are increased, which is due to suppressed growth of low-k SiO_x interlayer. The interlayer can act as oxygen reaction/diffusion barrier and thus reduce the growth of low-k SiO_x interlayer [7]. Moreover, the capacitance of the $HfTaO_xN_y/TaO_xN_y$ sample increases a lot, which should be associated with the higher dielectric constant of TaO_xN_y (~26) than that of AlO_xN_y (10). It is worth pointing out that the C-V curve of the $HfTaO_xN_y/AlO_xN_y$ sample shifts significantly to the positive side. It is possibly due to the change of coordination number of Al^{3+} from six (octahedral) to four (tetrahedral) at the SiO_x interfacial layer [5]. And tetrahedrally coordinated Al^{3+} is the source of negative charges in Al_2O_3. In this case, the Al of AlO_xN_y interlayer would diffuse into the interfacial SiO_x, thus introducing negative charges and positive V_{fb} shift [8]. On the other hand, the C-V curve of the $HfTaO_xN_y/TaO_xN_y$ sample shifts negligibly to the right, indicating no obvious charge introduction after the TaO_xN_y insertion.

Table 1 Device parameters extracted from C-V curve.

Sample	C_{ox} (pF)	EOT (nm)	V_{fb} (V)	D_{it} at midgap (cm^{-2} eV^{-1})	Q_{ox} (cm^{-2})
HfTaO	55.8	4.9	0.15	2.2×10^{12}	-1.3×10^{12}
$HfTaO_xN_y$	60.6	4.5	-0.22	6.6×10^{11}	3.6×10^{11}

Table 2 Device parameters extracted from C-V curve.

Sample	C_{ox} (pF)	EOT (nm)	V_{fb} (V)	D_{it} at midgap (cm^{-2} eV^{-1})	Q_{ox} (cm^{-2})
$HfTaO_xN_y$	60.6	4.5	-0.22	6.6×10^{11}	3.6×10^{11}
$HfTaO_xN_y/TaO_xN_y$	90.8	3.0	-0.19	3.3×10^{11}	2.8×10^{11}
$HfTaO_xN_y/AlO_xN_y$	61.9	4.4	0.11	4.3×10^{11}	-1.3×10^{12}

Table 2 shows the device parameters extracted from the 1-MHz C-V curves of the $HfTaO_xN_y$ samples. The two stacked samples have lower D_{it} than the non-stacked sample. It is partially due to the passivation of dangling bonds by the nitrogen in the TaO_xN_y and AlO_xN_y interlayers. Another reason is that the TaO_xN_y and AlO_xN_y interlayers can act as a barrier to prevent O or Hf from diffusing into the Si substrate and thus further reduce the interface-state generation [13]. Compared with the $HfTaO_xN_y/TaO_xN_y$ sample, the $HfTaO_xN_y/AlO_xN_y$ sample has larger D_{it}, which is due to the Al piling up at the high-k/Si interface which produces extra interface states [9].

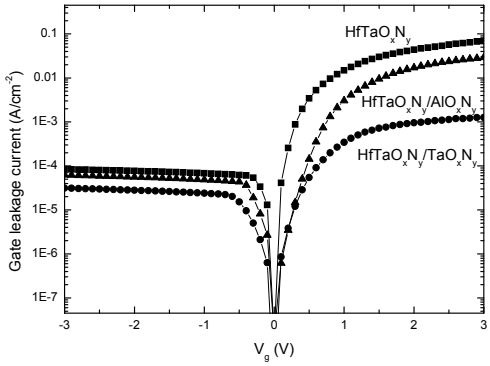


Fig. 4 Gate leakage current of the $HfTaO_xN_y$ samples.

Fig.4 shows the gate leakage current for all the samples. The gate leakage current is decreased after the TaO_xN_y or AlO_xN_y interlayer insertion, due to less interface states, thus smaller trap-assisted tunneling current. Compared to the $HfTaO_xN_y/AlO_xN_y$ sample, the $HfTaO_xN_y/TaO_xN_y$ sample has smaller gate leakage current, and hence better interface quality.

In order to study the reliability properties, the samples are biased in the accumulation region under a high-field (10 MV/cm) stress. Fig. 5 depicts the gate leakage current before and after a 3000-s stress. It is shown that the $HfTaO_xN_y/TaO_xN_y$ sample has the smallest increase of gate leakage current after the stress, because of its best interface with lowest D_{it}. Also, the bonding energy of Ta-N is 22.9 eV, which is larger than that of Al-N (20.6 eV).

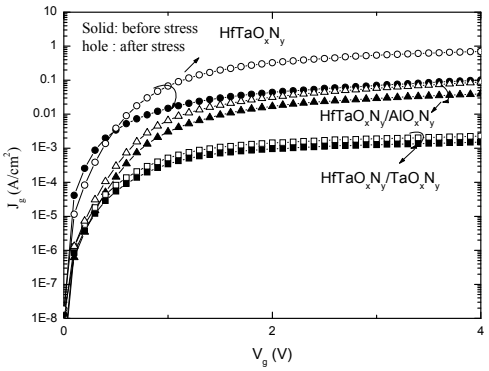
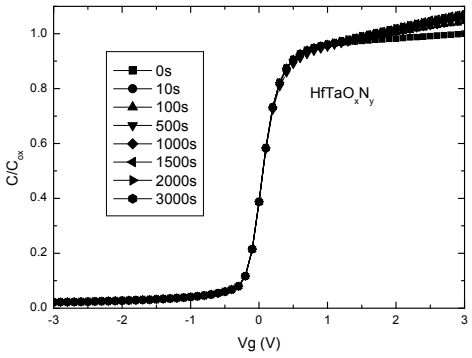
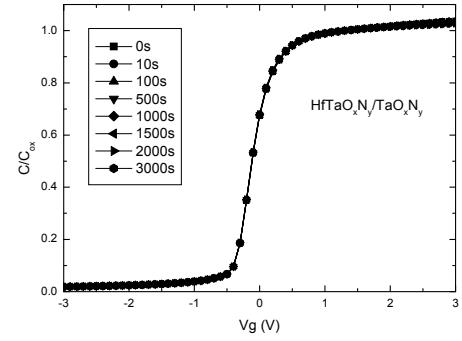


Fig. 5 Gate leakage of the $HfTaO_xN_y$ samples before and after a high-field stress at 10 MV/cm for 3000 s



6(a)



6(b)

Fig. 6 C-V curve of the $HfTaO_xN_y$ and $HfTaO_xN_y/TaO_xN_y$ samples after different stress times

Fig. 6 shows the typical C-V curves of the $HfTaO_xN_y/TaO_xN_y$ and $HfTaO_xN_y$ sample after different stress times. It is observed that the C-V curve of

$HfTaO_xN_y/TaO_xN_y$ sample hardly change compared to the $HfTaO_xN_y$ sample, further demonstrating the excellent interface quality of the TaO_xN_y interlayer. The V_{fb} shift after a 3000-s stress is 10 mV, which is consistent with others' data [6].

III. CONCLUSION

In this work, Si MOS capacitors with HfTa oxide or oxynitride as gate dielectric were fabricated. TaO_xN_y and AlO_xN_y interlayers were used to further enhance the electrical properties and reliability of the capacitors. Experiment results show that the nitrogen added in the dielectric is useful to improve the electrical properties with less mid-gap interface states and smaller gate leakage current. Moreover, adding a thin TaO_xN_y interlayer can further improve the electrical characteristics with larger capacitance, smaller gate leakage current, fewer interface states and less gate-leakage increase after high-field stress.

ACKNOWLEDGEMENT

The work is financially supported by the RGC of HKSAR, China (Project No. HKU 713308E), the HKU Small Project Funding (Project No. 200707176147), and the National Natural Science Foundation of China (Grant no. 60776016).

REFERENCES

[1] M. Gutowski, J. T. Jaffe, C. L. Liu and etc, Thermodynamic stability of high-K dielectric metal oxides ZrO_2 and HfO_2 in contact with Si and SiO_2, *Applied Physics Letters* 2002, 80(11):1897-1899

[2] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application, *IEEE IEDM*. 1999:133-136.

[3] J. Robertson, Band offsets of high dielectric constant gate oxides on silicon. *Journal of Non-Crystalline Solids* 2002, 303:94-100.

[4] E. P. Gusev, E. Cartier, D. A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt and C. D. Emic, Ultrathin high-K metal oxides on silicon: processing, characterization and integration issues, Microelectronic Engineering 2001, 59:341-349.

[5] Bae S H, Lee C H, Clark R, et al. MOS Characteristics of Ultrathin CVD HfAlO Gate Dielectrics. *IEEE Electron Device Letters*, 2003, 24(9): 556~558.

[6] C. L. Cheng, K. S. Chang-Liao, H. C. Chang and T. K. Wang, Electrical characteristic enhancement of metal-oxide-semiconductor devices by incorporating HfON buffer layer at HfTaSiON/Si interface, *Solid-State Electronics* 2006(50): 1024-1029

[7] W. Wang, W. Mizubayashi, K. Akiyama, T. Nabatame and A. Toriumi, Systematic investigation on anomalous positive V_{fb} shift in Al-incorporated high-k gate stacks, *Applied Physics Letters* 2008(92):162901-03

[8] Hoppe E E, Aita C, Suppression of near-edge optical absorption band in sputter deposited HfO_2-Al_2O_3 nanolaminates containing nonmonoclinic HfO_2. *Applied Physics Letters*, 2008, 92(14): 14912-14914.

[9] Zhu W J, Tamagawa T, Gibson M. Effect of Al inclusion in HfO_2 on the physical and electrical properties of the dielectrics, *IEEE Electron Device Letters*, 2002, 23(11): 649-651.

[10] M. Aoulaiche, M. Houssa, W. Deweerd and etc., Nitrogen incorporation in HfSi(N)/TaN gate stacks: impact on performances and NBTI, *IEEE Electron Device Letters*, 2007, 28(7):613-615.

[11] X.F. Yu, C. X. Zhu, M. F. Li, and etc., Mobility enhancement in TaN metal-gate MOSFETs using tantalum incorporated HfO2 gate dielectric, *IEEE Electron Device Letters*, 2004, 25(7): 501~503

[12] L. M. Terman, An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes, *Solid-State Electronics*, 1962, 5: 285–299

[13] N. Umezawa, K. Shiraishi, K, Torii and etc., Role of nitrogen atoms in reduction of electron charge traps in Hf-based high-k dielectrics, *IEEE Electron Device Letters,* 2007, 28(5): 363-365.