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Improved Properties of Ge MOS Capacitors with HfTiON or HfTiO Gate Dielectric by using Wet-NO Ge-Surface Pretreatment

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***Abstract* – HfTiO/GeO_xN_y and HfTiON/GeO_xN_y stack gate dielectrics are prepared by using wet-NO or wet-N_2O pretreatment on Ge substrate. Experimental results show that the wet NO pretreatment can lead to excellent interface properties, gate leakage properties and device reliability, especially for the HfTiON/GeO_xN_y dielectric. The involved mechanisms lie in the roles of N in blocking oxygen diffusion and Ge out-diffusion and suitable N incorporation in the GeO_xN_y interlayer, which effectively suppress further growth of GeO_xN_y interlayer and the growth of unstable GeO_x during subsequent processing.**

I. INTRODUCTION

For the past several decades, improved performance of silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) has been mainly accomplished by reducing the device dimensions to achieve higher packing density and less power consumption. However, saturation of drain current and unacceptable high gate leakage upon dimension shrinkage limit the prospect for future scaling. To overcome this problem, germanium channel material can be used to enhance the drive current due to its high carrier mobility, and also high-k (relative permittivity) gate dielectric with larger thickness can be utilized to decrease the gate leakage. At present, excellent reliability and high transistor performance have been demonstrated by depositing high-k gate dielectrics on Ge substrate, such as ZrO_2 [1], HfO_2 [2], GeON [3] and Ge_3N_4 [4]. A problem is that a thermodynamically unstable and low-permittivity GeO_x interlayer is inevitably grown during the formation of the high-k gate dielectric, thus increasing the equivalent oxide thickness and gate leakage current. Therefore, methods were proposed to fabricate high-quality gate dielectrics with largely suppressed growth of GeO_x, e.g. NH_3 surface nitridation [5-6], SiH_4 surface passivation [7, 8], and wet-NO thermal oxidation [9].

It is well known that Ti oxide has higher k value than Hf oxide [10]. So, addition of Ti in Hf oxide can form HfTi-based oxide with higher k value. In this work, Al/HfTiON/Ge and Al/HfTiO/Ge MOS devices are investigated and a wet NO Ge-surface pretreatment before the high-k dielectric deposition is employed to obtain good interface property. Due to formation of a GeO_xN_y interlayer by the NO surface pretreatment, diffusions of O, Ti and Hf to the substrate and out-diffusion of Ge can be effectively blocked, thus resulting in less oxide charges and interface states. Also, the post-deposition annealing (PDA) is performed in a wet-N_2 ambient to further suppress the GeO_x growth on the Ge surface [9]. Experimental results show that excellent device performance, including low gate leakage current and interface-state density, can be obtained by the proposed method.

II. DEVICE STRUCTURE

The Ge substrate was (100) Sb-doped n-type wafers from Umicore Ltd. with a resistivity of 0.040 ~ 0.047 Ωcm. The wafers were cleaned with acetone, trichloroethylene, toluene and ethanol, and lastly with de-ionized water rinsing followed by 30-s diluted HF (1:50) dipping for several cycles to remove the native oxide (GeO_x). After drying by N_2, a surface pretreatment was immediately carried out in wet N_2O or wet NO for 60 s at 500 °C (denoted as the N-N2O and N-NO samples respectively) to form a Ge oxynitride passivation layer. No surface pretreatment was done for the control sample (denoted as the N-N2 sample). The wet ambient for suppressing the growth of unstable GeO_x was realized by bubbling the pure gas through de-ionized water at 95 °C. A HfTiN film was subsequently deposited by reactive co-sputtering of Hf and Ti in an Ar + N_2 ambient at room temperature, followed by an annealing in wet N_2 ambient at 500 ^oC for 5 min to convert HfTiN into high-k HfTiON. For the purpose of comparison, another group of samples with HfTiO as high-k layer were prepared in an Ar + O_2 ambient on the passivated and non-passivated Ge surface, with the same annealing conditions, (accordingly denoted as O-N2O, O-NO and O-N2 respectively). Finally, Al was thermally evaporated

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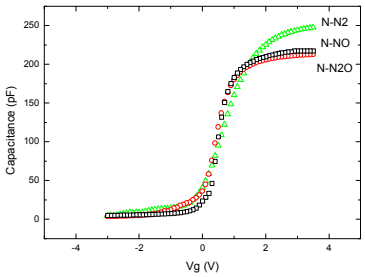
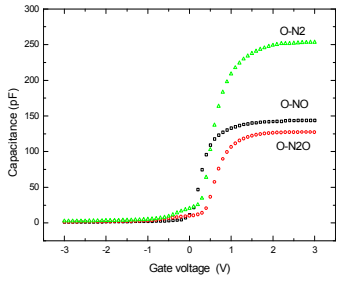
and patterned as gate electrode with an area of 7.85×10^{-5} cm^2, and followed by forming-gas annealing at 300°C for 20 min to achieve better electrical contacts.

High-frequency (HF, 1-MHz) capacitance-voltage (*C-V*) characteristics were measured at room temperature using HP4284A precision LCR meter. Gate leakage current was measured by HP 4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectrics was determined by a VASE Series Ellipsometer of J. A. Wollam Co. High-field stress (at 10 MV/cm), with the capacitors biased in accumulation by HP 4156A precision semiconductor parameter analyzer, was used to examine device reliability in terms of gate-leakage increase and flatband-voltage shift. All electrical measurements were carried out under a light-tight and electrically-shielded condition.

IV. RESULTS and DISCUSSION



1(a)



1(b)

Fig.1 High-frequency (1-MHz) C-V curves for (a) HfTiON gate-dielectric samples; (b) HfTiO gate-dielectric samples.

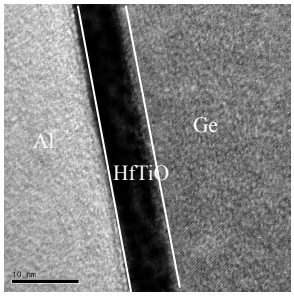
Table 1 Electrical parameters extracted from 1-MHz C-V curves for the samples.

Sample	t_{ox} (nm)	C_{ox} (pF)	CET (nm)	V_{fb} (V)	D_{it} ($cm^{-2}eV^{-1}$)	k
N-N2	6.07	249	1.09	0.21	8.1×10^{11}	24.5
N-NO	7.20	217	1.24	0.34	1.3×10^{11}	23.4
N-N2O	7.24	213	1.28	0.31	1.6×10^{11}	21.6
O-N2	7.18	253	1.08	0.29	1.3×10^{12}	25.9
O-NO	8.57	145	1.88	0.18	2.1×10^{11}	17.8
O-N2O	8.98	127	2.15	0.49	6.9×10^{11}	16.3

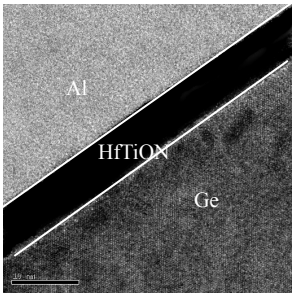
Typical HF *C-V* curves of the samples are depicted in Fig. 1. The values of gate-dielectric capacitance (C_{ox}), capacitance equivalent thickness (CET) and flat-band voltage (V_{fb}) extracted from the 1-MHz C-V curve are listed in Table 1. C_{ox} is the accumulation capacitance; CET = $A\varepsilon_{SiO2}\varepsilon_0 / C_{ox}$, where A is the area of capacitor; ε_{SiO2} and ε_0 are the permittivity of SiO_2 and vacuum respectively. Interface-state density at midgap (D_{it}) is also extracted from the 1-MHz *C-V* curve using the Terman's method for comparison purpose [11]. A large drop in C_{ox} is observed for the O-N2O and O-NO samples relative to their control sample (O-N2), indicating a large *CET*, as listed in Table 1. Fig.2 shows the TEM images of the O-N2 and N-N2 control samples. It can be seen that no visible interlayer between Ge and HfTiO or HfTiON dielectric is observed in the two control samples due to the wet annealing ambient [9]. The physical thickness (t_{ox}) of gate dielectric for the control sample is ~7.2 nm and ~6.0 nm from the TEM images, which is consistent with the measured result by ellipsometry (7.18 nm and 6.07 nm). So, the t_{ox}'s of other samples are determined by ellipsometry and listed in Table 1. The interlayer thickness between Ge and HfTiO or HfTiON can be calculated to be ~ 1.39 nm and 1.80 nm for the O-NO and O-N2O samples, and ~ 1.13 nm and 1.17 nm for the N-NO and N-N2O samples respectively, due to the same deposition conditions of HfTiO or HfTiON as the O-N2 or N-N2 control samples. Obviously, the large *CET*'s for the O-NO and O-N2O samples are ascribed to enhanced growth of GeO_xN_y interlayer with more O content during subsequent annealing due to existence of HfTiO dielectric. The largest interlayer thickness for the O-N2O sample results mainly from enhanced oxidation during N_2O pretreatment. For the N-NO and N-N2O samples with HfTiON dielectric, further growth of the GeO_xN_y interlayer is effectively suppressed by the oxygen-blocking role of the nitrogen in the dielectric, leading to only a small *CET* increase as compared with their control sample N-N2. The smaller *CET* for the O-NO sample than the O-N2O sample is attributed to the self-limiting nature of NO oxidation and better nitridation effect of NO gas (more nitrogen incorporation) [12].

The lowest D_{it}'s are found for the two NO-passivated samples (1.3×10^{11} $eV^{-1}cm^{-2}$ and 2.1×10^{11} $eV^{-1}cm^{-2}$) due to the growth of GeO_xN_y interlayer with suitable N content, which effectively blocks O diffusion to the substrate and out-diffusing of Ge, thus resulting in less structural defects near the interface. The larger D_{it} for the O-NO sample than the N-NO sample is probably due to more O content in GeO_xN_y for the former than the latter, as mentioned above. Similarly, higher D_{it} for the N_2O-passivated samples than the NO-passivated sample is also associated with out-diffusion of some Ge's due to lower N content in the interlayer and thus weakening its barrier role, especially for the O-N2O sample. The high interface-state density for the two control samples probably results from significant Ge out-diffusion which induces a large amount of defects through direct reaction of Ge with HfTiO or HfTiON near the interface [13] due to no oxynitride

interlayer. This problem is alleviated for the N-N2 sample due to N incorporation in HfTiN depostion.

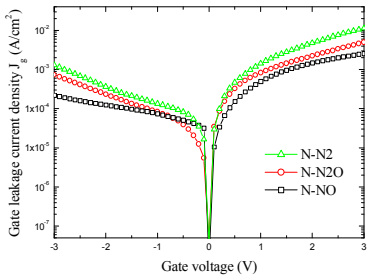


2(a)

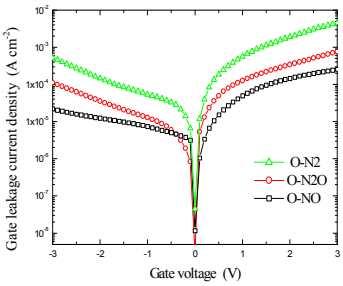


2(b)

Fig.2 TEM image of (a) Al/HfTiO/Ge control capacitor; (b) Al/HfTiON/Ge control capacitor.



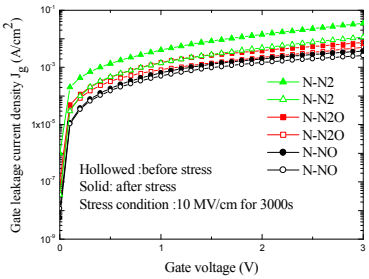
3(a)



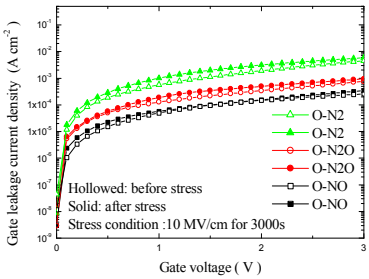
3(b)

Fig.3 Gate leakage current vs. gate voltage for (a) HfTiON gate-dielectric samples; (b) HfTiO gate-dielectric samples.

The gate-leakage properties of the samples are measured in Fig.3. The gate leakage of the HfTiO gate dielectrics is smaller than that of the HfTiON gate dielectrics due to larger physical thickness. For the two groups of gate dielectrics, the NO sample exhibits the lowest gate leakage current, e.g. 4.9×10^{-5} A/cm^2 and 8.0×10^{-4} A/cm^2 at V_g = 1 V (accumulation) for the O-NO and N-NO samples respectively, because of its superior interface property and good insulating property of the HfTiO/GeO$_x$N$_y$ or HfTiON/GeO$_x$N$_y$ gate dielectric. The higher gate leakage current of the N2O sample than that of the NO sample lies in its larger D_{it}. The largest leakage current of the control samples should be attributed to their smallest dielectric thickness and largest D_{it}.



4(a)



4(b)

Fig. 4 Gate leakage current of HfTiO and HfTiON gate-dielectric samples before and after a high-field stress (10 MV/cm for 3000 s).

Table 2 Changes of D_{it}, V_{fb} and J_g of HfTiON and HfTiO gate-dielectric MOS capacitors after stress.

Sample	ΔJ_g @V$_g$ = 1 V (A/cm^2)	ΔV_{fb} (V)	ΔD_{it} (cm^{-2}eV^{-1})
N-N2	2.6×10^{-3}	0.31	5.0×10^{11}
N-NO	1.4×10^{-4}	0.09	0.9×10^{11}
N-N2O	6.6×10^{-4}	0.16	1.9×10^{11}
O-N2	4.5×10^{-4}	0.42	6.3×10^{11}
O-NO	7.7×10^{-6}	0.13	1.7×10^{11}
O-N2O	7.8×10^{-5}	0.25	3.4×10^{11}

For the HfTiON and HfTiO gate-dielectric samples, a high-field stressing experiment (10 MV/cm for 3000 s) is done to evaluate the device reliability. Fig. 4 shows the leakage current in accumulation region before and after stressing. The stress-induced changes of D_{it}, J_g, and V_{fb} (flatband voltage) for the samples are listed in Table 2. It is clearly shown that the NO sample has the smallest increases of D_{it}, V_{fb} and J_g due to more nitrogen incorporation, and thus better interlayer quality. Compared with the N2O sample, the NO sample with more nitrogen incorporation in the passivation layer has more strong Ge-N bonds (E_{Ge-N} = 275 kJ/mol) (instead of unstable Ge-O bonds), which enhance the resistance of the dielectric against the

generation of interface states during stress, thus suppressing the increases of D_{it}, V_{fb} and J_g.

The k of the gate stack dielectric, as calculated by $\varepsilon_{SiO2} \times (t_{ox}/CET)$, is listed in Table 1 too. It should be noted that k is an equivalent k-value of the dielectric and interlayer. Based on the formula of $k = \varepsilon_{SiO2} \times t_{ox}/CET = t_{ox}/(t_{IL}/\varepsilon_{IL} + t_{die}/\varepsilon_{die})$, where t_{IL} and ε_{IL}, and t_{die} and ε_{die} are physical thickness and permittivity of the interlayer and high-k dielectric layer respectively, the relative permittivity of the GeO_xN_y interlayer can be calculated to be 6.81 and 6.56 for the O-NO and O-N2O samples respectively by using ε_{die} = 25.9 for the HfTiO dielectric layer. The ε_{IL} of the NO sample is larger than that of the N2O sample due to higher N content.

V. Conclusion

HfTiON/GeO_xN_y and HfTiO/GeO_xN_y stack gate dielectrics have been prepared on Ge substrate by Ge-surface pretreatment in wet NO or N_2O ambient. Experimental results indicate that the wet-NO surface nitridation can effectively decrease the interface-state density, and thus gate leakage current. The involved mechanisms lie in the formation of a GeO_xN_y interlayer, good GeO_xN_y/Ge interface property and insulating property of the HfTiON/GeO_xN_y or HfTiO/GeO_xN_y dielectric. Furthermore, it is found that the HfTiON/GeO_xN_y dielectric has better interface properties and higher equivalent k value than the HfTiO/GeO_xN_y dielectric due to good O-blocking role of nitrogen and more N incorporation in the GeO_xN_y interlayer, thus suppressing the growth of the interlayer. In addition, high-field stressing shows that the HfTiON/GeO_xN_y dielectric with wet-NO surface pretreatment exhibits excellent device reliability (smaller increases of D_{it}, V_{fb} and J_g after electrical stress) through the formation of more strong Ge-N bonds. Therefore, the wet-NO surface pretreatment plus wet-N_2 post-deposition anneal should be a promising method for fabricating high-k HfTiON/GeO_xN_y gate-dielectric Ge MOSFETs with excellent interface and gate-leakage properties, and device reliability.

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