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Improved electrical properties of Ge metal-oxide-semiconductor capacitor with HfTa-based gate dielectric by using TaO_xN_y interlayer

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HfTa-based oxide and oxynitride with or without TaO_xN_y interlayer are fabricated on Ge substrate to form metal-oxide-semiconductor (MOS) capacitors. Their electrical properties and reliabilities are measured and compared. The results show that the MOS capacitor with a gate stack of HfTa-based oxynitride and thin TaO_xN_y interlayer exhibits low interface-state/oxide-charge densities, low gate leakage, small hysteresis, small capacitance equivalent thickness (~0.94 nm), and high dielectric constant (~24). All these should be attributed to the blocking role of the TaO_xN_y interlayer against penetration of O into the Ge substrate and interdiffusions of Hf, Ge, and Ta, thus effectively suppressing the formation of unstable low-*k* GeO_x and giving a superior TaO_xN_y/Ge interface. Moreover, incorporation of N into both the interlayer and high-*k* dielectric greatly improves device reliability through the formation of strong N-related bonds. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2954012]

With the continuous scaling down of the dimensions of metal-oxide-semiconductor field-effect transistor (MOSFET), silicon is approaching its fundamental scaling limits. Germanium is an alternative candidate for future channel material because of its high carrier mobility.[1–3] However, unlike Si oxide, the thermodynamically unstable and soluble Ge oxide hinders the development of high-quality Ge MOSFET. Recently, Ge-based MOS capacitors and transistors with high-permittivity (high-*k*) stacked gate dielectrics using a thin germanium oxynitride (GeO_xN_y) interlayer have shown superior electrical properties.[4–6] It has been shown that the GeO_xN_y interlayer provides a stable and smooth interface with improved electrical properties. However, its lower *k* value limits the scalability of Ge MOS devices, even as an interlayer. More recently, Lu *et al.*[7] reported that an ultrathin tantalum nitride film deposited between high-*k* dielectric and Si substrate could suppress the formation of the SiO_x interlayer during subsequent high-temperature annealing. This is because tantalum nitride can function as a diffusion barrier and can be oxidized to form nonconductive TaO_xN_y after annealing in O_2. Moreover, Sugawara *et al.*[8] demonstrated that a thin plasma-synthesized TaON interlayer on Ge could reduce stress-induced flatband-voltage shift. Since TaO_xN_y has a high *k* value (~26) and high thermal stability,[9] it should also be a promising candidate as the interlayer between high-*k* dielectric and Ge substrate. In this work, a thin TaN_x layer is deposited by reactive sputtering prior to HfTa-based oxide or oxynitride deposition. The thin TaN_x is used to suppress the formation of inferior GeO_x and interdiffusions of relevant elements during the annealing of the deposited high-*k* dielectric, and at the same time TaN_x itself is converted to TaO_xN_y during the annealing. Ta is intentionally added to improve the crystallization temperature and dielectric constant of Hf-based oxide and oxynitride.[10] As a result, excellent electrical properties such as low interface-state density, low gate leakage, and high reliability are obtained for the Ge MOS capacitors with HfTaON/TaO_xN_y and HfTaO/TaO_xN_y gate stacks.

N-type (100) Ge wafers with a resistivity of 0.040–0.047 Ω cm were cleaned in organic solvents and rinsed in de-ionized water followed by a 30 s diluted HF (1:50) dipping for several cycles to remove the native oxide (GeO_x). After drying in N_2, the wafers were immediately transferred into Denton Vacuum Discovery Deposition System. First, a ~1 nm TaN_x interlayer was deposited by reactive sputtering of Ta in an Ar+N_2 ambient (Ar:N_2=12:18), followed by the deposition of a 5 nm HfTaO or HfTaN by cosputtering of Ta and Hf in an Ar+O_2 (Ar:O_2=24:3) or Ar+N_2 (Ar:N_2=24:6, a smaller ratio used to incorporate more nitrogen in the dielectric) ambient, respectively (denoted as HfTaO/TaON or HfTaON/TaON sample). For comparison, a 6 nm HfTa or HfTaN was directly deposited on the cleaned Ge substrate without the TaN_x interlayer as control samples (denoted as HfTaO or HfTaON sample). A postdeposition annealing was carried out in wet N_2 (500 ml/min) at 500 °C for 5 min to transform the films into oxides or oxynitrides (i.e., HfTaO, HfTaON, and TaO_xN_y) by using the oxygen in water vapor.[11] The wet-N_2 atmosphere was realized by bubbling pure N_2 through de-ionized water at 95 °C with a flow rate of 500 ml/min. Subsequently, Al was evaporated and patterned by lithography as gate electrodes with an area of 7.85×10^{-5} cm^{-2}. Finally, forming-gas annealing was performed at 280 °C for 20 min. Physical thicknesses of the gate dielectrics for the samples were determined by a multiwavelength ellipsometer. All electrical measurements were carried out under a light-tight and electrically shielded condition using HP4284A precision *LCR*

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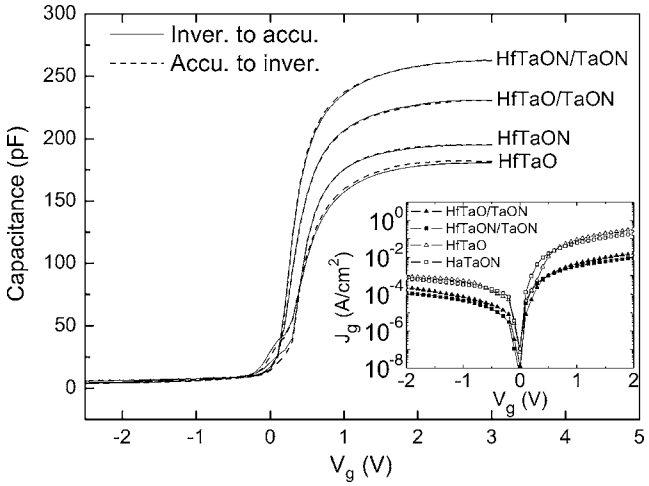

FIG. 1. Typical high-frequency *C-V* curves of the Ge MOS capacitors under dark condition at room temperature, swept in both directions at a frequency of 1 MHz. Inset is gate leakage current density of the samples.

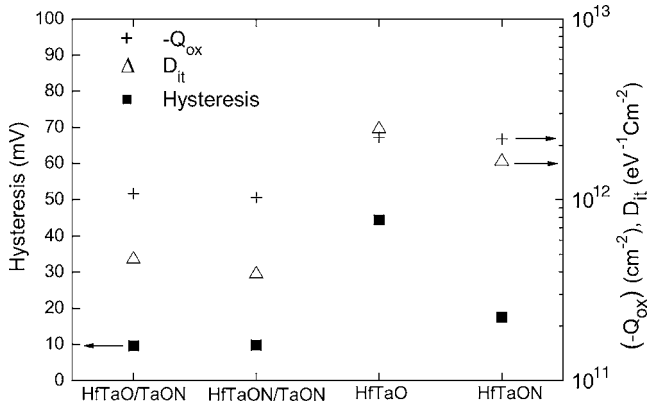

FIG. 2. Hysteresis, interface-state density and equivalent oxide-charge density extracted from the HF *C-V* curves of the Ge MOS capacitors.

meter and HP4156A precision semiconductor parameter analyzer.

Typical HF (1 MHz) *C-V* curves of the samples, swept in bidirections at 1 MHz, are shown in Fig. 1. The oxide capacitance (C_{ox}) obtained by correcting for frequency dispersion from maximum accumulation capacitance,[12] physical thickness (t_{phys}), capacitance effective thickness (CET) and equivalent k value ($=C_{ox}t_{phys}/\varepsilon_0 A$) for all the samples are extracted and listed in Table I. An obvious distortion is observed in the region from depletion to inversion of the *C-V* curves for the two samples without the TaO_xN_y interlayer, especially for the HfTaO sample, but does not exist for the two samples with a thin TaO_xN_y interlayer. This should be associated with significant interfacial defects originated from the interdiffusion between the gate dielectric and substrate, and the growth of a low-k GeO_x interlayer, especially for the HfTaO sample. Therefore, it can be concluded that the TaO_xN_y interlayer can effectively block the oxidation of Ge surface and thus suppress the formation of unstable GeO_x. Another fact is that C_{ox} of the oxynitrides is larger than that of their oxide counterparts, indicating that larger k values have been obtained for the oxynitrides than the oxides for almost the same physical thickness, with the largest k value ($\sim$24) and the smallest CET ($\sim$0.94 nm) for the $TaHfON/TaO_xN_y$ sample. Furthermore, the *C-V* hysteresis, the equivalent oxide-charge density [$Q_{ox}=-C_{ox}(V_{fb}-\varphi_{ms})/q$, where the work-function difference ϕ_{ms} between Al gate and n-Ge substrate is calculated to be 0.0706 V] and the interface-state density near midgap (D_{it}) estimated from the HF *C-V* curve by the Terman's method[13] are depicted in Fig. 2. As compared to the control samples, D_{it} is obviously reduced by inserting a thin TaO_xN_y interlayer between the high-k gate dielectrics and Ge substrate, especially for the $HfTaON/TaO_xN_y$ sample. Moreover, the hysteresis and Q_{ox} are less for the two samples with the TaO_xN_y interlayer than the control samples, with $HfTaON/TaO_xN_y$ sample being the smallest. The negative Q_{ox} might arises from OH^-, which is related to the wet-annealing ambient,[14,15] the acceptorlike interface states and electron traps in the oxide since the oxide charge density calculated from flatband voltage is a net effect of all charges in the oxide and at the interface. The smaller Q_{ox} of HfTaO/TaON and HfTaON/TaON samples should be partly attributed to their smaller D_{it} (hence, less acceptorlike interface-state charges), as shown in Fig. 2. Further examination of the data in Fig. 2 implies the HfTaO/TaON and HfTaON/TaON samples having more positive charges than the samples without the TaON interlayer because their Q_{ox} reduction is only a portion of their D_{it} reduction. These additional positive charges could be introduced due to the HfTaO/TaON and HfTaON/TaON interfaces.

TABLE I. Physical parameters extracted from the HF C-V curves of the Ge MOS capacitors.

Sample	C_{ox} (pF)	t_{phys} (nm)	CET (nm)	Equivalent k
$HfTaO/TaO_xN_y$	253	5.86	1.07	21.4
$HfTaON/TaO_xN_y$	289	5.83	0.94	24.2
HfTaO	201	5.96	1.35	17.2
HfTaON	240	6.06	1.13	20.9

The inset of Fig. 1 shows the gate-leakage properties of the samples. The two samples with the TaO_xN_y interlayer have lower leakage current than their control samples. Moreover, the oxynitride samples have lower leakage current than their oxide counterparts, with the $HfTaON/TaO_xN_y$ sample being the lowest and HfTaO sample being the highest (3.3×10^{-3} and 8.9×10^{-2} A cm^{-2} at $V_g=V_{fb}+1$ V, respectively). It was reported that the incorporation of nitrogen into high-k dielectrics could reduce their leakage current by inhibiting species interdiffusion and changing the local coordination of high-k material, thus suppressing the onset of crystallization.[16] So, the smaller leakage current for the oxynitride samples should be ascribed to the N incorporation. In fact, this is closely associated with the D_{it} and Q_{ox} of the samples shown in Fig. 2.

A high-field stress at 10 MV/cm [$=(V_g-V_{fb})/t_{phys}$] for 3600 s, with the capacitors biased at accumulation, is used to examine the reliability of the samples. The leakage current density (J_g) is measured for all the samples before and after the stress, as shown in Fig. 3. The V_{fb} shift after the stress is extracted from the HF *C-V* curves measured before and after the stress, as shown in the inset of Fig. 3. Increase of the leakage current and shift of flatband voltage after the stress are larger for the control samples than the samples with the TaO_xN_y interlayer because of an unstable GeO_x layer grown at the interface of the former samples. Among all the samples, the $HfTaON/TaO_xN_y$ sample exhibits the best reliability due to the formation of strong N-related bonds by

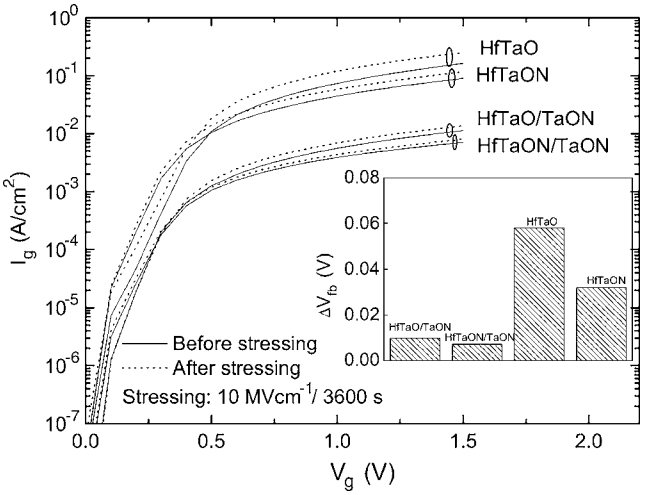

FIG. 3. Gate-leakage increase and flatband-voltage shift (insrt) of the Ge MOS capacitors after a high-field stressing at 10 MV/cm for 3600 s, with the samples biased at accumulation.

significant incorporation of N into both the interlayer and high-k gate dielectric.

Therefore, the thin TaO_xN_y interlayer can give excellent device performances due to its strong barrier role against diffusions of Hf, Ta, Ge, and O, and its good interface properties with the Ge substrate. Moreover, when the high-k dielectric layer is oxynitride, the electrical properties and reliability of the devices are further improved due to the formation of strong N-related bonds.

The electrical properties and reliability of HfTa-based oxide and oxynitride with or without TaO_xN_y interlayer are investigated as the gate dielectric of Ge MOS capacitors. The thin TaO_xN_y interlayer can effectively block the interdiffusions of Ge, Hf, and Ta and also the penetration of oxygen into the Ge substrate, thus greatly suppressing the growth of unstable low-k GeO_x during high-temperature annealing, and improving the interface quality and reliability of the devices. Low interface-state density and low leakage current have been achieved for the devices with $HfTaON/TaO_xN_y$ or $HfTaO/TaO_xN_y$ gate stack. Particularly, the sample with $HfTaON/TaO_xN_y$ gate stack exhibits higher dielectric constant (~24) and better high-field reliability than the other samples while keeping small CET (~0.94 nm), D_{it}, Q_{ox}, and low leakage current. Therefore, the $HfTaON/TaO_xN_y$ stack structure is a promising gate dielectric for making advanced small-sized Ge MOSFET with excellent electrical performances and high reliability.

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[1] A. Ritenour, S. Yu, M. L. Lee, N. Lu, Wu. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, Tech. Dig. - Int. Electron Devices Meet. **2003**, 18.2.1.
[2] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, Tech. Dig. - Int. Electron Devices Meet. **2006**, 655.
[3] S. Joshi, C. Krug, D. Heh, H. J. Na, H. R. Harris, J. W. Oh, P. D. Kirsch, P. Majhi, B. H. Lee, H.-H. Tseng, R. Jammy, J. C. Lee, and S. K. Banerjee, IEEE Electron Device Lett. **28**, 308 (2007).
[4] C. O. Chui, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, IEEE Trans. Electron Devices **53**, 1509 (2006).
[5] C. X. Li, P. T. Lai, and J. P. Xu, Microelectron. Eng. **84**, 2340 (2007).
[6] J. J. Chen, N. A. Bojarczuk, H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, IEEE Trans. Electron Devices **51**, 1441 (2004).
[7] J. Lu, Y. Kuo, J. Y. Tewg, B. Schueler, Vacuum **74**, 539 (2004).
[8] T. Sugawara, Y. Oshima, R. Sreenivasan, and P. C. Mclntyre, Appl. Phys. Lett. **90**, 112912 (2007).
[9] H. Jung, K. Im, H. Hwang, and D. Yang, Appl. Phys. Lett. **76**, 3630 (2000).
[10] X. Yu, C. Zhu, M. F. Li, A. Chin, A. Y. Du, W. D. Wang, and D. L. Kwong, Appl. Phys. Lett. **85**, 2893 (2004).
[11] K. Muraoka, in *13th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, 2005 (unpublished), p. 37.
[12] K. J. Yang and C. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999).
[13] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, Hoboken, NJ, 1982), p. 325.
[14] J. P. Xu, P. T. Lai, C. X. Li, X. Zou, and C. L. Chan, IEEE Electron Device Lett. **27**, 439 (2006).
[15] H. Yano, F. Katafuchi, T. Kimoto, and H. Matsunami, IEEE Trans. Electron Devices **46**, 504 (1999).
[16] P. S. Lysaght, J. Barnett, G. I. Bersuker, J. C. Woicik, D. A. Fischer, B. Foran, H. H. Tseng, and R. Jammy, J. Appl. Phys. **101**, 024105 (2007).