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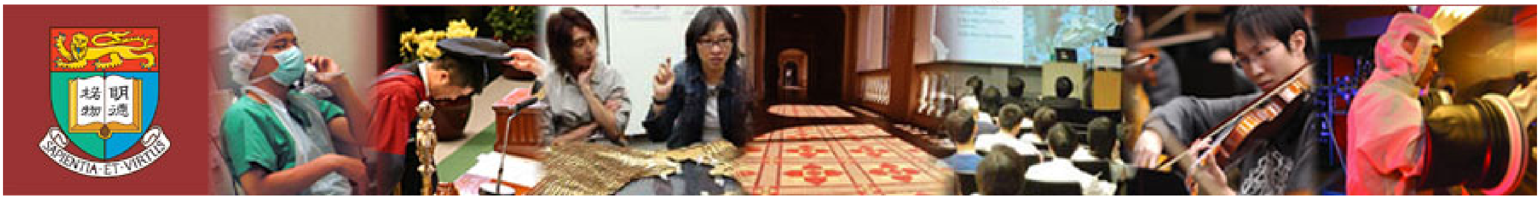

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Citation	Applied Physics Letters, 2007, v. 90 n. 16
Issued Date	2007
URL	http://hdl.handle.net/10722/57474
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APPLIED PHYSICS LETTERS **90**, 163502 (2007)

Suppressed growth of unstable low-*k* GeO_x interlayer in Ge metal-oxide-semiconductor capacitor with high-*k* gate dielectric by annealing in water vapor

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(Received 8 December 2006; accepted 15 March 2007; published online 16 April 2007)

The effects of water vapor added in the N_2 annealing of high-*k* HfTiON gate dielectric on Ge metal-oxide-semiconductor capacitor are investigated. Both transmission-electron microscopy and ellipsometry indicate that, as compared to dry-N_2 annealing, the wet-N_2 annealing can greatly suppress the growth of unstable low-*k* GeO_x at the dielectric/Ge interface, thus resulting in smaller equivalent dielectric thickness, as well as less interface states and dielectric charges. All these are attributed to the hydrolyzable property of GeO_x in water. Moreover, the wet-N_2 annealed capacitor has ten times lower gate-leakage current due to its better dielectric morphology as confirmed by atomic force microscopy. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2723074]

As the scaling of classical Si metal-oxide-semiconductor (MOS) device continues, the fundamental limit of Si technology is in sight. In order to further enhance the current-drive capability of the device, alternative channel materials are needed for better performance. One of these materials is Ge, which is currently under investigation as a replacement for Si. The main advantages of Ge are its high electron and hole mobilities for carrier transport. However, there is an intrinsic problem in the formation of gate dielectric on Ge substrate: Ge oxide is known to be thermally unstable, water hydrolyzable, and has poor electrical properties. Recently, high-*k* gate dielectrics on Si substrate have been proved to significantly reduce the leakage current as compared to the traditional SiO_2/Si system, while still maintaining excellent reliability and high transistor performances. Therefore, deposition of high-*k* dielectric as gate oxide on Ge substrate has received much attention. Up to now, several metal oxides, e.g., ZrO_2,[1] $HfAlO_x$,[2] HfO_2,[3–5] and GeON,[6] have been demonstrated to be suitable for Ge MOS devices. However, it is inevitable to grow a GeO_x interlayer during the preparation of these gate dielectrics because they are usually formed in an oxidizing ambient. The unstable GeO_x deteriorates the quality of the Ge/dielectric interface, thus increasing the interface-state density and gate-leakage current. Therefore, it is highly desirable to prepare high-*k* gate dielectric in a non oxidizing ambient to suppress the growth of the GeO_x interlayer. In this work, we demonstrate that this goal can be easily achieved by annealing the high-*k* gate dielectric in water vapor because GeO_x is highly soluble in water even at room temperature. The electrical characteristics of the relevant MOS capacitors and the effects of the wet-N_2 annealing on dielectric performance are analyzed.

Ge substrate used was (100) Sb-doped *n*-type wafers with a resistivity of 0.4–0.6 Ω cm. The wafers were cleaned with acetone, trichloroethylene, toluene, and ethanol and rinsed with deionized water, followed by 60 s diluted HF (1:50) dipping for several cycles to remove the unstable native oxide (GeO_x). After drying, HfTiN thin film was deposited by reactive cosputtering method in an $Ar+N_2$ ambient ($Ar:N_2=48:12$) with a Hf target at 65 W and a Ti target at 25 W, and a chamber pressure of 1 Pa. To minimize the interlayer growth, postdeposition annealing was carried out at 550 °C for 5 min in a dry-N_2 or wet-N_2 ambient instead of O_2 (denoted as DN2 and WN2 samples, respectively). The wet-N_2 atmosphere was realized by bubbling pure N_2 through de-ionized water at 95 °C with a flow rate of 500 ml/min. Then, Al was thermally evaporated and patterned as gate electrode with an area of 7.85×10^{-5} cm^2. Finally, forming-gas annealing was performed at 300 °C for 20 min.

High-frequency (1 MHz) capacitance-voltage (*C*-*V*) characteristics were measured at room temperature using HP4284A precision impedance meter. Gate-leakage current was measured by HP4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectrics was determined by ellipsometry and listed in Table I. Structure of the films was determined by transmission-electron microscopy (TEM). All electrical measurements were carried out under a light-tight and electrically shielded condition.

The TEM images in Fig. 1 show that both Ge MOS capacitors have a HfTiON film thickness of 9.1 nm. Moreover, Fig. 1(a) depicts a thin GeO_x interlayer (0.9 nm) between Ge and HfTiON in the WN2 sample, while a thicker GeO_x interlayer (2.7 nm) exists in the DN2 sample, as shown in Fig. 1(b). This phenomenon indicates that the wet-N_2 annealing is effective for suppressing the oxidation of Ge and thus the growth of the interlayer (GeO_x). This is due to the well-known hydrolyzable property of GeO_x in water. On the other hand, the total physical thicknesses (t_{ox}) of gate dielectric for the DN2 and WN2 samples measured by ellipsometry are 11.8 and 10.0 nm, respectively. These results are consistent with those obtained from the TEM images in

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TABLE I. Gate-dielectric capacitance, equivalent dielectric thickness, physical thickness, flatband voltage, and dielectric-charge and interface-state densities.

Sample	C_{ox} (pF)	t_{eq} (nm)	t_{ox} (nm)	V_{fb} (V)	D_{it} at midgap ($cm^{-2}\,eV^{-1}$)	Q_{ox} (cm^{-2})
DN2	79	3.4	11.8	0.25	7.9×10^{11}	-1.3×10^{12}
WN2	114	2.4	10.0	0.13	2.8×10^{11}	-7.3×10^{11}

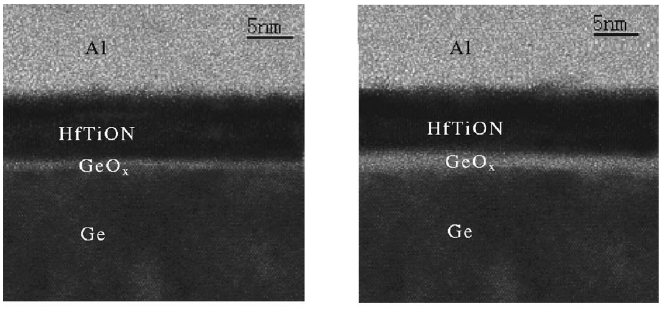
Fig. 1. It should be noted that this wet-N_2 annealing is also applicable when thinner HfTiON films with high quality can be prepared by more advanced deposition techniques.

Typical HF *C-V* curves of the two samples are depicted in Fig. 2. Distortion is observed in the depletion and inversion regions of the *C-V* curve for the DN2 sample, indicating poor interface quality. This should be associated with significant interfacial defects originating from the growth of the GeO_x interlayer during the dry-N_2 annealing. On the other hand, the growth of the GeO_x interlayer can be effectively suppressed when the annealing is carried out in a wet-N_2 ambient, as shown by the smooth *C-V* curve of the WN2 sample, implying less interface and near-interface traps.

The values of gate-dielectric capacitance (C_{ox}), equivalent dielectric thickness (t_{eq}), and flatband voltage (V_{fb}) extracted from the 1 MHz *C-V* curves are listed in Table I. Approximate interface-state density at midgap (D_{it}) is also extracted from the 1 MHz *C-V* curve using the Terman method for comparison purpose only.[7] Equivalent dielectric-charge density (Q_{ox}) is calculated as $-C_{ox}(V_{fb}-\varphi_{ms})/q$, where the work-function difference φ_{ms} between Al and Ge is calculated to be 0.053 V. It can be noted from Table I that t_{eq} of the DN2 sample is larger than that of the WN2 sample, further indicating the excessive growth of GeO_x interlayer during the dry-N_2 annealing for the DN2 sample. Lower D_{it} is found for the WN2 sample than the DN2 sample due to suppressed growth of GeO_x interlayer in the wet ambient. Obviously, the high interface-state density for the DN2 sample probably results from the unstable GeO_x interlayer, which can lead to Ge atoms outdiffusing into the HfTiON film near the interface to generate a large amount of defects.[8] Therefore, the wet-N_2 annealing is favorable for suppressing the growth of the GeO_x interlayer and thus decreasing D_{it} because GeO_x once grown could be easily hydrolyzed in the wet ambient. The negative Q_{ox} of the WN2 sample should be largely related to the wet annealing ambient and the final forming-gas annealing.[9] The origin of the negative charges might be OH^-, which cannot diffuse out from the interface at temperature less than 550 °C.[10] For the DN2 sample, the negative Q_{ox} should be mainly due to the high acceptorlike interface and near-interface trap densities of the GeO_x interlayer because Q_{ox} includes not only fixed charge but also interface and near-interface trap charges.[10] Therefore, a larger $|Q_{ox}|$ of the DN2 sample results in a larger flatband voltage shift than the WN2 sample.

The dielectric constants ε_{ox} of the gate stack dielectric, as calculated by $\varepsilon_{SiO_2}(t_{ox}/t_{eq})$, are found to be 16.3 and 13.5 for the WN2 and DN2 samples, respectively. The difference between the two dielectric constants is due to the different thicknesses of the GeO_x interlayer, based on the formula of $\varepsilon_{ox}=\varepsilon_{SiO_2}(t_{ox}/t_{eq})=t_{ox}/(t_{GeO_x}/\varepsilon_{GeO_x}+t_{HfTiON}/\varepsilon_{HfTiON})$. Obviously, the larger the thickness of the low-*k* GeO_x interlayer (t_{GeO_x}), the smaller is ε_{ox}. Therefore, it is very important to suppress the growth of the GeO_x interlayer and thus achieve large ε_{ox} for the gate dielectric like in the WN2 sample.

The gate-leakage properties of the two samples are shown in the inset of Fig. 2. The DN2 sample has a large gate leakage of 1.5×10^{-4} A/cm^2 at $V_g=-1$ V due to large D_{it} associated with the unstable GeO_x interlayer. On the other hand, even with a thinner gate dielectric, the WN2 sample displays a much lower gate leakage of 1.4×10^{-5} A/cm^2 at $V_g=-1$ V, thus exhibiting superior bulk and interface properties than the DN2 sample. This should be attributed to the suppressed growth of the unstable GeO_x interlayer and thus smoother dielectric surface, because it has been reported that the roughness at the dielectric/gate interface can significantly increase the gate-leakage current.[11] Atomic force microscopy (AFM) images of the HfTiON film surface after the wet-N_2 and dry-N_2 annealings are shown in Fig. 3. The rms surface roughness of the dry-N_2 annealed sample (0.56 nm) is much larger than that of the wet-N_2 annealed sample (0.21 nm).



(a) (b)

FIG. 1. TEM images of MOS capacitor. (a) WN2 sample and (b) DN2 sample.

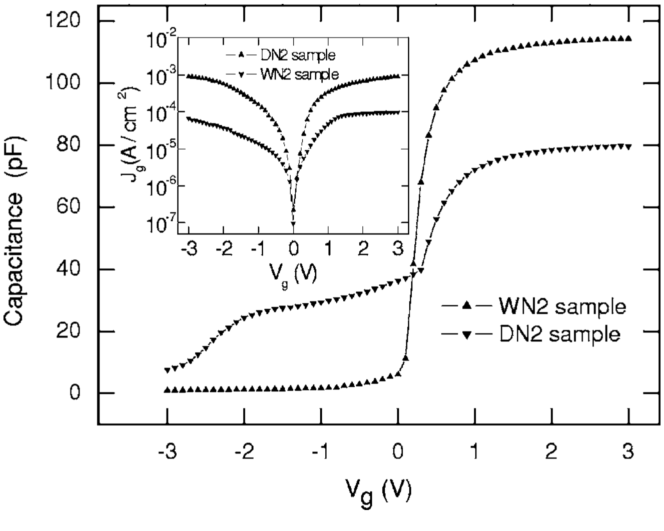
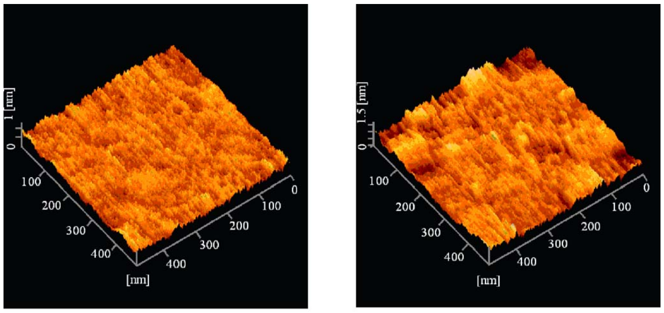


FIG. 2. High-frequency (1 MHz) *C-V* curves of the samples. The inset shows their gate-leakage current density vs gate voltage.



(a) (b)

FIG. 3. (Color online) AFM images ($0.5 \times 0.5\ \mu m^2$) of HfTiON films with (a) wet-N_2 annealing and (b) dry-N_2 annealing.

The reason is that owing to the stronger growth of the GeO_x interlayer during the dry-N_2 annealing, more Ge atoms can outdiffuse from the GeO_x interlayer to the high-*k* dielectric film and then pile up at the surface, resulting in larger roughness.

In summary, the effects of postdeposition annealing in water vapor on the physical and electrical properties of Ge MOS capacitors with HfTiON gate dielectric have been investigated. Wet-N_2 annealing for deposited HfTiON film can induce a great reduction of interface-state/dielectric-charge densities and gate-leakage current due to the suppressed growth of unstable GeO_x interlayer in the wet ambient. This is attributed to the well-known hydrolyzable property of GeO_x in water. Therefore, depositing HfTiN film followed by wet-N_2 annealing to form HfTiON gate dielectric is a promising process for fabricating advanced Ge MOS transistors with high-*k* gate dielectric.

This work is financially supported by the National Natural Science Foundation of China (NSFC) under Grant No. 60576021, the Research Grants Council (RGC) of Hong Kong Special Administrative Region (HKSAR), China under Project No. HKU7142/05E, and the University Development Fund (Nanotechnology Research Institute, 00600009) of The University of Hong Kong.

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