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Improved high-field reliability for a SiC metal–oxide–semiconductor device by the incorporation of nitrogen into its HfTiO gate dielectric

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Materials with high dielectric constant (k) have been used in SiC-based metal–oxide–semiconductor (MOS) devices to reduce the electric field in the gate dielectric and thus suppress a high-field reliability problem. In this work, high-k gate dielectrics $Hf_xTi_{1-x}O_2$ and $Hf_xTi_{1-x}ON$ are applied in SiC MOS devices and an ultrathin thermally grown SiO_2 is used as an interlayer between SiC and the high-k materials to block electron injection from SiC into the low-barrier high-k materials. Incorporating nitrogen into the Hf-Ti oxide (by adding nitrogen gas during its sputtering) stacked with a SiO_2 interlayer ($Hf_xTi_{1-x}O/SiO_2$) results in a better gate dielectric for the MOS capacitor, such as smaller frequency dispersion in the capacitance-voltage curve, less oxide charges, and better interface quality. Moreover, the nitrogen incorporation increases the dielectric constant of the oxide, but causes higher dielectric leakage, which can be suppressed by the SiO_2 interlayer. High-field stress under constant electric field is performed on the stacked/nonstacked Hf-Ti oxides and oxynitrides, and it turns out that the two oxynitrides show a much smaller flatband shift and a less stress-induced leakage current compared with the two oxides. Based on these results, the $Hf_xTi_{1-x}ON/SiO_2$ stack could be a promising high-k gate dielectric for SiC MOS devices with enhanced reliability. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2776254]

I. INTRODUCTION

SiC has been a dominant semiconductor material used in high-temperature, high-power devices for a long time.[1,2] Superior-quality SiO_2 thermally grown on SiC provides SiC significant advantages over other wide-bandgap materials. However, there are still some obstacles for the SiO_2/SiC MOS devices. First, SiO_2 growth for SiC is much slower than for Si, thus requiring more thermal budget.[3] Second, excess carbon clusters originated from SiC oxidation create oxide and interface traps, which make the interface-trap density D_{it} normally two orders of magnitude higher than that of SiO_2/Si devices.[4] Third, when SiC ($k=9.6-10$) reaches its critical field of 3 MV/cm, the electric field in SiO_2 ($k=3.9$) is 7.4–7.7 MV/cm (the ratio of the two electric fields is equal to the inverted ratio of the dielectric constants of the two materials) and such a high electric field leads to a severe reliability problem for the SiO_2 dielectric.[5] High-k dielectrics can be applied on SiC to alleviate the electric field in the dielectric and some examples are Al oxides/oxynitrides,[6,7] HfO_2,[8] TiO_2,[9] Ta_2O_5,[10] and Ta_2Si.[11] Among these materials, Al oxides/oxynitrides have a relatively low dielectric constant (<10).[8] HfO_2 ($k=20-25$) is one of the most popular high-k materials applied on Si due to its good thermal stability with poly-Si.[12] TiO_2 has a much higher dielectric constant (50–80), which makes adding Ti to HfO_2 a promising way to further increase the dielectric constant for Si MOS devices.[13] Moreover, incorporating nitrogen in the Hf-based high-k dielectrics of Si MOS devices can improve their thermal stability and resistance against boron penetration.[14,15]

In this work, Hf-Ti oxides and oxynitrides are applied to SiC MOS devices. Nitrogen atoms are added into hafnium-titanium oxide to give a more reliable high-k dielectric with a higher dielectric constant. Moreover, an ultrathin thermally grown SiO_2 is used as an interlayer between the high-k dielectrics and SiC for effectively blocking the injection of electrons from SiC into the high-k materials and thus suppressing the dielectric leakage. It is found that the $Hf_xTi_{1-x}ON/SiO_2$ stack could be a promising high-k gate dielectric for high-reliability SiC MOS devices.

II. DEVICE FABRICATION

n-type (0001) Si-face 6H-SiC wafers were purchased from Cree, Inc. They had an n-type epitaxial layer with a doping concentration of 6.5×10^{15} cm^{-3}. A SiO_2 interlayer was thermally grown on two SiC wafers in dry oxygen at 1100 °C for 5 min and its thickness was 3.3 nm as measured by spectroscopic ellipsometry (SE) with an error of 0.5%–3%. After that, one SiO_2/SiC wafer and one fresh SiC wafer were exposed to a cosputtering of Hf and Ti in an ambient of $Ar:O_2$ (24:6) for depositing a layer of the high-k dielectric ($Hf_xTi_{1-x}O_2$). Two similar wafers were also exposed to the same cosputtering but in an ambient of $Ar:N_2$ (24:6) to form the nitrided high-k dielectric ($Hf_xTi_{1-x}ON$). Then, the four samples were annealed in dry nitrogen at 700 °C for 6 min to improve their dielectric quality. Finally, Al was deposited by thermal evaporation as a gate electrode and backcontact. By SE, the thickness of $Hf_xTi_{1-x}O_2$ was 14.5 nm and that of $Hf_xTi_{1-x}ON$ was 19.6 nm. The area of the resulting MOS capacitors was 7×10^{-5} cm^2. Capacitance-voltage characteristics were measured by using HP4284A LCR meter with a bias sweep rate of 0.1 V/s. The current-voltage characteristics were measured by an HP4156B semiconductor parameter analyzer. All measurements were conducted in a dark ambient at room temperature.

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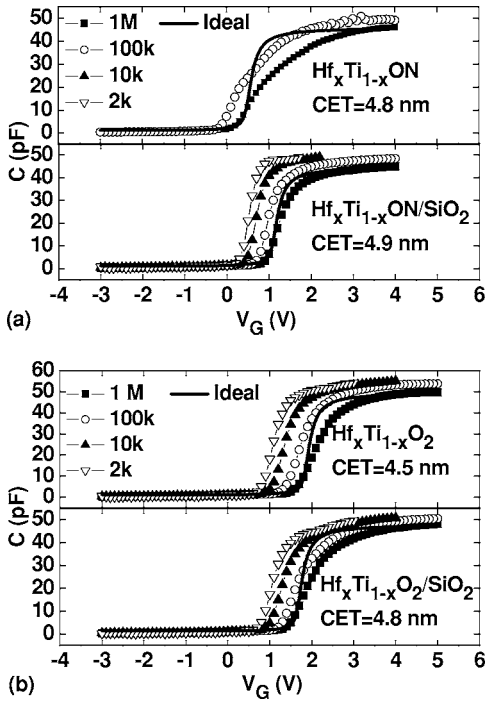

FIG. 1. Capacitance of SiC MOS capacitors vs voltage under different frequencies ranging from 2 kHz to 1 MHz. (a) $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}ON/SiO_2$; (b) $Hf_xTi_{1-x}O_2$ and $Hf_xTi_{1-x}O_2/SiO_2$.

III. RESULTS AND DISCUSSIONS

A. Capacitance-voltage characteristic under different frequencies

Figure 1 shows the capacitance-voltage (C-V) curve measured at different frequencies ranging from 2 kHz to 1 MHz, except that the $Hf_xTi_{1-x}ON$ sample cannot produce the C-V characteristic under 100 kHz due to the poor quality of its gate dielectric. Table I presents the electrical parameters extracted from the C-V curve. As frequency increases, the capacitance in the accumulation region decreases even after series-resistance correction by the two-frequency correction method.[16] Therefore, this C-V dispersion should be due to a large lattice mismatch between SiC and the high-k material which produces interfacial dislocations and generates interface states during the deposition of high-k materials.[17,18] Meanwhile, a parallel shift of the C-V curve along the x axis should also be related to the traps in the oxide bulk or at the interface. The flatband voltage (V_{fb}) difference between 1 MHz and 2 kHz is −0.68 V for the $Hf_xTi_{1-x}ON$ sample, followed by −0.74 V for the $Hf_xTi_{1-x}O_2/SiO_2$ sample and −0.89 V for the $Hf_xTi_{1-x}O_2$ sample. The $Hf_xTi_{1-x}ON$ sample has the largest dispersion of −0.4 V even between 1 MHz and 100 kHz (see Table I). Based on the earlier results, the C-V dispersion can be suppressed due to the reduction of interface traps by adding a thermally grown SiO_2 interlayer. As frequency decreases, the C-V curve shifts to the left, probably due to some deep-level positive oxide charges responding at lower frequency, and this frequency-dependent flatband shift also happened in other MOS devices.[19] Since the flatband voltage minus the work function difference between Al and SiC is positive, the oxide charges should be mainly negative and have two origins: singly and doubly negatively charged interstitial oxygen atoms;[20] broken Hf-O bonds to form negative charges localized at the O atoms.[21] Since the nitrided dielectrics have less oxygen, they have less negative oxide charges. The oxide-charge density Q_{ox} can be determined from the flatband voltage V_{fb},

$$V_{fb} = \phi_{Al,SiC} - \frac{Q_{ox}}{C_{ox}}, \tag{1}$$

$$\phi_{Al,SiC} = \chi + E_g/2 - (kT/q)\ln(N_d/n_i), \tag{2}$$

where $\phi_{Al,SiC}$ is the work function difference between Al and SiC; C_{ox} is the maximum oxide capacitance in the accumulation region; χ is the electron affinity of SiC (4 eV); N_d is the doping concentration of SiC (6.5×10^{15} cm^{-3}) n_i is the

TABLE I. Parameters extracted from capacitance-voltage curve with frequency ranging from 2 kHz to 1 MHz. Area of capacitor is 7×10^{-5} cm^2.

Sample	C_{ox} (pF)	CET (nm)	V_{fb} (V)	ΔV_{fb} [a] (V)	Q_{ox} ($\times10^{12}$ cm^{-2})	k	D_{it} ($\times10^{12}$ cm^{-2} eV^{-1})		f (Hz)
							0.2 eV	1.4 eV	
$Hf_xTi_{1-x}ON$	45.9	5.3	0.49	NA	−1.6	17.0	13.4	1.02	1 M
	50.0	4.8	0.09	−0.4	−0.16	18.5			100 k
$Hf_xTi_{1-x}ON/SiO_2$	45.5	5.3	1.11	NA	−3.88	16.8	3.7	0.35	1 M
	49.5	4.9	0.86	−0.25	−3.22	18.3			100 k
	49.4	4.9	0.60	−0.51	−2.18	18.3			10 k
	51.7	4.7	0.43	−0.68	−1.57	19			2 k
$Hf_xTi_{1-x}O_2$	49.5	4.9	1.88	NA	−7.21	14.2	12.0	2.54	1 M
	53.4	4.5	1.54	−0.34	−6.34	15.3			100 k
	54.6	4.4	1.18	−0.70	−4.93	15.7			10 k
	53.8	4.5	0.99	−0.89	−4.05	15.5			2 k
$Hf_xTi_{1-x}O_2/SiO_2$	47.9	5.0	1.67	NA	−6.18	13.8	10.7	2.0	1 M
	50.4	4.8	1.46	−0.21	−5.65	14.5			100 k
	50.8	4.8	1.16	−0.51	−4.47	14.6			10 k
	49.5	4.9	0.93	−0.74	−3.45	14.2			2 k

[a] $\Delta V_{fb} = V_{fb}$(1 MHz)-V_{fb} (other frequency).

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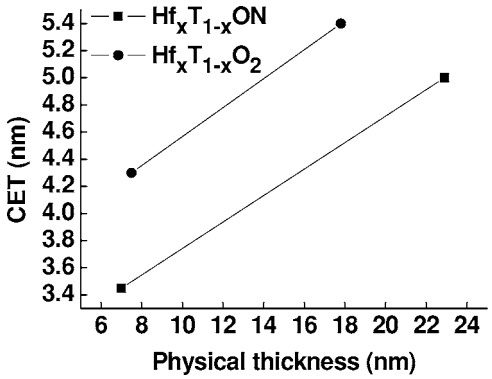

FIG. 2. CET of SiC MOS capacitors as a function of dielectric thickness for $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}O_2$. Physical thickness is measured by spectroscopic ellipsometer.

intrinsic carrier concentration of 6H-SiC at room temperature (3.0×10^{-6} cm^{-3});[18] and E_g is the forbidden bandgap of 6H-SiC (3.0 eV).

The solid lines in Fig. 1 are the ideal *C-V* curves calculated from the data measured at 1 MHz by the following equation:[22]

$$C_{\text{ideal}} = \frac{C_s C_{\text{ox}}}{C_s + C_{\text{ox}}}, \tag{3}$$

where the surface capacitance C_s is

$$C_s = \frac{C_{\text{FBS}}}{\sqrt{2}} \frac{\exp(v_s) - (n_i/N_d)^2 \exp(-v_s) - 1}{[-(v_s+1) + \exp(v_s) + (n_i/N_d)^2 \exp(-v_s)]^{1/2}}, \tag{4}$$

with C_{FBS} as the value of C_s at the flatband and v_s as the surface band-bending potential.

The $Hf_xTi_{1-x}ON/SiO_2$ sample has the smallest deviation from the ideal *C-V* curve, indicating best interface quality. Interface-trap density D_{it} in Table I is calculated by using the Terman's method.[23] The D_{it} close to the conduction band and near the midgap are both effectively suppressed for the $Hf_xTi_{1-x}ON/SiO_2$ sample, resulting in the smallest D_{it} of 3.5×10^{11} cm^{-2} eV^{-1} at 1.4 eV below the conduction band (see Table I). The improvement of interface quality should be due to the following reasons: (1) SiO_2 has better interface quality with SiC than a high-*k* dielectric; (2) $Hf_xTi_{1-x}ON$ has less negative oxide charges than $Hf_xTi_{1-x}O_2$ (see Table I); and (3) nitrogen in $Hf_xTi_{1-x}ON$ can diffuse into SiO_2 to passivate the carbon clusters at the interface.

B. Calculations of dielectric constant and electric field

Capacitance equivalent thickness (CET) is extracted from the high-frequency *C-V* curve at 100 kHz (see Fig. 1). Physical thickness of $Hf_xTi_{1-x}ON$, $Hf_xTi_{1-x}O_2$, and the thermally formed interlayer are measured by SE. The dielectric constants are extracted by using the data of two thicknesses of both $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}O_2$ dielectrics deposited on dummy wafers without the SiO_2 interlayer, but with the same growth conditions as SiC (see Fig. 2). The following equation is used for calculating the dielectric constant of the high-*k* materials (k_{hk}):

$$k_{hk} = k_{lk} \times \left(\frac{T_{\text{phy1}} - T_{\text{phy2}}}{\text{CET1} - \text{CET2}} \right), \tag{5}$$

where k_{lk} is dielectric constant of the low-*k* interlayer and T_{phy} is the physical thickness of the dielectric measured by SE. Assuming the low-*k* interlayer is SiO_2 with a dielectric constant of 3.9, the dielectric constant for $Hf_xTi_{1-x}ON$ is 40 and $Hf_xTi_{1-x}O_2$ is 32. Based on the fact that the ratio of electric fields across the dielectric and SiC is equal to the inverted ratio of their dielectric constants

$$E_{\text{SiC}}/E_{\text{Hf}_x\text{Ti}_{1-x}\text{ON}} = k_{\text{Hf}_x\text{Ti}_{1-x}\text{ON}}/k_{\text{SiC}} = 40/9.6 = 4.2, \tag{6}$$

$$E_{\text{SiC}}/E_{\text{Hf}_x\text{Ti}_{1-x}\text{O}_2} = k_{\text{Hf}_x\text{Ti}_{1-x}\text{O}_2}/\varepsilon_{\text{SiC}} = 32/9.6 = 3.3. \tag{7}$$

If the SiC surface reaches its critical electric field of 3 MV/cm (at which electrons reach their saturation velocity), $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}O_2$ have to endure an electric field of 0.7 and 0.9 MV/cm, respectively, which is lower than the 1.5 MV/cm of HfO_2 for a $HfO_2/SiO_2/SiC$ structure.[8] In this work, $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}O_2$ can stand a high constant-voltage stress at 12.6 and 7.2 V, respectively, for 3000 s without breakdown. Based on the stress voltage *V*, the electric field in the high-*k* dielectric ($E_{\text{high-}k}=V_{\text{high-}k}/T_{\text{high-}k}$) of the stacked samples can be calculated from

$$\frac{k_{\text{SiO}_2}}{k_{\text{high-}k}} = \frac{E_{\text{high-}k}}{E_{\text{SiO}_2}} = \frac{V_{\text{high-}k}/T_{\text{high-}k}}{(V - V_{\text{fb}} - V_{\text{high-}k})/T_{\text{SiO}_2}}, \tag{8}$$

($V_{\text{high-}k}$ is the voltage across the high-*k* dielectric; $T_{\text{high-}k}$ is the physical thickness of the high-*k* dielectric; and T_{SiO_2} is the physical thickness of the SiO_2 interlayer), and is equal to 2.2 and 1.4 MV/cm for $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}O_2$, respectively, both values exceeding the corresponding field in the dielectric when the SiC surface is subjected to its critical field. The advantages of hafnium-titanium oxide and oxynitride over SiO_2 can be summarized as follows: (1) the electric field across the dielectric is much lower and (2) the margin between dielectric breakdown and required electric field is (2.2–0.7)/2.2=68% for $Hf_xTi_{1-x}ON$ and (1.4–0.9)/1.4 =36% for $Hf_xTi_{1-x}O_2$, as compared to (8–7.4)/8=7.5% for thermal SiO_2 (thermal SiO_2 on 6H-SiC has a breakdown field of 8 MV/cm,[24] and has to endure 7.4 MV/cm when SiC reaches its critical field of 3 MV/cm). The leakage current of the capacitors versus electric field is shown in Fig. 3. It can be clearly seen that the oxynitrides have a higher leakage current than the oxides, which is probably due to several reasons: (1) the smaller bandgap of the former (3.6 eV for $Hf_xTi_{1-x}ON$ and 3.9 eV for $Hf_xTi_{1-x}O_2$ measured by SE, as shown in Fig. 4), which may result in smaller conduction bandgap offset; (2) the samples with oxynitrides have less SiO_2 grown at the dielectric/SiC interface during the high-temperature nitrogen annealing due to oxygen blocking by the incorporated nitrogen[25,26] and less oxygen in the oxynitrides; and (3) TiN in the oxynitrides is a good conductor. However, by adding a thermally grown ultrathin SiO_2 interlayer, electrons can be largely blocked from injecting into the high-*k* material and leakage can be significantly suppressed (see Fig. 3).

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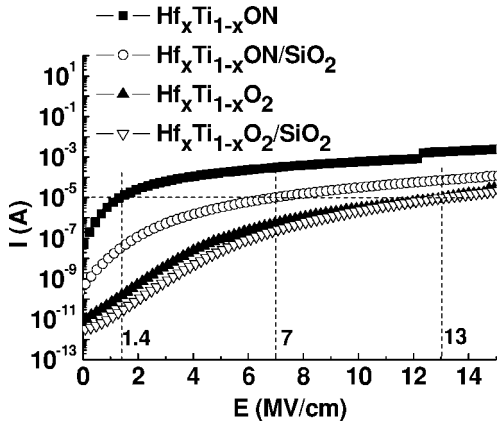

FIG. 3. Leakage current (I) of SiC MOS capacitors vs electric field (E) at room temperature in dark ambient.

C. Electrical stress under a constant field (E=11 MV/cm)

A constant electric field [$E=(V-V_{fb})/\mathrm{CET}=11$ MV/cm] is used to stress the stacked and nonstacked hafnium-titanium oxides and oxynitrides. Figure 5 shows the C-V curves of the samples after different stress times. It can be clearly seen that after stressing, there is negligible distortion of C-V curve for the two oxynitride samples and their flatband shifts are smaller than those of the two oxide samples. Specifically, a significant distortion of C-V curve happens in the oxides after a 10 s stress. After stress, the curve shifts right, indicating increase of negative oxide charges, which may have two sources: (1) electrons injected from the substrate during the stress and (2) the stress can activate the defects (the seed model)[27] or generate defects via breaking bonds by the injected electrons (the percolation model).[27] Since Hf-N bonds (396 eV) are weaker than Hf-O bonds (531 eV)[28] and Ti-N bonds (454 eV) are also weaker than Ti-O (458 eV) bonds,[29] the percolation model cannot explain the results here. Therefore, the seed model should be adopted: the two oxide samples have more oxygen-related defects generated during their fabrication which can be activated during stressing. In Fig. 6, the smaller flatband shift of the oxynitrides versus stress time implies much less oxide defects activated by the stress, thus revealing that the nitride dielectrics have less defects and better stress reliability. Some important parameters after a 3000 s stress are listed in Table II. The Hf$_x$Ti$_{1-x}$ON/SiO$_2$ sample has the smallest capacitance degradation (in the accumulation region) of 1.1%, followed by the Hf$_x$Ti$_{1-x}$O$_2$ (2.9%), Hf$_x$Ti$_{1-x}$O$_2$/SiO$_2$ (3.9%), and Hf$_x$Ti$_{1-x}$ON (9%) samples. Although the Hf$_x$Ti$_{1-x}$ON sample has less defects and oxide charges than the two oxide samples, it has the largest capacitance degradation, possibly due to its poor interface without the SiO$_2$ interlayer and significant electron injection across the low barrier between SiC and the nitride. However, after adding the SiO$_2$ interlayer, the interface quality is greatly improved and leakage is suppressed, together with less defects and charges in the dielectric, resulting in the smallest capacitance degradation for the Hf$_x$Ti$_{1-x}$ON/SiO$_2$ sample. Figure 7 shows the leakage-current degradation caused by the stress,

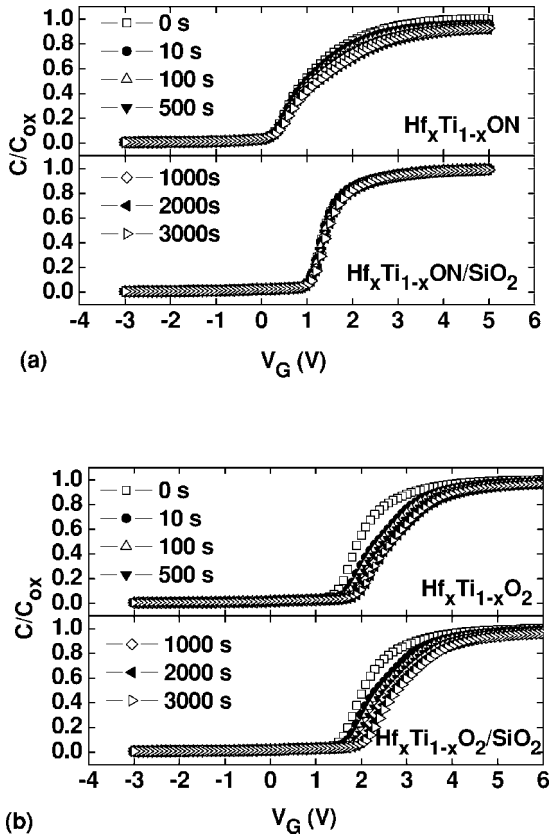

FIG. 5. Capacitance of SiC MOS capacitors vs voltage measured at 1 MHz after different stress times. (a) Hf$_x$Ti$_{1-x}$ON and Hf$_x$Ti$_{1-x}$O$_2$/SiO$_2$; (b) Hf$_x$Ti$_{1-x}$O$_2$ and Hf$_x$Ti$_{1-x}$O$_2$/SiO$_2$.

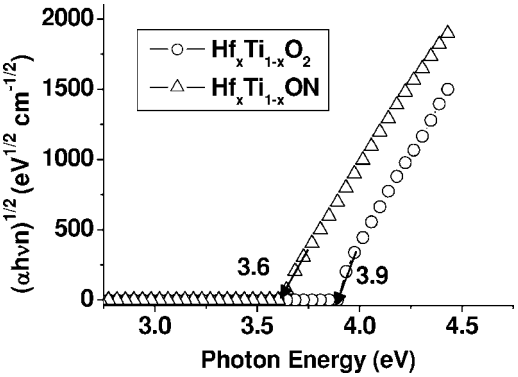

FIG. 4. $(\alpha h\nu n)^{1/2}$ vs photon energy ($h\nu$) for dielectrics. α is absorption coefficient of dielectric and n is its refractive index.

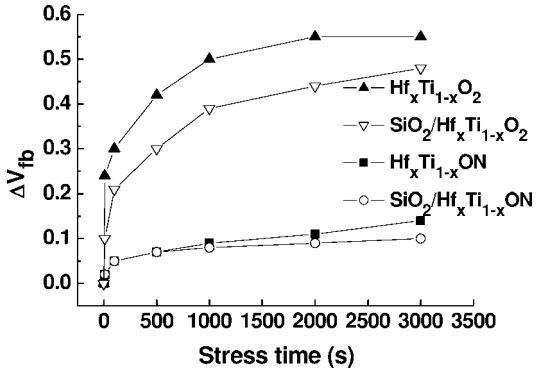

FIG. 6. Flatband shift of SiC MOS capacitors during high-field stressing (E=11 MV/cm) on their gate dielectrics.

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TABLE II. Electrical parameters variation after stressing at a constant electric field [$E=(V-V_{fb})/CET=11$ MV/cm] for 3000 s. CET is capacitance equivalent thickness. Negative sign means the values are smaller than prestressed ones.

Sample	ΔC_{ox} (%)	ΔV_{fb} (V)	ΔQ_{ox} ($\times 10^{11}$ cm^{-2})	ΔI (%) ($E=4$ MV/cm)
$Hf_xTi_{1-x}ON$	−9	0.14	5.1	−20
$Hf_xTi_{1-x}ON/SiO_2$	−1.1	0.1	3.6	−10
$Hf_xTi_{1-x}O_2$	−2.9	0.55	18	188
$Hf_xTi_{1-x}O_2/SiO_2$	−3.9	0.48	14	156

with the stress-induced shift of the flatband voltage included in the calculation of the electric field. The oxynitrides seem to have less leakage after stress, probably due to some error in calculating the flatband voltage, e.g., measured accumulation capacitance not fully saturated. Compared with the oxynitrides, the oxides have larger increase of leakage current (188% for the $Hf_xTi_{1-x}O_2$ sample and 156% for the $Hf_xTi_{1-x}O_2/SiO_2$ sample), again supporting the seed model that stress can activate defects and thus increase the leakage current. Moreover, repeating the measurements after exposure to air for one month shows that the $Hf_xTi_{1-x}O_2$ sample has 16% reduction in accumulation capacitance and the $Hf_xTi_{1-x}O_2/SiO_2$ sample has 12%. However, the oxynitrides have negligible degradation over this time, probably due to the reduction of oxygen-related defects by incorporating nitrogen into the dielectric.

IV. CONCLUSIONS

Titanium is added into hafnium oxide to increase its dielectric constant and to reduce its electric field when used as the gate dielectric of SiC MOS devices. Moreover, nitrogen is incorporated into the hafnium-titanium oxide to further increase its dielectric constant, reduce its negative oxide charges, and improve its reliability during electrical stress. Then, a SiO_2 interlayer is added to suppress the leakage associated with high-k materials; improve the interface quality and reduce the frequency-dependent C-V dispersion. In conclusion, $Hf_xTi_{1-x}ON/SiO_2$ can achieve better interface quality with SiC by passivating carbon clusters with nitrogen, less oxide charges, and better stress reliability compared with $Hf_xTi_{1-x}O_2$ with or without the SiO_2 interlayer, therefore, $Hf_xTi_{1-x}ON/SiO_2$ is a promising high-k dielectric for making high-performance SiC MOS devices.

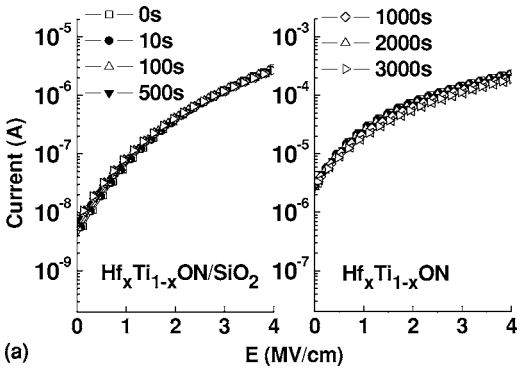

FIG. 7. Leakage current (I) of SiC MOS capacitors vs electric field (E) during high-field stressing ($E=11$ MV/cm) on their gate dielectrics. (a) $Hf_xTi_{1-x}ON$ and $Hf_xTi_{1-x}ON/SiO_2$; (b) $Hf_xTi_{1-x}O_2$ and $Hf_xTi_{1-x}O_2/SiO_2$.

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