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Picosecond All-Optical Logic Gates (XOR, OR, NOT, and AND) in a Fiber Optical Parametric Amplifier

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Abstract: We demonstrate all-optical XOR, OR, NOT, and AND gates in a fiber optical parametric amplifier within the same experimental setup. Error-free operation was achieved for 10Gb/s RZ signals with pulsewidth suitable for 100Gb/s operation.

1. Introduction

All-optical gates of high speed operation of 40Gb/s or beyond have been of rising interest due to the limitations of traditional electrical methods. Generation of logic gates using single or multiple SOA's [1-3] or a single spool of nonlinear fiber [4] has been demonstrated. Here, we use pulses of picosecond full-width at half-maximum (FWHM) pulsewidth as our inputs to an OPA. The OPA uses a single spool of highly-nonlinear dispersion-shifted fiber (HNL-DSF) for multiple logic gates. The bit-rate of the setup was of 10Gb/s, and input pulses of FWHM pulsewidth of 4.6ps. The FWHM pulsewidth was measured to be 5.1ps at the output. This reveals a possibility of operating at 100Gb/s or beyond.

2. Theory of Operation

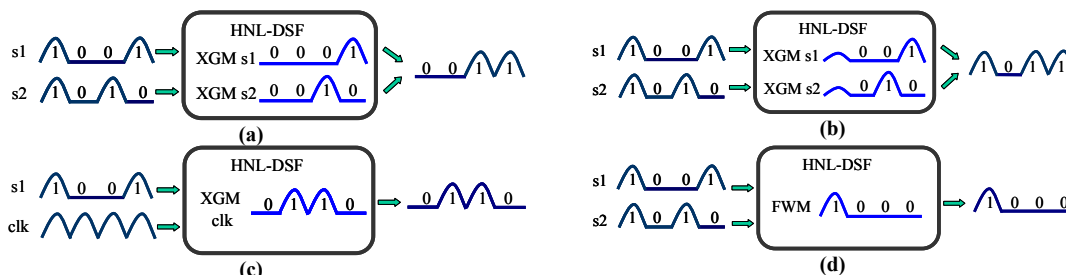We summarize the operating principles of the XOR, OR, NOT, and AND gates in fig. 1(a-d), respectively.

Fig. 1 Operating principle of (a) XOR, (b) OR, (c) NOT, (d) AND gates; FWM: four-wave mixing, XGM: cross-gain modulation

Two synchronized return-to-zero on-off keying (RZ-OOK) 10Gb/s signals of picosecond pulse widths are launched to a HNL-DSF with their wavelengths within the optical parametric amplification (OPA) gain spectrum of each other. Consequently, when both of the data stream co-propagate through the HNL-DSF, they will be depleted by cross-gain modulation (XGM) effects under the OPA effects [5], with the power transferred to the newly generated four-wave mixing (FWM) components [4]. It has been shown that this phenomenon can strongly deplete the input signals, which are the OPA pumps in this case [5]. The amount of depletion can be controlled by adjusting the signal input power and the state of polarization (SOP) between the input signals. When only one of the signals is launched to the HNL-DSF, it emerges at the output with no significant power loss, shown in Fig. 1(a) and (b), when only one of the bits is HIGH. By coupling these two output signals together, we can then achieve an XOR gate or an OR gate depending on the strength of the XGM. An XOR gate is generated by a complete depletion for the input signals as shown in Fig. 1(a), while an OR gate has a ~ 50 % power depletion of an individual signal as in Fig. 1(b). The NOT gate is generated by setting one of the signals as a clock source synchronous to the signal to be inverted. Hence, the XGM on the clock due to the input signal will serve as the inverted signal shown in Fig. 1(c). The AND gate is generated by FWM alone within the HNL-DSF (Fig. 1(d)), with a filter is applied to select one of the FWM components.

3. Experimental Setup

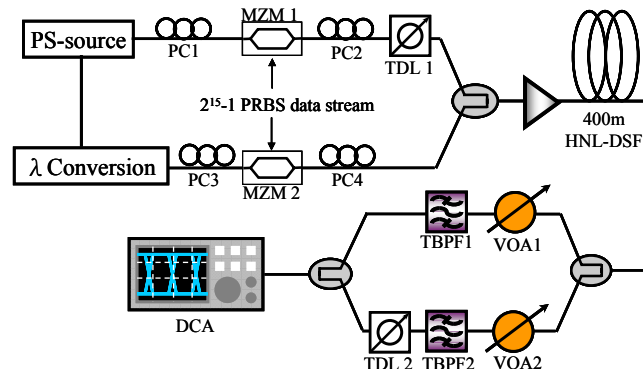The experimental setup is shown in Fig. 2 below.

Fig. 2. Experimental Setup. TDL: Tunable delay line. TBPF: tunable band pass filter. VOA: Variable optical attenuator. MZM: Mach-Zehnder modulator. PC: Polarization controller. PS-source: Picosecond pulse source. DCA: Digital Communications Analyzer. All couplers are 50/50 couplers.

For the XOR, OR, and NOT gates, the ps-source was operated at 1563.9nm. The wavelength conversion was achieved by a Kerr-shutter [6] based scheme to generate a wavelength at 1557.2nm. For the AND gate, the ps-source was operated at 1558.6nm while the converted wavelength was 1550.2nm. The different wavelengths for the AND gate was to avoid the wide continuum generated by OPA effects that will hamper the integrity of the FWM signal. Pulsewidth after the wavelength conversion was 4.6ps. The nonlinear medium was a piece of HNL-DSF of 400m long with a nonlinear coefficient of $11W^{-1}km^{-1}$ and a zero-dispersion wavelength of 1554nm. The signal from the ps-source and the converted signal were both amplitude modulated by 2^{15}-1 pseudo-random bit sequence (PRBS) for the XOR, AND, and OR gates. The converted signal was not modulated in the case of the NOT gate. The signal from the ps-source was delayed using TDL1 to ensure that the two signals were of integer number of bits separated from each other. They were set to have parallel polarization by PC4 and amplified to 62mW for XOR, OR, NOT gates and 42mW for AND gate before entering the HNL-DSF. The higher power for XOR, OR, and NOT gates was required for more significant XGM effects.

For the XOR and OR gates setup, TBPF1 and TBPF2 filtered out each of the input wavelengths since they were composed of both of the input signal wavelengths. TDL2 ensured that both branches were of the same path length. For the AND gate, TBPF1 was set to filter out a FWM component at 1567.0nm. For the NOT gate, TBPF1 was set to filter at 1557.2nm, which was the pump which experienced XGM. The lower branch consisting TBPF2 was switched off by setting VOA2 to a high attenuation for both the NOT and AND gates. The result was then viewed by a DCA with 53GHz electrical bandwidth.

4. Results and Discussion

Clear open eye diagrams are shown in fig. 3(a) and 3(b), proving the operating principle. The non-zero off-state for the XOR and NOT gate was primarily attributed to incomplete depletion of the signals after the OPA process. Since the XOR gate was built from the sum of two different signals, the effect on the eye of incomplete depletion was more severe in the XOR gate than that in the NOT gate.
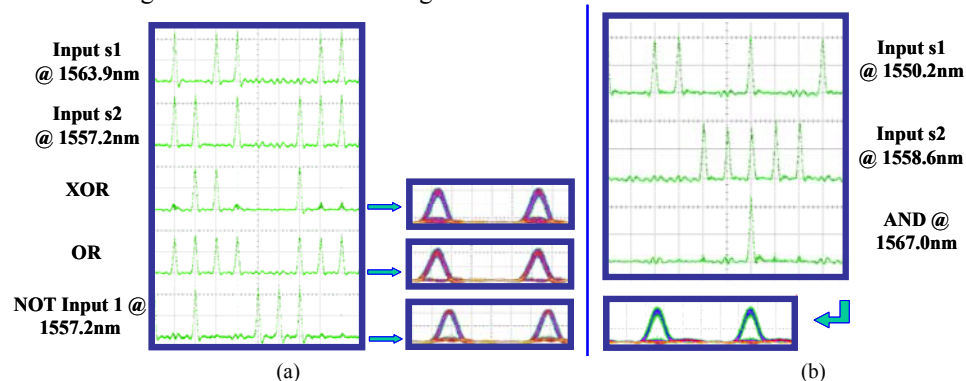

Fig. 3 Bit patterns for the inputs and outputs, and eye patterns of outputs of (a) XOR, OR, and NOT gate outputs and eye diagrams, (b) AND gate

The residue at the off-state in the AND gate was perceived to be inherited from the two MZMs due to finite extinction ratios. FWHM pulsewidths for XOR, OR, AND, and NOT gates were measured by an autocorrelator, and were found to be 5.1ps, 4.9ps, 4.1ps, and 4.8ps, respectively. The decreased pulsewidth for the AND gate output was due to pulse compression in a FWM process [7]. They were comparable to the input pulsewidth of 4.6ps. Narrower output pulsewidths were expected with the use of a wider filter bandwidth in the setup.
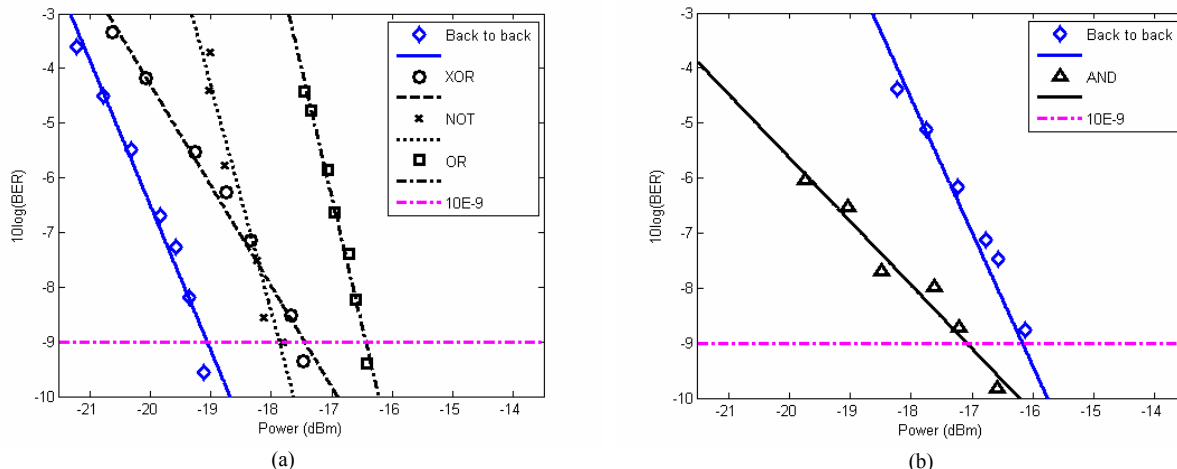

(a)   (b)

Fig. 4 Bit-error rate for each of the input and output signals for the (a) XOR, NOT, OR gates, (b) AND gate

Bit-error rate (BER) curves for the outputs and back-to-back are shown in Fig. 4. Power penalties when BER is at 10^{-9} for OR, XOR, AND, NOT are 2.6dB, 1.6dB, -1.1dB, and 1.2dB, respectively. The back-to-back lines for both diagrams correspond to the BER performance of the converted signal. The slopes were generally more gentle for the AND gate setup than for the other gates. That was due to the choice of wavelengths was not optimum for the Kerr-shutter based wavelength converter, leaving a small CW residue. This small CW residue, together with the ultra-short duty cycle of the pulse, reduced the slope of the BER curves. The negative power penalty at the AND gate was mainly due to a reduced mark ratio and pulse compression due to FWM [7]. The higher power penalty for the OR gate was inherited from an increased mark ratio relative to the back-to-back setup. The gentle slope for the XOR gate was due to the weakened extinction ratio caused by incomplete XGM.

5. Conclusion

We have demonstrated XOR, OR, NOT and AND all-optical logic gates for 10Gb/s RZ signals. It is worth noting that signals with a maximum of 5.1ps are recorded. This indicates a potential possibility for data rate up to 100Gb/s.

Acknowledgment

6. References

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