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AN ECONOMICAL FABRICATION TECHNIQUE FOR SIMOX USING PLASMA IMMERSION ION IMPLANTATION

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ABSTRACT

Buried oxide layers in Si were fabricated using non-mass analyzed plasma immersion ion implantation (PIII). The implantation was carried out by applying a large negative bias to a Si wafer immersed in an oxygen plasma and a dose of $3 \times 10^{17} \text{ cm}^{-2}$ of oxygen was implanted in about three minutes. Cross section transmission electron microscopy (XTEM) and Rutherford backscattering spectrometry (RBS) were used to characterize the wafers. Our results indicate that a continuous buried oxide layer with a single crystal silicon overlayer was synthesized.

INTRODUCTION

The advantages of using devices fabricated on silicon on insulator (SOI) wafers are well documented [1]. The low power requirements and device scaling to sub $0.25 \mu\text{m}$ minimum dimensions required for future integrated circuit devices appear to necessitate the use of SOI wafers in order to attain the required level of performance in speed, device isolation and short channel effects [2].

Separation by implantation of oxygen (SIMOX) is one of the most widely used SOI materials for IC fabrication today. In this process, oxygen is implanted into a silicon wafer to the required depth and the wafer is then annealed at a temperature of 1300°C or higher for about 6 hours. If the oxygen dose is high enough, the nucleated oxide precipitates ripen and form a buried oxide layer of the desired thickness under the Si surface layer with atomically sharp and smooth surfaces [1]. The silicon surface can be prevented from amorphization by holding the wafer temperature above 600°C during implantation. One of the principal reasons for the high cost of the SIMOX wafers is the long time required during the implantation step which limits the throughput.

In this paper, we describe an alternative method for SIMOX fabrication using plasma immersion ion implantation (PIII). In PIII, implantation is performed by immersing the whole wafer in an oxygen plasma while applying a negative bias on the wafer [3] (Figure 1). The applied bias determines the depth to which the oxygen ions are implanted. The inherent advantage of this process is that the rate of implantation is limited only by the heat dissipation capability of the wafer holder and the current limitation of the power supply, but does not depend on the scanning speed, as in a conventional implanter. Therefore, in the PIII process, the implantation time is independent of the wafer area (Figure 2). This is important considering the increasing size of wafers used in the IC industry.

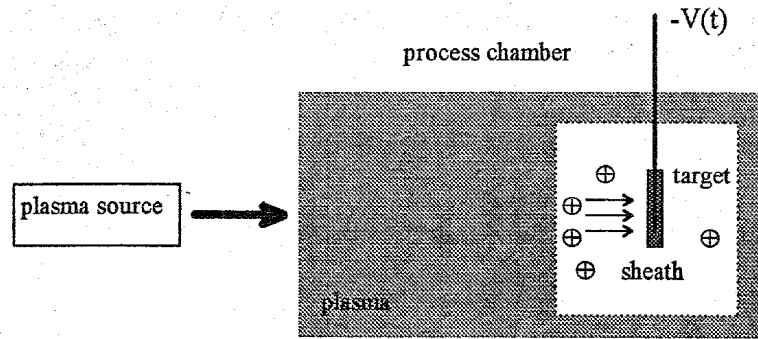


Figure 1: Schematic diagram of plasma immersion ion implantation (PIII)

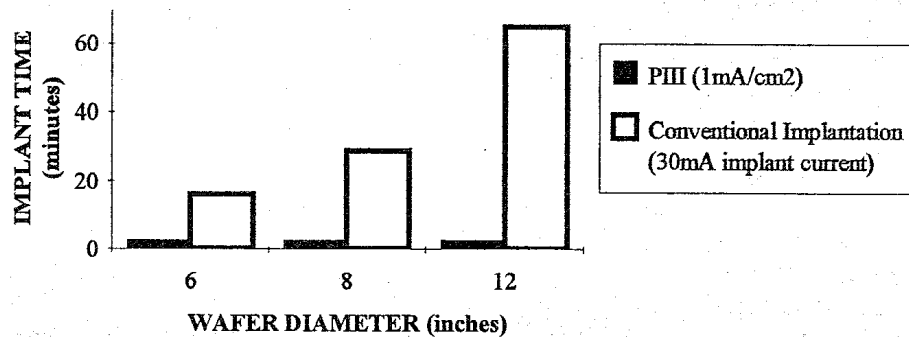


Figure 2: Comparison of the implantation time for a $1 \times 10^{18} \text{ cm}^{-2} \text{ O}^+$ implant by PIII with a current density of 1 mA cm^{-2} with that required by a high-current conventional implant with an ion current of 30 mA.

EXPERIMENTAL

The oxygen implantation was performed using a prototype PIII reactor developed in the Plasma Assisted Materials Processing Laboratory at U.C. Berkeley [3]. The ECR source for the oxygen plasma was excited with 2.45 GHz microwaves with input power of 200-300 W. The implantation was carried out at a substrate bias of -50 kV. The wafer temperature during the implantation was above 600°C as measured with a pyrometer. The nominal implantation time was 3 minutes for an oxygen dose of $3 \times 10^{17} \text{ cm}^{-2}$. The implanted oxygen profile was characterized by RBS.

The implanted wafer was annealed at 1270°C for 2 hours in a nitrogen ambient. Before annealing, the wafer was capped with silicon nitride to prevent surface oxidation during the high temperature step. The annealed sample was analyzed by XTEM to reveal the buried oxide.

RESULTS AND DISCUSSION

The as-implanted oxygen profile was studied by RBS (Figure 3a). Comparing the depth of the oxygen peak with theoretical projected range values calculated by the Monte Carlo simulator TRIM (version 90.05), it is clear that O_2^+ was the dominant species implanted. The peak concentration of oxygen corresponds to an atomic fraction value of 0.67.

Due to the high concentration of oxygen at the peak, oxide nucleation was initiated during the subsequent thermal treatment. By annealing the sample at 1250°C for two hours, the oxide precipitates ripened and formed a continuous buried oxide (Figure 3b). The high resolution XTEM micrograph depicts a single-crystal silicon surface-layer, verifying that holding the wafer temperature above 600°C during implantation was effective in preserving the crystallinity of the top Si layer.

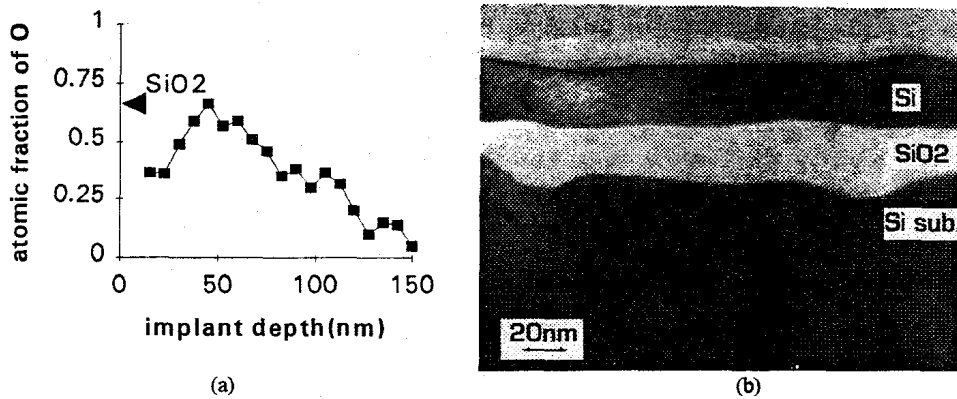


Figure 3: (a) Oxygen depth profile determined by RBS in a silicon wafer implanted with $3 \times 10^{17} \text{ cm}^{-2}$ oxygen at 50kV. (b) XTEM micrograph of the sample after annealing at 1270°C for 2 hours depicting a continuous buried oxide layer.

Our results demonstrate that PIII is potentially a viable technique for the commercial production of thin SIMOX wafers. The implantation time for a 300-mm silicon wafer is less than 3 minutes, as compared to over an hour required by a conventional ion implanter with a current of 30mA. The implantation time could be further reduced by improving the heat sink and temperature control of the wafer and by better controlling the ion species in the plasma to get negligible O^+ ions.

CONCLUSION

PIII is an alternative high-throughput method for making SOI. The implantation time, which is independent of the wafer area, is an order of magnitude lower than that required by conventional beamline ion implantation. Owing to the increased throughput and the lower cost of the implanter, the PIII process is a potential candidate for the economical production of SOI substrates.

ACKNOWLEDGMENT

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REFERENCES

- [1] J.-P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, (Kluwer Academic Publisher, Boston, 1991).
- [2] T. Tsuchiya, T. Ohno and Y. Kado, in Silicon-On-Insulator Technology and Devices, edited by Sorin Cristoloveanu (The Electrochemical Society Inc., Pennington, New Jersey, 1994) pp 401-412.
- [3] N. W. Cheung, Nuclear Instruments and Methods in Physics Research B, **51**, 811 (1991).