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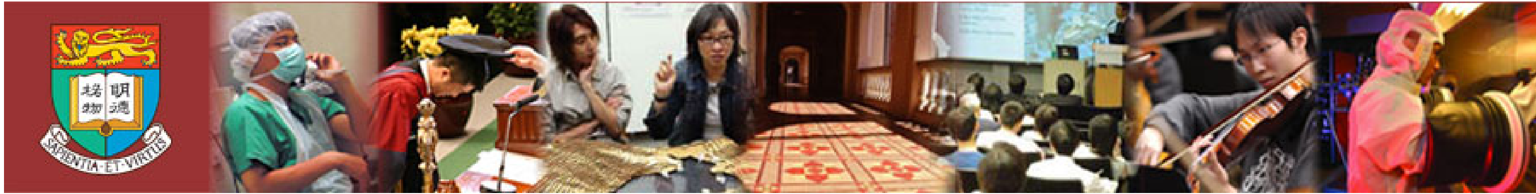

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Planar microwave devices fabricated by ion-implantation patterning of high-temperature superconductors

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We have applied ion-implantation inhibit patterning as a new method of fabricating low-loss microwave transmission lines in high-temperature superconductor thin films. To determine the effectiveness of this technique, we fabricated coplanar waveguide transmission lines in $YBa_2Cu_3O_{7-\delta}$ thin films that had been deposited on $LaAlO_3$ substrates using pulsed laser deposition. Microwave characterizations of these lines are compared to a reference line fabricated with conventional ion milling. At 76 K and 12 GHz, the attenuation constants of the ion-implanted transmission lines are approximated 0.02 dB/mm, and the overall loss response is indistinguishable from that of the ion-milled device. © *1996 American Institute of Physics.* [S0003-6951(96)03840-5]

Over the past few years, there have been several demonstrations of high-temperature superconductor (HTS) microwave circuits.[1] Planar filters, resonators, and delay lines all benefit from the low microwave losses intrinsic to HTS materials. However, device topologies are currently limited to a single layer due to the lack of adequate multilayer processing techniques. Typically, HTS devices are fabricated using conventional patterning methods such as wet-chemical etching or ion-milling.[2,3] These patterning processes remove material in select regions and leave nonplanar surfaces. The resulting topology limits the quality of subsequent HTS layers, since the step edges in the etched film induce grain boundary formation in the overlaying film.

Inhibition patterning using ion-implantation provides a promising alternative patterning technique well suited for multilayer device processing. This method uses Si or B doping to ''poison'' select regions of thin film $YBa_2Cu_3O_{7-\delta}$ (YBCO) without removing material or significantly altering the original crystal structure. The implanted YBCO material is transformed into an insulator for Si doses as low as $1\times10^{21}/cm^3$. Previous reports[4,5] have documented the success of ion implantation in the microlithographic patterning of YBCO for devices such as bolometers[6] and dc superconducting quantum interference devices (SQUIDs).[7] Such multilayer processing techniques are critical in the development of both junction based and planar microwave HTS devices.

While dc resistivities of 10^4 Ω cm have been measured in Si-doped YBCO at 77 K, the microwave losses have not been determined. Without microwave measurements, the applicability of ion-implantation patterning to microwave device fabrication could not have been predicted, particularly since other crystalline perovskite insulators exhibit very large dielectric losses. In this letter, we apply ion-implantation patterning techniques to the fabrication of coplanar waveguide (CPW) microwave transmission lines in thin film $YBa_2Cu_3O_{7-\delta}$. We report on the microwave performance of these devices and compare the results to the performance of YBCO transmission lines fabricated using a conventional ion-milling process.

For this study, three transmission lines of the same design were made: one reference device patterned with conventional ion milling and two test devices patterned with ion implantation of two different Si ion doses. The ion-milled line was made by depositing 350 nm thick YBCO on 0.5 mm thick $LaAlO_3$ (LAO) substrates using pulsed laser deposition. The thin films were patterned using standard photolithography and Ar ion milling. Following an O_2 plasma cleaning, Ti/Au contact metallization was deposited on a photoresist lift-off pattern using electron-beam evaporation. After the liftoff process, the chips were diced for testing.

The ion-implanted CPW lines were fabricated using thinner YBCO films, 100–120 nm thick, on LAO substrates following the procedure described previously.[4,5] The films were patterned by photoresist masking and Si ion implantation. Si ions were implanted into the films at an energy of 80 keV with two different doses: $1\times10^{16}/cm^2$ and $3\times10^{16}/cm^2$. Since Kain and others[8] showed the microwave loss and phase velocity in HTS CPW structures similar to ours to be only weakly dependent on film thickness over the thickness range 100–300 nm, the thinner films (100–120 nm) were used here to reduce the implantation time and potential dam-

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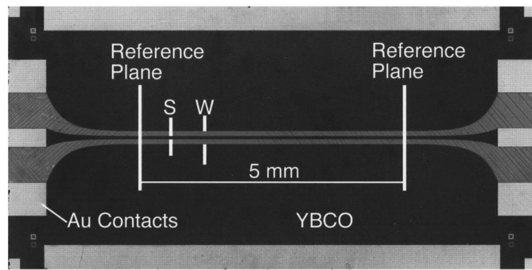

FIG. 1. Labeled photograph of ion-milled reference CPW device. Outer dimensions of the chip are 5 mm×10 mm.

age to the photoresist mask. After implantation, the photoresist was removed by oxygen plasma ashing, followed by Ti/Au metal deposition for the electrical contacts.

A labeled photo of the ion-milled test chip is shown in Fig. 1. The ion-implanted devices look the same as the device in Fig. 1 since the implanted regions are transparent. The CPW line in Fig. 1 was designed for use with a cryogenic test system employed in previous CPW characterizations.[9] The outer dimensions of the chip are 5 mm ×10 mm. Exponential tapers at each end of the chip provide smooth electrical transitions from the launcher contacts to the 5 mm long straight section of CPW. Our test system employs an on-wafer calibration method that places the measurement reference planes on the chip itself, so the electrical parameters of just the 5 mm long straight section are determined. The ratios of the center conductor width (s) to the outer width (w) were calculated to give a characteristic impedance (Z_0) of 50 Ω for infinitesimally thin conductors on a semi-infinite dielectric slab of LAO.[10] A line geometry of $s=53$ μm and $w=253$ μm was chosen for the 5 mm length of straight CPW line, and this s/w ratio was maintained in the exponential tapers at each end of the line.

An automated measurement system consisting of a control computer, a vector network analyzer (VNA), and a custom cryogenic probe was used to characterize the CPW lines at a temperature of 76 K. The device under test was placed in a brass chip carrier and loaded into the test fixture at the end of the cryogenic probe. The carrier supported the chips at the edges along the length, leaving an open rectangular volume 9 mm deep under the bottom surface of the substrate. A Be–Cu spring lifted the carrier, pressing the chip against the center conductor electrodes of the launchers. Two Be–Cu spring contacts provided ground connections at each launcher, and brass retaining clips along the clip edges provided additional low-impedance ground and thermal contacts to the chip.

The fixture stage was cooled by inserting the probe into a liquid nitrogen dewar to a point where the lower portion of the stage was immersed in the liquid, but where the chip was located just above the liquid surface. Enough time was allowed for the chip temperature to come into equilibrium before the measurements.

The particular VNA in our test system required a two-tier calibration. The first tier was a room temperature open-short-load-thru (OSLT) calibration conducted at the end of the cryogenic probe where the test fixture would normally be connected, and the second tier was a multiline thru-reflect-

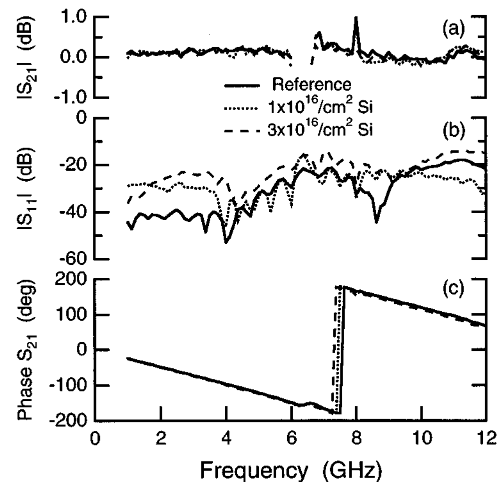

FIG. 2. Calibrated S parameters of ion-implanted CPW transmission lines shown with data from ion-milled reference device: (a) Magnitude of transmission coefficient S_{21}; (b) magnitude of reflection coefficient S_{11}; (c) phase of S_{21}.

line (TRL) calibration[11] performed at 76 K using ion-milled YBCO on LAO calibration standards. The set of TRL standards consisted of a thru connection defined as zero length, two CPW transmission lines of different lengths (1.68 and 5.00 mm), and one chip with short-circuit reflection standards (0 mm offset). The 5.00 mm standard line is the same as the reference device depicted in Fig. 1. The other standards were of the same design, but varied in line length. All were fabricated using the ion-milling procedure described above.

For the second tier calibration, a standard was loaded into the test fixture, cooled to 76 K in liquid nitrogen, and measured. After all the standards were measured in this manner, the calibration software calculated the correction factors from the acquired data and loaded these factors into the network analyzer for the subsequent device measurements. As a result of the multiline TRL procedure, all S parameters are referenced to the characteristic impedance of the standards.

Measurement results for the two ion-implanted CPW test devices are shown in Fig. 2 along with data from the ion-milled reference line. Graphs (a) and (b) show the magnitudes of the transmission (S_{21}) and reflection coefficients (S_{11}) over the frequency range 1–12 GHz, and the lower graph (c) gives the phase of the S_{21} parameters. With the exception of deviations at 6.5 and 8 GHz attributed to limitations in the repeatability of the test fixture with temperature cycling, the S parameters from all three lines agree exceptionally well. The S_{21} data display low-loss and nondispersive behavior over a broad band and the S_{11} data reveal small reflections that increase gradually with frequency. Though not shown here, S_{12} and S_{22} display reciprocal behavior.

To further compare the transmission lines, we calculated the differences in the transmission responses of the ion-implanted test lines and the reference line. The curves in Fig. 3(a) give the difference in the S_{21} magnitudes $|S_{21}|_{\text{implant}} - |S_{21}|_{\text{reference}}$ when the magnitudes are expressed in dB, and Fig. 3(b) shows the corresponding difference in the S_{21} phase responses. Within the scatter of the data, the

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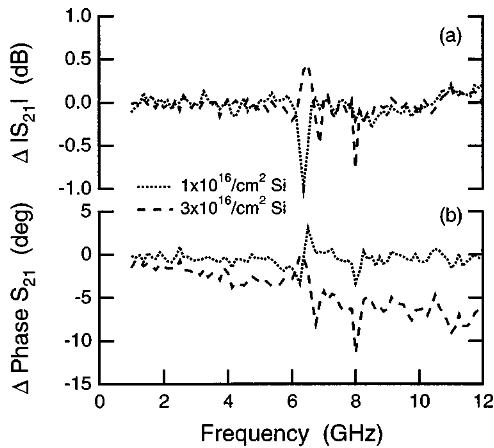

FIG. 3. The difference in S_{21} between ion-implanted test devices and the reference device: (a) difference in the magnitude of S_{21} when both terms are expressed in dB; (b) difference in phase of S_{21}.

losses of the ion-implanted CPW lines are the same as those measured in the ion-milled reference, and there is little difference between the phase response of the low-dose line and that of the reference. The line doped with the higher Si ion dose, $3\times10^{16}/\mathrm{cm}^2$, displays a slightly larger phase constant, possibly indicating that the doping level influences the permittivity of the implanted material.

Before this study we anticipated that the implanted material would significantly influence the microwave response of the CPW lines. In previous studies using the same measurement techniques,[9] we observed increases in both the loss and phase constants when we added thin (150 nm) layers of high-dielectric constant material to ion-milled CPW transmission lines like the reference device used in this work. We have also measured loss factors as large as 1 dB/mm when the material between the center conductor and ground planes was semiconducting. For this work, we estimate a worst case loss factor of 0.02 dB/mm from the minimum in $|S_{21}|$ at 10 GHz (-0.1 dB for a 5 mm line). The fact that the ion-implanted regions did not significantly increase the attenuation constant is remarkable. The observed attenuation factor is significantly less than the 0.1 dB/mm we have obtained at 76 K for gold CPW lines of the same geometry, and demonstrates that insulating Si-doped YBCO can be used in a variety of multilayer transmission line and interconnect applications.

While this study did not reveal significant differences between the ion-implanted lines and the conventional ion-milled lines, the short line length limits the accuracy of this comparison. Based on the method of Holloway and Kuester[12] and the measured surface resistance of the starting material (≈ 1 mΩ at 10 GHz and 76 K), we would expect the loss factor for the ion-milled lines to be 0.002 dB/mm. This suggests that the 0.02 dB/mm estimate is an upper bound on the losses and that improvements can be made in the measurement and/or processing techniques. Additional work is currently under way to make a more complete assessment of the transmission line parameters using a cryogenic probe station and lines and resonators of longer lengths.

To summarize, we have fabricated CPW microwave transmission lines in thin film YBCO using an ion-implantation patterning technique and have measured the microwave response at 76 K using a calibrated cryogenic test system. The patterning technique converts the exposed YBCO areas into low loss, insulating regions through Si doping rather than material removal, and leaves a uniform surface capable of supporting growth of additional crystalline thin films. The creation of insulating regions in the YBCO by this technique does not appear to contribute significantly to the microwave losses in the coplanar waveguide transmission lines. In fact, the line patterned with the lower Si dose did not display any significant deviations from the microwave response of a nearly identical line fabricated with conventional ion milling.

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