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Author(s)	Wang, J; Wong, AKK
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A Study on Theoretical Representation of Intermodulation in CMOS Balanced Mixers

Jun Wang and Alfred K.K. Wong

Department of Electronic and Electrical Engineering
University of Hong Kong, Pokfulam Road, Hong Kong

E-mail: junwang@eee.hku.hk

Abstract—Intermodulation of CMOS balanced mixers is analyzed in this paper with the aim to reduce the effects of intermodulation distortion into a set of simple equations. The analysis consists of a theoretical study and simulation results. Analysis and simulation results reveal that the mechanism of intermodulation in balanced mixer is too complex to be represented by simple equations. Numerical methods must be used to predict the effects of intermodulation in balanced mixer.

I. INTRODUCTION

With the increasing demand for highly integrated transceivers, the bulk off-chip filters used in the conventional double-conversion (heterodyne) receivers have been an obstacle to the increase level of integration. Several transceiver architectures were proposed in the last decade [1–4]. Among them, the Direct Conversion Receiver [1] is promising because the radio-frequency (RF) signals are transfer to baseband directly. In this architecture, the bulk off-chip intermediate-frequency (IF) filters and image rejection filters can be eliminated. However, direct conversion receiver exhibits some disadvantage comparing to conventional heterodyne receivers [1][2]. One critical problem of direct conversion receivers is mismatch-induced second-order intermodulation which decreases the dynamic range of transceivers.

As critical blocks in the front-end of wireless transceivers, mixers are very susceptible to mismatch effects. The double-balanced CMOS mixer [5][6], as shown in Fig. 1, is a commonly used topology in CMOS integrated receivers for frequency translation. Intermodulation distortions of double-balanced CMOS mixers have been analyzed extensively in literature [7–9]. However, these analyses usually concentrate only on the third-order intermodulation. Although the numerical method in [5] can be used to calculate the second-order intermodulation, it does not offer intuition on the effects of mismatch in the performance of mixer. An attempt was made in [10], but the resulting model cannot well-predict the second-order intermodulation in high frequency operation.

This paper performs a theoretical analysis of second-order intermodulation caused by mismatches in CMOS double-balanced mixer. A description of intermodulation in receivers will be presented in Section II. The theoretical analyses of single- and double-balanced mixers are discussed in Section III. Section IV details the simulation results and section V summarizes the work.

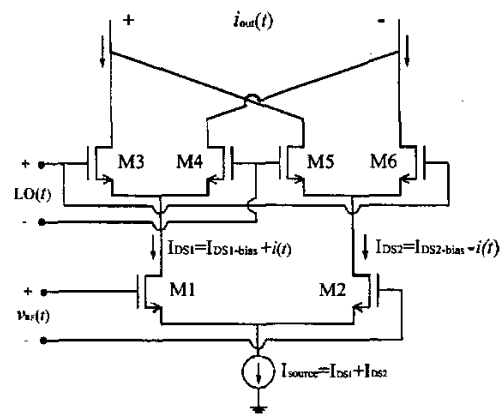


Fig.1 Double-balanced CMOS mixer [10].

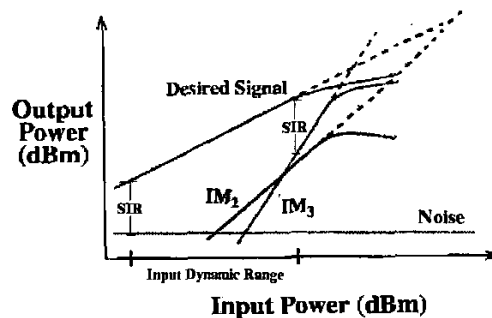


Fig.2 Definition of input dynamic range.

II. EFFECT OF INTERMODULATIONS ON DYNAMIC RANGE

One important characteristics of a receiver is the range of input signals over which the receiver can recognize data correctly (Dynamic Range). This is determined by the signal-to-interference ratio (SIR) required by the back-end of the receiver to reconstruct data from the front-end of receiver output.

Typically, there are two kinds of interference. One is noise. It determines the low-end of the input range because noise is generally low-amplitude and its magnitude does not vary with the amplitude of input signals. When the input signals become large, intermodulation caused by nonlinearity of the circuits becomes

more important and this determines the high-end of the input range, as shown in Fig.2.

Generally, the transfer function of a circuit may be expressed by a Taylor series expansion:

$$Out(t) = a \cdot In(t) + b \cdot [In(t)]^2 + c \cdot [In(t)]^3 + \dots \quad (1)$$

The terms $b \cdot [In(t)]^2$ and $c \cdot [In(t)]^3$ represent the second- and third-order response respectively. They generate undesirable spectral components in the output signals. For a typical Super-heterodyne receiver, only the third-order intermodulation is close to the channel of interest. But both second- and third-order terms interfere with the desired signal in a Direct-conversion receiver because all these signals are located in baseband. So the largest input signal of a Direct-conversion receiver can be calculate by solving this equation:

$$\frac{a \cdot In}{b \cdot In^2 + c \cdot In^3} = SIR. \quad (2)$$

One way to reduce the effect of second-order intermodulation is the use of a differential structure in the circuit, such as the switch pair in balanced mixers. If there is perfect matching between the two switch transistors (e.g., transistors M3 and M4 in Fig.1), parameter b should be zero. In an actual circuit, mismatch between the two switch transistors will destroy the symmetry of the balanced mixer, so b can be reduced but not eliminated. Even so, when mismatch is not very large, $b \cdot [In(t)]^2$ is still much smaller than $c \cdot [In(t)]^3$ near the high-end of the input range, as shown in Fig.2. In this scenario, Equ.2 can be simplified to:

$$\frac{a \cdot In}{c \cdot In^3} = SIR \Rightarrow In_{max} = \sqrt{\frac{a}{c \cdot SIR}}. \quad (3)$$

With the decrease of transistor dimension, mismatch will become more and more severe. When the second-order intermodulation become comparable to the third-order intermodulation near the maximum of the input dynamic range (typically about -10~-20dBm), their effect cannot be ignored anymore. The figures of merit are also specified by IIP2 and IIP3. For example, IIP2 represents the fictitious input amplitude at which the energy of the second-order intermodulation output becomes equal to the desire output.

III. INTERMODULATION ANALYSIS IN BALANCED MIXER

A. Single-balanced mixer.

Typical operating frequency of wireless receivers ranges from several hundred mega Hz to several giga Hz. In such a high frequency, the effects of capacitors inside the mixer must be considered. These capacitors include the gate-source and source-body capacitors of the switch transistors and the drain-body capacitance of the RF input transistor.

Fig.3 is schematic of single-balanced mixer. V_{LO} is the local oscillator signal. I_B is the bias current of RF input transistor. i_s is the small current signal converted from the input RF signal. C_1 and C_2 are the gate-source capacitors of the transistors M1 and M2 respectively. The total capacitance from the common-source node to ground consisting of the source-body capacitance of M1 and M2 and the drain-body capacitance of RF input transistor is represented by C_b .

Denoting the I-V relation of a transistor by $I = f(V)$, the behavior of the switching pair can be described by the following [8]:

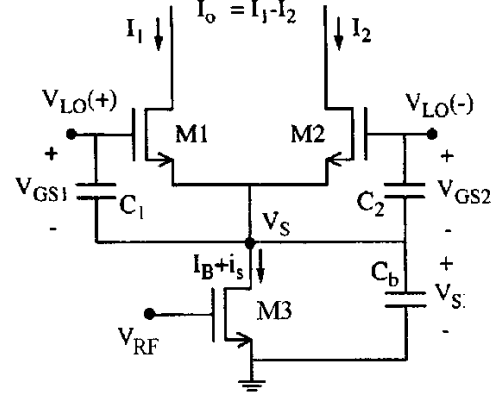


Fig. 3 Schematic of single-balanced mixer [8].

$$I_B + i_s = f_1(V_1) + f_2(V_2) - C_b \frac{d(V_S)}{dt} \dots + C_1 \frac{d(V_{GS1} - V_S)}{dt} + C_2 \frac{d(V_{GS2} - V_S)}{dt} \quad (4)$$

Because $V_{LO} = V_{GS1} - V_{GS2}$, we can re-write Equ.1 as:

$$I_B + i_s = f_1(V_{GS1}) + f_2(V_{GS2}) \dots + \frac{1}{2}(C_1 - C_2) \frac{d(V_{LO})}{dt} - (C_b + C_1 + C_2) \frac{d(V_S)}{dt} \quad (5)$$

Setting $V_{LO} = A_{LO} \cos(\omega_{LO} t)$, $\Delta C = \frac{1}{2}(C_1 - C_2)$ and $C = (C_b + C_1 + C_2)$, Equ.2 can be simplified as:

$$I_B + \underbrace{[i_s + \Delta C \omega_{LO} A_{LO} \sin(2\pi f_{LO} t)]}_{\text{Equivalent small input current signals}} = -C \frac{d(V_S)}{dt} \dots + f_1(V_{GS1}) + f_2(V_{GS2}) \quad (6)$$

Typically $\Delta C \omega_{LO} A_{LO}$ is small compared with the bias current. So it can be treated as a small input signal of the switch pair with the same frequency of LO.

From Equ.6, it can be concluded that the LO signal will leak into the input of the switch pair due to capacitor mismatch of the two switch transistors. The leakage becomes more severe with increase of the frequency or the amplitude of LO.

Using the result in [8], the output current of the switch pair can be represented using the time-varying Volterra series [11-13], such that:

$$I_{out} = f_1(V_{GS1}) - f_2(V_{GS2}) = I_{out-DC} + i_{out}(t) = P_0(t) \cdot I_B + P_1(t, f_a) \circ i + P_2(t, f_a, f_b) \circ i^2 \dots + P_3(t, f_a, f_b, f_c) \circ i^3 + \dots \quad (7)$$

where I_B and i are the bias and small signal input current of the switch pair respectively, and $P_i, i=1,2,3,\dots$ are the Volterra series coefficients. They can be calculated by the numerical method described in [8]. If there is a perfect match between the two transistors in the switch pair, all the even-order Fourier coefficients of P_i will be zero. In an actual circuit, they are always nonzero due to mismatch.

Because the RF input transistor M3 in Fig.3 is a time-invariant nonlinear circuit, it can be represented using the

traditional Tyler-series. Assume $v_{rf} = r_{rf} \cos(\omega_{rf}t)$ is the input RF small signal, the input current of the switch pair can be written as:

$$\begin{aligned} I_{input} &= I_B + i_{RF} + i_{LO_leakage} \\ &= I_B + a \cdot v_{rf} + b \cdot v_{rf}^2 + c \cdot v_{rf}^3 \dots \\ &\quad + \Delta C A_{LO} \omega_{LO} \sin(\omega_{LO}t) \end{aligned} \quad (8)$$

Substituting Equ.7 into Equ.8, using $p_{i,j}$ as the j-th order Fourier coefficient of P_i and a , b and c are first-, second- and third-order transfer characteristics of RF input transistor, and through some mathematical manipulation and simplification, we obtain equations for the first 4 orders of the output current as below:

- 0-order output (DC-feedthrough):

$$I_{out-DC} = p_{0,0} \cdot I_B + p_{1,1} \cdot \frac{\Delta C A_{LO} \omega_{LO}}{2}, \quad (9)$$

- 1st-order output (Desired):

$$i_{desire} \approx (p_{1,1} \cdot a) \cdot r_{rf}, \quad (10)$$

- 2nd-order output (IM2):

$$i_{IM2} = \left(p_{2,0} \cdot a^2 + p_{3,1} \cdot \frac{\Delta C A_{LO} \omega_{LO}}{2} \cdot a^2 + p_{0,0} \cdot \frac{b}{2} \right) \cdot r_{rf}^2, \quad (11)$$

- 3rd-order output (IM3):

$$i_{IM3} = \left(p_{3,1} \cdot a^3 + p_{1,1} \cdot \frac{3}{4} c \right) \cdot r_{rf}^3. \quad (12)$$

From Equ.9 and Equ.11, it can be found that the DC-feedthrough and IM2 will increase with increasing frequency, while the desired output signal is virtually unchanged with frequency. That means the DC-feedthrough and the IP2 will decrease with increasing frequency.

B. Doubled-balanced mixer.

After obtaining the equations for the output of single-balanced mixers, it is not difficult to get the equations for double-balanced mixers from the result of single-balanced mixer by inputting two single-balanced mixers with RF signal in opposite phase and subtracting one output from the other:

- 0-order output (DC-feedthrough):

$$I_{out-DC} = \Delta p_{0,0} \cdot I_B + p_{1,1} \cdot \frac{\Delta \Delta C A_{LO} \omega_{LO}}{2}, \quad (13)$$

- 1st-order output (Desired):

$$i_{desire} \approx (p_{1,1} \cdot a) \cdot r_{rf}, \quad (14)$$

- 2nd-order output (IM2) :

$$i_{IM2} = \left(\Delta p_{2,0} \cdot a^2 + p_{3,1} \cdot \frac{\Delta \Delta C A_{LO} \omega_{LO}}{2} \cdot a^2 + \Delta p_{0,0} \cdot \frac{b}{2} \right) \cdot \frac{r_{rf}^2}{4}, \quad (15)$$

- 3rd-order output (IM3):

$$i_{IM3} = \left(p_{3,1} \cdot a^3 + p_{1,1} \cdot \frac{3}{4} c \right) \cdot \frac{r_{rf}^3}{4}. \quad (16)$$

One assumption is used in the course to get these equations. That is: when j is an even, no matter $p_{i,j}$ or $\Delta p_{i,j}$, ΔC or $\Delta \Delta C$, they are all random numbers with mean of zero and small variances comparing with a or b .

Two conclusions can be reached from Equ.13 to Equ.16 for the double-balanced mixer. First, only the mismatch in the switch pair is important for the output DC-feedthrough and IIP2, the mismatch in the input RF converter almost has no any effects for DC-feedthrough and IIP2. The second, the variances of $\Delta p_{i,j}$

and $\Delta \Delta C$ are $\sqrt{2}$ times of those of $p_{i,j}$ and ΔC respectively. The DC-feedthrough of double-balanced mixer will increase 3 dBm compare with that of single-balanced mixer while IIP2 will also increase 9 dBm statistically.

IV. SIMULATION RESULTS

Because the value of parameters $p_{i,j}$ only can be calculated by numerical methods [8], it is still impossible to use theoretical equations to predict intermodulation of mixer accurately. Instead, we can obtain some qualitative results with the simplification methods found in [10] and [14]. To test the accuracy of the simplified theoretical method, simulations are performed in Matlab and Cadence SpectreRF to calculate the IIP2 of a double-balanced mixer with different transistor width in the input V-I converter and switch pair, as shown in Fig.4 and Fig.5 separately. Amplitude of LO and bias common mode input voltage are the X-axis and Y-axis respectively. The ratio of transistor width $\frac{W_{switch}}{W_{CM-input}}$ is $\frac{300\mu m}{300\mu m}$. The model in Section III is simplified by the methods in [10] and [14] so that it can be represented by a set of equations and calculated in Matlab. Fig.4 is the result of Matlab.

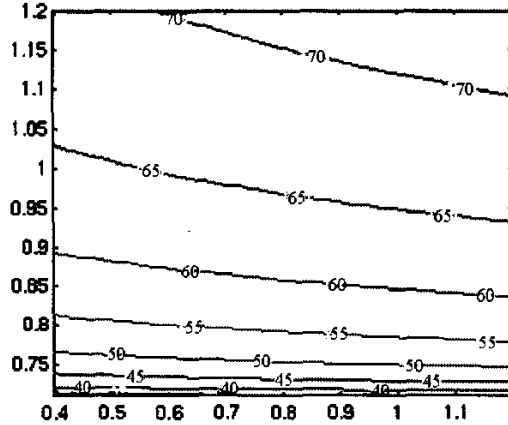


Fig.4 Calculation results of IIP2 using Matlab.

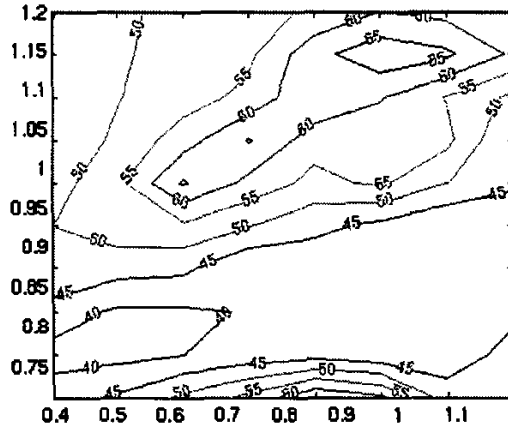


Fig.5 Simulation results of IIP2 using Cadence SpectreRF.

IIP2 increases with the increasing of the common mode RF input voltage *OR* the amplitude of LO. Figures 5 are the simulation results of SpectreRF. Different from the results of Matlab, in this figure IIP2 increases when the common mode RF input voltage *AND* the amplitude of LO increase. Apparently, theoretical equations are too simplistic to predict IIP2 correctly.

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V. CONCLUSIONS

A study of theoretical representation of intermodulation of CMOS balanced mixer has been performed. Time- variance and nonlinearity characteristics of switch pair in balanced mixer make it too complex to be described by simply equations. Although qualitative results can be obtained by the described theoretical method, accurate quantification of intermodulation can only be predicted by numerical methods.

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