The HKU Scholars Hub The University of Hong Kong 香港大學學術庫



Title	Electrical performance and reliability of n-MOSFETs with gate dielectrics fabricated by different techniques	
Author(s)	Xu, Z; Lai, PT; Ng, WT	
Citation	The 1994 IEEE Hong Kong Electron Devices Meeting, The Hong Kong University of Science and Technology, Hong Kong, 18 July 1994. In Conference Proceedings, 1994, p. 18-21	
Issued Date	1994	
URL	http://hdl.handle.net/10722/46216	
Rights	Creative Commons: Attribution 3.0 Hong Kong License	

Electrical Performance and Reliability of n-MOSFET's with Gate Dielectrics Fabricated by Different Techniques

Zeng Xu, P. T. Lai, and W. T. Ng

Dept. of Electrical and Electronic Engineering, The University of HongKong.

I. INTRODUCTION

There have been extensive studies on fabricating high-quality and reliable thin gate dielectrics for MOS applications in VLSI technology. Nitrogen incorporation into the gate oxide is one of the promising methods to achieve excellent immunity to hot-carrier degradation, and effective diffusion barrier against dopants. Many techniques have been proposed [1-4], and among these, reoxidized NH₃-nitrided SiO₂ and N₂O-based dielectrics have received most attention. Compared with NH₃based processes, the N₂O-based processes have an important advantage in addition to the process simplicity, i.e., the absence of any hydrogen-related species during processing, which are believed to be the cause of an increase in electron traps in the gate oxide [5]. In this paper, electrical characteristics and reliability of n-MOSFETs under DC/AC stress are investigated and results are compared among the devices with gate dielectrics fabricated by different techniques.

II. EXPERIMENTAL

n-MOSFET's were fabicated on p-type (100)-oriented silicon wafers (8~10 Ω -cm) by a conventional polysilicon self-aligned MOS process. Four kinds of gate dielectrics were prepared as shown in Table 1. All gate oxides were finally annealed in N₂ at 950°C for 25 min. Oxide thickness was measured by CV technique, the value is 94Å for N₂O-grown oxide, and 99Å for other gate oxides. No passivation film was used. Devices with 1µm/60µm effective channel length/width were used in this work.

Table 1. Preparation sequences of gate oxide employed in this study

sample	oxidation	nitridation	reoxidation
OX	O ₂ , 850°C, 35min	*	
NO	O ₂ , 850°C, 35min	NH3, 950°C, 35min	
RONO	0 ₂ , 850°C, 35min	NH3, 950°C, 35min	O ₂ , 950°C, 15min
N2OG	N ₂ O, 950°C, 30min		

III. RESULTS AND DISCUSSION

Drain current and transconductance versus gate drive measured in linear and saturation regions (Vd=50mV and 3.5V) are shown in Fig.1 and Fig.2 respectively. Devices with control (OX) and N₂O-grown (N2OG) gate oxides exhibit better subthreshold slopes (~ 125 mV/decade for N₂O-grown oxide and ~150 mV/decade for control gate oxide) than the NO device (~250 mV/decade), as can be seen from Fig.1(a). This agrees well with the interface state density values obtained from MOS capacitors using CV techniques. (~1.5×10¹⁰ cm⁻²•eV⁻¹ for OX and N₂O-grown oxides and ~3×10¹¹ cm⁻²•eV⁻¹ for NO oxide). Fig.1(b) shows that the Gm of the device with N₂O-grown gate oxide is improved in both the low and high Vg regions comparing to the control (OX) device. This result is different from that in the device with NH₃-nitrided (NO) gate oxide [1], [6], where Gm is improved only in the high Vg region but degraded in the low Vg region, also shown in Fig.1(b). The degradation of G_m in NO device in the low Vg region was attributed to Coulombic

0-7803-2086-7/94/\$4.00@1994 IEEE.

scattering due to nitridation-induced fixed-charge, interface state charge, and/or near-interface electron trapping [7]. The near-interface bulk electron traps can capture electrons tunneled from the channel regions, and thus reduce the density of channel mobile charge. In addition, those trapped electrons serve as additional Coulombic scattering centers, thus the electron mobility is reduced. One possible reason for Gm improvement in the low Vg region for N2OG device is due to the improved charge trapping property demonstrated by small gate voltage shift during constant current stress [8]. This is also verified by the better stability of N2OG device under channel hotelectron injection as presented in Fig.4. Another possible reason is the effect of residual mechanical stress [1]. N₂O-based oxide is supposed to have less compressive stress due to the compensating tensile stress effect through nitrogen incorporation at the interface. Fig.2(a) and (b) illustrate the improved current drivability (ld) and transconductance (Gm) in the saturation region (Vd=3.5V) for n-MOSFET with N2O-grown gate oxide, as compared to the control and NO devices. Similar results were reported in [9] for n-MOSFET with N2O-nitrided gate oxide. It is worth noting that Gm starts to degrade beyond Vg-V_t ~ 3V for the N2OG device. This may result from $\mu_{n,eff}$ degradation at higher vertical field [10]. In Fig.3, better characteristics of N2OG device than OX device were confirmed, especially under high Vg. Even under low Vg, the drivability is comparable to that of the pure gate oxide sample. This is different from the RONO device, which exhibits lower current drivability under low gate drive voltage [11].

Presented in Fig.4 is the stress-time dependence of V_t and G_m instability induced by channel hot-carrier stress (CHCS). The stress condition was chosen to result in channel hot-electron injection into the gate oxide (Vg=Vd=7V). V_t shift is much smaller for the RONO and N2OG devices than the control device, implying electron trapping is significantly suppressed by the nitridation steps. The n-MOSFET with N₂O-grown gate oxide shows the least ΔG_m , indicating improved interface hardness against CHCS. The improved interface hardness and suppressed electron trapping are believed to be due to interfacial strain relaxation as well as substitution of Si-O bonds with stronger Si-N bonds through the formation of oxynitride (SiO_xN_y) [12], and the elimination of H-related species during the N₂O nitridation process.

Fig.5 depicts V_t shifts for OX, RONO and N₂OG gate oxide devices subjected to AC stress and then DC stress continuously. As can be seen clearly that N₂O device has very stable V_t under the whole combined AC/DC stress, while OX device has a slight V_t increase (~37mV) in the AC stress session, but a very large increase in V_t (~410mV) in the subsequent DC stress, which results from channel hot electron injection. It should be noted that the V_t shift here during DC stress session is even larger than that shown in Fig.4(a) (~210mV) for fresh OX device, although lower stress voltage ($Vg=V_d=5V$) was employed, suggesting large amount of electron traps was created during the AC stress in the pure thermal gate oxide. On the other hand, the same AC stress did not generate any significant amount of electron traps in the RONO and N₂O-grown gate oxide, indicating device reliability with nitrided gate oxides is also enhanced under dynamic stress. Again, N₂O-grown oxide behaves even better than reoxidized NH₃-nitrided oxide.

IV. CONCLUSION

 N_2O nitridation is a more promising technique to incorporate nitrogen into gate oxide than NH₃ nitridation both from the view of electrical performance and stability under CHCS and dynamic stress.

REFERENCES

[1] H. S. Momose, T. Morimoto, K. Yamabe, and H. Iwai, "Relationship between mobility and residual-mechanical-stress as measured by Raman spectroscopy for nitrided-oxide-gate MOSFETs," in IEDM Tech. Dig., 1990, p65.

[2] P. J. Wright, A. Kermani, and K. C. Saraswat, "Nitridation and post-nitridation anneals of SiO₂ for ultrathin dielectrics," IEEE Trans. Electron Device, vol.37, p.1836, 1990.

[3] T. Ito, T, Nakamura, and H. Ishikawa, "Advantages of thermal nitride and nitroxide gate films in VLSI process," IEEE Trans. Electron Device, vol.29, p.498, 1982.

[3] Z. H. Liu, P. T. Lai, and Y. C. Cheng, "Characterization of charge trapping and high-field endurance for 15-nm thermally nitrided oxides," IEEE Trans. Electron Device, vol.38, p.344, 1991.

[4] H. Hwang, W. Ting, D. L. Kwong, and J. Lee, "Electrical and reliability characteristics of ultrathin oxynitride gate dielectric prepared by rapid thermal processing in N_2O ," in IEDM Tech. Dig., 1990, p.421.

[5] T. Hori, etc., "Demands for submicron MOSFET's and nitrided oxide gate-dielectrics," Extended Abstracts of the 21th conference on Solid State Devices and Materials, pp.197-200, 1989.

[6] T. Hori, "Deep-submicron nitrided-oxide CMOS technology for 3.3-V operation," in IEDM Tech. Dig., 1990, p.837.

[7] M. A. Schmidt, etc., "Inversion layer mobility of MOSFET's with nitrided oxide gate dielectrics," IEEE Trans. Electron Device, vol.35, p.1627, 1988.

[8] Z. H. Liu, H. J. Wann, P. K. Ko, C. Hu, and Y. C. Cheng, "Improvement of charge trapping characteristics of N₂O-annealed and reoxidized N₂O-annealed thin oxides," IEEE Electron Device Lett., vol.13, p.519, 1992.

[9] J. Ahn, W. Ting, and D. L. Kwong, "Furnace nitridation of thermal SiO₂ in pure N₂O ambient for ULSI applications," IEEE Electron Device Lett., vol.13, p.117, 1992.

[10] C. G. Sodini, P. K. Ko, and J. L. Moll, "The effect of high fields on MOS devices and circuit performance," IEEE Trans. Electron Device, vol.31, p.1386, 1984.

[11] H. S. Momose, etc., "Very lightly nitrided oxide gate MOSFET's for deep-sub-micron CMOS devices," in IEDM Tech. Dig., 1991, p.359.

[12] M. M. Moslehi, K. C. Saraswat, and S. C. Shatas, "Rapid thermal nitridation of SiO₂ for nitroxide thin dielectrics," Appl. Phys. Lett., vol.47, p.1113, 1985.



Fig.1. (a) Id and (b) Gm measured at linear region (Vd=50mV) as a function of gate drive for n-MOSFET's (Leff/Weff= $1.0/60 \mu m$) with control(OX), NH₃-nitrided (NO), and N₂O-grown (N2OG) thermal gate oxides.



Fig.2. (a) Id and (b) Gm measured at saturation region (Vd=3.5V) for n-MOSFETs with control (OX), NH3-nitrided (NO), and N2O-grown (N2OG) thermal oxides.



Fig.3. Id - Vd characteristics. Dot lines for N2OG device, and solid lines for control (OX) device.



Fig.5. V_t shifts versus stress time during AC stress and subsequent DC stress for OX, RONO, and N2OG devices. For AC stress, Vd = 5V and Vg was pulsed between Vgl =0V and Vgh = 5V at a frequency of 100kHz with 50% duty cycle squarewave. For DC stress, Vg=Vd=5V



Fig.4. Stress-time dependence of (a) V_1 shift and (b) G_m degradation under channel hot electron stress (Vg=Vd=7V) for n-MOSFETs (Leff/Weff=1/60 μ m) with control (OX), reoxidized NH₃-nitrided (RONO), and N₂O-grown (N2OG) thermal oxides.