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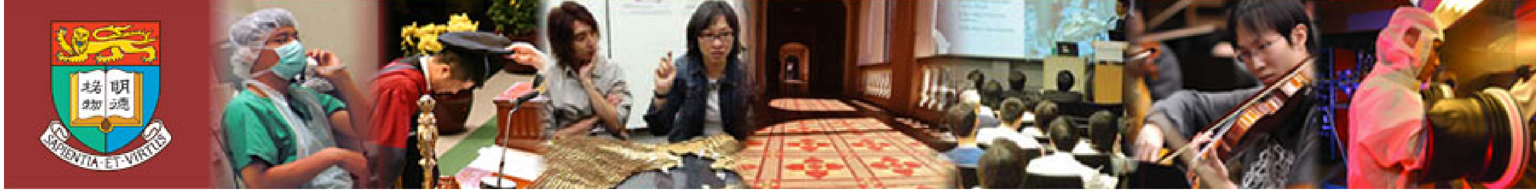

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A Self-aligned Structure AlGaAs/GaAs HBT's Using Silicon Nitride Sidewall Technique

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Suggested area: Compound Semiconductor Devices and Technology

Abstract---A self-aligned fabrication process for AlGaAs/GaAs heterojunction bipolar transistors (HBT's) is presented. The advantage of this process is that self-aligned structure and device passivation can be realized simultaneously using silicon nitride sidewall technique. The silicon nitride sidewall functions both as an isolation layer to prevent shorting between the base metal and the emitter mesa and as an etching mask to prevent AlGaAs passivation layer to be removed. A current gain cutoff frequency f_T of 30GHz and a maximum oscillation frequency f_{max} of 50 GHz have been obtained from the device with 3μm×15μm emitter size.

1. Introduction

AlGaAs/GaAs heterojunction bipolar transistors(HBT's) are very attractive devices for high-speed digital circuit and microwave power applications. This is because AlGaAs/GaAs HBT's possess many inherent advantages, such as very short transit time[1], high current handling capacity[2], large transconductance exponentially dependent on Vbe[3], clean pinch off in the off cycle[3], and controllable breakdown voltage with collector epitaxial design[4]. Using these advantages, excellent RF performance have been demonstrated [5-6]. In order to reach high speed and excellent microwave performance, many self-aligned schemes have been presented to reduce base resistance and parasitic capacitance, as well as intrinsic transit time. However, the device passivation is also a very important issue related to the device reliability. In this paper, a self-aligned fabrication process for AlGaAs/GaAs HBT's is presented. The advantage of this process is that self-aligned structure and device passivation can be realized simultaneously using silicon nitride sidewall technique. A current gain cutoff frequency f_T of 30GHz and a maximum oscillation frequency f_{max} of more than 50 GHz have been achieved from the device with 3μm×15μm emitter size.

2. Device Fabrication

The epitaxial device structure was grown on 3-inch-diameter semi-insulating GaAs substrates using MOCVD technique. The material structure is shown in Table. 1.

Table 1

The HBT epitaxial layer structure

Layer	x	Doping (/cm^3)	Thickness (A)
n+ -$In_xGa_{1-x}As$	0.15	1×10^{19}	200
n^+-GaAs		5×10^{18}	800
n^--$Al_xGa_{1-x}As$	0.3-0	5×10^{17}	300
n^--$Al_xGa_{1-x}As$	0.3	5×10^{17}	1200
n^--$Al_xGa_{1-x}As$	0-0.3	5×10^{17}	300
p^+-GaAs		4×10^{19}	1000
n^--GaAs		5×10^{16}	5000
n^+-GaAs		4.5×10^{18}	6000
S. I. Substrate			

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The emitter -base graded junction was adopted. The thickness and doping level of the heavily C-doped base were 100nm and $4x10^{19}cm^{-3}$, respectively. The collector was designed to give the base-collector breakdown voltage higher than 17V without increasing collector transit time too much.

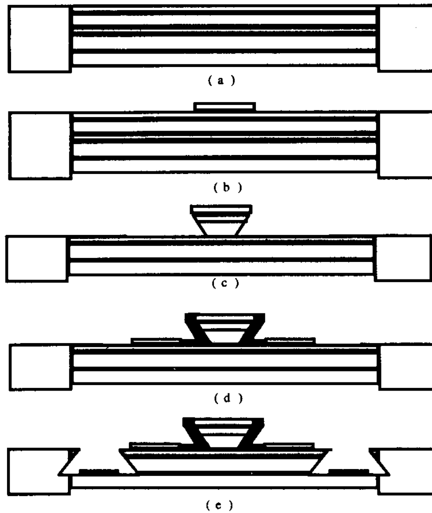

Fig. 1 The process sequence for self-aligned HBT (a) proton implantation (b) emitter contact formation (c) etch down to base and form nitride sidewall (d) base contacts formation (e) etch subcollector and form collector contacts

The process sequence is shown in Fig. 1. Device fabrication begins with a proton implantation to isolate the active device region defined by the isolation mask. The masking material for implantation consists of 1150 Å of silicon nitride deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) plus 6μm of photoresist AZ 4620. The proton implantation is done with a dose of $2\times10^{15}/cm^2$ at 200KeV, followed by a dose of $1\times10^{15}/cm^2$ at 120KeV and $1\times10^{15}/cm^2$ at 30KeV, respectively. The substrates are misaligned during implantation to avoid channeling.

After implantation, the masking materials of photoresist and silicon nitride are removed by acetone and buffered HF acid. An Au/Ge/Ni/Au metal layer is then evaporated and selectively lifted off using the emitter mask. The metal emitter contacts are subsequently used as a natural mask to wet-etch the regions other than the emitter mesas down to approximately 500Å above the p^+ base layer. The etching process includes an initial etch of 3:1:50 H_3PO_4:H_2O_2:H_2O solution to remove the top InGaAs cap layer, followed by a 10:4:500 NH4OH: H_2O_2:H_2O solution to etch down to approximately 500 Å above the p^+ base layer. After this etching step, around 500 Å AlGaAs emitter layer is exposed to air. This layer is, to a first approximation, fully depleted due to the combination of surface Fermi level pinning on the top and being the more lightly doped layer in the base-emitter junction below. After that, a layer of silicon nitride is then deposited by PECVD. The nitride is then etched by RIE, leaving only sidewall silicon nitride covering the sides of the emitter mesas and external base surface under the emitter metal. Next, 10:4:500 NH4OH: H_2O_2:H_2O solution is used again to etch down to the base. Because the AlGaAs surface under emitter metal is covered by silicon nitride, this etching step does not remove the depleted AlGaAs layer under emitter metal. The base contact region is subsequently defined and a base contact metal of Ti/Pt/Au is e-beam evaporated and lifted off. The base is self-aligned to the emitter, and the nitride sidewall functions both as an isolation layer to prevent shorting between the base metal and the emitter mesa and as a etching mask to prevent AlGaAs passivation layer to be removed. In this way, we both realize the self-aligned structure HBT's and complete the device passivation

simultaneously. The device active region is then defined with base island mask. The area outside this masked region is etched down well into the subcollector layer. The collector is then defined and contact metal of Au/Ge/Ni/Au is used. The contact is alloyed at 410C for 10s. Finally, interconnect metal Ti/Au is applied to contact the different electrodes. The SEM photograph of the final device fabricated is shown in Fig. 2.

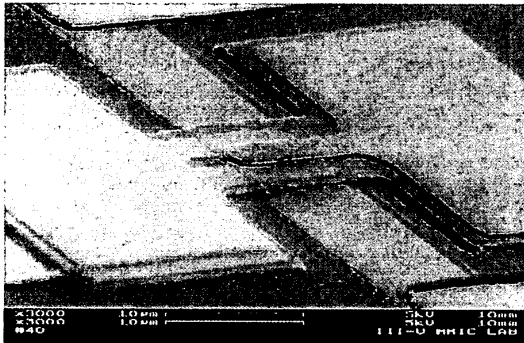

Fig. 2 The SEM photograph of the self-aligned HBT with sidewall technique

3. Device Performance and Discussions

The device dc characteristics were measured by directly probing on the wafer using HP4155 parameter analyzer.

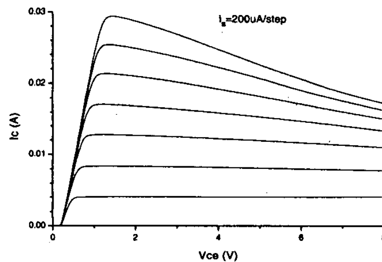

Fig. 3 I_C-V_{CE} characteristics of self-aligned HBT

Fig. 3 shows the dc common-emitter I_C-V_{CE} characteristics of single-finger HBT fabricated by sidewall technique. The area of the device is $3\times15\ \mu m^2$. As can be seen from Fig. 3, device shows excellent dc performance. The current gain is more than 20 and offset voltage is about 200mV. The knee voltage is about 1V at collector current of 30 mA. The negative slope in I-V curve is caused by device self-heat, which will give rise to the current gain decrease.

Fig. 4 shows the Gummel plot of the device. It can be seen from fig. 4 that the junction performance is good and the leakage current is small.

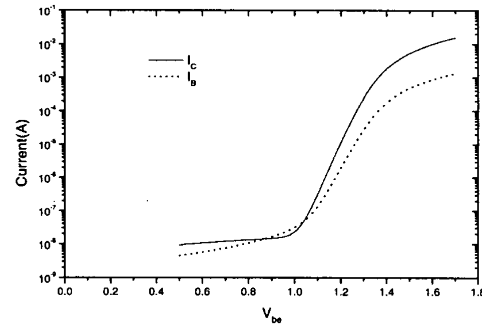

Fig. 4 The Gummel plot of the self-aligned HBT

Fig. 5 shows the RF performance of the device. It demonstrates a current gain cutoff frequency f_T of 30GHz and a maximum oscillation frequency f_{max} of more than 50 GHz .

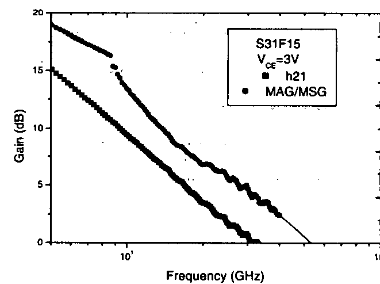

Fig. 5 Microwave performance of self-aligned HBT

4. Conclusion

A self-aligned fabrication process for AlGaAs/GaAs HBT's is presented. The advantage of this process is that self-aligned structure and device passivation

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