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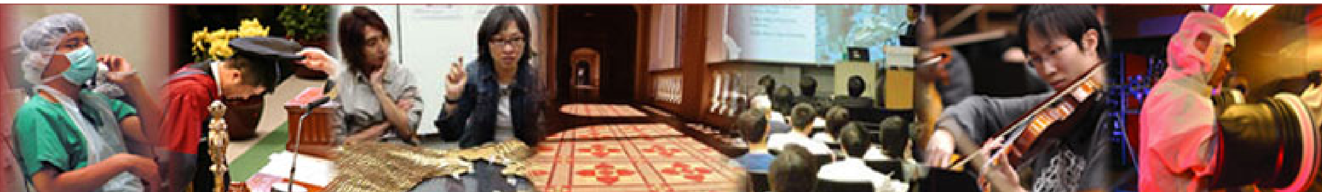

Title	Influences of processing technique on electrical characteristics of TVS used in communication systems
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Influences of Processing Technique on Electrical Characteristics of TVS used in Communication Systems

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Area: Silicon Devices and Technology

Abstract – An improved technique is proposed in fabricating a semiconductor surge protection device which is used in high-speed wideband information transmission systems. In order to increase the surge handling capability of the device, a double p-type diffusion is used. Specifically, in the diffusion step of gallium, SiO_2 is used as a mask to obtain a very small base width and to avoid the reduction of carrier lifetime. It is found that this is a very useful way to reduce the on-state voltage drop and therefore the energy dissipation of the device.

I. INTRODUCTION

Nowadays, electronics are increasingly based on digital signals. Digital systems are providing more and more advanced electronic communication services (simultaneous voice and data transfer, screenphone, message handling, *etc*.). The growing integration of functions makes these systems operate at a wider working band and higher transfer rate, and the energy required for information transfer has been considerably reduced. Furthermore, these systems are mainly made up of VLSI's which are very vulnerable to electromagnetic interference, such as lightning stroke, industrial or operating transient overvoltage. Therefore, the safety and protection of these systems are very important. The protection semiconductor devices used in these systems are generally named as transient voltage suppressor (TVS), whose requirements are summarized as :

1. high surge current handling capability;
2. fast response to the surge and low device capacitance to reduce transmission loss in high-speed wideband transmission systems;
3. high holding current, ensuring the device can be turned off when a surge current rapidly decays;
4. proper protection voltage (i.e. forward breakover voltage), whose exact value is predetermined by the detailed structure of the device;
5. very low leakage current.

A bi-directional TVS is shown in Figure 1(a). It is similar to un-gated pnpn switches which are designed to switch from off-state to on-state when a specified voltage or dV/dt is reached, as described by the I-V characteristic of TVS in Fig.1(b). Since the influences of device area on both the surge capability and the device capacitance are conflicting, the basic consideration of TVS design lies on a small device area adopted to keep device capacitance low enough, and increasing the per-unit-area surge handling capability, which implies that the energy dissipation and temperature rise in the device must be greatly decreased when a surge is induced. On-state voltage drop is a key parameter for the requirement of low energy dissipation. This paper presents an improved fabrication process for decreasing the on-state voltage drop of TVS.

II. THEORETICAL CONSIDERATION

1 *Device capacitance*

From Fig.1(a), device capacitance C_{TVS}

$$\frac{1}{C_{TVS}} = \frac{1}{C_{j1}} + \frac{1}{C_{j2}} + \frac{1}{C_{j3}} \qquad (1)$$

C_{j2} is the single-side linearly graded junction capacitance under reverse bias[1]

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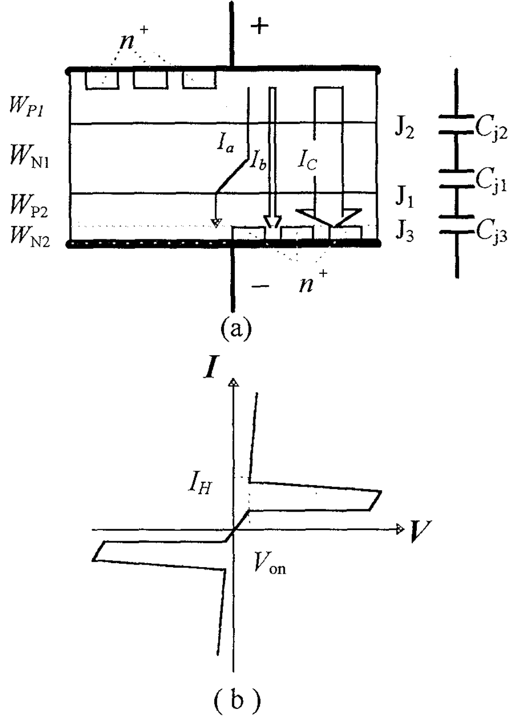

Fig.1 (a) Cross-sectional view and (b) typical I-V characteristic of a bi-directional TVS

$$C_{j2} = \left[\frac{q\varepsilon N_{N1}}{2\left(V_{bi} + V - 2kT/q\right)} \right]^{1/2} \quad (\text{pF/cm}^2) \quad (2)$$

where N_{N1} is the doping concentration of the N_1 layer; V_{bi} is the built-in potential of the pn junction; V is the applied voltage. C_{j1} ,C_{j3} are the depletion capacitance plus diffusion capacitance of the other two pn junctions under forward bias. Since $C_{j1} >> C_{j2}$ and $C_{j3} >> C_{j2}$, $C_{TVS} \approx C_{j2}$. When $N_{N1} = 7.3\times10^{14}/\text{cm}^3$, $C_{j2} = 4.2\times10^3$ pF/cm^2 at V=0V. Hence, for a device area of 0.21×0.21 cm^2, C_{TVS} is 185 pF at V = 0 V, and C_{TVS} = 79 pF at V = 40 V. These values satisfy the requirement of the TVS used in communication systems[2].

2 *On-state voltage drop*

Surge capability, i.e. the ability of a device conducting a large transient surge current without being damaged, mainly depends on the total energy dissipation E in the device during an induced surge which can be expressed as in equation (3), where E_a is the energy dissipation related to the avalanche current I_a; E_b and E_{on} are the energy dissipations of the device in turn-on and on-state periods respectively. Since the period of t_3 - t_4 is much longer than t_1 - t_3 in (3), E_{on} dominates E. Therefore, the reduction of on-state voltage drop V_{on} is a key for the reduction of E.

Under high-injection level , V_{on} is given by[3] equation (4), where L_a, D_a and τ_a are the diffusion length, mobility and lifetime of the charge carriers respectively. W_{N2} and N_{N2} are the width and doping concentration of the N_2 layer. Base width $W_T = W_{P1} + W_{N1} + W_{P2}$, as shown in Fig.1. R_B and R_{CONT} are bulk resistance and ohmic contact resistance of the device. Equation (4) shows that V_{on} is a very strong function of W_T, approximating to a square-law dependence and is inversely proportional to the square root of the carrier lifetime.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

1. *Sample preparation*

The TVS was fabricated mainly by two steps of p-type and n-type impurity diffusions. The electrical characteristics of the device such as breakover forward voltage, on-state voltage drop, holding current are dependent on the first p-type diffusion step which results

$$E = E_a + E_b + E_{on} = \int_{t_1}^{t_2} V_a(t) I_a(t) dt + \int_{t_2}^{t_3} V_b(t) I_b(t) dt + \int_{t_3}^{t_4} V_{on}(t) I_C(t) dt \quad (3)$$

$$V_{on} = \frac{kT}{q} \ln\left(\frac{W_{N2} N_{N2}}{2qD_a n_i^2} J \right) + \frac{W_T^2}{2\mu\tau_a^{1/2}} \frac{\sinh(W_T / L_a)}{[\cosh(W_T / L_a) - 1](2qW_{N2}N_{N2})^{1/2}} + (R_B + R_{CONT}) \cdot I_C \quad (4)$$

Table I p-type diffusion methods

method	I	II	III
	boron-aluminium coated source sealed-tube	aluminium-gallium sealed-tube	aluminium-gallium sealed-tube
Group A	1250 °C 38~45h	1250 °C 32h (Al) + 4h (Ga) +8h (drive in)	Same as method II except 0.8 μm SiO_2 used as a mask during Ga diffusion
Group B	1250 °C 32h	1250 °C 24h (Al) + 4h (Ga) +4h(drive in)	

in an optimum junction depth, impurity profile and carrier lifetime. The choice of diffusion technique is decisive to achieving the required characteristics. The present experiment used three p-type diffusion methods with two diffusion times in each case. The details of the sample preparation are summarized in Table I. These methods are all double impurity diffusion, *i.e.* a deep diffusion of aluminum with low concentration followed by a shallower diffusion of gallium or boron with high concentration. The resulting doping profile is sketched in Fig.2. The size of the samples is 0.044 cm^2, and the original thickness of silicon chip is 0.26 mm.

2 *Results and discussions*

The I-V characteristics of the samples are measured and their V_{on} and I_H are plotted in Fig.3. It is clear that V_{on} of group B is greater than that of group A, as predicted in (4). It is particularly meaningful that the samples made by method III have a slightly lower V_{on} than those by method II. This phenomenon is probably due to the higher carrier lifetime resulting from the diffusion III. Gallium doping source or the processing system may be contaminated by heavy metal species, such as copper, iron, gold, etc, which introduce at least two impurity levels in the band gap that act as the recombination centers and result in a shorter hole lifetime in the n-base. These heavy metal elements are fast diffusing elements in silicon, but have a very low diffusion coefficient in SiO_2[4]. On the other hand, the diffusion coefficient of gallium in SiO_2 is very high (about 8×10^{-9} cm^2/s at 1200 °C), and over 1000 times larger than those of the heavy metal contaminants. In other words, SiO_2 is transparent to gallium but is a mask for the heavy metal contaminants at high temperatures. In method III, SiO_2 resists the heavy metal contaminants into silicon, and avoids the reduction of carrier lifetime. A lower V_{on} can therefore be obtained.

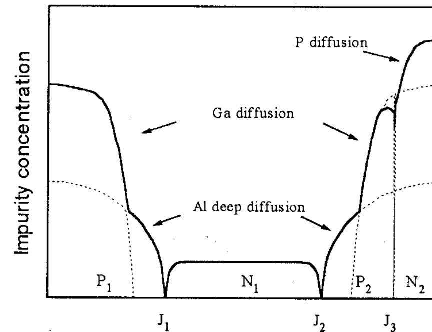

Fig.2 Doping profile of the TVS device with double impurity diffusion

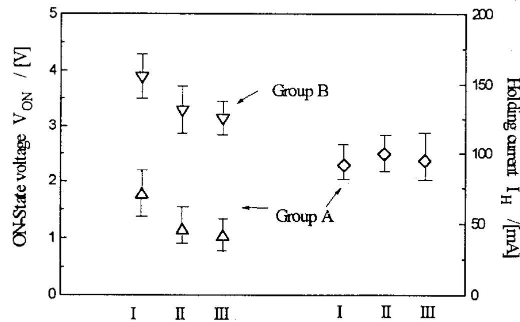

Fig.3 On-state voltage (triangles) and holding current (diamonds) resulting from different diffusion methods

A theoretical I-V characteristic of a pnpn structure was derived by Kurata[5] by solving a complete set of semiconductor device equations. It was shown that the holding

current was reduced by a factor of 100 as the lifetime increased from 0.8 to 2 μs. However, the holding current remains almost the same in our experiment. This is probably due to the existence of cathode shorting which dominates the value of holding current.

IV CONCLUSION

Three types of p-type diffusion methods are studied to clarify the dependence of the surge capability of TVS on base width and carrier lifetime by measuring the on-state voltage drop of the device. Aluminum and gallium double diffusion can produce a very narrow base. Furthermore, a layer of SiO_2 is used as a mask against heavy metal contaminants in the gallium diffusion step to avoid the degradation of carrier lifetime and to decrease the on-state voltage drop further.

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SESSION 5: MODELING AND SIMULATION

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