INTERFACE-STATE-INDUCED DEGRADATION OF GIDL CURRENT IN N-MOSFET'S UNDER HOT-CARRIER STRESS

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Interface-state creation due to hot-carrier stress constitutes a major device-reliability concern and attracts much research interest [1]-[3]. It has been found that interface-state generation (ΔD_{it}) takes place mainly in the low-to-medium gate-voltage (V_G) region. Its effect on the electrical characteristics of MOSFET's is obvious in terms of threshold voltage V_T, subthreshold gradient and gate-induced-drain-leakage (GIDL) current. By measuring the shift in V_T or GIDL current, it is possible to determine the change in interface-trap density. It was suggested by Duvvury et al. [4] that the increase in GIDL current was a direct result of the shift of flat-band voltage due to ΔD_{it}. However, Chen et al. [5] reported that for an n^+ gated diode, ΔD_{it} merely enhances GIDL current via an increase in surface generation velocity. More recently, Hori [6] discussed ΔD_{it}-related GIDL current based on the band-to-band (B-B) tunneling process via interface state. The present work intends to make further exploration on the dependence of stress-enhanced GIDL current on the created interface traps during stressing.

Conventional-S/D n-MOSFET's with thermal SiO_2 (OX) and nitrided oxide (NO) as gate dielectrics were used. NO samples were nitrided at 1150 °C for 120 s in pure NH_3 ambient in a rapid thermal processing (RTP) system. The final oxide thickness of OX and NO samples (measured by C-V) was 120 Å and 90 Å respectively. The devices were subject to hot-electron stress with $V_G = 0.5V_D = 3$ V, for 1000 - 4000 s to create interface traps. GIDL current was measured before and after stress with $V_D = 3$ and 5 V, $V_G = -3$ V for OX devices, and $V_G = -2$ V for NO devices in order to attain approximately the same vertical-field dependence as the one in OX devices. The source and substrate were grounded. All the stressings and measurements were performed for MOSFET's with 1.2-μm channel length and 24-μm width in a nitrogen ambient under light-tight and electrically shielded condition, using an HP 4145B semiconductor parameter analyzer.

Fig.1 shows the measured pre-stress (solid line) and post-stress (broken lines) GIDL currents for OX samples. Along the arrow direction, stress time increases from 0 s to 4000 s with an increment of 1000 s. It can be seen that after stressing for 1000 s, GIDL current increases significantly, and for stress time above 1000 s, the shift of GIDL current becomes gradually smaller and then the GIDL current reaches almost a saturation value after stressing for 4000 s. This saturation phenomenon seems to indicate that the interface-trap creation is limited by the number of potential trap sites available. The observed increase in post-stress GIDL current is obviously different from that induced by oxide traps because oxide traps only induce GIDL current transient in a time scale of seconds. So it should be solely ascribed to interface traps created during stress since the stress method of $V_G = 0.5V_D$ is mostly responsible for the interface- state generation [1]. In other words, an interface-trap-assisted tunneling conduction mechanism [7] may exist after hot-electron stress. In detail, when drain voltage is low and the band is not sufficiently bent, the Fermi level is still within the bandgap and the direct B-B

tunneling hardly happens. But the excitation of trapped electron from interface traps into higher energy levels, followed by tunneling into the conduction band is possible since the tunneling barrier height is smaller for excited electrons than for direct B-B tunneling. Furthermore, it can be deduced that the interface states created during stress have different energy levels based on the fact that post-stress GIDL current increases under both measurement conditions of V_D = 3 V and 5 V . The role of the interface traps with deeper levels (closer to valence band) corresponds to the increase in GIDL current for V_D = 5 V, and shallower-trap-assisted tunneling contributes to the increase for V_D = 3 V, which even becomes the dominant conduction mechanism due to the absence of direct B-B tunneling.

However, for NO samples after a 3000-s stressing, post-stress GIDL current changes scarcely at V_D = 5 V, and for the measurement condition of V_D = 3 V, only a small increase (~ 2.4 pA) in post-stress GIDL current occurs, as shown in Fig.2. As compared to the results of OX samples, it can be concluded that creation of interface states is effectively suppressed during stress, especially the one with deeper levels hardly takes place, which is attributed to nitrogen incorporation at the Si/SiO_2 interface. It is worth noting that the GIDL current measured at V_D = 5 V has a transient, which is possibly attributed to initial oxide traps.

For the above OX and NO samples subject to hot-carrier stress, we repeated the measurement of GIDL current after a sufficiently long time. No significant difference in the measured results was observed, further testifying interface-trap generation and excluding the stress effect of the measurement itself.

Under the band-trap-band tunneling condition, the increased GIDL current can be derived as follows [7]:

$$\Delta I_d = A \exp(-B_{it} / F) \qquad (1)$$

$$B_{it} = \frac{4}{\hbar}(2m_n)^{1/2} \frac{(E_C - E_t)^{3/2}}{3q} \qquad (2)$$

$$E_t = \frac{E_v + (F_1 / F)^{2/3} E_C}{1 + (F_1 / F)^{2/3}} \qquad (3)$$

where A is proportional to the interface trap density, F_1 is lateral field, F is total field, and E_t is the energy level of interface traps which are most effective in the band-trap-band tunneling process. Other variables have their usual definitions. From [2], the trap-assisted leakage mechanism can be further divided into vertical-field (F_2) dominant tunneling and lateral-field dominant tunneling which correspond to different values of B_{it}. On the other hand, for fixed drain and gate bias conditions, F is approximately constant. Thus, qualitatively speaking, the increase in GIDL current is proportional to the generated interface-state density. This implies that some useful information on interface traps created during hot-carrier stressing can be obtained from the observed increase in post-stress GIDL current for stress condition with $V_G \approx 0.5V_D$.

For both extreme cases, 1) if F_1 is much greater than F_2, $F_1 / F \approx 1$ and $E_t \approx 0.5(E_C + E_v) = E_i$ (intrinsic Fermi level) from (3); 2) if F_2 is dominant, $F_1 / F \approx 0$ and $E_t \approx E_v$. This shows that E_t is somewhere between E_v and E_i, strongly dependent on the drain and gate biases. For MOSFET's with conventional S/D, the vertical-field-induced tunneling plays a more important role [2], and B_{it} has a theoretically maximum value of 36 MV/cm. According to [7], A can be expressed as $\Delta D_{it} q W L_1 / (2\tau_{0c})$, where τ_{0c} is effective transit time in the conduction band and L_1

is effective width of ΔD_{it} distribution, about 300 Å (at the gate-drain overlap region near the drain). So, from the measured pre-stress and post-stress curves (e.g. stressing for 3000 s) in Fig.1, the ΔD_{it} values were found to be 8×10^{11} cm^{-2} for $V_D = 5$ V and 3.6×10^9 cm^{-2} for $V_D = 3$ V respectively (in the calculation, $\tau_{0C} = 0.1$ ps [7]). From (3), E_t for the former case is very close to E_v, and E_t for the latter case is a little away from E_v. Therefore, it can be concluded that a large amount of interface traps created during the hot-carrier stress is distributed mainly in a narrow region very close to the valence band. The above calculations are just a rough estimation on interface-state generation, because precise calculation requires an accurate field distribution.

In summary, the dependence of increase in post-stress GIDL current on creation of interface states during hot-carrier stress with $V_G = 0.5V_D$ was investigated. An interface-trap-assisted tunneling conduction mechanism is proposed to account for the increase. The stress method of $V_G = 0.5V_D$ can generate a lot of interface traps near the valence band in OX samples, which is considerably suppressed in NO samples. From the linear relationship between increase in post-stress GIDL current and created interface-state density during hot-carrier stress, ΔD_{it} values can be estimated.

References

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