A Novel High Frequency Current-Driven Synchronous Rectifier Applicable to Most Switching Topologies

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***Abstract*—A novel current-driven synchronous rectifier is presented in this paper. With the help of current sensing energy recovery circuit, the proposed current-driven synchronous rectifier can operate at high switching frequency with high efficiency. Compared with those voltage-driven synchronous rectification solutions, this current-driven synchronous rectifier has several outstanding characteristics. It can be easily applied to most switching topologies like an ideal diode. Constant gate drive voltage can be obtained regardless of line and load fluctuation. This makes it desirable in high input range application. Converters designed with this synchronous rectifier are also capable of being connected in parallel without taking the risk of reverse power sinking. Principle of operation is given in the paper. A series of experiments verify the analysis and demonstrate the merits.**

***Index Terms*—Current-driven, low voltage high current, synchronous rectification, voltage-driven.**

I. Introduction

THERE are ever-increasing demands in telecommunication system and computer equipment for low voltage, high current power supplies. To lower the severer rectification loss associated with low voltage and high current, synchronous rectifier (SR) is commonly used to replace conventional schottky diode as rectification component. The major difficulty in synchronous rectification technique is the gate drive design. Generally speaking, this SR drive signal can be obtained through two ways, self-derived and external-controlled. Self-derived method develops SR gate drive signal by detecting either the current flowing through SR [1]–[3] or the voltage drop across a SR [4]–[6]. External-controlled method develops a SR drive signal from the voltage signal that exists in the switching topology and coincides with the desired drive timing. It is also called voltage-driven or self-driven method. Many researchers did a lot of work in voltage-driven synchronous rectification [7]–[23]. Circuit implementation and operation are generally known. The salient advantage of these voltage-driven SR solutions is simple. Nevertheless, they do have some weaknesses as listed below:

1) Different switching topologies need different voltage-driven SR solutions. Forward, flyback, half-bridge center tap or current doubler, each needs its specific drive method [7]–[19]. Design becomes more complicate in some operation modes, such as discontinuous mode, or in some topologies, such as symmetric drive half-bridge center tap or current doubler.
2) Gate drive voltage of voltage-driven SR is proportional to the input voltage. This input voltage range has to be limited in order to drive a SR properly. However, there do exist cases that demand wider input voltage variation. For example, in a universal input ac/dc system, input voltage varies from 85 Vac to 275 Vac. Another case is in dc/dc telecommunication system, where sometimes the input of 18 V$\sim$72 V is required. In these applications, driving a SR safely and efficiently at both low line and high line becomes a great challenge.
3) In most circumstances, voltage-driven SR converter is not suitable to be connected in parallel [20]–[22]. The simple reason is that voltage-driven SR is a bi-directional switch that allows both forward current as well as reverse current flowing through itself. So converters built with voltage-driven SR usually can either source or sink power. If they are connected in parallel so as to increase output power, there exists the possibility that certain amount of reverse current flows into some converters while other converters have to provide extra power to the system. It may easily cause system failure if this happens.

In this paper, a novel current-driven synchronous rectifier that aims at circumventing all the above-mentioned weaknesses is proposed. It makes use of a current transformer to detect SR current and generate drive signal according to the current direction. When there is forward current flowing through source to drain of SR, the SR gate turns on. When there is reverse current trying to flow through drain to source of SR, the SR gate turns off.

Although the concept of current-driven synchronous rectifier was proposed more than ten years ago [1], feasible operation frequency reported is low, for example, 100 kHz for a bipolar transistor SR [2] and 25 kHz for a MOSFET SR [3]. The reported frequency range and SR performance obviously cannot meet the requirement of modern power conversion where efficiency and size are of primary concerns. Fig. 1 shows the block diagram of a conventional current-driven SR. Under conventional design, current sensing circuit is dissipative. To minimize this current sensing loss, voltage drop across current sensing part must be as small as possible. If voltage drop of a SR is 0.1 V (typical), then voltage drop of current sensing component has

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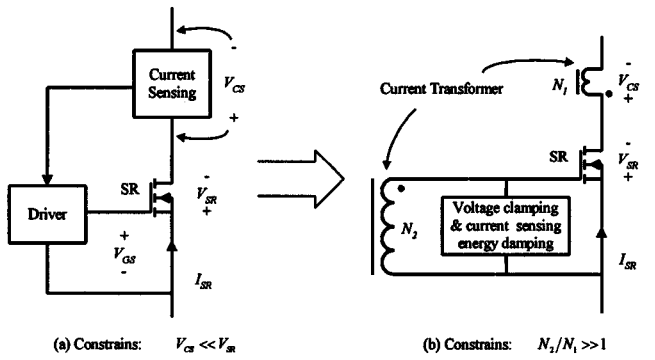

Fig. 1. Conventional current-driven synchronous rectifier: (a) block diagram and (b) implementation.

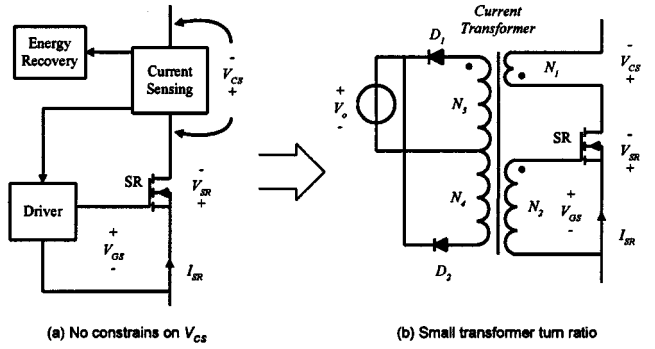

Fig. 2. Proposed current-driven synchronous rectifier: (a) block diagram and (b) implementation.

to be significantly smaller than 0.1 V (e.g., 0.01 V, one tenth of SR drop). The minuscule current signal needs to be magnified to at least 5 V to properly drive a SR. This would require a very high gain-bandwidth product voltage amplifier when converter operates at high switching frequency. If current sensing and voltage amplifying circuit is implemented with a current transformer, we will need a current transformer with a very high turn-ratio (500 : 1 in this example). First, this will make practical implementation of a current transformer rather awkward. Moreover, low current gain and large leakage effect associated with a high turn ratio transformer will introduce significant delay at switching transient and further deteriorate the SR performance. These explain why conventional current-driven SR is not feasible to operate at high switching frequency.

II. Energy Recovery Current-Driven Synchronous Rectifier

To push up operation frequency of conventional current-driven SR, an energy recovery current-driven SR is proposed as shown in Fig. 2. A power conversion circuit is added to deliver the current sensing energy to a dc source. By recovering this sensing energy, current sensing voltage can be designed even higher than voltage drop of SR while not introducing too much extra loss. For example, current sensing voltage can be designed to be 0.5 V, which is five times as high as the typical 0.1 V SR voltage drop. To convert this current sensing signal to the same 5 V SR drive voltage, only ten times voltage amplification is now needed. In other words, a voltage amplifier with the same gain-bandwidth product can operate at much higher frequency (in this example, 50 times higher than under conventional design). If current sensing and voltage amplifying circuit is implemented with a current transformer, turn ratio of only 10 : 1 can be used. It significantly eases the design of a current transformer. Smaller turn-ratio also brings other benefits such as higher current gain and less leakage effect. All these contribute to implementing a high-frequency high performance current-driven SR.

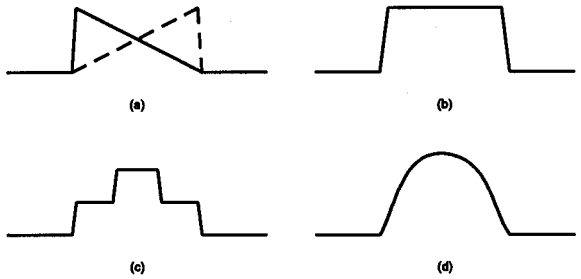

Fig. 3. Typical rectifier current waveform: (a) discontinuous mode, (b) continuous mode, forward, flyback, asymmetric drive half-bridge center-tap or current doubler, (c) symmetric drive half-bridge center-tap or current doubler, and (d) resonant topologies.

Basic operation of this energy recovery current-driven synchronous rectifier is straightforward. As shown in Fig. 2(b), when current flows through source to drain of SR and N_1 winding of current transformer, diode D_1 conducts and delivers energy taken in from winding N_1 to a dc voltage source. This dc source can be any dc voltage within a converter. Usually it is just the converter dc output. Reflected voltage of winding N_2 turns on the SR. As long as SR current continues to flow in current transformer and the dc voltage is stable, the SR drive voltage keeps constant regardless of line fluctuation. When the SR forward current drops to zero and tends to go negative, diode D_1 blocks but diode D_2 turns on to reset the magnetizing energy. Gate voltage of the SR goes negative and the SR shuts down. Hence no reverse current is allowed to flow through SR. Characteristic of the proposed current-driven SR is very much like an ideal diode.

In various switching topologies or under different operation modes, current shape of a rectifier can be any of the four types shown in Fig. 3. As can be understood from the following analysis and then verified by experiments, the proposed current-driven synchronous rectifier can work properly under all these current excitation cases. Trapezoidal wave shown in Fig. 3(b) is the most general case through which we can understand the mechanism of this proposed current-driven SR.

The circuit model used to study the behavior of this current-driven synchronous rectifier is shown in Fig. 4(a). Typical waveforms are given in Fig. 4(b). Current transformer is modeled as a perfectly coupled transformer with a magnetizing inductance L_M at N_2 winding. Leakage effect is omitted. SR MOSFET gate capacitance C_g is taken as a constant. Winding capacitance merges into gate capacitance as C_g. SR MOSFET is considered as an ideal switch with propagation delay omitted.

Detailed description of this energy recovery current-driven synchronous rectifier will be given in the next section. The following merits are highlighted.

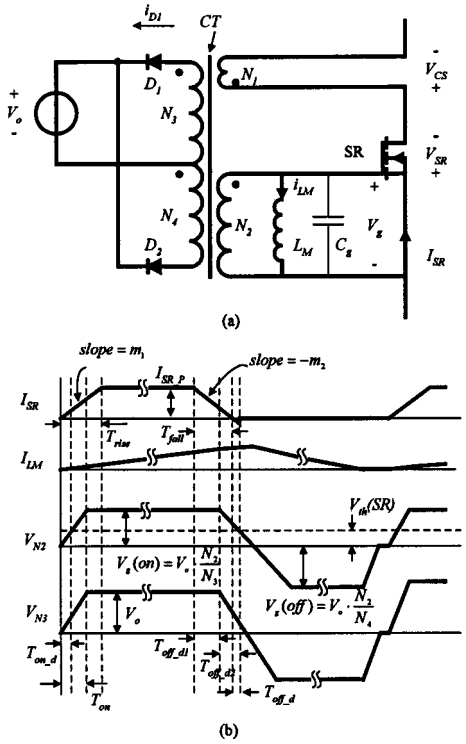

Fig. 4. Current-driven synchronous rectifier: (a) circuit model and (b) critical waveforms.

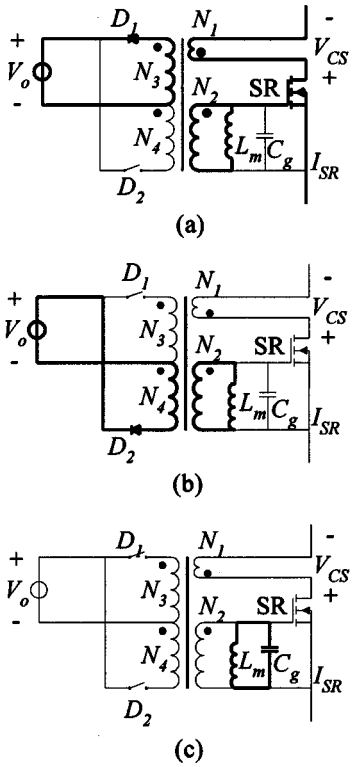

Fig. 5. Steady state operation of energy recovered current driven SR: (a) on mode, (b) off mode I, and (c) off mode II.

1) The proposed current-driven SR can operate at high frequency with high efficiency.
2) The proposed current-driven SR can be applied to most popular topologies.
3) Constant drive voltage can be obtained during line variation. This drive voltage can also be programmed through the adjustment of winding turn-ratio.
4) Converters built with the proposed current-driven SR can be paralleled without taking the risk of reverse power sinking.

III. Principle of Operation

A. Steady State Analysis

Steady state here represents the operation period when the current-driven SR is driven fully on or fully off after switching transition period. As shown in Fig. 5, there are all together three operating modes during steady state.

On Mode: This mode is shown in Fig. 5(a). SR current flows into N_1 winding of current transformer and the reflected current flows out through two paths. One goes through N_3 winding and diode D_1 to dc voltage V_o. The other one goes through N_2 winding to magnetizing inductance. Winding N_1 and N_2 is clamped by dc source V_o. During this period, magnetizing current builds up linearly. The following equations can be obtained:

$$V_{\rm CS} = V_o \times \frac{N_1}{N_3} \tag{1}$$

$$V_g(\text{on}) = V_o \times \frac{N_2}{N_3} \tag{2}$$

$$i_{Lm}(t) = \frac{V_g(\text{on})}{L_m}\, t = \frac{V_o}{L_m} \times \frac{N_2}{N_3}\, t; \quad 0 \le t \le DT_S \tag{3}$$

$$I_{Lm\_\max} = \frac{V_o}{L_m} \times \frac{N_2}{N_3}\, DT_S \tag{4}$$

$$i_{D1}(t) = \frac{N_2}{N_3}\left[I_{\rm SR\_P} \times \frac{N_1}{N_2} - i_{Lm}(t)\right] \tag{5}$$

where

$I_{\rm SR\_P}$ peak forward SR current as illustrated in Fig. 4(b);
D equivalent duty cycle of this SR;
T_S switching period;
$N_1 \sim N_4$ numbers of turn of four windings.

Other parameters are defined as shown in Fig. 4(b).

Gate drive voltage can be programmed by (2). The maximal magnetizing current can be found by (4). Current transformer should not saturate at this maximal current. To ensure SR safely turn on, current in diode D_1 should always conduct so as to clamp SR gate voltage. If magnetizing current goes so high so that it takes over the whole reflected current, diode D_1 will shut down and gate voltage will resonate back to zero. To avoid this, from (5)

$$I_{Lm\_\max} \le I_{\rm SR\_P}\, \frac{N_1}{N_2}. \tag{6}$$

From (5) and (6), we can find the minimal magnetizing inductance

$$L_m \ge \frac{V_o \cdot DT_S \cdot N_2^2}{I_{\rm SR\_P} \cdot N_1 \cdot N_3}. \tag{7}$$

In a practical design, the maximal magnetizing current is usually much smaller than the reflected winding current $I_{\mathrm{SR\_}P} \times N_1/N_2$, so (5) can be simplified as

$$i_{D1}(t) \approx I_{\mathrm{SR\_}P} \times \frac{N_1}{N_3}. \tag{8}$$

OFF Mode I: This mode is shown in Fig. 5(b). When current flows through SR drops to the point that is insufficient to sustain magnetizing current, reset winding N_4 and diode D_2 conduct and take over magnetizing energy while diode D_1 and winding N_3 don't conduct. Again winding N_2 is clamped by V_o. SR drive voltage is now negative. Magnetizing current decreases linearly until it reaches zero. There are following equations:

$$V_g(\mathrm{off}) = -V_o \times \frac{N_2}{N_4} \tag{9}$$

$$i_{Lm}(t) = I_{Lm\_\max} - \frac{V_g(\mathrm{off})}{L_m}(t - DT_S). \tag{10}$$

To ensure magnetic reset, magnetizing current should drop to zero before the next switching cycle. From (4), (9), (10), we can get the following constrain for winding turn ratio and duty cycle

$$D \le \frac{N_3}{N_3 + N_4}. \tag{11}$$

OFF Mode II: This mode is shown in Fig. 5(c). When magnetizing current resets to zero, diode D_2 blocks. In winding N_2, SR gate capacitance resonates with magnetizing inductance. The SR gate voltage drops to zero and then remains around zero. Some damping network can be added in practical design to absorb the excessive resonant energy in case drive voltage goes beyond SR threshold voltage and falsely triggers the SR on.

Extra energy loss during steady state is mainly from the current flowing through diode D_1. Current transformer itself can be designed with high efficiency due to magnetizing energy recovery. Loss due to current flowing thorough diode D_2 can be neglected because magnetizing energy is usually much smaller than the current sensing energy

$$P_{Loss\_D1} = V_{F\_D1} \times I_{D1} \times D = V_{F\_D1} \times I_{\mathrm{SR\_}P} \times \frac{N_1}{N_3} D \tag{12}$$

where V_{F_D1} is the forward voltage drop of diode D_1.

B. Transient Analysis

Transient analysis describes the SR operation during switching transition period. This period is short compared with the switching period but it more or less determines the overall performance of the SR. Any timing discrepancy between current and gate drive voltage will introduce either SR body diode conduction loss or cross-conduction loss. Turn on and turn off transition is described as follows.

1) Turn On Transient: At turn on transient, a rising current with slope m_1 flows into the SR and current transformer. This slope is determined by the external applied voltage and the parasitic inductance in the rectification loop. As can be shown in Fig. 6(a), when this SR current starts to build up, the coupled current in current transformer first flows out from N_2 winding and charges up SR gate. N_3 and N_4 windings dont conduct. Equivalent circuit can be redrawn as Fig. 6(b) and Fig. 6(c). Solving this second order circuit with zero initial conditions, we get

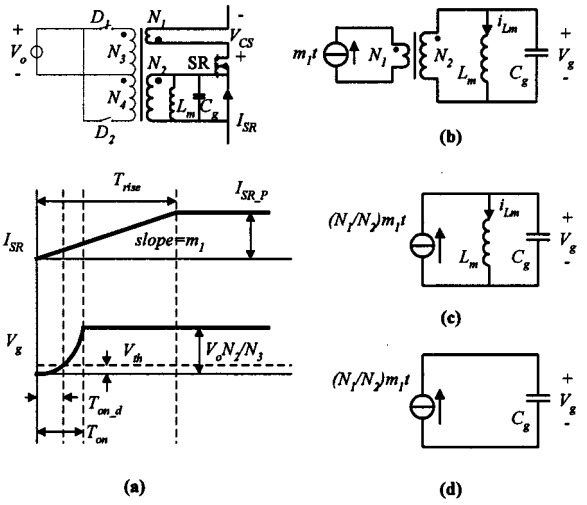

Fig. 6. Turn on transient equivalent circuit: (a) circuit model and critical waveforms, (b) turn on circuit model, (c) turn on equivalent circuit, and (d) simplified turn on equivalent circuit.

$$\omega = (L_m C_g)^{-1/2} \tag{13}$$

$$v_g(t) = -m_1 \frac{N_1}{N_2} L_m \cos \omega t + m_1 \frac{N_1}{N_2} L_m \tag{14}$$

$$i_{Lm}(t) = m_1 \frac{N_1}{N_2} t - m_1 \frac{N_1}{N_2} L_m \omega C_g \sin \omega t. \tag{15}$$

Turn on delay time $T_{\mathrm{on\_}d}$ is defined as the time period from the time when SR current starts to flow into current transformer to the time SR gate voltage reaches beyond SR threshold voltage V_{th}. Turn on time T_{on} is defined as the time when SR current starts to build up to the time gate voltage reaches the clamped voltage $V_o(N_2/N_3)$

$$T_{\mathrm{on\_}d} = \frac{1}{\omega} \arccos\left(1 - \frac{V_{th}}{m_1 \dfrac{N_1}{N_2} L_m}\right) \tag{16}$$

$$T_{\mathrm{on}} = \frac{1}{\omega} \arccos\left(1 - \frac{V_o \dfrac{N_2}{N_3}}{m_1 \dfrac{N_1}{N_2} L_m}\right). \tag{17}$$

Usually SR current rising time T_{rise} is much longer than T_{on}. So the case when T_{on} is shorter than T_{rise} is omitted in the analysis although it can be found following the same procedure.

Considering that this turn on transient occupies only a small part of switching period, and magnetizing current cannot build up instantly within such a short period. The magnetizing inductance with zero initial current can be just taken as open circuit.

Equivalent circuit can be further simplified as Fig. 6(d). Then we can get

$$v_g(t) = \frac{1}{C_g}\int_0^t m_1 \frac{N_1}{N_2}\, t\, dt = \frac{1}{2C_g} m_1 \frac{N_1}{N_2} t^2 \tag{18}$$

$$T_{\text{on\_}d} = \sqrt{\frac{2V_{th}C_gN_2}{m_1N_1}} \tag{19}$$

$$T_{\text{on}} = \sqrt{\frac{2V_oC_gN_2^2}{m_1N_1N_3}} \tag{20}$$

where V_{th} is threshold voltage of SR MOSFET.

From the above analysis, we can find that SR gate capacitance C_g is the critical parameter that would influence turn on delay time. Smaller gate capacitance will speed up turn on process. Lower SR MOSFET threshold voltage and higher current slope rate are also of help to decrease turn on delay time.

It should be noted here that this turn on process is always a preferable zero-voltage-switching process because body diode of the SR conducts before the time gate drive voltage is applied.

Body diode conduction loss $P_{\text{BD\_on}}$ due to turn on delay can be expressed as (21). To address the extra loss caused by SR body diode conduction, SR resistive loss (22) during this turn on transient should be deducted. Then this extra loss becomes

$$P_{\text{BD\_on}} = \frac{m_1 T_{\text{on\_}d}^2 V_{F\_BD}}{2T_S} \tag{21}$$

$$P_{\text{SR\_on}} = \frac{1}{T_S}\int_0^{T_{\text{on\_}d}} (m_1 t)^2 R_{ds\_\text{on}}\, dt = \frac{m_1^2}{3T_S} T_{\text{on\_}d}^3 R_{ds\_\text{on}} \tag{22}$$

$$P_{extra\_loss\_on} = P_{BD\_\text{on}} - P_{SR\_\text{on}} \tag{23}$$

where V_{F_BD} is the voltage drop of SR body diode, R_{ds_on} is the SR turn on resistance.

2) Turn Off Transient: Turn off transient analysis begins at the time when current flowing through SR starts to decline at a rate of $-m_2$ and ends at the time when gate voltage goes negative and is clamped by N_4 winding and V_o. As shown in Fig. 7, there are two operation modes during this transient.

Turn Off Mode I: Circuit diagram is shown in Fig. 7(a). Diode D_1 still conducts and delivers energy to V_o. Gate drive voltage is clamped by winding N_3 and V_o. Current of diode D_1 also drops accordingly with respect to the falling SR current.

Turn Off Mode II: When current in diode D_1 drops to zero, D_1 blocks and circuit model changes to Fig. 7(b). Now N_1 reflected current is less than magnetizing current. There is a resonance in N_2 winding between the magnetizing inductance and gate capacitance.

Critical waveforms during this turn off transient are shown in Fig. 7(c). $T_{\text{off\_}d1}$ is defined as the time period from SR current starts to drop until this SR current drops to the reflected magnetizing current and diode D_1 blocks. $T_{\text{off\_}d2}$ is defined as the time period from this point to the time when SR voltage drops to its threshold voltage. T_{fall} is defined as the duration SR current drops from its steady state value to zero. $T_{\text{off\_}d}$ is defined as the time duration from SR current reaches zero until SR voltage

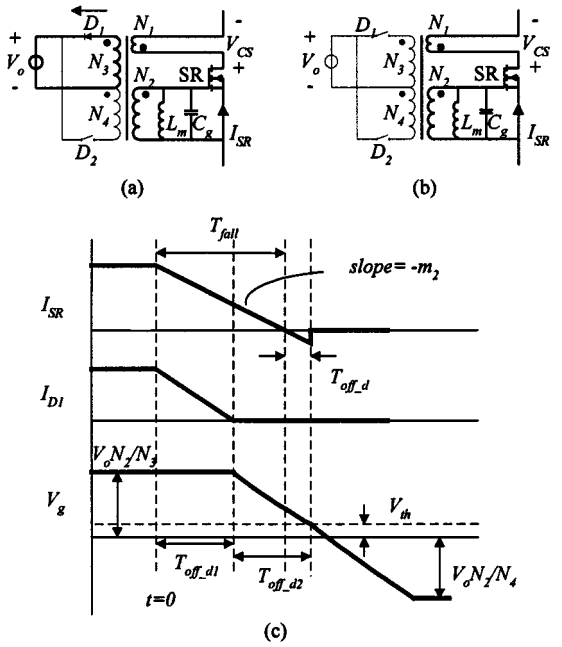

Fig. 7. Circuit modes and waveforms at turn off transient: (a) turn off mode I, (b) turn off mode II, and (c) critical waveforms during turn off transient.

drops below its threshold voltage and SR shuts down. It is obvious that

$$T_{\text{off\_}d} = T_{\text{off\_}d1} + T_{\text{off\_}d2} - T_{fall} \tag{24}$$

$$T_{fall} = \frac{I_{\text{SR\_}P}}{m_2} \tag{25}$$

$$T_{\text{off\_}d1} = \frac{I_{\text{SR\_}P} - \dfrac{N_2}{N_1}\cdot I_{Lm\_\max}}{m_2}. \tag{26}$$

To find $T_{\text{off\_}d2}$, let us consider its equivalent circuit as shown in Fig. 8(a). It is equivalent to Fig. 8(b). We can get

$$v_g(t) = \left(m_2 \frac{N_1}{N_2} L_m + Vo \frac{N_2}{N_3}\right)\cos\omega t - m_2 \frac{N_1}{N_2} L_m \tag{27}$$

$$i_{Lm}(t) = I_{Lm\_\max} - \frac{N_1}{N_2} m_2 t - \omega C_g \left(m_2 \frac{N_1}{N_2} L_m + Vo \frac{N_2}{N_3}\right)\sin\omega t \tag{28}$$

$$T_{\text{off\_}d2} = \frac{1}{\omega}\arccos\left(\frac{V_{th} + m_2 \dfrac{N_1}{N_2} L_m}{V_o \dfrac{N_2}{N_3} + m_2 \dfrac{N_1}{N_2} L_m}\right). \tag{29}$$

Taking (4), (25), (26), and (29) into (24), we get

$$T_{\text{off\_}d} = \frac{1}{\omega}\arccos\left(\frac{V_{th} + m_2 \dfrac{N_1}{N_2} L_m}{V_o \dfrac{N_2}{N_3} + m_2 \dfrac{N_1}{N_2} L_m}\right) - \frac{N_2^2}{N_1N_3}\cdot\frac{V_o}{m_2L_m}\cdot DT_S. \tag{30}$$

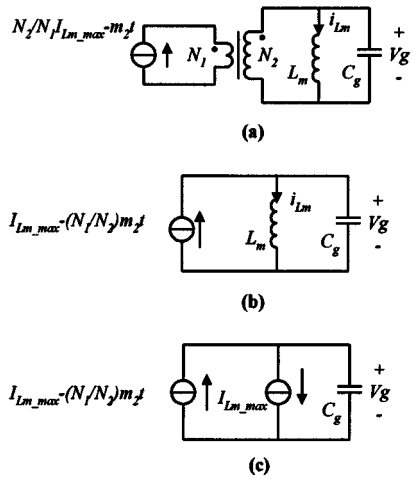

Fig. 8. Circuit model at $T_{\text{off\_}d2}$.

The above analysis can be simplified when we consider the magnetizing inductance is large and magnetizing current keeps constant during this transient. As shown in Fig. 8(c), inductance can be just taken as a current source. Then, we can get

$$v_g(t) = V_g(\text{on}) - \frac{1}{2C_g}\frac{N_1}{N_2}m_2 t^2 \tag{31}$$

$$T_{\text{off\_}d2} = \sqrt{2\cdot\frac{V_g(\text{on})-V_{th}}{m_2}\cdot\frac{N_2}{N_1}\cdot C_g} \tag{32}$$

$$T_{\text{off\_}d} = \sqrt{2\cdot\frac{V_g(\text{on})-V_{th}}{m_2}\cdot\frac{N_2}{N_1}C_g} - \frac{N_2}{N_1}\cdot\frac{V_g(\text{on})}{m_2 L_m}\cdot DT_S \tag{33}$$

$$I_{shut\_down} = m_2\cdot T_{\text{off\_}d} = \sqrt{2\cdot m_2\cdot(V_g(\text{on})-V_{th})\cdot\frac{N_2}{N_1}C_g} - \frac{N_2}{N_1}\cdot\frac{V_g(\text{on})}{L_m}\cdot DT_S \tag{34}$$

$$P_{extra\_loss\_\text{off}} = \frac{1}{T_S}\int_0^{T_{\text{off\_}d}}(m_2 t)^2 R_{ds\_\text{on}}\,dt = \frac{m_2^2}{3T_S}T_{\text{off\_}d}^3 R_{ds\_\text{on}}. \tag{35}$$

The SR shut down current is given in (34). Equation (35) represents the extra loss due to SR turn off delay. It should be noted that turn off delay time $T_{\text{off\_}d}$ as calculated from (33) is not necessarily positive. When negative $T_{\text{off\_}d}$ is obtained, it means SR MOSFET channel switches off before the time SR current drops to zero. In this case, the remaining SR current is carried by its internal body diode. This might occur in discontinuous conduction mode operation where m_2, is much smaller than that in continuous conduction mode.

C. Performance Evaluation

1) Loss Analysis and Efficiency Improvement: From the above transient analysis, we can find out that the proposed current-driven synchronous rectifier introduces extra loss compared with a normal synchronous rectifier with precise drive timing signal due to the turn on delay, turn off delay and conduction loss of Diode D_1. This total extra loss is

$$\begin{aligned}P_{extra} &= P_{loss\_D1} + P_{extra\_loss\_\text{on}} + P_{extra\_loss\_\text{off}}\\ &= P_{loss\_D1} + P_{\text{BD\_on}} - P_{\text{SR\_on}} + P_{extra\_loss\_\text{off}}\\ &\approx P_{loss\_D1} + P_{\text{BD\_on}}\end{aligned} \tag{36}$$

where $-P_{\text{SR\_on}}$ and $P_{extra\_loss\_\text{off}}$ partly cancel out each other. Bear in mind that both of these two items are much smaller than the first and second items so the total extra loss can be simplified as the SR body diode conduction loss during turn on period plus the diode D_1 conduction loss. From (2), (12), (19), and (21), this total extra loss can be expressed by

$$P_{extra} = \frac{N_3}{N_1}\cdot\frac{V_{th}\cdot V_g(\text{on})\cdot C_g\cdot V_{F\_\text{BD}}}{V_o\cdot T_S} + \frac{N_1}{N_3}\cdot V_{F\_D1}\cdot I_{\text{SR\_}P}\cdot D. \tag{37}$$

It can be seen that an optimal N_3/N_1 turn ratio exists to get the minimal extra loss. This optimal turn ratio can be found by differentiating (37)

$$\left.\frac{N_3}{N_1}\right|_{optimal} = \sqrt{\frac{D\cdot V_{F\_D1}\cdot V_o\cdot I_{\text{SR\_}P}\cdot T_S}{V_{th}\cdot V_g(\text{on})\cdot V_{F\_\text{BD}}\cdot C_g}} \tag{38}$$

$$P_{extra}|_{\min} = 2\sqrt{\frac{V_{th}\cdot V_g(\text{on})\cdot V_{F\_\text{BD}}\cdot V_{F\_D1}\cdot I_{\text{SR\_}P}\cdot C_g\cdot D}{V_o T_S}}. \tag{39}$$

N_3 can be determined from (38). N_2 is determined by (2). And N_4 winding is determined by (11). Winding N_4 and diode D_2 only carry magnetizing energy. So low power components can be used.

To further improve the performance of energy recovery current-driven synchronous rectifier so that it can be applied at high frequency, turn on and turn off delay time should be always kept as small as possible. A driver circuit as shown in Fig. 9 can be added between the drive winding N_2 and SR gate capacitance to speed up the switching process. A simple NPN-PNP transistor totem pole driver can fulfill this task. As can be seen from (19) and (33), a critical parameter that affects both turn on and turn off delay time is the SR gate capacitance. Surely the smaller the gate capacitance is, the less the delay time. If the driver has current gain of A, effective input impedance of the driver is then C_g/A, hence turn on and turn off time can all be significantly reduced.

From (39), we can also find out that the minimal extra loss is dependent to practical component parameters. The SR MOSFET with low gate charge and logic level threshold will be beneficial to the reduction of this extra loss. The portion of extra loss induced by current-driven solution should be reasonably

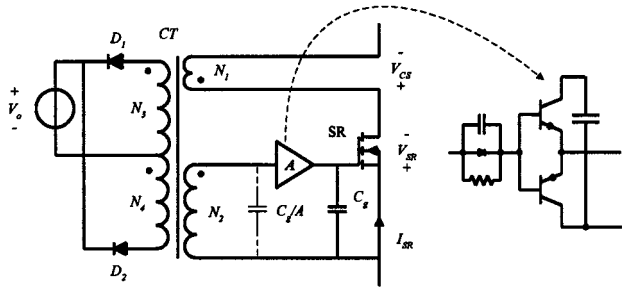

Fig. 9. Improve switching transition process with a driver.

small compared to the loss of an ideal synchronous rectifier. Equations (40) and (41) give the conduction loss of an ideal SR and an ideal schottky diode, where D is the operation duty cycle and V_F is the forward voltage drop of schottky diode. The total loss of this proposed current driven SR is represented by

$$P_{\mathrm{SR}\_ideal} = I_{\mathrm{SR}}^2 \cdot R_{ds\_\mathrm{on}} \cdot D \tag{40}$$

$$P_{sch\_ideal} = V_F \cdot I_F \cdot D \tag{41}$$

$$P_{\mathrm{CDSR}} = P_{\mathrm{SR}\_ideal} + P_{extra}. \tag{42}$$

A design example of a 3.3 V/30 A output low voltage, high current converter is shown here to illustrate the performance of current-driven SR. Assuming that the typical parameters are as follow. SR MOSFET has 2 V threshold voltage, 3000 pf input gate capacitance, 0.8 V body diode voltage drop and 5 mΩ on resistance. SR is driven fully on at 5 V. Forward voltage drop of the energy delivery diode $D1$ is 0.3 V. The operation duty ratio is 0.5. The current transition time from 0 A to 30 A is 60 ns. The operation frequency is 200 kHz. From these parameters, we know that this minimal extra loss is only 7.9% of the ideal SR conduction loss. The total conduction loss is only 53.9% of the conduction loss when a 0.3 V schottky diode is used

$$\frac{P_{extra}|_{\min}}{P_{\mathrm{SR}\_ideal}} = \frac{2\sqrt{\dfrac{2\times 5\times 0.8\times 0.3\times 30\times (3000\times 10^{-12})\times 0.5}{3.3\times (5\times 10^{-6})}}}{30^2\times (5\times 10^{-3})\times 0.5} = 7.9\%$$

$$\frac{P_{\mathrm{CDSR}}|_{\min}}{P_{sch\_ideal}} = \frac{P_{\mathrm{SR}\_ideal} + P_{extra}|_{\min}}{P_{sch\_ideal}} = 53.9\%.$$

The performance is even better when a driver circuit with 10 times current gain is used. Then this minimal extra loss is only 2.5% of the ideal conduction loss

$$\frac{P_{extra}|_{\min}}{P_{ideal}} = \frac{2\sqrt{\dfrac{2\times 5\times 0.8\times 0.3\times 30\times (300.0\times 10^{-12})\times 0.5}{3.3\times (5\times 10^{-6})}}}{30^2\times (5\times 10^{-3})\times 0.5} = 2.5\%.$$

From the above design parameters, the influence of current transformer turn ratio on the extra conduction loss can be illustrated as in Fig. 10. The extra loss is normalized according to the base power of P_{SR_ideal}. If we want to keep the extra loss to be less than 10% of the base power, N_3/N_1 should be about 25 : 1 or more. The effect of driver circuit can also be clearly seen from the same figure. Adding a driver can always minimize the extra loss. This is reasonable because the turn on delay associated loss is smaller when a driver is added. Obviously, the higher the current gain of driver circuit, the lower the extra loss.

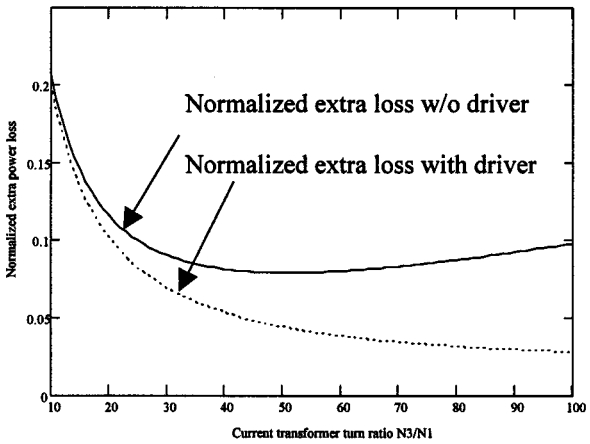

Fig. 10. Normalized extra loss at different transformer ratio $N3/N1$, compared with an ideal SR.

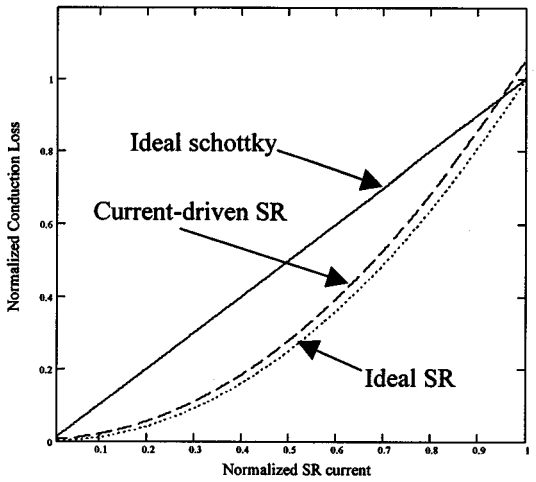

Fig. 11. Normalized conduction loss of CDSR, ideal SR, and ideal Schottky.

Fig. 11 illustrates the loss comparison of an ideal schottky diode, an ideal SR, and this proposed current-driven SR. The base current is the current where forward voltage drop of SR is equal to the forward drop of schottky. The base power is the ideal schottky loss power at base current. Here the base current is 0.3 V/5 mΩ = 60 A. The base power is 0.3 V $\times$ 60 A $\times$ 0 $\cdot$ 5 = 9 W. Transformer ratio is chosen at $N_3/N_1 = 20$, which is a tradeoff between the complexity of transformer implementation and reduction of conduction loss. It can be easily seen that the ideal SR can always save conduction loss over an ideal schottky diode when the current is smaller than the base current. The proposed current-driven SR introduces an extra loss compared with an ideal SR but it is better than an ideal schottky diode in most of the current range.

In general, it is true that the proposed current driven SR introduces extra loss over an ideal SR. But the extra loss is not significant under proper current transformer and driver design. Bear in mind that an ideal SR is nonexistent. Even for a voltage-driven SR, it is very difficult to drive the turn on and turn off precisely according to its current. It also has the same turn on/off delay problem and its associated loss.

2) Effect of Output Ripple Introduced by the Proposed Current-Driven SR Solution: In this proposed current-driven synchronous rectification solution. The current sensing energy will be delivered to the output through the energy recovery winding, which may affect the output current ripple. In a conventional forward SR converter, output current ripple can be expressed by

$$\Delta I_{PP} = \frac{Vo \cdot (1-D) \cdot Ts}{L} \tag{43}$$

where L is the output inductance.

If the two SR's in the forward converter are replaced by two current-driven SR, in the continuous current mode, the output current ripple can be expressed by

$$\Delta I_{PP1} = \frac{(Vo+Vc) \cdot (1-D') \cdot Ts}{L'} \tag{44}$$

where

L' same value as L or another designed value;
Vc clamping voltage of freewheeling current driven SR;
D' duty cycle.

Assuming that the clamp voltage is small compare with Vo, through the volt-second principle, we can prove that

$$D' \approx D \cdot (1+K) \tag{45}$$

where K is the current transformer turn ratio N_1/N_3. Vc can be expressed by (1), then (44) can be expressed

$$\Delta I_{PP1} = \frac{Vo \cdot (1+K) \cdot [1-D \cdot (1+K)] \cdot Ts}{L'}. \tag{46}$$

At the output terminal, the switching ripple is actually the ripple of choke plus the ripple of energy delivery diode, which is just in phase while proportional to the choke ripple. So the total switching ripple is (47), and (48) describes the relative ripple value for comparison

$$\begin{aligned}\Delta I'_{PP} &= \Delta I_{PP1} \cdot (1+K) \\ &= \frac{Vo \cdot (1+K)^2 \cdot [1-D \cdot (1+K)] \cdot Ts}{L'}\end{aligned} \tag{47}$$

$$\frac{\Delta I'_{PP}}{\Delta I_{PP}} = \frac{1-D \cdot (1+K)}{1-D} \cdot \frac{L}{L'} \cdot (1+K)^2. \tag{48}$$

When the same choke is used for the two forward converter, (48) is simplified as

$$\frac{\Delta I'_{PP}}{\Delta I_{PP}} = \frac{1-D \cdot (1+K)}{1-D} \cdot (1+K)^2. \tag{49}$$

For the typical value $0.1 < D < 0.6$ and $0.01 < K < 0.1$, (49) is always greater than 1. This means the output ripple will increase if current-driven SR is used in a forward converter. For example, $D = 0.4$, $K = 0.05$, then $\Delta I'_{PP}/\Delta I_{PP} = 1.07$. This shows that the ripple increment is not so significant.

Due to the energy recovery process, the dc current carried by the output choke is smaller than the conventional forward choke. It indicates that for the same the size of magnetic component, a larger inductance value can be obtained. This tends to cancel out the effect of ripple increment.

Usually the conventional voltage-driven SR converter operates at continuous current mode even at light load. The proposed current-driven SR can operate at both continuous current mode and discontinuous current mode just like a diode. So at light load, conventional voltage-driven SR will have much higher ripple than the current-driven SR operating at discontinuous current mode.

3) Some Practical Concerns of Current Transformer Implementation: The proposed current-driven SR solution uses a current transformer to sense current and provide drive signal with sensing energy recovery. This inevitably increases the overall size and cost of a converter. The current transformer is usually implemented with a small toroid core. It is very cheap compared with other power components in the converter. The size of current transformer is mainly determined by the amount of current sensing power taken in by the transformer. As the sensing voltage is much smaller than the output voltage, the sensing power is only a small portion of the total power. For a 3.3 V/30 A power conversion, if the sensing voltage is designed as 0.3 V, the operation duty is 0.5. Then the sensing power is 0.3 V $\times$ 30 A $\times$ 0.5 $=$ 4.5 W. If the efficiency of current transformer is 98%, the loss on the current transformer is only 0.09 W. Practically a small toroid core with dimensions 10 mm $\times$ 5 mm $\times$ 2.5 mm can be used to implement this current transformer.

IV. Experimental Demonstration

A. Wide Input Range, Continuous and Discontinuous Mode

A flyback current-driven SR converter that operates at 80 kHz switching frequency is built. Input voltage of this converter is from 90 V to 315 V (input range 3.5 : 1), the output is 5 V with 3 A maximal current. Current transformer is implemented with turn ratio of 3 : 80 : 40 : 8 ($N_1 \sim N_4$). A driver circuit is added between N_2 winding and SR gate terminal to speed up turn on and turn off transient. SR MOSFET is implemented by HUF76113T3ST (30 mΩ, 30 V, Intersil). Gate capacitance Cg of this MOSFET is measured through an impedance analyzer HP4194 under rated frequency and bias current. Current waveform is measured with Tektronix current probe TCP202. Figs. 12 and 13 show the waveforms captured when converter operates at 90 V and 315 V input, 5 V/2.5 A output. It can be seen clearly that the SR gate voltage properly builds up with respect to its current. A constant drive voltage of 10 V is obtained at both low line and high line. At low line, the converter operates at continuous current mode. At high line, the converter operates at discontinuous current mode. Discontinuous mode is not easily achievable in a voltage-driven SR converter.

To verify the above analysis, the driver circuit is removed so that gate capacitance is driven directly by N_2 winding. The input voltage is set at 120 V. Load current varies from 0.5 A to 3 A full load. Under this input and load range, the flyback converter operates at CCM under heavy load and DCM under light load.

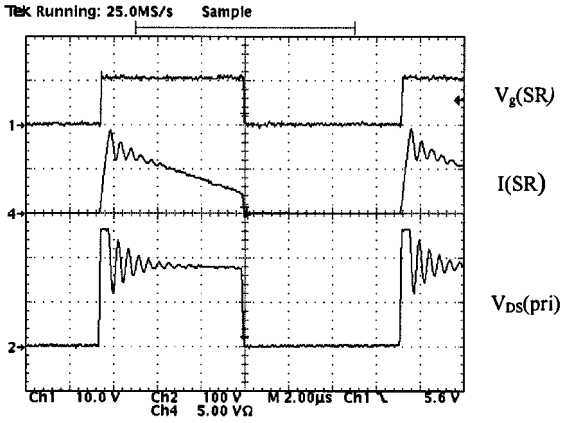

Fig. 12. Flyback converter at 90 V low line (CCM).

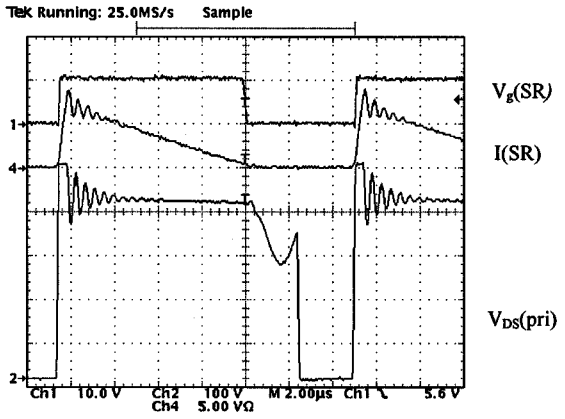

Fig. 13. Flyback converter at 315 V high line (DCM).

TABLE I
TURN ON DELAY MEASUREMENT

120V Input 5V output	Measured T_{on_d} (ns) w/o driver	Calculated T_{on_d} (ns) w/o driver	Error(%)	Measured T_{on_d} (ns) with driver
0.5A	113	105	7.6	25.6
1.0A	72	71	1.4	17.2
1.5A	58	59	1.7	12.8
2.0A	55	53	3.6	12.0
2.5A	52	48	8.3	12.0
3.0A	50	46	8.7	11.0

Calculated and measured turn on delay time is shown in Table I. Current slope m_1 is directly measured through current probe. It should be noted that the current probe has 16 ns propagation delay and this delay should be taken into consideration in all the above measurement. The maximal error is less than 10%. With a NPN-PNP totem pole driver circuit, this turn on delay time can be significantly reduced. This turn on speed is comparable to other voltage driven synchronous rectification solutions.

Turn off delay analysis can also be verified following the similar procedure. Table II shows the measured $T_{\text{off\_}d2}$. It can be

TABLE II
$T_{\text{off\_}d2}$ MEASUREMENT

120V Input 5V output	Measured T_{off_d2} (ns) w/o driver	Calculated T_{off_d2} (ns) w/o driver	Error(%)	Measured T_{off_d2} (ns) with driver
0.5A	840	844	0.5	102
1.0A	840	854	1.6	118
1.5A	840	864	2.8	138
2.0A	93	106	12.3	152
2.5A	91	98	7.1	40
3.0A	87	93	6.5	34.4

TABLE III
$T_{\text{off\_}d}$ MEASUREMENT

120V Input 5V output	Measured T_{off_d} (ns) w/o driver	Calculated T_{off_d} (ns) w/o driver	Error (%)	Measured T_{off_d} (ns) with driver
0.5A	500	485	3.0	-56
1.0A	392	367	6.8	-140
1.5A	304	265	10.7	-258
2.0A	112	91	23.1	-314
2.5A	107	88	21.5	38
3.0A	103	84	22.6	27

seen that the calculated value is also close to the measured value. Finally, turn off delay time $T_{\text{off\_}d}$ is also measured and shown in Table III.

It should be pointed out that when the flyback converter operates at DCM, the SR current slope m_2 is determined by the output voltage and the secondary inductance of the main transformer. Hence it is very small. This makes turn off delay time relatively long. However, this also helps prevent too much excessive reverse current from flowing through the SR. When the experimental converter delivers more than 2 A output current, it operates at CCM. When the converter operates at CCM, the current slope m_2 is determined by the parasitic parameters of the main transformer so it is much higher than in discontinuous mode. From (33), we know the turn off delay is also reduced with respect to. However, from (34), the SR shut down current also increases with respect to m_2. To make sure the SR can shut down as fast as possible, turn off delay time must be kept as small as possible. Adding a driver circuit will significantly speed up the turn off process. Table III also gives the measured turn off delay time at both when a NPN_PNP totem pole driver is added. It can be seen that the turn off delay with a buffer can be as short as 27 ns at 3 A full load. The exemplified waveforms at turn off process are shown in Fig. 14(a) and (b). They clearly illustrate the effect of driver circuit.

In the voltage-driven synchronous rectification, SR is usually shut down before its current goes zero. SR Body diode then carries the current and cause reverse recovery problem. From component datasheet, we know the body diode reverse recovery time of HUF76113T3ST is 44 ns. Most currently available MOSFET body diode reverse recovery time falls in the range of 40∼120

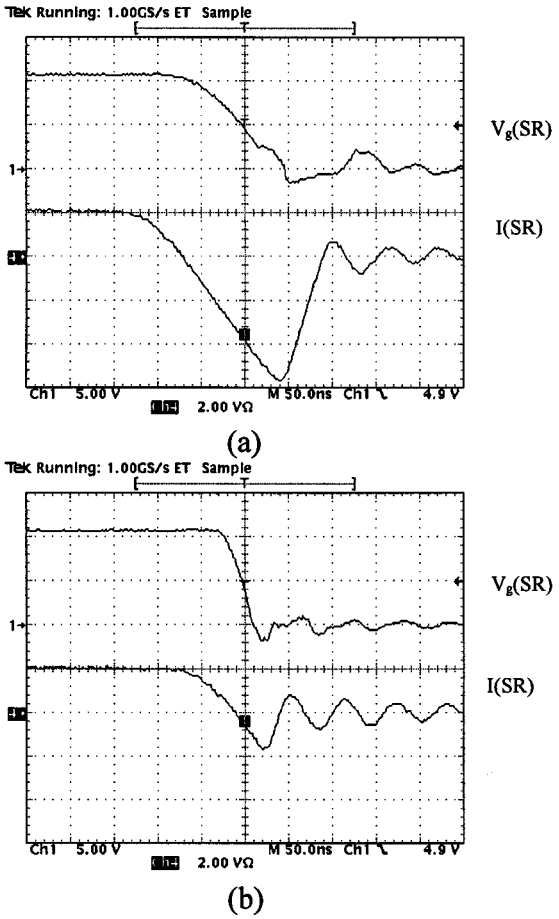

Fig. 14. Exemplified turn off waveforms of Flyback converter at 120 V input 5 V/3: (a) w/o driver and (b) with a totem pole driver.

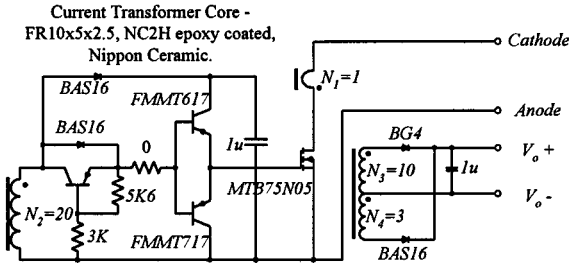

Fig. 15. Current-driven synchronous rectifier module.

ns. With a turn off driver circuit, the turn off delay time of the proposed current driven SR can at least be comparable to the body diode of SR. A better driver design with higher current gain and less propagation delay will shorten the turn off delay time. The loss associated with the turn off delay is the MOSFET channel conduction loss and switching loss. It is much smaller than the body diode conduction loss in a voltage-driven solution.

B. Current Driven SR in Different Switching Topologies

To demonstrate the fact that the proposed current-driven SR can be applied in various switching topologies, in the following experiments, current-driven SR modules as shown in Fig. 15

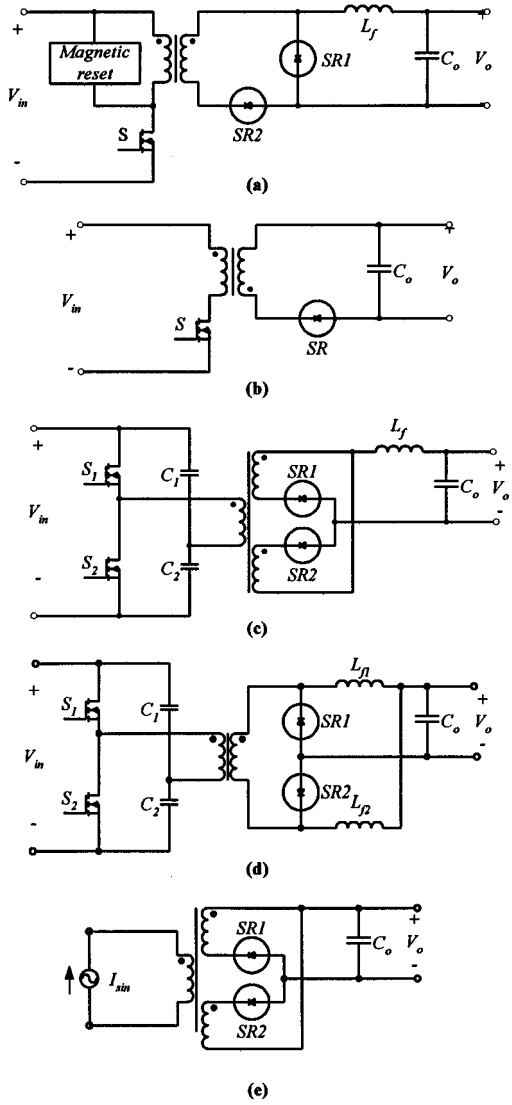

Fig. 16. Current-driven SR in different switching topologies: (a) forward, (b) flyback, (c) half-bridge center tap, (d) half-bridge current doubler, and (e) sinusoidal input full-wave rectification.

are used into different topologies. Applying the current-driven SR module into a switching topology becomes very easy. The module has four terminals. Two of which are the anode and cathode of SR. The left two are energy recovery terminals to be connected to the dc output. Topologies to be evaluated are shown in Fig. 16. For fair comparison, all converters operate at the same 250 kHz switching frequency. Converters shown in Fig. 16(a)–(d) all have 48 V input, 5 V/10 A output except the flyback converter whose output is 5 V/5 A. Fig. 17∼–Fig. 22 show the critical waveforms of current driven SR forward, flyback and half-bridge circuits. Figs. 19 and 21 should be especially highlighted. With conventional voltage-driven solution, it is difficult to drive the two SRs in symmetric drive half-bridge center tap and current doubler topologies. Waveforms of sinusoidal input full wave rectification converter are shown in Fig. 23. Sinusoidal SR current is typical in various resonant topologies. It cam be seen that SR gate drive voltage can also be self-derived. A peak current of 3.8 A is observed. This current is limited by the available power amplifier.

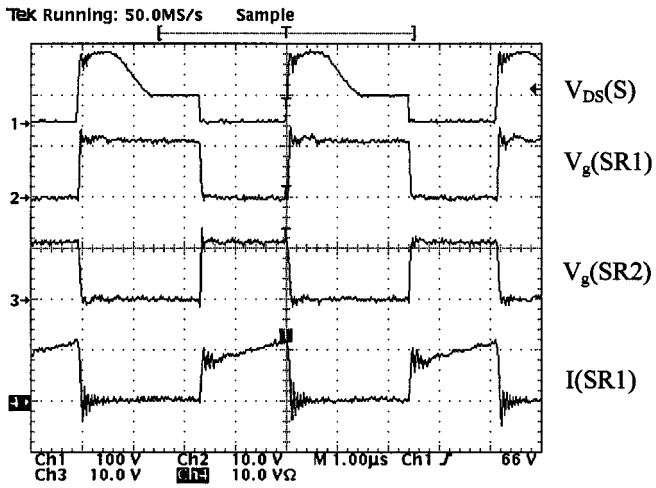

Fig. 17. Critical waveforms in a forward converter.

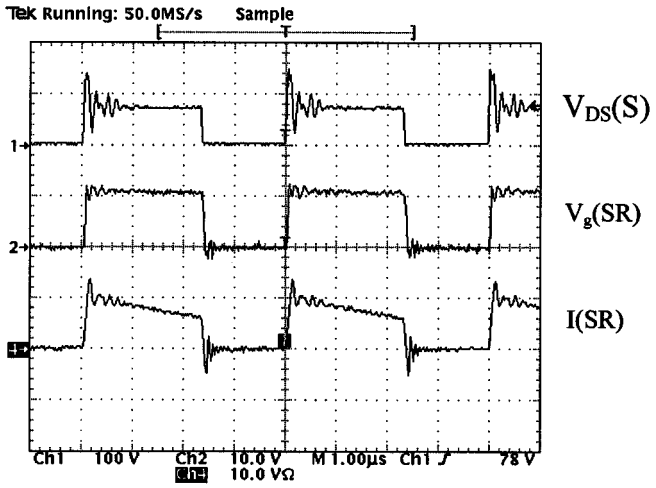

Fig. 18. Critical waveforms in a flyback converter.

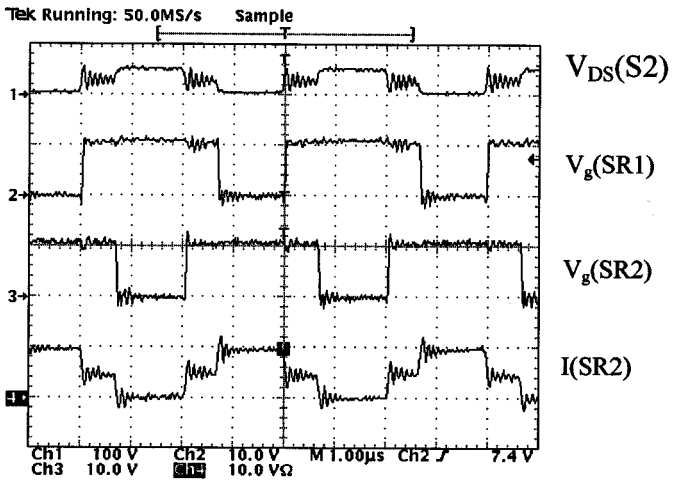

Fig. 19. Critical waveforms in a symmetric half-bridge center tap converter.

In all these experiments, drive voltage is self-derived from the current signal. Current-driven SR module works very much like a diode rectifier.

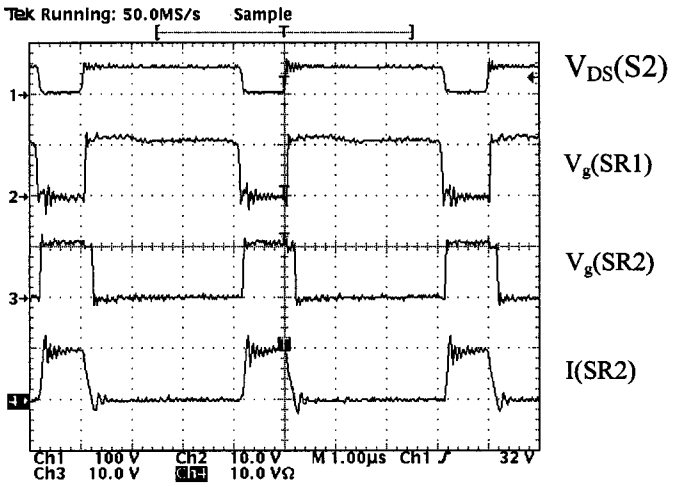

Fig. 20. Critical waveforms in an asymmetric half-bridge center tap converter.

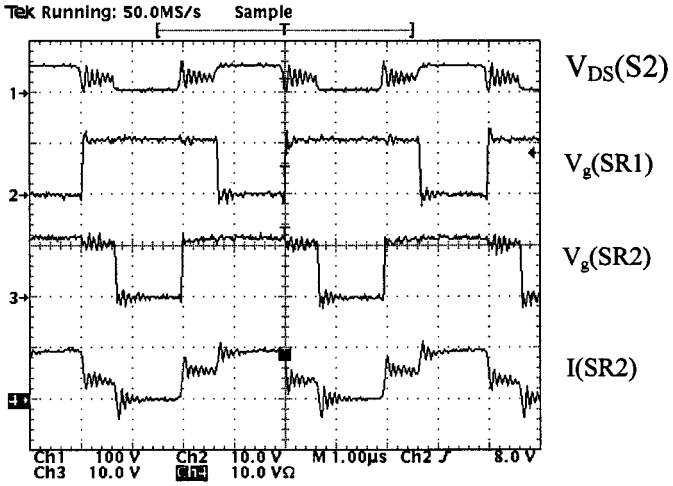

Fig. 21. Critical waveforms in a symmetric half-bridge current doubler converter.

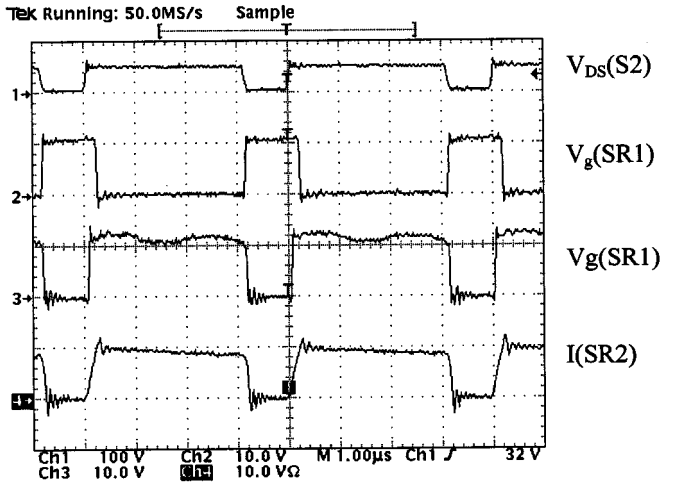

Fig. 22. Critical waveforms in an asymmetric half-bridge current doubler converter.

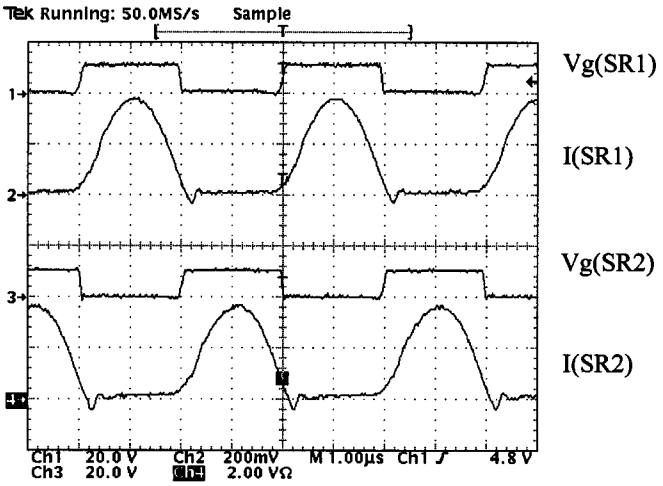

Fig. 23. Critical waveforms in a high frequency full-wave rectification converter.

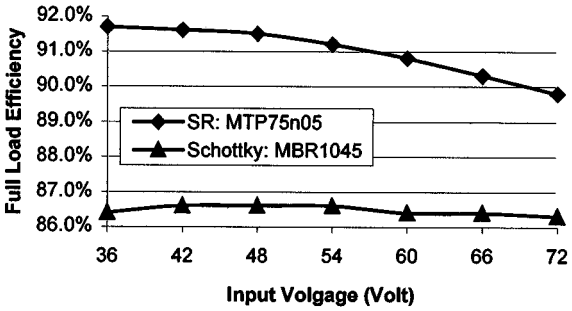

Fig. 24. Efficiency of a 250 kHz, 5 V/10 A current-driven SR forward converter.

C. Efficiency of Current-Driven SR Converters

Although SR modules with the same design parameters are implemented in a variety of switching topologies, it's unfair just to compare the individual efficiency of these converters. Efficiency depends on many parameters such as components selection, PCB layout, and magnetic design. Measured full load efficiency of a 250 kHz, 50 W current-driven SR forward converter is shown as in Fig. 24. The converter has an input voltage between 36 V and 72 V. Its output is 5 V with 10 A maximal current. A maximal efficiency of 91.7% can be achieved at low line. The two SR's are 10 mΩ MTP75N05 (On Semi.). For comparison, the efficiency of this converter with schottky diode MBR1045 is also measured. The efficiency improvement of current-driven SR is 3∼5% over the schottky diode.

D. Paralleling of Current-Driven SR Converters

A conventional voltage-driven SR converter is not suitable to be connected in parallel directly. The reason is that SR MOSFET is a bi-directional switch that allows both forward and reverse current flow. If two voltage-driven SR converters are paralleled together, in some extreme cases, one converter provides power while the other sinks the power. Usually it may cause a system failure when this happens. However, if current-driven SR is used in converter design, no reverse power is allowed to flow into a converter because of its diode like characteristic.

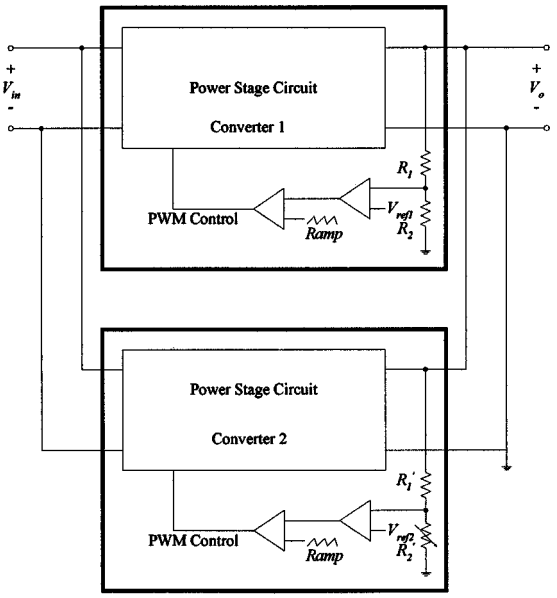

Fig. 25. Paralleling two current-driven SR converters.

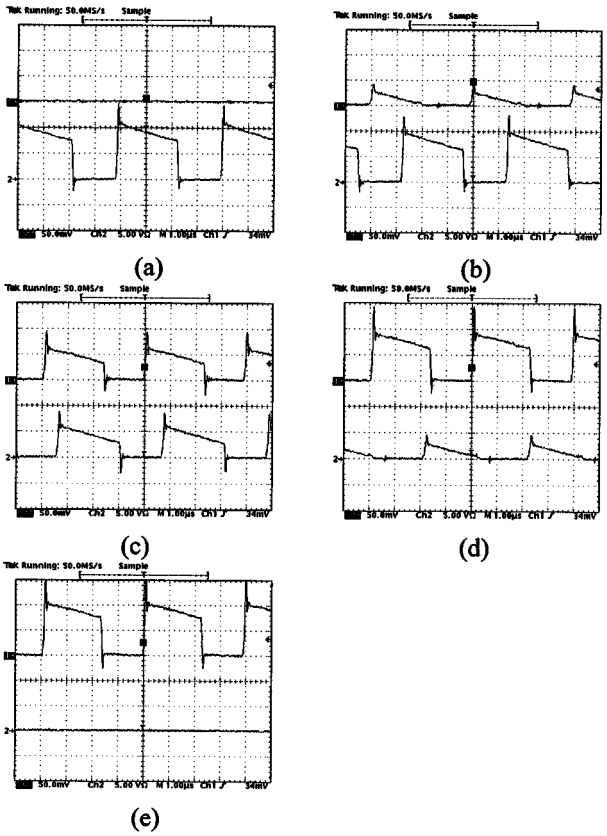

Fig. 26. Current of freewheeling SR in two paralleled forward current-driven SR converters Ch1: freewheel SR current in converter 1 (5 A/div) Ch2: freewheel SR current in converter II.

Converter paralleling experiments are performed as follow. Two 5 V output current-driven SR forward converters are paralleled as shown in Fig. 25. Each of them has its independent control loop. Their input terminals are connected in parallel to the

48 V line voltage. Their output terminals are connected in parallel to a 10 A constant current load. By manually adjusting the sampling resistor R_2', current share ratio between two converters can be changed. Current of freewheeling SR's in the two converters is measured and shown in Fig. 26. In Fig. 26(a), converter 2 provides all output power and converter 1 completely shuts down. There is no reverse current flowing through converter 1. In Fig. 26(b), converter 1 operates at discontinuous mode and converter 2 provides most of the power. In Fig. 26(c), each of the two converters provides around half of the total power. In Fig. 26(d), converter 1 provides most of the power while converter 2 works at discontinuous mode. In Fig. 26(e), converter 1 provides all the power to output and convert 2 shuts down. In all cases, no dangerous reverse power is allowed to flow in any paralleling connected current-driven SR converter.

V. Conclusion

A novel high frequency current-driven synchronous rectifier is proposed and analyzed. Compared with the existing synchronous rectification solutions, this proposed synchronous rectifier has several outstanding characteristics.

Firstly, it provides a universal approach to drive a synchronous rectifier in most switching topologies. It is a four-terminal device with two terminals of anode and cathode as a diode and the other two connected to dc output. It can be easily applied in various topologies such as forward, flyback, half-bridge center tap, half-bridge current doubler and resonant topologies.

Secondly, the proposed current-driven SR has constant drive voltage during line voltage variation. This makes it desirable in high input range application. The SR drive voltage is also easily programmable by adjusting winding turn ratio.

Thirdly, converters built with this current-driven SR can be connected in parallel without taking the risk of reverse power sinking.

These advantages are fully demonstrated through a series of experiments.

References

[1] W. R. Archer, "Current drives synchronous rectifier," *Electron. Des. News*, vol. 30, p. 279, Nov. 1985.

[2] E. Sakai and K. Harada, "A new synchronous rectifier using bipolar transistor driven by current transformer," in *Proc. IEEE Telecommun. Energy Conf. (INTELEC'92)*, 1992, pp. 424–429.

[3] B. Acker, C. R. Sullivan, and S. R. Sanders, "Current-controlled synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'94)*, 1994, pp. 185–191.

[4] H. P. Yee, S. Meyer, K. Horiguchi, M. Wakatabe, A. Sugai, G. Dittmer, and P. O. Lauritzen, "A self-driven synchronous rectifier," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'94)*, 1994, pp. 627–633.

[5] B. Acker, C. R. Sullivan, and S. R. Sanders, "Synchronous rectification with adaptive timing control," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'95)*, 1995, pp. 88–95.

[6] H. L. Pan, Y. C. Liang, and R. Oruganti, "Design of smart power synchronous rectifier," *IEEE Trans. Power Electron.*, vol. 14, pp. 308–315, Mar. 1999.

[7] I. D. Jitaru and G. Cocina, "High efficiency DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'94)*, 1994, pp. 638–644.

[8] J. A. Cobos, O. Garcia, J. Uceda, J. Sebastian, and E. de la Cruz, "Comparison of high efficiency low output voltage forward topologies," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'94)*, 1994, pp. 887–894.

[9] J. A. Cobos and J. Uceda, "Low output voltage DC/DC conversion," in *Proc. 20th Int. Conf. Ind. Electron., Contr., Instrum. (IECON 94)*, 1994, pp. 1676–1681.

[10] J. Blanc, "Practical application of MOSFET synchronous rectifiers," in *Proc. IEEE Telecommun. Energy Conf.*, 1991, pp. 495–501.

[11] H. K. Ji and H. J. Kim, "Active clamp forward converter with MOSFET synchronous rectification," in *Proc. IEEE Power Electron. Spec. Conf. (PESC '94)*, 1994, pp. 895–901.

[12] J. A. Cobos, O. Carcia, J. Sebastian, J. Uceda, and F. Aldana, "Optimized synchronous rectification stage for low output voltage (3.3 V) DC/DC conversion," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'94)*, 1994, pp. 902–908.

[13] J. Uceda and J. A. Cobos, "Supplying power at low voltage (3.3 V)," in *Proc. IEEE Int. Caracas Conf. Devices, Circuits, Syst.*, 1995, pp. 244–251.

[14] M. M. Jovanovic, M. T. Zhang, and F. C. Lee, "Evaluation of synchronous-rectification efficiency improvement limits in forward converters," *IEEE Trans. Ind. Electron.*, vol. 42, pp. 387–395, Aug. 1995.

[15] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," *IEEE Trans. Power Electron.*, vol. 13, pp. 538–546, May 1998.

[16] Y. Panov and M. M. Jovanovic, "Design and performance evaluation of low-voltage/high-current DC/DC on-board modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'99)*, 1999, pp. 545–552.

[17] J. A. Cobos, P. Alou, O. Garcia, J. Uceda, and M. Rascon, "New driving scheme for self driven synchronous rectifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'99)*, 1999, pp. 840–846.

[18] X. F. Xie, H. Y. Chung, and M. H. Pong, "Studies of self-driven synchronous rectification in low voltage power conversion," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst. (PEDS'99)*, 1999, pp. 212–217.

[19] X. F. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "Two methods to drive synchronous rectifiers during dead time in forward topologies," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'00)*, 2000, pp. 993–999.

[20] T. Kohama, T. Ninomiya, M. Shoyama, and R. Tymerski, "Analysis of abnormal phenomena caused by synchronous rectifiers in a paralleled converter system," in *Proc. IEEE Telecommun. Energy Conf. (INTELEC'98)*, 1998, pp. 404–411.

[21] D. K. W. Cheng, X. C. Liu, and Y. S. Lee, "Parallel operation of DC–DC converters with synchronous rectifiers," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'98)*, 1998, pp. 1225–1229.

[22] H. P. Yee and S. Sawahata, "A balanced review of synchronous rectifiers in DC/DC converters," in *Proc. IEEE Appl. Power Electron. Conf. (APEC'99)*, 1999, pp. 582–588.

[23] F. N. K. Poon, J. C. P. Liu, M. H. Pong, and X. F. Xie, "Current driven synchronous rectifier with energy recovery," U.S. Patent 6 134 131, 2001.

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