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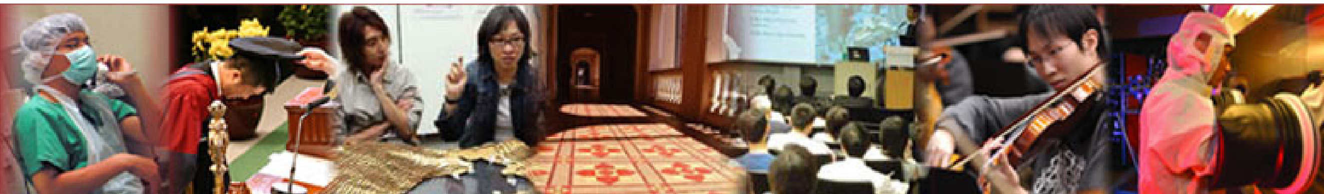

Title	Current transport property of n-GaN/n-6H-SiC heterojunction: Influence of interface states
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HTML ABSTRACT + LINKS

Current transport property of *n*-GaN/*n*-6H–SiC heterojunction: Influence of interface states

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Heterostructures of *n*-GaN/*n*-6H–SiC grown by hydride vapor phase epitaxy (HVPE) and molecular-beam epitaxy (MBE) are characterized with the current–voltage ($I-V$), capacitance–voltage ($C-V$), and deep level transient spectroscopy (DLTS) techniques. Using different contact configurations, the $I-V$ results reveal a rectifying barrier in the *n*-GaN/*n*-6H–SiC heterostructures. When GaN is negatively biased, the current is exponentially proportional to the applied voltage with the built-in barrier being 0.4–1.1 eV for the HVPE samples and 0.5 eV for the MBE sample. DLTS measurements reveal intense band-like deep level states in the interfacial region of the heterostructure, and the Fermi-level pinning by these deep level defects is invoked to account for the interfacial rectifying barrier of the heterostructures. © *2005 American Institute of Physics*.
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GaN/SiC heterostructures have important technological relevance, as SiC is a good substrate for growing GaN-based device structures, such as the high electron-mobility transistors (HEMTs), due to the relatively close lattice match between SiC and GaN and its high thermal conductivity.[1] Dislocations and stacking faults have been identified at the GaN/SiC interface.[2,3] These extended defects are expected to degrade the characteristics of the devices. They may, for example, provide a source of leakage current in GaN-based HEMTs limiting the frequency of operation.[1] In the past, electrical and optical characterizations of GaN-based heterobipolar transistors showed that interface-related deep levels existed in the GaN/SiC $n-p$ heterojunctions.[4–6] However, little is yet known about the electrical properties of $n-n$ GaN/SiC heterojunctions prepared by epitaxial growth of GaN directly on *n*-SiC substrates. In this work, we present an electrical characterization of *n*-GaN/*n*-6H-SiC heterostructures grown by hydride vapor phase epitaxy (HVPE) and molecular-beam epitaxy (MBE) that indicates the existence of a Schottky-like rectification barrier between the thin GaN epifilm and the *n*-6H–SiC substrate.

The GaN/SiC heterostructures were fabricated by growing GaN epilayers directly on the Si-face 6H–SiC substrate using HVPE and MBE. For the HVPE samples, a 500 nm undoped GaN layer was deposited directly (without a buffer layer) on a 2 in. Lely grown, nitrogen-doped 6H–SiC(0001) ($n \approx 1 \times 10^{18}$ cm^{-3}), according to the specification of the supplier, TDI Inc. The wafer was cut into pieces that measured 3×3 mm^2 in size. For the MBE sample, the growth details can be found in Ref. 7. The GaN/SiC samples were rinsed consecutively in boiling acetone, ethanol, and de-ionized water before being chemically treated in HCl/HF acid solution to remove the excess metal or oxidation layer. Ohmic contacts on the SiC side were then fabricated by thermally evaporating Ni dots 2 mm in diameter followed by 700 °C annealing in flowing argon gas, whereas those on the GaN side were made by thermally depositing 2 mm diameter In dots followed by 350 °C annealing in flowing N_2 gas. Current–voltage ($I-V$) and capacitance–voltage ($C-V$) measurements were performed using a HP semiconductor analyzer (4145A) and a capacitance meter (Boonton 72B). Deep level transient spectroscopy (DLTS) measurements were carried out with a reverse bias, V_r, ranging from 0 to -1 V and a forward filling pulse $V_p = 0.5$ V.

The $I-V$ measurements were performed on the GaN/SiC heterostructures using different contact configurations (refer to the inset of Fig. 1). Typical $I-V$ data corresponding to these configurations are given in Fig. 1. The data in Fig. 1(a) suggest that electrical conduction within the GaN and the SiC layers are ohmic. However, for the case of $I-V$ measurements made across the *n*-GaN/*n*-6H–SiC heterojunction, the data of Fig. 1(b) show strong rectification characteristics. Since that the In/GaN and Ni/SiC contacts are ohmic within the same layer, such highly nonlinear

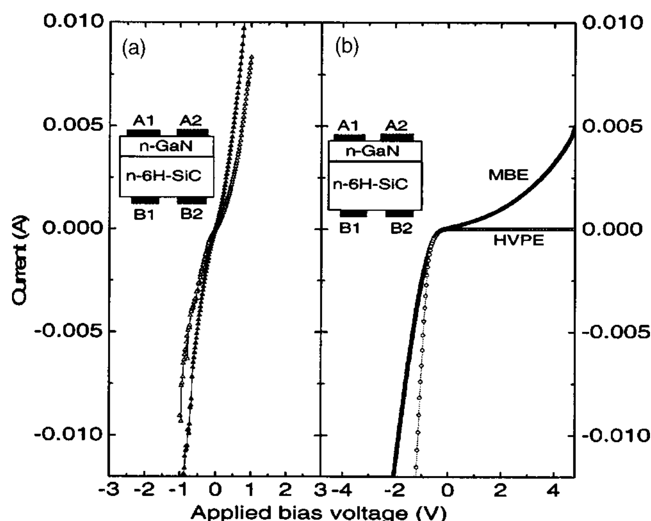

FIG. 1. $I-V$ characteristics for different contact configurations depicted in the inset. (a) $I-V$ curve measured between contact A1 and A2 (▲) and $I-V$ curve measured between contact B1 and B2 (△). (b) $I-V$ curve measured between contact A1 and B1. (○) for HVPE and (●) for MBE grown sample, respectively. During the measurements, the SiC terminal was taken as the voltage reference, and GaN was biased either positively or negatively.

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$I-V$ characteristics must therefore originate from the n-GaN/n-6H–SiC heterojunction.

For the GaN side negatively biased, the obtained $I-V$ curves of Fig. 1(b) are fitted well with an exponential expression $I=I_0 \exp(qV/nkT)$. The barrier height (φ) and ideality factor (n) are found to be 0.67 eV and 1.8, respectively. It is worth noting that for different samples cut from different locations of the same 2 in. HVPE wafer, $I-V$ measurements lead to the extraction of the barrier height varying from 0.4 to 1.1 eV. This variation suggests an inhomogeneous distribution of barriers across the 2 in. wafer. For the MBE sample with a size of 11×3 mm^2, the $I-V$ curves yield a barrier height of $\varphi \approx 0.5$ eV.

To understand the rectifying behavior observed in these $n-n$ GaN/SiC heterojunctions, one first notes that there exists an offset between the conduction bands of GaN and 6H–SiC. Previous studies of n-GaN/p-6H–SiC junctions have given a band offset value of $\Delta E_C = -0.1$ eV for a type II heterojunction.[5,6] On the other hand, $I-V$ and $C-V$ measurements of Schottky barrier heights with different metals such as Au, Pd, and Pt made on n-GaN and n-6H–SiC separately resulted in a value of $\Delta E_C = -0.18-0.45$ eV for the conduction band offset.[8] All of these values are, however, far smaller than the derived 1.1 eV for the barrier height of the heterojunction in this experiment. Therefore, it is unlikely that the observed barrier originates solely from the conduction band offset at the n-GaN/n-6H–SiC heterojunction. Moreover, the observed rectifying behavior of the heterojunction cannot be explained by the Anderson model[9] for $n-n$ semiconductor heterojunctions because of the presence of a high density of dislocations at the heterointerface. The Anderson model, which is valid for materials with less than 1% lattice mismatch, assumes an abrupt semiconductor–semiconductor interface and negligible interface states. For GaN/SiC heterostructures, however, although SiC is more closely lattice matched to GaN than most other substrates, the 3.4% lattice mismatch between the two materials is still quite large and inevitably leads to a high density of misfit dislocations at the heterointerface as revealed by TEM and EBIC experiments.[2,3] In a previous study of n-GaN/n^+-GaAs heterostructures,[10] it was found that the structure behaved like a back-to-back diode or a metal–

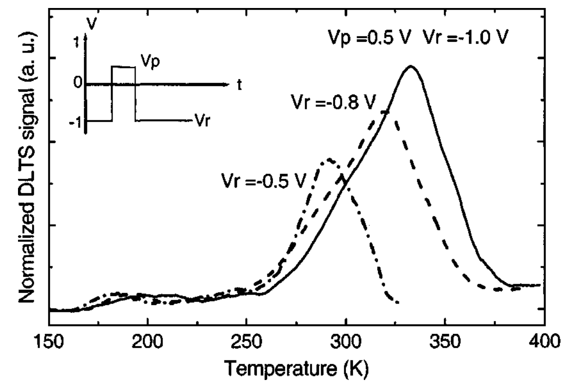

FIG. 2. DLTS spectra of n-GaN/n-6H–SiC heterostructure under various reverse bias conditions. A rate window of 6.82 ms was used in the measurements. The inset shows the filling pulse V_p and reverse bias V_T applied to sample for DLTS measurements.

insulator–semiconductor device depending on the growth condition. This result indicates that defects at the heterointerface are electrically active, which alter the energy band diagram.

To investigate the deep level interface states of the rectifying junctions, DLTS measurements were performed. The resulting spectra under different reverse biases (V_r) and filling pulse amplitudes (V_p) for one of the samples are shown in Fig. 2. For V_p fixed at 0.5 V and varying V_r from -0.5 to -1.0 V, an intense DLTS peak with the peak position dependent upon V_r was observed. The voltage dependence of the peak position indicates a continuum of (band-like) states in the gap.[11,12] Moreover, the DLTS peaks measured under forward filling pulse conditions suggest that the traps are in the interface region. The apparent activation energy of the trap E_T deduced from the Arrhenius plot is 0.4–0.9 eV below the conduction band depending on the applied reverse bias voltage.

From the previous discussion, we believe there are band-like deep level traps in the interfacial region between GaN and SiC. A model in terms of Fermi-level pinning by the band-like states at the heterointerface is thus suggested to explain the observed interface barrier. Figure 3 depicts schematically the band bending under different bias conditions.

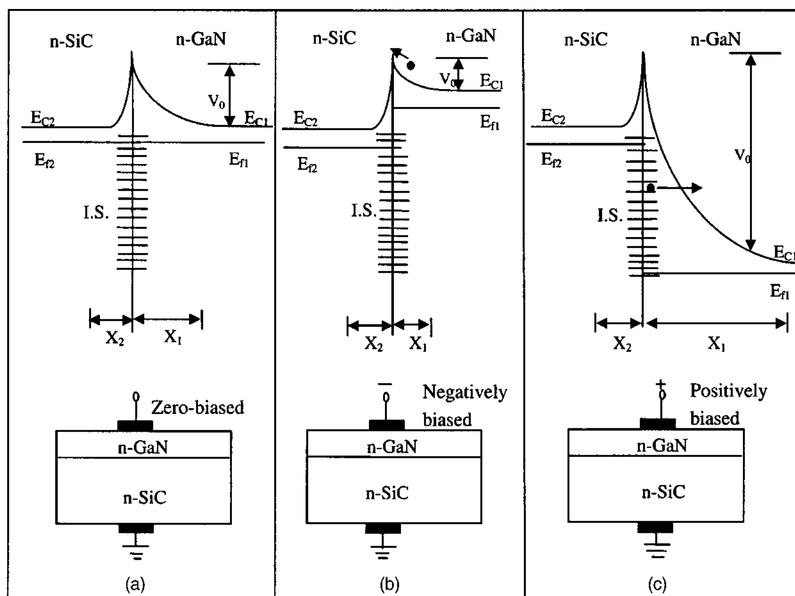

FIG. 3. Schematic energy band diagram of an $n-n$ GaN/SiC heterojunction with the band-like interface states and biased (a) at zero, (b) negatively, and (c) positively.

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The interfacial states are assumed to be negatively charged with a peak density of states located far below the Fermi level.[13–15] The interface potential $\Phi(V,x)$ can then be expressed as a function of the applied voltage V and the distance x from the interface (or the depletion width) according to:

$$\Phi(V,x) = \begin{cases} -(qN_1/2\varepsilon_1)(x-x_1)^2 + V + \Delta, & 0 \leqslant x \leqslant x_1, \\ -(qN_2/2\varepsilon_2)(x+x_2)^2, & -x_2 \leqslant x \leqslant 0, \end{cases} \tag{1}$$

$$x_1 = \sqrt{\frac{2\varepsilon_1[V+\Delta-\Phi(V,0)]}{qN_1}} \tag{2}$$

$$x_2 = \sqrt{\frac{2\varepsilon_2\Phi(V,0)}{qN_2}} \tag{3}$$

where N and ε are the concentration of the ionized space charge and dielectric constant, respectively. The subscript 1 and 2 denote the corresponding parameters for GaN and SiC, respectively. Δ accounts for the differences in work function and electron affinity between GaN and SiC. When GaN is negatively biased [Fig. 3(b)], the potential barrier above E_c of GaN will decrease from $-[\Phi(0,0)-\Delta]$ to $[V-(\Phi(V,0)-\Delta)]$ and the $I-V$ curve will follow an exponential relation $I \sim \exp[V-(\Phi(V,0)-\Delta)]/kT$. When the GaN is positively biased [Fig. 3(c)], electrons from the interface states can tunnel into the GaN by multistep hopping through the depletion region and the unoccupied interface states will be refilled by electrons again via hopping from the SiC side. The $C-V$ measurements carried out on two of the HVPE samples give rise to high densities of the ionized space charge ($6-9 \times 10^{19}$ and $3-5\times 10^{20}$ cm^{-3}). As can be seen from the previous discussion, when the GaN is positively biased, the measured space-charge density will be dominantly the ionized interface traps. Indeed, the carrier concentration of GaN estimated from the resistivity measurements of the control samples with the same growth condition is many orders of magnitude lower than that obtained from the $C-V$ measurement.

As for the origin of the high density, band-like deep level states at the GaN/SiC interface inferred from DLTS measurements, previous experiments by various techniques have already shown that high density of defects (up to $10^{10}-10^{12}$ cm^{-2}) exist in the epitaxial GaN thin films on SiC substrate. For such interfaces, Fermi-level pinning will occur at the dislocation states, which results in carrier depletion in a region around the dislocation. The misfit dislocations lie in the interface of GaN/SiC, and the introduced deep level states deplete free charge carriers in the GaN layer. By solving Poisson's equation determining the radius r_s of the depletion boundary, one may yield an expression for the Fermi-level pinning position as[14]

$$\varphi = qNr_s^2/2\varepsilon[\ln(r_s/r_0) - 0.5] \tag{4}$$

where r_0 denotes the effective radius of the dislocation. Taking the value of the doping concentration n in GaN to be 8×10^{16} cm^{-3}, as estimated from the resistivity measurement, and the effective radius of the dislocation r_0 to be $5-50$ nm,[3,16,17] the calculated pinning position φ is about $0.5-1.2$ eV from GaN conduction band edge. This value compares well with the $n-n$ GaN/SiC interface barrier height derived earlier from the $I-V$ measurements, assuming that the Fermi level is close to the conduction band edge of GaN. Finally, we would like to point out that the defect structure at the GaN/SiC interface is much more complicated than that of a grid of misfit edge dislocations as pictured here. Indeed, besides other extended defects such as stacking faults, grain boundaries, etc., there exists a high density (10^9-10^{10} cm^{-2}) of threading dislocations interacting with the misfit dislocations.[8] How these defects affect the analysis and the electrical parameters of the heterojunction needs further investigation.

In conclusion, GaN films epitaxially grown on n-6H–SiC substrates have been investigated for their electrical properties. A rectifying behavior due to an interface barrier at the n-GaN/n-6H–SiC heterostructure is observed, which is attributed to Fermi-level pinning by interface defects. According to DLTS experiments, there exist band-like deep level states in the GaN energy band gap, which may originate from structural defects at the heterointerface. Using a Fermi-level pinning model, the calculated barrier height compares well with the experimental value.

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