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Deep level defect in Si-implanted GaN n^+-p junction

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A deep level transient spectroscopy (DLTS) study has been performed on a GaN n^+-p junction fabricated by implanting Si into a Mg-doped p-type GaN epilayer. A high concentration of a deep level defect has been revealed within the interfacial region of the junctions by the unusual appearance of a minority peak in the majority carrier DLTS spectra. The deep level defect appears to be an electron trap at E_C-0.59 eV in the p-side region of the junction and has tentatively been attributed to the V_N–Mg complex. The high concentration of this electrically active deep level defect in the depletion layer of the Si-implanted GaN n^+-p junction diodes suggests the need for further investigations. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1578167]

Gallium nitride (GaN)-based devices are of importance for both optoelectronic and electronic applications.[1] Recently, an n^+-p junction was fabricated by implanting Si into Mg-doped p-type GaN followed by 1000 °C annealing in an N_2 ambient.[2] The ion-implantation produced GaN n^+-p junction is particularly useful in lateral GaN-based electronic device fabrication. It is well known, however, that the ion-implantation process introduces deep level defects in GaN, which act as carrier traps and/or recombination–generation centers and which thereby significantly influence device properties.[3,4] Deep level transient spectroscopy (DLTS) has previously been employed to study as-grown GaN films,[5–7] ion-implanted, and electron-irradiated n-type GaN films.[3,8] GaN p-n junctions prepared by epitaxial growth have also been studied using the technique.[9] Electron traps with energy levels at around 0.49 eV, 0.58 eV, and 0.62 eV below the conduction band have been reported on n-type GaN films.[5–7] Hole traps with energy levels at 0.41, 0.49, and 0.59 eV above the valence band have been reported on p-type GaN films.[10,11] In addition, an energy level at $\sim E_C$-0.6 eV has been reported for ion-implanted n-type GaN.[3] In this article, we present a DLTS study on GaN n^+-p junctions fabricated by Si implantation.

The starting material used for the present experiment was Mg-doped GaN metalorganic vapor phase epitaxy grown on a c-face sapphire substrate. The hole concentration and mobility of the GaN film were measured to be 3 $\times 10^{17}$ cm^{-3} and 12 cm^2 V^{-1} s^{-1}, respectively. ^{28}Si$^+$ implantation was carried out with implantation conditions of 3.8×10^{14} cm^{-2}/40 keV, 6.8×10^{14} cm^{-2}/100 keV, and 1.5 $\times 10^{15}$ cm^{-2}/150 keV, to ensure an uniform Si-implanted

layer. After implantation, the samples were capped with another GaN wafer and treated by rapid thermal annealing (RTA) in an N_2 ambient at 1150 °C for 60 s. Hall measurement showed that after the annealing, the implanted film became n type with an electron concentration of 1 $\times 10^{19}$ cm^{-3}, indicating that an n^+-p junction had been formed. The planar GaN n^+-p junction was fabricated by using a lift-off process to define the electrode area. Ti/Al/Ti/Au (30/100/50/100 nm) dots were evaporated onto the Si-implanted area (i.e., the n^+-type region) and Ni/Au rings were evaporated onto the unimplanted p-type region. A RTA in an N_2 ambient with temperature 650 °C was performed to form the electrodes. The planar structures for the Si-implanted GaN n^+-p diodes are illustrated in Fig. 1(a), and the cross section structure of one junction is shown schematically in Fig. 1(b).
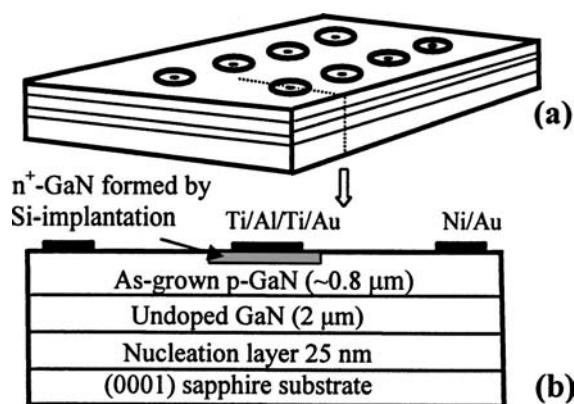

FIG. 1. Schematic diagram of the planar GaN n^+-p diodes fabricated from Si-implantation into p-type Mg-doped GaN epilayer. (a) The multidiode structure on a single wafer. (b) The schematic cross section structure of the Si-implanted GaN n^+-p junction.
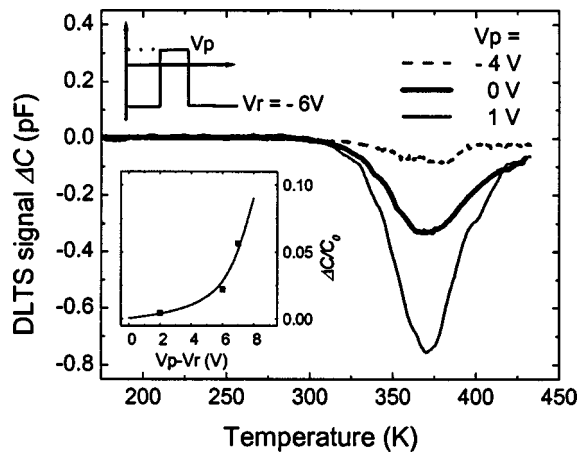
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FIG. 2. DLTS spectra for the GaN n^+-p junction taken at a constant reverse bias $V_r = -6$ V and different amplitude of forward filling pulse $V_p = 1$, 0, and -4 V, respectively. The inset shows the V_p variation of the normalized intensity of the negative-going DLTS peak where the line gives the minority bulk trap model fit.

FIG. 3. DLTS spectra for the GaN n^+-p junction created by Si implantation into Mg-doped GaN as a function of rate window constants. The inset shows the Arrhenius plot for the observed deep level defect.

DLTS measurements were carried out in the temperature range 100–450 K. It should be noted that for the present DLTS system, the DLTS signal (S_p) was defined as $S_p = C(t_2) - C(t_1)$, so that majority give rise to positive-going peaks.[12] Typical DLTS spectra for the GaN n^+-p junction at a constant reverse bias ($V_r = -6$ V) and different forward filling pulse amplitude ($V_p = 1$, 0, and -4 V, respectively) are shown in Fig. 2. Interestingly, a strong negative-going peak at around 360 K is observed with $V_p = 1$ V. Furthermore, the negative peak can clearly be seen at $V_p = 0$ and becomes smaller but still visible at $V_p = -4$ V. Such a peak is unexpected since the Si-implanted layer has been shown to form an n^+ layer. With the diode under reverse bias, the depletion region is mainly in the side of the p-type layer and hole (majority carrier) traps in this layer are expected to give positive-going DLTS peaks. The intensity of the negative peak was found to be similar in all the diodes [as shown in Fig. 1(a)] indicating that the observed deep level defect is a common feature of the Si-implanted GaN n^+-p junctions.

In considering the origin of the negative-going peak in Fig. 2, it should also be noted that surface states could mimic minority (holelike trap) DLTS peaks. Such an effect has been reported for surface state electron traps between gate and source/drain electrodes in n-type GaAs metal semiconductor field-effect transistors.[13–15] Since the switch-on voltage and series resistance of the present Si-implanted n^+-p junction were found to be far larger than those of epitaxially grown n^+-p junctions, it is quite likely that some surface dissociation occurred during high-temperature annealing.[2] Contributions from surface state traps as an explanation for the negative-going peaks should thus be considered. Modeling the effects of such surface states, however, Zhao[14] has shown that the resulting minority peak will decrease rapidly with the initial delay t_1 thus providing an effective way to distinguish surface state related peaks from those arising from real bulk minority carrier traps. Figure 3 shows the DLTS spectra of the GaN n^+-p junction as a function of rate window constant, the initial delays t_1 being 3, 12, 24, and 60 ms with t_2/t_1 set as 4.33 (corresponding rate window constants 6.82, 27.3, 54.6, and 136.4 ms respectively). The intensity of the
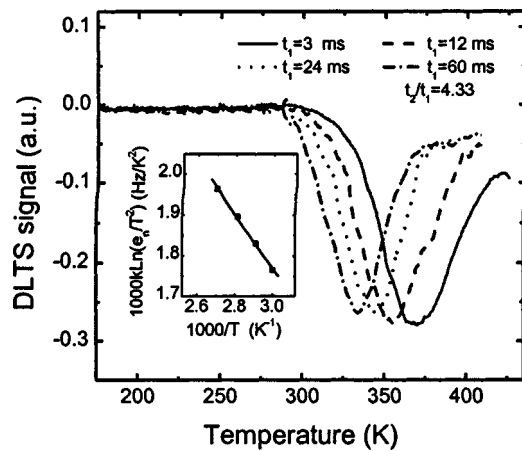
observed negative-going peak is seen to be essentially independent on the initial delay time t_1 as well as the rate window constants used suggesting that the observed negative-going peak is not surface state related. Additional support for this conclusion comes from DLTS measurements made as a function of the filling pulse width t_p where we found the same DLTS peak height for filling pulses of $t_p = 100$ μs and 1 ms (not shown). The observation thus contradicts the surface state model, in which a peak height depending on the filling pulse width is expected.

The most likely explanation of the negative-going DLTS peak is emission from a bulk minority (i.e., electron) carrier trap within the majority carrier side (i.e., the p side for the present case) close to the interface and that traps in this region are being populated by the extended minority carrier trap tail.[12,16] To understand this effect, the band diagram is shown in Fig. 4. As shown the electron Fermi energy E_{fn} intersects the electron trap energy at positions of $\mu(V_r)$ and $\mu(V_p)$ as the diode is, respectively, in reverse and filling pulse bias. During filling pulse, the electron traps in the region between $\mu(V_r)$ and $\mu(V_p)$ are occupied. Switching the diode into reverse bias causes electron emission from the traps within this region, thus producing a decrease in the negative net space charge and giving rise to a negative-
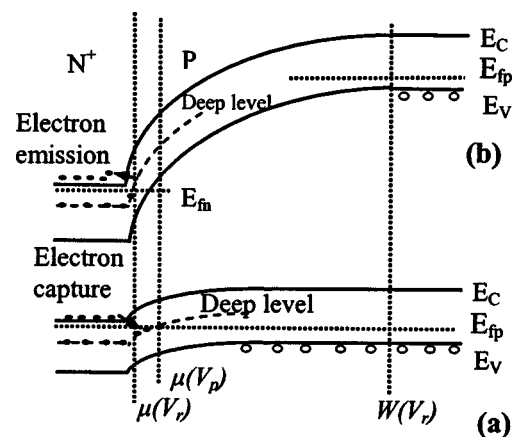

FIG. 4. Band diagram showing electron emission and capture in the interfacial region $\mu(V_r) - \mu(V_p)$ of the Si-implanted GaN n^+-p junction under (a) filling pulse and (b) reverse bias conditions.

going peak in the DLTS spectrum. During the next filling pulse period, electron capture occurs back onto the traps from the electron tail extending from the n^+ side of the junction. Assuming a temperature independent capture cross section of the electron trap, the energy level of the trap E_T can be deduced from the Arrhenius plot, (inset of Fig. 3) to be at E_C-0.59 eV.

The above minority trap model can be further tested by considering the V_p dependence of the DLTS signal shown in the inset of Fig. 2. The amplitude of the negative-going DLTS peak based on this model has been obtained theoretically[16] and when written as a normalized DLTS signal ($\Delta C/C_0$), takes the form:

$$\frac{\Delta C}{C_0} = \frac{N_T}{2N} \frac{[\mu(V_p)^2 - \mu(V_r)^2]}{W(V_r)^2}, \tag{1}$$

where C_0 is the reverse bias junction capacitance, N_T is the deep level concentration, N is the net p-side region hole concentration, and $W(V_r)$ is the width of the depletion region under reverse bias V_r. Moreover, the standard abrupt junction depletion theory gives the width of the free carrier tail region at reverse bias V as

$$\mu(V) = W(V_r)\left[\frac{(V_{bi}-V)^{1/2} - (V_{bi}-E_T-V)^{1/2}}{(V_{bi}-V_r)^{1/2}}\right], \tag{2}$$

where V_{bi} is the built-in potential. The model fit using Eqs. (1) and (2) is shown in the inset of Fig. 2 and is seen to describe the data well. In this fit, N was estimated to be $\sim 5\times 10^{16}$ cm^{-3} from capacitance–voltage measurements on the same junction as used for the DLTS study. Taking V_{bi} as 3.2 eV and C_0 as the measured value of 18 pF, a value of $N_T = 10^{16}$ cm^{-3} is found. The good agreement of the V_p data with theory is strongly supportive of the minority trap model. Moreover if the negative-going DLTS signal were surface state related, it would have a V_p independent value as seen in Ref. 15, since in this case the capacitance transient only depends on the surface current flow which is determined from V_r.

Recent research has shown that a deep level electron trap at E_C-0.62 eV is formed on lightly Mg-doped n-GaN samples, its concentration depending on the biscyclopentadienyl magnesium flow rate during growth of the n-GaN layer, being increased under higher flow conditions.[7] Hierro *et al.*[9] using DLTS reported an electron trap at E_C-0.58 eV on the n-side region close to the epitaxially grown p^+-n junction. Moreover, secondary ion mass spectrometry data clearly indicated that this level was accompanied by a higher concentration of Mg dopant in the n-type region close to the Mg-doped p^+ layer.[9] Furthermore, a study on a Schottky contacted n-type GaN epilayer revealed a 0.62 eV electron trap whose concentration increased with the residual Mg concentration. These authors suggested that this Mg related defect was the complex V_N–Mg.[17]

With the starting material used in the present experiment being Mg-doped p-type GaN, it is not surprising that we also observe a similar deep level electron trap (E_C-0.59 eV) that closely matches the aforementioned Mg related level seen by others.[7,9,17] This assignment would certainly explain the origin of our observed DLTS signal since V_N would be ex-

pected to form through implantation damage. On the other hand, x-ray diffraction spectra have shown that a significant concentration of defects were induced by Si implantation in the n^+ layer of the Si-implanted GaN n^+-p junction.[2] This result is consistent with recent studies on Si- and Ge-implanted GaN which have shown the presence of ion-implantation induced vacancy defects in the implantation region and some of the implantation induced defects appears far behind the implanted layer.[18] The implantation induced defects may act as compensation centers which possibly decrease the net hole concentration to be around the observed value of $\sim 5\times 10^{16}$ cm^{-3} in the depleted p-type region near the interface of the Si-implanted GaN n^+-p junction. This may be one reason why the series resistance of the presently used Si-implanted n^+-p junctions is larger than those of epitaxially grown n^+-p junctions.[2]

In summary, our experiment demonstrates that there exists a dominant deep level defect at E_C-0.59 eV in the vicinity of the Si-implanted GaN n^+-p junction. This deep level has been attributed to an implantation induced defect or complex within the Mg-doped p-type layer which acts as an electron trap in the interfacial region of the Si-implanted GaN n^+-p junction.

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