Improved interface properties of *p*-type 6H–SiC/SiO_2 system by NH_3 pretreatment

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Effects of preoxidation NH_3 treatment on *p*-type 6H–SiC/SiO_2 interface properties were investigated as compared to conventional thermally oxidized devices. It was found that NH_3 treatment before oxidation can reduce the SiC/SiO_2 interface states and fixed oxide charge. Furthermore, less shift of flatband voltage, and smaller increases of effective oxide charge and interface states during high-field stress were observed for the NH_3 pretreated devices. © *2000 American Institute of Physics.* [S0003-6951(00)01803-9]

SiC offers many advantages over Si for high-temperature, high-power, and high-freuqency devices due to its large band gap, high thermal conductivity, and high electron saturation drift velocity. Moreover, one of the most important advantages of SiC over other wide band gap semiconductors is that it can be thermally oxidized to form SiO_2. However, it has been frequently reported that oxides grown on SiC have high interface-state density and a large amount of fixed oxide charges, especially for the SiO_2/p-SiC structure.[1,2] Like silicon processing, an important factor affecting the interface and oxide is the passivation of SiC surface before oxidation. Relevant research has been reported using a H_2 surface cleaning technique[3–5] and high-mobility metal–oxide–semiconductor field effect transistors (MOSFETs) were obtained by this method.[5] Although this technique can form a hydrogen-terminated surface for 6H–SiC, Si–H bonds have a small binding energy ($E_{Si-H}=3.17$ eV),[6] thus degrading device resistance against hot-carrier bombardment. In this work, an alternative surface-passivation technique with NH_3 substituting H_2 is employed to alleviate the above problem, because a nitrogen/hydrogen-terminated surface is probably formed during NH_3 annealing, giving stronger Si–N bonds ($E_{Si-N}\approx 4.6$ eV).[6] As demonstrated by the following experimental results on electrical properties and stress-induced degradation, this passivation step is indeed effective in improving the reliability of *p*-SiC MOS devices.

p-type (0001) Si-face 6H–SiC wafers, manufactured by CREE Research, were used in this study. The SiC wafers had a 5 μm epitaxial layer grown on heavily doped substrates. The doping level of the epitaxial layer was 4×10^{15} cm^{-3}. The wafers were cleaned using the conventional Radio Corporation of America (RCA) method followed by a 60 s dipping in 1% HF, and then loaded into a quartz furnace at 850 °C. After raising to an oxidation temperature of 1100 °C in a N_2 ambient, a 1 h NH_3 treatment on the surface of the wafers was first performed at a flow of 250 ml/min, and then a 380 min oxidation was carried out in a wet ambient by bubbling oxygen through deionized water at 95 °C (denoted as NH3 sample) at a flow rate of 250 ml/min. The control sample without preoxidation NH_3 treatment was also thermally oxidized under exactly the same conditions (denoted as OX). After the oxidation, the two samples were annealed in N_2 at a flow of 250 ml/min at 1100 °C for 1.5 h. Finally, aluminum was thermally evaporated, and then patterned as gate electrode of MOS capacitors (120 μm$\times$150 μm), followed by a forming gas anneal at 410 °C for 30 min. The final oxide thickness, determined from high frequency (hf) accumulation capacitance, was 508 Å. High-field stress (-7.87 MV/cm), with the capacitor biased in accumulation, was used to examine device reliability. The SiO_2/SiC interface properties were characterized by hf (1 MHz) capacitance–voltage ($C-V$) measurements at room temperature under dark condition and after light illumination at deep depletion. The total deep interface states and fixed charges were estimated from a ledge feature occurred on hf $C-V$ curves and flatband voltage shift.[7] All measurements were carried out under a light-tight and electrically shielded condition.

Figure 1 shows the typical hf $C-V$ curves of the two samples under dark conditions, swept in both directions, and no appreciable hysteresis occurs, implying little slow traps. A smaller flatband shift of the NH3 sample than the OX sample indicates reduced positive fixed charges and deep donor-type interface states in NH3 oxide, as further demonstrated below.

Depicted in Fig. 2 are the hf $C-V$ curves of the two samples after light illuminations at deep depletion. A 100 W tungsten lamp was used as the light source,[7] and the capacitors were illuminated for 3 min with a 10 V bias to form an inversion layer. After removing the illumination, $C-V$ curves were recorded first from depletion to accumulation and then from accumulation to depletion. It can be seen that an interface–state ledge[8] appears when sweeping from depletion to accumulation, implying that deep donor-type inter-

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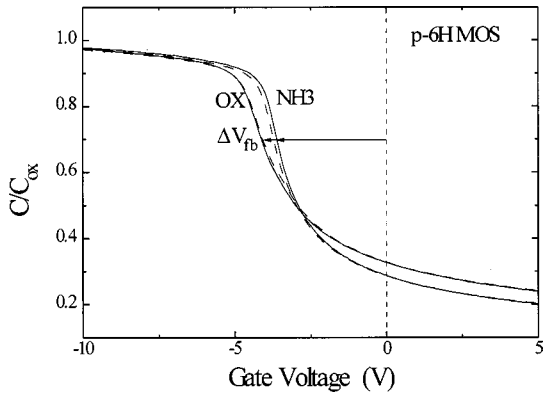

FIG. 1. High-frequency C–V curves of the two kinds of capacitors under dark conditions, swept in two directions: depletion to accumulation (dashed lines) and accumulation to depletion (solid lines). Area of capacitor is 1.8×10^{-4} cm^2.

face states exist at the interface. Moreover, smaller shifts of gate voltage at the ledge and flatband voltage (ΔV_G and $\Delta V_{\rm fb}$) are observed for the NH3 sample than the OX sample. The total deep interface-state density and fixed charge density can be estimated as follows:[7]

$$D_{\rm it}=\frac{C_{\rm OX}|\Delta V_G|}{qAE_g}, \tag{1}$$

$$Q_f=\frac{C_{\rm OX}(|\Delta V_{\rm fb}|-|\Delta V_G|)}{qA}, \tag{2}$$

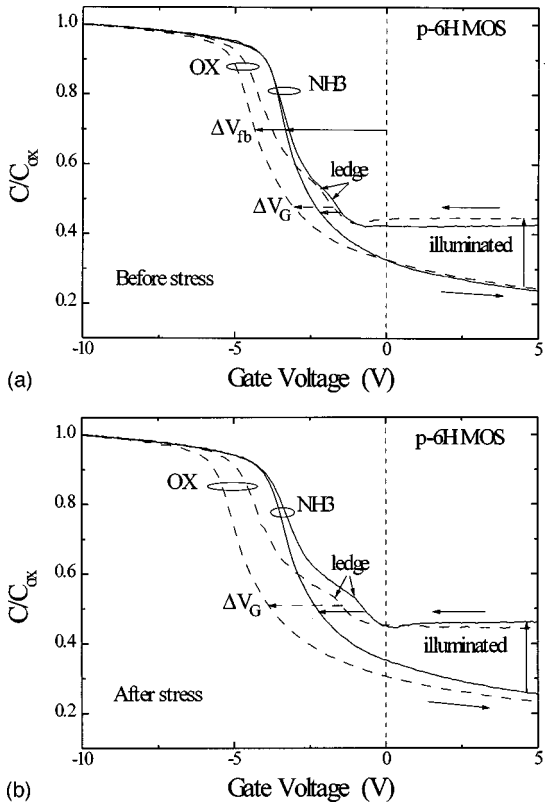

FIG. 2. High-frequency C–V curves of the two samples after light illumination at deep depletion, swept in two directions. (a) Before and (b) after a 5000 s high-field stressing (-7.87 MV/cm) at room temperature. Area of capacitor is 1.8×10^{-4} cm^2.

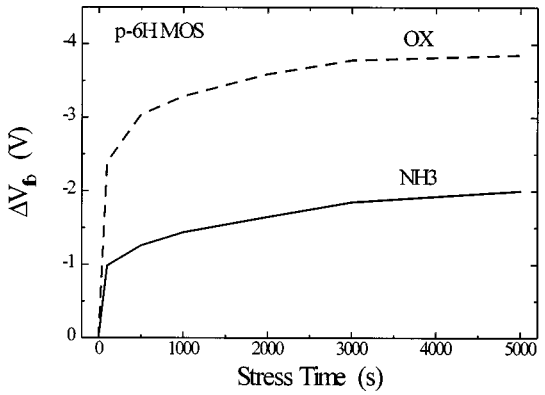

FIG. 3. Flatband voltage shifts of the two samples under high-field stressing (-7.87 MV/cm) at room temperature. Area of capacitor is 1.8×10^{-4} cm^2.

where $C_{\rm OX}$ is the oxide capacitance, q electronic charge, A device area, and E_g energy gap (3.0 eV for 6H–SiC at room temperature).[9] $\Delta V_{\rm fb}$ is determined from the flatband capacitance $C_{\rm fb}$ (Ref. 10) by using 6H–SiC dielectric constant of 9.66:[9]

$$\frac{C_{\rm fb}}{C_{\rm OX}}=\left(1+\frac{150\sqrt{T/300}}{t_{\rm OX}\sqrt{N_A}}\right)^{-1}. \tag{3}$$

Here, $t_{\rm OX}$ is oxide thickness, N_A acceptor doping density, and T temperature (K). In Fig. 2(a), it can be found that $\Delta V_G=1.25$ V and $\Delta V_{\rm fb}=-4.4$ V for the OX sample, and $\Delta V_G=-0.75$ V and $\Delta V_{\rm fb}=-3.3$ V for the NH3 sample. Hence, $D_{\rm it}$ and Q_f are estimated to be 1.74×10^{11} cm^{-2} eV^{-1} and 1.31×10^{12} cm^{-2} for the fresh OX sample, and 1.04×10^{11} cm^{-2} eV^{-1} and 1.06×10^{12} cm^{-2} for the fresh NH3 sample. Smaller $D_{\rm it}$ and Q_f of the NH3 sample should be associated with NH_3-treatment-induced nitrogen-hydrogen-terminated SiC surface, because the initial surface structure is succeeded by the SiO_2/SiC interface even after oxidation.[5] So, it is reasonable to consider the surface passivation as an important issue in improving the interface quality of SiC MOS devices.

Figure 3 shows the flatband voltage shifts of the two samples during high-field stressing (-7.87 MV/cm) at room temperature. Obviously, a much smaller $\Delta V_{\rm fb}$ is obtained for the NH3 sample. The negative $\Delta V_{\rm fb}$ means generations of donor-type interface states and positive oxide charges. From Fig. 2(b) and Eq. (1), it can be found that after stressing for 5000 s. $D_{\rm it}$ increases to 3.33×10^{11} cm^{-2} eV^{-1} for the OX sample and 2.22×10^{11} cm^{-2} eV^{-1} for the NH3 sample, i.e., $\Delta D_{\rm it}=1.59\times10^{11}$ and 1.18×10^{11} cm^{-2} eV^{-1}, respectively. On the other hand, from the maximum $\Delta V_{\rm fb}$ at 5000 s stress time, the increase of effective oxide charge is estimated to be 1.6×10^{12} cm^{-2} for the OX sample and 8.3×10^{11} cm^{-2} for the NH3 sample. Similar to NO-annealed devices,[11] the enhanced resistance of the NH3 device against the high-field stress is likely linked to the formation of strong Si–N bonds during NH_3 treatment. In addition, during the initial 100 s stress time, $\Delta V_{\rm fb}$ should mainly result from pre-existing donor-type interface states and near-interface hole traps, which are both neutral due to electron occupation before stress. From this, it can be deduced that NH3 oxide has much fewer donor-type interface state and oxide traps than OX

oxide. This is consistent with the results in Fig. 2(a). Therefore, it can be suggested that NH_3 treatment before oxidation is significantly conductive to improving *p*-SiC/SiO_2 interface and oxide qualities, probably due to formation of a nitrogen- and hydrogen-terminated and atomically flat surface.

Improved *p*-SiC/SiO_2 interface and oxide qualities were demonstrated in MOS devices with NH_3 pretreatment. Enhanced reliability of the NH_3-treated oxide was also observed under high-field stress. These facts indicate that NH_3 treatment before oxidation is effective in forming a nitrogen/hydrogen-passivated layer on SiC surface, thus reducing the interface states and oxide charge, and enhancing the stability of MOS devices. The reported results here will encourage research on the optimization of surface-passivation conditions for better SiC device properties.

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