

Title	Influence of backsurface argon bombardment on SiO2-Si interface characteristics
Author(s)	Lai, PT; Huang, MQ; Zeng, X; Zeng, SH; Li, GQ
Citation	Applied Physics Letters, 1996, v. 68 n. 19, p. 2687-2689
Issued Date	1996
URL	http://hdl.handle.net/10722/42104
Rights	Applied Physics Letters. Copyright © American Institute of Physics.

Influence of backsurface argon bombardment on SiO₂–Si interface characteristics

P. T. Lai^{a)}

Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong

M. Q. Huang

Department of Applied Physics, South China University of Technology, People's Republic of China

X. Zena

Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong

S. H. Zeng and G. Q. Li

Department of Applied Physics, South China University of Technology, People's Republic of China

(Received 16 January 1996; accepted for publication 27 February 1996)

A low-energy (550 eV) argon-ion beam was used to directly bombard the backsurface of polysilicon-gate metal-oxide-semiconductor (MOS) capacitors after the completion of all conventional processing steps. The interface characteristics of the MOS capacitors were investigated. The results show that, as the bombardment dose increases, the active dopant concentration near the oxide-semiconductor interface gets higher; maximum midgap energy increases; and interface-state density becomes lower. This simple technique is compatible with existing integrated-circuit processing, and can easily improve the interface characteristics, and therefore the electrical characteristics of MOS devices. © *1996 American Institute of Physics*. [S0003-6951(96)00219-7]

The recent and future trends in very-large-scale integration (VLSI) and ultra-large-scale integration (ULSI) are characterized by an ever-increasing exposure of devices to ion and other high-energy particle beams¹ because ion implantation, ion-assisted etching, and deposition are presently essential processing steps. Emerging applications include ion-beam lithography and ion-beam annealing. It has become apparent that these processes introduce lattice-damage layer¹⁻³ and/or electronic trapping centers at SiO₂-Si interface (including positive charge, neutral electron traps, and interface states).⁴⁻⁸ It is well known that the performance and reliability of MOS devices are very sensitive to ionbeam damage, especially in the SiO₂ layer and the SiO₂-Si interface.⁹ Studies of ion beam in the past focused on how it affects the electronic properties of the SiO₂ layer, SiO₂-Si interface, and/or Si surface. This letter, however, investigates the effects of intentional ion-beam bombardment at the back of the devices on these properties.

MOS capacitors $(100 \times 100 \ \mu m^2)$ used in this work were fabricated next to *n*-channel MOS field-effect transistors on 8–10 Ω cm *p*-type (100)-oriented silicon wafers by a conventional four-mask polycrystalline-silicon gate self-aligned MOS process. A 200-Å gate oxide was thermally grown by argon-diluted dry oxidation at 950 °C. A channel implantation with a boron dose of 2×10^{12} cm⁻² at 25 keV was performed. A low-pressure chemical-vapor-deposition (LPCVD) polycrystalline-silicon gate of 400 nm was deposited and doped with phosphorus. The drain and source regions of the transistors were formed by self-aligned arsenic implant and anneal. After completing all these normal processing steps, the wafers were put into a vacuum chamber and a low-energy (550 eV) Ar⁺ beam with 0.5 mA/cm² intensity was applied to directly bombard the backsurface of the wafers at room temperature under a vacuum of 3.2 mPa. Four different bombardment durations 0, 15, 30, and 45 min, were performed. The corresponding bombardment doses are 0, 2.8×10^{18} , 5.6×10^{18} , and 8.4×10^{18} cm⁻², and the samples are denoted as OX0, OX15, OX30, and OX45, respectively. Subsequently, a layer of aluminum was evaporated on the back of the wafer and the devices were then annealed in nitrogen at 450 °C for 20 min.

Bias-temperature C-V measurements were also performed on the capacitors to estimate the mobile-ion level in the gate oxide. After biasing at 4 MV/cm for 15 min at 150 °C, mobile-ion contamination was found to be negligible for the gate oxide. Interface characteristics were determined by high-frequency and quasistatic C-V measurements on the MOS capacitors. All the measurements were carried out in a light proof and electrically shielded probe station.

Figure 1 shows a typical set of high-frequency and quasistatic C-V curves measured at room temperature for the MOS capacitors before and after backsurface Ar^+ beam bombardment. As can be seen from this figure, a displacement of the C-V curve occurs after the bombardment. This shift can be translated to a decrease in the fixed oxide charge density of the MOS capacitors from 5.1×10^{10} cm⁻² (OX0) to 2.4×10^{10} cm⁻² (OX45) as the bombardment proceeds.

The changes of the C-V curve and the parameters for the MOS capacitors have to be related to the change of SiO₂-Si interface characteristics because there is no change in the structure of the MOS capacitors. In order to look into the causes of the change of the SiO₂-Si interface characteristics, the channel dopant profile near the interface was measured and is given in Fig. 2. Two features in Fig. 2 are worth noting. First, the active dopant concentration close to the silicon surface increases by a factor of about 5 after the back-

^{a)}Electronic mail: laip@hkueee.hku.hk



FIG. 2. The active dopant profile near the surface of oxidized silicon: (OX0) before Ar^+ beam bombardment for 45 min; (OX45) after Ar^+ beam bombardment for 45 min.

surface ion bombardment. Second, the channel implant extends slightly deeper into the wafer after the bombardment. For an implant energy of 25 keV and a dose of 2 $\times 10^{12}$ cm⁻² as in our experiments, the projected range R_p of boron ion is 0.084 μ m and the standard deviation ΔR_p is 0.032 μ m.¹⁰ The corresponding average concentration is about 2.5×10¹⁷ cm⁻³. As can be seen from Fig. 2, the average concentration measured from the C-V curve is 1.5 $\times 10^{17}$ cm⁻³ and the depth of the channel implant is 0.082 μ m for the sample OX0. It is obvious that the profiles of the channel implant obtained from calculation and measurement are in good agreement. The increase in dopant concentration near the silicon surface could be due to two factors. First, the backsurface ion bombardment could relieve the stress at the interface, thus activating more dopants. Second, the bombardment could also produce a heating or annealing effect on the channel implant. This annealing may be further supported by the fact that the channel implant is slightly deepened after the bombardment.

Figure 3 shows the midgap energy E_{MG} versus gate voltage V_G of the MOS capacitors before and after the backsurface ion bombardment. The maximum and minimum of the



FIG. 3. The midgap energy E_{MG} vs gate voltage V_G of MOS capacitors after back-surface Ar⁺ bombardment for different times: (OX0) 0 min; (OX15) 15 min; (OX30) 30 min; (OX45) 45 min.

midgap energy get farther apart as the bombardment continues, with their separation increased by about 40% for the sample OX45. The increase of the maximum midgap energy indicates that the Fermi level E_F of the wafer increases due to the increase of active dopant concentration near the silicon surface as shown in Fig. 2.^{9,11}

The interface-state D_{it} of the MOS capacitors before and after the backsurface ion bombardment is given in Fig. 4. It is quite evident that, with an increase of bombardment dose (time), the interface-state density decreases on one hand while the maximum midgap energy increases on the other hand. One possible explanation is that the bombardment could create a lattice-damaged layer at the back of the wafer which then induces some stress at the surface of the wafer, partially compensating the original interface stress created by processing steps. This reduced stress could be translated to higher mobility for the charge carriers in MOS transistors.¹²

In summary, backsurface Ar⁺ bombardment can change the interface characteristics of the MOS capacitor. As bombardment dose increases, surface dopant concentration of silicon wafer increases, maximum midgap energy gets larger,



FIG. 1. High-frequency (HF) and quasistatic (QS) C-V curves of MOS capacitors with Ar⁺-bombardment times of 0 and 45 min.



FIG. 4. The interface-state density D_{ii} of MOS capacitors after back-surface Ar⁺ bombardment for different times: (OX0) 0 min; (OX15) 15 min; (OX30) 30 min; (OX45) 45 min. $E-E_i$ is electron energy relative to the middle of the band gap of silicon.

2688 Appl. Phys. Lett., Vol. 68, No. 19, 6 May 1996 Huang et al. Downloaded¬09¬Nov¬2006¬to¬147.8.21.97.¬Redistribution¬subject¬to¬AIP¬license¬or¬copyright,¬see¬http://apl.aip.org/apl/copyright.jsp and interface-state density decreases. This simple technique which is compatible with existing integrated-circuit processing, can readily improve the performance of MOS devices.¹² It is hoped that by varying the energy, dose, or type of ions, even better results could be obtained.

The authors would like to thank C. L. Chan and H. H. Ng for their technical support in the Microelectronics Laboratory. This work was partially supported by RGC Research Grant, Hong Kong, and the Li Ka Shing Scholarship Foundation, University of Hong Kong, Hong Kong.

¹Y. Wang, T. P. Ma, and R. C. Barker, Appl. Phys. Lett. 54, 2339 (1989).
²P. U. Kenkare and S. A. Lyon, Appl. Phys. Lett. 55, 2328 (1989).

- ³S. W. Pang, D. D. Rathman, D. J. Silversmith, R. W. Mountain, and P. D. DeGraff, J. Appl. Phys. 54, 3272 (1983).
- ⁴P. A. Miller, D. M. Fleetwood, and W. K. Schubert, J. Appl. Phys. **69**, 488 (1991).
- ⁵M. C. Busch, A. Slaoui, P. Siffert, E. Dooryhee, and M. Toulemonde, J. Appl. Phys. **71**, 2596 (1992).
- ⁶R. Singh, S. J. Fonash, P. J. Caplan, and E. H. Poindexter, Appl. Phys. Lett. **43**, 502 (1983).
- ⁷G. J. Dunn, IEEE Electron Device Lett. **EDL-12**, 8 (1991).
- ⁸S. Kar, K. Srikanth, and S. Ashok, Appl. Phys. Lett. 60, 3001 (1992).
- ⁹E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
- ¹⁰H. Ryssel and I. Ruge, *Ion Implantation* (Wiley, New York, 1983).
- ¹¹C. N. Berglund, IEEE Trans. Electron Devices **ED-13**, 701 (1966).
- ¹² P. T. Lai, X. Zeng, G. Q. Li, and W. T. Ng, IEEE Electron Device Lett. EDL-16, 354 (1995).