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Vertical Nanowire Transistors with Low Leakage Current

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A vertical field-effect transistor based on semiconductor nanowires is reported. The fabrication of the device uses a self-supporting flexible nanostructured polymer foil as a template and an electrochemical growth technique for the preparation of the semiconductor. The fabrication process is substantially simpler, and the mechanical robustness is strongly increased as compared to the original device. The channel region of the transistor has a diameter of ~100 nm and a length of ~50 nm. Operation in the hole depletion mode allows a change of the transfer conductance by ~50% when the gate voltages is changed in the range ∓ 1 V. The gate leakage current is ~600 fA per transistor. The overall layout is suitable for optical pixel control on large-area flexible substrates. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1784037]

The fabrication of nanowire transistors has spurred considerable activity in material science, in nanotechnology, and also in the development of novel logic architectures. Nanowire transistors have been explored mostly using the interesting properties of carbon nanotubes. A first working transistor was demonstrated as early as 1998 by Dekker *et al.*[1] using a horizontally arranged wire on SiO_2/Si substrate. In the following years the capabilities of these transistors were extended and memory and circuit applications were proposed and demonstrated.[2,3] With the development of InP and Si nanowires the horizontal device 1ayout was taken over, and quantum effects and transistor action were soon observed in these devices.[4] To take full advantage of the small dimensions of nanowire devices, a vertical orientation is, however, more desirable, since in the vertical geometry packing densities beyond 10^8 cm^{-2} appear feasible. These densities are interesting for optical pixel control, field emission, and other applications. A stacking of several layers of vertical transistors may even lead to higher densities and open applications in information processing, as reconfigurable architectures may tolerate considerable randomness in densely packed structures.[5,6]

A vertical device structure with a packing density of $\sim 10^7$ cm^{-2} has recently been rea1ized,[7] but the fabrication scheme and the observed large gate leakage current, limited the usefulness of this experimental approach. Here we report on a substantially improved device version which can also be fabricated in a simpler process. The new device is more robust and exhibits a strongly reduced gate leakage current. The fabrication involves a sequential deposition of metal, insulator, and semiconductor layers on a nanostructured polymeric template, consisting of a flexible self-supporting polyethylenterephthalat (PET) foil. The PET foil is provided with vertical cylindrical holes of some 100 nm diameter. In the present work the holes are 180 nm in diameter and are obtained by ion track etching. In this process the PET film is first exposed to a beam of fast heavy ions. Subsequently the amorphized ion track regions[8,9] are etched away by use of suitable solvents such as ethanol, acetone, etc. Polymeric materials like kapton, polysterene, PET, and others can be used in this fabrication process. Material-specific additional treatment of the films before and after the ion beam exposure can enhance the etch rate of the damaged material, and nearly cylindrical etch cones can be fabricated, as shown in Fig. 1.[10] In the Ion Beam Lab Berlin a square foot area of polymer films can be irradiated within 1 s with 0.5 GeV Au ions at a density of $10^8 cm^{-2}$.[11] So far only randomly distributed tracks have been generated, but efforts are now under way at several labs worldwide to implement guided beams which allow a precision in the sub-100 nm range.[12]

We have used self-supporting PET films of 8 μm thickness and etch cylinder densities of $\sim 10^7$ cm^{-2} as templates for the vertical transistor arrays. At these densities the transistors operate independently of each other. The arrays had typical areas of 1 cm^2. Vacuum evaporation of a ~70-nm-thick metallic contact layer on the top side of the template foil is used to provide a gate contact [Fig. 2(a)]. Due to the directional character of the evaporation process most of the metal deposition occurs on the flat surface of the template, there is little deposition inside the etch cones. The next step in the fabrication process is the deposition of an insulating film on the metal surface and inside the etch cones. For this a ZnS layer of ~10 nm thickness is deposited using solution deposition and a subsequent chemical reaction

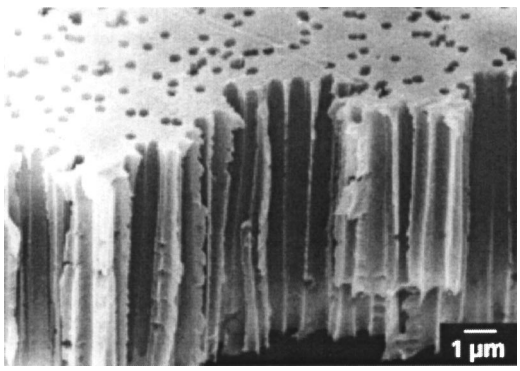

FIG. 1. Scanning electron micrograph of etched ion tracks in PET foil. In the present work the diameter of the tracks is approximately 180 nm, the lateral density was 7×10^7 cm^2.

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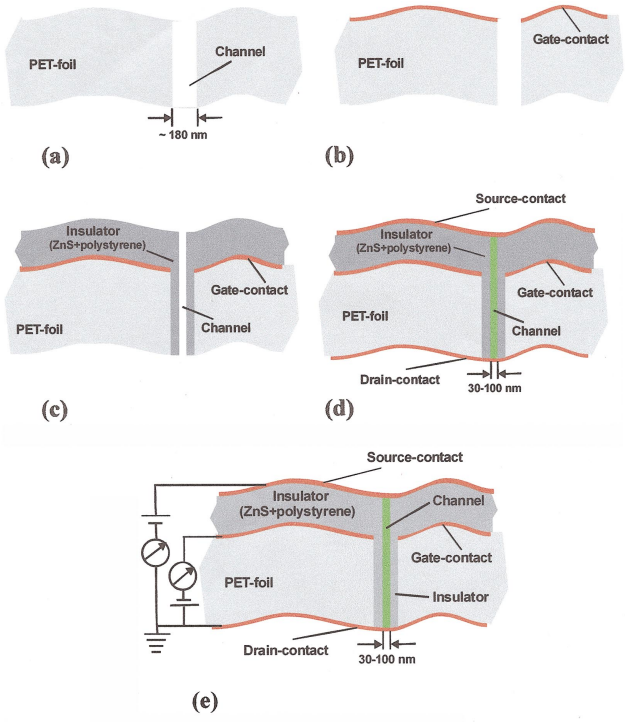

FIG. 2. (Color) Schematic diagram of the vertical nanowire transistor. (a) PET foil with etch cylinder of 180 nm diameter; (b) first metal layer used as a gate electrode; (c) ZnS and polystyrene deposited to cover the metal layer and serving as gate insulator; (d) second metal layer serving as working electrode in electrodeposition and as a source contact in device operation; semiconductor nanowire grown by electrodeposition; final metal layer serving as drain electrode on top of the nanowire; (e) characterization setup.

at moderate temperatures, $T \sim 80\ ^\circ\mathrm{C}$.[13] Then a thin layer of polystyrene is deposited on top of the ZnS layer using vacuum filtration of a polystyrene solution of low molecular weight, as described in more detail in Ref. 14. The function of the thin ZnS layer is to improve the adhesion of the polystyrene layer and to act as a strain relief layer during the shrinking of the polysterene when it dries. The procedure ensures that continuous dense layers are reliably deposited. Typically the insulating coatings have a thickness of 2 μm on top of the metal layer and of a few 10 nm inside the etch holes. In our present design the etch holes have a diameter of $\sim$180 nm after the etching. With a 40-nm-thick insulating layer, the diameter is reduced to $\sim$100 nm, as illustrated in Fig. 2(c). In the next step the bottom side of the structure is coated with a thin Au layer. This Au layer serves as the working electrode for the deposition of the active channel material and as a source contact in the operation of the device. We previously established that electrodeposition affords a convenient and efficient method for the filling of deep nanostructures with compound semiconductors.[15] The deposited material used here is CuSCN, a polycrystalline wide-gap, *p*-type semiconductor with a bulk hole mobility in the range of 20-50 $\mathrm{cm}^2/\mathrm{V\ s}$.[16] The deposition process is carried out in a standard three-electrode electrochemical setup and has been described in detail earlier.[10] By monitoring the deposition current a well-defined amount of material can be grown. In the present case we grew columns with a somewhat larger height than the polymer thickness, as shown in Fig. 2(d). A final vacuum-deposition of a 150 nm Au layer contacting the CuSCN columns on the top side of the arrangement completes the device structure.

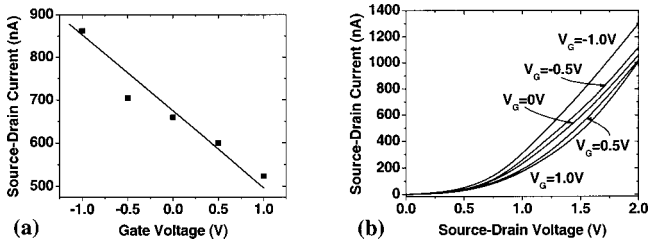

FIG. 3. Electrical characteristic of an array of $\sim$1600 nanowire transistors in polymer foil. (a) Transfer characteristic; the source–drain voltage is 1.6 V. (b) Source–drain characteristics at different gate potentials.

This fabrication procedure produces a highly robust device,[5,12] since the electronically active semiconductor material is completely embedded in the soft polymeric template. The device therefore shows little sensitivity to forces arising from bending, shearing, or stretching the polymer foil. Figure 3 shows the electrical performance of a structure with an area of 0.016 mm^2, comprising approximately 1600 vertical transistors. With positive gate voltages, V_G, the channel volume is progressively depleted of holes, the majority carriers. This results in a decreased transconductance. Upon changing the gate voltage from -1 to $+1$V the conductance is decreases by $\sim$50%. It is expected that a reduction of the channel diameter will result in a stronger current variation, but experimental results have not yet been obtained. Typically the gate leakage current remains well below $\sim$1 nA, i.e., $\sim$600 fA per column, confirming the good insulating properties of the solution-grown polysterene layer.

Our previous transistor design used a stacked arrangement of foils with an intermediate metal layer as a gate contact. In this arrangement the gate layer is located at half height of the etch cylinder and efficient insulation between the channel and the gate layer proved very difficult. Typical gate leakage currents for 1500 transistors amounted to 20–50 nA, at similar operating conditions. In the new device the gate layer is located at the surface of the template and the access for the insulator deposition is improved. Moreover, the two-step deposition results in a very homogeneous coverage of the gate metal. Accordingly the overall leakage current is reduced substantially, with typical values now well below 1 nA. In the previous design the stacking of three films also involved a delicate chemical attachment between the different layers, which limited the structural and thermal stability of the device. The fabrication process for the new device is technically simpler, and results in a markedly improved robustness. The long term stability of the new device will be addressed in the near future.

In the present configuration patterning by masking techniques or by lithography can be applied to all of the three metal contact layers. These patterns could, for example, be used to define optical pixels for flexible display applications.

For other applications it may be desirable to replace the macroscopic contact layers by nanostructures, such as horizontally embedded nanowires. While this step has not been accomplished and is likely to involve experimental challenges, it is noteworthy that theoretical work is beginning to explore the potential for logic processing in arrays with some inherent randomness.[6] This work suggests that statistical fluctuations in the connectivity and contact placement can be accommodated in configurable networks.

In conclusion we have reported the fabrication of a transistor array consisting of vertically, oriented nanowire field-effect transistors. These are deposited on a flexible nanostructured template. In its present form the template is a single self-supporting polymer foil provided with randomly placed vertical etch cylinders with ~100 nm diameter and a packing density of $\sim 10^7$ cm^{-2}. The transistors are operated in the hole depletion mode. At present the conductance variation is ~50% for gate voltages between ∓ 1 V. The leakage current density is typically less than 1 nA for a total of ~1600 transistors. Applications of this device in flexible optical displays appear feasible. Replacement of the source, drain, and gate contacts by horizontal nanowires may eventually open the way to the addressing of single transistors in a three terminal mode. We understand our results as a proof-of-concept that will initiate further research on materials, techniques, and devices on self-supporting flexible films.

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