Topology, Efficiency Analysis and Control of Four-level π-type Converters

By

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Abstract

The main focus of my PhD is to investigate and explore more efficient, reduced switching devices count four-level π-type converter topologies for low voltage applications (V_{dc}<600V). This thesis presents the work on four-level π-type converters during my PhD period. Average analytical mathematical models for analyzing the device power loss and the efficiency of the four-level π-type converter topology have been established. It has been found out that with the same input power level and the same dc input voltage, the four-level π-type converter can provide higher efficiency when switching frequencies are above 5 kHz compared to two-level and three-level converters due to lower switching losses.

In order to resolve dc-link neutral points (NP) voltages unbalancing issues of neutral points clamped (NPC) multilevel converters, a carrier-based modulation (CB-PWM) NPs' voltages balancing control with optimum zero-sequence signals injection for the four-level π-type converter has been investigated. Simulations and 300V dc input voltage experimental results proved that with a back-to-back configuration, the proposed control method is able to balance the three dc-link capacitors' voltages even at high modulation indices and high-power-factor conditions.

For the purpose to make the four-level π-type converter topology work as a single-end converter (inverter or rectifier) with balanced dc-link capacitors' voltages, a modified topology based on the original four-level π-type converter has been developed and analyzed. This new topology is named as the hybrid-clamped four-level π-type converter with one more flying capacitor (FC) as well as two additional switching devices. With such layout modification, more redundant switching states can be generated to regulate neutral path currents. Therefore, the hybrid clamped four-level π-type converter does not have modulation index or power factor limitations when operating as a single-end converter.

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Author's Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and code of Practice for Research Degree Program and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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List of abbreviations

CB-PWM	Carrier-based pulse width modulation
DSP	Digital signal processer
EV	Electric vehicle
FC	Flying capacitor
FPGA	Field programmable logic array
FTT	Fast Fourier Transform
KVL	Kirchhoff’s Voltage Law
NP	Neutral point
NPC	Neutral point clamped
NTV PWM	Nearest three vectors pulse width modulation
p.u.	Per-unit
PI	Proportional-Integral
PS	Phase-shifted
PV	Photovoltaic
SHE-PWM	Selective harmonic elimination pulse width modulation
SVM	Space vector modulation
THD	Total harmonic distortion
VV PWM	Virtual vector pulse width modulation

Contents

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List of symbols

Chapter 2

Symbol	Description	Units
a, b, c	switching energy curve fitting parameters	-
E_{sw_ins}	Switching device switching energy	J
f_{sw}	IGBT switching frequency	Hz
i_c	IGBT switching current	A
i_C	DC-link capacitor current	A
i_{rr}	Diode reverse recovery current	A
J	Energy on the dc-link capacitor	J
P_{con}	Average conduction loss	W
P_{con_ins}	Instantaneous conduction loss	W
P_{on}	Switching device turn-on loss	W
P_{off}	Switching device turn-off loss	W
P_{rr}	Diode reverse recovery loss	W
P_{sw}	Average switching loss	W
P_{sw_ins}	Instantaneous switching loss	W
Q_{rr}	Diode reverse recovery charge	C
t1	IGBT switching current rising time during turn-on transient	s
t2	IGBT switching voltage falling time during turn-on transient	s
t3	IGBT switching voltage rising time during turn-off transient	s
t4	IGBT switching current falling time during turn-off transient	s
trr	Diode reverse recovery time	s
T0-T7	Dwell time for zero vectors V0, V7 and active vectors V1-V6	s
Ts	Switching period	s
V_{base}	Switching device blocking voltage on the datasheet	V
V_α, V_β	alpha-beta variables on alpha-beta frame	V

V_{an} , V_{bn}, V_{cn}	A,B,C phase variables on A, B, C frame	V
V_{dc}	dc-link input voltage	V
V_{ref}	Reference vector for SVM	V
V_{sw}	IGBT blocking or switching voltage	V
α	Vref location angle on the αβ plane	rad
Δv_c	Difference between the ideal dc-link capacitor voltage and the actual dc-link capacitor voltage	V
ΔT	Pre-defined pulse width in power loss simulation model	1/s

Chapter 3

Symbol	**Description**	**Units**
$L_i(t)$	Level function	-
m	Modulation index	-
$T_i(t)$	Modified modulation index	-
$u_i(t)$	Modulation wave	-
V_{dc}	Total dc-link voltage	V
$V_{parasitic}$	Voltage overshoot during switching transient induced by parasitic components in the circuit	V
ω	Fundamental frequency	rad/s

Chapter 4

Symbol	Description	Units
A_0, B_0, C_0	Parameters of relationship between the switching energy and the device current	-
E_{off}	IGBT turn-off energy	J
E_{on}	IGBT turn-on energy	J
E_{rr}	Diode reverse recovery energy	J
E_{sw_ins}	Instantaneous switching energy	J
E_{sw}	Average switching energy over one fundamental cycle	J
f_s	Carrier frequency/switching frequency	Hz
i_c	Device conduction current	A
I_{CM}	Load current peak value	A
k	IGBT conduction duty cycle	-
P_{con_ins}	Instantaneous conduction power loss	W
P_{con_T}	Average IGBT conduction loss	W
P_{con_D}	Average anti-parallel diode conduction loss	W
P_{sw}	Average switching power loss	W
r_{0D}	Diode equivalent turn-on resistance	Ω
r_{0T}	IGBT equivalent turn-on resistance	Ω
T_d	Deadtime	s
T_o	Fundamental period	Hz
T_s	Switching period	s
v_{CE}	Switching device forward conduction voltage	V
v_p	Converter output phase voltage fundamental component	V
V_{base}	Reference switching voltage	V
V_{CE0}	Equivalent IGBT on-state threshold voltage	V
V_{F0}	Equivalent diode on-state threshold voltage	V
V_{GE}	IGBT gate driver voltage	V
V_{sw}	Actual switching voltage	V

ΔV_{d}	Decay on the output voltage	V
φ	Power factor angle	rad
θ_2, θ_1	Integration boundaries	rad

Chapter 5

Symbol	**Description**	**Units**
$c(t)$	Zero-sequence components	-
i_{ai}, i_{bi}, i_{ci}	Inverter three-phase output currents	A
i_{ar}, i_{br}, i_{cr}	Rectifier three-phase ac currents	A
i_{C1}, i_{C2}, i_{C3}	DC-link capacitor currents	A
$\bar{\imath}_{N2\_r}$, $\bar{\imath}_{N1\_r}$	Average rectifier neutral path currents	A
$I_{\mathrm{N1\_i}}$, $i_{\mathrm{N2\_i}}$	Inverter neutral path currents	A
$I_{\mathrm{N1\_r}}$, $i_{\mathrm{N2\_r}}$	Rectifier neutral path currents	A
$\bar{\imath}_{N2\_i}$, $\bar{\imath}_{N1\_i}$	Average inverter neutral path currents	A
I_{i}	Inverter output current peak value	A
I_{r}	Rectifier ac current peak value	A
$K_{\mathrm{aN1\_i}}$, $K_{\mathrm{bN1\_i}}$, $K_{\mathrm{cN1\_i}}$	Duty cycles of inverter three-phase currents contribute to neutral path currents flows through N1	-
$K_{\mathrm{aN2\_i}}$, $K_{\mathrm{bN2\_i}}$, $K_{\mathrm{cN2\_i}}$	Duty cycles of inverter three-phase currents contribute to neutral path currents flows through N2	-
$K_{\mathrm{aN1\_r}}$, $K_{\mathrm{bN1\_r}}$, $K_{\mathrm{cN1\_r}}$	Duty cycles of rectifier three-phase currents contribute to neutral path currents flows through N1	-
$K_{\mathrm{aN2\_r}}$, $K_{\mathrm{bN2\_r}}$, $K_{\mathrm{cN2\_r}}$	Duty cycles of rectifier three-phase currents contribute to neutral path currents flows through N2	-
m_{i}	Inverter modulation index	-
m_{r}	Rectifier modulation index	-
P_{r}, P_{i}	Active power of the rectifier and inverter	W
$u^*_{\max}$, $u^*_{\min}$	Maximum and minimum values of the three-phase sinusoidal fundamental components	-

$u_i(t)$	Modified final modulation waveforms	-
$u_i^*(t)$	Original sinusoidal fundamental waveforms	-
v_{Cj}	Actual measured voltage of the dc-link capacitor	V
V_{rp}, V_{ip}	Peak phase voltages of the rectifier and inverter	V
φ_i	Inverter output power factor angle	rad
φ_r	Rectifier ac-side power factor angle	rad

Chapter 6

Symbol	**Description**	**Units**
C_{fc}	FC capacitance value	F
d	Duty cycle when the current flowing through neutral points	-
d_{fc}	Duty cycle of the switching period that current flows through FC	-
d_{fc_p}	Proportion of the switching period where the current flowing through the flying capacitor causes the maximum FC voltage ripple	-
g_p	coefficient which represents the corresponding value of the unity load current trigonometric function $\sin(\omega_o t+\varphi)$ when the maximum FC voltage ripple occurs	-
I_o	Converter output current	A
k	Values determine which NP the current should flow through	-
V_{tol}	Voltage error tolerance range for the FC voltage	V
V_p	Single-phase output phase voltage	V
ΔV_{fc}	Variation of the FC voltage	V
ΔV_{fc_p}	Peak voltage ripple on FC	V

1 Introduction

1.1 Why multilevel converters and background

Since the invention of semiconductor devices, power electronics has become the core technology in the industry to manipulate the electrical power [1][2][3]. Semiconductor devices make the electronics controllable power supply system available, which is helpful for the automatic control system development in the industry [4]. Meanwhile, with the popularization of the power electronics system, the demand of power electronics in the low-voltage applications market (nominal line voltage up to 690V under the IEC standard, or 575 V under the ANSI standard) [5] includes commercial use area as well as civil use area have increased [6]. These applications include the renewable energy generation such as wind turbines and photovoltaic (PV) energy systems [7][8][9][10], the electric vehicle (EV) drive system [11], electric train traction, more electric ship propulsion systems and more electric aircraft systems[4][8][12]. All these low voltage applications require compact system volume as well as lighter system weight.

All these applications areas require high power density power converter systems. Which means under the same power level requirement, the total converter volume and the system weight are the important factors which should be considered. This creates a challenge for the power electronics system development. Meanwhile, the traditional two-level converter is still the standard industry solution for low-voltage and medium voltage applications. The efficiency of this topology restricted by the high switching losses at high switching frequencies can be deemed as the main drawback of this topology [2][13][14]. However, it has the simple structure and the simple modulation scheme which is still preferred in most industries and companies. Engineers faced in two ways. The first way is to employ or develop semiconductors with high current ratings in order to increase the power rating of traditional two-level converter topologies. Alternatively, advanced SiC and GaN devices with high switching speed are currently under development and can be employed to reduce the switching losses [15][16][17]. Even though, their cost is still very high which will increase the total expense of the whole system. The second way is to use and develop advanced multilevel converter topologies based on conventional low power

rating semiconductors [18][19]. A multilevel converter is able to provide an ac output voltage waveform with multiple steps, synthesize the staircase output voltage waveform in order to follow the sinusoidal modulation waveform [20]. Multilevel converters are normally employed for high voltage applications (>33kV) and medium-voltage applications(3-33kV) [21][22], as they allow working at the high dc-link voltage levels due to the shared voltage drop on each device on the series interconnection of the devices. Therefore, compare to the traditional two-level converter, they provide a series of advantages as follow. 1) Lower output harmonic content [23][24]. The higher output voltage levels, the closer sinusoidal output waveforms. Which means at the same switching frequency, the output harmonic content is less than that of the two-level converter and three-level converters. It can provide a higher power quality at the ac side and reduce the output filter size.

2) Lower voltage stress [22]. With the same dc-link voltage, the higher output voltage level, the lower switching voltage on each switching device. Consequently, device dv/dt is lower. This feature can make the multilevel converter be able to employ lower voltage ratings switching devices with lower price, which can save the total cost of the converter system.

3) Lower switching losses [25][26]. With the same dc-link voltage level, due to the lower switching voltage on switching devices, switching losses can be kept low. The converter efficiency drops less with the switching frequency increasing [27]. Meanwhile, in order to keep the equivalent output harmonics, the switching frequency of the converter can be set as a lower value compares to a two-level or three-level converter. This feature can also reduce switching losses. Both aspects increase the converter output efficiency and shrink the heatsink size.

Therefore, the multilevel converter has the ability to be used in low voltage applications as well.

Even multilevel converters have advantages mentioned above, however, they do possess some drawbacks. For example, each phase-leg will have greater number of switching devices, which will increase the total converter system complexity regarding the circuit configuration as well as the control strategy. And this phenomenon becomes more obvious with output voltage levels increase [28]. Therefore, a multilevel converter topology with reduced complexity but without losing original advantages is required.

Currently, three main types of multilevel converters are generally used in the industry: cascaded H-

bridge converters, flying capacitor (FC) converters and neutral point clamped (NPC) converters [18] [19][29][30]. Among which the NPC converter does not require numbers of FCs or separated dc voltage supplies compares to the other two types multilevel converters. Therefore, the NPC converter can have the smaller total size with the same output voltage levels. It then can be the best candidate among these three types of multilevel converters. According to the derivation principle of reduced-devices-count multilevel converters [18][31][32][33][34], an active NPC four-level π-type converter (in the rest part of this thesis, it will be called as the four-level π-type converter for short) was introduced. This converter topology has only six active switching devices (IGBT or MOSFET) in each phase leg [20][35][36]. Compares to other traditional four-level or even five-level NPC converters, no clamping diodes in the phase-leg configuration. The configuration characteristic shows this topology has less total switching devices count compare to other four-level converters or even higher-level converters, which simplifies the converter configuration, reduces the total conduction loss. Meanwhile, compares to three-level converters as well as two-level converters, it has advantages such as lower switching voltages and lower harmonics. All these make the four-level π-type converter suitable for low-voltage applications. So far, there are no comprehensive topology characteristic and performance analysis as well as control strategy design for this converter topology. Among which, the power loss analysis based on effective converter power loss models require to be developed in order to quantitatively evaluate the loss distribution as well as the efficiency of the π-type converter against the traditional two-level converter and other popular low voltage applications multilevel converters.

One big challenging issue for the four-level π-type converter is to resolve the dc-link capacitors' voltages/neutral point (NP) voltages unbalancing problem as other NPC multilevel converters have [28][37][38][39][40][41][42]. The unbalancing of the dc-link capacitors votlages can cause couple of issues such as the unwanted higher switching votlage, the higher output harmonics, which may affect the system stability and reilability. Among various dc-link NP voltages regulation methods, the active NP voltage control methods based on advanced modulation strategies are still most popular technical approaches, and have been researched in [26][37][38][40][41][42][43][44][45][46] [47][48][49][50][51].

One method is to use control methods based on a virtual vector PWM (VV PWM) [26][47][48][49]. This method can guarantee the dc-link NP voltage balancing with passive front-ends for any voltage

level converters with any power factors and modulation indices. However, the main disadvantage of this method is the switching pattern of each phase-leg within every switching period involves more than two output voltage levels. It consequently increases the total number of switching actions in each switching period, which eventually increases the total switching loss as well as the output harmonics.

Another method is more popular which uses the conventional nearest-three-vectors PWM (NTV PWM) in order to balance the dc-link NP voltage, optimize the switching loss and the total harmonic distortion (THD) at the mean time [28][41][42][46][50][51]. In this case, there are only two voltage levels involved in each switching period and only two switching actions are within each switching period. This NTV PWM based control method can also be realized with a CB-PWM implementation with appropriate zero-sequence signals injection to the original sinusoidal modulation signal for each phase [24][36][40][44][45][52][53][54][55]. Compares to the VV PWM based control method above, the CB-PWM implementation of this method is relatively easy to implement. The main disadvantage of this control method is it cannot guarantee the dc-link capacitor voltage balancing at high modulation indices and high power factors, if only the single-end inverter or rectifier is employed [41][42][46][50][51]. This issue can be resolved with a symmetrical back-to-back configuration [24][36] [40][41][42][46][51].

Experimental verifications on NTV PWM based dc-link NP voltage balance control exist for some other specific topologies. Experimental verifications based on a back-to-back five-level NPC converter by the NTV PWM method have been published in [41][42][46]. [24][40] present the case study based on the method by manipulating power angles on both the rectifier side and the inverter side with offline modulation wave calculation. Therefore, an appropriate analysis and implementation for the dc-link NP voltage balancing control of the four-level π-type converter is required. Appropriate experimental verification for control strategy implementation for the four-level π-type converter is also required.

1.2 Research objectives

The primary target of the research work for this PhD thesis is the theoretical investigation and experimental implementation on a four-level π-type converter under the low voltage condition. As it is designed for low voltage applications such as renewable energy boat, electric aircraft, electric vehicle, or photovoltaic system, therefore, some specifications for the research should be briefly listed.

- The whole system volume should be kept small. As the main space occupying components are the converter ac-side filter, therefore, it should employ small output filter to realize the same output harmonics or employ the same size output filter to realize the smaller output harmonics compares to the two-level and three-level converters under the same input voltage and power condition.
- High and stable efficiency with the change of the switching frequency in order to make the system has higher power density for the applications such as electric car, renewable energy boat, or electric aircraft. Given the small switching voltage on the four-level π-type converter compares to the two-level and three-level converters, it has the less switching loss. System efficiency should be kept high and drops as minimum as possible with the increase of the switching frequency. This feature should be better than that of the two-level converters and three-level converters.
- Appropriate control strategy needs to be developed and implemented in order to eliminate the dc-link NP voltage unbalance issue.

Therefore, according to the system specification, the primary research target can be expanded to several sub-objectives as follows.

- As no cascaded cells are required in the phase-leg layout, meanwhile, over three output voltage levels are still required, therefore, compares to the three-level T-type converter or even two-level converter, the overall NO. of the switching devices of each phase-leg increases. It is required to investigate the structure characteristic of the four-level π-type converter, and compare with the other popular NPC multilevel converters in order to prove its advantage on output filter size selection and switching device selection.
- As for the low voltage applications such as renewable energy boat or electric vehicle, high power density is required. Therefore, it is required to use mathematical method to investigate the power

loss distribution as well as total efficiency to prove its advantage on lower switching losses based on the same power input and load conditions. Relevant experimental works will be needed to prove this investigation.

- As the intrinsic unbalancing issue on the dc-link NP voltages of NPC multilevel converter, investigations on the dc-link NP voltage unbalancing situation of the four-level π-type converter should be investigated. After that, appropriate NP voltage balancing control strategy should be developed and implemented on it. Theoretically or experimentally summarize the control applicable region for the back-to-back four-level π-type converter.
- If possible, try to find the NP voltage balancing solution in order to make the four-level π-type converter be able to work as the single-end converter without the restriction.

1.3 Thesis layout

This thesis is separated into 7 chapters. Except for the chapter 1 introduction part, the remaining 6 chapters in the following cover the key aspects of the work.

Chapter 2

Literature review on the popular NPC multilevel converter topologies, the various sorts of converter power loss analysis methods, and the development review of the dc-link NP voltages balancing control.

Chapter 3

The four-level π-type converter topology configuration introduction. Its phase-leg layout characteristic is presented based on the each switching device selection, modulation scheme introduction, and the voltage rating selection on each switching device. Comparison with the other popular topology which includes two-level converter, three-level diode NPC converter, three-level T-type converter.

Chapter 4

Analytical average power loss models of the four-level π-type converter have been analyzed. Depending on the modulation index, the analytical average loss model on each individual switching device has been separately analyzed. The three-phase converter operation efficiency has been verified by simulations as well as experiments. The efficiency measurement experiments of a traditional two-level converter have been taken in order to provide the intuitive comparison with the four-level π-type converter.

Chapter 5

A NP voltage balancing control method for the four-level π-type converter based on NTV PWM has been analyzed. This control scheme has been implemented with an NTV PWM equivalent level shift CB-PWM with the dynamic optimum zero-sequence signals injections in order to simplify the control algorithm and provide the NP voltage balancing function at the meantime. A back-to-back configuration is used to realize the high modulation index operation when both sides are in the unity power factor conditions. The fully controllable region for the back-to-back system when both sides in the unity power factor has been verified by simulations as well as experiments.

Chapter 6

A hybrid-clamped four-level π-type converter based on the original four-level π-type converter has been proposed. This new topology is able to operate at high modulation index and high power factor conductions as a single-end inverter or rectifier. It improved the operation limit of the original four-level π-type converter. Due to the FC includes in each phase-leg, one important feature of this topology is able to operate with the single phase-leg structure. Simulation and experimental results verified the proposed topology and the control scheme.

Chapter 7

Conclusions based on the work presented in this thesis and recommendations of the additional work which could further develop and improve the ideas proposed and presented in this thesis

2 Literature review

2.1 Multilevel converter topologies review

This section presents main kinds of multilevel converter topologies. Generally, there are three basic kinds of multilevel converter topologies employed in the industry and the commercial areas: NPC converters, FC converters, and cascaded H-bridge converters.

2.1.1 Cascaded H-bridge converter

A cascaded H-bridge converter is based on couples of H-bridge converter cells connected in series with several individual dc voltage sources [30]. Each H-bridge cell in this converter topology is a H-bridge converter which consists of four switching devices, and is supplied by separate dc power supplies. The output voltage level of the H-bridge cascaded converter increases with the increase of the cell number. Due to its highly scalable and modularized features, it is a good candidate for high voltage applications. which is widely used in the industry.

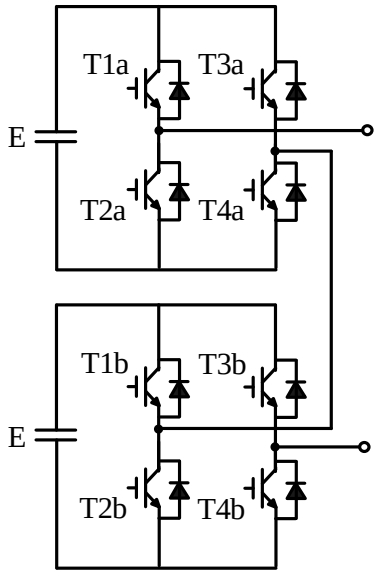


Figure 2.1 Phase-leg structure of a five-level cascaded H-bridge converter

Fig.2.1 presents the phase-leg structure of a five-level cascaded H-bridge inverter [30]. This topology is able to output 5 voltage levels at the ac side. And due to each H-bridge cell is supplied by the individual dc voltage supply with the same voltage value, this kind of cascaded H-bridge converter is

also known as the symmetrical cascaded H-bridge converter [8]. A symmetrical cascaded H-bridge converter is able to produce 2N+1 output voltage level with N H-bridge cells connected in series.

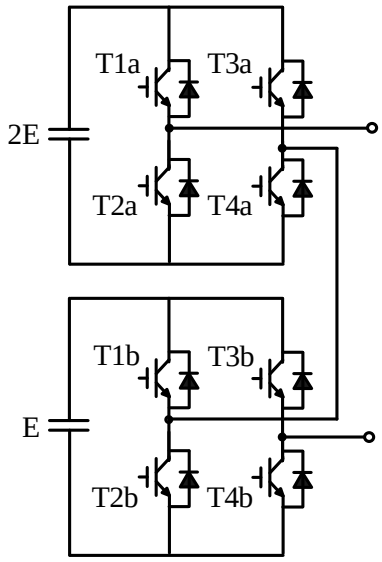


Figure 2.2 Phase-leg structure of the asymmetrical seven-level cascaded H-bridge converters

Fig.2.2 presents an asymmetrical 7-level cascaded H-bridge converter phase-leg configuration [30]. It can be found out that structure is similar to that of the symmetrical 5-level cascaded H-bridge converter as shown in Fig.2.1. The difference is the top H-bridge cell of the asymmetrical 7-level cascaded H-bridge converter is supplied twice the dc voltage than that of the bottom H-bridge cell. With such configuration, the asymmetrical H-bridge converter is able to generate more output voltage levels which is exponential to the H-bridge cells number N. An asymmetrical cascaded H-bridge converter with N H-bridge cells is able to generate $2^{(N+1)} - 1$ output voltage levels with dc voltage supplies varying in multiple of constant 2 like: E, 2E, 4E,… $2^{(N+1)}$E [56]. Meanwhile, due to different H-bridge cells are supplied by different dc voltages, switching devices in different cells have different voltage stress as well as the switching losses.

Consequently, the advantages and disadvantages of the cascaded H-bridge converter can be summarized as follow.

Advantages

- Cascaded H-bridge converter has highly modularity feature due to the repeatability connection of each H-bridge cell. Therefore, the cost as well as the complexity to build any desired voltage level converter are relatively lower than the other multilevel converters which requires

customization such as NPC converters or FC converters. This feature makes it be popular in high voltage and high power industries. And this feature makes it allow easy manufacturing and packaging.

Disadvantages

- As each H-bridge cell requires isolated dc voltage source, therefore, this topology is not suitable for low voltage applications such as EV, more electric aircraft where the converter size and weight are main concerns.

Reliability

- Block voltage rating on switching devices: With the same input voltage level, compare to the two-level converter, the H-bridge cascaded converters with more than three voltage levels at output voltage definitely have less block voltage rating. It means if using the same type of the switching devices, the actual block voltage of the switching devices of the H-bridge cascaded converter is less, which will reduce the risk of overvoltage shoot through due to the parasitic inductance [57][58].
- Fault tolerance: Assume the fault occurs at the specific switching devices. For the H-bridge cascaded converter, if the faulty devices in the system with redundant H-bridge cells standing by, then the redundant cell can take over the faulty cell to maintain the whole system continue working as normal. If the faulty devices in the system without redundant H-bridge cells, and the other cells are still in healthy condition, the whole system will continue the operation but loss the symmetrical operation condition and the total output voltage level will be affected [57]. On the opposite, the two-level converter will immediately shut down if any fault occurs on the switching devices.

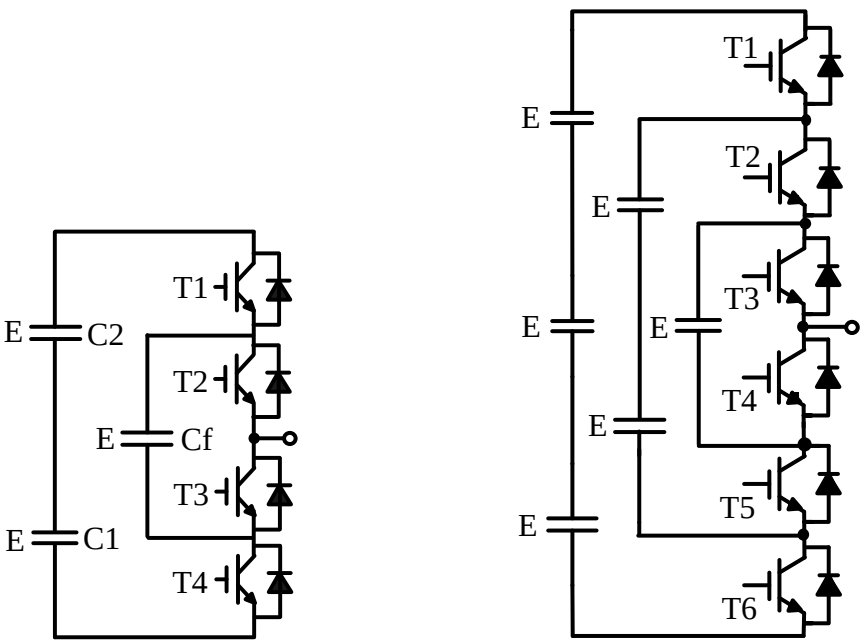
Output harmonics

- Similar to the other multilevel converters, the output harmonic content of the H-bridge cascaded converter is mainly depending on the actual converter voltage levels. If the modulation method is the same, higher the output voltage levels, less the output harmonics. Meanwhile, types of the modulation methods will affect the final output THD [59][60]. Generally, the level-shifted CB-PWM equivalent modulation method will have less output THD compares to the one with the phase-shifted CB-PWM equivalent modulation method [59][60]. Compares to the

traditional two-level converter, if the ac-side filters are the same, the H-bridge cascaded converter definitely shows better output THD [60].

2.1.2 Flying capacitor (FC) converter

The FC converter is first proposed in [61]–[63] by T.A. Meynard. It is a kind of multilevel converter topology using one or several floating capacitors inside the structure to realize the more output voltage levels [64][65][66]. It can be derived from the general converter circuit topology [18][29][31][65] [67][68]. FC multilevel converters can also be deemed as the substitution of the NPC multilevel converters by using FCs to generate more output voltage levels instead of using clamping diode or switching devices as the NPC converters do [69]. Generally, in order to correctly operate the FC converter, FCs voltages have to be well regulated in order to limit the voltage stress on each switching device during each commutation stage [69]. The FC in the phase-leg is generally a fast charging and discharging capacitors and generally within one switching period, its charging and discharging should be kept constant in order to maintain the voltage balance [18].



(a) (b)

Figure 2.3 Phase-leg structures of (a) three-level FC converter (b) four-level FC converter

Fig.2.3 presents phase-leg structures of the three-level FC converter and the four-level FC converter [64][65][66][69]. For the three-level FC converter as shown in Fig.2.3 (a), in order to successfully make

the converter work, the FC voltage has to be well maintained at ½ of the total dc-link voltage. Table II.I shows switching states and their corresponding output voltage levels for the three-level FC converter. It can be found out that if output voltage equals to E, there are two different available switching states. These two switching states which produce the same output voltage levels are called redundant switching states [62] [67]. For the three-level FC converter, these two redundant switching states provide the possibility to control the FC voltage. This feature makes FC converters have the ability to operate as the single-phase configuration.

TABLE II.I. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE THREE-LEVEL FC CONVERTER

Device / Voltage-level	T1	T2	T3	T4
2E	ON	ON	OFF	OFF
E	ON	OFF	ON	OFF
E	OFF	ON	OFF	ON
0	OFF	OFF	ON	ON

For the four-level FC converter as shown in Fig.2.3 (b), in order to successfully make the converter work, two FCs voltages have to be well controlled at 2/3 and 1/3 of the total dc-link voltage, respectively. Table II.II shows switching states and their corresponding output voltage levels for the four-level FC converter. It can be found out for inner output voltage levels 2E and E, there are three redundant switching states for each of them.

Therefore, with the increase level of the FC converter, more redundant switching states are existing for inner output voltage levels. And they improve the FC voltage control ability. However, the higher the voltage level, the more number of the FCs, which will increase the converter size significantly.

TABLE II.II. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE FOUR-LEVEL FC CONVERTER

Device / Voltage-level	T1	T2	T3	T4	T5	T6
3E	ON	ON	ON	OFF	OFF	OFF
2E	OFF	ON	ON	ON	OFF	OFF
2E	ON	OFF	ON	OFF	ON	OFF
2E	ON	ON	OFF	OFF	OFF	ON
E	OFF	OFF	ON	ON	ON	OFF
E	ON	OFF	OFF	OFF	ON	ON
E	OFF	ON	OFF	ON	OFF	ON
0	OFF	OFF	OFF	ON	ON	ON

Therefore, the advantages and drawback of the FC converter can be summarized as follow.

Advantages:

- No NPs in the dc-link, therefore, no dc-link NP voltage drift problem. It prevents the additional complex dc-link capacitor voltage balancing solution requirement.
- Compares to the cascaded H-bridge converter, there is only one dc-link bus. Therefore, only one dc voltage supply is required. Hence, it reduces the total system cost and size.
- More redundant switching states for inner voltage levels, which provide more choices for FC voltages control.
- Single-phase operation ability.

Disadvantages

- Except for the dc-link capacitor, additional FCs are required in order to generate desired voltage level. The required number of the additional FC increases with the output voltage increases. It increases the total system size and cost.
- Each FC requires the individual voltage sensor in order to monitor and feedback the correct signal to the control loop. With the increase of the output voltage levels, the cost of the extra voltage sensors will be dominant.

- Appropriate initial FC voltage charging up solution has to be provided in order to reduce the converter system start up shock. It will increase the whole system complexity to some extent.
- Different types of FC converters require the different circuit design. Therefore, the FC converter lacks of the modularity feature with respect to the industry applications.

Reliability

- Block voltage rating on switching devices: With the same input voltage level, compare to the two-level converters, the FC converters with more than two voltage levels at output voltage definitely have less block voltage rating. It is similar to the other multilevel converters, if using the same type of the switching devices, the actual block voltage of the switching devices of the FC converter is less, which will reduce the risk of overvoltage shoot through due to the parasitic inductance in the circuit [58].
- Fault tolerance: Assume the fault occurs at the specific switching devices. For the FC converter, if the faulty devices occur in the system, and the other switching devices are still in healthy condition, the whole system will continue the operation but loss the symmetrical operation condition and the total output voltage level will be affected [58]. Apart from that, the advanced protection control system can also adjust the FC voltage level in order to recover the system to the normal operation condition [70]. On the opposite, the two-level converter will immediately shut down if any fault occurs on the switching devices.

Output harmonics

- Similar to the other multilevel converters such as the H-bridge cascaded converter, the output THD of the FC converter is mainly depending on the actual converter voltage levels. And if the modulation method is the same, higher the output voltage levels, less the output harmonics. Meanwhile, types of the modulation method will affect the final output THD [71]. Generally, the level-shifted CB-PWM equivalent modulation method will have less output THD compares to the one with the phase-shifted CB-PWM equivalent modulation method [71]. Compares to the traditional two-level converter, if the ac-side filters are the same, the FC converter definitely shows better output THD [60].

2.1.3 Neutral point clamped (NPC) converter

Compares to the FC converter, the NPC converter uses neutral paths by switching devices to generate more output voltage levels rather than FCs. As indicated in the name, the dc-link of the NPC converter has been split into several sections by NPs. Each neural point connects to the converter phase-leg output by using one or several switching devices [1], [30], [72]–[74][75]. The concept of the n-level NPC converter is shown in Fig.2.4. With such structure, the converter is able to generate multilevel output voltages. If n-level output phase voltage is required, there are n-2 NPs at the dc-link. And for multiphase converter, all phases share the same dc-link neural points.

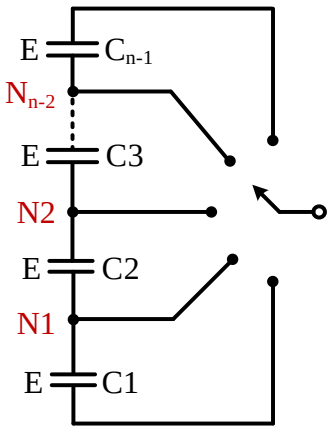


Figure 2.4 Concept of the n-level NPC converter

NPC converters can generate the multiple voltage levels at the ac side passively through a set of series-connected capacitors. Generally, there is no cascaded cells in the phase-leg, which makes its structure more simplicity compares to the cascaded H-bridge converter. Meanwhile, there are no connected FCs in the phase-leg, which makes its volume more smaller compares to the FC converter [32], [72].

Fig.2.5 shows the phase-leg of a three-level diode NPC converter [76], which is introduced by A. Nabae, I. Takahashi and H. Akagi in 1981. The output of phase-leg and the dc-link NP is connected through two neutral paths by D5 and D6. The corresponding switching states and output voltage levels for the three-level diode NPC converter is summarized in Table II.III. Unlike the two redundant switching states at output voltage E for the three-level FC converter as shown in Table II.I, there is only one switching state when the ac-side voltage level equals to E for the three-level diode NPC converter. Which means for the three-level diode NPC converter, there is no other redundant switching state

available for the output voltage level E. Therefore, the available option of the switching state to adjust the dc-link NP voltage is limited [77]. Appropriate active dc-link NP voltage control method is required otherwise the unbalanced or large fluctuated dc-link NP voltages may apply excessively large voltage on switching devices, and in consequence a failure may occur.

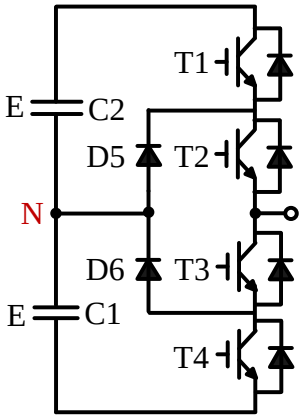


Figure 2.5 Three-level diode NPC converter

TABLE II.III. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE THREE-LEVEL DIODE NPC CONVERTER

Device / Voltage-level	T1	T2	T3	T4
2E	ON	ON	OFF	OFF
E	OFF	ON	ON	OFF
0	OFF	OFF	ON	ON

Therefore, the advantages and disadvantages of the NPC converter are summarized as follow.

Advantages:

- Compares to cascaded H-bridge converter, there is only one dc-link bus, which will only require single dc voltage supply, which reduce the total converter cost and volume.
- Compares to the FC converter, there is no additional capacitors in the phase-leg. This significantly reduce the total converter volume and cost as well.
- Suitable for low voltage applications due to the relatively simple and low volume phase-leg structure compares to FC converters and cascaded H-bridge converters.

Disadvantages

- Due to the NPs exist in the dc-link, the neutral path current flows through NPs during operation will cause the dc-link NP voltage drift issue. Therefore, additional dc-link NP voltage balancing control solution has to be provided. It increases the whole system complexity.
- Different NPC converter topologies require the specific customized circuit design. Therefore, it still lacks of the modular-build ability for the industry.

Reliability

- Block voltage rating on switching devices: With the same input voltage level, compare to the two-level converters, the NPC converters with more than three voltage levels at output voltage will have less block voltage rating if there are more than one switching device in series in each conduction path. If there is only one switching device in some of the commutation path such as the three-level T-type converter, this switching device will have less transient switching voltage but the same steady state block voltage compares to the two-level converter [70][78]. It means if using the same type of the switching devices, the actual block voltage rating of the switching devices of the NPC converter is less, which will reduce the risk of overvoltage shoot through during the switching action due to the parasitic inductance.
- Fault tolerance: Assume the fault occurs at the specific switching devices. For the NPC converter, If the faulty devices occur in the system, and the other switching devices are still in healthy condition, the whole system will continue the operation but loss the symmetrical operation condition and the total output voltage level will be affected [79][80][81]. On the opposite, the two-level converter will immediately shut down if any fault occurs on the switching devices.

Output harmonics

- Similar to the FC converter and the H-bridge cascaded converter, the output harmonic content of the NPC converter is mainly depending on the actual converter voltage levels. If the modulation method is the same, higher the output voltage levels, less the output harmonics. However, unlike the FC converter and the H-bridge cascaded converter, the NPC converter is not generally used for very high output voltage levels (>10) due to the complexity of the control requirement [82]. Meanwhile, types of the modulation method will affect the final output THD. Generally, the level-shifted CB-PWM equivalent modulation method will have less output THD

compares to the one with the phase-shifted CB-PWM equivalent modulation method [83][84]. And this will be a brief explanation in section 2.4.2.3. Compares to the traditional two-level converter, if the ac-side filters are the same, the H-bridge cascaded converter definitely shows better output THD compares to the one of the two-level converter [60]. FFT analysis on different NPC converters as well as the two-level converter will be presented in section 3.4.2.

2.1.4 Generalized multilevel converter topologies

Table II.IV shows the basic comparison of various aspects of different multilevel topologies discussed above, and take the five-level condition for example. It can be observed that for obtaining the same number of levels of voltage at the output, different topologies need different number of sources, diodes, capacitors etc. Suitability of topology is mostly application oriented. For low applications, as the passive components such as FCs and dc voltage supplies are the elements which will increase system size, therefore, the NPC converter is the most compact among these three kinds topologies.

TABLE II.IV. COMPARISON BETWEEN VARIOUS FIVE-LEVEL MULTILEVEL CONVERTERS

Topology / Parameters	Cascaded H-bridge converter	FC converter	Diode NPC converter
Voltage levels	5	5	5
NO. of switching devices	8	8	8
NO. of clamping diodes	0	0	6
NO. of FCs	0	3	0
NO. of dc voltage sources	2	1	1

Such like the above mentioned topologies, more topologies of multilevel inverters can be developed according to generalized topologies [18]. The first generalized topology was claimed by F. Z. Peng claims in 2001 [29]. This generalized topology uses the basic cell consists of two switching devise and one capacitor connect layer by layer as shown in Fig.2.6. This generalized topology is called generalized topology I [18]. Many other topologies can be derived from this topology.

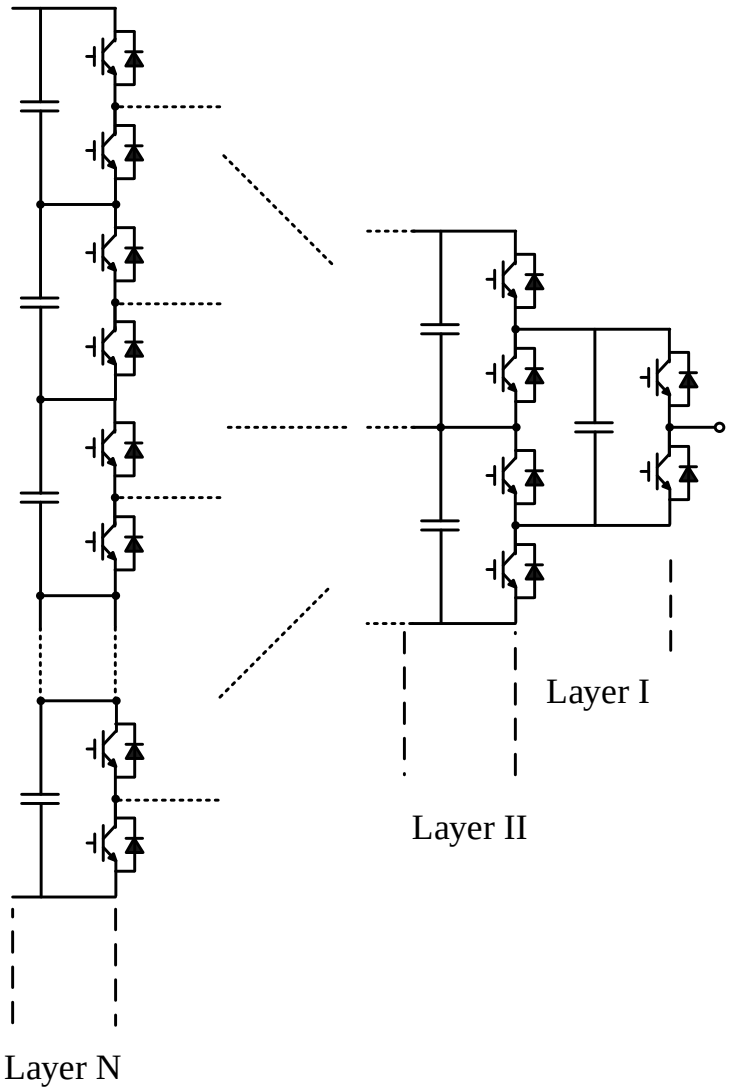


Figure 2.6 Generalized topology I

For example, Fig.2.7. shows the diagram of transfer from two-layer generalized topology I into the active three-level NPC converter and the three-level FC converter. By getting rid of the capacitor C1a in layer I, the active three-level NPC converter can be created. If further replace T2b and T3b with diodes, three-level diode NPC converter can be created. By getting rid of T2b and T3b in the two-layer generalized topology I, the three-level FC converter can be created.

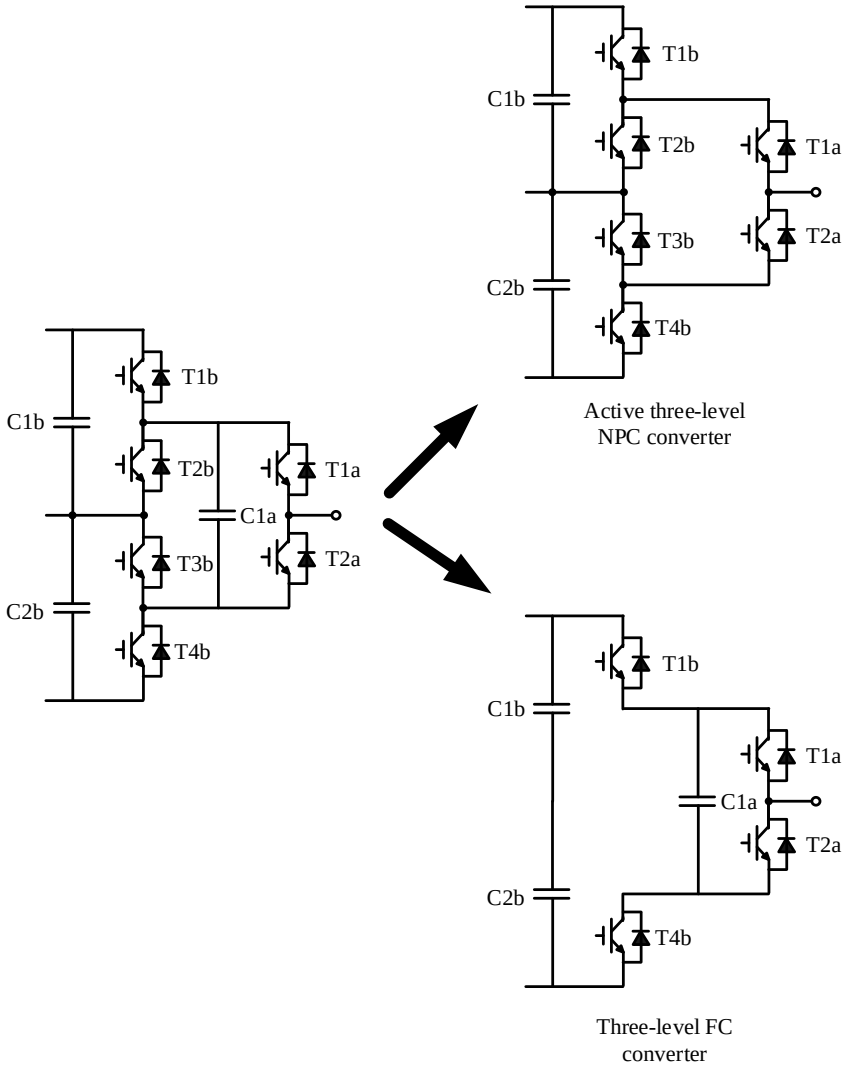


Figure 2.7 Transfer generalized topology I to the active three-level NPC converter and the three-level FC converter

The second generalized topology is proposed by P.M.Bhagwat in 1983 [31]. Fig.2.8 presents the phase-leg structure of the generalized topology II. This topology uses numbers of bidirectional neutral paths to divide the dc-link into numbers of sections. For a n-level generalized topology II, there are n-2 NPs in the dc-link side. The popular three-level T-type converter [33]–[37][90] and the four-level π-type converter [20][35][36] analyzed in this thesis are both derived from generalized topology II.

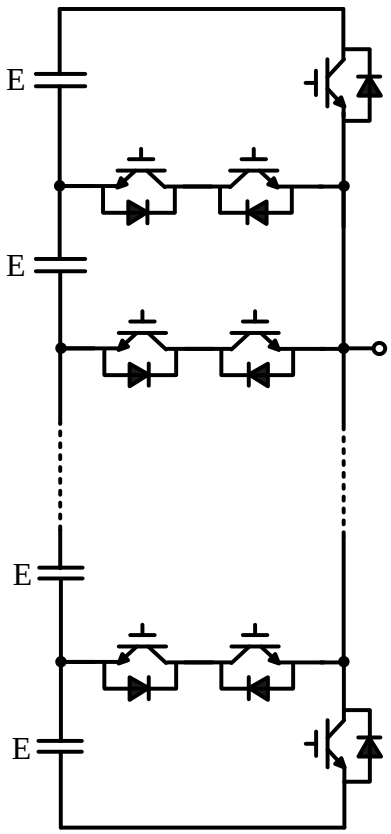


Figure 2.8 Generalized topology II

2.1.5 Discussion about different applications of topologies with their designs

For the cascaded H-bridge converter, according to the introduction in 2.1.1, it is of the highly modularity feature. This feature will make it a good choice for the high voltage industries especially the areas require a customized voltage and power levels such as mine industries and high voltage power transmission industries. Engineers could connect the H-bridge cells in series in order to fulfil the different voltage level demands. Therefore, the system volume is not the main concern for the design. For this purpose, the main design of the cascaded H-bridge converters should focus on the following directions

- System reliability which including the switching device over voltage and over current protection, devices status live time monitoring.
- Makes it easy to adjust the total H-bridge cells numbers of the system in order to fulfil the application power or voltage requirements.
- The cooling system layout should be carefully considered. It is the key aspect for the multiple

H-bridge cells modular configuration design, for example: each H-bridge cell contains the independent cooling system or multiple H-bridge cells share the external common cooling system. Therefore, switching devices power loss analysis should be conducted in order to find the appropriate cooling system design.

For the FC converter, as mentioned in 2.1.2, FC converters only require one dc-link power supply for multilevel voltage output requirement compares to cascaded H-bridge converters which require multiple independent dc power supplies for dc-ac conversions. Meanwhile, FC converters do not have dc-link clamping points, which means they do not have dc-link voltage balancing problem compare to NPC converters. Therefore, FC converters can be a good candidate for middle or low voltage level multi-phase applications such as renewable energy generation, electric traction/vehicle. Meanwhile, due to the single-phase operation ability, it can also be a good candidate for single-phase ac motor drivers such as drills driver, compressors driver, centrifugal pump driver, etc.

Therefore, the main design of the FC converters should focus on the following directions.

- System reliability which including the FC overvoltage and large voltage ripple protection. Relevant FC voltage sensors as well as appropriate FC voltage controllers have to be well designed.
- FC volume and size should be carefully considered in order to find the compromise between the whole system size and the capacitor voltage ripple level.
- Switching devices power loss analysis should be conducted in order to find the appropriate cooling system which is also relevant to the whole system volume.

For the NPC converter, as mentioned in 2.1.3, NPC converters only require one dc-link power supply for multilevel voltage output requirement such as that for FC converter, which is the adventure compares to cascaded H-bridge converters. Meanwhile, due to there are no FCs in the NPC converter layout, which makes it more compact compares to the FC converter. Therefore, apart from the general electric traction and renewable energy generation applications, NPC converters can also be a good candidate for middle or low voltage level applications where the whole system volume and weight requirements are a big consideration. These applications include unmanned aerial vehicles, electric passenger transport, and renewable energy boat, etc.

Therefore, the main design of the NPC converters should focus on the following directions.

- DC-link NP voltage balancing controller design. As in order to realize the full operation with only one dc power supply for dc-ac applications, its intrinsic dc-link NP voltage drift problem should be resolved before hand.
- Switching devices power loss analysis should be conducted in order to find the appropriate cooling system which is also relevant to the whole system volume.

2.2 Popular NPC multilevel converters

As introduced in section 2.1, the NPC multilevel converter does not require additional FC or separated dc voltage supply, which reduces the total system volume. This feature makes it suitable for low voltage applications. In this section, four existing NPC converter topologies in the industry has been introduced.

2.2.1 Three-level diode NPC converter

The three-level diode NPC converter is first proposed by A. Nabae, I. Takahashi and H. Akagi in 1981 in [76]. The dc-link capacitor is split into two by one neutral path in order to get the three voltage levels at the output phase voltage.

Three-level diode NPC converters have been widely employed in high-power medium-voltage (MV) applications [5][21][91][92][93][94][95][96]. However, due to its relatively compact structure compares the cascaded H-bridge converter and the FC converter, it is also widely used in the low-voltage application area. For example, with a 600V dc input voltage, the three-level diode NPC converter build with 600V IGBTs has shown a lower total power loss than the two-level converter build with 1200V IGBTs when the switching frequency is higher than 10 kHz [5]. The reason of this is that in the low switching frequency domain (<10 kHz) the conduction loss contributes for the dominant. While in the high switching frequency domain (>10 kHz), the switching loss contributes for the dominant. Therefore, the increased conduction loss caused by the higher number of series connected switching devices in the phase-leg has been overcompensated by the reduced switching loss of the relatively lower switching voltage [97].

For a three-level diode NPC converter as shown in Fig.2.9, there are four switching devices plus two clamping diodes in each phase-leg. And the four switching devices in each phase-leg require four individual gate driver supplies, which is double the number of the two-level converter. The output of this topology is connected to the dc-link capacitor NP (mid-point) via diodes to provide the third level at the output voltage as shown in Fig.2.10. The current is drawn from the NP upon the output is connected to the NP. And as NP does not directly connect to the dc voltage supply, the current is drawn through the dc-link NP, causing one charge whilst the other one discharge.

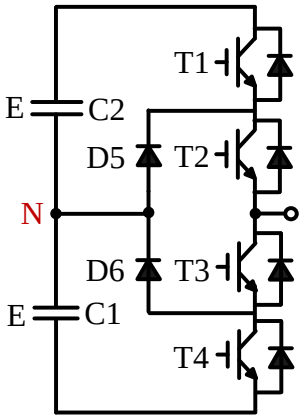


Figure 2.9 Phase-leg structure of the three-level diode NPC converter

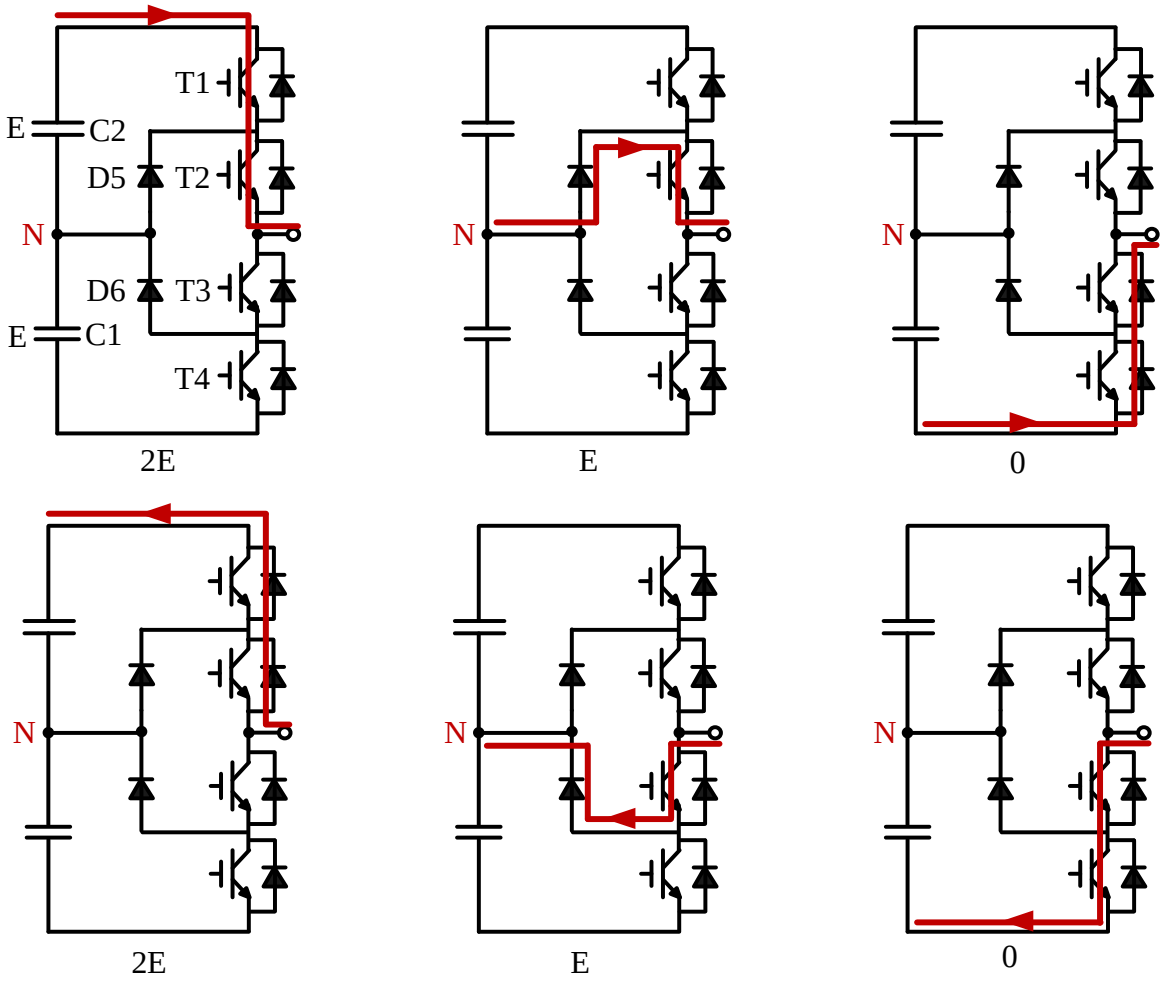


Figure 2.10 Switching states and current flow paths of the three-level diode NPC converter

Table II.V presents the switching state truth table with respect to the switching states as shown in Fig.2.10.

TABLE II.V. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE THREE-LEVEL NPC CONVERTER

Device / Voltage-level	T1	T2	T3	T4
2E	ON	OFF	ON	OFF
E	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON

Under the normal operation condition, the mean current drawn from the NP over one fundamental period is zero and the NP potential remains constant from the point of view of fundamental period. This feature can be deemed as the three-level diode NPC converter is fundamentally NP voltage balanced.

However, if the system is open loop, from the point of view of each switching period, non-zero neutral currents always exist and can not be regulated within each switching period, therefore, cause the low frequency voltage ripple at the NP [98]. If such low frequency voltage ripples are not well eliminated, higher voltage will be applied on the switching device which may cause the system unstable. Many publications have introduced control and modulation schemes to reduce or eliminate this low frequency voltage ripple in the NP [71][86]–[88][92], [102], which will be introduced in section 2.4.

Therefore, the main advantage of the three-level diode NPC converter can be presented as follows.

- Each switching device of the three-level diode NPC converter only has to withstand half of the whole dc-link voltage. Compare to the two-level converter, this feature effectively reduces the blocking voltage level for a given power switching device [92].
- Relative lower converter ac-side voltage harmonics compares with the two-level converter. The first group of the output voltage harmonics component in the harmonic spectrum is centered around twice the switching frequency [76][103].

However, the main drawback of this converter is also obvious. Such as relatively more complex topology layout. And even the dc-link capacitor voltage of this converter is fundamentally balanced, low frequency voltage ripples still occurs if no active control strategy or large dc-link capacitors applied.

2.2.2 Three-level T-type converter

The three-level diode NPC converter presents advantages of better output voltage and current harmonics, lower voltage stress on switching devices compares to the traditional two-level converter. However, its disadvantages are also obvious. For example, the increased converter topologies complexity and costs due to the additional switching devices as well as diodes, the two times the number of gate drive supplies compares to the one of two-level converters. In order to overcome these problems to some extent, the three-level T-type converter topology with reduced count of switching devices has been proposed in [33]–[37][90] according the generalized topology II discussed in section 2.1.4 as a tradeoff.

The phase-leg structure of the three-level T-type converter is shown in Fig.2.11. There are four switching devices in each phase-leg. This topology can be deemed as an extension of the two-level converter with one additional bidirectional neutral path (i.e two IGBTs connected back-to-back)

clamped between the NP and the phase-leg output. And if the two switching devices in the neutral path have their collectors connected, T1 and T3 can share one gate driver supply. The additional gate driver supply for T2 can be shared to all phases if multiphase system is required. Therefore, only one additional gate driver supply is required for the three-level T-type converter compares to the two-level converter. In terms of the switching device rated blocking voltage, due to the symmetrical structure of its phase-leg structure, the upper device T1 and lower device T4 have to block the whole dc-link voltage, and the devices T2, T3 only have to withstand half of the total dc-link voltage. Compare with the three-level diode NPC converter, there are no series-connected switching devices during each commutation process according to Fig.2.12. Therefore, under the same input and output condition, conduction losses can be reduced.

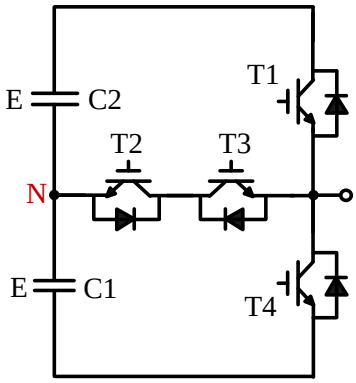


Figure 2.11 Phase-leg structure of the three-level T-type converter

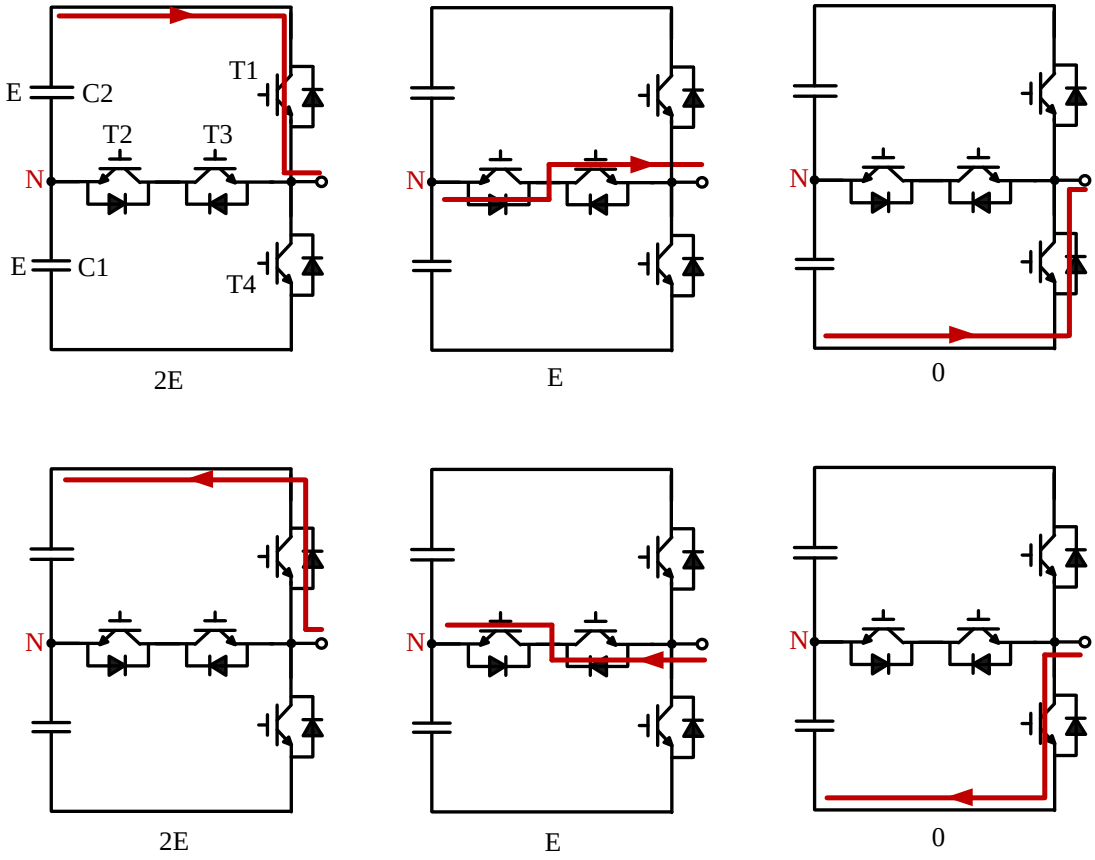


Figure 2.12 Switching states and current flow paths of the three-level T-type converter

Table II.VI presents the switching state truth table of the three-level T-type converter. It can be found out Table II.VI is identical to Table.II.V.

TABLE II.VI. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE THREE-LEVEL T-TYPE CONVERTER

Device / Voltage-level	T1	T2	T3	T4
2E	ON	OFF	ON	OFF
E	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON

Therefore, the main advantage of the three-level T-type converter is the more simplified structure compares to the three-level diode NPC converter. No clamping diode and less switching devices in the conduction path during commutation, which reduces the total conduction loss compares to the three-level diode NPC converter.

2.2.3 Four-level diode NPC converter

This is the most common four-level NPC converter [28][50][104]. In order to output four voltage levels at the ac-side, there are two NPs at the dc-link. Therefore, totally four clamping diodes as well as 6 active switching devices are allocated in each phase-leg as shown in Fig.2.13. Each switching device only has to withstand 1/3 of the total dc-link voltage, which is relatively more advanced compares to the three-level diode NPC converter as well as well the three-level T-type converter. However, due to the relatively higher number of switching devices as well as clamping diodes, the required gate driver supplies for each switching device increases, the totally converter topology complexity increases, the conduction loss during the operation also increases. Meanwhile, regarding to the multilevel NPC converter which has more than three-level output voltage levels, there is no redundant switching state for the inner voltage levels according to Table II.VII. Therefore, unlike the three-level NPC converter, the four-level diode NPC converter can not even realize the fundamental dc-link NP voltage balancing if no active control strategy applied [28]. The dc-link NP voltage balancing problem becomes a severe issue for the control requirement and system reliability. Therefore, the four-level diode NPC converter is not a good candidate for low power applications.

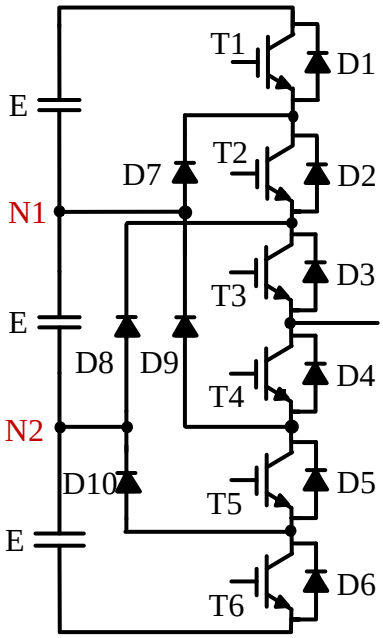


Figure 2.13 Phase-leg structure of the four-level diode NPC converter

TABLE II.VII. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE DIODE FOUR-LEVEL NPC CONVERTER

Device / Voltage-level	T1	T2	T3	T4	T5	T6
3E	ON	ON	ON	OFF	OFF	OFF
2E	OFF	ON	ON	ON	OFF	OFF
E	OFF	OFF	ON	ON	ON	OFF
0	OFF	OFF	OFF	ON	ON	ON

2.3 Power loss and efficiency analysis for the converter

2.3.1 Why power loss analysis and kinds of power loss

The power electronics converter plays the role to convert the power from ac to dc, dc to ac, or modify the ac signal frequency. Ideally, if ideal switching devices are employed, it will not consume energy. However, unlike the idea switching devices, the practical semiconductor switching devices exhibit the internal inherent characteristics such as the on-state resistance, the forward voltage drop, the turn-on rise time, the turn-off fall time, and the switching delay time [21][27][92]–[94]. These physical phenomenon accounts for the energy consumption and dropped efficiency inside power converters [108]. Therefore, in practical, the power conversion through the converter system employing the semiconductor switching devices is not 100% efficient, which means some parts of the energy has been dissipated. Apart from the energy waste, most of this energy loss converts into thermal loss and cause the converter system temperature rise, even failure. Thus, the power loss inside the power converter analysis is essential in order to employ the appropriate heatsink system to the converter preventing switching devices overheat and improve the whole power converter system efficiency.

Generally, converter losses can be divided into conduction losses and switching losses.

First one is the conduction loss. For practical switching device, it has the intrinsic resistance even when it is completely at on-state [21], [90], [104], [105], [109], [110]. The on-state resistance causes the forward voltage drop across the IGBT, MOSFET, and diode. Therefore, when the conduction current flowing through this on-state resistance, the actual switching device conduction voltage is above zero

to some extent as shown in Fig.2.14. Therefore, resultant conduction losses occur. The conduction loss can be calculated by multiplying the device forward voltage and corresponding converter current, and it generally can be realized by obtaining from the curve of forward voltage drop vs corresponding converter currents [21] [22][25] [109][111] [112][113][114].

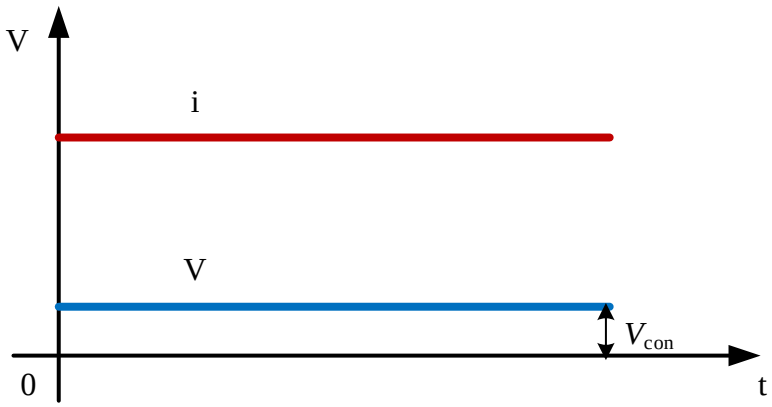


Figure 2.14 Switching device conduction voltage

Another kind of converter loss is the switching loss. For practical switching devices, intrinsic gate resistors and inductance make the devices gate voltages ramp up and down with the time. Therefore, the practical switching device can not switch on and off instantaneously. Therefore, during the switching transient, the overlap part between the current and the voltage on the switching device generates the switching loss as shown in Fig.2.15, where the dashed part is the overlap area.

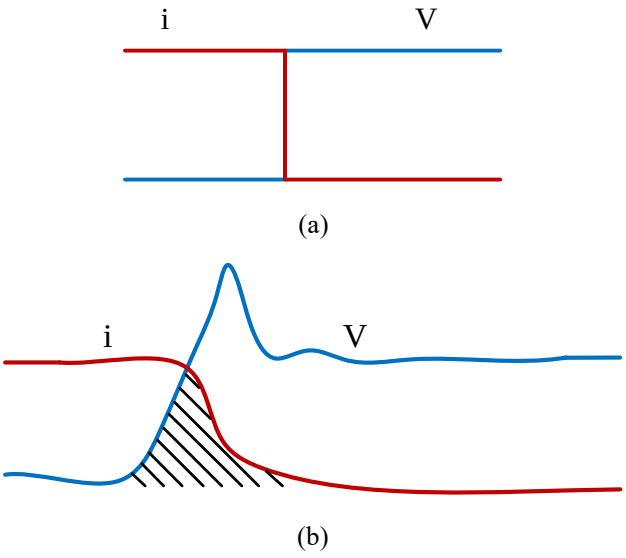


Figure 2.15 Relationship between voltage and current of the switching device during the switching transient (a) ideal switching device, (b) practical switching device

2.3.2 Average analytical model

The average analytical power loss model is normally derived based on averaging the power consumption over one fundamental cycle [115]. The average analytical power loss equations can directly present the relationship between the average power loss and system parameters such as voltages, currents, power factor and modulation indices, etc [22][108][115][116].

The switching device instantaneous conduction loss can be modelled as the product of the device conduction voltage drop Vce and the device collector current i_c [117][118]. The relationship between Vce and i_c of the switching device is generally given in the device datasheet. And this relationship is generally described as the first order polynomial fitting curve [117][119].

With regards to the switching device switching loss, it can be modelled by several methods.

One method is to build a very precious model based on the switching device physics characteristic which provides the voltage and current waveforms during the switching actions.

Take the IGBT based buck converter as an example as shown in Fig.2.16.

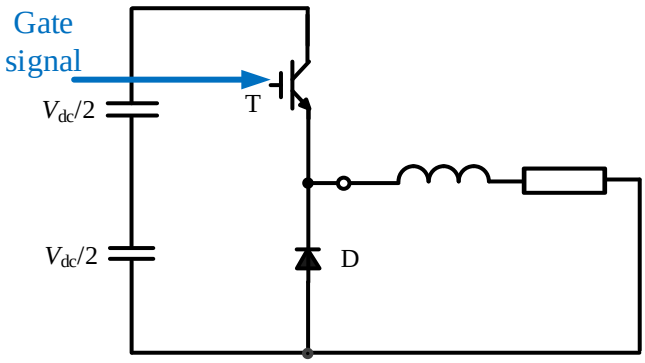


Figure 2.16 IGBT based buck converter

When a turn-on gate signal is sent to the IGBT gate terminal, T starts to turn on, the turn-on transient waveforms are shown in Fig.2.17 (a). The turn-on loss P_{on} can be expressed as (2.1)

$$P_{on} = V_{sw} \cdot i_c \cdot \frac{t1 + t2}{2} \cdot f_{sw} \tag{2.1}$$

where, V_{sw} is the IGBT blocking or switching voltage. i_c is the IGBT switching current. t1 is the IGBT switching current rising time. t2 is the IGBT switching voltage falling time. f_{sw} is the switching frequency.

When a turn-off gate signal is sent to the IGBT gate terminal, T starts to turn off, the turn-off transient waveforms are shown in Fig.2.17 (b). The turn-off loss P_{off} can be expressed as (2.2)

$$P_{off} = V_{sw} \cdot i_c \cdot \frac{t3 + t4}{2} \cdot f_{sw} \tag{2.2}$$

where, V_{sw} is the IGBT blocking or switching voltage. i_c is the IGBT switching current. t3 is the IGBT switching voltage rising time. t4 is the IGBT switching current falling time. f_{sw} is the switching frequency.

For the freewheeling diode, the most significant loss is the reverse recovery loss during its turn-off period as shown in Fig.2.17 (c). When the IGBT starts to turn on, its switching current i_c of the IGBT starts to rise up. At the meantime, the current flowing through the diode starts to fall down, and a negative current must flow through the diode to remove the stored charge before the diode can completely block any negative voltage [120]. The switching voltage value in the figure changes from zero to the negative value due to this switching voltage should be opposite to the diode forward conduction current. The diode reverse recovery loss P_{rr} can be expressed as in (2.3)

$$P_{rr} = Q_{rr} \cdot V_{sw} \cdot f_{sw} = V_{sw} \cdot i_{rr} \cdot \frac{trr}{2} \cdot f_{sw} \tag{2.3}$$

where, Q_{rr} is the reverse recovery charge. V_{sw} is the diode switching current. f_{sw} is the switching current. i_{rr} is the peak value of the diode reverse recovery current. trr is the diode reverse recovery time.

One thing should be noticed that t1, t2, t3, t4 or trr can be got from the switching device datasheet, or they can be derived from the practical test if required.

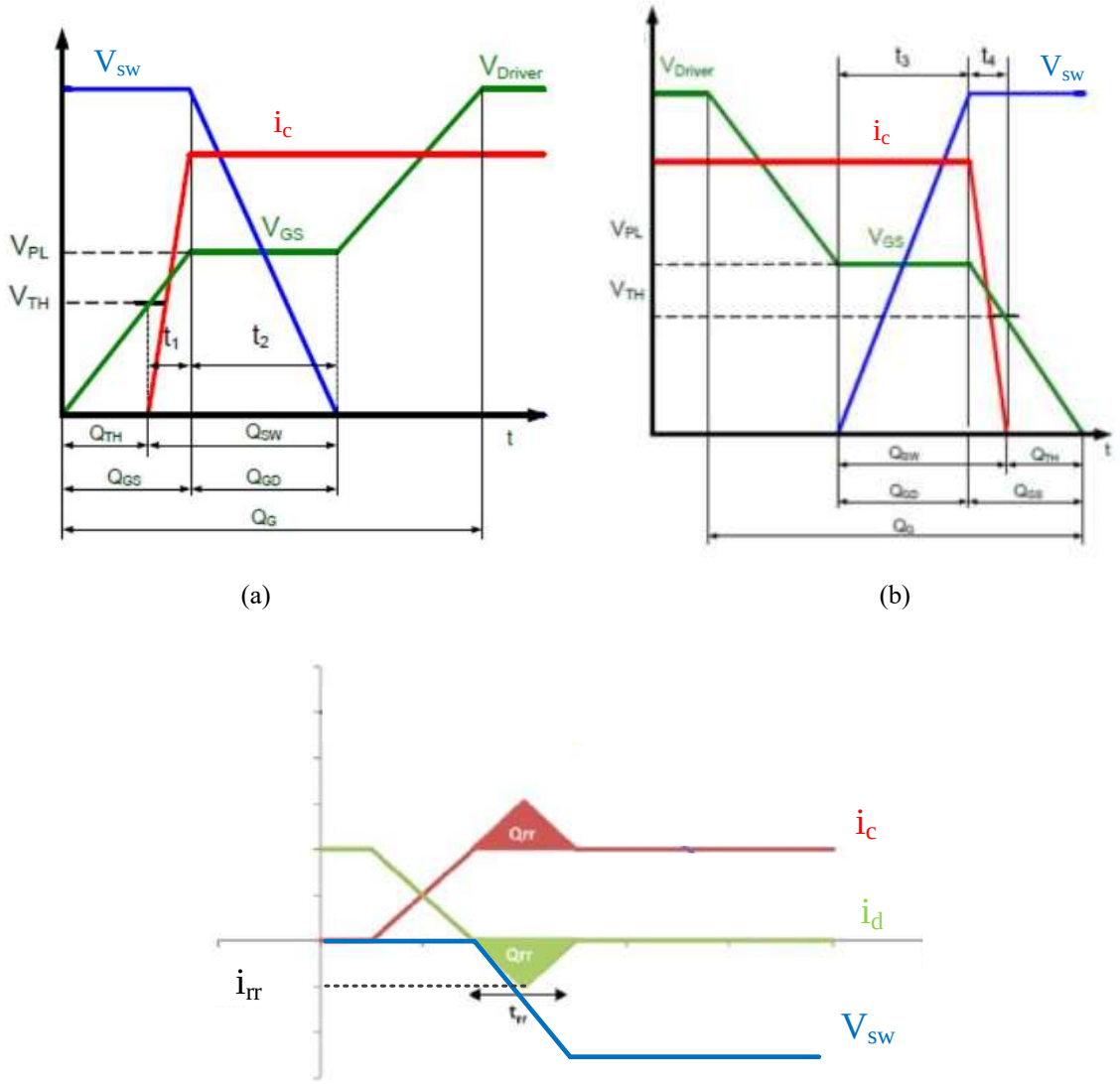


Figure 2.17 Switching transient processes of the switching devices (a) IGBT turn-on (b) IGBT turn-off (c) freewheeling diode reverse recovery

The second method is to derive the expression based on the total switching action times of the devices. This is generally based on well-defined PWM schemes [121]. If the PWM modulation wave can not be well defined or systems use hysteresis controller which show chaotic switching behavior, this method will not be a good option.

The third method is to establish the switching loss expression by a defined switching loss look-up table. This look-up table of the switching loss usually depends on certain parameters such as switching current, device blocking voltage, or/and junction temperature. This look-up could be found in switching devices datasheet but usually in the format as switching energy [115]. This is generally based on test data from

the devices manufactures, therefore, the blocking voltage might be different. If the blocking voltage on the datasheet V_{base} is different to the actual requirements, it can be adjusted by a linear approximation employing the factor V_{sw}/V_{base}. Or if a more accurate look-up table is required due to the specific circuit board layout, appropriate groups of practical double-pulse tests could be implemented [16][117]. The switching energy expression is generally as shown in (2.4)

$$E_{sw\_ins}=\left(a+b\cdot|i_c|+c\cdot i_c^2\right)\frac{V_{sw}}{V_{base}} \tag{2.4}$$

where, a, b, c are the switching energy curve fitting parameters as it is usually defined as the 2nd order function with regards to the switching current [117][122]. i_c is the switching device switching current.

So, based on the instantaneous power loss model, the analytical average expression can be derived. Eq (2.5) (2.6) express the average conduction loss mathematical expression and the average switching loss mathematical expression in a simplified manner, respectively

$$P_{con}=\frac{1}{2\pi}\int_{\theta_1}^{\theta_2}P_{con\_ins}\cdot d\theta \tag{2.5}$$

$$P_{sw}=\frac{1}{2\pi}\int_{\theta_1}^{\theta_2}P_{sw\_ins}\cdot d\theta \tag{2.6}$$

Where, P_{con} is the average conduction loss over one fundamental period, P_{con_ins} is the instantaneous conduction loss. P_{sw} is the average switching loss over one fundamental period, P_{sw_ins} is the instantaneous switching loss. θ_2, θ_1 are integration boundaries depending on conduction intervals or switching intervals for switching devices.

The average analytical analysis for the three-phase diode NPC converter has been presented in [21][97]. The average analytical power loss model based on CB-PWM for the three-phase T-type converter has been presented in [22]. The feature of the average power loss analytical expression is it can directly present the relationship between the switching device average power loss and other system parameters (such as dc input voltage, converter power factor, converter load current) [22]. Regardless of the converter topology type, the average analytical power loss model can be used to investigate converters' performance, power loss, and efficiency with any number of switching devices and any voltage levels multilevel converter with respect to the average power loss distribution. Furthermore, it is computationally efficient. In this thesis, as the average power loss analysis is selected for the four-level π-type converter, therefore, the detailed analysis will be presented in Chapter 4.

2.3.3 Numerical simulation

Numerical simulation power loss model is the method to establish the thermal model of the power switching devices and cooling systems (heatsink, fan cooling system, or liquid cooling system) by system parameters, then connect these thermal equivalent circuits in order to simulate and monitor dynamically in the software [27][117].

For the conduction loss, the actual conduction current can be set as the input to the instantaneous conduction loss model as described in section 2.3.2 in order to get the time behavior of the conduction loss as shown in Fig.2.18 [117][123].

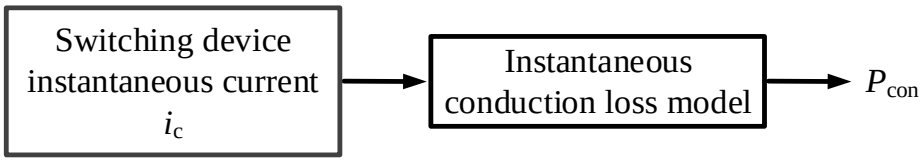


Figure 2.18 Conduction loss numerical simulation diagram

For the switching loss analysis, the general mathematical expression can use the methods which are the same as described in section 2.3.2. However, unlike the average analytical method, the method of implement these instantaneous switching power loss mathematical expressions to the numerical simulation system will be relatively more complicated. Fig.2.19 from [117] gives an example of such simulation process diagram. The switching device gate signal should be set as the input. When the switching signals detects on/off states change on the switching devices, an active pulse of height 1.0 will be generated with a pre-defined pulse width ΔT. This pulse signal has the unit 1/s, will multiply with mathematical instantaneous energy expression as described above to derive the corresponding switching power for this switching action.

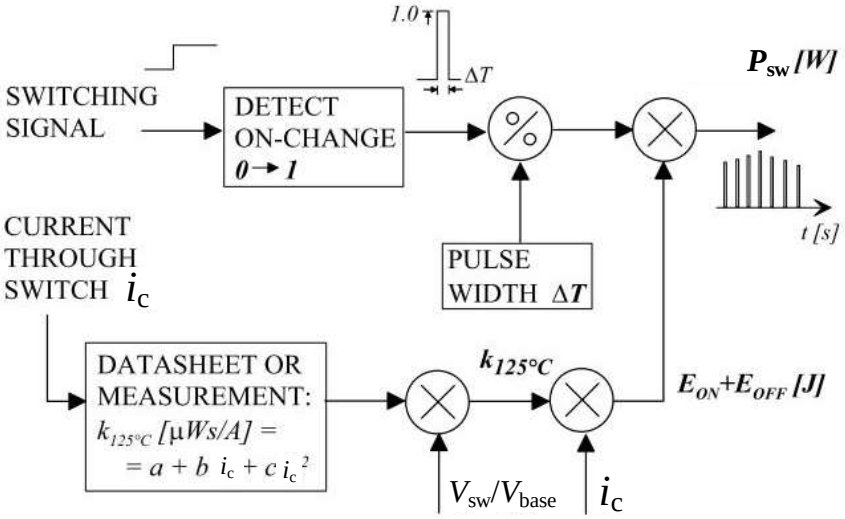


Figure 2.19 Implementation of the switching loss to numerical simulation diagram[117]

Fig.2.20 (a) presents the three-phase two-level converter system. Take the phase A upper device T1 for example. The collector current i_c measured from the device T1 provides the input for the power loss simulation. The gate signal (PWM signal) of T1 is also used as the input of the power loss simulation as shown in Fig.2.20 (b). The PWM signal can be used to count the switching actions and simulate the switching loss as described in Fig.2.19. The total power loss $P_{total}(t)$ of T1 then feeds into the T1 thermal model in order to calculate the junction temperature variables. The instantaneous calculated T1 junction temperature $T_{J,T1}(t)$ then feeds back to the T1 switching loss simulation block to dynamically adjust the temperature dependent model of the conduction loss and the switching loss.

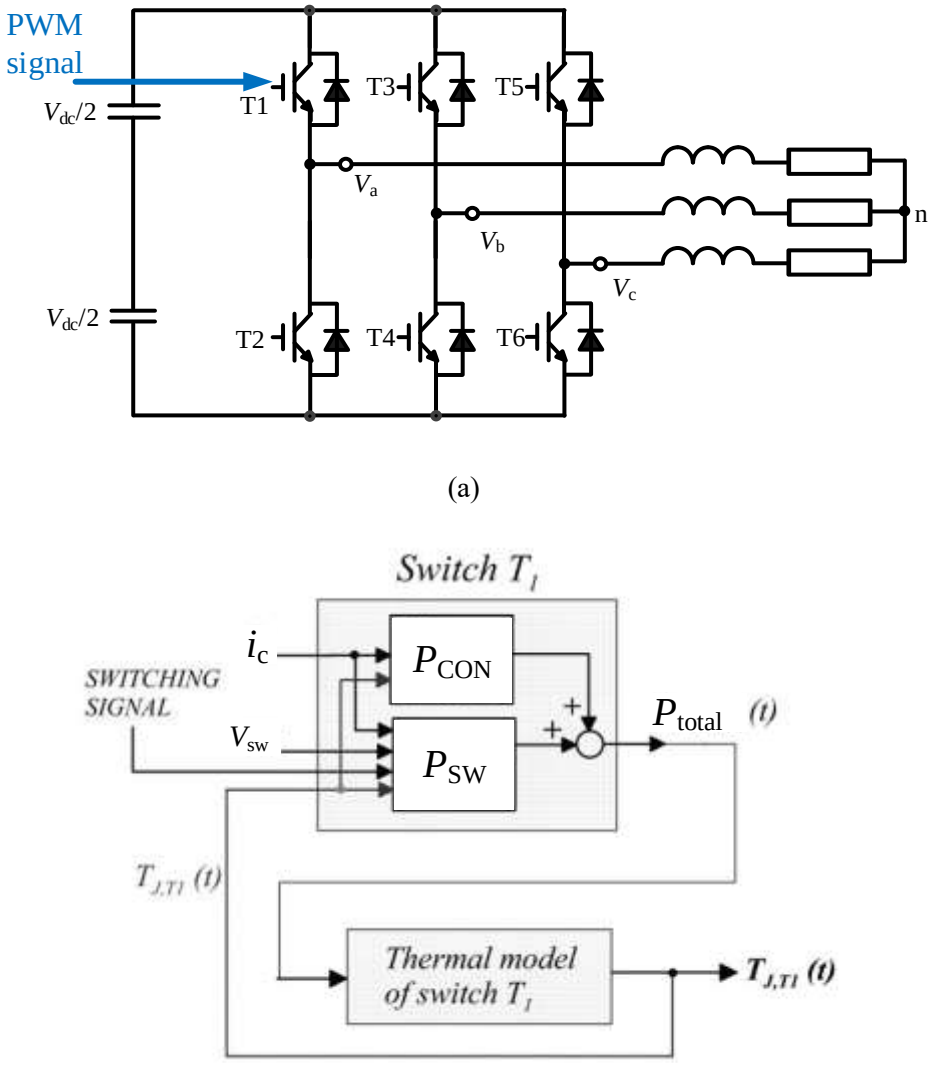


Figure 2.20 Example of the numerical simulation (a) three-phase two-level converter system (b) Implementation of the numerical power loss simulation as well as the junction temperature simulation [124]

The thermal model of the switching device can be established as a RC thermal circuit as an example shown in Fig.2.21. This model is usually derived from the thermal step response of the relevant switching device by 3D-FEM solver or through the experimental data [117]. The process of the thermal model establishment will not be discussed here, and the detail of the switching device thermal model setup process can be found in [125].

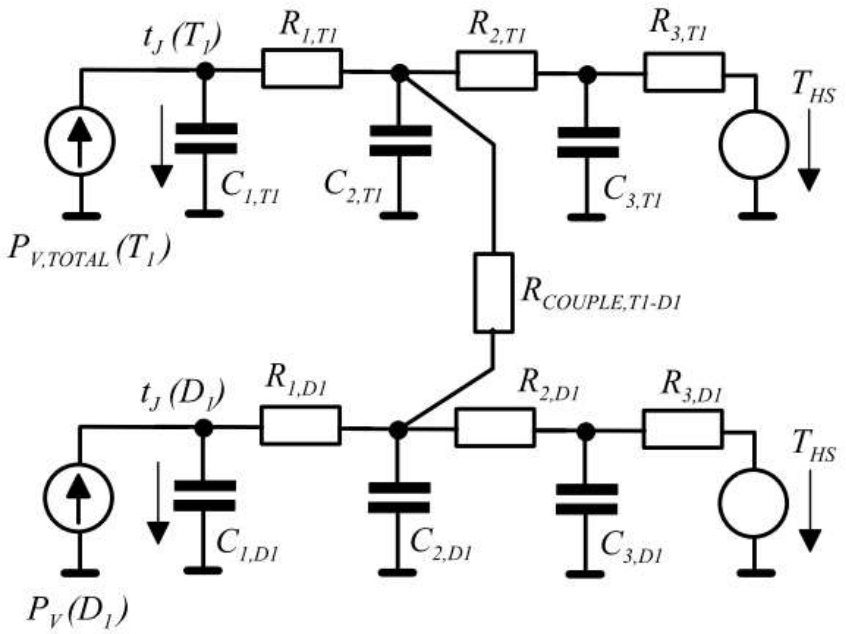
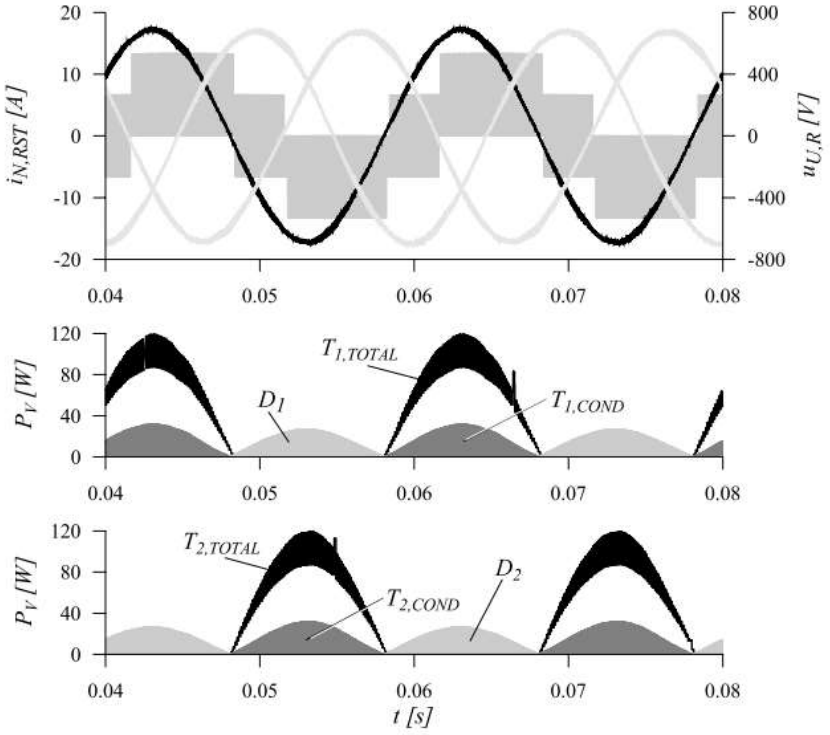
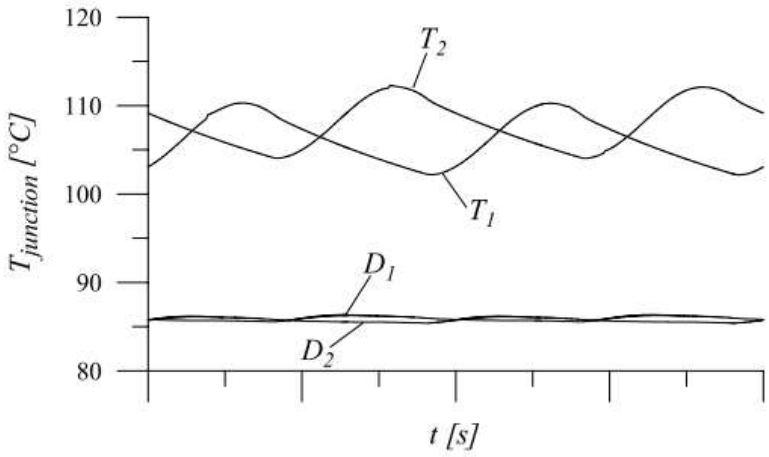


Figure 2.21 Thermal equivalent model of the switching device T1 and D1 in Fig.2.20 [117]

Fig.2.22 presents the example numerical power loss simulation results of two-level converter in [117] in order to demonstrate the concept of the final desired results. Fig.2.22 (a) gives the concept of the numerical power loss simulation based on the live time variation. With such simulation results, engineers are able to monitor and analyze the instantaneous power loss with regards to the change of the corresponding system voltage and current waveforms. Fig.2.22 (b) presents the concept of the numerical switching device junction temperature live time based variation, which is a good practice to predict the live time devices junction temperature variation in order to optimize the cooling system design.



(a)



(b)

Figure 2.22 Simulation output concept example (a) live time power loss of switching devices (b) live time junction temperature of switching devices [117]

The numerical simulation method of the power loss analysis is to demonstrate the live time based switching device power loss variation as well as the corresponding live time based switching device junction temperature variation. It is a good way to monitor the power loss and temperature change with

the converter devices voltage and current variation in a live simulation environment. Software such as PLEXIM, PSIM, Matlab can be selected as the simulation platform. For applications which require the real time power loss monitor function, the numerical simulation power loss analysis is a preferred solution. But the main drawback of this method is it requires more computation resource to calculate the instantaneous power.

2.4 Converter dc-link NP voltages balancing

2.4.1 The effect of the converter dc-link NP voltages unbalancing issue

The advantage of the NPC multilevel converter has been introduced in section 2.1.3. However, with the increase number of dc-link capacitors, the number of the NPs in the dc-link increases as well. It will cause the current flowing through each NP during each fundamental period hard to be coordinated [42][45][86][105][106]. Consequently, the dc-link NP voltage will eventually drift with the time pass. Therefore, the dc-link NP voltages drift issue has become a great challenge.

After figured out the reason of the dc-link NP voltage drift phenomenon, it is worth to take a look at what it will impact on the converter system. The negative impact on the unbalanced NP voltages for NPC multilevel converters can be summarized as follow.

- When the voltage applied on each dc-link capacitor is unbalanced, capacitors have to withstand undesired higher voltage, which may cause capacitors failure if the voltage is over the capacitor rated voltage. On the other hand, it disables the possibility to employ the cheaper capacitor with lower voltage rating on the dc-link, which is kind of loss in the advantage of the multilevel converter.
- Converters can not output desired voltage levels at high modulation indices due to the voltage collapse of inner capacitors of the dc-link. For example, the four-level converter can only output three voltage levels at high modulation indices as the whole dc-link voltage is distributed only on the top and the bottom capacitors of the dc-link. With a constant total dc-link voltage, switching devices have to withstand higher voltage during switching transients. Higher dv/dt increases the switching loss and reduces the switching devices reliability.
- The output waveforms harmonic increases due to the converter is not able to output desired

voltage levels.

- System reliability will be reduced as dv/dt of switching devices has to increase due to the voltage balancing lost in the dc-link capacitors. If it exceeds the voltage rating of switching devices, systems reliability will be significantly affected.

For the three-level NPC converter, such as three-level diode NPC converter and three-level T-type converter. Because there is only one neutral path between the dc-link and the converter output terminal, and due to their symmetry constructions, they have the fundamentally self-voltage balancing ability on the dc-link capacitors no matter what power factor conditions as shown in Fig.2.23. And there is only the low frequency voltage ripples at three times of the fundamental frequency for a three-phase system if there's no active NP voltage balancing control adopted [24][102][128].

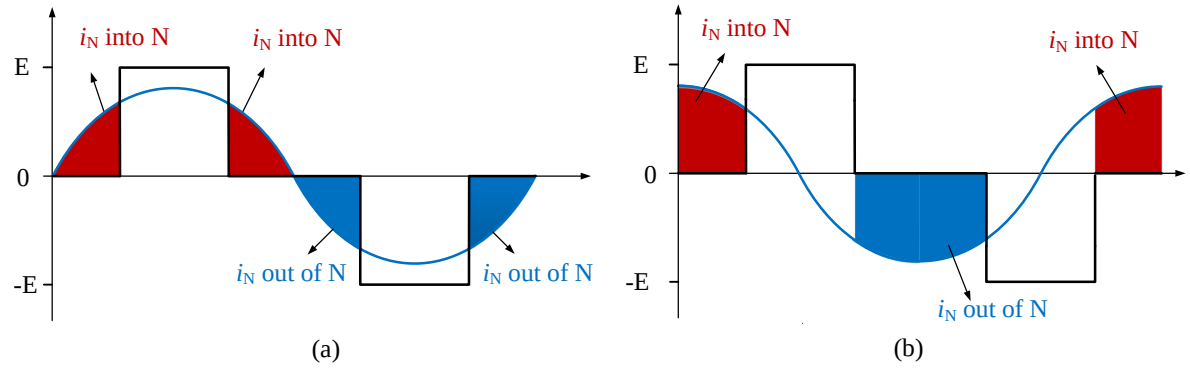


Figure 2.23 Neutral current flows condition for three-level NPC converter (a) power factor=1, (b) power factor=0

Some research work has addressed on reducing or eliminating the low ripple on three-level NPC converters by applying the appropriate modulation and control methods [19][92][128][129]. Publication [92] presented the dc-link NP voltage balancing control strategy based on the selection of the nearest three space vectors to synthesize the reference vector within each switching period (NTV SVM). This control method is not able to control the dc-link NP voltages for high modulation indices and low power factors. The reason of this limitation is the fact that in high modulation index conditions, the neutral path current produced by the medium vectors can not be fully compensated by the neutral path current caused by the small vectors [100]. From the point of view of the three-phase CB-PWM implementation, for the three-level NPC converter, under the low power factor condition, the higher the modulation index, the less zero-sequence components can be selected to inject into the original sinusoidal

modulation signals in order to regulate the neutral path current [43], [96], [101], [130].

The dc-link capacitors voltages share of the converter which has more than three output voltage levels during the operation is more complicated. When the NPC multilevel converter delivers non-zero real power to the load, the dc-link capacitors voltages balance is difficult to achieve [45][46]. This phenomenon exists when NPC multilevel converters work as inverters or rectifiers only. The charging and discharging problem has already appeared in the four-level converter [28][50] as shown in Fig.2.24. For the single phase-leg four-level NPC converter with the normal sinusoidal modulation, the middle capacitor C2 will be fully discharged within one fundamental period when PF=1. This is due to the fact as introduced in section 2.2.3 Table II.VII. For the single-phase four-level NPC converter, there is no other redundant switching states can be used for the neutral current adjustment for the dc-link capacitor voltage balancing. This phenomenon will severely limit the multilevel converter for the practical applications. And for the worse situation, the voltage unbalance may result in overvoltage of the switching devices and the dc-link capacitors, cause the converter system unstable or even fail [73], which limits the use of higher level NPC converter.

Therefore, appropriate dc-link NP voltage balancing method has to be employed in order to functional use the higher-level NPC converter.

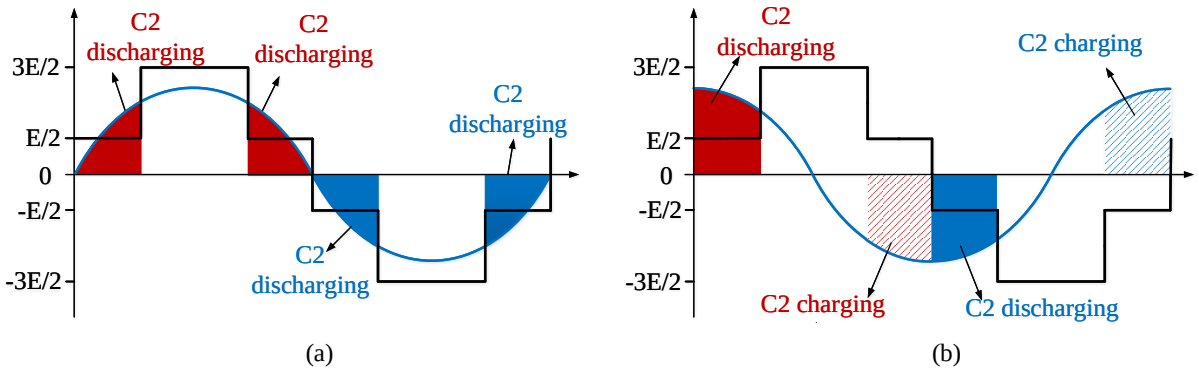


Figure 2.24 Charge and discharge conditions of C2 for the four-level NPC converter (a) power factor=1, (b) power factor=0

2.4.2 Existing converter dc-link voltage balancing control strategy

2.4.2.1 Isolated dc sources

The most directly way to balance the dc-link NP voltages is to use separated dc sources for each dc-link capacitor [131]. This method will be able to supply each dc-link capacitor with the stable dc voltage independently. The unbalance tendency caused by the neutral path current during the operation can be completely avoided [132][133]. However, this method requires numbers of the dc supplies in series connected for each dc-link capacitor. Fig.2.25 shows the concept of the four-level NPC converter supplied by three independent dc power supplies. For the four-level NPC converter, there are two NPs in the dc-link which splits the dc-link capacitor into three. Each dc-link capacitor requires an independent dc power supply in order to compensate the currents injected or extracted from NPs during the operation. The number of the required dc supplies increase with the increase of multilevel converter output voltage levels, which is not suitable for low voltage applications that requires the high power density and compact systems.

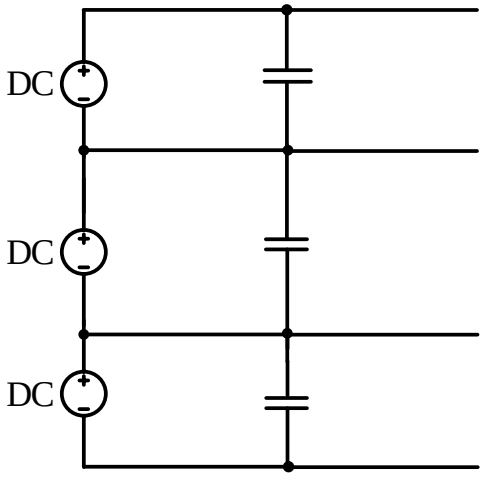


Figure 2.25 Concept of separated dc voltage supplies for the four-level NPC converter

2.4.2.2 Additional hardware/circuits to help with the NP voltage balancing

The NP voltages balance can be achieved by using additional passive or active components as shown in [65] in Fig.2.26. By employing a buck-boost converter, the energy will be forced to transfer from outer capacitors to inner capacitors.

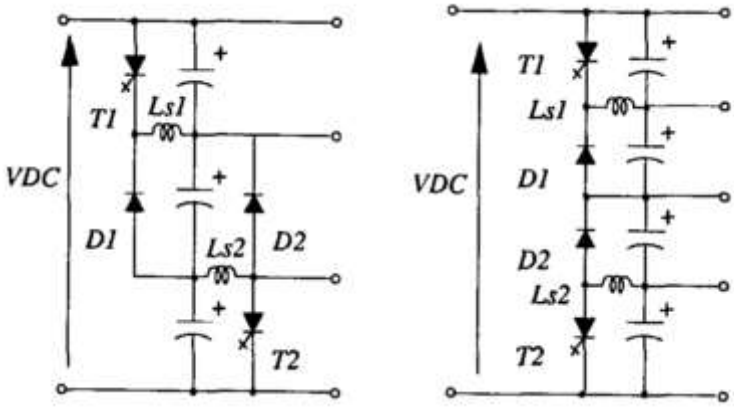


Figure 2.26 DC-link capacitors voltage balancing by using circuit remedy (a) four-level case (b) five-level case[65]

Similar approach is published in [98][134] as well, Based on the auxiliary converters, the current can be injected to the dc-link NPs of the main converter to balance the dc-link NP voltages. This method is able to employ pure sinusoidal modulation without the advanced modulation strategy. But the main shortcoming of this approach is the need for additional power hardware, which increases the complexity as well as the cost of the system and cause additional power losses [135].

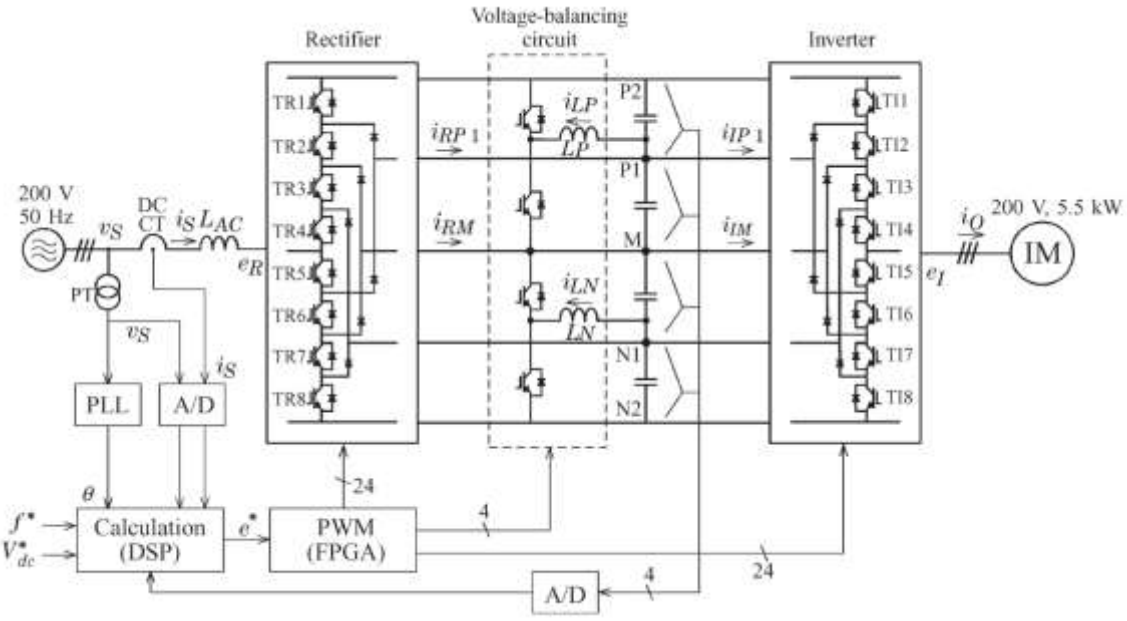


Figure 2.27 Bidirectional buck-boost chopper for dc-link capacitors voltage balancing for the five-level NPC converter[136] [137]

[136] [137]used two bidirectional buck-boost chopper to help with the dc-link voltage balancing for a

five-level NPC converter as shown in Fig.2.27. One of the two buck-boost chopper is used to balance the voltages of the top two capacitors (positive capacitors). Another one is for the voltage balancing of the bottom capacitors (negative capacitors). And they operated independent of each other.

The method uses additional passive components and auxiliary circuit can help with the dc-link capacitors voltage balancing and not increases the system volume too much compares to the method in section 2.4.2.1. However, this method still increases the total system cost by using more hardware components, and this method is not controllable during the operation as the hardware is fixed.

2.4.2.3 Advanced modulation strategy with active front end (back-to-back configuration)

As introduced in section 2.2 and section 2.4.1, for the NPC multilevel converter which has over three output voltage levels, the single phase-leg is not able to balance the dc-link NP voltages with the normal sinusoidal modulation. Therefore, the three-phase system with advanced modulation scheme has to be employed.

The key idea of the dc-link NP voltages balancing control strategy is the representation of the unbalance phenomena in a suitable capacitor energy-based cost function so that an optimum control approach can be used to minimize the goal function and to achieve the correct capacitor voltage balance [38][138][139]. This goal function can be mathematically expressed as shown in (2.7) [38]

$$\frac{dJ}{dt} = \sum \Delta v_c \cdot i_C \leq 0 \tag{2.7}$$

Where J is the energy of the dc-link capacitor, Δv_c is the difference between the ideal dc-link capacitor voltage value and the actual dc-link capacitor voltage value. i_C is the dc-link capacitor current. After the control goal function has been defined, the mathematical relationship between the goal function and the duty ratio of the output PWM signal could be established. This mathematical relationships have been discussed in many publications [28][41][44][51][53][140][141][142]. And this relationship will be detailed explained in Chapter 5 as well. With regards to the PWM techniques, there are two basic kinds of techniques: Space Vector PWM (SVM) [42][46][51][140] and Carrier-Based PWM (CB-PWM) [43][130].

SVM is very popular in converter control area which includes the NP voltage balancing control [2] [42][51][78][79][108] [120]–[122][144]. The space vector concept was first introduced as the technique

to analyze the electric machine by Pfaff, Weschta and Wich in 1982 [145]. The basic idea to analyze the converter switching states by considering per-phase quantities together as a group [146]. It means the generation of the converter control PWM signals will treat three-phase PWM as a single task, instead of generating three independent PWM signals or switching patterns.

Take the two-level converter as the example. Fig.2.28 presents a three-phase two-level inverter layout, V_{dc} is the input dc-link voltage for the inverter. V_{an} , V_{bn} , V_{cn} are three-phase output phase voltages applied to the star-connected RL load. S1 and S2 compose the phase leg A to control V_{an}. While S3 and S4 compose the phase leg B to control V_{bn}. S5 and S6 compose the phase leg C to control V_{cn}. And each pair of switches for each phase operate in a complimentary manner. For example, if phase A has S1 closed and S2 open, while phase B and phase C have their upper switches open and lower switches closed. This will lead to a positive voltage being applied to phase A

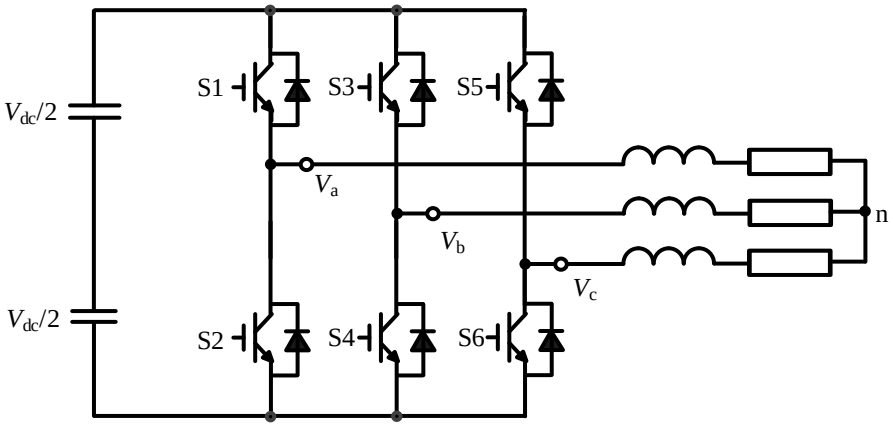


Figure 2.28 Three-phase two-level inverter layout

The concept of the space vector is a reference vector rotating at a constant frequency obtained from the three phase variables. The rotational vector or so-called reference vector is rotating in a stationary orthogonal αβ co-ordinate frame plane with the speed equals to the converter output fundamental frequency. Meanwhile, the frequency to refresh the new synthesized reference vector equals to the converter switching frequency [147][148]. At same time, the three-phase system is not an orthogonal coordinate frame. While in order to synthesize the reference vector, an orthogonal coordinate frame is required. Therefore, the Clarke Transformation can be used to transform the three-phase ABC frame into the equivalent orthogonal two-phase αβ coordinate frame [148][149]. Equation (2.8) expresses the Clarke Transformation.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (2.8)$$

The 2/3 term used here is to rescale the amplitude of the alpha-beta variables in order to maintain the same amplitude as in the three-phase frame system. Therefore, Table II.VIII summaries the switching states corresponding to the relevant vectors.

TABLE II.VIII Switching states and corresponding vector of two-level converter

Voltage Vectors	Switching states			Phase voltages			Vector values
	S1	S2	S3	V_{an}	V_{bn}	V_{cn}	
V0	0	0	0	0	0	0	0
V1	0	0	1	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 0^\circ$
V2	0	1	1	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 60^\circ$
V3	0	1	0	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 120^\circ$
V4	1	1	0	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 180^\circ$
V5	1	0	0	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 240^\circ$
V6	1	0	1	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}\angle 300^\circ$
V7	1	1	1	0	0	0	0

Therefore, there are total 8 different combinations of switching states on phase-leg A, phase-leg B, and phase-leg C. These 8 switching states make up six active space vectors (100), (110), (010), (101), (011), (001), and two zero vectors (000), (111) on the stationary orthogonal αβ co-ordinate frame plane as shown in Fig.2.29. The magnitudes of all six active vectors are equal and there is a 60° phase displacement between each two adjacent vectors.

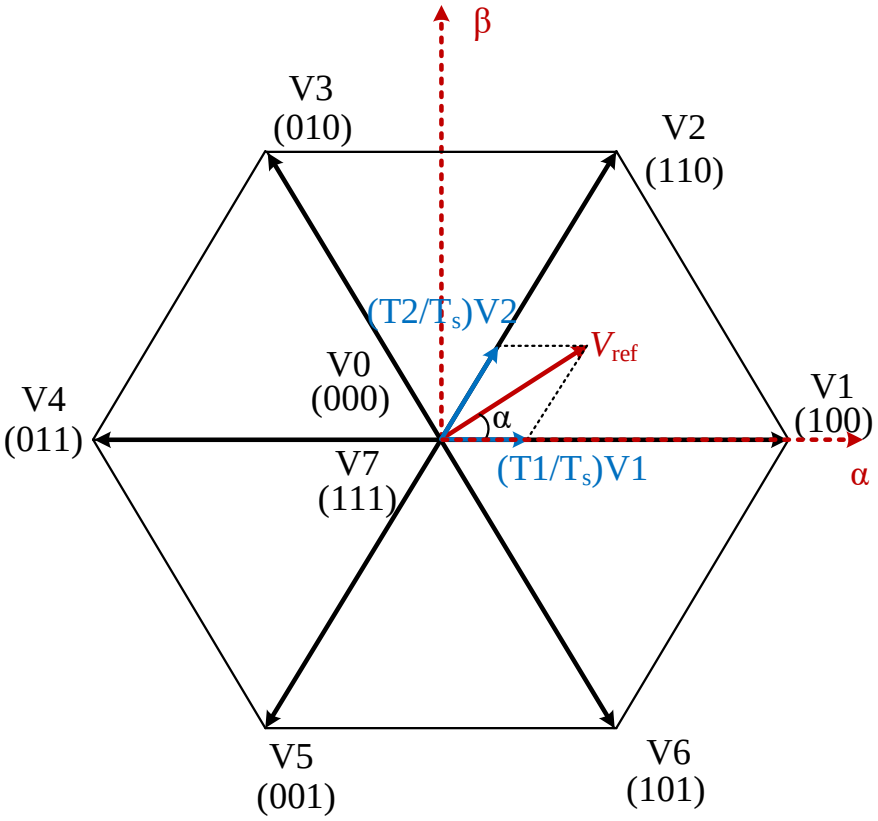


Figure 2.29 Principle of the SVM hexagon of the two-level converter

After the vector hexagon has been defined, the process to synthesize the reference vector could begin. First, the desired switching state vectors to synthesize the reference vector should be selected. Generally, Vref should be synthesized by nearest two active vectors plus one or two zero vectors within each sampling/switching period [28][143][150]. As presented in Fig.2.29, the SVM hexagon has been divided into 6 sections by six active vectors. Take the condition in Fig.2.29 as well. In this situation, Vref is located in the section between V2 and V1. Therefore, the nearest two active vectors to Vref are V2 and V1.

Second, the time duration (dwell time) of each selected vector should be calculated. Take the condition in Fig.2.29 as well, if two zero vectors are selected at the same time, Vref could be expressed in (2.9)

$$V_{ref} = \frac{T0 \cdot V0 + T1 \cdot V1 + T2 \cdot V2 + T7 \cdot V7}{T_s} \tag{2.9}$$

where T0, T1, T2, T7 are dwell times for V0, V1, V2, V7, respectively. Ts is the switching period. And T0, T1, T2, T7 could be expressed in (2.10) to (2.12).

$$T1 = \sqrt{3}T_s \frac{V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{3} - \alpha\right) \quad (2.10)$$

$$T2 = \sqrt{3}T_s \frac{V_{ref}}{V_{dc}} \sin(\alpha) \quad (2.11)$$

$$T0 = T7 = \frac{T_s - T1 - T2}{2} \quad (2.12)$$

where Vdc is the inverter dc-link input voltage. α is the Vref location angle on the αβ plane.

And third, after the dwell time for the two active vectors and the zero vectors within one sampling period have been calculated, it is possible to produce the switching sequence/pattern for the three phase-legs within each switching period. In order to make the switching actions minimum within each sampling period, the switching patterns should follow the symmetric principle: All on switching states on each phase should be at the center [147][148]. It is shown in Fig.2.30. Therefore, there will be only six switching actions (one switch-on action and one switch-off action for each phase) within one switching period.

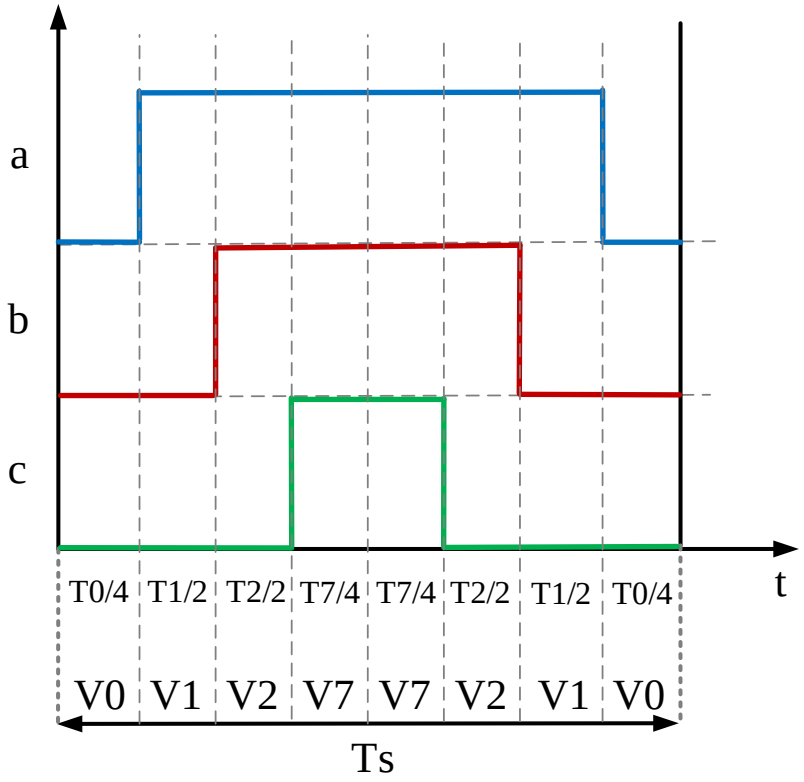


Figure 2.30 Switching pattern based on two active vectors and two zero vectors of two-level converter

It can be noticed above, Vref is synthesized by totally four vectors (two active vectors and two zero

vectors) within each switching period, which contains six switching actions within one switching period as mentioned above as well. The total switching actions within each switching period can be further reduced by using only one zero vector rather than two. Fig.2.31 presents the switching pattern when only uses zero vector V7. It can be found out that only two phases occur switching actions. This method is called the nearest three vector modulation (NTV). Therefore, the NTV modulation mentioned in Chapter 1 is a method by only using three vectors (two active vectors and one zero vectors) to synthesize the reference vector. With the NTV modulation, switching actions only occur on two phases, which reduce the switching loss at the same time.

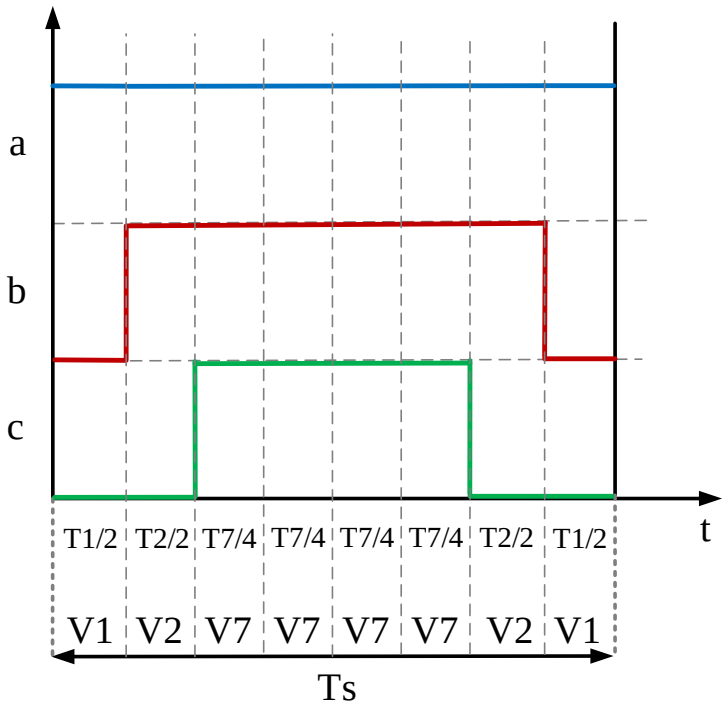


Figure 2.31 Switching pattern based on two active vectors and one zero vectors of two-level converter

Above introduction shows the reference vector synthesis process when the reference vector is within section as shown in Fig.2.29. The synthesis process when the reference vector is in other sections follows the same method by just using the corresponding different adjacent active vectors. This is the basic process of the SVM for the two-level converter.

Similarly, for the three-level converter, the SVM hexagon is shown in Fig.2.32. There is one more voltage level at the output phase-voltage compares to the one of the two-level converter. Therefore, there are totally 27 initial vectors, and the vector hexagon has been divided into 24 sections. Due to the

relative more sections within the hexagon compares to the condition of the two-level converter, all voltage vectors can be classified into four categories by the magnitude: zero vectors, small vectors, middle vectors, and large vectors [151]. Therefore, the procedure of the SVM algorithm for the three-level converter can be briefly introduced (similar to the two-level condition): First, identify the small triangle in which the reference vector locates. Second, calculate dwell times of the three vectors that in order to synthesize the reference vector. Third, identify switching states as well as the corresponding duty cycles according to the before mentioned dwell time calculations and the control goal function such as (2.7) [152]. And similar to the two-level condition, the reference vector can be synthesized by nearest three vectors [127]. Generally, it has been found out that large vectors and zero vectors have no effect on the NP voltages change, however the middle vectors as well as the small vectors have the effect on it [42].

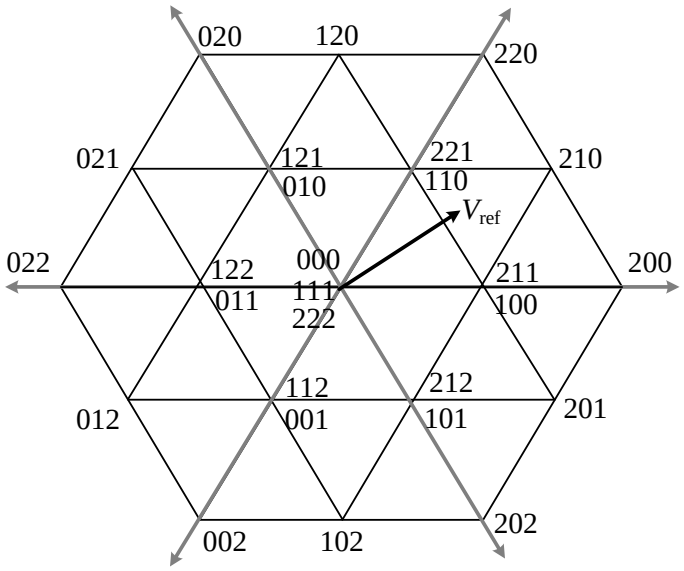


Figure 2.32 SVM hexagon for the three-level NPC converter condition

With converter output voltage level increases, the selection of redundant vectors leads to more and more difficult. However, the level shifted CB-PWM can be implemented relatively easier as it does not require to select the redundant vectors within each switching period. And the implementation complexity to realize almost does not increase with the converter output voltage levels increase. Therefore, the level shifted CB-PWM based control strategy can be deemed as the more preferred dc-link NP voltages balancing control when the NPC converter voltage levels are over three. In order to get the dc-link NP voltages balanced with the level shifted CB-PWM, the main task is to identify the

desired zero-sequence components according to the control target function.

Meanwhile, the dc-link NP voltage balancing control method based on NTV can also be implemented by CB-PWM. SVM synthesizes the V_{ref} by three or four vectors during each switching period can be substituted by CB-PWMs [153]. Many publications have presented the work on NTV based dc-link NP voltage balancing control strategy or its equivalent CB-PWM implementation [41][42][51] [52][55] [88] [124]–[126]. And the selection process of the desired zero-sequence signals are equivalent to the process of the proper selection of dwell times in equivalent redundant switching states [52] [55] [121][154] [156][157]. The fundamental frequency of zero-sequence components is three times of the fundamental frequency of original sinusoidal modulation waveforms. Therefore, the zero-sequence components injection into modulation waveforms does not affect the output line voltages as they can be cancelled out in the line voltage [101] [128][151] [158][159], but influences the switching states, consequently effects NP voltages. The third order harmonic signal is one of the zero-sequence signals. The concept of three-phase modulation waves with third order harmonic components as zero sequence signals injection is shown in Fig.2.33. Where in the upper figure, there are three-phase original sinusoidal modulation signals, and the third order harmonic signal as shown as the black waveform. In the lower figure, by adding the third order harmonic signal in to the original three-phase sinusoidal modulation signals, the final three-phase signals are not sinusoidal but a bit notch at tops due to the third order harmonics signals injection.

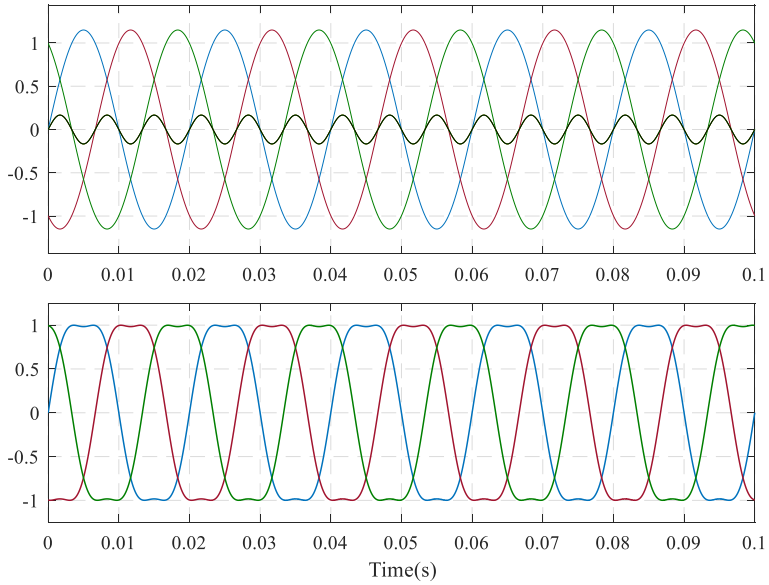


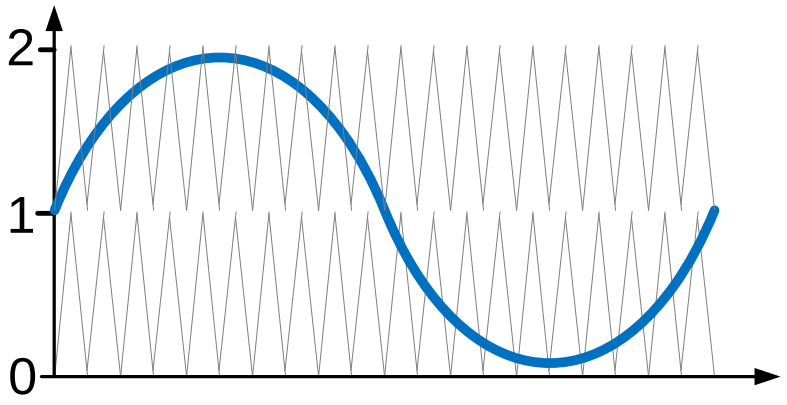
Figure 2.33 Concept of three-phase modulation waves with third order harmonic components as zero sequence

signals injection

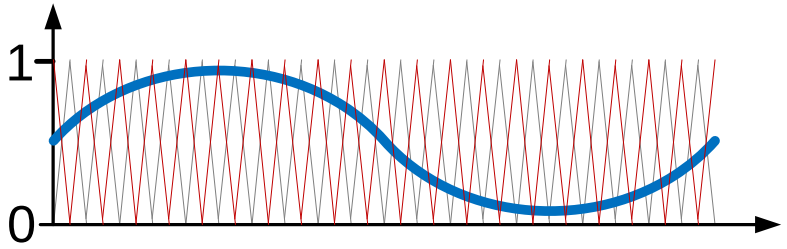
Meanwhile, for the CB-PWM, there are generally two kinds of implementations: level shifted CB-PWM [160], and phase shifted CB-PWM [66][161].

For the level shifted CB-PWM, two or more triangular carrier waves are vertically displaced with constant offset and can be deemed as stacked with each other. All carrier waves have the same amplitude and in phase with each other. Each carrier wave will interact with the modulation wave to control the switching condition of one pair of the complimentary switching devices. Meanwhile, for the level shifted CB-PWM, the modulation can only cross over one carrier wave at the specific part of the modulation wave. Take the three-level T-type converter condition for example, as shown in Fig.2.34 (a). There are two carrier waves (peak-peak value equal to 1) level shifted with each other. When the modulation wave instantaneous value above 1, only the top carrier wave has the interaction with it, which means, only S1 and S2 are continuously switching on and off within this region. S3 and S4 are kept on and off, respectively. Similarly, when he modulation wave instantaneous value below 1, only the bottom carrier wave has the interaction with it, which means, only S3 and S5 are continuously switching on and off within this region. S1 and S2 are kept off and on, respectively. Therefore, total switching actions can be kept minimum.

For the phase shifted CB-PWM, there is phase shift between carrier waves but no level shift with each other [145]. Similar to the level shifted CB-PWM, each carrier wave controls the switching condition of one pair of the complimentary switching devices. However, the modulation wave has to interact with all two carrier waves on both the first half fundamental cycle and the second half fundamental cycle as shown in Fig.2.34 (b). Therefore, the total switching actions significantly increase compare to the condition of the level shifted CB-PWM. So, this feature will make it generate more THD at the output line to line voltage. Therefore, the phase-shifted CB-PWM is not recommended for the NPC multilevel converter, but is more popular for the H-bridge cascaded multilevel converter. While each H-bridge cell is equivalent to a three-level converter. Two bipolar opposite triangular carrier waves are generated for each H-bridge cell. Four switches of the H-bridge cell are operated according to the comparison between the two triangular carrier waves and the modulation wave. The coordination among different H-bridge cells can be realized by the phase-shift of the different groups of the carrier waves [162].



(a)



(b)

Figure 2.34 Concepts of CB-PWM (a). level shifted (b). phase shifted

According to the review above, it is generally accepted that the level shifted CB-PWM is superior to phase shifted CB-PWM because it produces large harmonic concentration at some specific frequencies (such as three times the fundamental frequency) that can be cancelled in the line voltage, hence reducing their THD [14][163][164]. It can be monitored through an example on three-level T-type converter as shown in Fig.2.35. The THD value of the output line voltage based on phase shifted CB-PWM is about 10% higher than that of the level shifted CB-PWM condition. Therefore, the level shifted CB-PWM is generally preferred for the NP multilevel converter control.

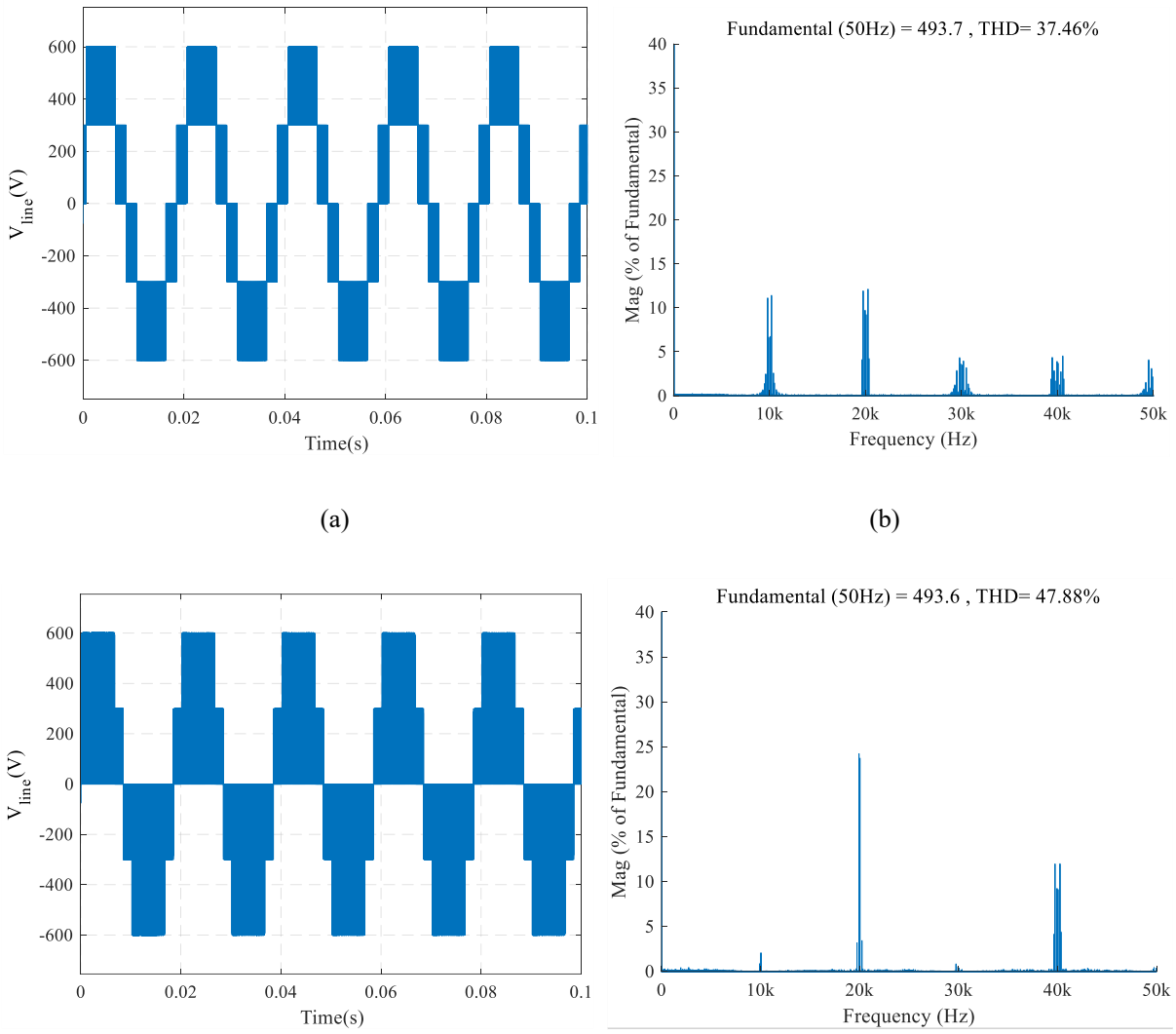


Figure 2.35 Different THD values of three-level T-type converter output line voltage based on (a) (b) level shifted CB-PWM (c) (d) phase shifted CB-PWM

Even the above control strategy is able to control the NPC converter dc-link NP voltage, however, when the voltage level is larger than three and the ac side power factor is close to 1 with the single-end inverter or rectifier employed, the control effect will be limited to about 0.6 modulation index [28][41][134][135]. Fig.2.36 from [41] presents the dc-link NP votlages balancing limit for five-level NPC converters and four-level NPC converters with respect to modulation indices and ac side power factor angles.

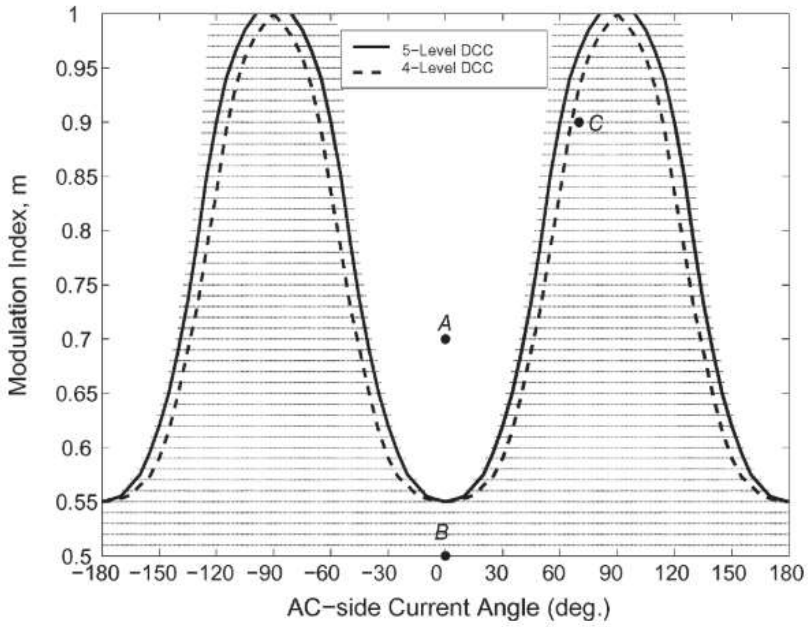


Figure 2.36 DC-link NP voltage balancing control limit for single-end NPC multilevel converters[41]

For NPC converters with over three voltage levels, based on NTV control strategy, when ac side unity power factor closes to 1, the higher the modulation index, the less redundant switching states can be selected for the dc-link NP voltages control. One solution is to use the back-to-back configuration [42][46][166]. When two NPC converters connect back-to-back through the same dc-link, these two converters can share the task of balancing the NP voltages. Converters on both sides are able to contribute the neutral path current to the NPs to help balance the dc-link NP voltages [38][42][46]. It means with the back-to-back configuration, the dc-link NP voltages balancing control ability can be significantly increased [38]. Additional advantages by adopting the back-to-back configuration include: 1) The ability to use the ac power supply. 2) The input power factor of the rectifier side can be controlled. 3) The power can be regenerated back to the supply through the back-to-back configuration [167][168], which is preferred for bidirectional power flow applications. Therefore, the back-to-back connected NPC multilevel converter which can output more than three phase voltage levels can be used as (i) interface medium for two asynchronous ac utility grids [51], (ii) high voltage dc system, (iii) controllable speed ac motor drive.

DC-link NP voltages balancing control limit for the back-to-back system based on NTV SVM when both side modulation indices and power factors different is also investigated in several publications. [129] analysed the dc-link NP voltages balancing control limits for back-to-back three-level diode NPC

converters in order to eliminate the NP voltage ripple as shown in Fig.2.37. It can be found, for the three-level diode NPC converter, the most difficult control area is close to a 90-degree output power factor angle. And the higher the modulation index, the less controllable ability on this point. DC-link NP voltages balancing control limits for back-to-back five-level diode NPC converters have been presented in [44][45][136] with offline-calculated modulation signals by various simulations attempts. Reduce the power factor on either side can help with the control ability.

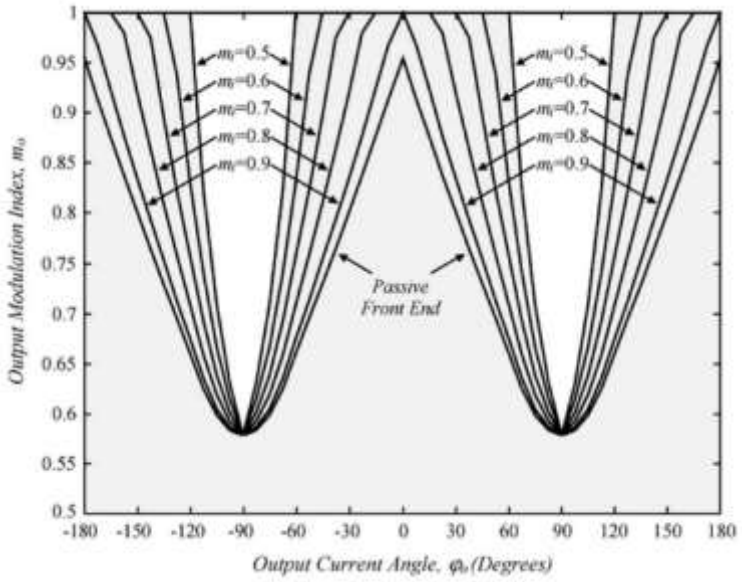


Figure 2.37 Theoretical dc-link capacitor voltage balancing control limit for the back-to-back three-level NPC converter[129]

2.4.2.4 Virtual vector PWM (VV PWM)

DC-link capacitors voltage unbalancing issues can also be resolved by employing the control method based on a VV PWM with a passive front-end for multilevel NPC converters under any power factors and modulation indices [26][43][47]–[49][54][86][87][120][121][140]. The idea of this modulation strategy as well as the control method is to coordinate switching actions within each carrier-waveform period in order to reduce the neutral path current to zero. Compared to the NTV based control strategy, the VV PWM based control strategy will have more than two switching actions on each phase leg within each switching period. And during each switching period, the converter phase is allowed to switch between any voltage level. Fig.2.38 presents the concept of output voltage switching sequence within one switching period for a four-level NPC converter, where the output voltage switched between all

four voltage levels.

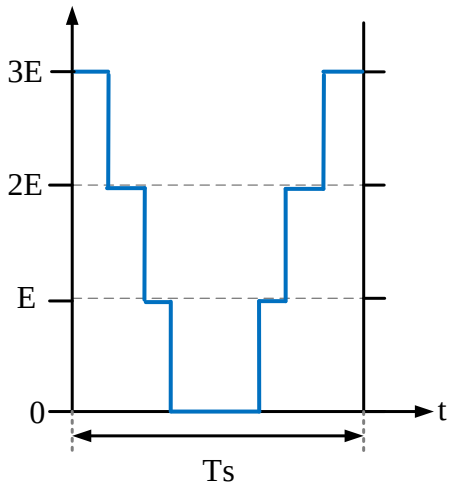


Figure 2.38 concept of output voltage switching sequence within one switching period for a four-level NPC converter.

Even the VV PWM based dc-link NP voltage balancing control strategy is able to guarantee the control effect at any operation points, its drawback is still obvious. The output voltage for each phase in each switching period involves more than two voltage levels, and the number switching actions can increase significantly. This feature increases the switching loss significantly and the output harmonics increase to some extent as well [54][86][87].

The VV PWM based control strategy can also transfer to the CB-PWM implementation. Fig.2.39 presents the concept of the CB-PWM implementation of VV PWM for the four-level NPC converter. There are three modulation waves in total in order to force the neutral path current to zero by coordinating the switching actions [43][54][171].

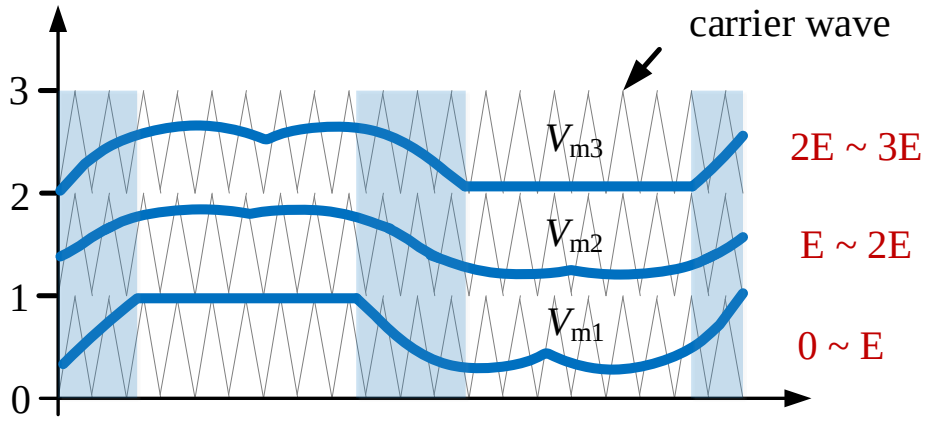


Figure 2.39 Concept of CB-PWM implementation of VV PWM based control

2.5 Summary

The NPC converter presents the suitability for low voltage applications. As compare to cascaded H-bridge converters, there is only one dc-link bus for the NPC converters, which will only require single dc voltage supply, reduce the total converter cost and volume. Compare to the FC converters, there is no additional capacitors in the phase-leg of the NPC converters. This significantly reduce the total converter volume and cost as well.

Among different NPC converter topologies, under the same output voltage level condition, the NPC topology derived from the generalized topology II such as the three-level T-type converter can have the reduced count of the switching devices which reduces the conduction loss, and is preferred for low applications. The four-level π-type converter is the NPC converter derived from this generalized topology and can be deemed as the potential candidate for low voltage applications.

In order to provide comprehensive power loss/thermal analysis for the cooling system design, the average analytical power loss model can be selected. This power loss model provides the mathematical expression of the power loss model for switching devices based on average power loss distribution as the function of voltage, current, power factor, modulation index, etc. It provides a preferred way to adjust the parameters such as voltage, current, power factors, etc during the design.

In order to resolve the dc-link NP voltage drift issue, the back-to-back configuration with the NTV based control strategy can be employed for bidirectional power flow applications.

The topology analysis, power loss analysis as well as the dc-link NP voltage balancing control design

for the four-level π-type converter will be presented in the following chapters based on the reviews in Chapter 2.

3 Four-level π-type converter topology and modulation technique

3.1 Introduction

According to the introduction in section 2.1, multilevel converters have advantages such as lower voltage stress (*dv*/*dt*), lower output harmonic content, and lower switching losses under the same switching frequency and input voltage conditions. However due to the increased number of switching devices, actual conduction losses as well as the total converter topology complexity are the considerable drawback. At the same time, according to the reduced number of switching devices multilevel converter derivation methods published in [18][31]–[34][36], an active NPC four-level π-type converter was introduced. This topology has only six switching devices per phase-leg. Compares to the popular employed three-level diode NPC converter and the three-level T-type converter, the four-level π-type converter only has two more switching devices on each phase-leg, no clamping diodes required, but has lower output harmonics and lower voltage stress on the switching device under the same input voltage condition. Compares to the even higher-level NPC converters such as five-level NPC converters, the total topology complexity as well as the modulation control complexity of the four-level π-type converter reduce. In order to give an initial understanding as well as the clear view of the proposed four-level π-type converter, this chapter introduces the structure configuration, modulation concept as well as the appropriate switching device voltage rating selection for the four-level π-type converter. Meanwhile, in order to adopt the literature review and demonstrate advantages of the four-level π-type converter compares to the other popular NPC converters as well as the traditional two-level converter, the topology configuration feature comparison and the simple open-loop operation comparison among the traditional two-level converter, three-level diode NPC converter, as well as three-level T-type converter has been analyzed in this chapter. It can be found out with the same input dc voltage level as well as the same switching frequency, the proposed four-level π-type converter is of the lower voltage stress on switching devices, lower output harmonics, as well as the compromised phase-leg configuration complexity among these four converter topologies.

Some of the work in this chapter has been published in [78], [115] by the author already.

3.2 Topology introduction and modulation scheme

In this section, the topology characteristic as well as the corresponding modulation scheme for the four-level π-type converter will be introduced. Fig. 3.1 (a) shows the structure of the phase-leg for a four-level π-type converter, which contains six switching devices. Take IGBTs as unit switching devices for this topology, two bidirectional neutral paths can be created by connecting two IGBTs back-to-back between dc-link NPs (N1 and N2) and the output terminal. Four output voltage levels then can be realized by clamping the phase-leg output terminal to the appropriate dc-link junction point with this configuration.

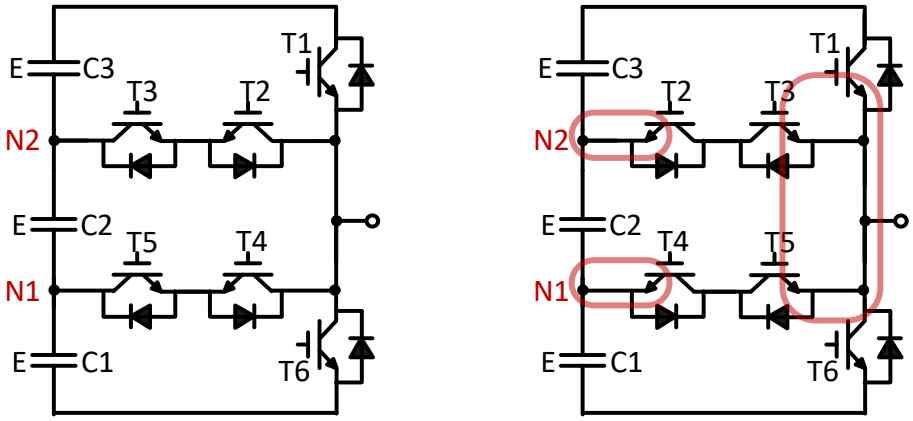


Figure 3.1 Phase-leg structure of a four-level π-type converter (a) common-emitter connection in neutral paths (b) common-collector connection in neutral paths

With respect to the number of required switching devices gate driver supplies, as shown in Fig. 3.1 (a), T2, T3 or T4, T5 can employ the same gate drive supply with a common-emitter connection. Thus, for a three-phase four-level π-type converter, there will be 6 additional isolated gate driver supplies required compares to the traditional two-level converter. In order to further reduce the number of required gate driver supplies, T2, T3 pair or T4, T5 pair can have a common-collector connection as shown in Fig.3.1 (b). With such configuration, T1, T3 and T5 can use the same gate driver supply as they share the same emitter potential. T2 and T4 then require two additional individual gate driver supplies, which can also be shared by another two phase-legs as their emitters are connected to the dc-link NPs. Therefore, with the configuration in Fig.3.1 (b), compares to the two-level converter, only two additional gate power supplies are required for a three-phase four-level π-type converter system.

In this thesis, the PWM has been selected to modulate the converter. Meanwhile, the carrier/switching frequency is set far higher than the modulation/fundamental frequency. From each switching period point of view, the modulation signal value can be treated as constant during each switching period, which is convenient for the implementation through a digital signal processer (DSP) in practice.

Next, the operation principle and the modulation for the four-level π-type converter will be analyzed. Fig.3.2 shows converter output voltage levels and corresponding switching states with respect to the converter current directions. There are total 8 switching states with considering the converter current directions.

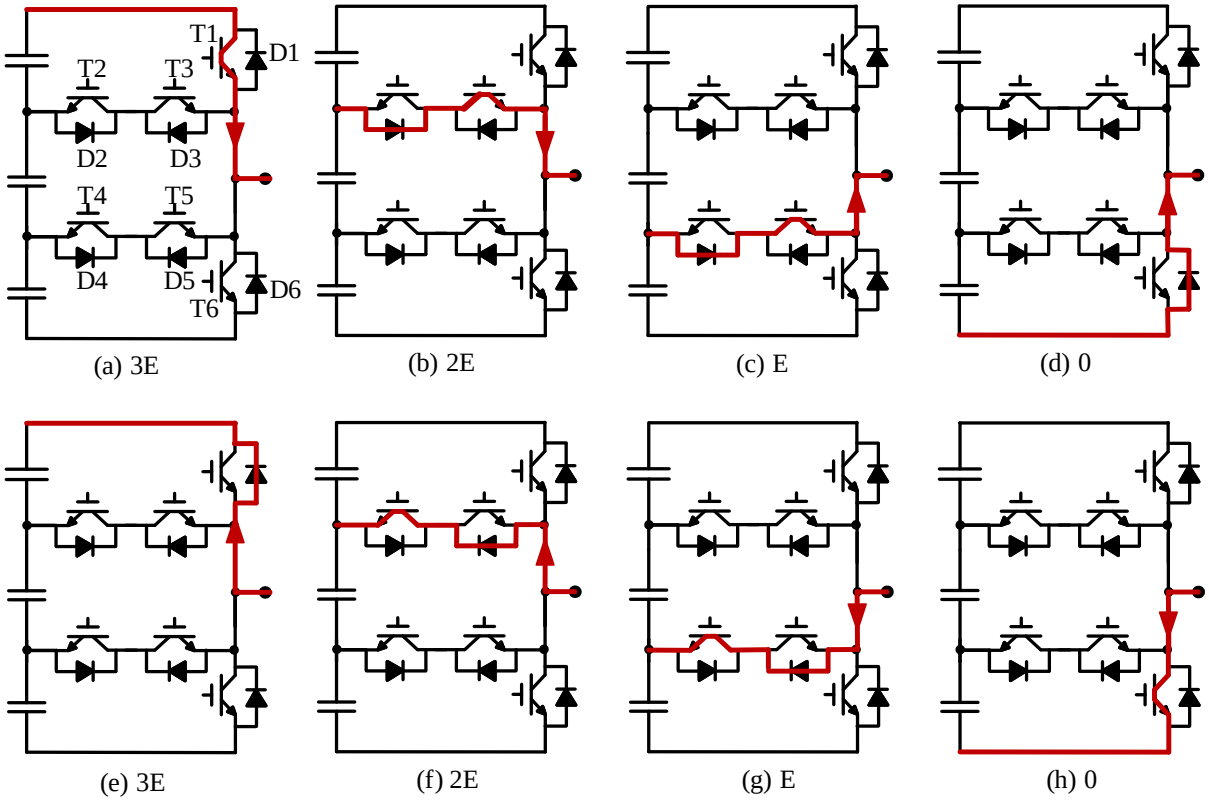


Figure 3.2 Switching states and current flow paths

Fig.3.3 (a) shows the original concept of this traditional level shifted CB-PWM scheme, where intersections between the modulation wave and three carrier waves determine switching states for three different pairs of switching devices, respectively. For example, when the modulation wave across the top carrier wave, T1, and T2 switch on and off in a complimentary manner. Meanwhile, during this period, the modulation wave is always over the middle and bottom carrier waves, therefore, T3, T5 stay in on-state, while T4 and T6 stay in off-state. In order to make it easy to be implemented in the digital

control chip, the modulation wave can be set as per-unit (p.u.) value. Assume dc-link NP voltages are balanced under this condition. Set the voltage E on each dc-link capacitor as the based value, then the total dc-link voltage can be converted to 3. The p.u. amplitude value of each carrier wave can be normalized to 1/3 of the total dc-link voltage and equals to 1. Then, the p.u. peak-to-peak amplitude value of the modulation wave will be in the range of 0~3 with reference to the negative side of the dc-link. Take the pure sinusoidal PWM for example, the modulation wave can be expressed as (3.1)

$$u_i(t)=1.5m\cdot\sin(\omega t)+1.5 \qquad i=a,b,c \tag{3.1}$$

where m is the modulation index. ω is the fundamental frequency. $u_i(t)$ is the modulation wave.

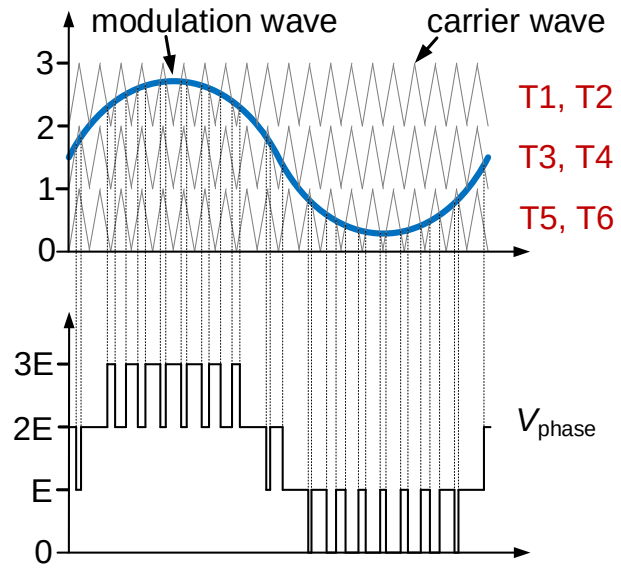
This modulation method will require multiple level shifted carrier waves, which occupies more logic resource when program in the field programmable logic array (FPGA). To resolve this problem, the modulation wave can be adjusted according to Fig.3.3 (b). The level function can be derived as in (3.2)

$$L_i(t)=\text{floor}[u_i(t)] \tag{3.2}$$

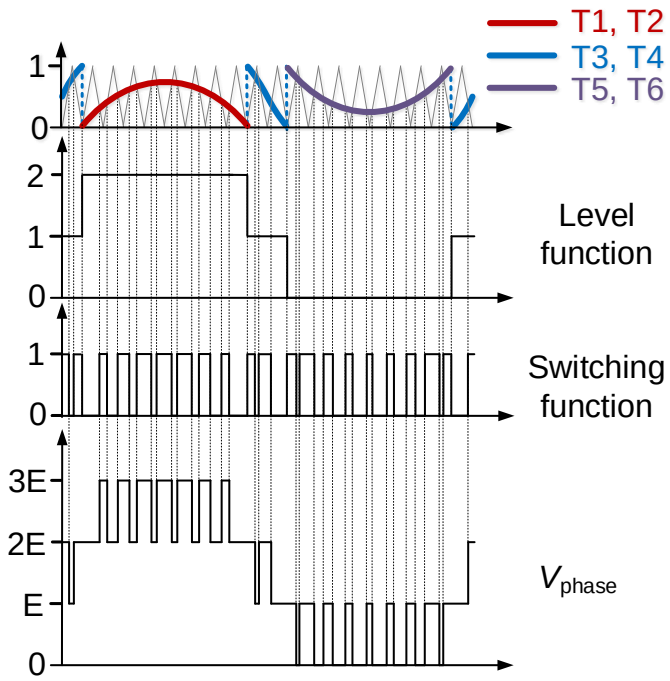
The floor function is able to output the greatest integer $L_i(t)$ less than or equal to $u_i(t)$ which denotes the level number of the modulation wave/output voltage. Then the modified modulation wave can be derived in (3.3)

$$T_i(t)=u_i(t)-L_i(t) \tag{3.3}$$

With the modified modulation wave $T_i(t)$, only a single carrier wave is required to determine its intersections with the modulation wave. Then the resultant PWM signal (switching function) will be superposed on the level function to apply on the appropriate switching devices, then obtain the final phase voltage.



(a) Three level shifted carriers with sinusoidal modulation wave



(b) Single carrier with modified modulation wave

Figure 3.3 Traditional level shifted CB-PWM scheme for the four-level π-type converter

With the traditional level shifted CB-PWM, the four-level π-type converter is able to operate appropriately. Table III.I summarizes the logic switching groups for each switching device according to different commutation processes during the operation.

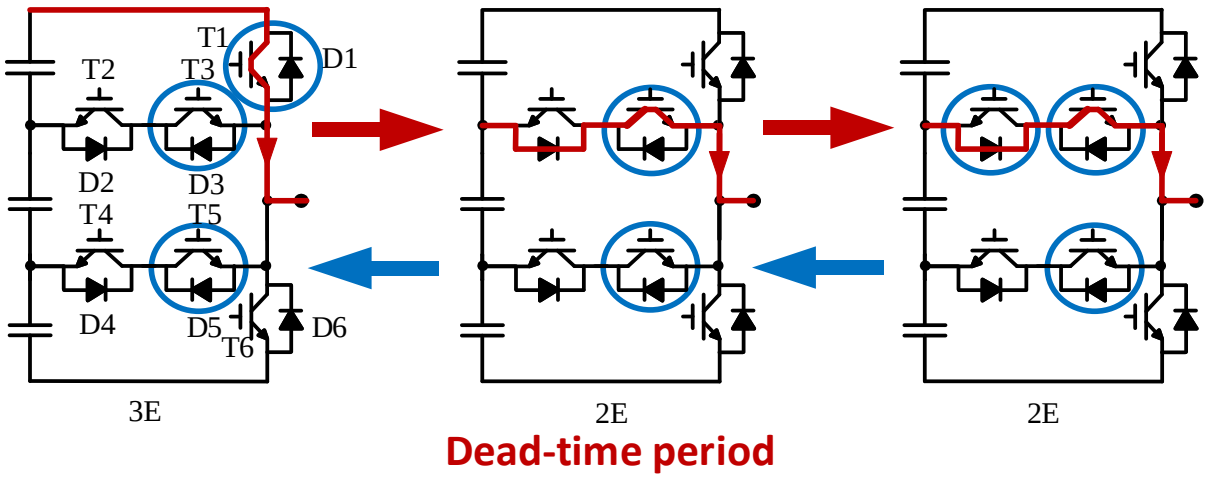
TABLE III.I. SWITCHING STATES AND OUTPUT VOLTAGE LEVELS FOR THE FOUR-LEVEL Π-TYPE CONVERTER

Voltage-level \ Device	T1	T2	T3	T4	T5	T6
3E	ON	OFF	ON	OFF	ON	OFF
2E	OFF	ON	ON	OFF	ON	OFF
E	OFF	ON	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON	OFF	ON

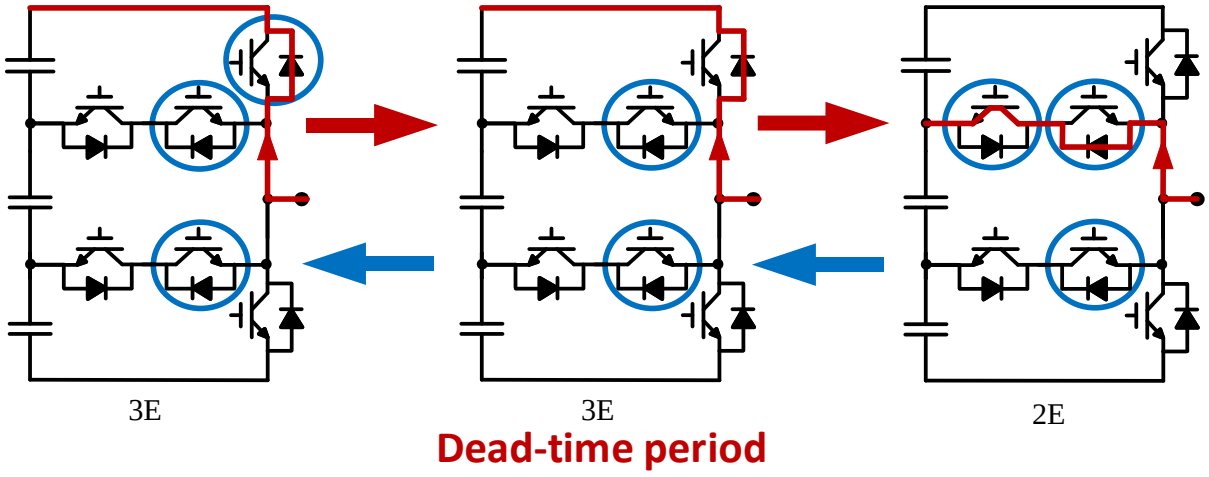
In order to prevent the shot through phenomenon in a practical converter circuit during commutations, an appropriate dead-time has to be inserted between switching actions of the two complementary devices. Fig.3.4 presents each commutation process with considering the dead-time effect. Fig.3.4 (a) (b) present the commutation process between 3E and 2E. In this case, T3 and T5 should be always "ON". T1 and T2 switch in turn in a complementary manner. T1 turns ON in order to get a 3E voltage output. T2 turns ON in order to get a 2E voltage output. Meanwhile, when the output voltage is 2E, and the output current flows out of the converter, during the dead-time period, the current flows through D2 and T3. When the output voltage is 3E, and the current flows into the converter, during the dead-time period, the current flows through D1.

For the commutation between 2E and E as shown in Fig.3.4 (c) (d), T2 and T5 are always "ON". T3 and T4 switch in turn in order to output voltages 2E and E respectively. When the output voltage is E, and the current flows out of the converter, during the dead-time period, the current flows through D4 and T5. When the output voltage is 2E, and the current flows into the converter, during the dead-time period, the current flows through T2, D3.

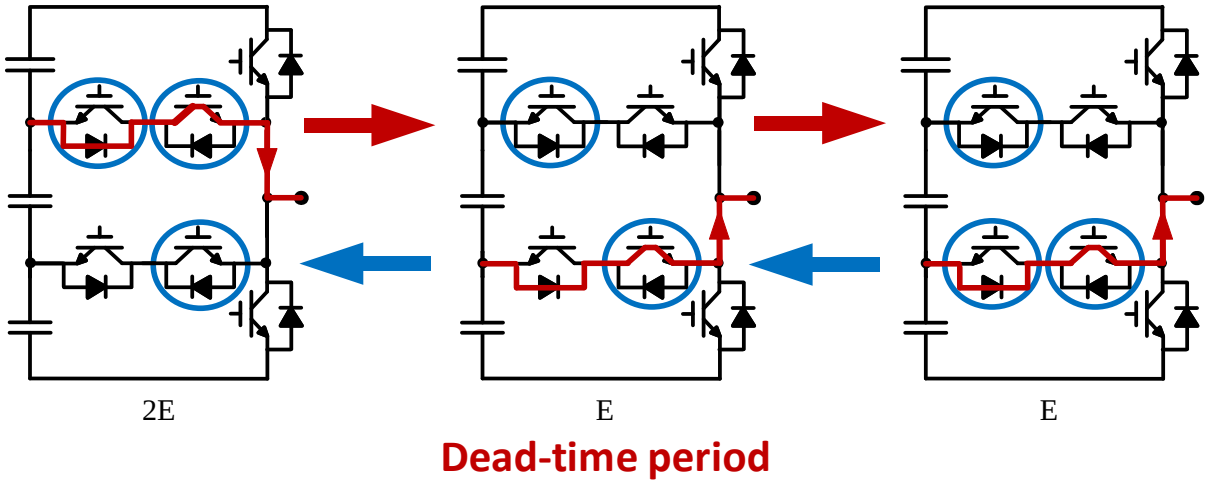
For the commutation between E and 0 as shown in Fig.3.4 (e) (f), T2 and T4 are always "ON". T5 and T6 switch in turn in order to output voltages E and 0, respectively. When the output voltage is 0, and the current flows out of the converter, during the dead-time period, the current flows through D6. When the output voltage is E, and the current flows into the converter, during the dead-time period, the current flows through T4 and D5.



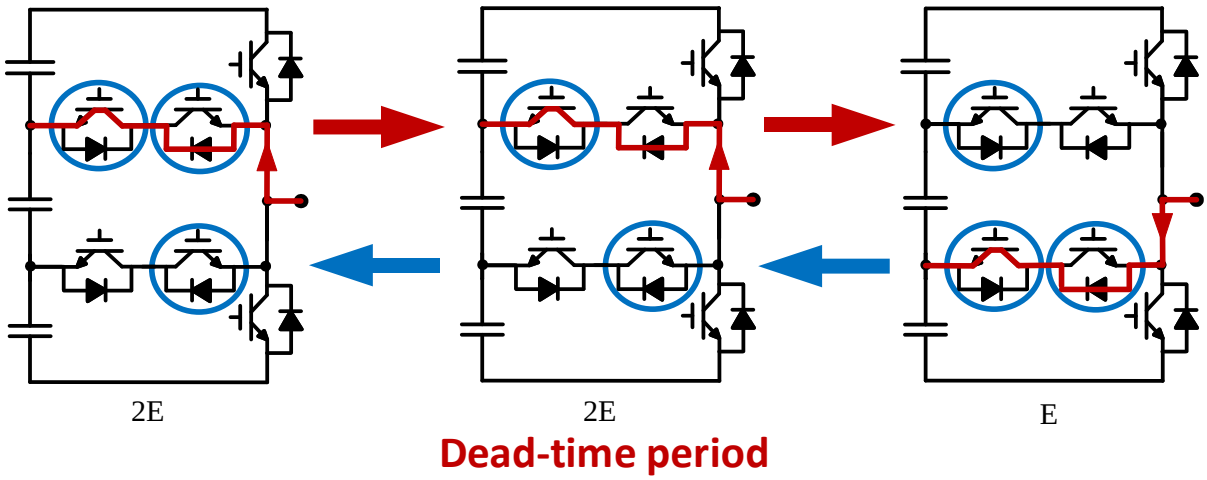
(a) 3E, 2E commutation when i_o>0



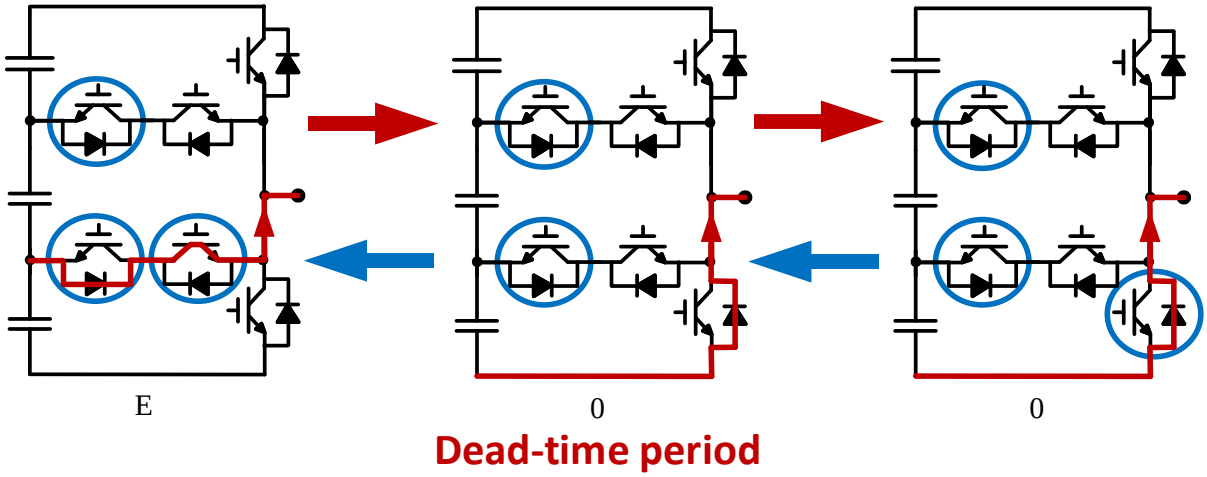
(b) 3E, 2E commutation when i_o<0



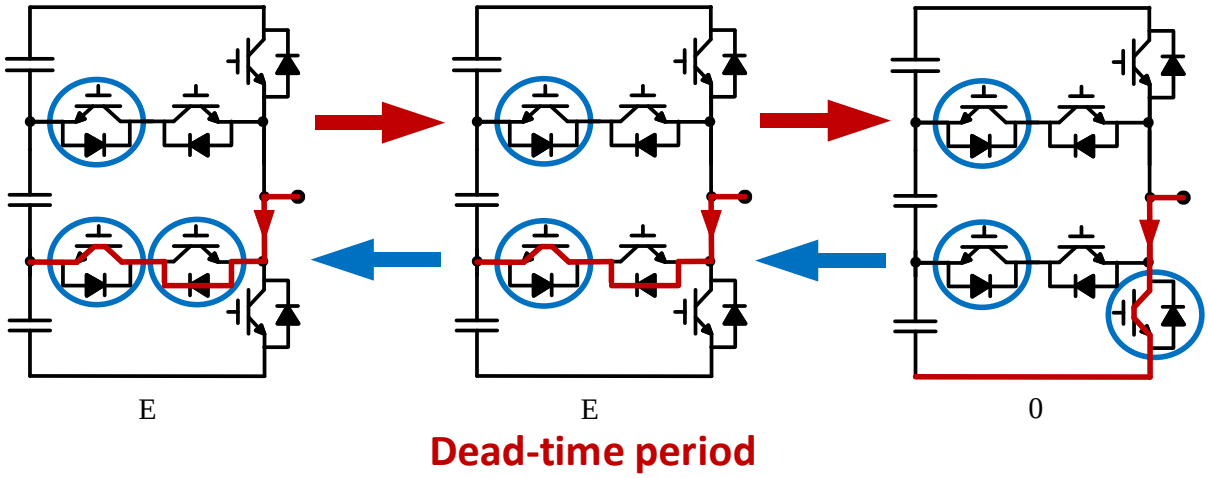
(c) 2E, E commutation when i_o>0



(d) 2E, E commutation when i_o<0



(e) E, 0 commutation when i_o>0



(f) E, 0 commutation when i_o<0

Figure 3.4 Commutation process of the four-level π-type converter with consideration of the dead-time effect

3.3 Switching devices voltage rating analysis

The general operation of the four-level π-type converter has been analyzed in section 3.2, and the switching truth table corresponding to each switching state has been summarized in Table III.I. It can be found out, unlike the standard two-level converter, switching devices voltage ratings of the multilevel converter such as the proposed four-level π-type converter are not the same for . Therefore, the switching device voltage rating analysis is necessary here in order to optimize the selection for switching devices. According to Table III.I as well as Fig.3.2, the appropriate devices selection for T1 to T6 can be analyzed as follows. The device blocking voltage can be analyzed with two aspects: steady state voltage and transient state voltage.

a) Steady State voltage

The steady state is with reference to each switching period. It means switching devices have finished switching actions, and keep in on or off state for specific period during each switching period. Generally, the steady state period is far more than the transient period. For the switching state as shown in Fig.3.2 (a) (e), T1, T3, T5 are in on-state, while T2, T4, T6 are in off-state. The phase-leg is clamped to the positive dc-link top point through T1, which results in an output voltage 3E. According to Kirchhoff's Voltage Law (KVL) as shown in Fig.3.5, under this condition, T2 has to hold 1/3 the total dc-link voltage (E), T4 has to hold 2/3 the total dc-link voltage (2E), and T6 has to withstand the whole dc-link voltage (3E).

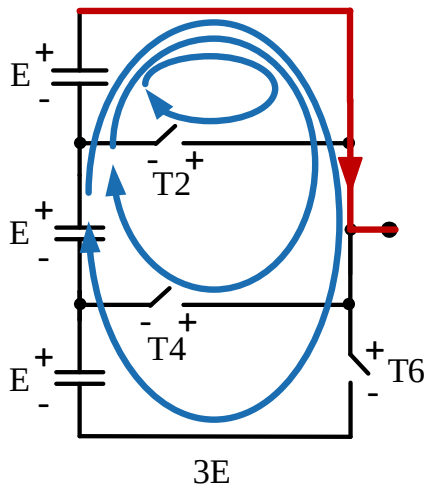


Figure 3.5 Devices blocking voltages during 3E

For the switching state 2E as shown in Fig.3.6, T2, T3, T5 are in on-state, while T1, T4, T6 are in off-state. In this situation, the phase-leg output terminal clamps to the upper NP (N2) through T2 and T3, which results in an output voltage 2E. T1 has to hold 1/3 the total dc-link voltage (E), T4 has to hold 1/3 1/3 the total dc-link voltage (E) as well, and T6 has to hold 2/3 the whole dc-link voltage (2E) at this stage.

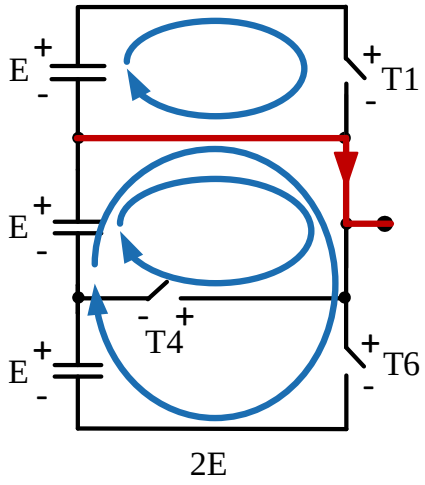


Figure 3.6 Devices blocking voltages during 2E

For the switching state as shown in Fig.3.7, T2, T4, T5 are in on-state, while T1, T3, T6 are in off-state. The phase-leg output terminal clamps to the lower NP (N1) through T4 and T5, which results in an output voltage E. T1 has to hold 2/3 the total dc-link voltage (2E), T3 has to hold 1/3 the total dc-link voltage (E), and T6 has to block 1/3 the total dc-link voltage (E) in this condition.

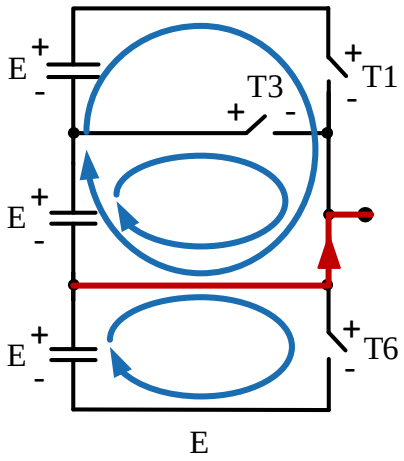


Figure 3.7 Devices blocking voltages during E

For the switching state as shown in Fig.3.8, T2, T4, T6 are in on-state, while T1, T3, T5 are in off-state.

The output terminal of the phase-leg clamps to the negative dc-link bottom point through T6, which results in an output voltage 0. T1 has to block the whole dc-link voltage (3E), T3 has to hold 2/3 the total dc-link voltage (2E), while T5 has to hold 1/3 the total dc-link voltage (E).

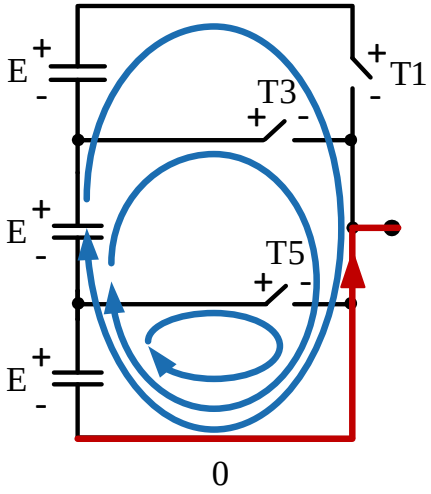


Figure 3.8 Devices blocking voltages during 0

According to the analysis above, in the static state, T1 and T6 have to withstand the whole dc-link voltage (3E). T3 and T4 need to hold 2/3 of the dc-link voltage (2E). T2 and T5 have to hold 1/3 of the dc-link voltage (E).

b) Transient state voltage

The transient state is a dynamic switching process when a switching device switching from the on-state to the off-state, and vice versa. During each pair of the complimentary devices switching on and off, the converter output voltage jumps between adjacent voltage levels. For the four-level π-type converter, if the modulation index is high enough, the output phase voltage contains four voltage levels. Therefore, the voltage difference between each adjacent voltage level is E. Consequently, the ideal switching voltage for each switching device of the four-level π-type converter during the transient is E. For example, when commutating between 3E and 2E, T1 and T2 are the complimentary devices switching on and off. During 3E switching state as shown in Fig.3.5, voltages on T1 and T2 are 0V and E respectively. During 2E switching state as shown in Fig.3.6, voltages on T1 and T2 are E and 0V respectively. Therefore, switching voltages on T1 and T2 are both E, which proves the above analysis.

In a practical PCB circuit or any other format converter circuit, the distance between dc-link capacitors

and switching devices may not be ideally zero. Meanwhile, the practical copper path, the capacitor as well as the switching device itself contain parasitic inductance. Fig.3.9 presents the simplified phase-leg structure of the four-level π-type converter with parasitic inductance.

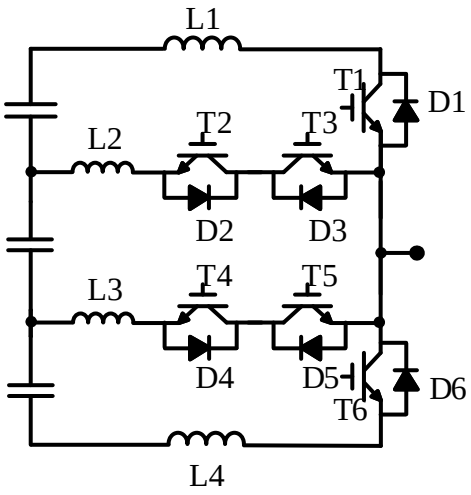


Figure 3.9 Simplified phase-leg structure of the four-level π-type converter with parasitic inductance

During the commutation transient process, the current of the switching device is relatively large, which will cause the induced voltage of the circuit parasitic inductance. Therefore, apart from the ideal switching voltage, the induced voltage on the parasitic inductance will also affect the actual blocking voltage on the switching device during the commutation transient process. Fig.3.10 presents the turn-off process of the collector current and the collector-emitter voltage of the IGBT. When an IGBT abruptly turns off, the trapped energy in the circuit parasitic inductance will continue against the current change in the circuit, causing a voltage overshoot ($V_{\text{parasitic}}$) across the IGBT as shown in Fig.3.10. The magnitude of the induced voltage on the parasitic inductance is proportional to the amount of the parasitic inductance and the rate of the current fall. This can be expressed in (3.4)

$$V_{\text{parasitic}} = -L\frac{di}{dt} \tag{3.4}$$

(3.4) indicates the induced voltage of the parasitic inductance depends on the rate of the current change as well as the value of parasitic inductance, and always opposes the direction of the current change.

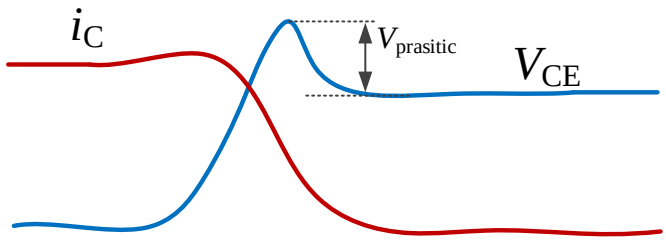


Figure 3.10 Turn-off process of the collector current and the collector-emitter voltage

However, exactly values of the parasitic inductance in different commutation loops are different and hard to measure. Therefore, the value of the induced voltage of the parasitic inductance plus the ideal switching voltage ($V_{parasitic} + V_{sw}$) for each switching device can be assumed to be equal to the blocking voltage during the transient state for each switching device. This is the reason that the rated voltage for the switching device of the traditional two-level converter has to be generally 2 times the dc-link voltage in order to leave an enough margin for the parasitic inductance induced voltage plus the switching voltage. For a four-level π-type converter, the device rated voltage can be reduced because of the lower switching voltage.

For low voltage applications, take a 600V dc-link voltage application for example. According to the analysis above, during the static period, T1 needs to withstand the whole dc-link voltage 600V. While during the commutation process 3E to 2E, the voltage across T1 during the switching transient will be the sum of the switching voltage E (200V) and the induced voltage from the parasitic inductance. In summary, T1 has to hold 600V in static, while 200V plus the induced voltage of parasitic inductance during the commutation (e.g. < 600V). Therefore, 900V super-junction MOSFETs or 1200V IGBT/MOSFET are both suitable for this purpose. It is the same for T6 as T1 and T6 are in the symmetrical positions in the phase-leg configuration. Similarly, T3 and T4 have to hold 400V in static, while 200V plus the induced parasitic voltage (<400V) during the commutation. 600V IGBTs or MOSFETs can be employed. For T2 and T5, they have to block 200V in static, while 200V plus the induced parasitic voltage (<200V) during the commutation. Therefore, 400V switches can be employed. Table III.II summarizes the candidate devices types with the minimum device voltage rating for the four-level π-type converter phase-leg based a 600V dc-link voltage application.

TABLE III.II. APPROPRIATE SWITCHING DEVICES VOLTAGE RATINGS AND CANDIDATE DEVICES

	T1, T6	T3, T4	T2, T5
Minimum device voltage rating	900V	600V	400V
Candidate devices	1200V IGBT or 900V MOSFET	600V IGBT/MOSFET	600V IGBT or 400V MOSFET

3.4 Topology comparison between four-level π-type converter, three-level T-type converter, three-level diode NPC converter, and two-level converter

In this section, topology characteristics of the four-level π-type converter and the three-level T-type converter, the three-level diode NPC converter, as well as the two-level converter have been compared. Practically, for three-level converters, there exist alternatives such as active NPC three-level converters [172], three-level FC converters [5], or the more complex three-level split-inductor converters [173] and three-level matrix converters [5], for four-level converters there exist alternatives such as four-level NPC converters [50], four-level FC converters [93]. However, considering the popularity in the industry as well as the low voltage application tendency, the selected three-level T-type converters and three-level diode NPC converters are more competitive and worthy to take into the comparison.

3.4.1 Layout characteristics comparison between four-level π-type converter, three-level T-type converter, three-level diode NPC converter, and two-level converter

Fig.3.11 presents the phase-leg structure of the four-level π-type converter, the three-level T-type converter, the three-level diode NPC converter, and the two-level converter.

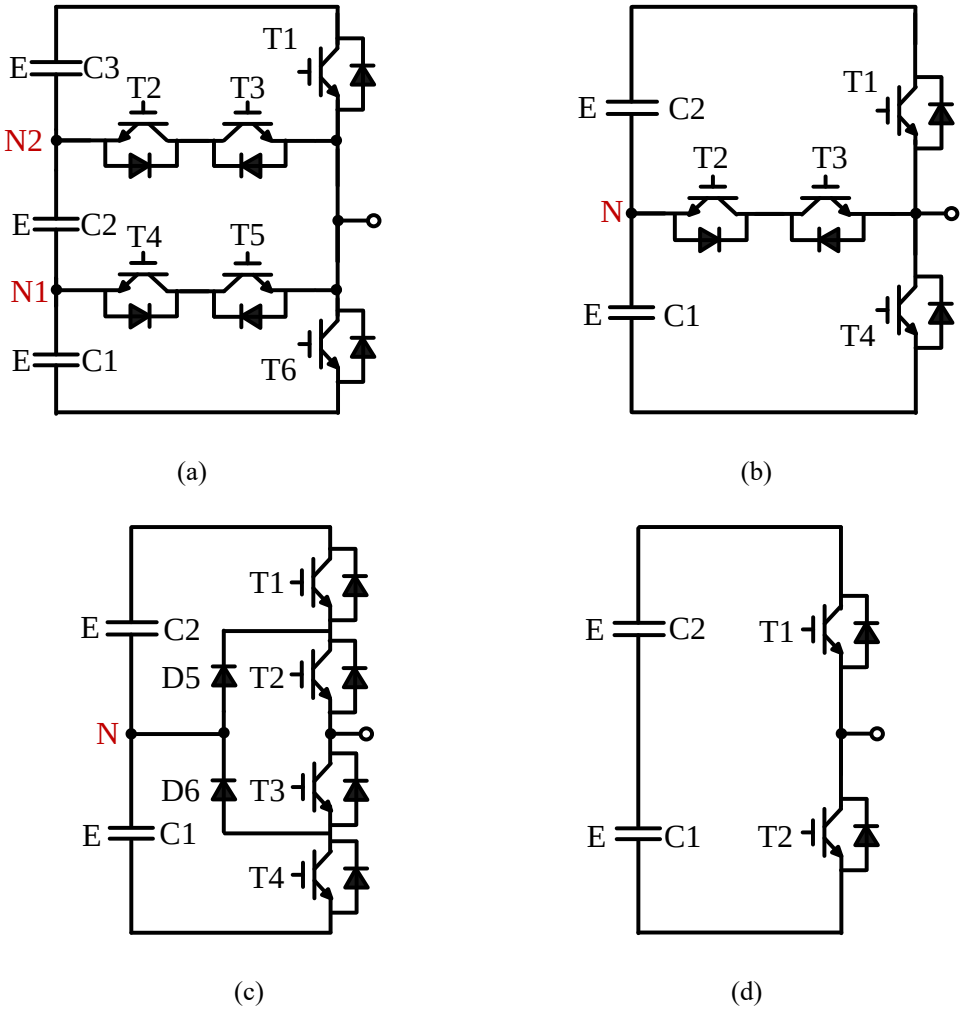


Figure 3.11 Phase-leg structures: (a) four-level π-type converter, (b) three-level T-type converter, (c) three-level diode NPC converter, (d) two-level converter

Fig.3.11 intuitively presents phase-leg structures of these four types of converter topologies. According to the literature introduction in section 2.2, and take a 600V dc-link input voltage as the example, topology characteristics comparisons have been summarized in Table III.III and Table III.IV.

TABLE III.III. TOPOLOGY CHARACTERISTICS COMPARISON A

Topology / Parameter	Four-level π-type converter	Three-level T-type converter	Three-level diode NPC converter	Two-level converter
NO. of voltage levels	4	3	3	2
NO. of IGBTs each phase-leg	6	4	4	2
NO. of clamping diodes each phase-leg	0	0	2	0
NO. of separate dc-link voltage sources for open loop systems	3	2	2	1
NO. of switching states	4	3	3	2
Min NO. of isolated gate driver supply for single phase-leg	4	3	4	2
Min NO. of isolated gate driver supply for three-phase	6	5	10	4

TABLE III.IV. TOPOLOGY CHARACTERISTICS COMPARISON B

Topology / Parameter	Four-level π-type converter	Three-level T-type converter	Three-level diode NPC converter	Two-level converter
NO. of 1200V IGBTs	2	2	0	2
NO. of 600V IGBTs	4	2	4 + 2 diodes	0
Switching voltage	200V	300V	300V	600V

Through the initial layout characteristics comparison above, the main advantage of the four-level π-type converter is the lower switching voltage, which can lead to the lower voltage stress on each switching device. This allows to use lower voltage rating devices and reduce the switching loss at the same time. However, consider of the number of switching devices, the number of the dc-link voltage sources, and the number of the isolated gate driver supplies, the three-level converter as well as the two-level converter show the advantage over the four-level π-type converter.

3.4.2 Operation comparison between four-level π-type converter, three-level T-type converter, three-level diode NPC converter, and two-level converter

Considering the traditional level shifted CB-PWM, for the two-level converter, only one carrier wave is required to interact with the modulation wave to determine the turn-on and turn-off state of the complimentary devices of the phase-leg. For the three-level T-type converter and three-level diode NPC

converter, two level shifted carrier waves are required to interact with the modulation wave to determine two pairs of complimentary devices of the phase-leg. For the four-level π-type converter, three level shifted carrier waves are required to interact with the modulation wave to determine three pairs of complimentary devices of the phase-leg.

In order to operate the simulation, the Simulink toolbox integrated in the MATLAB has been selected as the operation platform. Operational verification simulations have been implemented on these four topologies, respectively. Table III.V to Table III.VII list the simulation models setup parameters for the three-phase two converter, the three-phase three-level NPC converter, the three-phase three-level T-type converter, and the three-phase four-level π-type converter, respectively. The modulation indices for all four topologies are set to 0.95 as the modulation wave used in all simulations are purely sinusoidal. The screen shots of the Matlab/Simulink simulation models for all four topologies are shown in Appendix B.

The purpose of this group of simulations is to validate the operation of each topology listed in Fig.3.11. Therefore, the simulation models are proposed to be established as practical as possible. The Solver of the simulation models are selected as discrete, and Zero-order Hold is employed in order to imitate the ADC sampling process of the practical circuit. The Internal resistance Ron is selected as the default value 0.01 in order to make it similar to a practical IGBT. The snubber resistance and capacitance are selected as the default.

TABLE III.V THREE-PHASE TWO-LEVEL CONVERTER SYSTEM SIMULATION PARAMETERS

Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs in powergui
Zero-Order Hold sample time	100 μs
Sinusoidal fundamental signals generator model for the inverter	Sine Wave (Sine type: Time based, Time(t): Use simulation time, Frequency=100π rad/s (50Hz), Phase=[0, 2/3π, -2/π3] rad, Sample time=0)
Triangular carrier wave generator model for the inverter	Repeating table (frequency = 10 kHz)
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, C=2000μF, cap initial voltage =600V)
DC-link parallel protection resistors model	Series RLC Branch (Branch type: R, resistance value: 100kΩ)
DC voltage supply model	DC Voltage Source (Amplitude=600V)
Inverter side load model	Three-Phase Series RLC Branch (Branch type: RL, Resistance=25Ω, Inductance=5mH)

TABLE III.VI THREE-PHASE THREE-LEVEL DIODE NPC AND T-TYPE CONVERTERS SYSTEM SIMULATION PARAMETERS

Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs in powergui
Zero-Order Hold sample time	100 μs
Sinusoidal fundamental signals generator model for the inverter	Sine Wave (Sine type: Time based, Time(t): Use simulation time, Frequency=100π rad/s (50Hz), Phase=[0, 2/3π, -2/π3] rad, Sample time=0)
Triangular carrier wave generator model for the inverter	Repeating table (frequency = 10 kHz)
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, C=2000μF, cap initial voltage: C1=C2=300V)
DC-link parallel protection resistors model	Series RLC Branch (Branch type: R, resistance value: 100kΩ)
DC voltage supply model	DC Voltage Source * 2 (in series, Amplitude=300V)
Inverter side load model	Three-Phase Series RLC Branch (Branch type: RL, Resistance=25Ω, Inductance=5mH)

TABLE III.VII THREE-PHASE FOUR-LEVEL Π-TYPE CONVERTERS SYSTEM SIMULATION PARAMETERS

Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs in powergui
Zero-Order Hold sample time	100 μs
Sinusoidal fundamental signals generator model for the inverter	Sine Wave (Sine type: Time based, Time(t): Use simulation time, Frequency=100π rad/s (50Hz), Phase=[0, 2/3π, -2/π3] rad, Sample time=0)
Triangular carrier wave generator model for the inverter	Repeating table (frequency = 10 kHz)
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, C=2000μF, cap initial voltage: C1=C2=C3=200V)
DC-link parallel protection resistors model	Series RLC Branch (Branch type: R, resistance value: 100kΩ)
DC voltage supply model	DC Voltage Source * 3 (in series, Amplitude=200V)
Inverter side load model	Three-Phase Series RLC Branch (Branch type: RL, Resistance=25Ω, Inductance=5mH)

Fig.3.12 shows simulation output waveforms based on open loop systems of the two-level converter, the three-level diode NPC converter, the three-level T-type converter as well as the four-level π-type converter with simulation parameters shown in Table III.V to Table III.VII.

As mentioned above, the reason this simulation is carried out with Simulink as well as the above parameters is to simulate the practical prototypes operations in order to get a reasonable prediction for converter prototypes. Considering the switching device internal resistor, the zero-order hold blocks as

well as deadtime, the operation comparison between difference converter topologies can be more practical and convincing. And all simulation topologies have been converted to the discretization system, and are supplied with the same input voltage as well as the same load condition to make the comparison more reasonable. And one thing needs to be mentioned here is the simulation parameters setting will be used for the practical prototypes test in Chapter 4.

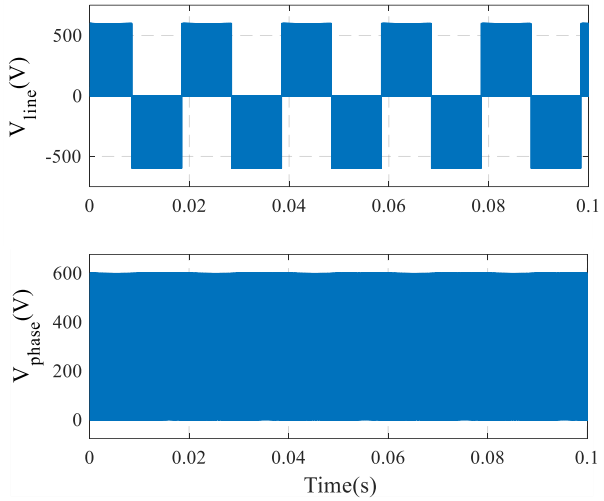
Fig.3.12 (a) (b) show operation waveforms of the two-level converter. The phase A output phase voltage is with reference to the negative bottom point of the dc-link, which only jumps between 600V and 0V as shown in the bottom figure of Fig.3.12 (a). Meanwhile, the output line voltage has three levels as shown in the top figure of Fig.3.12 (a). Three-phase sinusoidal output currents are shown in Fig.3.12 (b).

Fig.3.12 (c) (d) show operation waveforms of the three-level diode NPC converter. Due to the two dc-link NP clamping diodes (as shown in Fig.3.11 (c)), the phase A output phase voltage has three levels as shown in the bottom figure of Fig.3.12 (c). Meanwhile, the output line voltage has five levels as shown in the top figure of Fig.3.12 (c). Three-phase sinusoidal output currents are shown in Fig.3.12 (d). It can be noted that the current waveform line in Fig.3.12 (b) is bolder than that in Fig.3.12 (d), which indicates the high frequency harmonics in the output current of the three-level converter is less than that of the two-level converter.

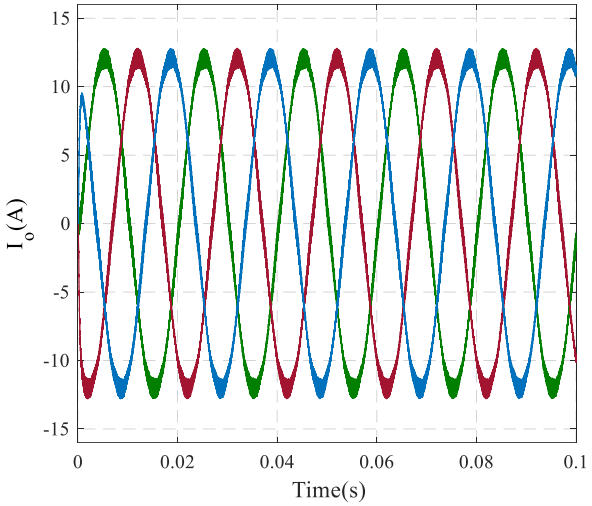
Fig.3.12 (e) (f) show operation waveforms of the three-level T-type converter. Similar to the three-level diode NPC converter, the back-to-back IGBT connected neutral path enables the three-level T-type converter to output three levels at its phase voltage as shown in the bottom figure of Fig.3.12 (e). The output line voltage also has five levels as shown in the top figure of Fig.3.12 (e). Three-phase sinusoidal output currents are shown in Fig.3.12 (f). Due to the same modulation technique as well as the same output voltage level, the current waveform line of the T-type converter is as bold as that of the three-level diode NPC converter.

Fig.3.12 (g) (h) show operation waveforms of the four-level π-type converter. Due to the two back-to-back IGBT connected neutral paths, the phase A output voltage has four level as shown in the bottom figure of Fig.3.12 (g). The output line voltage has seven levels as expected as shown in the top figure of Fig.3.12 (g). Three-phase sinusoidal output currents are shown in Fig.3.12 (h). It can be noticed that

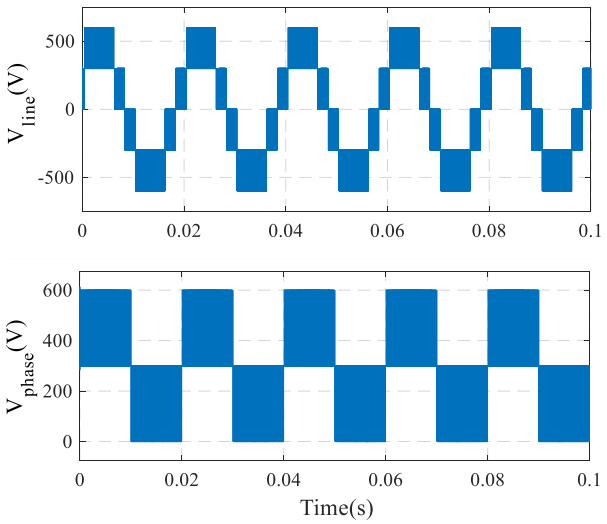
the current waveform line of Fig.3.12 (h) is less bold than those in Fig.3.12 (d) and (f), which indicates the high frequency harmonics in the output current of the four-level converter is further less than that of the three-level converter.



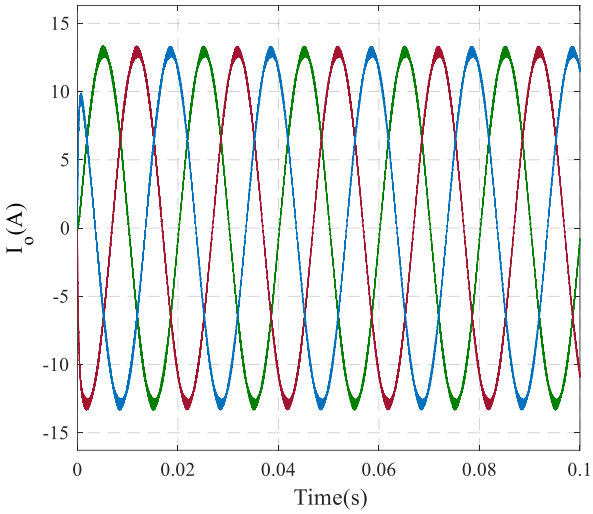
(a) Output voltages



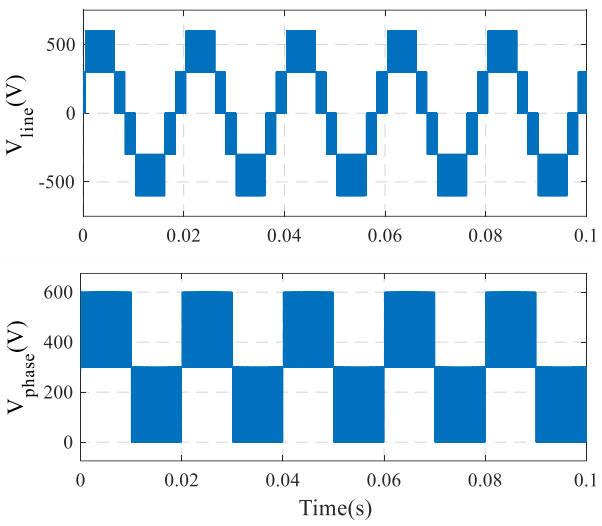
(b) Output currents



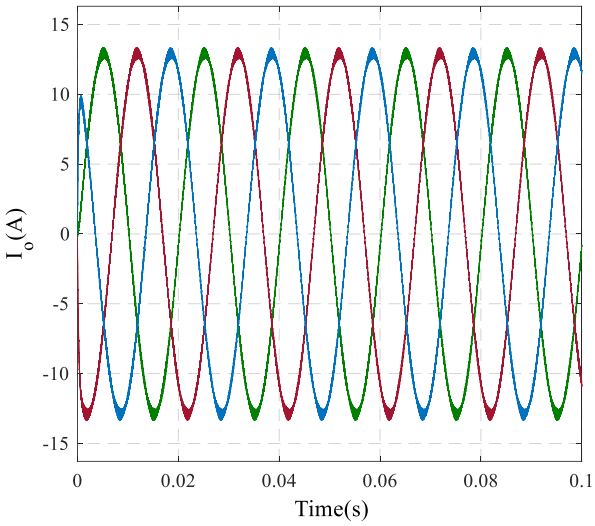
(c) Output voltages



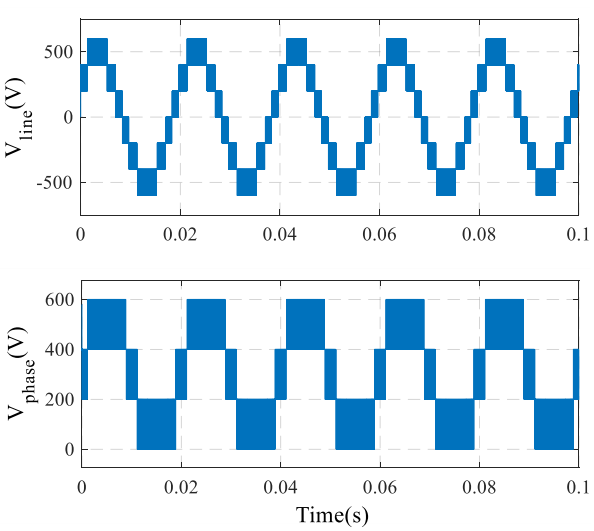
(d) Output currents



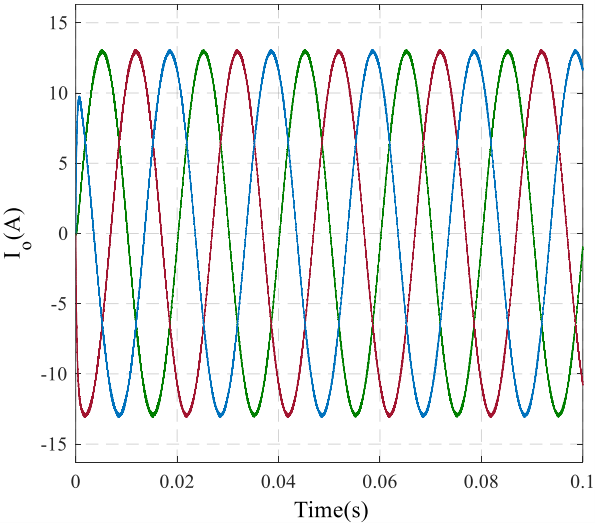
(e) Output voltages



(f) Output currents



(g) Output voltages



(h) Output currents

Figure 3.12 Simulation waveforms of (a) (b): two-level converter, (c) (d): three-level NPC converter, (e) (f): three-level T-type converter, (g) (h): four-level π-type converter

Fig.3.13 shows the corresponding simulation output harmonic analysis through the Fast Fourier Transform (FFT) in MATLAB for open loop systems of the two-level converter, the three-level diode NPC converter, the three-level T-type converter, and the four-level π-type converter.

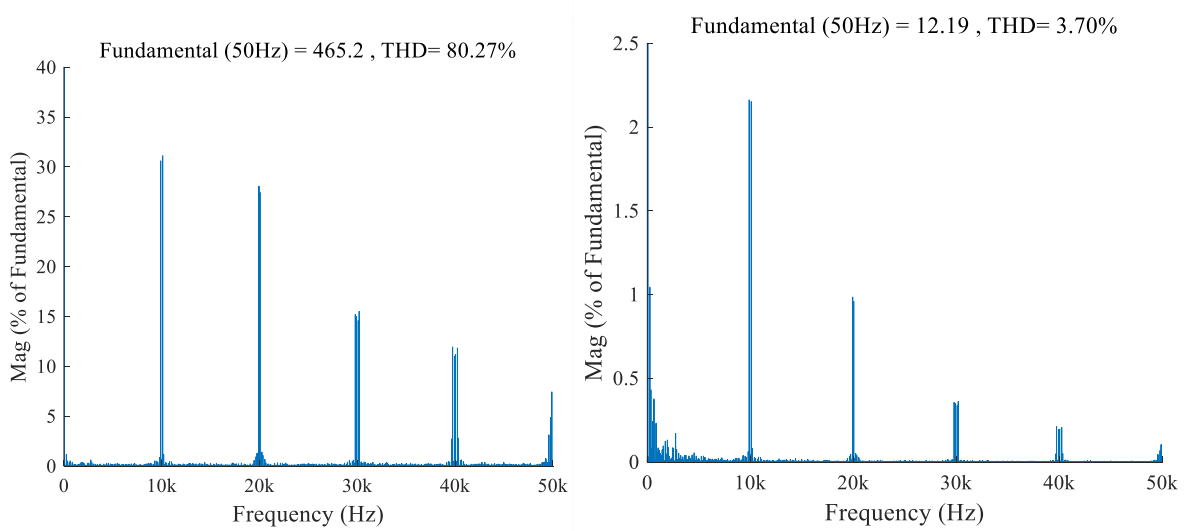
Fig.3.13 (a) (b) show harmonic spectrums of the line voltage and the output current for the two-level converter, respectively. The THD of the line voltage is relatively large due to only three levels at the output line voltage. The THD of the output current is 3.7%, which is much less than that of the voltage

THDs due to the 5mH output inductor adopted.

Fig.3.13 (c) (d) show harmonic spectrums of the line voltage and the output current for the three-level diode NPC converter, respectively. The THD of the line voltage in Fig.3.13 (c) is now 37.53%, less than half of the THD of the line voltage for the two-level converter in Fig.3.13(a). It is due to the two more voltage levels on line voltages compare to that of the two-level converter. Therefore, the THD of the current for the three-level diode NPC converter in Fig.3.13 (d) is less than half of the current THD of the two-level converter as shown in Fig.3.13(b). It proves the advantage that in order to get the same output harmonic level, the output filter of the three-level converter can be much smaller.

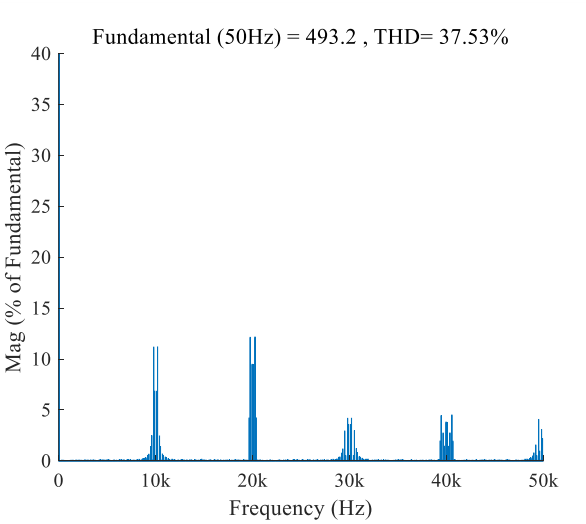
Fig.3.13 (e) (f) present harmonic spectrums of the line voltage and the output current for the three-level T-type converter, respectively. With the same output voltage levels, the THD of the line voltage as well as the current of the three-level T-type converter are almost the same to the ones of the three-level diode NPC converter.

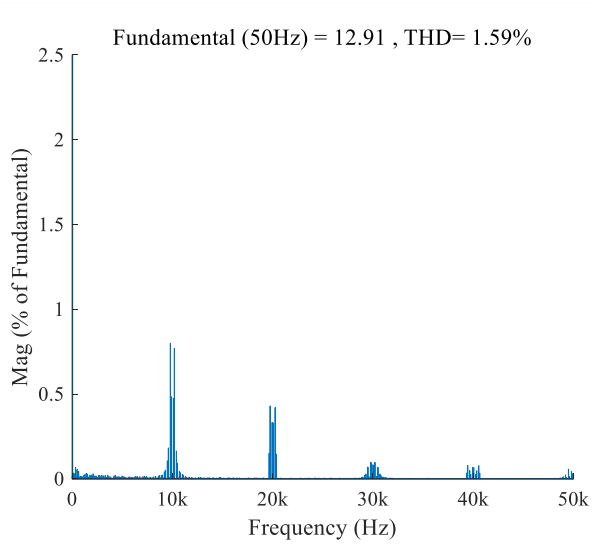
Fig.3.13 (g) (h) present harmonic spectrums of the line voltage and the output current for the four-level π-type converter, respectively. Due to even more line voltage levels, the THD of the line voltage in Fig.3.13 (g) is now 24.09%, which almost 2/3 of the THD of the line voltage for three-level converters as shown in Fig.3.13 (c) (e). Meanwhile, the THD of the current for the four-level π-type converter further reduces compares with the current THD of three-level converters. It proves that to get the same output harmonic level, the output filter of the four-level converter can be further reduced compares to the three-level converter.



(a) Line voltage

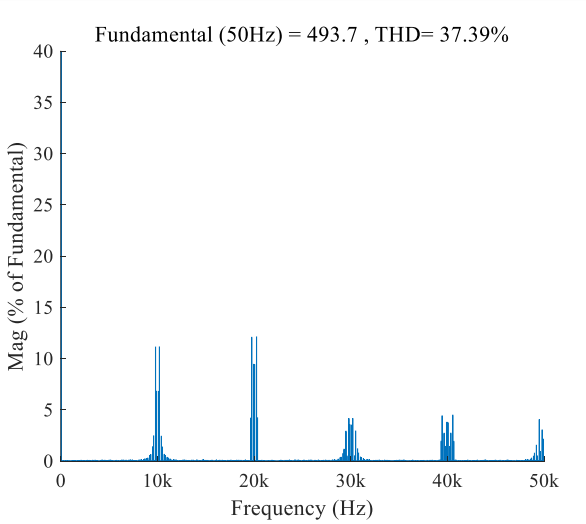
(b) Output current

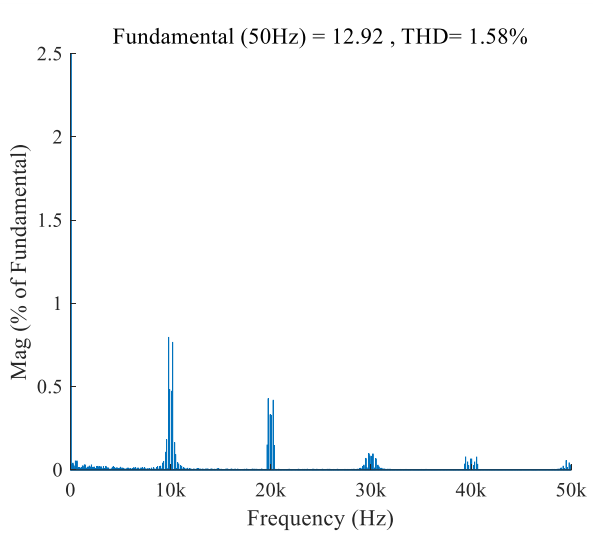




(c) Line voltage

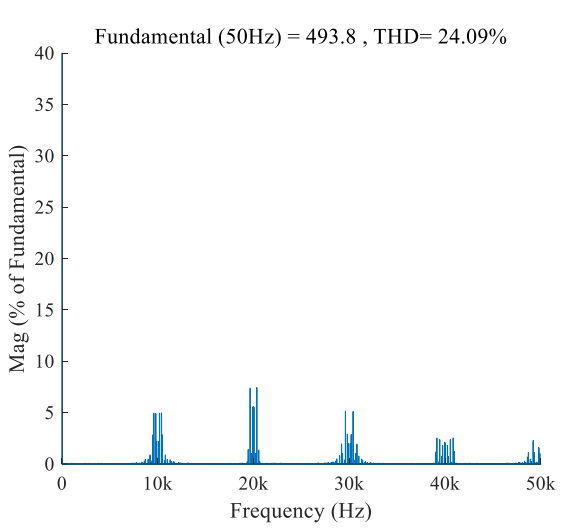
(d) Output current



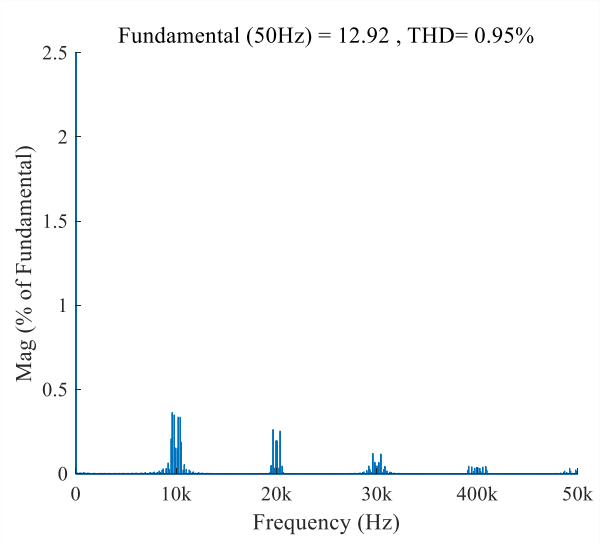


(e) Line voltage

(f) Output current



(g) Line voltage



(h) Output current

Figure 3.13 FFT analysis of simulation waveforms of (a) (b): two-level converter, (c) (d): three-level NPC converter, (e) (f): three-level T-type converter, (g) (h): four-level π-type converter

Through the phase-leg layout characteristic as well as the simulated operation comparison among these four topologies above, with the same input and load condition, disadvantages and advantages of the four-level π-type converter can be summarized as follow.

Disadvantages

- For the aspect of the number of switching devices: the switching devices number of the three-level T-type converter and the two-level converter are 33.33% less and 66.67% less than that of the four-level π-type converter, respectively. The number of switching devices of the three-level diode NPC converter is the same as the one of the four-level π-type converter due to the two clamping diodes.
- For the aspect of the minimum number of the isolated gate driver supplies for three-phase system, the number of the three-level T-type converter, and the two-level converter is 16.67% less, and 33.33% less than that of the four-level π-type converter, respectively.
- If open loop systems used, the four-level converter requires more separated dc-link voltage sources

Advantages

- For the aspect of the THD of output waveforms, THDs of the line voltage and the current of

the four-level π-type converter are 35.57% less, and 39.87% less than those of the two kinds three-level converters, respectively. While, THDs of the line voltage and the current of the four-level π-type converter are 70% less, and 74.32% less than those of the two-level converter, respectively.

- For the aspect of the switching voltage of switching devices, the switching voltage for the four-level π-type converter is 33.33% less, and 66.67% less than those for the three-level converter, and the two-level converter, respectively.

Even the tradeoff has been made between disadvantages and advantages of the four-level π-type converter. From the numerical comparison analysis above, and consider the compact system requirement for the low voltage applications such as electric vehicles, advantages still take the dominant position for the four-level π-type converter. And the separated dc-link voltage sources problem can also be resolved by employing the proposed dc-link NP voltages control strategy which will be introduced in Chapter 5.

3.5 Summary of Chapter 3

This chapter introduced and investigated the layout as well as basic modulation operations of the four-level π-type converter.

From the aspect of the configuration, the proposed four-level π-type converter consists of only 6 switching devices on each phase-leg. Two back-to-back connected neutral paths make the converter topology be able to output four voltage levels at the phase voltage. Compares to the three-level T-type converter, it only has two more switching devices on each phase-leg. Compares to the three-level diode NPC converter, it does not require clamping diodes. If the two switching devices in two neutral paths are common-collector connected, then there will be only two more gate driver supplies for the three-phase converter compares to the three-phase two-level converter topology. Therefore, the four-level π-type is less complexity compares to other four-level NPC converters.

From the aspect of the device voltage rating requirement, the switching voltage of each switching device on the proposed topology is only 1/3 of the total dc-link voltage, which allows it to employ the device with the lower block voltage rating compares to the three-level converter and the two-level converter.

Lower switching voltage can help to reduce the switching loss when the dc-link voltage is the same.

From the aspect of the output harmonics, this four-level π-type converter can be well operated with a traditional level shifted CB-PWM scheme. With the traditional level shifted CB-PWM, and the same input, load conditions, by taking the numerical comparison about the layout characteristics as well as the open loop operation performance among the two-level converter, the three-level diode NPC converter, the three-level T-type converter, as well as the four-level π-type converter, the four-level π-type converter demonstrates much lower output harmonic contents.

Therefore, the lower switching voltage, the comprised topology configuration complexity, and lower output harmonic contents make the four-level π-type converter as a qualified candidate for low voltage applications which require the compact and higher power density requirements.

4 Power loss analysis for the four-level π-type converter

4.1 Introduction

In chapter 3, topology characteristics, the switching device voltage rating feature, the operation based on initial modulation, as well as output harmonic contents have been analyzed and compared with existing popular NPC converters. Initial results in chapter 3 verified the proposed four-level π-type converter can be a qualified candidate for low voltage applications. Therefore, the next step is to systematically analyze the power loss situation for the four-level π-type converter based on the mathematical power loss model. Meanwhile, it is worth to compare the topology operation efficiency of the four-level π-type converter to other popular NPC converters and the two-level converter in order to verify the advantage of the proposed four-level topology. In this chapter, an average analytical power loss model has been established in order to investigate the power loss distribution as well as the operation efficiency of the four-level π-type converter. Based on the proposed average power loss model, the average power loss distribution of each individual switching device of the four-level π-type converter phase-leg can be calculated in order to investigate the power stress of each device under different operation modes. Apart from that, the total power converter output efficiency under different switching frequencies can be calculated in order to compare the efficiency characteristic of four-level π-type converter to other power converter topologies. The average analytical expressions of the proposed average power loss model can be varied according to the modulation wave shape. In this chapter the pure sinusoidal modulation has been used out of the simplification. A 3kW four-level π-type converter prototype has been established to verify the proposed power loss model. A 3kW two-level converter prototype with the same switching device (IGBT) has also been built to provide a practical efficiency comparison to the four-level π-type converter in order to validate the power loss advantage of the four-level π-type converter. Through the power loss model calculation, simulation as well as the test verification, the proposed power loss model calculated converter efficiency which matches well with practical experimental results. Meanwhile, the four-level π-type converter presents a lower total output loss compares to other three converters.

The work in this chapter has been published in [78], [115] by the author.

4.2 Average analytical power loss model establishment

In this chapter, the average analytical approach is adopted to analyze the power loss distribution of the four-level π-type converter. According to the literature review in section 2.3, the power loss of the switching device can split into two parts. One part is the conduction loss out of the power dissipation on the device conduction forward resistance. Another part is the switching loss due to the power consumption during the switching transient. And due to silicon co-packed IGBTs are selected as example switching devices in this thesis, the reverse recovery loss of the anti-parallel diode should be considered as well.

4.2.1 Average analytical model of conduction losses

Conduction losses occur when the conduction current is flowing through the switching device on-state resistance. Therefore, the instantaneous conduction power for any switching device in the phase-leg is shown in (4.1).

$$P_{con\_ins} = v_{CE} \cdot |i_c| \tag{4.1}$$

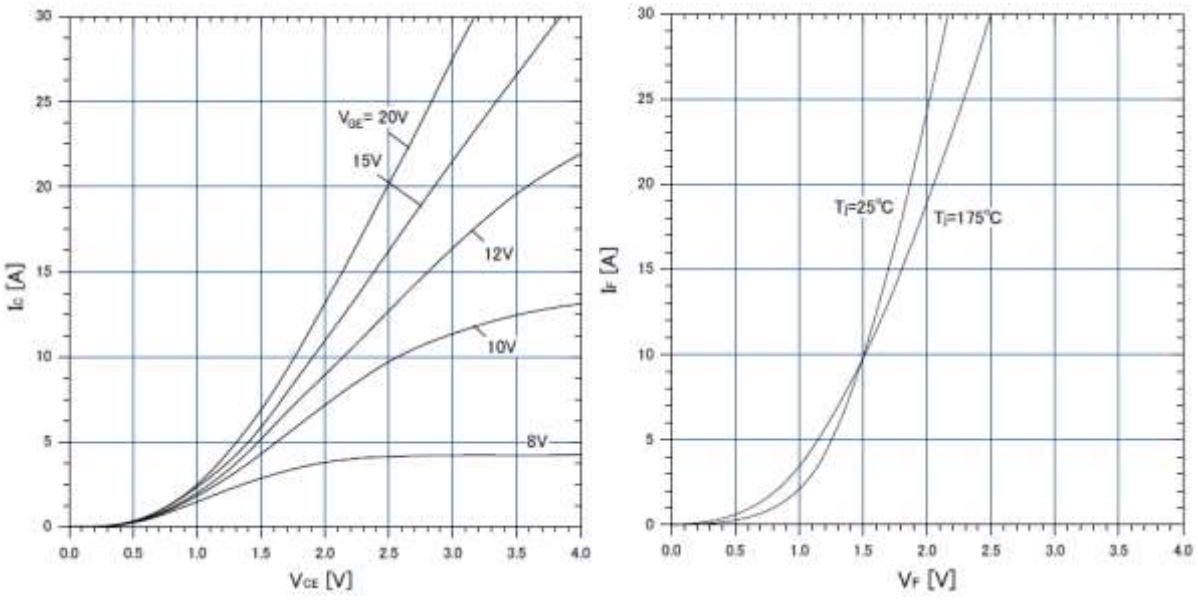
where, i_c is the IGBT collector conduction current or diode forward current. From the piecewise point of view, i_c can be deemed and expressed as the converter load current when corresponding devices are in on-state. Generally, for a sinusoidal PWM converter, the output load current is fundamentally sinusoidal and bidirectional. Therefore, the reason for using the absolute value of the device forward conducting current $|i_c|$ is that the forward conducting current of the on-state switching device should be always positive, regardless of the direction of the output load current. v_{CE} is the switching device forward conduction voltage drop. Fig. 4.1 (a) (b) show forward conduction voltage drops vs conduction collector/diode currents curves of the IGBT and anti-parallel diode of FGW15N120VD [174] under a 175℃ junction temperature. They both follow the exponential law. Generally, in most of the working range, the device forward conduction voltage drop increases linearly with the forward current increases. Therefore, for analysis simplification, v_{CE} can be expressed as a first order linear equation as shown in (4.2).

$$v_{CE} = V_{CE0} + r_{0T} \cdot |i_c| \tag{4.2}$$

where, V_{CE0} represents the equivalent IGBT on-state threshold voltage. r_{0T} represents the IGBT equivalent turn-on resistance. They can be derived by extending the linear region of the conduction voltage drop vs conduction collector current curve to get across the v_{CE} axis. Thus, the distance between the origin and the cross point on the v_{CE} axis is equal to V_{CE0}. The reciprocal of the gradient of the extended line is expressed as $\Delta v_{CE}/\Delta i_c$ which equals to r_{0T}. Fig. 4.1 (c) demonstrates this method for the IGBT intuitively, where the blue dash lines are extended lines of the linear region of the conduction voltage drop vs conduction collector current curves.

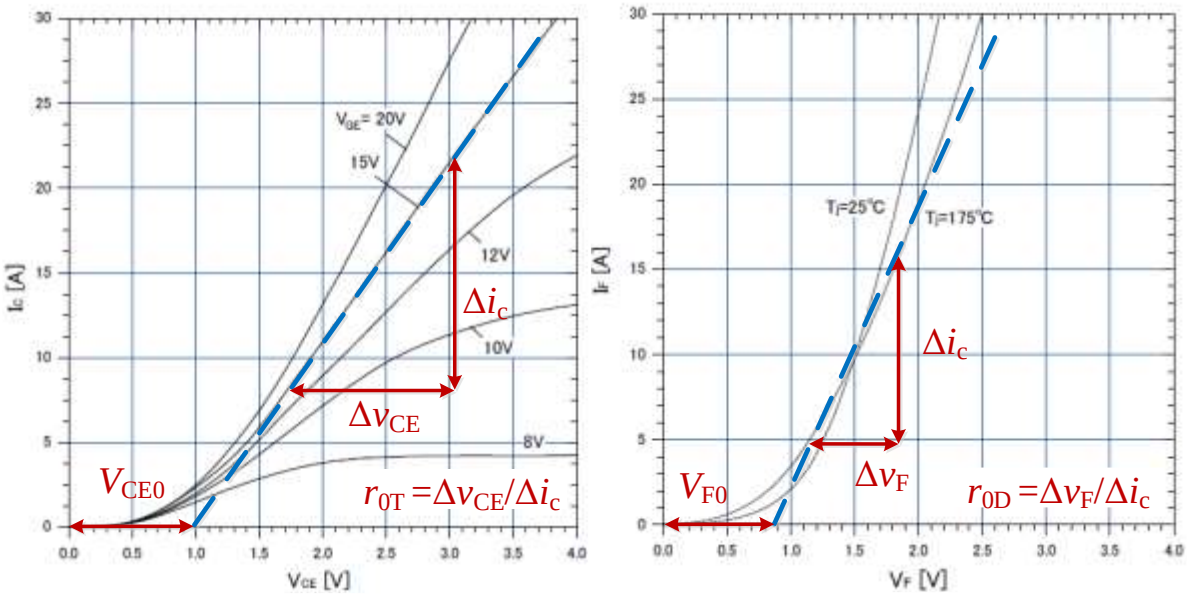
When current flows through the anti-parallel diode, the diode forward conduction voltage drop can be expressed by using the same principle as shown in (4.3). Fig. 4.1 (d) demonstrates the method to get the diode equivalent turn-on resistance r_{0D}, and the diode equivalent on-state threshold voltage V_{F0}.

$$v_F = V_{F0} + r_{0D} \cdot |i_c| \tag{4.3}$$



(a) IGBT

(b) Anti-parallel diode



(c) Conduction parameters derivation for IGBTs (d) Conduction parameters derivation for diodes

Figure 4.1 Curves of conducting collector/diode currents vs turn-on voltages of FGW15N120VD

It should be noticed that all curves and data should be taken at a high junction temperature condition (175℃), which is the worst case for consideration [108][109][175]. And the condition V_{GE}=15V curve is selected for IGBT is due to it is a typical gate driver voltage, and the gate-emitter voltage used for the test later will be 15V as well.

As mentioned before, for the sinusoidal PWM modulation method, when the frequency ratio is greater than 15 or so [25], the switching frequency is much larger than the fundamental frequency. In this case, with a proper output filter, the load current can be assumed as sinusoidal [25]. Therefore, i_c can be expressed as (4.4)

$$i_c = I_{CM}\sin(\omega t-\varphi) \tag{4.4}$$

where, I_{CM} is the load current peak value. φ is the power factor angle.

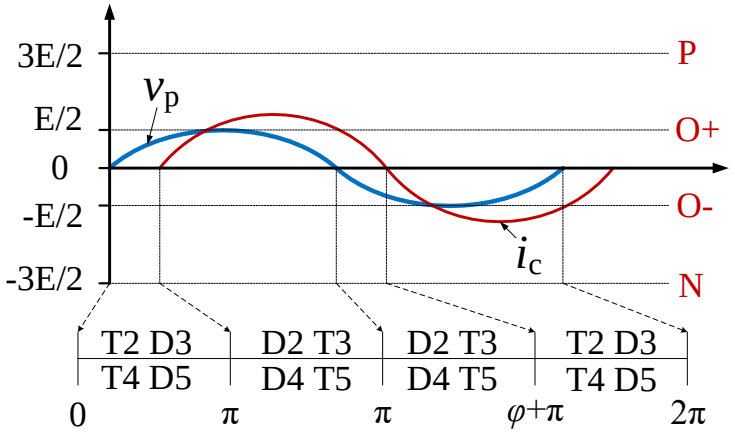
The average conduction loss of the IGBT over one fundamental cycle can be expressed as an integration formula in (4.5a) by combing (4.1) and (4.2). Similarly, the average conduction loss of the anti-parallel diode within one fundamental period can be expressed in (4.5b).

$$P_{con,T}=\frac{1}{2\pi}\int_{\theta_1}^{\theta_2} k\cdot\left[V_{CE0}\cdot|I_{CM}\sin(\omega t-\varphi)|+r_{0T}\cdot(I_{CM}\sin(\omega t-\varphi))^2\right]d\omega t \tag{4.5a}$$

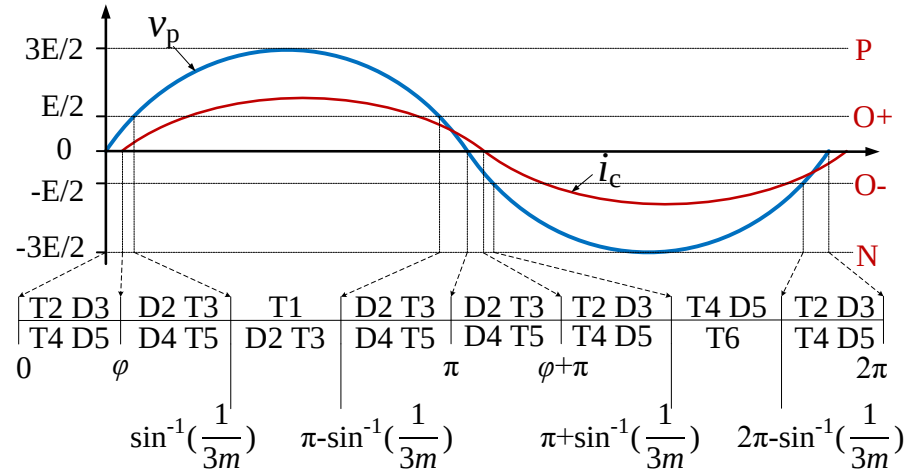
$$P_{con,D} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} k \cdot \left[V_{F0} \cdot |I_{CM} \sin(\omega t - \varphi)| + r_{0D} \cdot (I_{CM} \sin(\omega t - \varphi))^2 \right] d\omega t \quad (4.5b)$$

k represents the switching device conduction duty cycle which is the device on/off ratio. θ_2, θ_1 are integration boundaries depending on conduction intervals for switching devices. Devices on different positions on the converter topology may have different integration boundaries, as their corresponding conduction intervals are different. Therefore, due to the topology configuration as well as the CB-PWM being used, the on/off ratio k in (4.5) has different expressions in various regions which has been derived according to the method in [25]. The derivation of k will be described as follows.

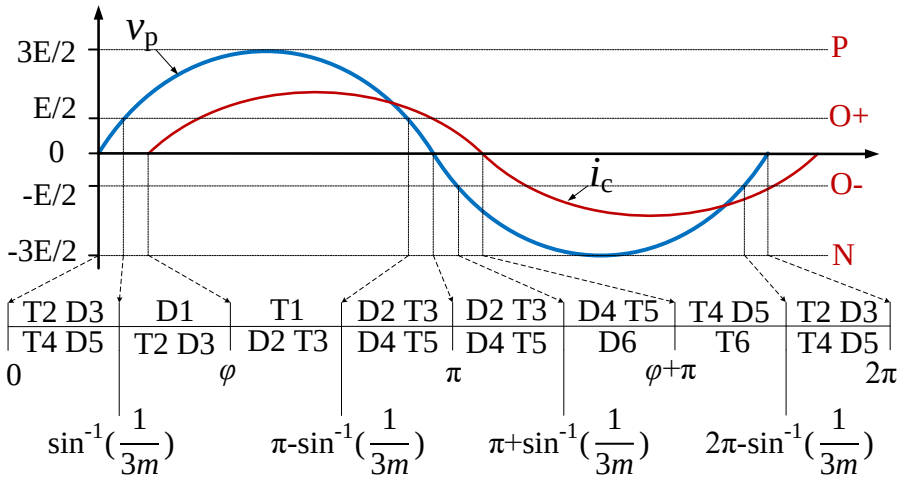
Assuming an inductive load, Fig.4.2 shows conduction intervals of switching devices with related to the converter output phase voltage fundamental component v_p (take the dc-link middle point as the reference point) and the converter output load current i_c for the four-level π-type converter with respect to the angle domain. Different modulation indices m and power factor angles φ can result different conduction intervals as shown in Fig.4.2 (a) (b) (c) (d), respectively. And the integration boundary (θ_2, θ_1) in (4.5a) or (4.5b) can be obtained from Fig.4.2. Assume the total dc-link voltage equals to 3E, and according to Table III.I in section 3.2, in Fig.4.2, the switching state P indicates the inverter output phase voltage v_p equals to 3E/2, T1 and T3, T5 are ON. O+ means v_p= E/2, T2, T3 and T5 are ON. O- means v_p= -E/2, T2, T4 and T5 are ON. And N indicates v_p= -3E/2, T2, T4 and T6 are ON.



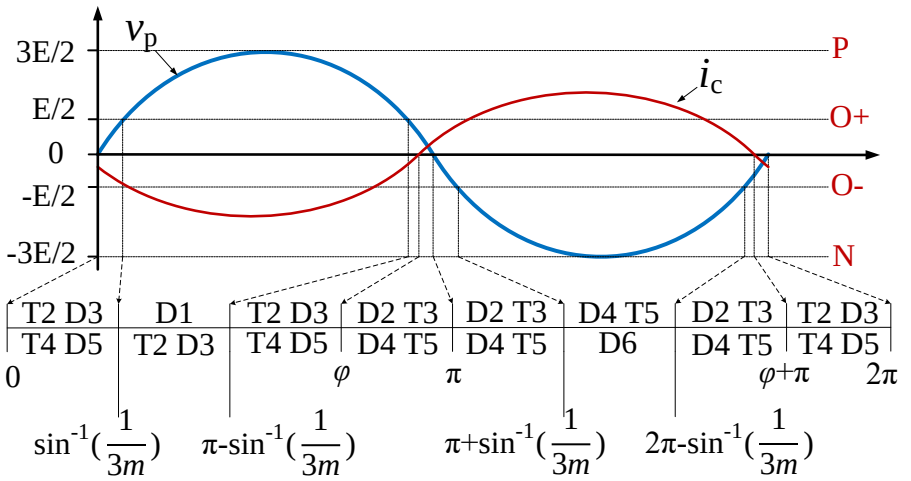
(a)



(b)



(c)



(d)

Figure 4.2 Conduction intervals for switching devices(a) $m \le \frac{1}{3}$. (b) $m > \frac{1}{3}$, $0 < \varphi \le \sin^{-1}(\frac{1}{3m})$. (c) $m > \frac{1}{3}$, $\sin^{-1}(\frac{1}{3m}) < \varphi < \pi - \sin^{-1}(\frac{1}{3m})$. (d) $m > \frac{1}{3}$, $\pi - \sin^{-1}(\frac{1}{3m}) \le \varphi < \pi$.

Assume the sinusoidal modulation, Fig.4.2 (a) presents the situation when the modulation index is less than 1/3. Assume the waveform of output phase voltage fundamental component v_p=sin(θ), then the current waveform is i_c=sin(θ-φ). With this situation, when the level-shifted CB-PWM is adopted as shown in Fig.3.3, the modulation wave always below the upper carrier wave and over the bottom carrier wave. Therefore, T1 is always in off-state, while T6 is always in off-state as well, which means T1, T6, D1, D2 will neither switch nor conduct at all according to Table III.I. During one fundamental period, the current only flows through T2, T3, T4, T5, D2, D3, D4, D5. Under this situation, the converter output phase voltage only has two voltage levels, therefore, the converter is equivalent to a two-level converter.

Fig.4.2 (b) presents the situation when the modulation index is larger than 1/3. Meanwhile the power factor angle is large 0 but less than $\sin^{-1}(\frac{1}{3m})$. Under this situation, the converter is able to output the phase voltage with four voltage levels. Please note, the angle $\sin^{-1}(\frac{1}{3m})$ is an important angle value. The relationship between $\sin^{-1}(\frac{1}{3m})$ and the power factor angle φ will determine conduction intervals and switching intervals of each switching device even the modulation index *m* is the same.

Fig.4.2 (c) presents the situation when the modulation index is larger than 1/3. And the power factor angle is larger than $\sin^{-1}(\frac{1}{3m})$ but less than $\pi-\sin^{-1}(\frac{1}{3m})$. Even in this situation the converter works as a four-level converter, however, devices conduction intervals are different compare to Fig.4.2 (b) due to different power factor angles. For example, D1 doesn't conduct at all in Fig.4.2 (b), but does conduct in Fig.4.2 (c) in the region $[\sin^{-1}(\frac{1}{3m}), \varphi]$. For the four-level π-type converter, there're three commutation regions P~O+, O+~O-, O-~N. With a sufficient large modulation index, current directions in different commutation regions will result in devices switching on and off differently.

Fig.4.2 (d) presents the situation when the modulation index is larger than 1/3. And the power factor angle is larger than $\pi-\sin^{-1}(\frac{1}{3m})$ but less than π. This situation is close to a rectifier operation, where the v_p and i_c are nearly out of phase. This situation should still be taken into consideration when establish the power loss model and calculate the efficiency.

Devices conduction intervals have been summarized in Table IV.I, Table IV.II, Table IV.III, Table IV.IV.

TABLE IV.IV. $M \leq \frac{1}{3}$

Device	Conduction intervals
T1, T6	Null
D1, D6	Null
T2, T5	$[0, \varphi]$, $[\pi+\varphi, 2\pi]$
D2, D5	$[\varphi, \pi+\varphi]$
T3, T4	$[\varphi, \pi+\varphi]$
D3, D4	$[0, \varphi]$, $[\pi+\varphi, 2\pi]$

TABLE IV.II $M > \frac{1}{3}$, $\Phi \leq \text{SIN}^{-1}(\frac{1}{3M})$

Device	Conduction intervals
T1, T6	$[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$
D1, D6	Null
T2, T5	$[0, \varphi]$, $[\pi+\varphi, \pi+\sin^{-1}(\frac{1}{3m})]$, $[2\pi-\sin^{-1}(\frac{1}{3m}), 2\pi]$
D2, D5	$[\varphi, \sin^{-1}(\frac{1}{3m})]$, $[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$, $[\pi-\sin^{-1}(\frac{1}{3m}), \pi+\varphi]$
T3, T4	$[\varphi, \sin^{-1}(\frac{1}{3m})]$, $[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$, $[\pi-\sin^{-1}(\frac{1}{3m}), \pi+\varphi]$
D3, D4	$[0, \varphi]$, $[\pi+\varphi, \pi+\sin^{-1}(\frac{1}{3m})]$, $[2\pi-\sin^{-1}(\frac{1}{3m}), 2\pi]$

TABLE IV.III. $M > \frac{1}{3}$, $\text{SIN}^{-1}(\frac{1}{3M}) < \Phi < \Pi - \text{SIN}^{-1}(\frac{1}{3M})$

Device	Conduction intervals
T1, T6	$[\varphi, \pi - \sin^{-1}(\frac{1}{3m})]$
D1, D6	$[\sin^{-1}(\frac{1}{3m}), \varphi]$
T2, T5	$[0, \sin^{-1}(\frac{1}{3m})], [\sin^{-1}(\frac{1}{3m}), \varphi], [2\pi - \sin^{-1}(\frac{1}{3m}), 2\pi]$
D2, D5	$[\varphi, \pi - \sin^{-1}(\frac{1}{3m})], [\pi - \sin^{-1}(\frac{1}{3m}), \pi + \sin^{-1}(\frac{1}{3m})]$
T3, T4	$[\varphi, \pi - \sin^{-1}(\frac{1}{3m})], [\pi - \sin^{-1}(\frac{1}{3m}), \pi + \sin^{-1}(\frac{1}{3m})]$
D3, D4	$[0, \sin^{-1}(\frac{1}{3m})], [\sin^{-1}(\frac{1}{3m}), \varphi], [2\pi - \sin^{-1}(\frac{1}{3m}), 2\pi]$

TABLE IV.IV. $M > \frac{1}{3}$, $\Pi - \text{SIN}^{-1}(\frac{1}{3M}) \leq \Phi < \Pi$

Device	Conduction intervals
T1, T6	Null
D1, D6	$[\sin^{-1}(\frac{1}{3m}), \pi - \sin^{-1}(\frac{1}{3m})]$
T2, T5	$[0, \sin^{-1}(\frac{1}{3m})], [\sin^{-1}(\frac{1}{3m}), \pi - \sin^{-1}(\frac{1}{3m})], [\pi - \sin^{-1}(\frac{1}{3m}), \varphi], [\varphi + \pi, 2\pi]$
D2, D5	$[\varphi, \pi + \sin^{-1}(\frac{1}{3m})], [2\pi - \sin^{-1}(\frac{1}{3m}), \varphi + \pi]$
T3, T4	$[\varphi, \pi + \sin^{-1}(\frac{1}{3m})], [2\pi - \sin^{-1}(\frac{1}{3m}), \varphi + \pi]$
D3, D4	$[0, \sin^{-1}(\frac{1}{3m})], [\sin^{-1}(\frac{1}{3m}), \pi - \sin^{-1}(\frac{1}{3m})], [\pi - \sin^{-1}(\frac{1}{3m}), \varphi], [\varphi + \pi, 2\pi]$

Fig.4.3, Fig.4.4 and Fig.4.5 show different switching states according to the relative geometrical position between the modulation wave and the triangular carrier wave within one switching period T_s. As mentioned before, the large frequency index condition is employed in this chapter, therefore, switching period T_s is much less than the fundamental period T_o. Consequently, within a single carrier/switching period, the value of the modulation wave can be deemed as constant. Therefore, the modulation wave can be drawn as a horizontal straight line across the carrier wave during each carrier period as shown in Fig.4.3 to Fig.4.5. According to this assumption, the corresponding on/off ratio k can be derived by the essential mathematical analysis of the geometrical triangle proportional relation

between the modulation wave and the carrier wave. Detailed analysis shows as follows.

(a) P~O+ region

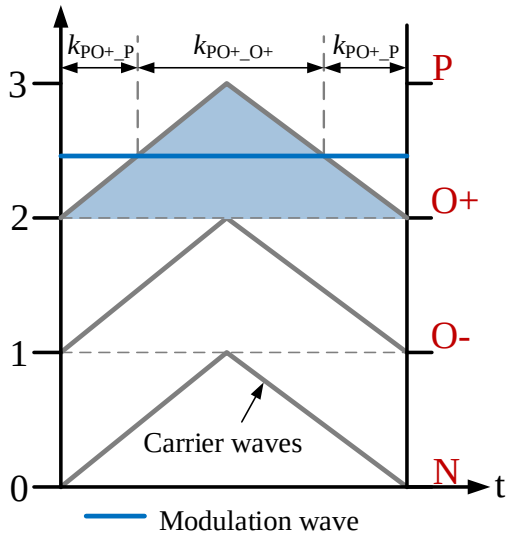


Figure 4.3 The switching state when the modulation wave between P and O+ (P ~ O+ commutation)

Take Fig.4.3 for example, it shows the condition when the commutation happens within the P ~ O+ region. The modulation wave across the top triangular wave (top carrier wave). The length of the straight line (modulation wave) across the blue triangle in Fig.4.3 is the duty cycle (k_{PO+_O+}) of the switching state O+ within P ~ O+ region. Consequently, use the similar triangles geometrical relationship, the O+ switching state ratio k_{PO+_O+} can be evaluated as follows

$$\frac{3-[1.5m\cdot\sin(\omega t)+1.5]}{3-2}=\frac{k_{PO+\_O+}}{1}$$

$$(3-2):1=\left[\frac{3}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t)\right]:k_{PO+\_O+}$$

$$k_{PO+\_O+}=\frac{3}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.6}$$

Due to P switching state ratio k_{PO+_P} has the complementary relation with the O+ switching state ratio, within P ~ O+ region, thus it can be calculated as

$$k_{PO+\_P}=1-k_{PO+\_O+}=-\frac{1}{2}+\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.7}$$

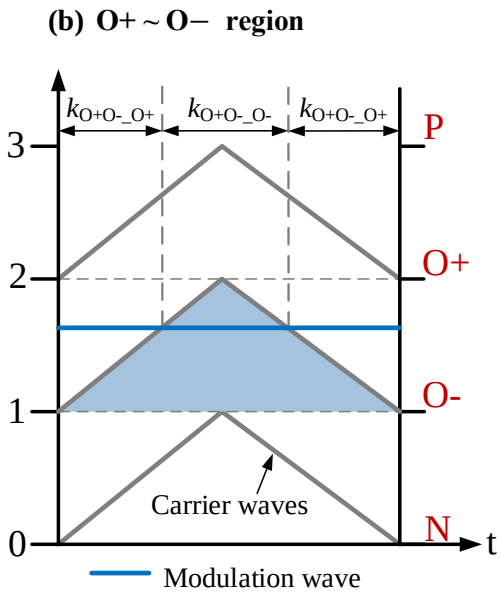


Figure 4.4 The switching state when the modulation wave between O+ and O- (O+ ~ O- commutation)

For the commutation of O+ ~ O- as shown in Fig.4.4, O− switching state ratio k_{O+O-_O-} can be evaluated as

$$\frac{2-[1.5m\cdot\sin(\omega t)+1.5]}{2-1}=\frac{k_{O+0-\_O-}}{1}$$

$$(2-1):1=[\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t)]\ :k_{O+O-\_O-}$$

$$k_{O+O-\_O-}=\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.8}$$

O+ switching state ratio k_{O+O-_O+} can be calculated as

$$k_{O+O-\_O+}=1-k_{O+O-\_O-}=\frac{1}{2}+\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.9}$$

(c) O− ~ N region

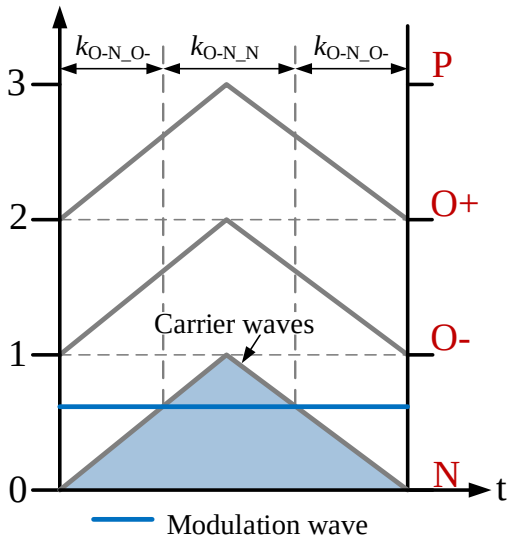


Figure 4.5 The switching state when the modulation wave between O- and N (O- ~ N commutation)

For the commutation of O- ~ N as shown in Fig.4.5, N switching state ratio $k_{O\text{-}N\_N}$ can be evaluated as

$$\frac{1-[1.5m\cdot\sin(\omega t)+1.5]}{3-2}=\frac{k_{O\text{-}N\_N}}{1}$$

$$(1-0):1=[-\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t)]\ :\ k_{O\text{-}N\_N}$$

$$k_{O\text{-}N\_N}=-\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.10}$$

O− switching state ratio $k_{O\text{-}N\_O\text{-}}$ can be obtained as

$$k_{O\text{-}N\_O\text{-}}=1-k_{O\text{-}N\_N}=\frac{3}{2}+\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4.11}$$

In summary, the on/off ratio (duty cycle) k in different commutation regions can be listed in Table IV.V

TABLE IV.V. ON/OFF RATIO WITHIN DIFFERENT COMMUTATION REGIONS

Region	P ~ O+		O+ ~ O−		O− ~ N	
State	P	O+	O+	O−	O−	N
k	$-\frac{1}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{3}{2}-\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{1}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{1}{2}-\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{3}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$-\frac{1}{2}-\frac{3}{2}m\cdot\sin(\omega t)$

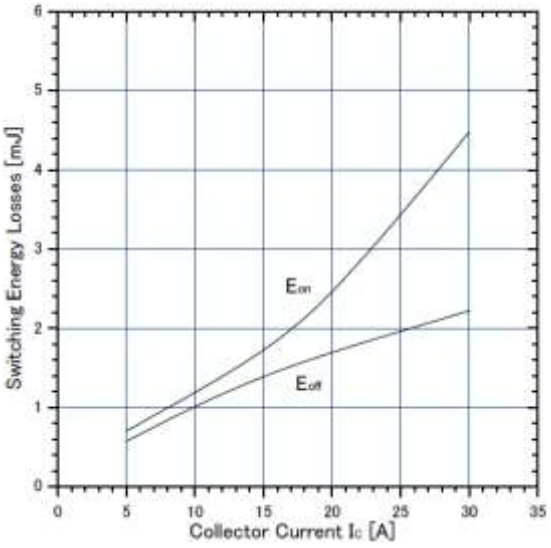
Detailed average conduction loss analytical expressions are listed in Appendix A.IV.

4.2.2 Average analytical model of the switching loss

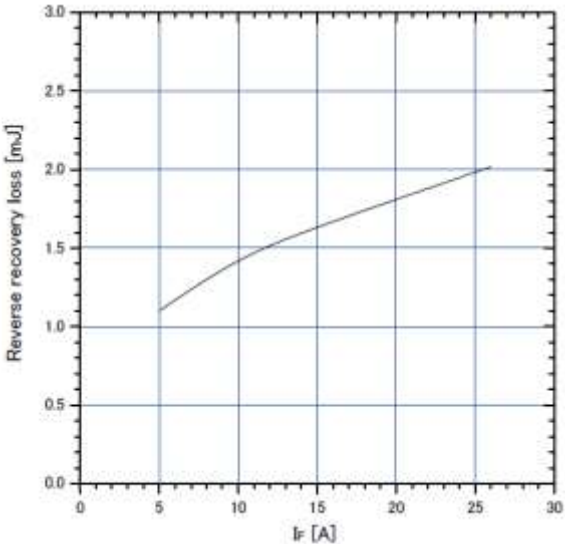
After conduction losses have been analyzed in the previous section, another important part the switching loss which consists of the total converter power loss will be discussed here. Switching losses contain turn-on losses and turn-off losses. For anti-parallel diodes, only reverse recovery losses will be considered. The forward recovery loss during the diode switching on transient is negligible here, and most datasheets do not provide this data at all [14][101][117] [161][175][176]. Generally, the switching energy vs the device current curve is provided by the switching devices datasheets [174], [177]. For example, Fig.4.6 (a) (b) present switching energy vs device collector/diode current curves of 1200V silicon IGBTs (FGW15N120VD). Even all three curves are from the datasheet of FGW15N120VD, however, the detailed mathematical relationship between the switching energy and the device collector/diode current is still unknown. In order to get this mathematical relationship, a hypothesis model can be made according to the shape of the curve first. It can be monitored from Fig.4.6 (a) (b), all turn-off energy E_{on}, turn-off energy E_{off}, and diode reverse recovery energy E_{rr} curves present a parabola shape. Therefore, the switching energy of switching devices can be formulated as shown in (4.12), where the switching energy is assumed to be proportional to the device switching voltage (V_{sw}) and has a quadratic relationship with the device current at the meantime [21].

$$E_{sw\_ins}(i_c(\omega t))=\left(A_0+B_0\cdot|i_c(\omega t)|+C_0\cdot i_c^2(\omega t)\right)\frac{V_{sw}}{V_{base}} \tag{4.12}$$

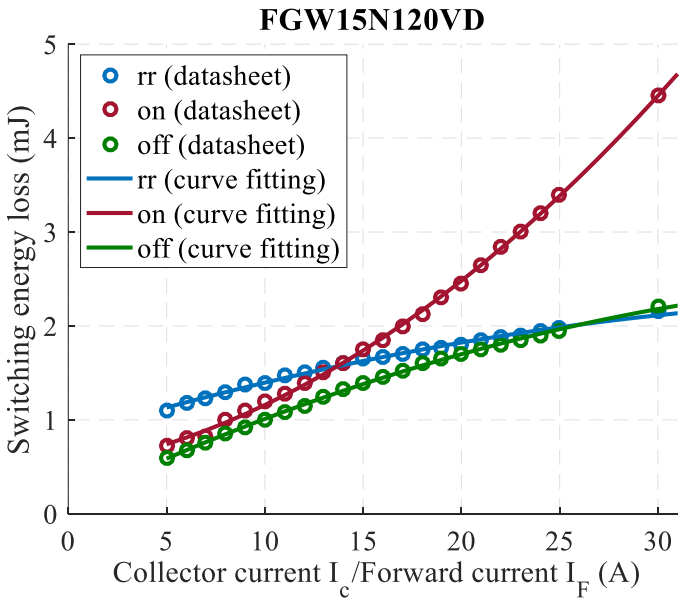
where, $E_{sw\_ins}(i_c(\omega t))$ is the instantaneous switching energy as a function of the load current. V_{sw} is the actual switching voltage of the switching device. V_{base} is the reference switching voltage provided in the datasheet which used for characterizing the switching energy. V_{sw}/V_{base} means the assumption made here that the device switching energy has a linear relationship with the device switching voltage. A_0, B_0, C_0 are parameters describing the relationship between the switching energy and the device collector/diode current. Then the next step is to find out specific values of parameters A_0, B_0, C_0. Import these three curves to the mathematical analysis software (here, MATLAB has been used), then utilize the curve fitting function to generate values of A_0, B_0, C_0, respectively. Curves in the datasheet can be imported to MATLAB by selecting some data points on each curve as shown in Fig.4.6 (c)



(a) IGBT turn-on and turn-off energy curves



(b) Anti-parallel diode reverse recovery energy curve



(c) Curve fitting methods of switching energy curves

Figure 4.6 FGW15N120VD switching energy vs collector current and MATLAB curve fitting

Obviously, the curve generated by curve fitting approach matches well to datasheet points.

Of course, the data on the datasheet might not be precise when actual junction temperatures, switching voltages, or even different converter layouts are different. In order to get a more precise energy curve, groups of double pulse tests should be taken under the desirable operation condition. However, it may take too much time to carry out specific double pulse tests once the temperature requirement, the voltage requirement or the converter prototype layout change. Therefore, the method which takes the data

directly from the datasheet under a high junction temperature not only gives an approximation of switching energy function parameters, but also takes the worst case as mentioned before.

Once switching energy curve parameters have been generated, the switching loss can be analyzed. Assuming a sinusoidal PWM operation, there are j switching actions within each fundamental period. In order to calculate switching losses, all j switching actions during one fundamental period have to be considered. Therefore, the switching energy averaged over one fundamental cycle E_{sw} can be expressed as

$$E_{\mathrm{sw}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} g(\omega t) \cdot E_{\mathrm{sw\_ins}}(i_c(\omega t)) \tag{4.13}$$

where g(ωt) is a piecewise function indicating switching intervals, and has been expressed in (4.14). θ_{sw1}, θ_{sw2} are switching intervals (expressed as angle/radian, where the devices switching transient happen) within one fundamental cycle.

$$g(\omega t) = \begin{cases} 0, & if\ \omega t \notin (\theta_{\mathrm{sw1}}, \theta_{\mathrm{sw2}}) \\ 1, & if\ \omega t \in (\theta_{\mathrm{sw1}}, \theta_{\mathrm{sw2}}) \end{cases} \tag{4.14}$$

Substitute (4.14) into (4.13), the average switching energy over one fundamental cycle can be expressed as shown in (4.15).

$$E_{\mathrm{sw}} = \frac{1}{2\pi} \cdot \int_{\theta_{\mathrm{sw1}}}^{\theta_{\mathrm{sw2}}} E_{\mathrm{sw\_ins}}(i_c(\omega t)) \tag{4.15}$$

Meanwhile, the average switching loss power during each fundamental period can be generally expressed as

$$P_{\mathrm{sw}} = f_s \cdot E_{\mathrm{sw}} \tag{4.16}$$

where, f_s is the carrier frequency (switching frequency). Then, substitute (4.12) and (4.15) into (4.16), the average switching loss during one fundamental period can be expressed as

$$P_{\mathrm{sw}} = \frac{f_s}{2\pi} \cdot \frac{V_{\mathrm{sw}}}{V_{\mathrm{base}}} \int_{\theta_1}^{\theta_{\mathrm{sw2}}} \left[A_0 + B_0 \cdot |I_{\mathrm{CM}} \sin(\omega t - \varphi)| + C_0 \cdot (I_{\mathrm{CM}} \sin(\omega t - \varphi))^2\right] d\omega t \tag{4.17}$$

With (4.17), the switching device average switching loss has been expressed as the function of switching frequency, load current, switching intervals as well as the load power factor angle. It should be noted, due to the sinusoidal PWM operation, the IGBT collector current or anti-parallel current in each

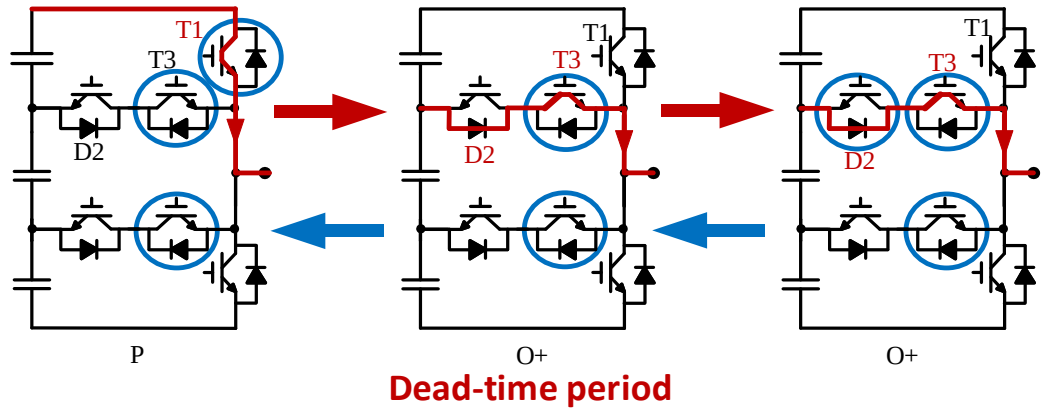
switching action can be presented as the instantaneous value of the output load current. Therefore, the current in (4.17) presents as the instantaneous value of the output load current, where I_{CM} is the load current peak value. Thus, the switching loss is expressed as a function of the switching frequency, the peak load current as well as the power factor.

Theoretically, switching losses of different switching devices are depending on switching transients as well as output current directions. Therefore, in order to find out turn-on losses, turn-off losses of IGBTs and anti-parallel diode recovery losses (The forward recovery loss of the diode during the switching transient is negligible here as mentioned before), it is important to analyze the detailed the commutation process for each switching transition.

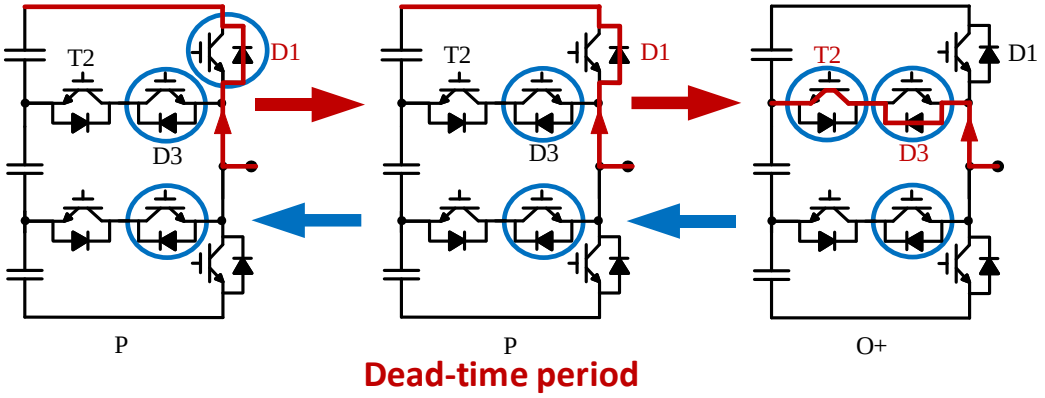
Assume the current flows out of the converter as the positive direction. Fig.4.7 (a) shows the switching transitions between P and O+ when the current is positive, the blue circles indicate the switching devices in ON-state. The red arrows indicate the switching transition from P to O+. According to Table III.I, when switching from P to O+, T3 is always in ON-state, therefore, no switching losses occur on T3. With the switching-off of T1 and switching-on of T2, the current flows through T1 during P-level state commutates to D2 and T3, which causes the turn-off loss on T1. As forward recovery loss of the diode does not consider here, so no switching losses occur on D2. In opposite, the blue arrows indicate the switching transition from O+ to P. According to Table III.I, when switching from O+ to P, T3 is always in ON-state, therefore, no switching losses occur on T3. With the switching-on of T1 and the switching-off of T2, the current flows through D2 and T3 commutates to T1, which causes the turn-on loss on T1 and the reverse recovery loss on D2.

Similarly, Fig.4.7 (b) shows the switching transitions between P and O+ when the current is negative. The red arrows indicate the switching transition from P to O+. According to Table III.I, when switching from P to O+, T3 is always in ON-state, therefore, no switching losses occur on D3. With the switching-off of T1 and switching-on of T2, the current flows through D1 during P-level state commutates to T2 and D3, which causes reverse recovery loss on D1 and the turn-on loss on T2. In opposite, the blue arrows indicate the switching transition from O+ to P. According to Table III.I, when switching from O+ to P, T3 is always in ON-state, therefore, no switching losses occur on D3. With the switching-on of T1 and the switching-off of T2, the current flows through T2 and D3 commutates to D1, which causes

the turn-off loss on T2. As forward recovery loss of the diode does not consider here, so no switching losses occur on D1.



(a)



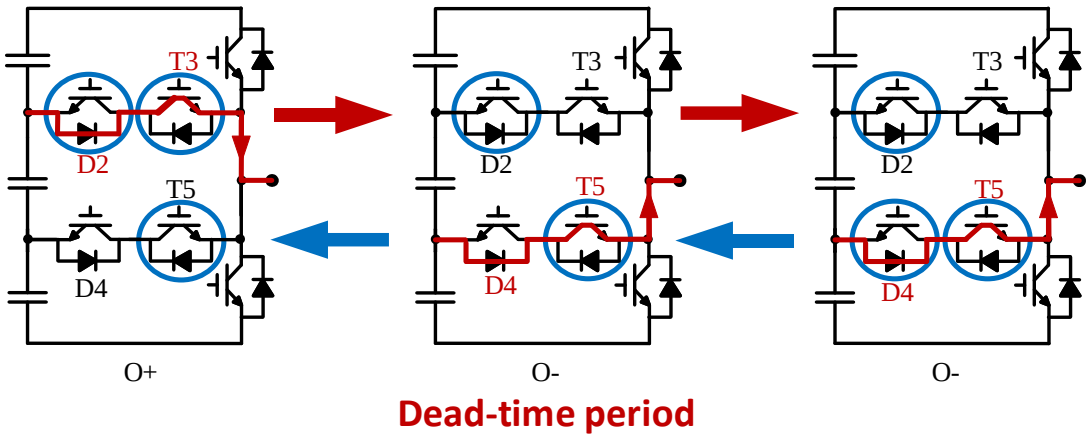
(b)

Figure 4.7 Switching transition between P and O+ (a) i > 0, (b) i < 0

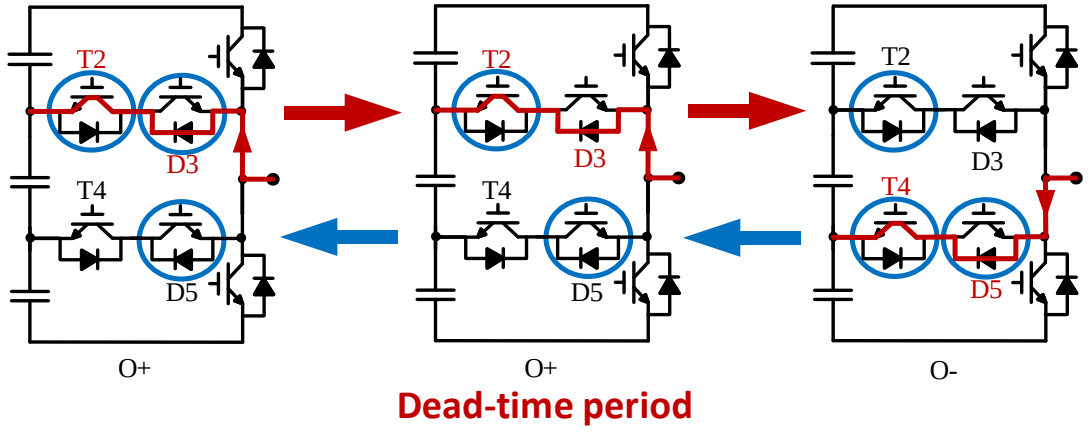
Fig.4.8 (a) shows the switching transitions between O+ and O- when the current is positive, the blue circles indicate the switching devices in ON-state. The red arrows indicate the switching transition from O+ to O-. According to Table III.I, when switching from O+ to O-, T2 and T5 are always in ON-state, therefore, no switching losses occur on D2, T5. With the switching-off of T3 and switching-on of T4, the current flows through D2 and T3 during O+ level state commutates to D4 and T5, which causes the turn-off loss on T3. As forward recovery loss of the diode does not consider here, so no switching losses occur on D4. In opposite, the blue arrows indicate the switching transition from O- to O+. According to Table III.I, when switching from O- to O+, T2 and T5 are always in ON-state, therefore, no switching losses occur on D2 and T5. With the switching-on of T3 and the switching-off of T4, the current flows through D4 and T5 commutates to D2 and T3, which causes the turn-on loss on T3 and the reverse

recovery loss on D4.

Similarly, Fig.4.8 (b) shows the switching transitions between O+ and O- when the current is negative. The red arrows indicate the switching transition from O+ to O-. According to Table III.I, when switching from O+ to O-, T2 and T5 are always in ON-state, therefore, no switching losses occur on T2, D5. With the switching-off of T3 and switching-on of T4, the current flows through T2 and D3 during O+-level state commutates to T4 and D5, which causes reverse recovery loss on D3 and the turn-on loss on T4. In opposite, the blue arrows indicate the switching transition from O- to O+. According to Table III.I, when switching from O- to O+, T2 and T5 are always in ON-state, therefore, no switching losses occur on T2, D5. With the switching-on of T3 and the switching-off of T4, the current flows through T4 and D5 commutates to T2 and D3, which causes the turn-off loss on T4. As forward recovery loss of the diode does not consider here, so no switching losses occur on D3.



(a)

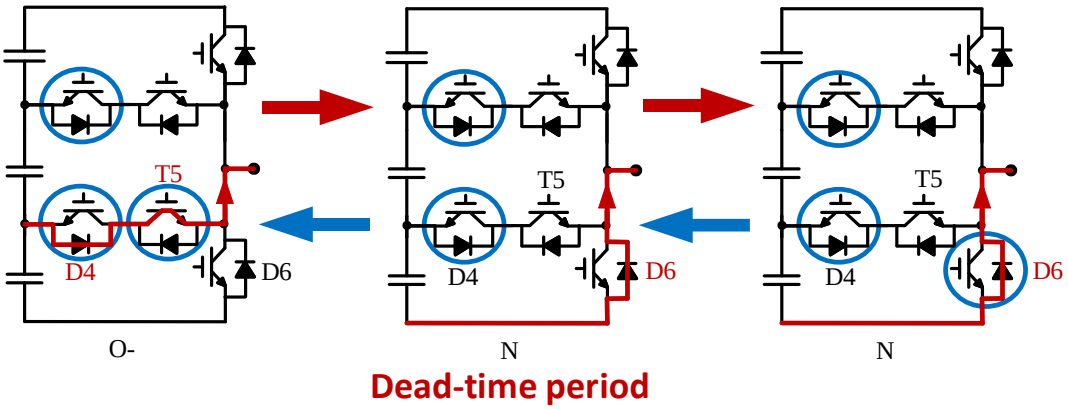


(b)

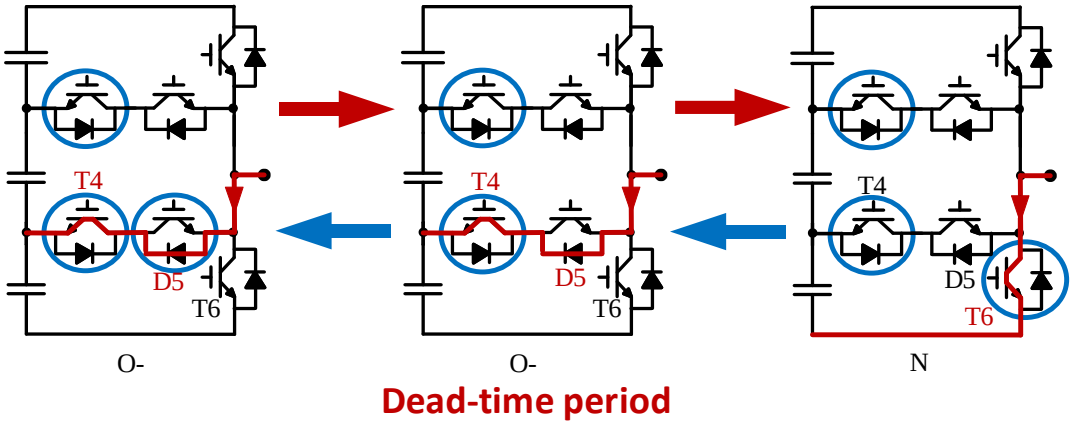
Figure 4.8 Switching transition between O+ and O- (a) i > 0, (b) i < 0

Fig.4.9 (a) shows the switching transitions between O- and N when the current is positive, the blue circles indicate the switching devices in ON-state. The red arrows indicate the switching transition from O- to N. According to Table III.I, when switching from O- to N, T4 is always in ON-state, therefore, no switching losses occur on D4. With the switching-off of T5 and switching-on of T6, the current flows through T1 and D4 during O- level state commutates to D6, which causes the turn-off loss on T5. As forward recovery loss of the diode does not consider here, so no switching losses occur on D6. In opposite, the blue arrows indicate the switching transition from N to O-. According to Table III.I, when switching from N to O-, T4 is always in ON-state, therefore, no switching losses occur on D4. With the switching-on of T5 and the switching-off of T6, the current flows through D6 commutates to T5 and D4, which causes the turn-on loss on T5 and the reverse recovery loss on D6.

Similarly, Fig.4.9 (b) shows the switching transitions between O- and N when the current is negative. The red arrows indicate the switching transition from O- to N. According to Table III.I, when switching from O- to N, T4 is always in ON-state, therefore, no switching losses occur on T4. With the switching-off of T5 and switching-on of T6, the current flows through T4 and D5 during O- level state commutates to T6, which causes reverse recovery loss on D5 and the turn-on loss on T6. In opposite, the blue arrows indicate the switching transition from N to O-. According to Table III.I, when switching from N to O-, T4 is always in ON-state, therefore, no switching losses occur on T4. With the switching-on of T5 and the switching-off of T6, the current flows through T6 commutates to T4 and D5, which causes the turn-off loss on T6. As forward recovery loss of the diode does not consider here, so no switching losses occur on D5.



(a)



(b)

Figure 4.9 Switching transition between O- and N (a) i > 0, (b) i < 0

Table IV.VI summarizes the resulted switching losses during different switching transitions as shown in Fig.4.7, Fig.4.8 and Fig.4.9.

TABLE IV.VI SWITCHING LOSSES DURING DIFFERENT COMMUTATIONS

	Switching Losses	
Switching Transitions	$i_c \geq 0$	$i_c \leq 0$
P → O+	$P_{\_T1\_off}$	$P_{\_T2\_on}$, $P_{\_D1\_rr}$
O+ → P	$P_{\_T1\_on}$, $P_{\_D2\_rr}$	$P_{\_T2\_off}$
O+ → O-	$P_{\_T3\_off}$	$P_{\_T4\_on}$, $P_{\_D3\_rr}$
O- → O+	$P_{\_T3\_on}$, $P_{\_D4\_rr}$	$P_{\_T4\_off}$
O- → N	$P_{\_T5\_off}$	$P_{\_T6\_on}$, $P_{\_D5\_rr}$
N → O-	$P_{\_T5\_on}$, $P_{\_D6\_rr}$	$P_{\_T6\_off}$

In order to get the analytical expression of the switching loss of different switching devices, switching intervals θ_{sw1}, θ_{sw2} in (4.17) are key factors. Through Fig.4.2, switching intervals of different switching devices can be summarized in TABLE IV.VII to TABLE IV.X according to different modulation indices and power factor angles.

TABLE IV.VII. $M \leq \frac{1}{3}$

Device	Switching intervals
T1, T6	Null
D1, D6	Null
T2, T5	Null
D2, D5	Null
T3, T4	$[\varphi, \pi+\varphi]$
D3, D4	$[0, \varphi]$, $[\pi+\varphi, 2\pi]$

TABLE IV.VIII. $M>\frac{1}{3},\ \Phi \leq \text{SIN}^{-1}(\frac{1}{3M})$

Device	Switching intervals
T1, T6	$[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$
D1, D6	Null
T2, T5	Null
D2, D5	$[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$
T3, T4	$[\varphi,\ \sin^{-1}(\frac{1}{3m})], [\pi-\sin^{-1}(\frac{1}{3m}), \pi+\varphi]$
D3, D4	$[0, \varphi], [\pi+\varphi, \pi+\sin^{-1}(\frac{1}{3m})], [2\pi-\sin^{-1}(\frac{1}{3m}), 2\pi]$

TABLE IV.IX. $m > \frac{1}{3},\ \sin^{-1}(\frac{1}{3m}) < \varphi < \pi-\sin^{-1}(\frac{1}{3m})$

Device	Switching intervals
T1, T6	$[\varphi, \pi-\sin^{-1}(\frac{1}{3m})]$
D1, D6	$[\sin^{-1}(\frac{1}{3m}), \varphi]$
T2, T5	$[\sin^{-1}(\frac{1}{3m}), \varphi]$
D2, D5	$[\varphi, \pi-\sin^{-1}(\frac{1}{3m})]$
T3, T4	$[\pi-\sin^{-1}(\frac{1}{3m}), \pi+\sin^{-1}(\frac{1}{3m})]$
D3, D4	$[0,\ \sin^{-1}(\frac{1}{3m})], [2\pi-\sin^{-1}(\frac{1}{3m}), 2\pi]$

TABLE IV.X. $M > \frac{1}{3}$, $\Pi - \sin^{-1}(\frac{1}{3M}) \leq \Phi < \Pi$

Device	Switching intervals
T1, T6	Null
D1, D6	$[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$
T2, T5	$[\sin^{-1}(\frac{1}{3m}), \pi-\sin^{-1}(\frac{1}{3m})]$
D2, D5	Null
T3, T4	$[\varphi, \pi+\sin^{-1}(\frac{1}{3m})]$, $[2\pi-\sin^{-1}(\frac{1}{3m}), \varphi+\pi]$
D3, D4	$[0, \sin^{-1}(\frac{1}{3m})]$, $[\pi-\sin^{-1}(\frac{1}{3m}), \varphi]$, $[\varphi+\pi, 2\pi]$

Compare Table IV.I ~ Table IV.IV to Table IV.VII ~ Table IV.X, it can be noticed that switching intervals of some switching devices are different compared to their conduction intervals. The reason is that in some specific intervals, specific devices do conduct but don't switch. For example, when $m \leq 1/3$, the conduction intervals of T2 are $[0, \varphi]$ and $[\pi+\varphi, 2\pi]$ over one fundamental period. However, within these two intervals, T2 is always ON. Consequently, during this commutation, even the current flows through them changed, there's no switching loss, the voltage drops on T2 and D2 are always 0. Therefore, in this situation, the switching interval of T2 is Null. The detailed average switching loss analytical expressions are listed in Appendix A.IV.

In summary, proposed average analytical power loss models for the four-level π-type converter present the switching device power loss as a function of the load power factor, switching frequency, modulation index, device voltage, and converter current. It gives an intuitive vision of the power loss distribution from each individual switching device of the converter.

It should be noticed, all calculation parameters from the datasheet are based on the worst case (175°C junction temperature). Meanwhile, the parasitic parameters of specific converter board layouts are not considered as well. The reason of this can be divided into two parts. First, the purpose of the proposed loss model derived for the proposed four-level π-type converter is to provide a quick estimation for the converter thermal analysis based on the selected switching device datasheet. If temperature conditions and parasitic effects have to be considered, devices conduction parameters as well as switching

parameters have to be re-measured through double-pulse tests once the operation temperature or porotype layout are changed. Therefore, it will be too complicated, and time consuming even it can provide relative more precise parameters for the system optimization design. Second, the thermal design based on the worst case calculation can provide the most reliable operation.

The proposed loss model derived in this chapter is a generalized method. Therefore, even the proposed loss model is based on the most basic sinusoidal modulation, if any pre-calculated zero-sequence single components need to inject into the original sinusoidal modulation waveform such as third order harmonic contents, the final fundamental phase voltage v_p in Fig.4.2 needs to be changed. Therefore, devices conduction intervals in Fig.4.2, Table IV.I to Table IV.IV and switching intervals in Table IV.VII to Table IV.X need to be changed accordingly.

4.3 Power loss calculation analysis based on the proposed power loss model

TABLE IV.XI IGBT DEVICES CANDIDATES

Switch	Device
T1, T6	FGW15N120VD (1200V)
T2, T3, T4, T5	IKW30N60H3 (600V)

In this thesis, 1200V Si IGBTs with co-pack anti-parallel diodes (FGW15N120VD) [174] are selected as candidate devices for T1(D1) and T6(D6). Meanwhile, 600V Si IGBTs with co-pack anti-parallel diodes (IKW30N60H3) [177] are selected as candidate devices for T2(D2), T3(d3), T4(D4) and T5(D5) of the four-level π-type converter topology as shown in Table. IV.XI.

By employing the linear extended method introduced in Fig.4.1, parameters of conduction losses expressions (4.2) (4.3) (4.5a) (4.5b) can be derived. Similarly, use the curve fitting method introduced in Fig.4.6, parameters of switching losses expressions (4.17) can be derived as well. These parameters are summarized as shown in Table IV.XII and Table IV.XIII.

TABLE IV.XII PARAMETERS OF LOSS MODEL FOR FGW15N120VD

Parameters of the loss model (FGW15N120VD)	Value
V_{CE0}	1 V
r_{0T}	0.093 Ω
V_{F0}	0.9 V
r_{0D}	0.057 Ω
A_{0T_on}, B_{0T_on}, C_{0T_on}	2.15×10^{-4}, 2.6×10^{-5}, 3.5×10^{-6}
A_{0T_off}, B_{0T_off}, C_{0T_off}	0.4×10^{-4}, 1.007×10^{-4}, -1×10^{-6}
A_{0D}, B_{0D}, C_{0D}	8.002×10^{-4}, 6.8×10^{-5}, -8.627×10^{-7}

TABLE IV.XIII PARAMETERS OF LOSS MODEL FOR IKW30N60H3

Parameters of the loss model (IKW30N60H3)	Value
V_{CE0}	1.17 V
r_{0T}	0.042 Ω
V_{F0}	1.02 V
r_{0D}	0.038 Ω
A_{0T_on}, B_{0T_on}, C_{0T_on}	-3.256×10^{-5}, 2.61×10^{-5}, 5.36×10^{-7}
A_{0T_off}, B_{0T_off}, C_{0T_off}	-0.708×10^{-5}, 1.84×10^{-5}, 7.63×10^{-8}
A_{0D}, B_{0D}, C_{0D}	4.2×10^{-4}, 7.88×10^{-6}, -1.04×10^{-7}

TABLE IV.XIV SYSTEM PARAMETERS FOR SIMULATION AND CALCULATION

V_{dc}	600V
Output power	6.5 kW
Switching frequency	10 kHz and 50 kHz
Fundamental frequency	50 Hz
Modulation index	0.28 and 0.95

Substitute parameters of Table IV-XII and Table IV-XIII into devices average analytical loss expressions

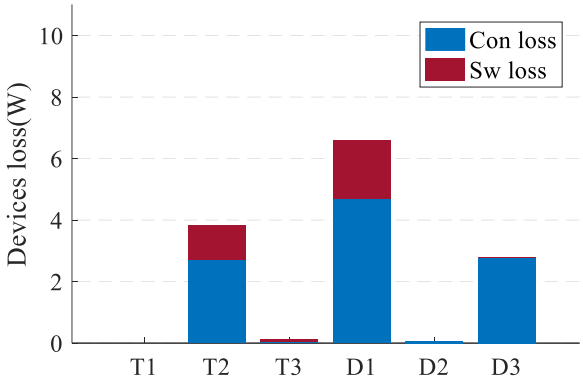
in Appendix A.IV, the power loss distribution on each switching device of the four-level π-type converter over one fundamental period can be calculated. This process can be done through MATLAB/Simulink, detailed MATLAB code is summarized in Appendix C.

Fig.4.10 shows the calculated power loss distribution among different switching devices of the four-level π-type converter under the same output power level, different modulation indices and different switching frequencies. Simulation parameters are shown in Table IV.XIV.

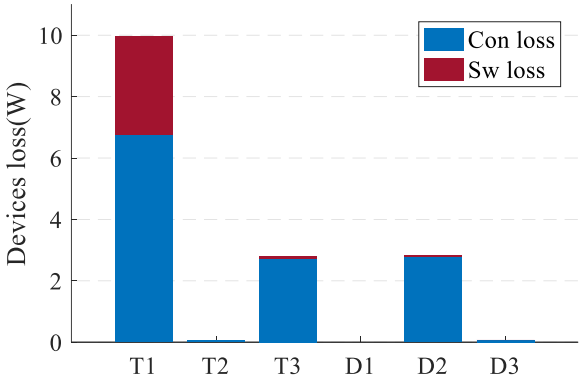
Fig.4.10 (a) (b) show conditions under a relative high modulation index (m=0.95) with inverter and rectifier operations based on a 10 kHz switching frequency. With the rectifier operation under the high modulation index (m=0.95) as shown in Fig.4.10 (a), power losses generated from D1, T2, D3 are higher than that from D2, T3, T1. In contrast, with the inverter operation as shown in Fig.4.10 (b), power losses on D2, T3 and T1 are higher than that on D1, T2, D3. Fig.4.10 (c) (d) present conditions under a low modulation index condition (m=0.28) with inverter and rectifier operations based on a 10 kHz switching frequency. It should be noted, the dc-link voltage utilization ratio when m=0.28 is approximately only 0.3 times the one of the conditions when m=0.95. Therefore, in order to get a same output power level, the output current of the condition in Fig.4.10 (c) (d) is approximately 3.4 times the output current of the condition in Fig.4.10 (a) (b). Consequently, as shown in Fig.4.10 (c), the total power loss is much higher than that of Fig.4.10 (c), and the conduction loss of T2 and D3 are much dominant. In Fig.4.10 (d) the total power loss is also much higher than that of Fig.4.10 (b), and T3 and D2 are more stressed. From the comparison of Fig.4.10 (a) (b) and Fig.4.10 (c) (d), it can be concluded that for the four-level π-type converter, in order to get the same output power level, the less modulation indices, the higher total power losses generated. Meanwhile, as introduced in Chapter 3, when $m \leq 1/3$, the converter operates as a general two-level converter, which loses the advantage of the low output harmonic characteristic.

Fig.4.10 (e) (f) show conditions under the high modulation index (m=0.95) with inverter and rectifier operations based on the 50 kHz switching frequency. The power loss distribution tendency on each switching device is similar as that of conditions on Fig.4.10 (a) (b), where D1, T2, D3 are more stressed than D2, T3, T1 during rectifier operation. And D2, T3, T1 are more stressed than D1, T2, D3 during the inverter operation. The difference is the switching loss of the corresponding switching device of

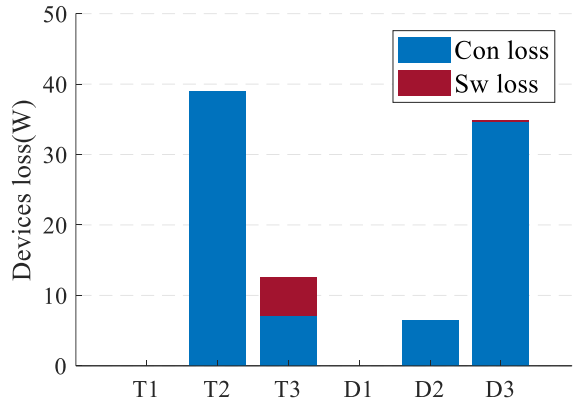
Fig.4.10 (e) (f) is much higher than that of Fig.4.10 (a) (b) due to the 5 times higher switching frequency. Fig.4.10 (g) (h) show conditions with the low modulation index (m=0.28) with inverter and rectifier operations based on the 50 kHz switching frequency. Similar to the tendency of Fig.4.10 (a) (b) (c) (d), with the same output power level, power losses of low modulation index conditions in Fig.4.10 (g) (h) are much higher than that of high modulation index conditions in Fig.4.10 (e) (f). Meanwhile, due to the high switching frequency, switching losses on corresponding switching devices of Fig.4.10 (g) (h) are much higher than that of Fig.4.10 (e) (f).



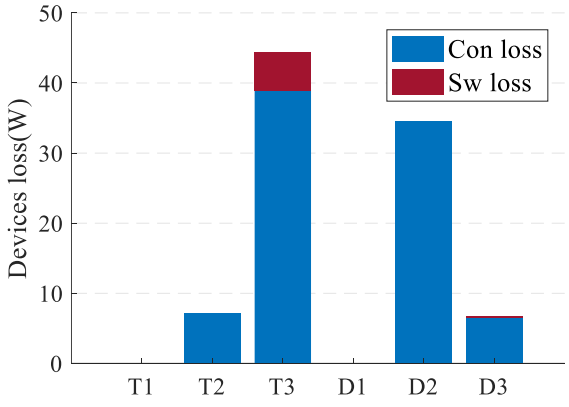
(a) 10 kHz m=0.95, rectifier



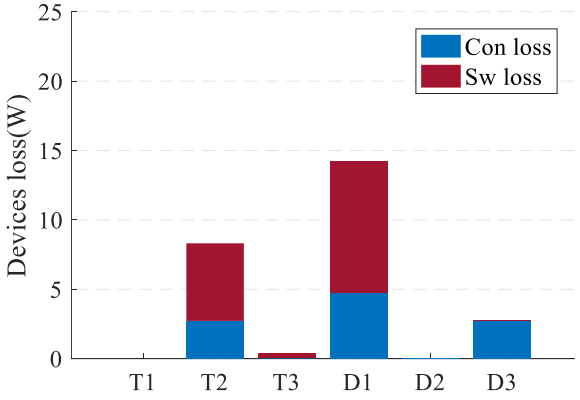
(b) 10 kHz m=0.95, inverter



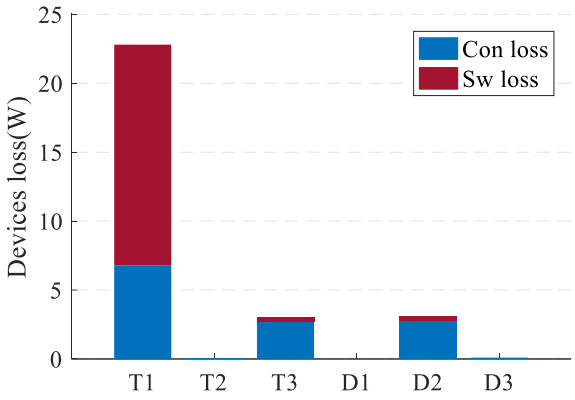
(c) 10 kHz m=0.28, rectifier



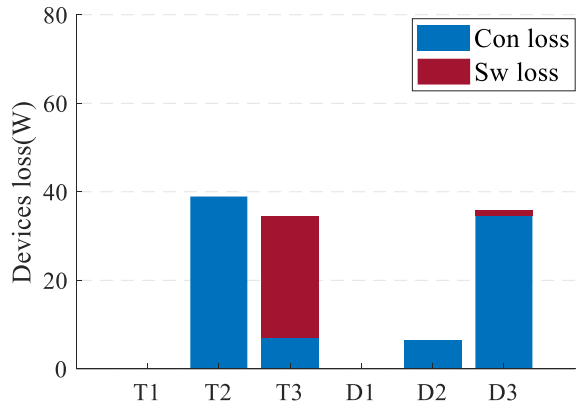
(d) 10 kHz m=0.28, inverter



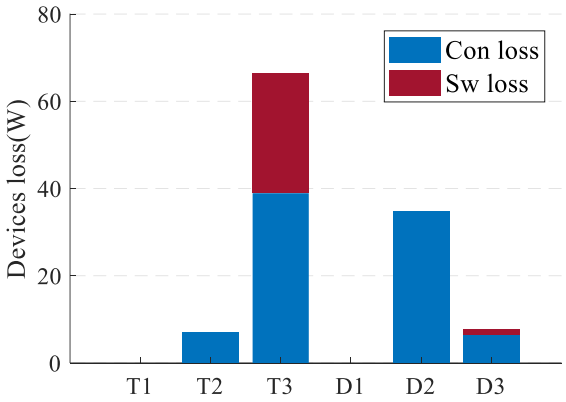
(e) 50 kHz m=0.95, rectifier



(f) 50 kHz m=0.95, inverter



(g) 50 kHz m=0.28, rectifier

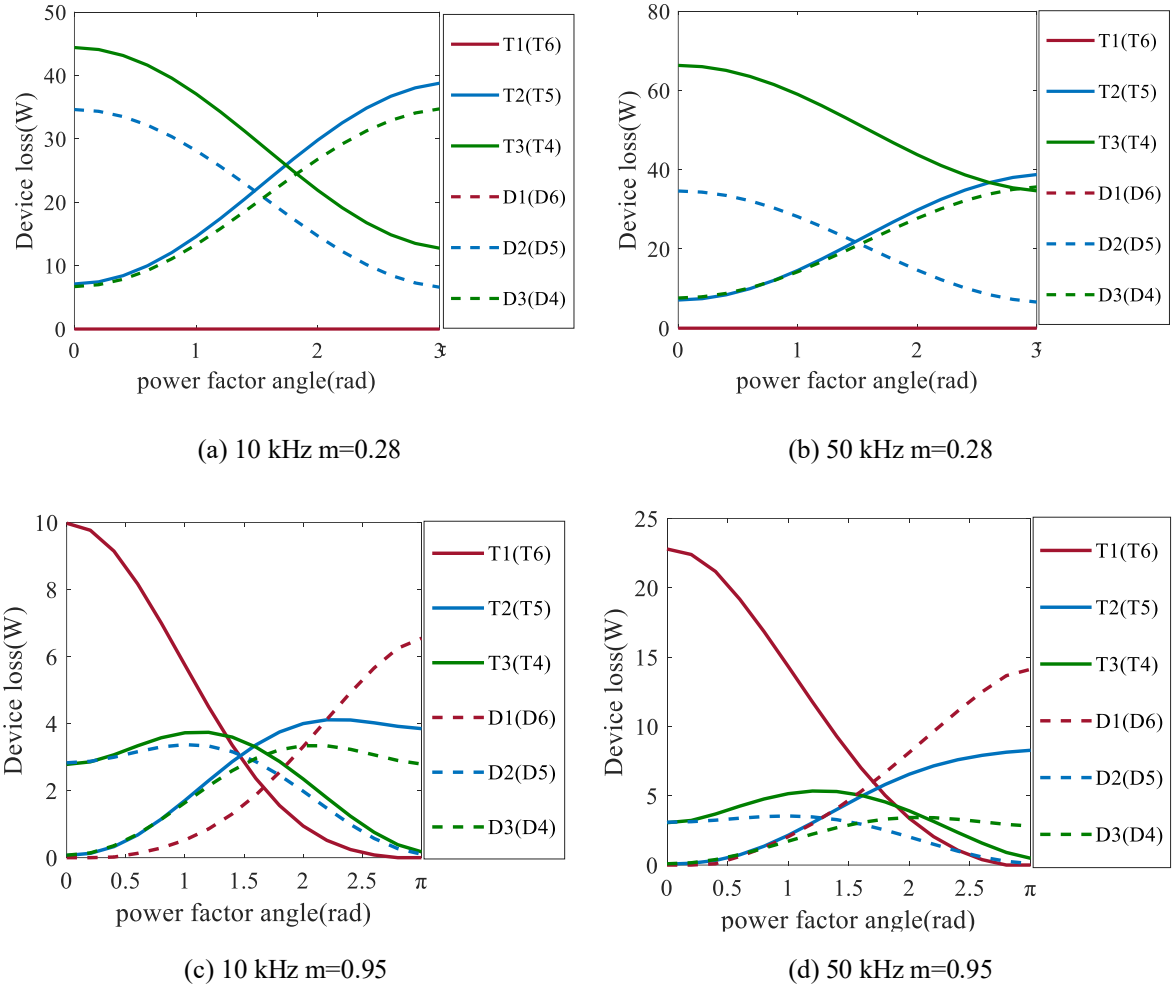


(h) 50 kHz m=0.28, inverter

Figure 4.10 Calculation average power losses of the four-level π-type converter

Fig.4.11 shows average switching device losses variation with the power factor angle under different carrier-waveform frequencies and different modulation indices. Fig.4.11 (a) (b) show conditions when the modulation index equals to 0.28 (low modulation index), where T1, T6, D1, D6 do not conduct or switch at all according to Table IV.IV and Table IV.VIII. Therefore, their corresponding average power losses are zero. In Fig.4.11 (a), the carrier wave frequency equals to 10 kHz (relatively low), T3, T4, D2, D5 are more stressed in the inverter mode, while T2, T5, D3, D4 are more stressed in the rectifier mode. Fig.4.11 (b) shows the condition when the carrier wave frequency equals to 50 kHz (relatively high), where the power loss distribution tendency is like the situation in Fig.4.11 (a). However, according to Table IV.I and Table IV.VIII and Appendix A.IV, when $m \leq 1/3$, T2, T5, D2, D5 do not switch but conduct, average switching loss expressions of T2, T5, D2, D5 also equal to 0, only switching loss expressions of T3, T4, D3, D4 are proportional to the carrier wave frequency. Therefore, compare

with the results in Fig.4.11 (a), the total average power losses of T3, T4, D3, D4 are higher in Fig.4.11 (b), but total average power losses of T2, T5, D2, D5 are the same in Fig.4.11 (b). Fig.4.11 (c) (d) show the conditions when the modulation index equals to 0.95 (high modulation index) with a same output power level as presented in Table IV.XIV. In Fig.4.11 (c), the carrier wave frequency equals to 10 kHz (relatively low), T1, T6 are most stressed at the inverter operation, T3, T4, D2, D5 are relatively mild at the inverter operation. D1, D6 are most stressed at the rectifier mode, T2, T5, D3, D4 are relatively mild at the rectifier operation. Fig.4.11 (d) shows the condition when the carrier wave frequency equals to 50 kHz (relatively high), where the power loss distribution tendency is like the situation in Fig.4.11 (c). Meanwhile, under a high modulation index condition, T1, T6, D1, D6 occupy the most switching and conduction time during each fundamental period, therefore, with the increase of the carrier wave frequency, switching losses increase on T1, T6, D1, D6 are more dominant. Switching losses on T2, T3, T4, T5, D2, D3, D4, D5 also increase with the increase of the carrier wave frequency. However, due to their switching and conduction time during each fundamental period is much smaller than that of T1, T6, D1, D6, therefore, switching losses increase on T2, T3, T4, T5, D2, D3, D4, D5 are not obviously at high carrier wave frequencies. In summary, compare Fig.4.11 (a) (b) and Fig.4.11 (c) (d), when outputs the same power level from the four-level π-type converter, the higher the modulation index, the less the total power loss. Meanwhile, with the high modulation index, the total power loss can be further shared on more devices, each device will not be that hard stressed compare with the condition under low modulation indices.



(a) 10 kHz m=0.28

(b) 50 kHz m=0.28

(c) 10 kHz m=0.95

(d) 50 kHz m=0.95

Figure 4.11 Variation of devices losses with different power factor angles

4.3.1 Loss model comparison

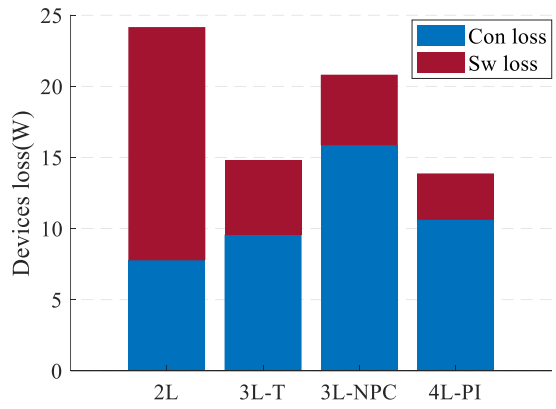
In this part, the total power loss distribution among different converter topologies has been compared through calculation/simulation based on the proposed average power loss model. Detailed average analytical loss expressions of each switching device for the two-level converter, the three-level diode NPC converter, the three-level T-type converter and the four-level π-type converter have been listed in Appendix A I, II, III, respectively.

Fig.4.12 shows the calculated total power loss distribution of these four kinds of power converter topologies based on parameters on Table IV.XIV but only with the high modulation index (m=0.95). Fig.4.12 (a) (b) show conditions under the 10 kHz carrier wave frequency with both rectifier and inverter operations. In the rectifier mode as shown in Fig.4.12 (a), the conduction loss of the two-level converter is the lowest due to the minimum value of the forward conduction voltage v_{CE} for conduction

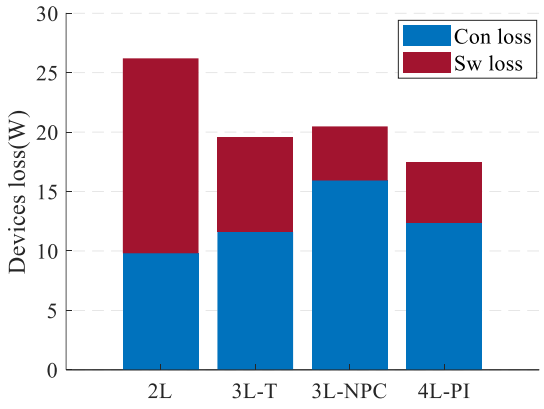
devices during each commutation period. However, due to the high switching voltage on each switching device (have to withstand the whole dc-link voltage), its switching loss is much higher than other three power converter topologies. This leads to a total highest power loss from the two-level converter. In comparison, the conduction loss of the three-level diode NPC converter is the highest. The number of the conduction devices of the three-level diode NPC is the highest (4 devices) among these four topologies during each commutation process. However, due to the switching voltage on each device of the three-level diode NPC converter only have to withstand 1/2 of total dc-link voltage, the total power loss will be still lower than that of the two-level converter. For the three-level T-type converter, the conduction loss of it is the second lowest among these four topologies. As there are only three devices conducting during each commutation period. From the switching loss point of view, even switching voltages of devices of the three-level T-type converter are also 1/2 of the total dc-link voltage. However, as introduced in chapter 3, for 600V dc-link voltage, there are two 1200V IGBTs with two 600V IGBTs in the three-level T-type converter, and four 600V IGBT with two 600V diode in the three-level diode NPC converter. According to Table IV.XII and Table IV.XIII, switching loss parameters of 600V IGBTs and 1200V IGBTs are different. Therefore, switching losses of the three-level T-type converter are relatively higher than that of the three-level diode NPC converter. For the four-level π-type converter, the analysis is a bit complicated. In 3E to 2E and E to 0 commutations processes, there are three devices conducting during each commutation. However, in 2E to E commutation processes, there are four devices conducting during each commutation. Therefore, the conduction loss of the four level π-type converter is higher than that of the three-level T-type converter but less than that of the three-level diode NPC converter. Meanwhile, the switching voltage of devices of the four-level π-type converter is 1/3 of the total dc-link voltage. This makes the four-level π-type converter still have the lowest switching loss among these four converter topologies. It can be found the four-level π-type converter has the lowest total power loss. In the inverter mode as shown in Fig.4.12 (b), the tendency is similar to the condition of Fig.4.12 (a). However, when the converter operates as an inverter, the ac side voltage is almost out of phase of the as side current, which leads to the IGBT conduction time and switching times much larger than that of the anti-parallel diode. Meanwhile, according to switching devices datasheets parameters summarized in Table IV.XII and Table IV.XIII, the equivalent IGBT on-state threshold voltage V_{CE0} and the IGBT equivalent turn-on resistance r_{0T} of both IGBTs are larger than their

corresponding anti-parallel diode equivalent turn-on resistance r_{0D}, and diode equivalent on-state threshold voltage V_{F0}. Due to the linear relationship between conduction losses and loads currents, therefore, conduction losses of the inverter mode are relatively larger than that of the rectifier mode. The switching parameters of IGBTs and anti-parallel diodes are also different in Table IV.XII and Table IV.XIII. Due to the quadratic relationship between switching losses and load currents, therefore, switching losses are different between the rectifier mode and the inverter mode.

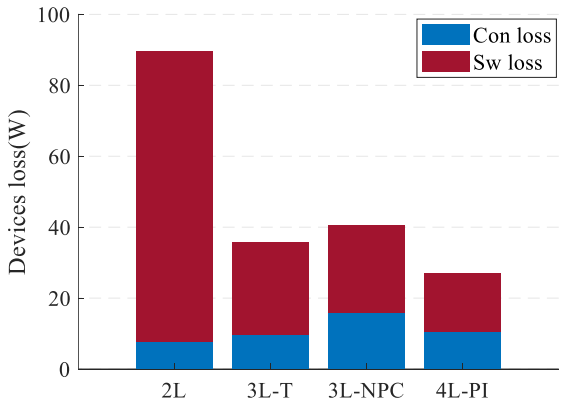
Fig.4.12 (c) (d) show conditions under the 50 kHz carrier wave frequency with both rectifier and inverter operations. With the increase of the switching frequency, switching losses on both modes increases and becomes dominant. Therefore, the advantage of the four-level π-type converter is more dominant, as its switching loss still keeps relatively low compare with other three topologies. It can be found out, the total loss of the four-level π-type converter in any conditions is the minimum.



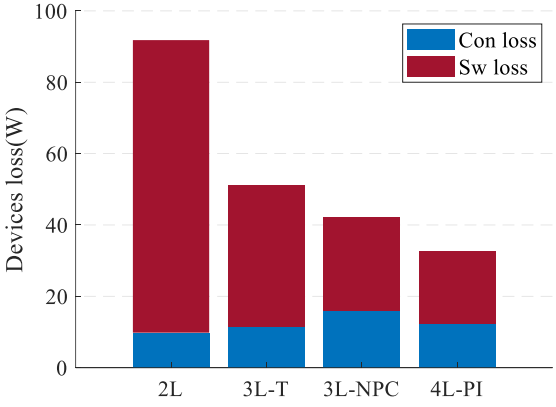
(a) 10 kHz m=0.95, rectifier



(b) 10 kHz m=0.95, inverter



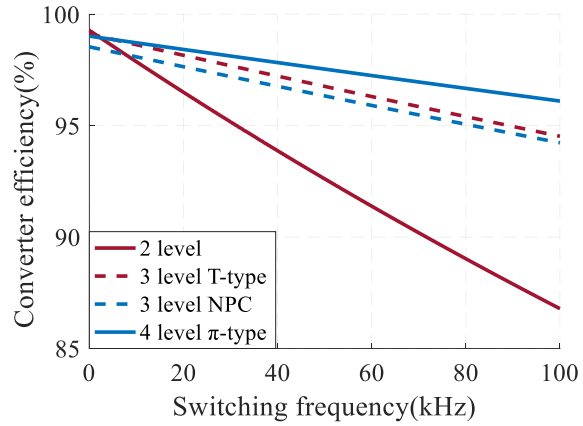
(c) 50 kHz m=0.95, rectifier



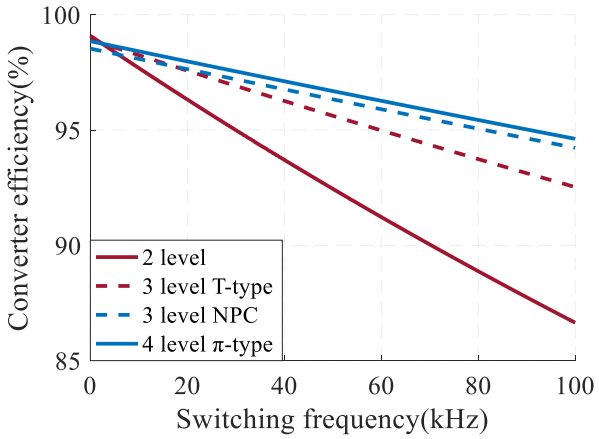
(d) 50 kHz m=0.95, inverter

Figure 4.12 Power losses comparison among different converter topologies

Fig.4.13 shows the converter efficiency variation with respect to different switching frequencies. The calculation is based on rectifier and inverter modes when m=0.95 in comparison to the two-level converter and three-level (diode NPC and T-type) converters. Due to more devices in series in conduction paths, the four-level π-type converter has higher conduction losses compares to those of other three converters. Meanwhile, under the low switching frequency region, where conduction losses are the dominant, therefore, as shows in Fig.4.13, the four-level π-type converter presents slightly lower efficiency when switching frequency is roughly below 5 kHz. In contract, the four-level π-type presents the higher efficiency when the switching frequency is higher than 5 kHz as shown in Fig.4.13. It is due to switching losses are the dominant at the high switching frequency domain, while the four-level π-type converter has the lowest switching losses. The efficiency curves match well to corresponding results in Fig.4.12.



(a) Rectifier efficiency



(b) Inverter efficiency

Figure 4.13 Calculated efficiencies vs switching frequencies curves of different converter topologies

4.4 Prototype design and converter efficiency measurement

In order the validate the proposed average analytical power loss model for the four-level π-type converter, the experimental case study need to be carried out. As used for the power loss analysis calculation, the 1200V Si IGBT (FGW15N120VD) and 600V Si IGBT (IKW30N60H3) are also selected for the converter prototype switching device. The prototype is designed with the ability to handle 3kW power flow. Therefore, during the PCB design procedure, 2 layer PTH, 1.6 mm FR4, 2oz Cu has been set as the converter PCB manufacturing specification. Consider of reducing the effect of disturbance in the gate signal during the transmission, gate driver circuits are integrated in converter board as well. The optocoupler from Avago (HCPL 315J000E) has been chosen as the gate driver chip. Fig.4.14 shows the three-phase four-level π-type converter prototype and Table IV.XV shows the bill of material for the construction of this prototype. The PCB layout view is shown in Appendix E I.

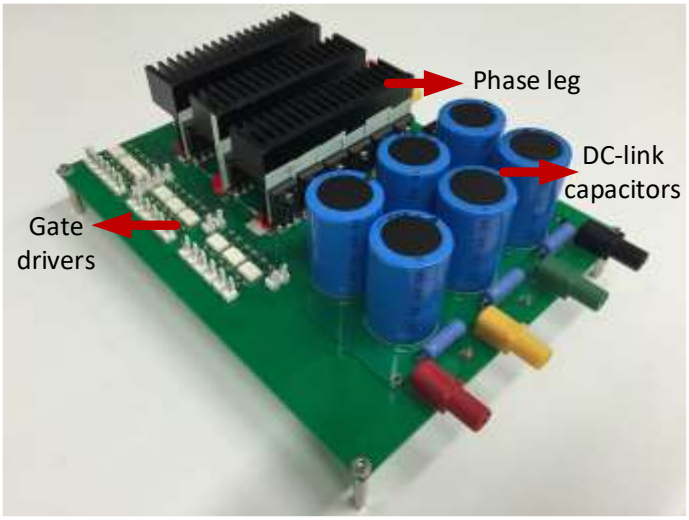


Figure 4.14 Three-phase four-level π-type converter prototype

TABLE IV.XV. LIST OF COMPONENTS FOR THE FOUR-LEVEL Π-TYPE CONVERTER

dc-link capacitors	MAL215990125E3 (1000μF/315V) × 6
dc-link parallel resistors	100kΩ/2W × 3
Switches (T1, T6)	FGW15N120VD (1200V) × 6
Switches (T2, T3, T4, T5)	IKW30N60H3 (600V) × 12
Gate driver chips	HCPL 315J000E × 9
Gate resistors	10Ω (SMD 0806) × 18
Gate driver input resistors	680Ω (SMD 0806) × 18
Gate driver output decoupling caps	0.1μF (SMD 0806) × 18
Heatsink	Elektronik 58/50SA × 3

The dc-link parallel resistors used here are for the system protection. With respect to their effects on the converter output efficiency, a quick Matlab/Simulink operation with the same setup as used on the prototype has been operated as shown in Appendix C.IV. This simulation is also identical to the models used in Appendix B.IV. The only difference is the load resistance on each phase changed from 25Ω to 44Ω. According to the simulation results, with a 600V dc voltage input (200V for each dc-link capacitor, respectively in this test), the average current flowing through each dc-link parallel resistor during each fundamental period is 2mA. The simulation results are shown in Fig.4.15. Thus, the average power on the three dc-link parallel resistors is 1.2W in total. Therefore, for a 2.5kW load converter system, this will only bring a 0.06% difference on the final output power efficiency compares to the results without the dc-link parallel resistors condition. Consequently, the effect on the output power converter from the dc-link parallel resistors can be ignored.

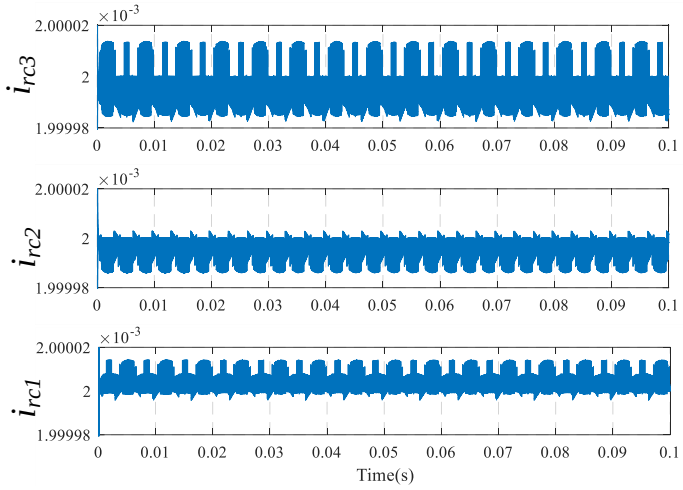


Figure 4.15 Simulation results of currents flow through dc-link parallel resistors

The inverter prototype is driven by three-phase PWM signals generated from a DSP/FPGA board existing in EEMG lab. Fig.4.16 presents the DSP/FPGA control board which consists of a Xilinx SPARTAN XC3S400 FPGA chip and a TI TMS320 F28335 DSP chip. All the operation and control codes in C program and VHDL are written by the author.

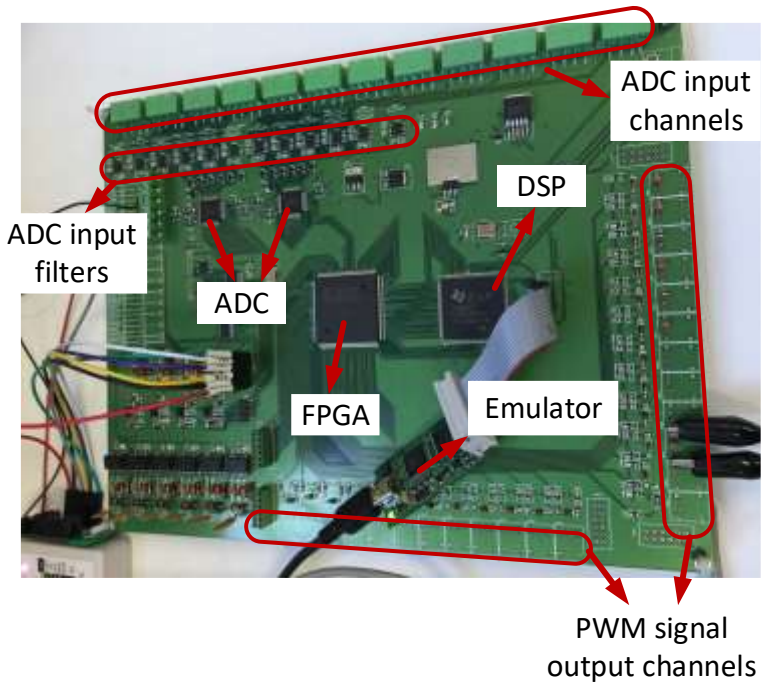


Figure 4.16 DSP/FPGA board

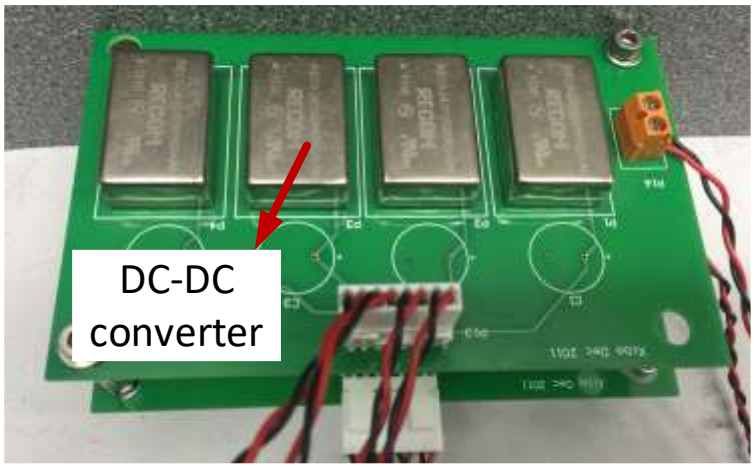


Figure 4.17 Gate driver supply board

The gate driver supply board is designed by Prof. Xibo Yuan, the main device is chosen as the DC-DC buck converter from RECOM (REC8-2415SRW/H2/A/M). Each of them offers single regulated 15V DC output voltage in a DIP24 package with the 2KV isolation. As introduced in Chapter 3, due to the common collector connection of two IGBTs in neutral paths in the converter phase-leg configuration as shown in Fig.3.1, only 8 gate driver supply chips are required for a three-phase inverter. Fig.4.17 shows the layout of the gate driver supply board, as one board contains 4 DC-DC converters, a double-deck is required.

Two NORMA 4000 high bandwidth power analyzers are employed to measure the input and output power of the four-level π-type inverter individually. EA-PS 8080-170 3U 5000W dc power supply is used for the power input. And Agilent DSOX3014A 100 MHz Oscilloscope is used for the waveform measurement. Fig.4.18 shows the test equipment setup. The test is based on a three-phase RL load (R=44Ω, L=6.32mH each phase), and modulation index m=0.95. As the prototype is operated with an open loop sinusoidal modulation, in order to prevent dc-link NP voltages drift, three individual dc power supplies provide 200V voltage to each of dc-link capacitors equally in order to get a total 600V dc input voltage. No forced cooling is applied. Detailed test parameters are summarized in Table IV.XVI.

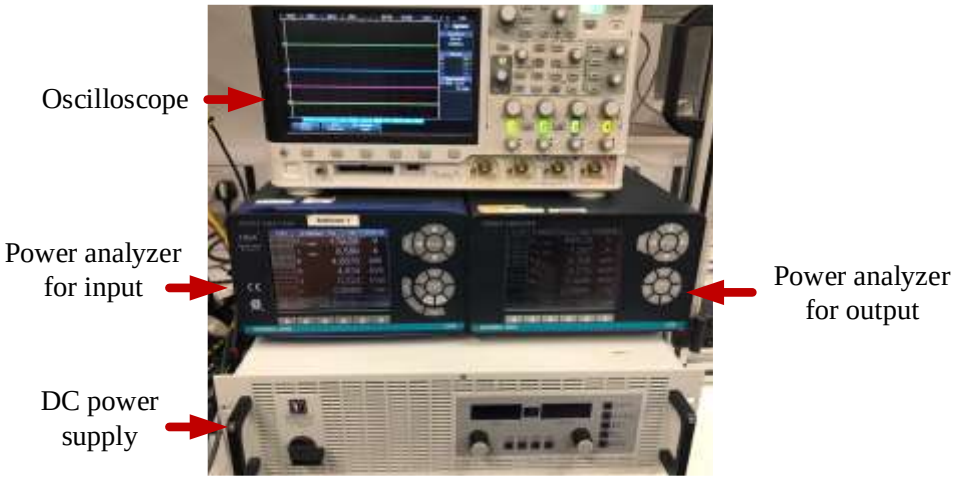


Figure 4.18 Power efficiency measurement test equipment

TABLE IV.XVI. TEST PARAMETERS

V_{dc}	600V
Load	44Ω, 6.32mH
Fundamental frequency	50 Hz
Each dc-link capacitor	1000μF
Modulation index	0.95
Power factor	0.987
Dead-time	2μs

In order to present a practical reference as well as an efficiency comparison, a three-phase two-level converter prototype based on FGW15N120VD (1200V) IGBTs is also built and tested. Fig.4.19 shows the photo of this two-level converter prototype, and Fig.4.20 shows the photo of the separated gate driver board. The PCB layout view is shown in Appendix E II. The bill of material of the two-level converter is shown in Table IV.XVII. The test equipment is the same as that for the four-level π-type inverter.

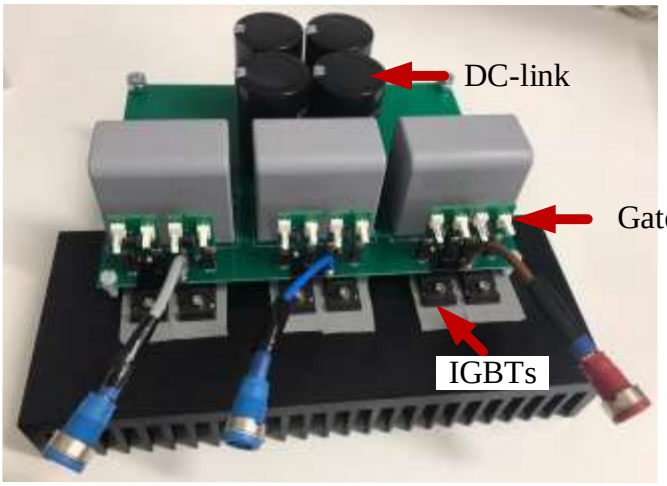


Figure 4.19 Three-phase two-level converter prototype

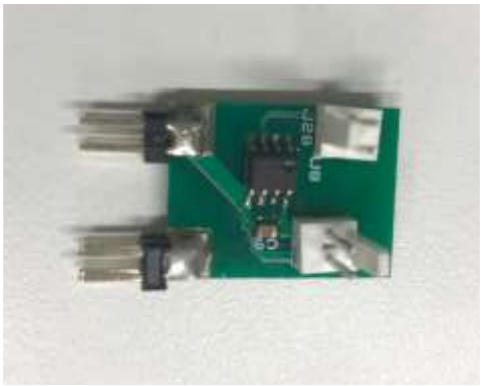


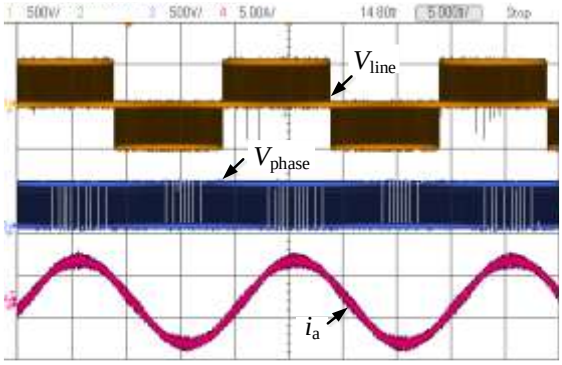
Figure 4.20 Gate driver board for the two-level converter

TABLE IV.XVII. LIST OF COMPONENTS FOR THE TWO-LEVEL CONVERTER

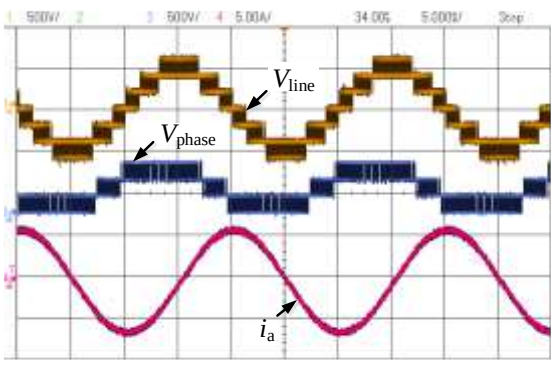
dc-link capacitors 1	B43644-A5687-M (680µF/450V) × 4
dc-link capacitors 2	VISHAY 1848 MKP (40µF/900V) × 3
dc-link parallel resistors	100kΩ/2W × 2
Switches	FGW15N120VD (1200V) × 6
Gate driver chips	HCPL 0314 × 6
Gate resistors	10Ω (SMD 0806) × 6
Gate driver input resistors	680Ω (SMD 0806) × 6
Gate driver output decoupling caps	0.1µF (SMD 0806) × 6
Heatsink	163AB1000B (0.4 C/W, 100*200*40mm)

4.4.1 Test output waveforms comparison

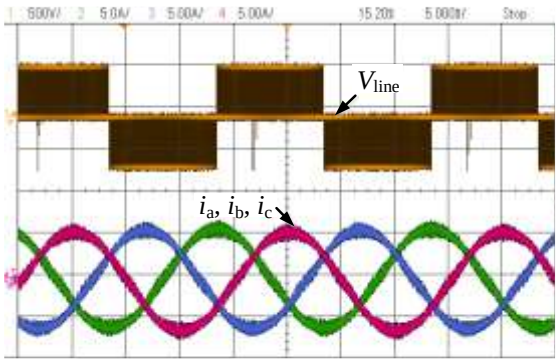
Fig.4.21 shows experimental output currents and voltages waveforms of the two-level inverter as well as the four-level π-type inverter under different switching frequencies. Fig.4.21 (a) (b) show the phase A line voltage, phase voltage (with regards to the dc-link bottom side) and the output current. In Fig.4.21 (a) the phase voltage has two voltage levels and the line voltage has three levels for the two-level inverter as expected. In Fig.4.21 (b) the phase voltage has four voltage levels and the line voltage has seven voltage levels for the four-level π-type inverter as expected. Fig.4.21 (c) (d), Fig.4.21 (e) (f), Fig.4.21 (g) (h), Fig.4.21 (i) (j) show the line voltage and output three-phase currents under f_s=10 kHz, f_s=20 kHz, f_s=30 kHz, f_s=40 kHz, respectively. It can be found out under the same switching frequency such as in Fig.4.21 (c) (d) f_s=10 kHz, output currents waveforms of the two-level inverter in Fig.4.21 (c) are thicker than that of the four-level π-type inverter in Fig.4.21 (d). It is due to the output current high frequency harmonic of the four-level π-type inverter is smaller than that of the two-level inverter. Meanwhile, compare Fig.4.21 (c) and Fig.4.21 (i), output currents in Fig.4.21 (i) are thinner than that of Fig.4.21 (c), which means with the increase of the switching frequency, output currents high frequency harmonic reduces with the same output filter setting.



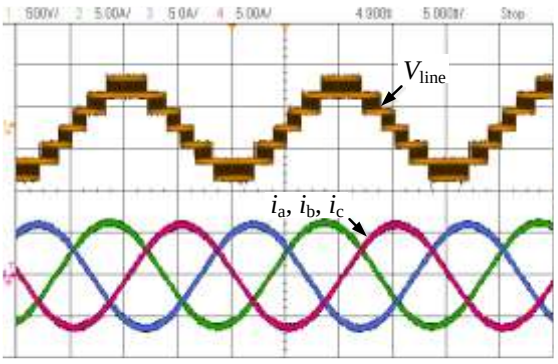
(a) f_s=10 kHz



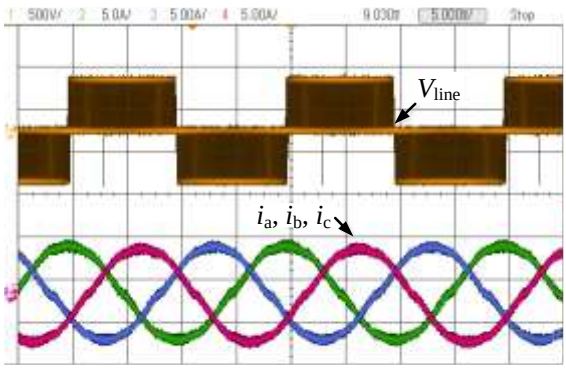
(b) f_s=10 kHz



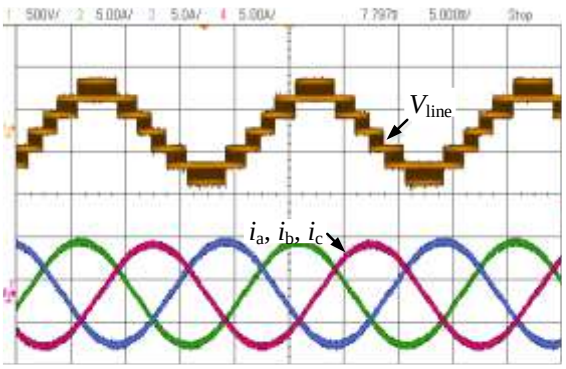
(c) f_s=10 kHz



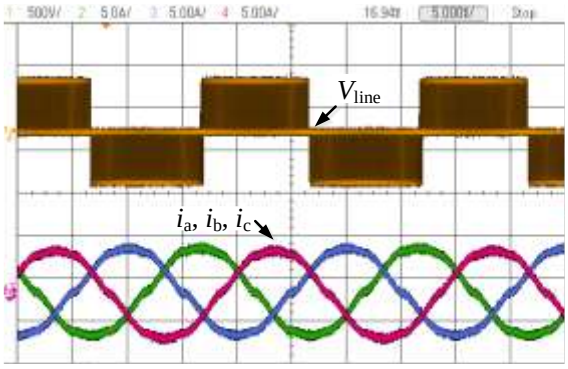
(d) f_s=10 kHz



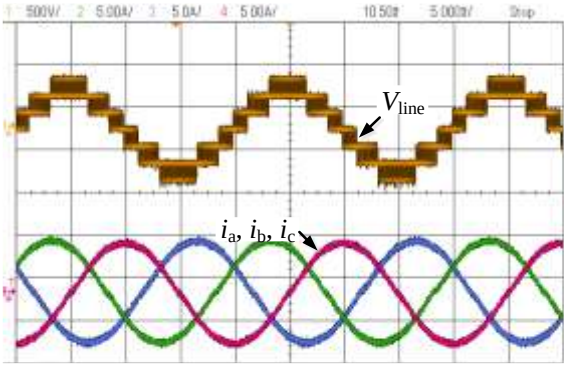
(e) f_s=20 kHz



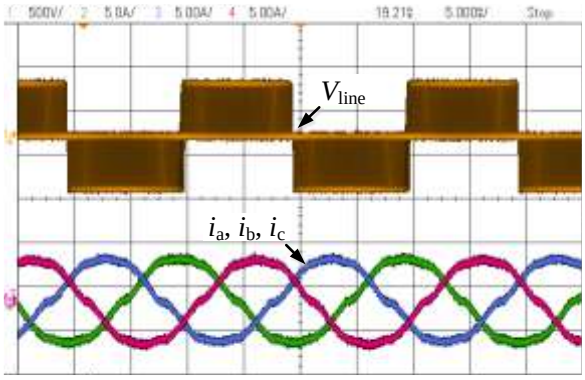
(f) f_s=20 kHz



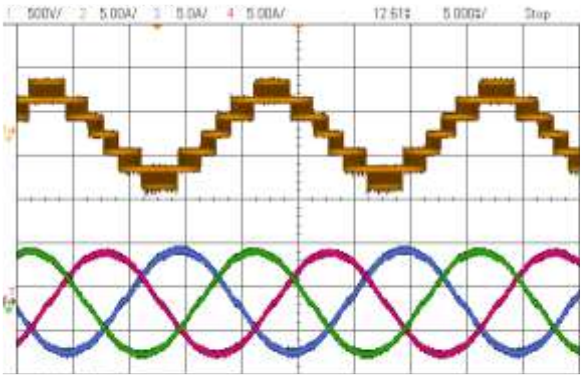
(g) f_s=30 kHz



(h) f_s=30 kHz



(i) f_s=40 kHz



(j) f_s=40 kHz

Figure 4.21 Test waveforms of the two-level inverter (a) (c) (e) (g) (i), and the four-level π-type inverter (b) (d) (f) (h) (j)

4.4.2 Harmonic analysis and comparison

Fig.4.22 shows the FFT analysis for test waveforms in Fig.4.21. Fig.4.22 (a) (b) (c) (d) show the conditions when f_s=10 kHz. Fig.4.22 (a) (b) show the FFT analysis for output current waveforms in Fig.4.21 (c) (d). As the output filter inductor is 6.32mH each phase, the THD of the line voltage and output current of the four-level π-type inverter are 24.60% and 2.86%, respectively. While the THD of

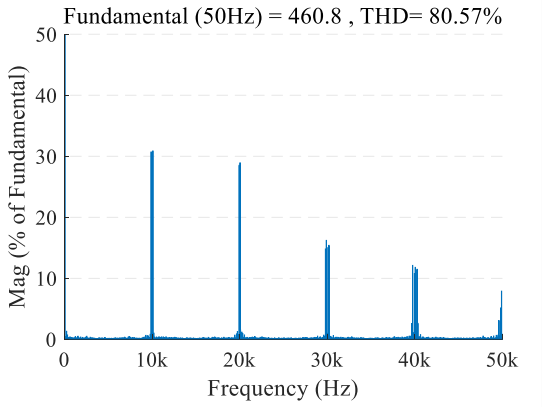
the line voltage and output current of the two-level inverter are 80.57% and 6.67%, respectively. Test results verify the four-level π-type inverter is able to output much lower output harmonics with the same output filter setting. It can prove on another side that smaller filters are required than that of the two-level converter when the output harmonic requirement is the same.

It can be noticed there is the decay on the fundamental components in Fig.4.22 (a) (c) of the four-level π-type converter. And this decay is higher than that in Fig.4.22 (d) (f) of the two-level converter. These decays on fundamental values are due to the dead-time injected to the PWM. The value of the decay on the output voltage practical value depends on the actual duration of the deadtime, switching frequency (switching period) as well as the switching voltage, which can be expressed as

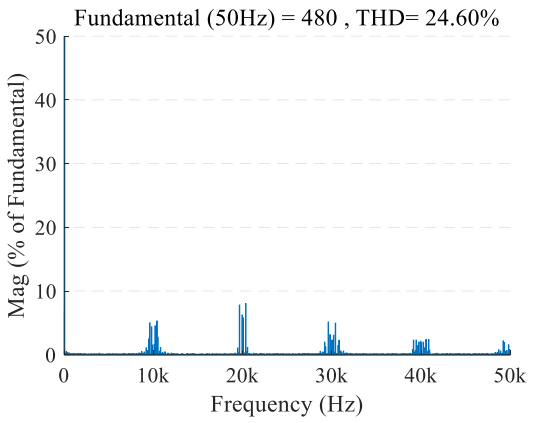
$$\Delta V_d = \frac{T_d}{T_s} V_{sw}$$

where ΔV_d is the value of the decay on the practical output voltage, T_d is the deadtime duration, T_s is the switching period, V_{sw} is the switching voltage. As the switching voltage of the four-level π-type converter is only 1/3 of the two-level converter, therefore, the actual amount of the decay on the four-level π-type converter is much smaller than that of the two-level converter. It can prove the dead-time will have less effect on the four-level π-type inverter compares to the two-level converter.

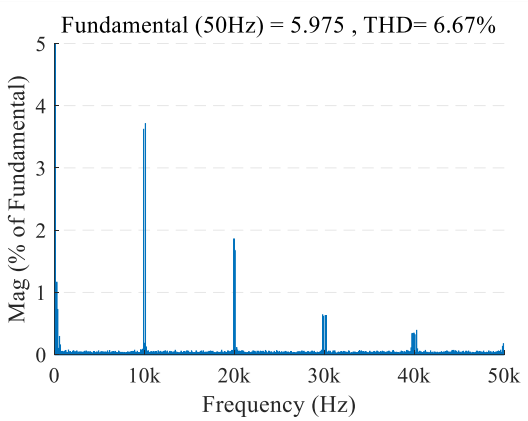
Fig.4.22 (e) (f) (g) (h) show conditions when f_s=20 kHz. It can be found out, with the increase of the switching frequency, output current harmonics contents of both topologies reduce to some extent. However, according to the previous power loss analysis, consider of the aspect of power losses, the two-level converter is very sensitive to the switching frequency. The higher the switching frequency, the higher the switching loss of the two-level converter, and the more significant drop of the output efficiency. In comparison, due to the much lower switching voltage on each switching device, switching losses of the four π-type converter are much lower than that of the two-level converter. Therefore, the four-level π-type converter has a much more flat output efficiency vs switching frequency curve. Consider either the harmonic content or high switching frequency applications, the four-level π-type inverter shows more advantages than the conventional two-level converter.



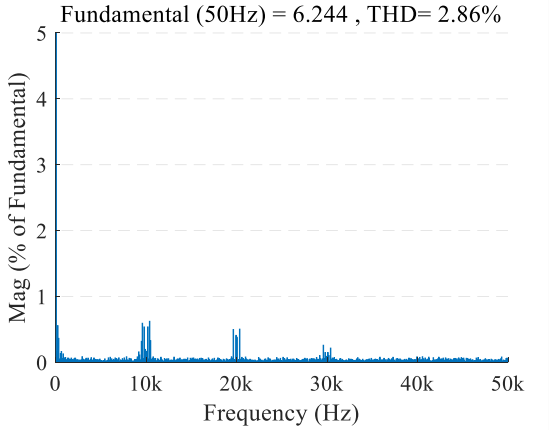
(a) Line voltage harmonics of the two-level inverter



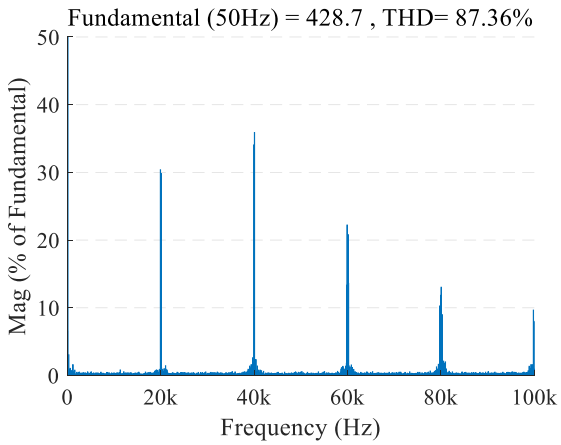
(b) Line voltage harmonics of the four-level π-type inverter



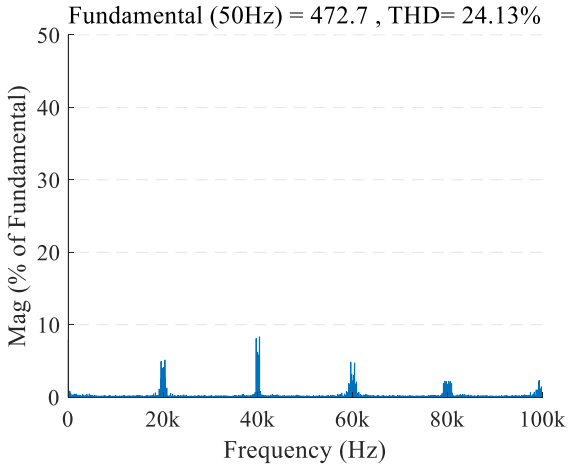
(c) Output current harmonics of the two-level inverter



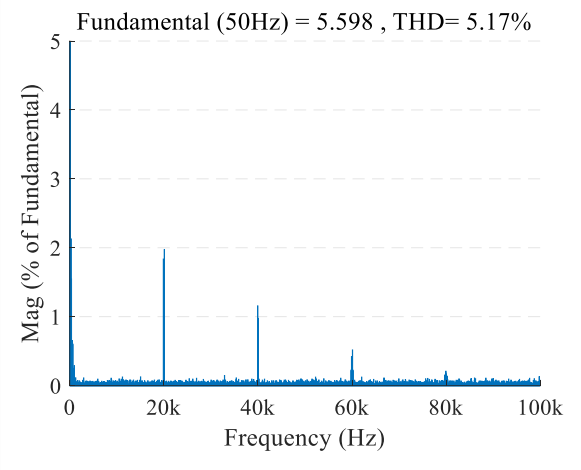
(d) Output current harmonics of the four-level π-type inverter



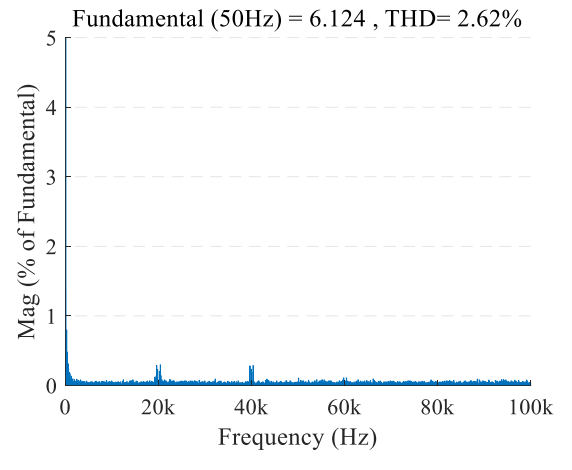
(e) Line voltage harmonics of the two-level inverter



(f) Line voltage harmonics of the four-level π-type inverter



(g) Output current harmonics of the two-level inverter

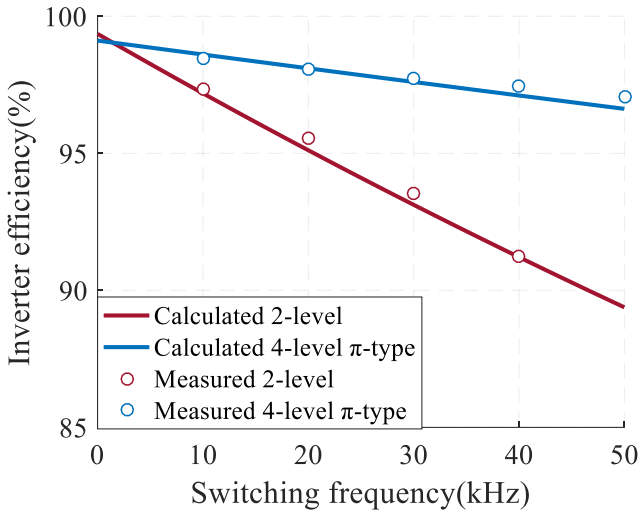


(h) Output current harmonics of the four-level π-type inverter

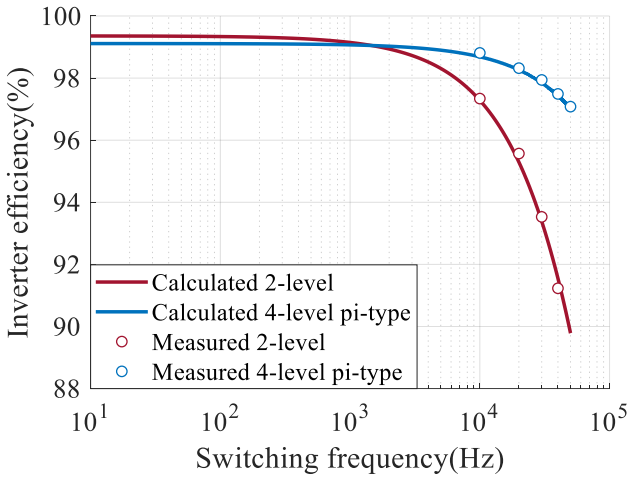
Figure 4.22 Harmonic analysis of test waveforms, fs=10 kHz: (a) (b) (c) (d), fs=20 kHz: (e) (f) (g) (h)

4.4.3 Efficiency simulation and test comparison

Fig.4.23 shows the efficiency measurement for both the four-level π-type inverter as well as the two-level inverter in comparison. The experimental efficiency curve on Fig.4.23 agrees with the calculation based on the proposed average analytical power loss model reasonably well for the four-level π-type inverter. It can be found out that actual measurements are a bit higher than calculation results when the switching frequency goes high. Apart from the measurement tolerance, the reason can be summarized into two parts. The first one is that all calculation parameters from the datasheet are based on the worst case (175°C junction temperature as mentioned in Section 4.2). However, the actual case temperature of devices measured through the thermal laser gun was about 40°C, which caused the difference of the power loss especially the switching loss at the higher switching frequency. The second one is the switching energy curve on the datasheet was based on a specific test setup. The converter prototype established in this paper has the different parasitic parameters due to the different PCB layout, which caused the switching power loss difference as well. In summary, experimental results match well with calculation results, which validated the proposed average power loss model for the converter. The efficiency doesn't drop too much with the increase of the switching frequency of the four-level π-type converter compare with the two-level converter. Fig.4.23 (b) sets the frequency axis as logarithm axis in order to show the cross point clearer.



(a)



(b)

Figure 4.23 Experimental results of efficiency measurements for four-level π-type converter and two-level converter (a) linear frequency axis (b) logarithm frequency axis

One thing needs to be mentioned that the test equipment as well as the measurement method can only measure the total converter operation loss. And as described in 4.4.3, experimental measurements can be used to verify the converter operation efficiency. The verification about the loss distribution on each switching device of the converter can not be made with the test method in this chapter. A good approach is to use the voltage probe and the current probe pair on each IGBT in order to measure the live voltage and live current of each individual switching device at the same time. Then use the math function on the oscilloscope to calculate the live conduction loss as well as the live switching loss of each switching

device within each fundamental period. For the three-phase four-level π-type converter, 18 differential voltage probes, 18 current probes as well as nine oscilloscopes with math function (assume four channels for each one) will be required. After the live conduction loss as well as the live switching loss have been measured, the switching device loss distribution can be verified. This is just a concept, the voltage probe bandwidth, the oscilloscope calculation capability as well as the total cost still need to be carefully concerned. It can be an interesting further investigation.

4.5 Summary of Chapter 4

This chapter investigated the power loss distribution and operation efficiency of the four-level π-type converter based on an average analytical average power loss model. This analytical average power loss model of this topology based on the average power loss expression of each individual switching device in order to proceed the analysis. The concept of this analytical average power loss is to provide the analytical average power loss expression as a function of such as IGBT collector current, power factor etc. within single fundamental period. The average analytical power loss investigated in this thesis is based on the pure sinusoidal modulation. The other pre-calculated modulation wave can also be used by changing conduction intervals summarized in TABLE IV.I to TABLE IV.IV as well as switching intervals summarized in Table IV.VII to TABLE IV.X. Based on the data from the devices datasheets, the proposal power loss model is able to provide the quick analysis for the converter system power loss distribution as well as the efficiency. Through the power loss model analysis as well as the efficiency curve comparison, the four-level π-type converter shows a higher efficiency than the two-level converter and three-level converters when the switching frequency is higher than 5 kHz due to the reduced switching loss. Meanwhile when the same output filter is employed, and operates at the same switching frequency, the four-level π-type converter presents lower output harmonics. It validated that in order to achieve the same output harmonic, the equivalent switching frequency of the four-level π-type converter can be kept low when compared to the two-level converter or three-level converters. This feature can reduce switching losses and the heatsink size for the compact application. Meanwhile, it can be derived if operates with the identical switching frequency, the filter required for the four-level π-type converter can be smaller. Either way can help for the reduce of the converter system volume or improve the system power density. This indicates the proposed four-level π-type converter topology is a qualified candidate

for low voltage applications such as compact applications as EVs and electric aircrafts where the power converter size should be kept as small as possible.

The theoretical converter operation efficiency calculation based on the proposed power loss model has been compared to experimental measurements. The case study is based on a four-level π-type inverter prototype as well as a two-level inverter prototype. Test parameters are chosen as the 600V dc-link input voltage, pure sinusoidal modulation with a 0.95 modulation index, unity output power factor, and a 2.5kW output power. By comparing calculation efficiencies and measured efficiencies, the experimental results of both the four-level π-type inverter and the two-level inverter match well with their corresponding theoretical calculations, which proved that the proposed average analytical power loss model works well to evaluate the operation efficiency of the four-level π-type converter

5 Control strategy for the four-level π-type converter

5.1 Introduction

In chapter 4, the analysis of the power loss distribution as well as the efficiency based on the proposed average analytical power loss model have implemented. The proposed four-level π-type converter has been verified has the higher efficiency compares to the popular two-level converter, the three-level T-type converter as well as the three-level diode NPC converter. It proved that the four-level π-type presents higher power efficiency when the switching frequency is more than 5 kHz. However, the experimental test in chapter 4 is based on the open-loop sinusoidal modulation operation, which means three individual dc power supply are required to supply its dc-link, otherwise, its dc-link NP voltage will drift. In order to resolve this problem and make it be able to operate with only one dc power supply, a proposed dc-link NP voltages balancing control strategy is investigated in this chapter. In this chapter, the dc-link NP voltages balancing control strategy for the proposed four-level π-type converter under the unity power factor condition (the worst case) has been presented. The dc-link NP voltages balancing strategy proposed in this section is based on the traditional level shifted CB-PWM. The core process to realize this control target can be briefly described as three steps. First, optimum zero-sequence signals will be dynamically selected according to a cost function which makes the energy variation on each dc-link capacitor as minimum as possible. Second, inject selected optimum zero-sequence signals into original sinusoidal modulation signals to form final modulation signals. Third, final modulation signals will compare with triangular carrier waves to generate desirable PWM signals to drive the converter and balance the dc-link NP voltages at the same time. The proposed control method is completely dynamic without the requirement of the preset look-up table. Meanwhile, in order to get a good NP voltage balancing control performance and fulfill the calculation speed of the existing control board at the same time, the system close loop bandwidth has been set equals to the PWM carrier frequency/converter switching frequency.

As the traditional level shifted CB-PWM control can be equivalent to the SVM, and the most important feature of this modulation is the minimum number of switching actions during each switching period. Therefore, when a single-end converter (inverter or rectifier) with more than three output voltage levels

is used, the dc-link NP voltages balancing can not be guaranteed at a high modulation index condition. To overcome this issue, a symmetrical back-to-back configuration is employed to make sure the system dc-link NP voltages can be balanced at high power factors and high modulation indices when power factors and modulation indices on both sides are the same. The back-to-back four-level π-type converter system has experimentally verified the proposed dc-link NP voltages control method with the symmetrical back-to-back structure. Meanwhile, with the back-to-back configuration, conditions when unity power factors on both sides but different modulation indices on both sides have been tested as well. And the guaranteed dc-link NP voltages balanced stable operation region when different modulation indices on both sides under the unity power factors has been summarized at the first time.

The work in this chapter has been published in [78], [178] by author.

5.2 DC-link NP voltages unbalancing analysis based on the four-level π-type converter

Before analyzing the dc-link NP voltages as well as their balancing control method, some assumptions need to be made first.

1) The total dc-link voltage should be constant. The influence of the dc-link voltage variance on the NP voltages can be eliminated. Actually, this can be realized by using a stable dc-link supply or a good dc-link voltage control loop.
2) Three dc-link capacitors have the same capacitance values.
3) The converter is three-phase symmetrical, operating under a three-phase balanced mode.
4) As mentioned in Chapter 3 and Chapter 4, the high frequency modulation index is adopted in this thesis, which means the carrier frequency is much higher than the fundamental frequency. Therefore, the values of phase current and modulation wave can be deemed as constant within each carrier period with the appropriate output filter employed.

It is known, there are two neutral paths clamped between dc-link NPs and the converter ac-side output. Therefore, similar to other multilevel NPC converters, the four-level π-type converter has the issue of three dc-link NP voltages drift problem. It is known that the function of these two neutral paths in the four-level π-type converter topology is to clamp the converter ac-side terminal to corresponding dc-link NPs in order to output desired voltage levels during the operation. Therefore, once one of these two

neutral paths conduct, the converter current will flow through the dc-link NP. Therefore, it will charge and discharge dc-link capacitors. Consequently, it will cause the valtage variation on them. As introduced in section 2.4.1, the fundamental criteria of the dc-link NP voltage balancing for the single phase-leg is the equally charge and discharge balance on each dc-link capacitor during each fundamental period. For the four-level converter, apart from regulating the top capacitor C3 and the bottom capacitor C1, the middle capacitor C2 should be dealt with special cares, otherwise, C2 will be fully discharged. Fig.5.1 presents four current flow situations on the two NPs N1 and N2 from the point of view of the single phase-leg structure. If the phase-leg output clamps to N2, and the current flows out of the converter. Then C3 charges, C1 and C2 discharge as shown in Fig.5.1 (a). If the phase-leg output clamps to N1, and the current flows into the converter. Then C1 charges, C2 and C3 discharge as shown in Fig.5.1 (b). If the phase-leg output clamps to N2, and the current flows into the converter. Then C3 discharges, C1 and C2 charge as shown in Fig.5.1 (c). If the phase-leg output clamps N1, and the current flows out of the converter. Then C1 discharges, C2 and C3 discharge as shown in Fig.5.1 (d). As introduced in section 2.4.1, the primary reason of the collapse of the dc-link NP voltage balancing condition for the multilevel NPC converter is the fully discharged inner capacitors due to the unbalance charge and discharge for them within one fundamental period for the single phase-leg. Therefore, for the four-level π-type converter, only the charge and discharge situation of C2 should be carefully analyzed here.

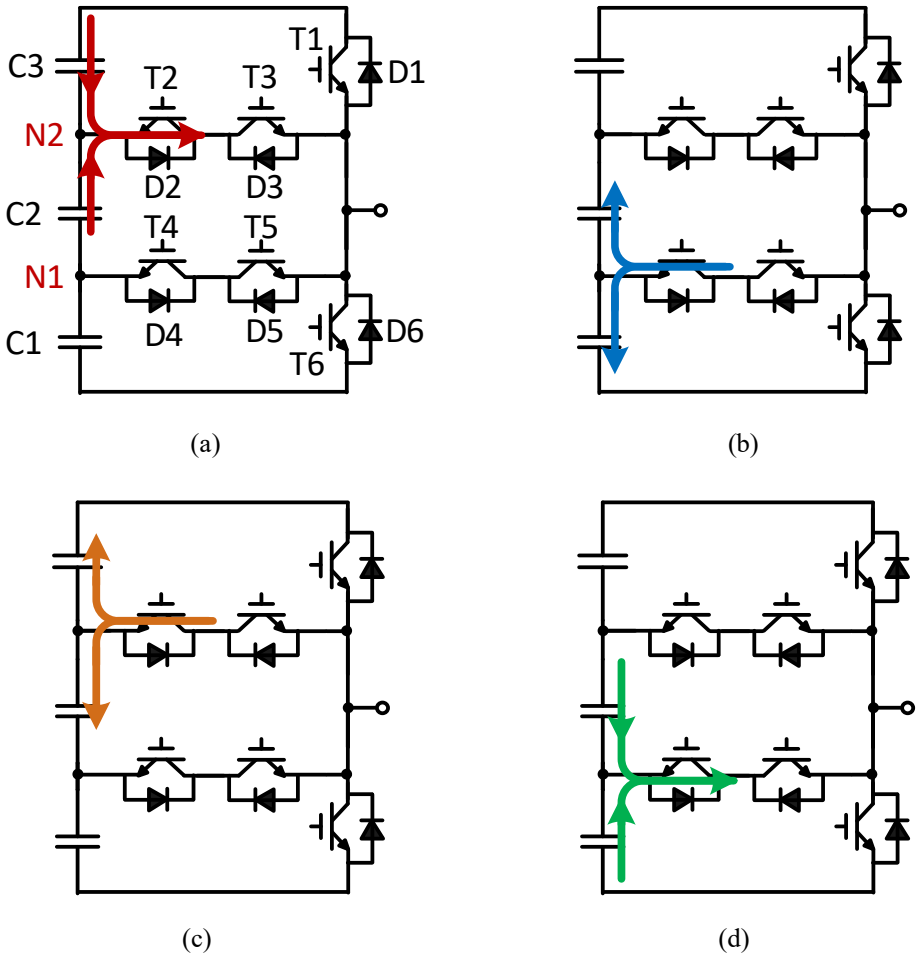


Figure 5.1 Situations of current flow paths with regards to N2 and N1. (a) current flows through N2 out of the converter (b) current flows through N1 into the converter (c) current flows through N2 into the converter (d) current flows through N1 out of the converter

Fig.5.2 illustrates charging and discharging conditions for C2 over one fundamental cycle based on the single phase-leg for the unity power factor situation and the zero power factor situation. Staircase output voltages are demonstrated here instead of PWM output voltages in order to simplify the analysis. Assume three dc-link capacitors voltages are balanced at the initial status. In Fig.5.2 (a), with the unity power factor, when the converter phase-leg output voltage level is E/2 or –E/2 with reference to the mid-point of the dc-link, the converter current always flows out of C2. Therefore, C2 keeps discharging in one fundamental period. Consequently, the voltage of C2 will eventually discharge to zero, which makes the total dc-link voltage distribute on C1 and C3. In contrast, with the zero power factor as shown in Fig.5.2 (b), when the converter phase-leg output voltage level is E/2 or –E/2, the converter current does not always flows out of C2. And the charging and discharging period for C2 are balanced within

one fundamental period. Even the above analysis is based on ideal situation, it still indicates that the higher the power factor, the harder dc-link NP voltages can be balanced for the proposed four-level π-type converter.

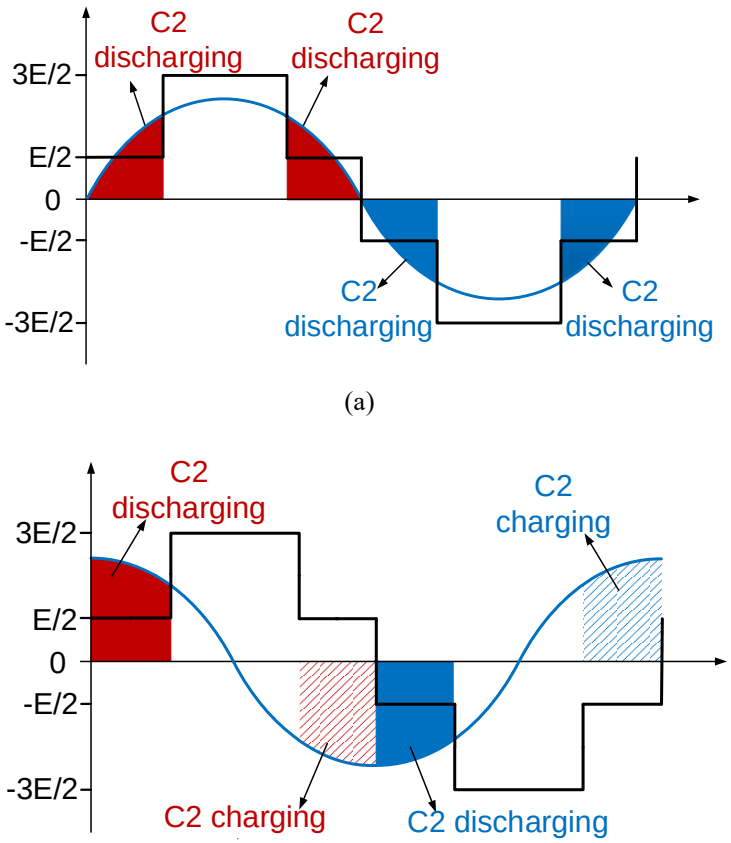


Figure 5.2 Charge and discharge conditions of C2 (a) unity power factor, (b) zero power factor

The above analysis is based on the single phase-leg configuration. From the point of view of the three-phase system, currents flow through two NPs N2 and N1 are not only from any specific single phase-leg, but are contributed by all three phase-legs. Therefore, some mathematical analysis regarding to neutral path currents has been presented below for the three-phase four-level π-type converter. Fig.5.3 shows the visual concept of neutral paths currents and three-phase output currents of the three-phase four-level π-type inverter.

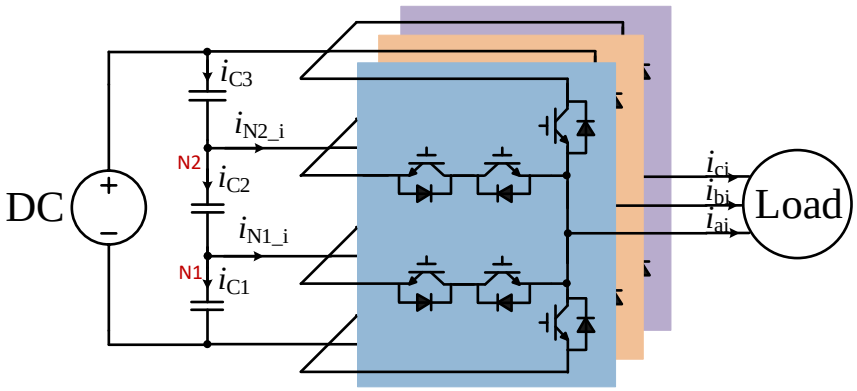


Figure 5.3 Neutral path currents and three-phase output currents of the three-phase four-level π-type inverter

According to sinusoidal modulation waves defined as (3.1), define inverter three-phase output currents as (5.1)

$$i_{ai} = I_i \cdot sin(\omega t + \varphi_i) \tag{5.1a}$$

$$i_{bi} = I_i \cdot sin\left(\omega t + \varphi_i - \frac{2\pi}{3}\right) \tag{5.1b}$$

$$i_{ci} = I_i \cdot sin\left(\omega t + \varphi_i + \frac{2\pi}{3}\right) \tag{5.1c}$$

Where, I_i is the peak inverter output current. Dynamically, at any time point, inverter neutral path currents i_{N2_i} and i_{N1_i} can be expressed as (5.2)

$$i_{N2\_i} = k_{aN2\_i} \cdot i_{ai} + k_{bN2\_i} \cdot i_{bi} + k_{cN2\_i} \cdot i_{ci} \tag{5.2a}$$

$$i_{N1\_i} = k_{aN1\_i} \cdot i_{ai} + k_{bN1\_i} \cdot i_{bi} + k_{cN1\_i} \cdot i_{ci} \tag{5.2b}$$

Take phase-A for example, where k_{aN2_i} and k_{aN1_i} are duty cycles of the inverter phase-A current acts as the neutral path current flows through N2 and N1, respectively. Their analytical expressions in different intervals under the sinusoidal modulation within each fundamental cycle have been analyzed in Section 4.2.1, Fig.4.2 to Fig.4.5, Table.IV.V, and can be expressed as (5.3)

$$k_{aN2\_i} = \begin{cases} \frac{3}{2}m_i \cdot \sin(\omega t) + \frac{1}{2} & 0 \le \omega t \le sin^{-1}(\frac{1}{3m_i}) \\ -\frac{3}{2}m_i \cdot \sin(\omega t) + \frac{3}{2} & sin^{-1}\left(\frac{1}{3m_i}\right) \le \omega t \le \pi - sin^{-1}(\frac{1}{3m_i}) \\ \frac{3}{2}m_i \cdot \sin(\omega t) + \frac{1}{2} & \pi - sin^{-1}\left(\frac{1}{3m_i}\right) \le \omega t \le \pi + sin^{-1}(\frac{1}{3m_i}) \\ 0 & \pi + sin^{-1}\left(\frac{1}{3m_i}\right) \le \omega t \le 2\pi - sin^{-1}(\frac{1}{3m_i}) \\ \frac{3}{2}m_i \cdot \sin(\omega t) + \frac{1}{2} & 2\pi - sin^{-1}\left(\frac{1}{3m_i}\right) \le \omega t \le 2\pi \end{cases} \tag{5.3a}$$

$$k_{aN1\_i}=\begin{cases}-\frac{3}{2}m_i\cdot\sin(\omega t)+\frac{1}{2} & 0\le\omega t\le sin^{-1}(\frac{1}{3m_i})\\ 0 & sin^{-1}\left(\frac{1}{3m_i}\right)\le\omega t\le\pi-sin^{-1}(\frac{1}{3m_i})\\ -\frac{3}{2}m_i\cdot\sin(\omega t)+\frac{1}{2} & \pi-sin^{-1}\left(\frac{1}{3m_i}\right)\le\omega t\le\pi+sin^{-1}(\frac{1}{3m_i})\\ \frac{3}{2}m_i\cdot\sin(\omega t)+\frac{3}{2} & \pi+sin^{-1}\left(\frac{1}{3m_i}\right)\le\omega t\le 2\pi-sin^{-1}(\frac{1}{3m_i})\\ -\frac{3}{2}m_i\cdot\sin(\omega t)+\frac{1}{2} & 2\pi-sin^{-1}\left(\frac{1}{3m_i}\right)\le\omega t\le 2\pi\end{cases}\quad(5.3b)$$

Neutral path currents duty cycles for Phase-B and Phase-C can be calculated by the similar method. Then the average neutral path currents during each fundamental cycle $\bar{\imath}_{N2\_i}$ and $\bar{\imath}_{N1\_i}$ can be calculated by using the integration calculation

$$\bar{\imath}_{N2\_i}=\frac{1}{2\pi}\int_0^{2\pi}(k_{aN2_i}\cdot i_{ai}+k_{bN2_i}\cdot i_{bi}+k_{cN2_i}\cdot i_{ci})d\omega t$$

$$\bar{\imath}_{N1\_i}=\frac{1}{2\pi}\int_0^{2\pi}(k_{aN1_i}\cdot i_{ai}+k_{bN1_i}\cdot i_{bi}+k_{cN1_i}\cdot i_{ci})d\omega t$$

Finally, the analytical expression of average neutral path currents can be expressed as (5.4)

$$\bar{\imath}_{N2\_i}=\frac{3}{8\pi}I_i\cdot cos\varphi_i(-3m_i\pi+18m_i\cdot sin^{-1}\left(\frac{1}{3m_i}\right)+2\sqrt{\frac{9m_i^2-1}{m_i^2}})\quad(5.4a)$$

$$\bar{\imath}_{N1\_i}=-\frac{3}{8\pi}I_i\cdot cos\varphi_i(-3m_i\pi+18m_i\cdot sin^{-1}\left(\frac{1}{3m_i}\right)+2\sqrt{\frac{9m_i^2-1}{m_i^2}})\quad(5.4b)$$

In order to make the dc-link NP voltages balancing, $\bar{\imath}_{N2\_i}$, $\bar{\imath}_{N1\_i}$ have to be zero. However, through (5.4) it can be derived that, with the sinusoidal modulation, when the inverter ac-side power factor $cos\varphi_i\neq 0$(real power transfer exists), $\bar{\imath}_{N2\_i}$ and $\bar{\imath}_{N1\_i}$ can not be zero, and results in deviations of the dc-link capacitors voltages. As introduced in section 2.4.2.3, the NTV PWM-based dc-link NP voltage balancing control strategy is able to prevent drifts of dc-link NP voltages of the four-level and five-level NPC converter, but with the ac-side modulation index upper limit 0.6 under the unity power factor condition [28][41].

As introduced in section 2.4.2.3, one method to extend the operation modulation index under the unity power factor condition for the multilevel NPC converter is to use the back-to-back configuration. For the four-level π-type converter topology, the corresponding back-to-back configuration is shown in Fig. 5.4.

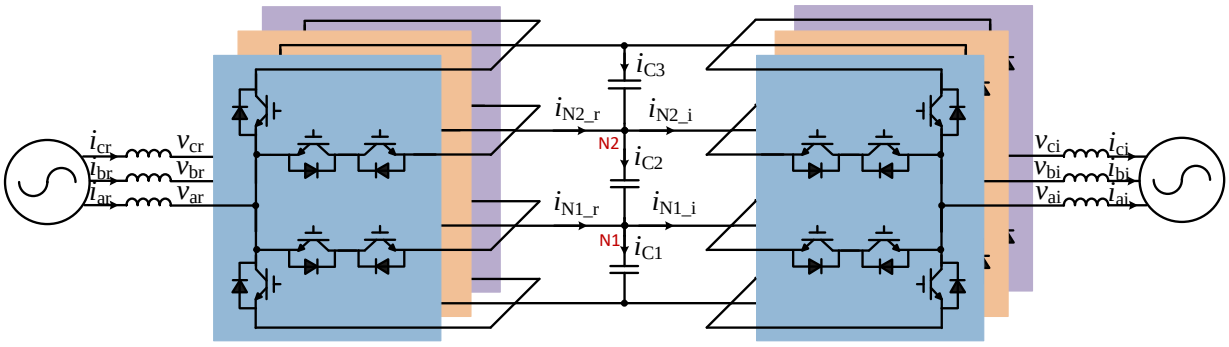


Figure 5.4 Back-to-back four-level π-type converter structure with a bidirectional power-flow structure

If the sinusoidal modulation is employed, average neutral path currents contributed by the front-end rectifier during each fundamental period can be expressed as (5.5)

$$\bar{\imath}_{N2\_r} = \frac{3}{8\pi} I_r \cdot cos\varphi_r \left(-3m_r\pi + 18m_r \cdot sin^{-1}\left(\frac{1}{3m_r}\right) + 2\sqrt{\frac{9m_r^2-1}{m_r^2}}\right) \quad (5.5a)$$

$$\bar{\imath}_{N1\_r} = -\frac{3}{8\pi} I_r \cdot cos\varphi_r \left(-3m_r\pi + 18m_r \cdot sin^{-1}\left(\frac{1}{3m_r}\right) + 2\sqrt{\frac{9m_r^2-1}{m_r^2}}\right) \quad (5.5b)$$

In order to guarantee dc-link NP voltages balancing, the net average current of the neutral paths within one fundamental period should be enforced to zero, i.e.

$$\bar{\imath}_{N2\_r} = \bar{\imath}_{N2\_i}$$

$$\bar{\imath}_{N1\_r} = \bar{\imath}_{N1\_i}$$

The active power of the rectifier and the inverter P_r and P_i can be expressed as follow, where, m_r and m_i are their corresponding modulation indices. V_{rp} and V_{ip} are rectifier and inverter ac-side peak phase voltages.

$$P_r = \frac{3}{2} V_{rp} \cdot I_r \cdot cos\varphi_r$$

$$P_i = \frac{3}{2} V_{ip} \cdot I_i \cdot cos\varphi_i$$

$$m_r = \frac{V_{rp}}{0.5V_{DC}}$$

$$m_i = \frac{V_{ip}}{0.5V_{DC}}$$

Considering the power balance on both sides, the active power in the rectifier side should be equal to the active power in the inverter side (assume the ideal switching action), then

$$I_r = I_i \cdot \frac{m_i \cdot cos\varphi_i}{m_r \cdot cos\varphi_r}$$

Consequently,

$$m_i\left(-3m_r\pi + 18m_r \cdot sin^{-1}\left(\frac{1}{3m_r}\right) + 2\sqrt{\frac{9m_r^2-1}{m_r^2}}\right) \tag{5.6}$$
$$= m_r\left(-3m_i\pi + 18m_i \cdot sin^{-1}\left(\frac{1}{3m_i}\right) + 2\sqrt{\frac{9m_i^2-1}{m_i^2}}\right)$$

(5.6) indicates that when the back-to-back three-phase four-level π-type converter system as shown in Fig.5.4, and transfers the active power between the rectifier and the inverter, nonzero average neutral paths currents always occur. It has been analyzed as shown in Fig.5.2. Therefore, only the case m_r=m_i implies that $\bar{\imath}_{N2\_r} = \bar{\imath}_{N2\_i}$ and $\bar{\imath}_{N1\_r} = \bar{\imath}_{N1\_i}$. If the modulation indices on both sides are not the same, then $\bar{\imath}_{N2\_r} \neq \bar{\imath}_{N2\_i}$ and $\bar{\imath}_{N1\_r} \neq \bar{\imath}_{N1\_i}$, the middle capacitor C2 will finally be fully discharged, and the bottom capacitor C3 as well as the top capacitor C1 will be unequally charged or discharged. DC-link NP voltage will not be balanced. This concludes that the pure sinusoidal modulation can not guarantee the dc-link capacitors voltages balancing, and not practical to implement.

Through the analysis above, even the back-to-back configuration has the feature to compensate the neutral path currents from both sides, the dc-link NP voltages balancing condition only applies to the same modulation indices on both sides if the sinusoidal modulation is employed. If initial voltages on each dc-link capacitor are different, or modulation indices are different on both sides, the dc-link NP voltages would tend to imbalance, and lead to the system unstable. Therefore, the appropriate dc-link NP voltage balancing close loop controller must be provided. In the next section, the CB-PWM based dc-link NP voltages balancing control method will be introduced and analyzed. The actual performance as well as the limit (different modulation indices on both sides) under the unity power factor condition will be tested by prototype in section 5.4 as well.

5.3 DC-link NP voltages balancing control

The proposed dc-link NP voltages balancing control scheme is a level shifted CB-PWM with desired zero-sequence signal injection. Therefore, the actual final modulation wave for the converter consists of two parts: sinusoidal fundamental components and zero sequence components as presented in (5.7).

$$u_i(t) = u_i^*(t) + c(t) \qquad i = a,b,c \tag{5.7}$$

where, $u_i(t)$ are modified final modulation waveforms. $c(t)$ are zero-sequence components. $u_i^*(t)$ are original sinusoidal fundamental waveforms in order to get the sinusoidal current waveforms.

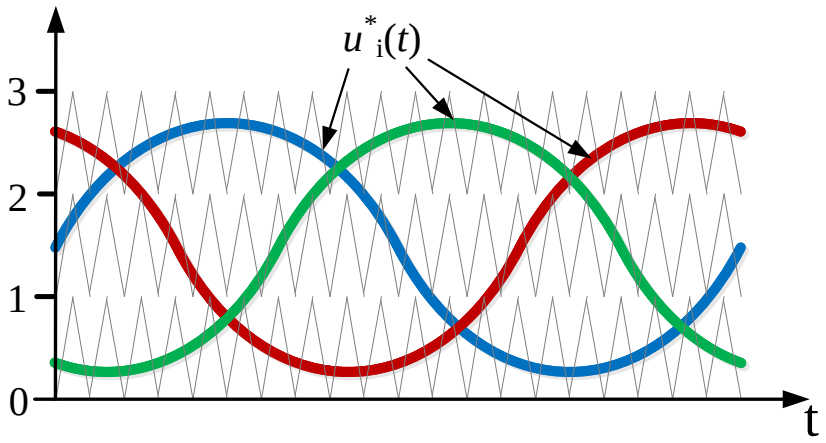


Figure 5.5 The relationship between carrier waves and modulation waves in a level shifted CB-PWM

As the level shifted CB-PWM scheme adopted for control is shown in Fig.5.5, three-phase sinusoidal fundamental components can be obtained by normalizing three-phase output phase voltage fundamental components with 1/3 of the dc-link voltage as introduced in section 3.2. Therefore, the p.u. value of three-phase fundamental components with regards to the negative terminal of the dc-bus will be in the range of 0~3. Thus, three-phase original sinusoidal fundamental waveforms $u_i^*(t)$ are expressed as below

$$\begin{cases} u_a^*(t) = 1.5m \cdot \sin(\omega t) + 1.5 \\ u_b^*(t) = 1.5m \cdot \sin\left(\omega t + \frac{2\pi}{3}\right) + 1.5 \\ u_c^*(t) = 1.5m \cdot \sin\left(\omega t - \frac{2\pi}{3}\right) + 1.5 \end{cases}$$

Technically, sinusoidal fundamental components can be obtained from the output of the converter current control loop, which is employed in order to control the converter fundamental current and track the desired reference value. At the same time, desired zero-sequence components can be obtained according to the appropriate cost function, then inject into three-phase fundamental components simultaneously to manipulate three dc-link capacitors voltages and extend the output voltage at the same time. Meanwhile, from the point of view of the practical realization (the discrete operation), zero-sequence components can be deemed as the same offset value injected to three-phase sinusoidal signals within each sampling period. Therefore, for a three-phase system, the effect of the zero-sequence can

be eliminated at the output line voltage as well as the output current.

In order to guarantee the linear modulation without any overmodulation, the equivalent range of modified modulation waves are shown as following

$$0 \le u_i(t) = u_i^*(t) + c(t) \le 3$$

The slash area in Fig.5.6 illustrates the region that three-phase modulation waves can be approached maximally by injecting zero-sequence components graphically.

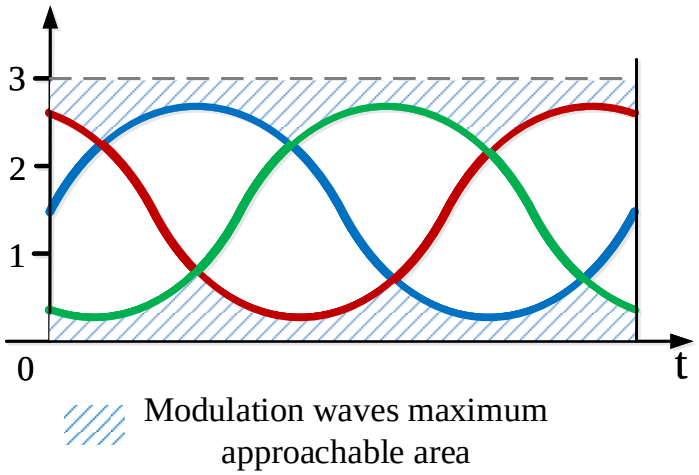


Figure 5.6 Modulation waves maximum approachable region

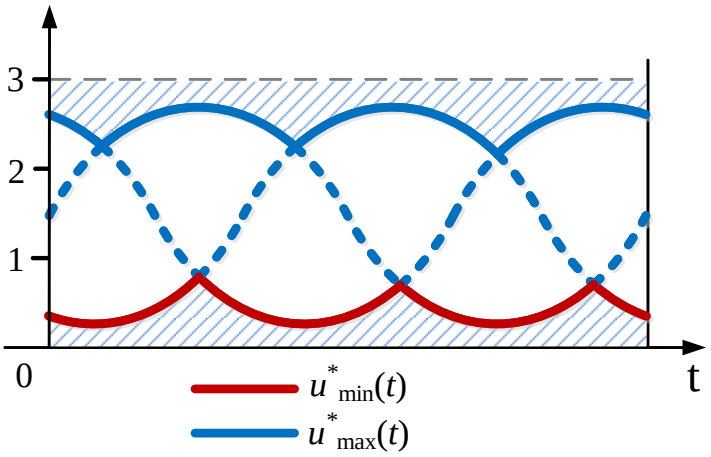
Therefore, the range of zero-sequence components $c(t)$ that can be injected into three-phase sinusoidal fundamental components can be expressed as in (5.8)

$$-u_{\min}^*(t) \le c(t) \le 3 - u_{\max}^*(t) \tag{5.8}$$

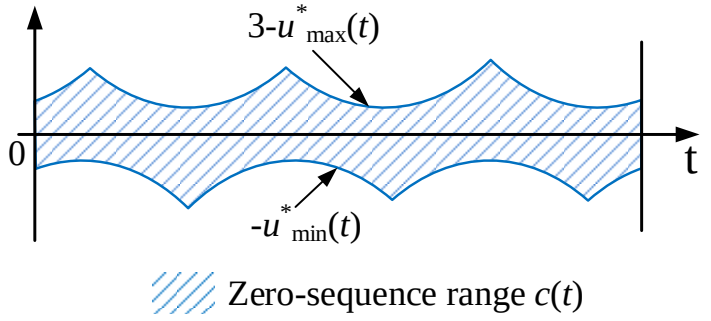
where, $u^*_{\max}(t)$ and $u^*_{\min}(t)$ are maximum and minimum values of three-phase sinusoidal fundamental components. Fig.5.7 (a) shows $u^*_{\max}(t)$ and $u^*_{\min}(t)$ graphically, where the top solid blue line is $u^*_{\max}(t)$ and the bottom solid red line is $u^*_{\min}(t)$. They can be expressed in (5.9)

$$\begin{cases} u_{\min}^*(t) = \min(u_a^*(t), u_b^*(t), u_c^*(t)) \\ u_{\max}^*(t) = \max(u_a^*(t), u_b^*(t), u_c^*(t)) \end{cases} \tag{5.9}$$

Finally, according (5.8) the available zero-sequence component can be used to inject into sinusoidal fundamental components is shown in Fig.5.7 (b).



(a)



(b)

Figure 5.7 Visual concept of (a) u*max and u*min (b) available zero-sequence component

In the process of modulation, zero-sequence signals are the only freedom degree that can be adjusted. Therefore, the key point of this control and modulation scheme is to find out optimum zero-sequence components within the available range of zero-sequence components which expressed in (5.8). With respect to the appropriate cost function/target, optimum zero-sequence components should be selected within the range in (5.8). The operable method is within each sampling period/switching period, several samples within the available range in (5.8) can be selected. For instance, as shown in Fig.5.8, from the point of view of discretization, within each sampling period, the available zero sequence components range $3\text{-}u^*_{max}(t) + u^*_{min}(t)$ will be equally divided into several parts, each part will then be sampled and evaluated in the incoming appropriate cost function. The one which can achieve the relevant optimum value of the cost function will be finally picked. In theory, the number of the above mentioned equally sampling method should be as many as possible, however, in practical implementation, this number depends on the actual system clock speed of the control chip as well as the time consumption of the

control algorithm code. In order to make sure the control code can be run thoroughly within each sampling period and get the desired PWM output refreshed within each sampling period, therefore, based on the control board introduced in section 4.4, 3- $u^*_{max}(t) + u^*_{min}(t)$ within each sampling period has been equally divided into 5 section, which means six potential zero-sequence components samples have been selected evenly according to (5.8) and evaluated through the cost function within each sampling period as shown in Fig.5.8. And this has been verified in section 5.5.

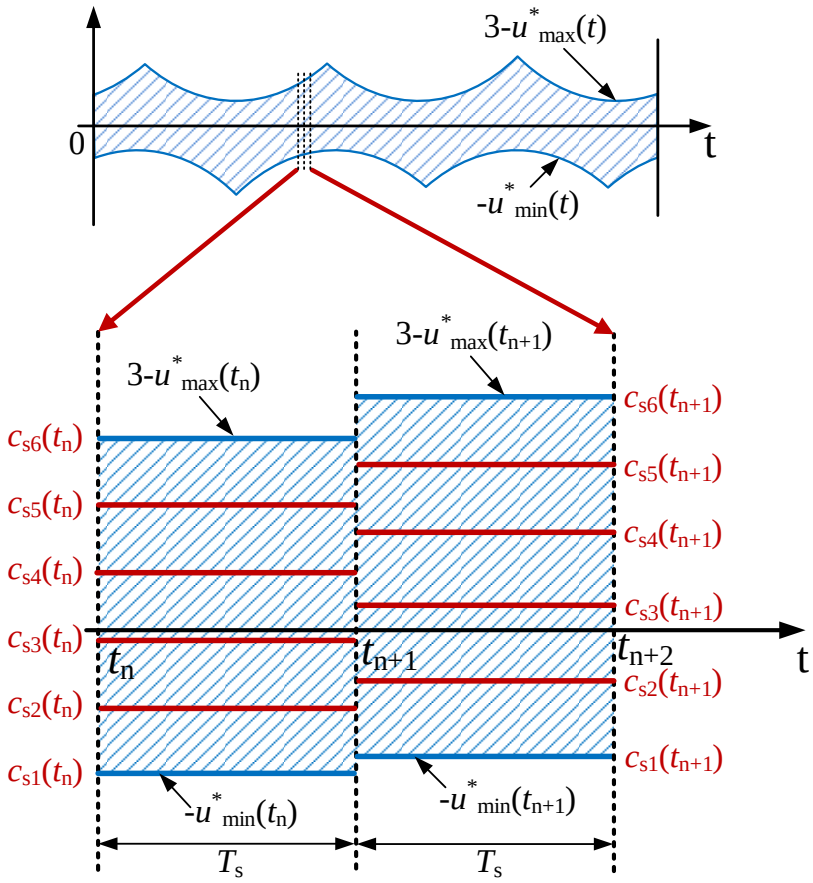


Figure 5.8 Discretization implementation concept of the zero-sequence components sampling method from the available zero-sequence components range

Then, how to select the appropriate cost function in order to balance dc-link NP voltages of a four-level π-type converter? The control cost function can be selected and established in order to minimize the energy variation J on each dc-link capacitor. The expression of the dc-link capacitor energy variation J is shown in (5.10) [38][51][169]

$$J = \frac{1}{2} C \sum_{j=1}^{3} \Delta v_{Cj}^2 = \frac{1}{2} C \sum_{j=1}^{3} (v_{Cj} - \frac{V_{dc}}{3})^2 \tag{5.10}$$

where, V_{dc} is the whole dc-link voltage. v_{Cj} is the actual measured voltage of the corresponding dc-link capacitor. Δv_{Cj} is the voltage deviation on the dc-link capacitor C_j in Fig.5.1 (a) from its reference value (1/3 of the total dc-link voltage V_{dc}). C is the capacitance value of each capacitor. According to (5.10), the parameter J is the summation of the quadratic operation $(v_{Cj} - \frac{V_{dc}}{3})^2$ for all three dc-link capacitors, which should be positive defined. Therefore, the relevant optimum zero-sequence component should be selected upon J has been minimized and close to zero as much as possible. Consequently, when J is minimized, the value of $\frac{dJ}{dt}$ should be no larger than zero and should be as negative as possible as shown in (5.11).

$$\frac{dJ}{dt} = C\sum_{j=1}^{3}\Delta v_{Cj}\frac{dv_{cj}}{dt} = \sum_{j=1}^{3}\Delta v_{Cj}i_{Cj} \le 0 \tag{5.11}$$

where, i_{Cj} are currents flowing through capacitors C_j. (5.11) can relate the dc-link capacitor energy variation J to dc-link capacitor currents i_{Cj}. As there will be six candidate zero-sequence components selected first as shown in Fig.5.8 to evaluate the value of (5.11) within each sampling period, therefore, the one which can lead to the most negative value of (5.11) will be finally selected. And of course, if none of the six candidate zero-sequence components can get a negative value of (5.11), the one which can make (5.11) close to 0 the most will be selected. One thing should be noticed that if the system is the back-to-back configuration, dc-link capacitor currents will be contributed by both the rectifier and the inverter side. Thus, for the back-to-back configuration, $i_{Cj} = i_{Cjr} + i_{Cj_i}$, where, i_{Cjr} are capacitors currents contributed by the rectifier, and i_{Cji} are capacitors currents contributed by the inverter.

Therefore, with the available zero-sequence components constraint defined in (5.8), the final cost function for the dc-link NP voltages balancing control can be expressed as (5.12).

$$\begin{cases} \min V = \sum_{j=1}^{3}\Delta v_{Cj}i_{Cj} = \sum_{j=1}^{3}(v_{Cj} - \frac{V_{dc}}{3})\cdot i_{Cj} \\ \text{Constriant}: \quad -u^*_{\min}(t) \le c(t) \le 3 - u^*_{\max}(t) \end{cases} \tag{5.12}$$

The next step is to find out the relationship between the cost function and available zero-sequence components in order to evaluate each zero-sequence component sample against the cost function. In (5.12), Δv_{Cj} can be obtained from the voltage sensor measurement. Therefore, the key is to find the

relationship between i_{Cj} and $c(t)$. Before that, the relationship between i_{Cj} in (5.12) and i_{N1}, i_{N2} can be derived as presented in Fig.5.9.

In Fig.5.9 (a), the converter output terminal is clamped to N1. It makes the converter output phase voltage equal to E. Assume the direction of arrows in Fig.5.9 are positive, the current flows through C1 can be expressed as follow

$$i_{C1} = -C \cdot \Delta V$$

The currents flow through C3 and C2 are

$$i_{C2} = i_{C3} = \frac{C}{2} \cdot \Delta V$$

Assume the total dc-link voltage is constant, the voltage variation on C1 equals to the whole voltage variation across C2 and C3. Then, the relationship between the i_{N1} and i_{C1}, i_{C2} and i_{C3} can be expressed as shown in (5.13a)

$$i_{C1} = -2i_{C2}$$

$$i_{C2} - i_{C1} = i_{N1}$$

$$\begin{cases} i_{C1} = -\frac{2}{3} i_{N1} \\ i_{C2} = \frac{1}{3} i_{N1} \\ i_{C3} = \frac{1}{3} i_{N1} \end{cases} \tag{5.13a}$$

Similarly, in Fig.5.9 (b), the converter output is clamped to N2. It makes the converter output phase voltage equal to 2E. With same method above, the relationship between i_{N2} and i_{C1}, i_{C2} and i_{C3} can be expressed as shown in (5.13b)

$$\begin{cases} i_{C1} = -\frac{1}{3} i_{N2} \\ i_{C2} = -\frac{1}{3} i_{N2} \\ i_{C3} = \frac{2}{3} i_{N2} \end{cases} \tag{5.13b}$$

Therefore, combine (5.13a) and (5.13b), the relationship between dc-link capacitors currents and neutral paths currents for the inverter operation can be established as shown in (5.14a). Similarly, the

relationship between dc-link capacitor currents and dc-link NP currents for the rectifier operation can be established as in (5.14b).

$$\begin{cases} i_{C1} = -\frac{1}{3} i_{N2} - \frac{2}{3} i_{N1} \\ i_{C2} = -\frac{1}{3} i_{N2} + \frac{1}{3} i_{N1} \\ i_{C3} = \frac{2}{3} i_{N2} + \frac{1}{3} i_{N1} \end{cases} \tag{5.14a}$$

$$\begin{cases} i_{C1} = \frac{1}{3} i_{N2} + \frac{2}{3} i_{N1} \\ i_{C2} = \frac{1}{3} i_{N2} - \frac{1}{3} i_{N1} \\ i_{C3} = -\frac{2}{3} i_{N2} - \frac{1}{3} i_{N1} \end{cases} \tag{5.14b}$$

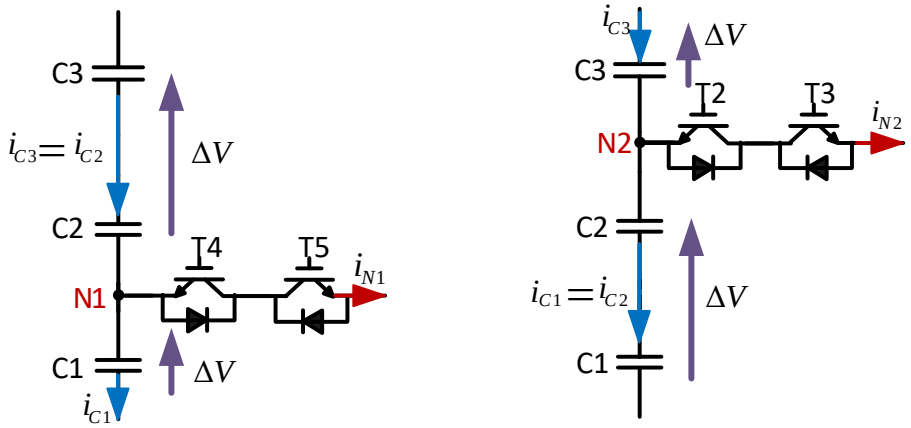


Figure 5.9 Relationship between dc-link capacitor current and neutral path currents (a) current flows through N1 (b) current flows through N2

The relationship between neutral currents (i_{N1}, i_{N2}) and zero-sequence components $c(t)$ can be derived as follows. Since the value of three-phase modulation waves has the range of 0~3, when a random point of one of modulation waves has been sampled, the integer part of this sample point (u_i) represents the voltage level (int(u_i)), while the fractional part determines the duty cycle (frac(u_i)). For example, when the modulation wave value is 1.2, it means the voltage level is 1 and the corresponding duty cycle for the switching device is 0.2. In this case, the output commutation is between E and 2E as illustrated in Fig.5.10. When commutations involve output phase voltage level 2E and E, the duty cycle of

corresponding switching devices can be adjusted. Therefore, i_{N1}, i_{N2} can be determined by (int(u_i)) and (frac(u_i)).

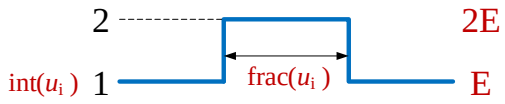


Figure 5.10 Concept of the modulation wave level and corresponding duty cycle

It can be found out that final modulation waves u_i can be regulated by zero-sequence components, which explains why zero-sequence components can affect neutral path currents, dc-link capacitor currents and eventually the cost function in (5.12). Therefore, the relationship between neutral path currents i_{N1}, i_{N2} and three-phase final modulation waves can be formulated as shown in (5.15) according to the method in [179].

$$\begin{cases} i_{N1}= \sum_{i=a,b,c} i_i\times[(\text{int}(u_i) == 0)\times\text{frac}(u_i)+(\text{int}(u_i)==1)\times(1-\text{frac}(u_i))] \\ i_{N2}= \sum_{i=a,b,c} i_i\times[(\text{int}(u_i) == 1)\times\text{frac}(u_i)+(\text{int}(u_i)==2)\times(1-\text{frac}(u_i))] \end{cases} \tag{5.15}$$

where, i_a, i_b, i_c are converter ac-side three-phase currents. int(u_i)= =0 is the operation used to check whether the reference voltage level is 0 or not. If it is zero, then (int(u_i)= =0) equals to 1, otherwise 0. It is obvious that when int(u_i) equals to 1 or 2, the converter output clamps to N1 or N2, and currents flow through N1 or N2. Therefore, the amount of neutral path currents can be adjusted by frac(u_i).

With (5.7) to (5.15), the relationship between the control objective and the zero-sequence signal can be established. Fig.5.11 presents this control algorithm in the format of a flow chart in order to present this control algorithm intuitively. In summary, the modulation and the NP voltages balancing control algorithm can be implemented as follows. First step, original three-phase fundamental components $u_i^*(t)$ are obtained from the current control loop (generally, it can be the Proportional-Integral (PI) control-based current loops). Second step, using (5.8) and (5.9), the range of available zero-sequence components can be defined. Third step, within each sampling period, equally sample six values within the available range of the zero-sequence components in (5.8), and add them to the original fundamental components one by one to obtain the potential reference voltages by using (5.7). that Fourth step, using (5.10) to (5.15) to check which zero-sequence component sampled in the third step above leads to the

minimum value of the objective function in (5.11). That zero-sequence component will be selected to form the final reference voltage. After the reference voltage is obtained, it will be compared with three triangle carrier-signals to generate the PWM signals for the device gate drivers. All these four steps should be done thoroughly within each sampling period.

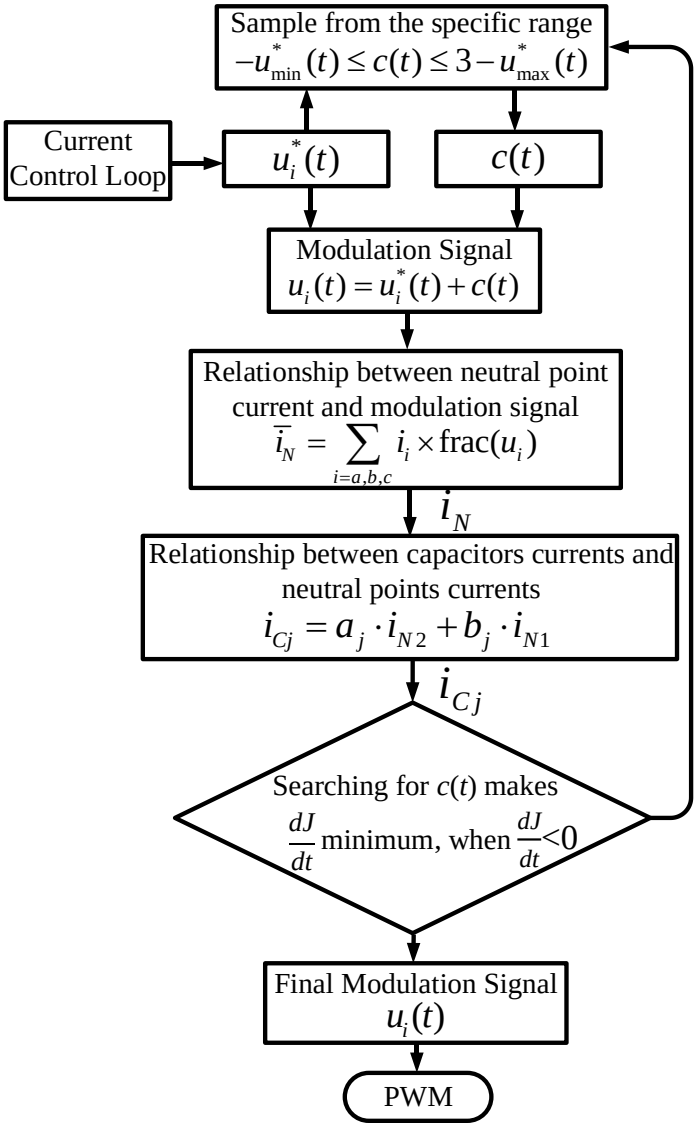


Figure 5.11 DC-link NP voltages balancing control algorithm flow chart

5.4 Simulation analysis

This section presents simulation results of the four-level π-type converter in order to give an initial validation for the proposed dc-link NP voltages balancing control strategy introduced in this chapter. The simulation model's setup parameters are summarized in Table V.I. Screen shots of the detail of the

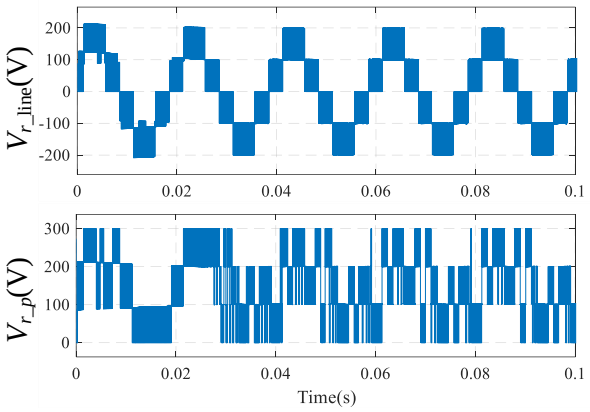
simulation blocks are presented in Appendix D. I and II. The Solver of the simulation models are selected as discrete, and Zero-order Hold is employed in order to imitate the ADC sampling process of the practical circuit. The Internal resistance Ron is selected as the default value 0.01 in order to make it similar to a practical IGBT. The snubber resistance and capacitance are selected as the default. In practical, initial voltages of dc-link capacitors usually differ to the desirable value 100V. Therefore, initial voltages of the upper and lower capacitors C3 and C1 are set as 80V, while the initial voltage of the middle capacitor C2 is set as 120V before the PWM signals applied on them. This setup will be able to simulate the practical startup process of the topology, and test the NP voltage balancing control strategy capability at the same time.

TABLE V.I THREE-PHASE FOUR-LEVEL Π-TYPE CONVERTER SYSTEM SIMULATION PARAMETERS

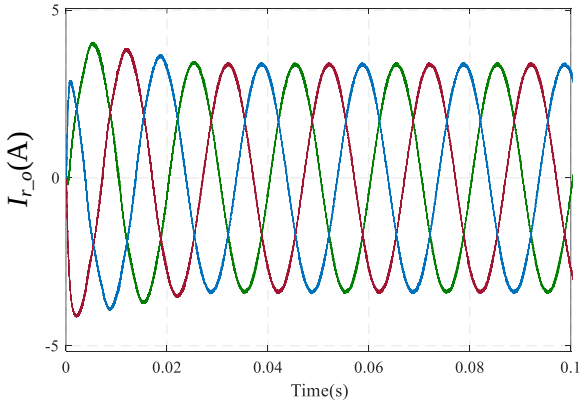
Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs in powergui
Zero-Order Hold sample time	100 μs
Deadtime model	On/Off Delay (On delay, Time delay:2μs)
Sinusoidal fundamental signals generator model for the inverter	Sine Wave (Sine type: Time based, Time(t): Use simulation time, Frequency=100π rad/s (50Hz), Phase=[0, 2/3π, -2/3π] rad, Sample time=0)
Triangular carrier wave generator model for the inverter	Repeating table (frequency = 10 kHz)
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, C=2000μF, cap initial voltage: C1=C3=80V, C2=120V)
DC-link parallel protection resistors model	Series RLC Branch (Branch type: R, resistance value: 100kΩ)
Inverter side load model	Three-Phase Series RLC Branch (Branch type: RL, Resistance=25Ω, Inductance=5mH)
Three-phase grid voltage model (back-to-back only)	Three-Phase Programmable Voltage Source (Generator type: swing)
Rectifier input choke (back-to-back only)	Three-Phase Series RLC Branch (Branch type: RL, Resistance=0.2Ω, Inductance=2mH)

Fig.5.12 presents simulation waveforms of the three-phase single-end four-level π-type inverter (the simulation model is shown in Appendix D I). Test parameters are set as: total dc-link input V_{dc}=300V,

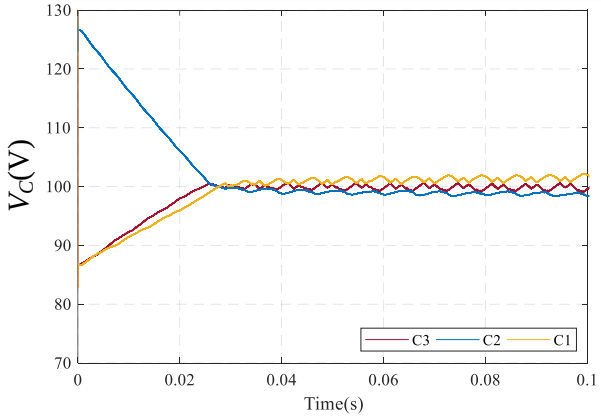
dc-link capacitor C1=C2=C3=2000μF, fundamental frequency f_o=50 Hz, switching frequency f_s=10 kHz, load R=25Ω L=5 mH each phase (makes output PF equals to 1), modulation index m_i=0.55. Fig.5.12 (a) presents the Phase-A line voltage and phase voltage, which are five levels (due to the low voltage modulation index) and three levels, respectively. Fig.5.12 (b) presents three-phase output currents. Fig.5.12 (c) shows three dc-link capacitors voltages. It can be monitored that the proposed NP voltage balancing control strategy can effectively pull back the voltages on each dc-link capacitor. And all three capacitors can be eventually well regulated at 1/3 of the total dc-link voltage. Fig.5.12 (d) upper figure presents the selected zero-sequence signal according to the algorithm in Fig.5.11, and Fig.5.12 (d) lower figure presents the phase-A final modulation signal with the injection of the selected zero-sequence signal.



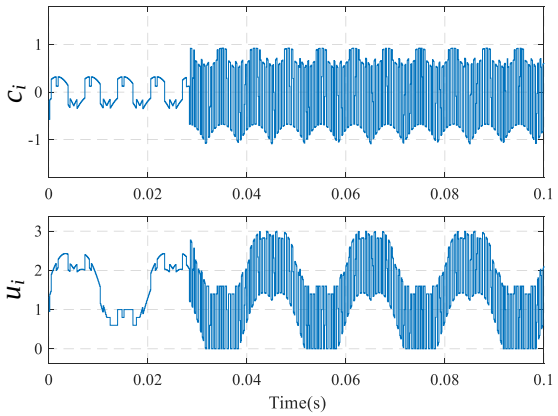
(a) Phase and line voltage



(b) Three-phase output currents



(c) Three dc-link capacitors voltages

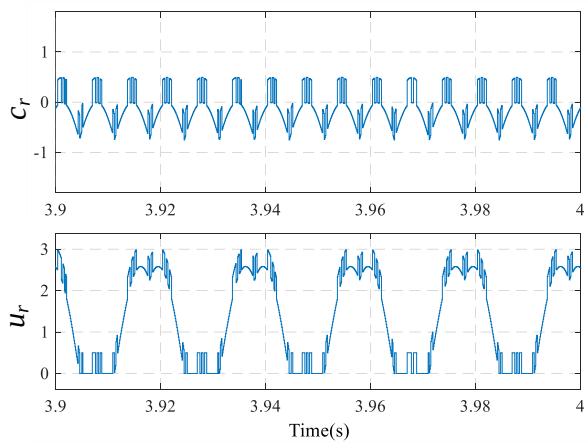


(d) Injected zero-sequence and modulation signals

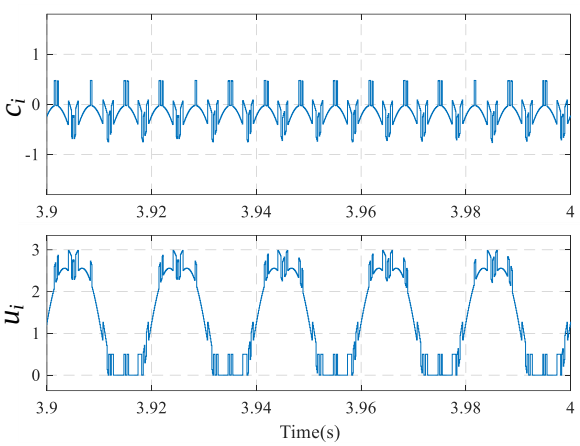
Figure 5.12 Simulation results of three-phase single-end four-level π-type inverter, mi=0.55

Fig.5.13 presents simulation waveforms of three-phase back-to-back four-level π-type converter with

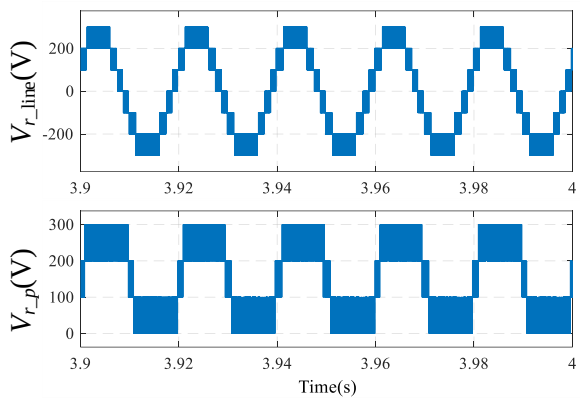
the same modulation indices on both sides under unity power factors condition (the simulation model is shown in Appendix D II). Test parameters are set as: total dc-link input V_{dc}=300V, dc-link capacitor C1=C2=C3=2000μF, fundamental frequency f_o=50 Hz on both sides, switching frequency f_s=10 kHz on both sides, grid side peak-to-peak voltage 287V, rectifier choke R_G=0.2Ω L_G=2 mH each phase, rectifier modulation index m_r=1.1, load R_L=25Ω L_L=5 mH each phase, inverter modulation index m_i=1.1. Fig.5.13 (a) upper figure presents the selected zero-sequence signal of the rectifier side according to the algorithm in Fig.5.11. Fig.5.13 (a) lower figure presents the rectifier side phase-A final modulation signal with the injection of the selected zero-sequence signal. Fig.5.13 (b) then similarly presents the selected zero-sequence signal as well as the final modulation signal of the inverter side. It can be monitored that both sides have the similar patterns on zero-sequence as well as final modulation signals due to the identical modulation indices. Fig.5.13 (c) presents the rectifier Phase-A line and phase voltage, which are seven levels and four levels, respectively. Fig.5.13 (d) shows rectifier three-phase currents. Fig.5.13 (e) presents inverter Phase-A line and phase voltage, which are seven levels and four levels, respectively. Fig.5.13 (f) shows inverter three-phase sinusoidal currents. Fig.5.13 (g) shows three dc-link capacitors voltages which have been well regulated at 1/3 of the total dc-link voltage.



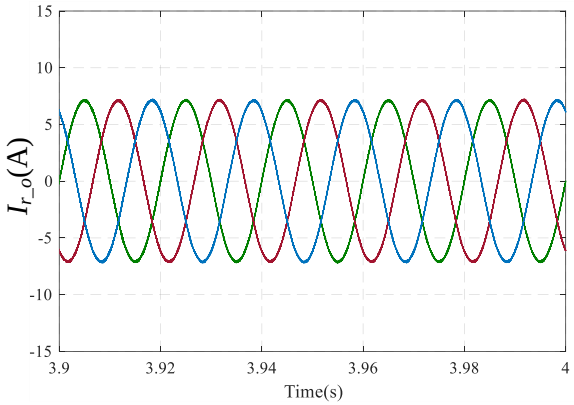
(a) Rectifier modulation and zero-sequence signals



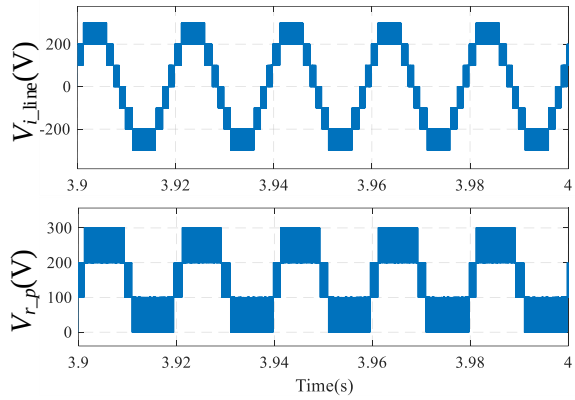
(b) Inverter modulation and zero-sequence signals



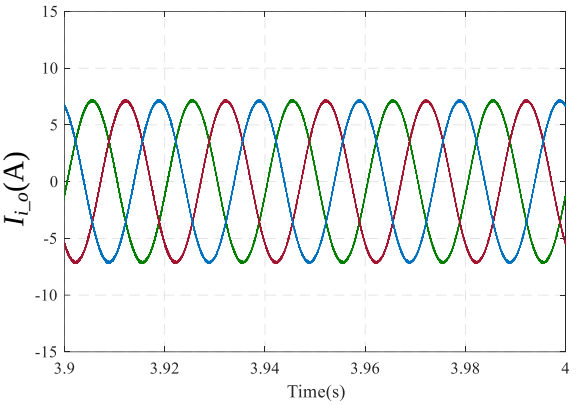
(c) Rectifier phase and line voltage



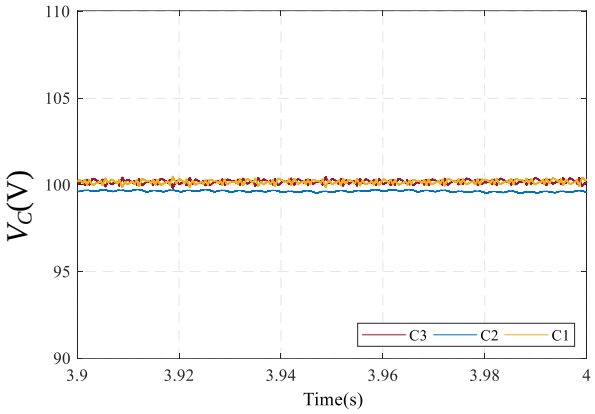
(d) Rectifier hree-phase output currents



(e) Inverter phase and line voltage



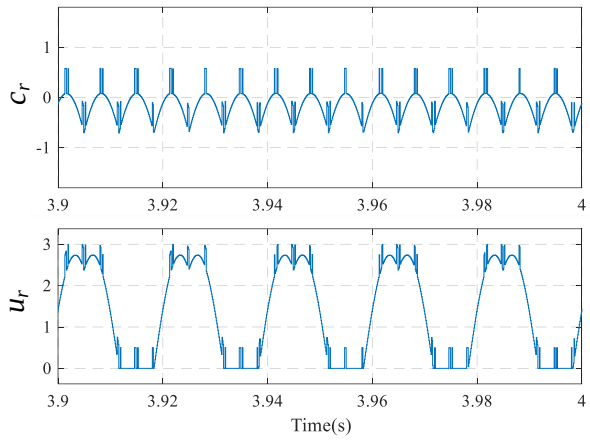
(f) Inverter three-phase output currents



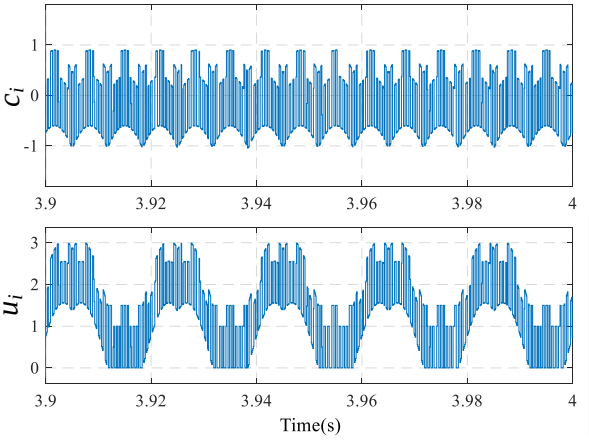
(g) Three dc-link capacitors voltages

Figure 5.13 Simulation results of three-phase back-to-back four-level π-type inverter, mr= mi =1.1

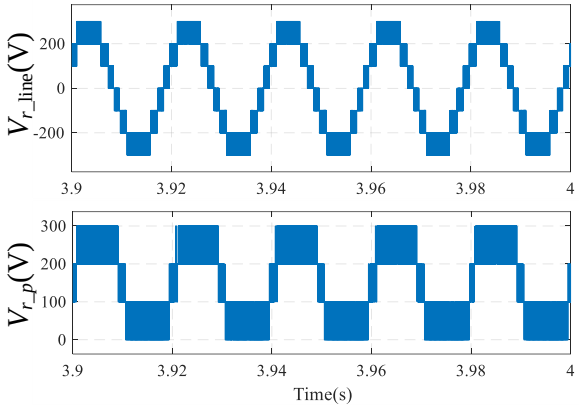
Fig.5.14 presents the simulation waveforms of three-phase back-to-back four-level π-type converter with the different modulation indices on both sides under unity power factors condition (the simulation model is shown in Appendix D II). Test parameters are set as: total dc-link input V_{dc}=300V, dc-link capacitor C1=C2=C3=2000μF, fundamental frequency f_o=50 Hz on both sides, switching frequency f_s=10 kHz on both sides, grid side peak-to-peak voltage 287V, rectifier choke R_G=0.2Ω L_G=2 mH each phase, rectifier modulation index m_r=1.1, load R_L=25Ω L_L=5 mH each phase, inverter modulation index m_i=0.65. Fig.5.14 (a) (b) present the selected zero-sequence and final modulation signals for the rectifier side and the inverter side, respectively. It can be monitored at this condition, the patterns of zero-sequence and final modulation signals for both sides are different. There are more selectable values for inverter side zero-sequence components (C_i) due to the lower modulation index m_i=0.65. In contract, the selectable points for rectifier side zero-sequence components (C_r) are relatively less due to the relative higher modulation index m_r=1.1. Fig.5.14 (c) presents the rectifier Phase-A line and phase voltage, which are seven levels and four levels, respectively. Fig.5.14 (d) shows rectifier three-phase currents. Fig.5.14 (e) presents inverter Phase-A line and phase voltage, which are five levels (due to low modulation index on the inverter side) and four levels, respectively. Fig.5.14 (f) shows inverter three-phase sinusoidal currents. Fig.5.14 (g) shows three dc-link capacitors voltages which have been well regulated at 1/3 of the total dc-link voltage.



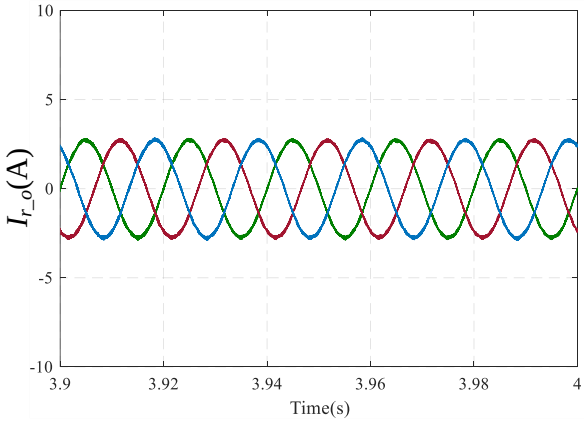
(a) Rectifier modulation and zero-sequence signals



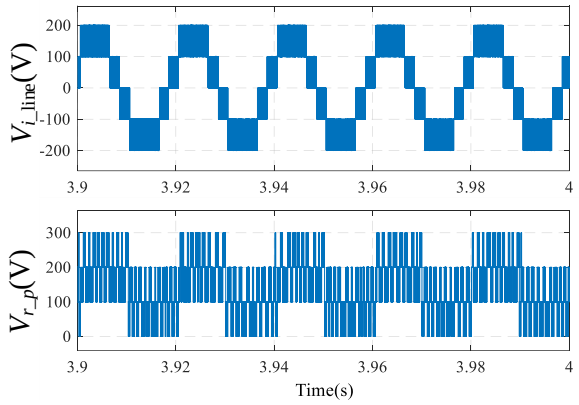
(b) Inverter modulation and zero-sequence signals



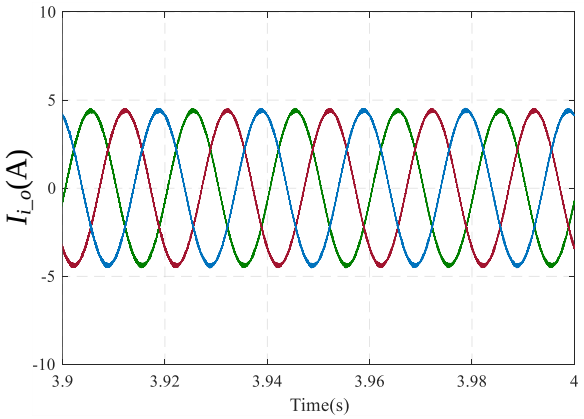
(c) Rectifier phase and line voltage



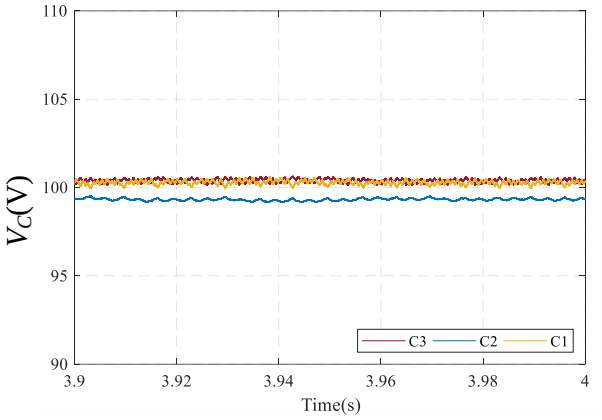
(d) Rectifier hree-phase output currents



(e) Inverter phase and line voltage



(f) Inverter three-phase output currents



(g) Three dc-link capacitors voltages

Figure 5.14 Simulation results of three-phase back-to-back four-level π-type inverter, mr=1.1, mi =0.65

Above simulations have provided the initial validation for the proposed dc-link NP voltages balancing control strategy for the four-level π-type converter. However, the practical control performance is affected accordingly by the practical DSP processing speed as well as the practical system tolerance [53]. Therefore, the actual validation as well as the controllable range based on the back-to-back four-level π-type converter prototype under the unity power factor condition will be provided in section 5.5.

5.5 Exprimental tests

In this section, experimental tests regarding the dc-link NP voltages balancing control for the proposed four-level π-type converter have been presented.

The established three-phase four-level π-type converter prototype presented in Chapter 4 will be used in Chapter 5 as well. As the closed loop control will be implemented on the converter, corresponding voltages as well as currents values have to be measured dynamically for the feedback purpose. Therefore, appropriate sensor boards will be required.

As mentioned above, the purpose of the sensor board is to dynamically measure the actual electrical variables such as dc-link capacitors voltages, load currents, grid voltages as feedback signals for the close-loop control system. Meanwhile, by measuring the real time electrical variables, overcurrent and overvoltage protection can be implemented.

The sensor board used in this thesis contains voltage transducers LEM LV25-P which are able to provide 40μs response time with maximum 500V measurement range. Current transducers LEM LA 55-P can

provide less than 1μs response time with maximum 50A measurement range. Both voltage transducers and current transducers provide rms ac 2.5kV galvanic isolation between the converter board and the control board where measurements signals are transferred which makes sure the reliability of the system. Meanwhile, both LEM LV25-P and LEM LA 55-P can share the +/-15V dc supply with the existing DSP/FPGA control board. The sensor board prototype presents as in Fig. 5.15. The control codes for DSP and FPGA are shown in Appendix F I.

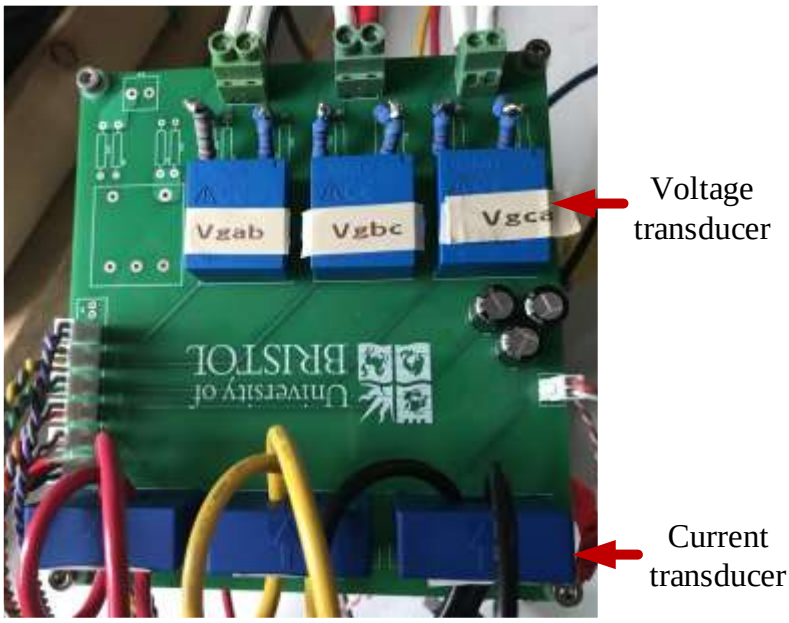


Figure 5.15 Sensor board prototype

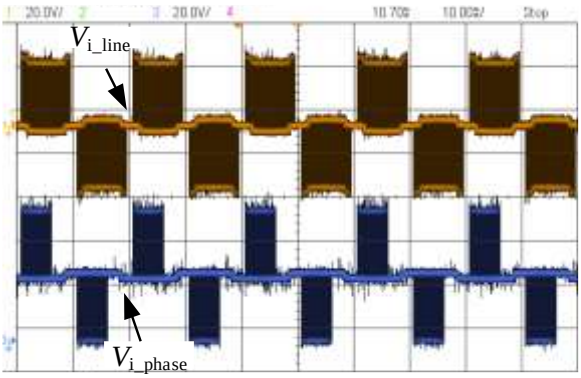
5.5.1 Single-end system test and investigation without the proposed control strategy

First, a trial operation for the single-end three-phase inverter system under the pure sinusoidal modulation open loop condition has been implemented. Operation parameters under a low modulation index are listed in Table V.II

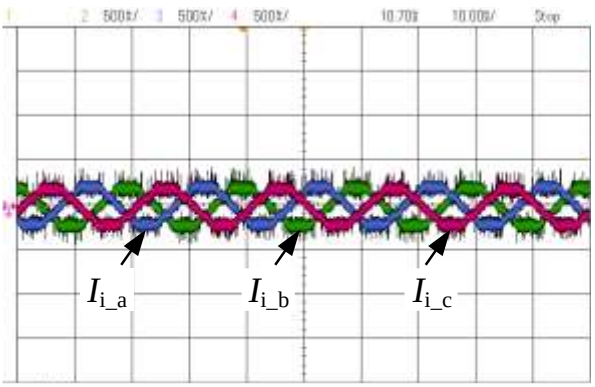
TABLE V.II. TEST PARAMETERS WITHOUT CONTROL APPLIED I

V_{dc}	60V
Load (each phase)	44Ω, 5mH
Switching frequency	10 kHz
Fundamental frequency	50 Hz
C1, C2, C3	2000μF
Modulation index	0.5
Dead-time	2μs

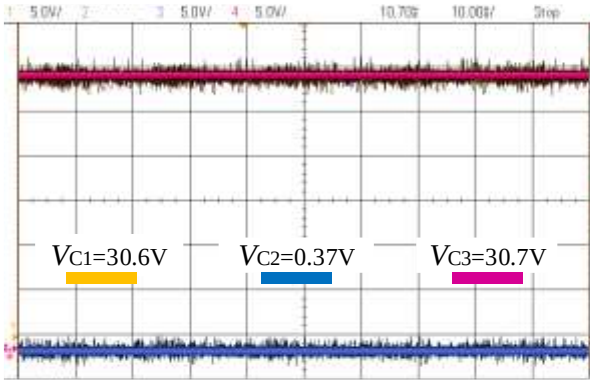
Fig.5.16 shows converter output waveforms when m=0.5. Fig.5.16 (c) shows three dc-link capacitors voltages. It is obvious that the middle capacitor C2 has been completely discharged, and the total dc-link voltage has been distributed on C1 and C3. Fig.5.16 (a) shows the output line voltage as well as the phase voltage. Due to the low modulation index, the open loop sinusoidal modulation operation makes the four IGBT T2, T3, T4, T5 in two neutral paths have more switching actions during each fundamental period. However, due to the dc-link central capacitor C2 is completely discharged, the two neutral paths can be deemed as clamping to the same NP. Therefore, there are no commutations between 2E and E in practice at all. That is the reason the phase voltage only has three levels and contains flat line in the middle. Fig. 5.16 (b) presents three-phase output currents which contain visible significant harmonics.



(a) Line and phase voltage



(b) Three-phase output currents



(c) Three dc-link capacitors voltages

Figure 5.16 Inverter open loop operation when m=0.5

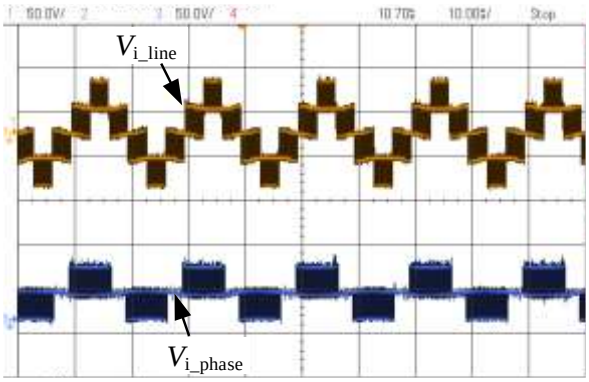
Operation parameters under a high modulation index are listed in Table V.III

TABLE V.III. TEST PARAMETERS WITHOUT CONTROL APPLIED II

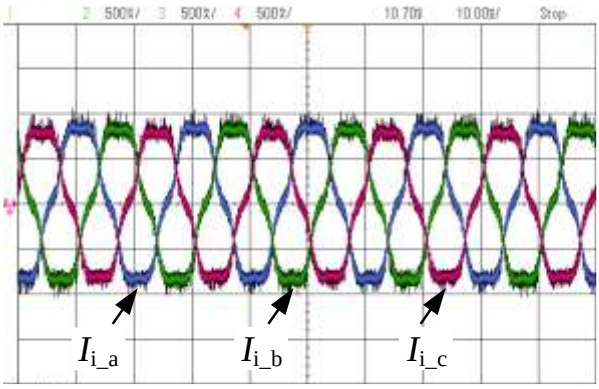
V_{dc}	60V
Load	44Ω, 5mH
Switching frequency	10 kHz
Fundamental frequency	50 Hz
C1, C2, C3	2000μF
Modulation index	0.85
Dead-time	2μs

Fig. 5.17 shows the output waveforms when m=0.85. Fig. 5.17 (a) shows the output line voltage as well as the phase voltage. It can be found out the phase voltage has three levels, while the line voltage has

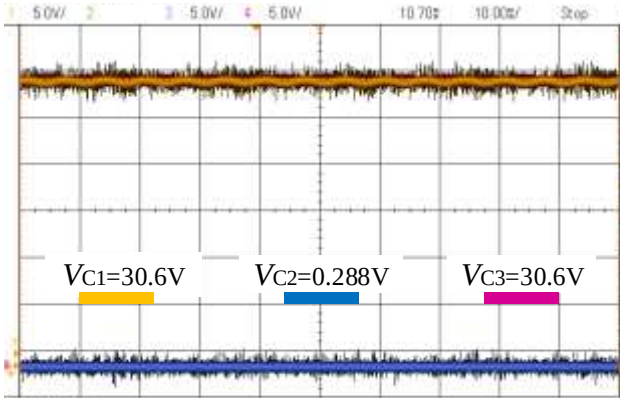
five levels even at the high modulation index. Fig. 5.17 (b) presents three-phase output currents. They are periodical but not sinusoidal, visible distortions have been monitored in current waveforms. Fig. 5.17 (c) presents three dc-link capacitors voltages. It is obvious that the middle capacitor C2 fully discharges. The whole 60V dc-link voltage has been almost equally distributed on the top capacitor C3 and the bottom capacitor C1.



(a) Line and phase voltage



(b) Three-phase output currents



(c) Three dc-link capacitors voltages

Figure 5.17 Inverter open loop operation when m=0.85

According to test waveforms in Fig. 5.16 and Fig. 5.17, it can be verified if there is no dc-link NP voltage balancing control applied on the single-end three-phase four-level π-type inverter system, the pure sinusoidal modulation open loop operation will cause the dc-link central capacitor C2 discharged completely with the time passes. Switching devices switching voltage increases, top and bottom dc-link capacitors withstanding voltage increases, significant harmonic contents occur at the output. All these reduce the system operation reliability as well as the output quality.

5.5.2 Single-end system test and investigation with the proposed control strategy

It has been experimentally verified in section 5.5.1, that if there is no active dc-link NP voltages balancing control applied, the central capacitor C2 will be finally discharged under the open loop operation, and cause three dc-link NP voltages unbalancing. Therefore, the proposed dc-link NP voltages balancing control has to be applied on the single-end three-phase inverter system. The system setup concept diagram is shown in Fig.5.18.

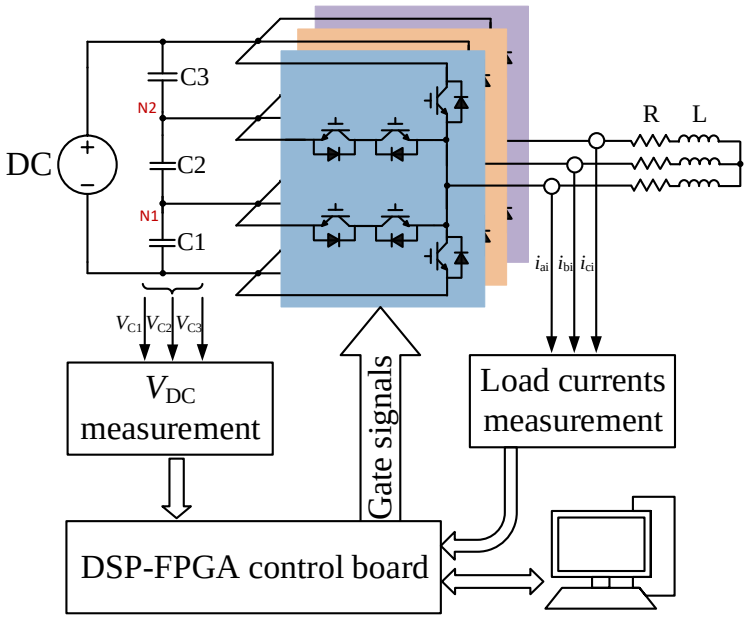


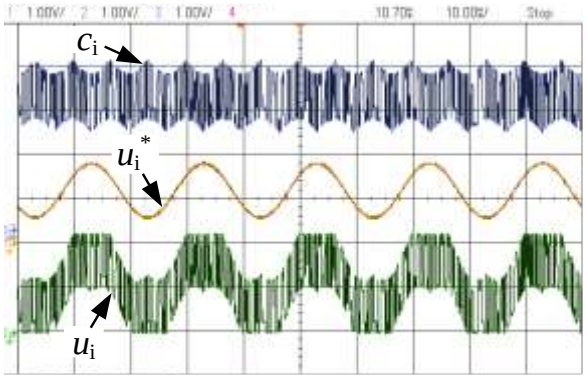
Figure 5.18 Concept diagram of the single-end three-phase inverter with proposed dc-link NP voltages balancing control strategy.

Table V.IV presents test parameters for the single-end three-phase four-level π-type inverter with the proposed dc-link NP voltages balancing control employed under m=0.6.

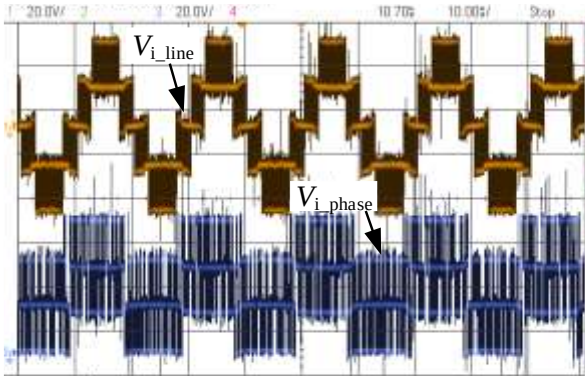
TABLE V.IV. TEST PARAMETERS OF WITH CONTROL APPLIED I

V_{dc}	60V
Load	44Ω, 5mH
Switching frequency	10 kHz
Fundamental frequency	50 Hz
C1, C2, C3	2000μF
Modulation index	0.6
Dead-time	2μs

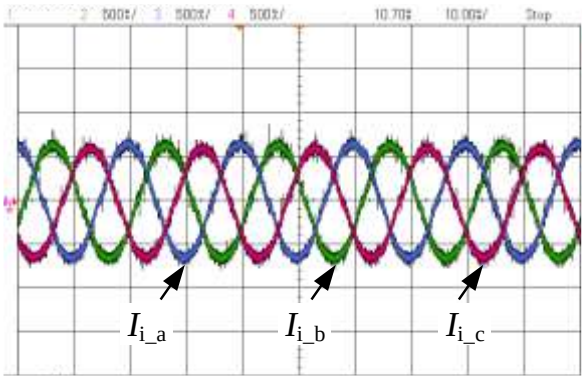
Fig.5.19 presents operation waveforms of three-phase four-level π-type inverter system with dc-link capacitors voltages balancing control applied. The AD5725 DAC chips can be employed to monitor the internal variables in the code through the oscilloscope. The phase A modulation waveform as well as the injected zero-sequence signal waveform are shown in Fig. 5.19 (a). The yellow waveform represents the phase A sinusoidal fundamental component. The blue waveform is the selected the zero-sequence component through the method introduced in section 5.3, whose fundamental frequency is triple the one of sinusoidal fundamental components. The green waveform is the phase A final modulation signal by adding sinusoidal fundamental waveforms and zero-sequence components together. Fig. 5.19 (b) bottom waveform presents phase voltage which has four levels. And due to the relative low modulation index, the output line voltage only has five levels as shown in Fig. 5.19 (b) top waveform. Fig. 5.19 (c) presents inverter three-phase currents which are sinusoidal. Fig. 5.19 (d) shows three dc-link capacitors voltages which are all balanced at 1/3 (20V) of the total dc-link voltage (60V). Fig. 5.19 (e) presents the dc-link three capacitors voltages clearer by setting different offset values on voltage probes.



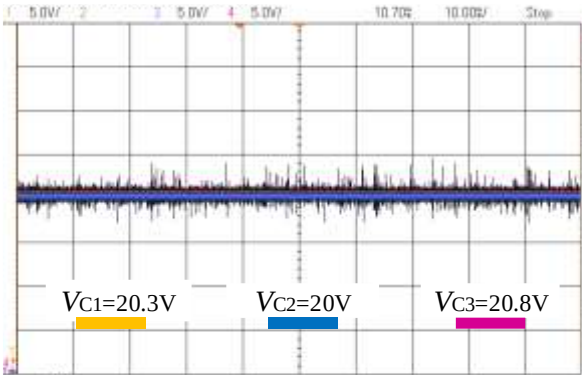
(a) Modulation and zero-sequence signals



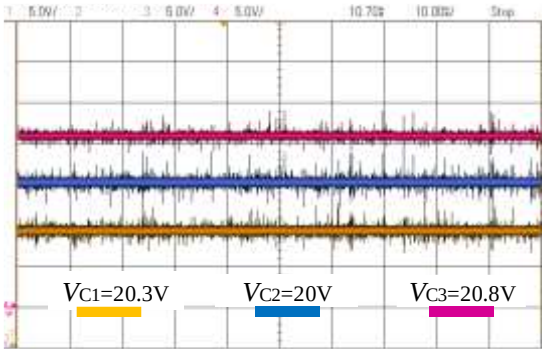
(b) Output phase and line voltages



(c) ac side three-phase output currents



(d) dc-link capacitors' voltages



(e) dc-link capacitors' voltages (channel offset values are different)

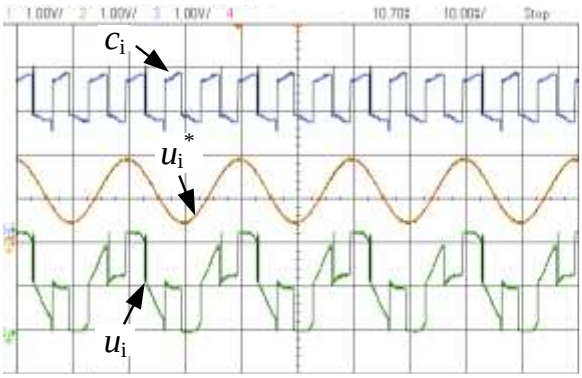
Figure 5.19 Single-end inverter operation with proposed control strategy m=0.6

Table V.V presents operation parameters based on 0.65 modulation index for the single-end three-phase four-level π-type inverter system with proposed dc-link NP voltages balancing control employed.

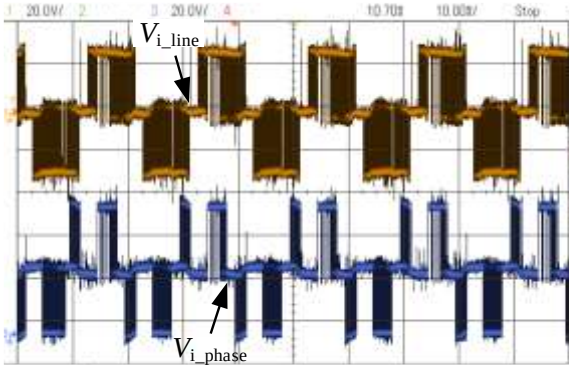
TABLE V.V. TEST PARAMETERS OF WITH CONTROL APPLIED II

V_{dc}	60V
Load	44Ω, 5mH
Switching frequency	10 kHz
Fundamental frequency	50 Hz
C1, C2, C3	2000μF
Modulation index	0.65
Dead-time	2μs

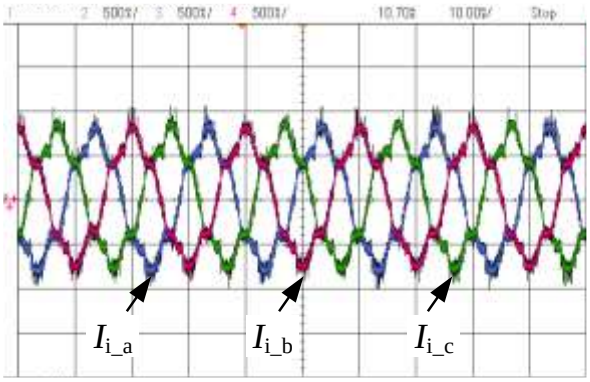
Fig.5.20 presents operation waveforms of three-phase four-level π-type inverter system with dc-link capacitors voltages balancing control applied, but with m=0.65. In Fig.5.20 (a), the yellow waveform represents the phase A sinusoidal fundamental component. The blue waveform is the selected the zero-sequence component. The green waveform is the phase A final modulation signal by adding previous two waveforms together. It can be monitored that the zero sequence signal varies less frequently than the m=0.6 condition as shown in Fig.18 (a), which means the available zero sequence to ensure the NP voltage balancing task is limited or does not exist. In Fig. 5.20 (b), both the phase voltage and the line voltage have only three levels and visible distortion appears on them due to the control algorithm failed to balance the dc-link NP voltages. The inverter worked inappropriately. Fig. 5.20 (c) shows three-phase currents, visible distortion occurs on current waveforms. Fig. 5.20 (d) shows three dc-link capacitors voltages, obviously the center capacitor C2 completely discharged. Triple fundamental frequency ripple occurs on the upper capacitor voltage as well as the lower capacitor voltage. In this case, the proposed dc-link NP voltages balancing control failed to keep the three dc-link capacitors voltages balanced.



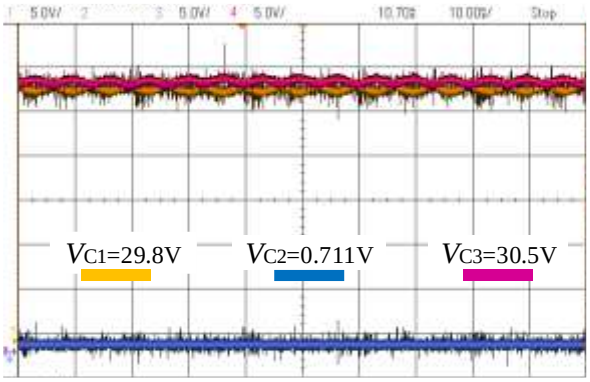
(a) Modulation and zero-sequence signals



(b) Output phase and line voltages



(c) ac side three-phase output currents



(d) dc-link capacitors' voltages

Figure 5.20 Single-end inverter operation with proposed control strategy m=0.65

Test waveforms in Fig.5.19 and Fig. 5.20 verified that the proposed dc-link NP voltages balancing control method has its limit to fulfil the task when a single-end converter is operating under a unity power factor condition. This limit is the decided by the modulation index, m=0.6 is approximately the upper limit under this condition.

5.5.3 Back-to-back configuration test

As the mentioned in Section 4.3 and test results in Section 5.5.2, due to the limitation of proposed control strategy, the single-end configuration is not able to balance the dc-link NP voltages at a high modulation index under the unity power factor condition. Therefore, the back-to-back configuration has been established and tested. The test setup concept is presented in Fig. 5.21. The rectifier and the inverter connect with each other through the dc-link, they share the same dc-link capacitors C1, C2, C3. Two dc-link NPs N1 and N2 are common between these two converters. The inverter ac-side connects

to the three-phase RL load. The rectifier ac-side connects to the grid, which transfers power to the dc-link, and also provides dc-link neutral path currents in order to help the dc-link NP voltages balancing. Both converters are controlled by the XC3S400 FPGA with TMS320F28335 DSP control board as used before.

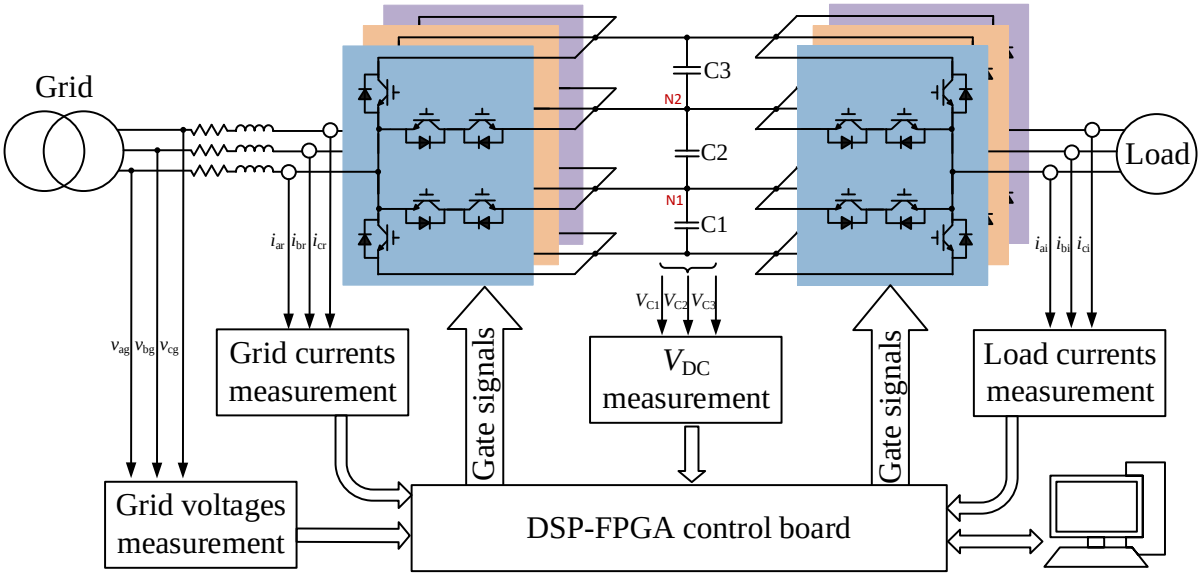


Figure 5.21 Concept diagram of the back-to-back three-phase four-level π-type converter with proposed dc-link NP voltages balancing control strategy.

Fig. 5.22 presents the back-to-back four-level π-type converter experimental prototype setup. The four-level π-type converter prototype PCB board has been designed to match the size of the existing DSP/FPGA control board in order to stack one by one for the space saving as shown in the figure. Meanwhile, as shown in Fig. 5.23, due to the front-end rectifier connects to the grid, the appropriate close loop current loop as well as the voltage loop are required to regulate the grid side current and maintain the whole dc-link voltage. Therefore, grid side three-phase voltages as well as rectifier three-phase currents have to be measured dynamically. Fig. 5.23 shows the sensor boards group for the rectifier and the inverter, respectively.

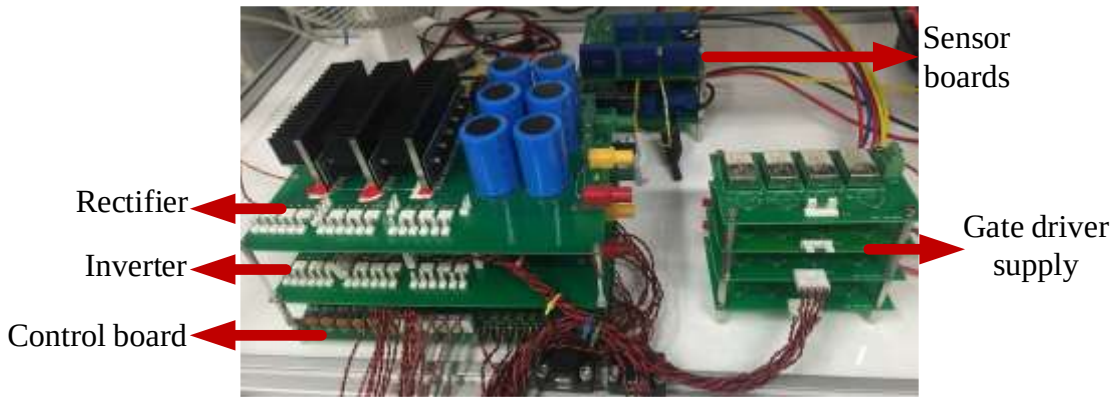


Figure 5.22 Experimental prototype of the back-to-back four-level π-type converter

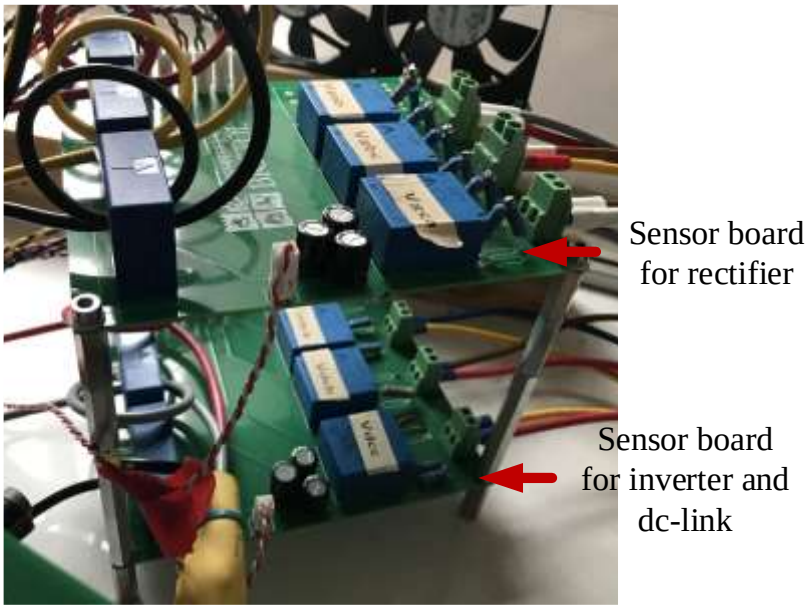


Figure 5.23 Sensor boards prototype

As this is a test prototype, for the purpose of the safe grid connection, three-phase isolation transformers as well as a three-phase variac have been connected between the grid and the rectifier as shown in Fig. 5.24. Meanwhile, the grid-connected variac can be used to modify the rectifier side modulation index for the test purpose. The inductance of the transformers as well as the variac can be used as the input choke of the rectifier (the maximum value of the sum of the inductance is about 5mH by measurement). A three-phase load (R=25Ω, L=6.32mH) is star-connected at the ac-side of the inverter side. This means the both sides have nearly unity power factors. The dc-link voltage is set to 300V. Each dc-link capacitor has the capacitance C=1000μF. Fundamental frequencies on both sides are both 50 Hz. And switching frequencies on both sides are both 10 kHz. As mentioned before, the rectifier ac-side is connected to the grid. Therefore Proportional-Integral (PI) control-based current loops are applied to the rectifier side

in order to manipulate grid-side rectifier ac currents. Meanwhile, a PI-based voltage control loop is also applied on the rectifier side in order to regulate the total dc-link voltage. No PI control is applied on the inverter side. The proposed dc-link NP voltages balancing control is used on both sides. Please note, only the unity power factors on both sides condition is considered and tested in this chapter in order to investigate the nearly pure active power transfer situation on the proposed four-level π-type converter system.

Figure 5.24 Grid-side isolation transformer as well as the variac

Due to the control algorithm is relatively complex, the control algorithm code execution is not instant and will cause the time delay. Meanwhile, the purposed control algorithm code should be able to meet the control target at the same time. In order to fulfill these two requirements, the number of the sampled zero-sequence components within each sampling period is set to six (the optimum value) based on the trial and error manually. And this has been mentioned in section 5.3. The detailed code execution principle in the DSP/FPGA board is introduced in Appendix F.III. Fig. 5.25 presents the signal delay concept within in the DSP/FPGA control board. Briefly speaking, the variable sampled at point n (let's say the n_{th} bottom of the carrier wave), after the AD conversion, the control algorithm calculation, the corresponding generated modulation wave as well as the PWN signals will be renewed at point n+1 (the $(n+1)_{th}$ bottom of the carrier wave) if the total DSP/FPGA code execution time is less than one sampling/switching period. Through the DAC chip, it can be monitored, the total DSP/FPGA code execution time for each sampling group is 44.5μs as shown in Fig. 5.26. Therefore, for a 10 kHz

sampling/switching period, a time delay of one sampling period/switching period can be guaranteed. This validated that the proposed control algorithm for the back-to-back system can be executed once during each sampling period, and the whole system AD samplings can be updated once during each sampling period for a 10 kHz sampling/switching period. It has been shown in Fig.5.26 (b) by zooming in the waveform in Fig.5.26 (a).

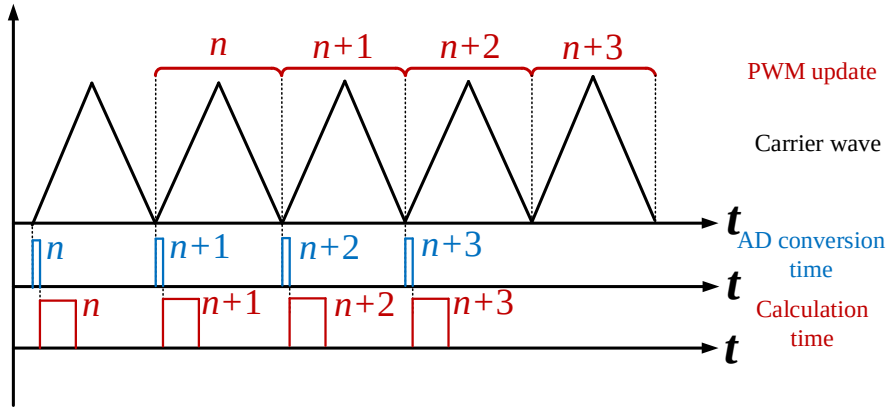
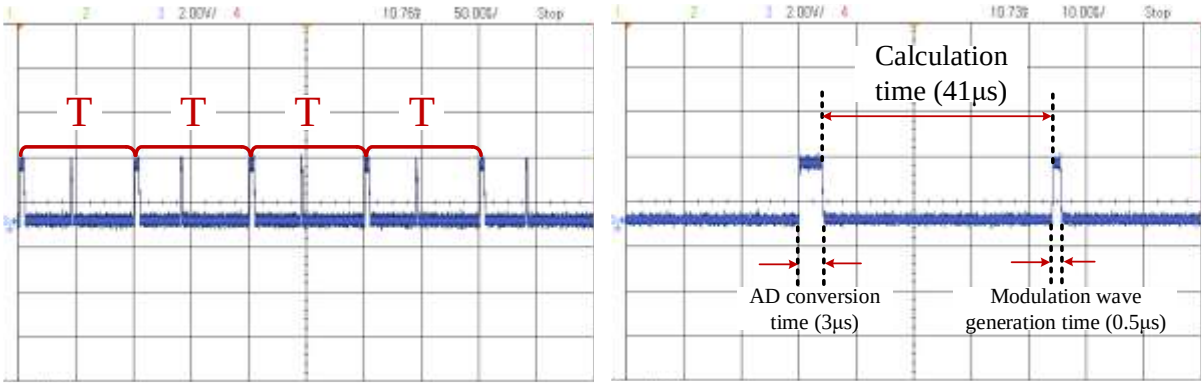


Figure 5.25 signal delay concept within in the DSP/FPGA control board



(a) Actual time of each sampling period (b) Zoomed-in actual code execution time

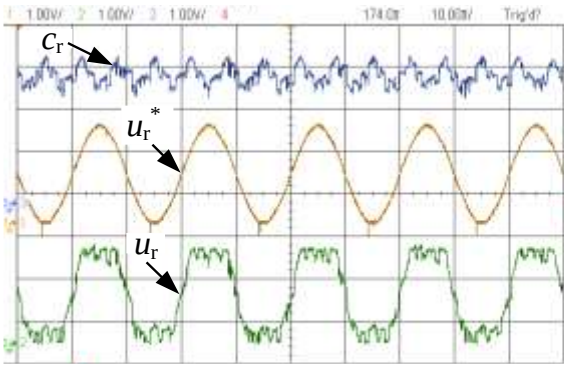
Figure 5.26 Monitored back-to-back system DSP/FPGA code execution time through DAC

Fig.5.27 presents converter operation waveforms with m_{rec}= m_{inv}=1.1. Modulation indices values employed here are larger than 1 is due to they are defined as the peak value of sinusoidal fundamental components divided by the peak value of the carrier waveforms. Thus, m=1 stands for the maximum modulation index that a standard sinusoidal modulation can achieve. And m=1.15 stands for the maximum modulation index that zero-sequence components injected modulation method can achieve ideally. The setting m_{rec}= m_{inv}=1.1 used here is nearly close to but slightly lower than the maximum modulation index 1.15, in order to leave some margin pretending the saturation out of the deviation of

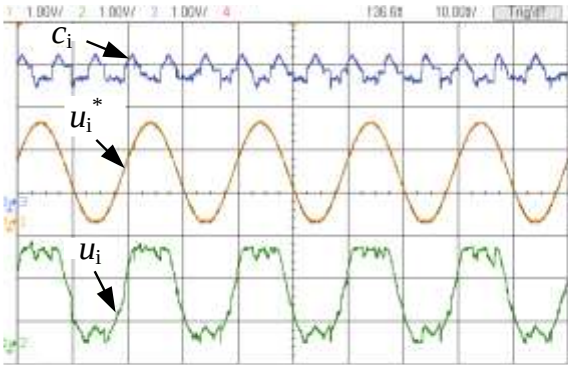
the sensor. As shown in Fig. 5.27 (a) (b). Yellow waveforms mean phase A sinusoidal fundamental components (u_r^*) and (u_i^*) on the rectifier and the inverter, respectively. Blue waveforms are the selected zero-sequence components (C_r) and (C_i), and their fundamental frequencies are triple the ones of (u_r^*) and (u_i^*). Green waveforms are phase A final modulation waves by combining yellow waveforms and blue waveforms.

Fig. 5.27 (c) shows phase voltage and the line voltage on the rectifier ac-side. With a 1.1 modulation index, four levels occur on the phase voltage, while seven levels occur on the line voltage. Inverter ac-side voltage waveforms in Fig. 5.27 (d) have the same characteristics. Fig. 5.27 (e) (f) show the rectifier and inverter ac-side currents.

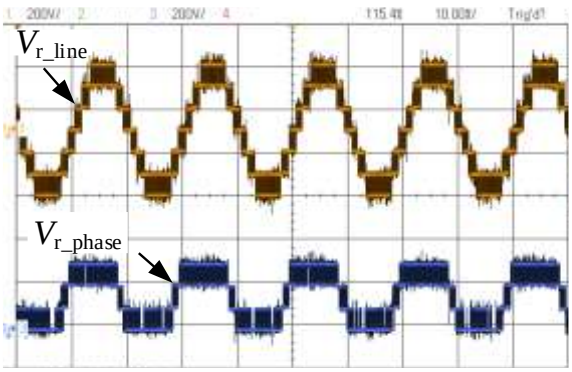
Fig. 5.27 (g) presents three dc-link capacitors' voltages. They are well regulated by the proposed control method employed as expected. Fig. 5.27 (h) presents three dc-link capacitors voltages with different offsets.



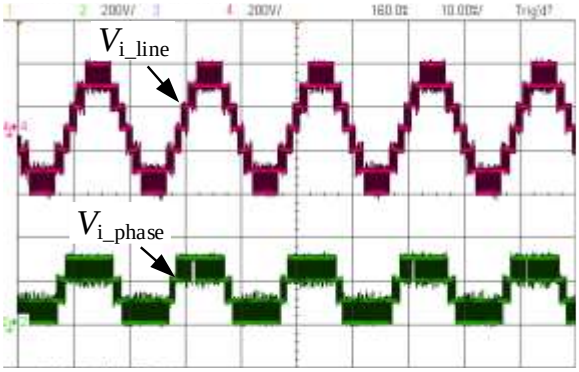
(a) Rectifier modulation and zero-sequence signals



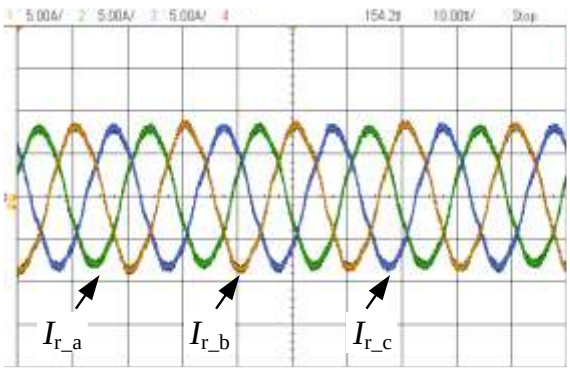
(b) Inverter modulation and zero-sequence signals



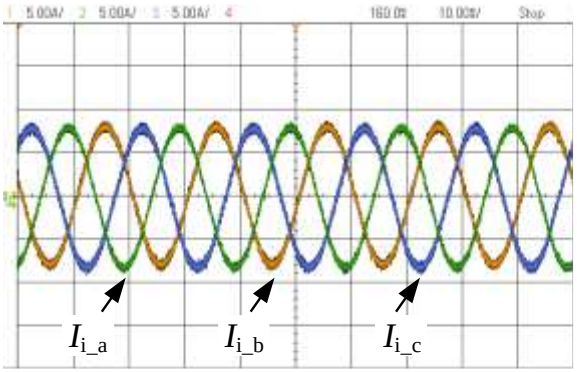
(c) Rectifier output phase and line voltages



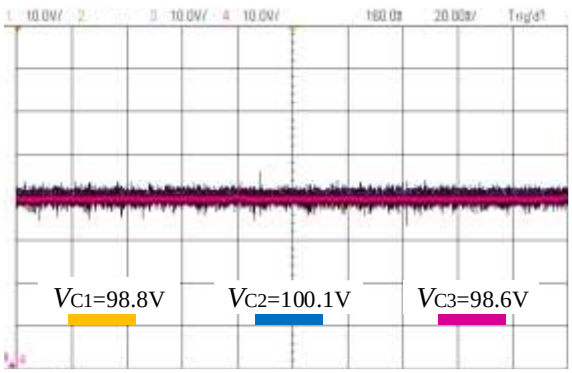
(d) Inverter output phase and line voltages

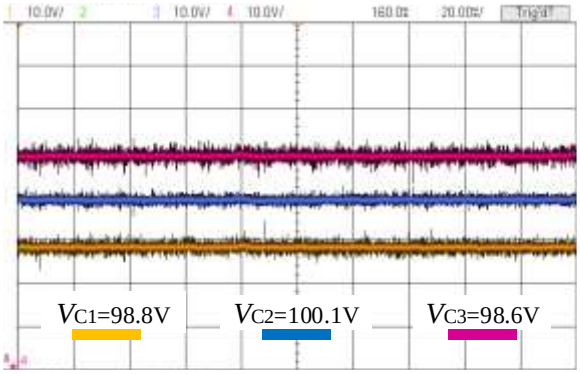


(e) Rectifier AC side three-phase currents



(f) Inverter AC side three-phase currents

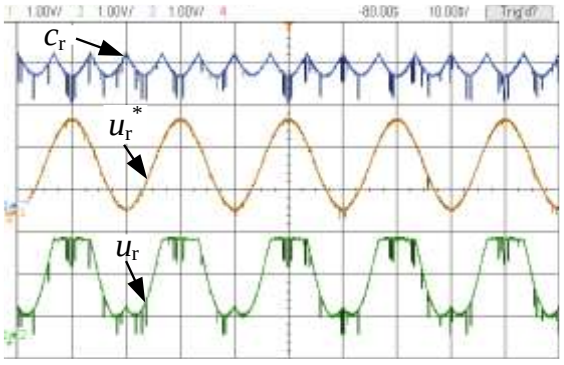




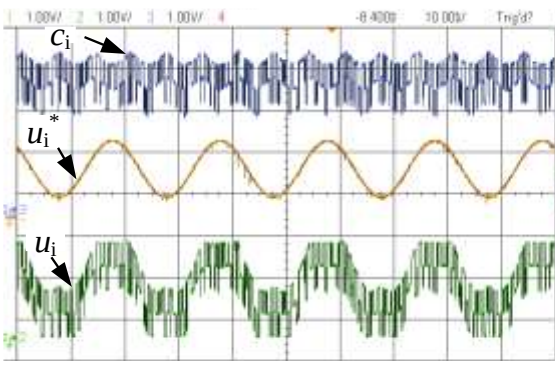
(g) Three DC-link capacitors voltages (h) Three DC-link capacitors voltages with different probe offsets

Figure 5.27 Test waveforms when mrec=minv=1.1

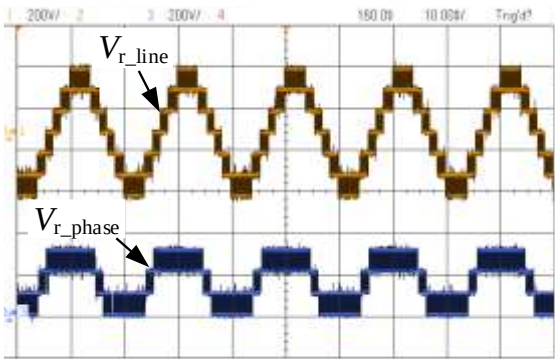
The toughest situation for the equal modulation index on both sides has been tested. Then the condition of different modulation indices on each side has been tested. Set the rectifier side m_{rec}=0.9 by adjusting the grid-side variac, meanwhile, set the the inverter m_{inv}=0.6 in the code. Modulation waveforms as well as injected zero-sequence components on both sides are shown in Fig. 5.28 (a) (b), as previous tests did. It can be monitored that there are more selectable points for inverter side zero-sequence components (C_i) due to the lower modulation index m_i=0.6. In contract, the selectable points for rectifier side zero-sequence components (C_r) are relatively less due to the relative higher modulation index m_r=0.9. Therefore, seven levels occur on the rectifier side line voltage as shown in Fig. 5.28 (c). While five levels occur on the inverter side line voltage as shown in Fig. 5.28 (d) due to the reduced modulation index. Meanwhile, as the inverter side modulation index is low, it can be considered as a load shedding condition. Thus, the total power transferred is reduced. Consider the equal power transfer between both the rectifier and the inverter, and the higher rectifier voltage, rectifier currents are lower than inverter currents in this situation as shown in Fig. 5.28 (e) (f). Fig. 5.28 (g) shows three dc-link capacitors' voltages. They are all well regulated at 1/3 of the total dc-link voltage. 5.28 (h) presents these three dc-link capacitors voltages with different offsets.



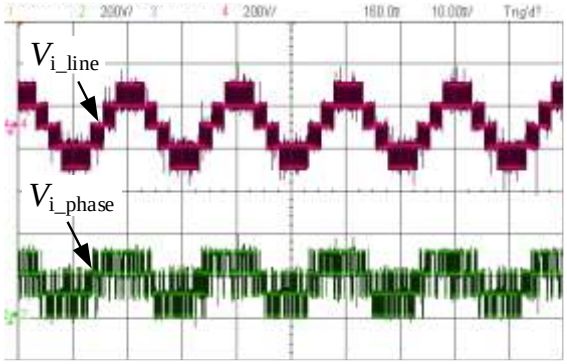
(a) Rectifier modulation and zero-sequence signals



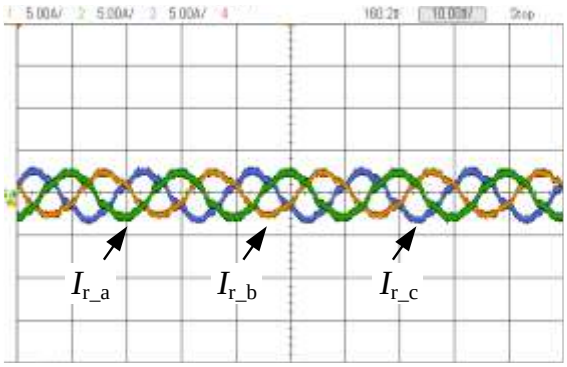
(b) Inverter modulation and zero-sequence signals



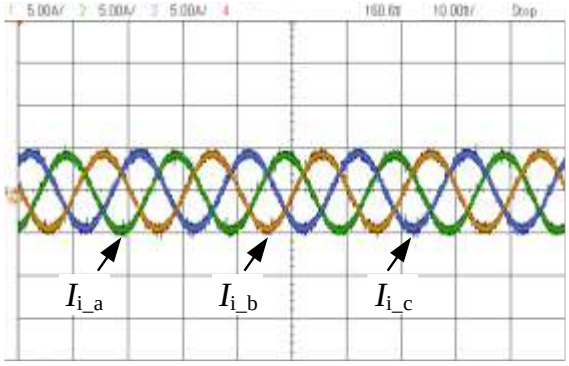
(c) Rectifier output phase and line voltages



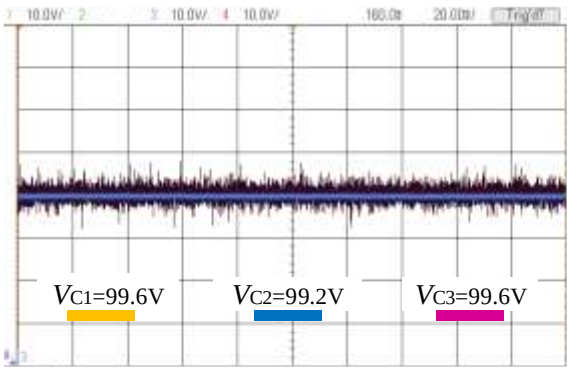
(d) Inverter output phase and line voltages

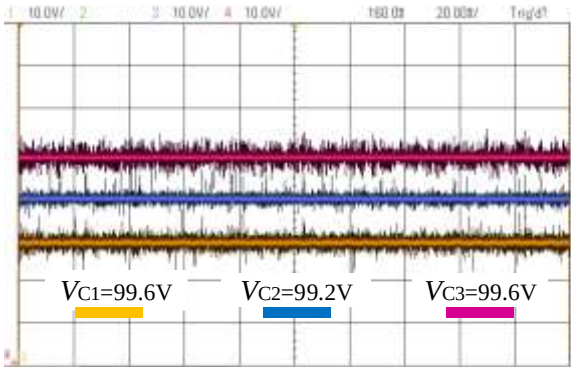


(e) Rectifier AC side three-phase currents



(f) Inverter AC side three-phase currents

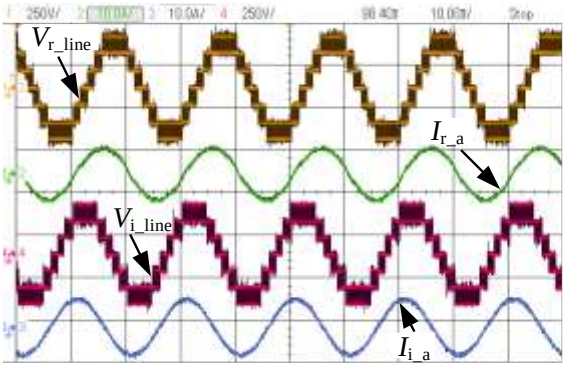


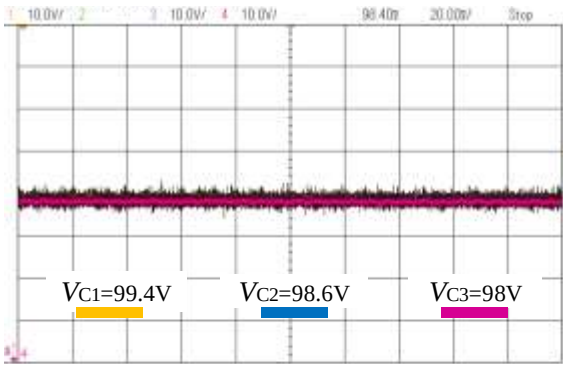


(g) Three DC-link capacitors voltages (h) Three DC-link capacitors voltages with different probe offsets

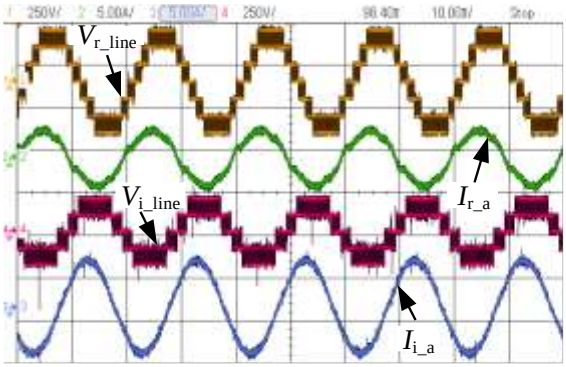
Figure 5.28 Test waveforms when mrec=0.9, minv=0.6

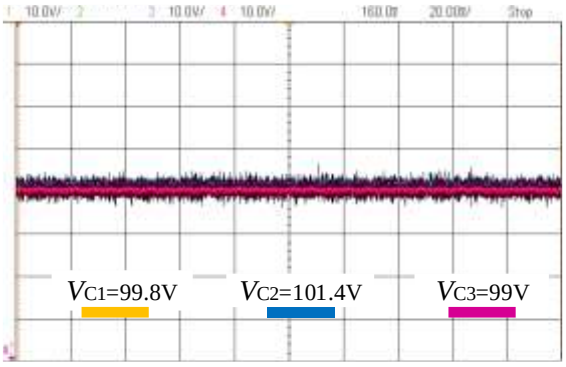
More scenarios when different modulation indices on both sides have been tested as shown in Fig.5.29. It provides results in order to experimentally verify the stable operation region for the back-to-back four-level π-type configuration with all dc-link capacitors voltage balanced under unity power factors condition. Fig.5.29 (a) presents the condition of m_{rec}=1.05 and m_{inv}=1.07, where m_{inv} is slightly higher than m_{rec}, and dc-link capacitors voltages have been well controlled. Fig.5.29 (b) presents the case of m_{rec}=1.05 and m_{inv}=1.02, where m_{inv} is slightly lower than m_{rec}. DC-link NP voltages have still been well balanced. Fig.5.29 (c) presents the case of m_{rec}=1.05 and m_{inv}=0.7, where m_{rec} is clearly much higher than m_{inv}. Seven levels occur on the rectifier line voltage, while five levels occur on the inverter line voltage. DC-link capacitor voltages are balanced as well. Fig.5.29 (d) and (e) show another two cases where the converter can operate stable with dc-link NP voltages balanced can well achieved, which are m_{rec}=0.9, m_{inv}=0.8 and m_{rec}=0.95, m_{inv}=0.6. Fig.5.29 (f) presents the case of m_{rec}=1.1, m_{inv}=0.75. It can be monitored that the middle capacitor voltage is close to zero. DC-link capacitors voltage can not be well balanced under this condition. Fig.5.29 (g) shows another unbalanced dc-link capacitors voltages condition of m_{rec}=1.05, m_{inv}=0.95. It is noticed that the phase position of the ac components on both sides not locked with each other and can vary. The reason is the rectifier/grid side current phase angle (I_{r_a}) depends on the grid voltage angle (which can change from time to time) when the system starts (control activated), because the grid current is in phase with the grid voltage. The inverter side current angle (I_{i_a}) depends on when the inverter control is activated (outputs voltage) and the load power factor. Therefore, the phase angle difference is not a result of different modulation depth.



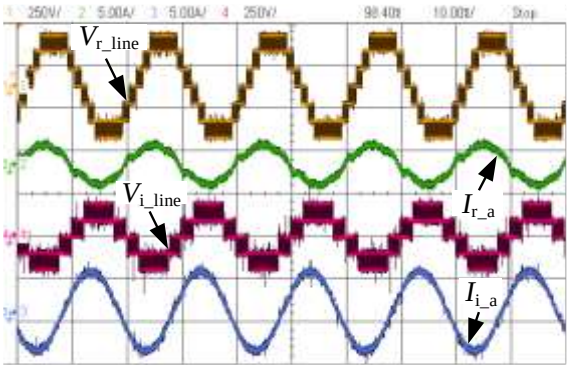


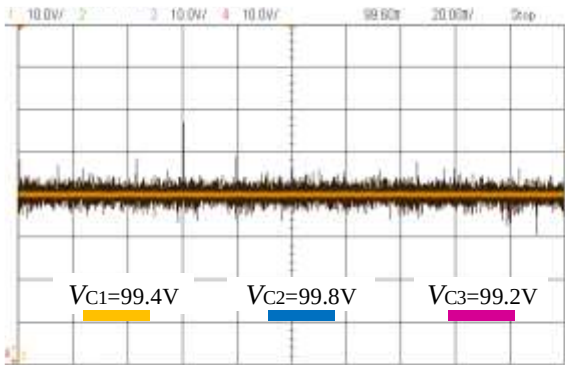
(a) m_{rec}=1.05, m_{inv}=1.07



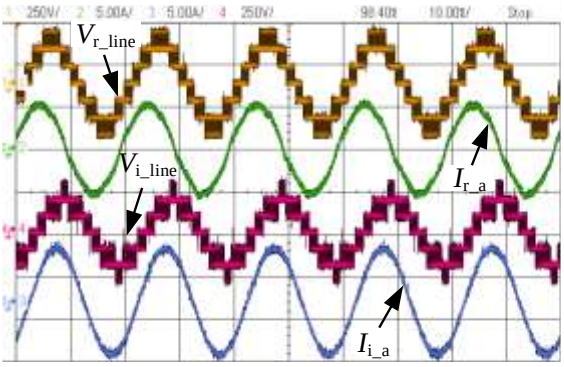


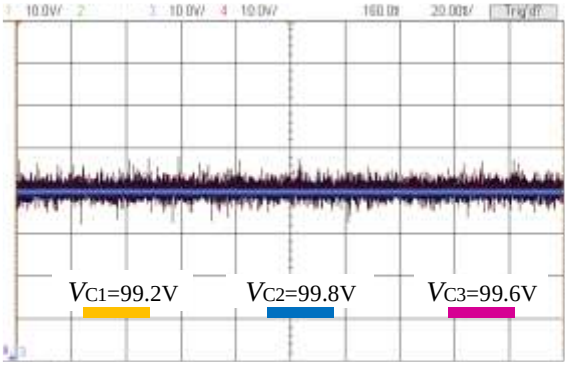
(b) m_{rec}=1.05, m_{inv}=1.02



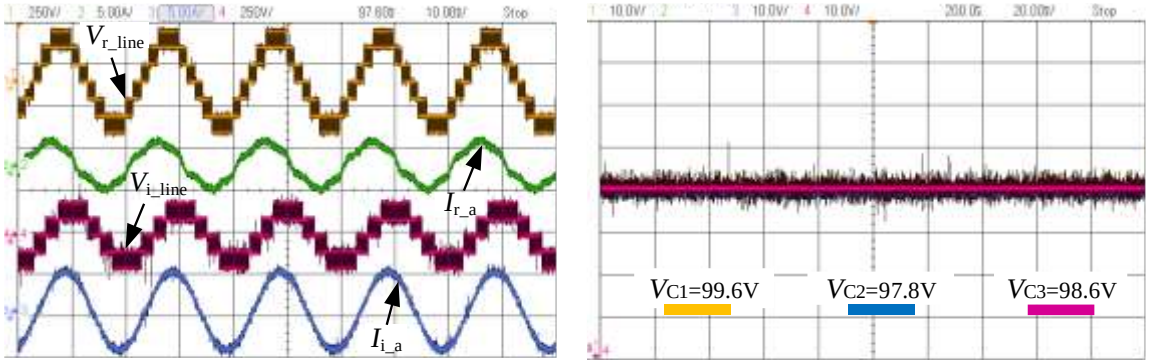


(c) m_{rec}=1.05, m_{inv}=0.7

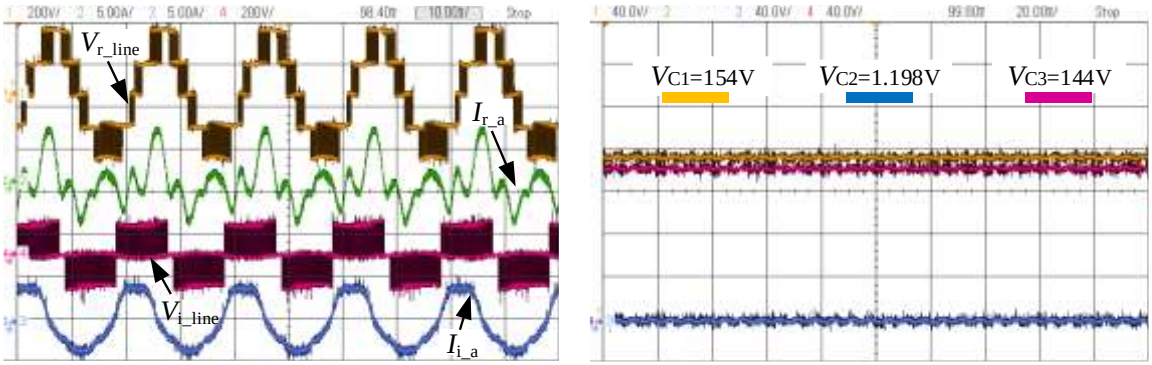




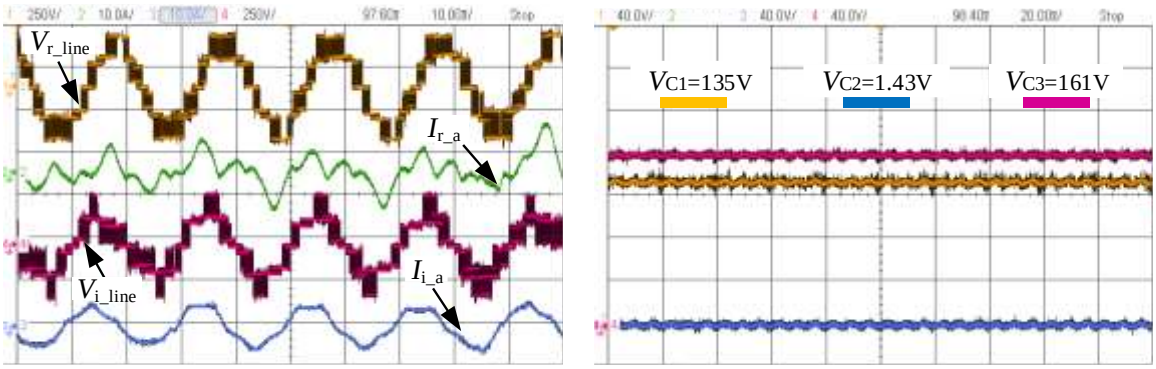
(d) m_{rec}=0.9, m_{inv}=0.8



(e) m_{rec}=0.95, m_{inv}=0.6



(f) m_{rec}=1.1, m_{inv}=0.75



(g) m_{rec}=1.05, m_{inv}=0.95

Figure 5.29 More experimental results of the different modulation indices on both sides

Through measurements of additional tests, Fig.5.30 summaries the controllable and un-controllable region of dc-link capacitors voltages balancing ability for the back-to-back four-level π-type converter under unity power factors conditions. Sample tests as shown in Fig.5.29 have also been spotted in Fig.5.30.

It can be found out, with unity power factors on both sides, dc-link NP voltages are more difficult to be

balanced with high modulation indices on both sides. According to Fig.5.30, if modulation indices on both sides are the same, the NP voltage balancing can always be achieved as similar to the equation (5.6) expressed. If modulation indices on both sides are different, and if the modulation index on either side is below 0.65, then no matter how large the value of the modulation index on the other side, the NP voltage balancing can be achieved. It is matched the test results in section 5.5.1 and section 5.5.2. If modulation indices on both sides are different and both larger than 0.65, the closer modulation indices at both sides, the more achievable dc-link NP voltage balancing. The above analysis gave the general explanation of the curve shape in Fig.5.30. The precise derivation of the actual shape of the unbalanced region in Fig.5.30 has not been derived here mathematically, and it could be investigated in the future.

Through the analysis in Section 5.2 and 5.3 and experimental results above, the main difference between the loading mode and grid connected mode can be summarized as below.

- From the fundamental frequency point of view, the grid-side converter is locked to the grid frequency of 50/60Hz while the load-side converter fundamental frequency will be determined by the load requirement, which can be variable, e.g. for variable-speed motor drive applications.
- From the power factor point of view, at the grid-side, the power factor is normally regulated to unity to reduce reactive power. In this case, it is more difficult to balance dc-link NP voltages as described in Section 5.2. At the load side, the power factor is not fixed, depending on the load.
- From the modulation index point of view, at the grid side, the modulation index is close to the maximum value if connects to the grid directly without the stepdown variac, as the grid voltage amplitude is fixed. It is also the most difficult condition to balance dc-link NP voltages. Therefore, the grid-side converter generally can not work independently to balance the NP voltages due to both high modulation index and high-power factor, unless a back-to-back configuration is used. The modulation index of the load-side converter can be variable depending on the load requirement.
- From the coordination between the rectifier and the inverter point of view, due to the symmetrical configuration of the back-to-back system, both the rectifier and the inverter will contribute to the dc-link NP voltages balancing. References [42][53] have concluded for a symmetrical back-to-back multilevel converter, if the power factor as well as the modulation index on both sides are equal, the system can operate at any operation points. For the pure active power transmission (both sides unity

power factors), the dc-link capacitor voltage balancing ability under variable modulation indices on both sides have been concluded in Fig.5.30.

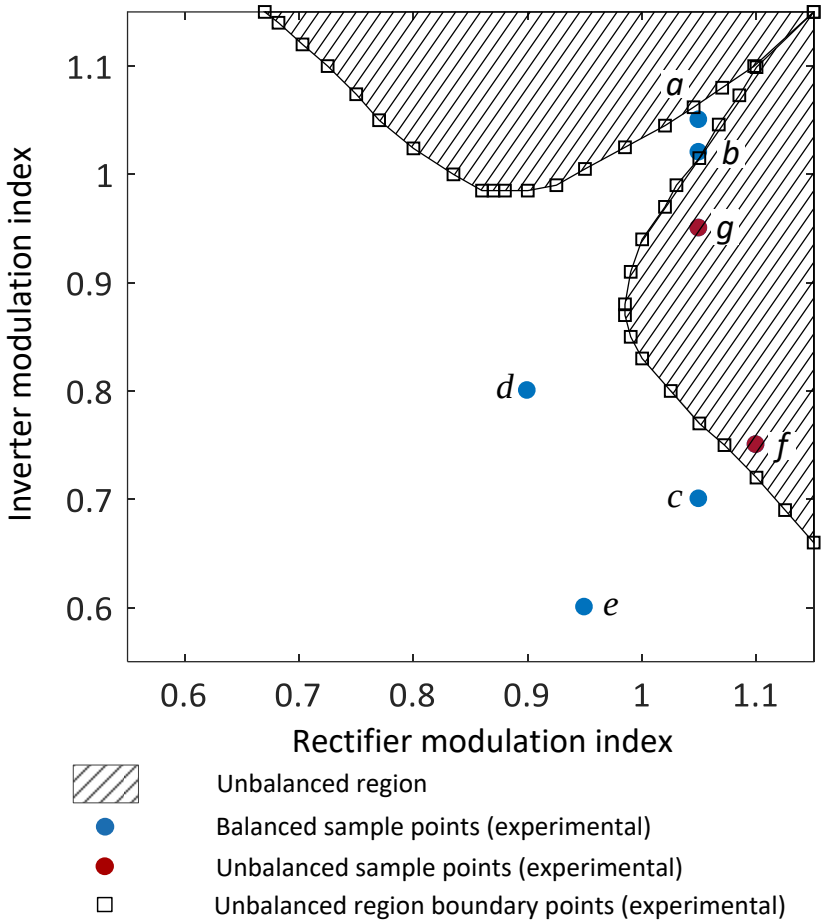


Figure 5.30 Controllable and uncontrollable region for dc-link capacitors voltage balancing based on experimental measurements under unity power factor operation on both sides

5.6 Summary of Chapter 5

According to the analysis in chapter 3, there are two NPs in the dc-link of the four-level π-type converter. Meanwhile, two neutral paths connect these two NPs to the phase-leg output terminal in order to output four voltage level. Therefore, as analyzed in section 5.2, when active power transfer occurs, and if there is no appropriate closed loop dc-link capacitors voltages control, the inner capacitors of the dc-link will be eventually fully discharged with the operation goes. It makes the converter become a three-level

converter. This will lose advantages of the four-level π-type converter and reduce the reliability of the system. In order to keep dc-link NP voltages balanced and do not increase the number of switching actions during each switching period, the appropriate control scheme has to be implemented on the four-level π-type converter in this chapter.

In this chapter, the dc-link NP voltages balancing control solution for the four-level π-type converter under the unity power factor condition (worst case) has been analyzed and proposed. The optimum zero-sequence injection based on the traditional level shifted CB-PWM based control strategy has been implemented on the three-phase four-level π-type converter to resolve the dc-link NP voltages balancing issue during the unity power factor operation. Advantages of the proposed control method are the less complex algorithm compares to the SVM based control, and less switching actions compared to the VV PWM based control. With the proposed control strategy, three dc-link capacitors voltages of the four-level π-type converter can be initially balanced. However, When the single-end converter (rectifier or inverter) is used, the dc-link NP voltages balancing can only be limited to modulation index 0.6. It is due to the fact that with the increase of the modulation index, available zero-sequence signals which can be used to force the average current variation on three dc-link capacitors are limited. It is verified according to the experimental results in section 5.5.2. If the modulation index needs to be extended without limitation, the symmetrical back-to-back configuration can be used due to neutral path currents caused from the rectifier side and the inverter side can be coordinated with each other. With the back-to-back configuration, the dc-link NP voltages can be balanced without the limitation of the modulation index when both sides have the same modulation indices according to the analysis in section 5.2. The practical back-to-back four-level π-type prototype with 300V dc-link voltage experiments verified the proposed dc-link NP voltages balancing control method can successfully balance three dc-link capacitors voltages at same modulation indices on both sides (m_{rec}=m_{inv}=1.1, close to the maximum modulation index which can be achieved) under the unity power factor condition in section 5.5.3. Meanwhile, the control method used in this chapter is based on dynamic modulation wave generation. Therefore, it is hard to calculate to the controllable region with different modulation indices on both sides under the unity power factor condition. Consequently, 300V dc-link voltage experiments based on different modulation indices on both sides have be implemented to summarize the region that dc-link NP voltages can not be guaranteed. Fig.5.30 demonstrated test results and proved that the dc-link

NP voltages balancing is more difficult to achieve with the increase of modulation indices. However, closer modulation indices on both sides help to balance dc-link capacitors voltages.

6 New hybrid-clamped four-level π-type converter

6.1 Introduction

Compares to the two-level and three-level converters, the four-level π-type converter presents advantages such as lower voltage stress on switching devices during commutations, lower switching losses under the same switching frequency, and lower ac harmonic components under the same filter setting. Even the dc-link NP voltages drift problem can be resolved by adopting an optimum zero-sequence components injection voltage balancing method, the converter operation is still limited by the modulation index as a single-end rectifier or inverter. One method to resolve this problem is to use two identical converters connected through dc-link as shown in Chapter 5. With the back-to-back configuration, the four-level π-type converter can operate with high modulation indices and high power factors on both sides.

However, some applications such as electrical car and electric aircraft drives require the single-end converter configuration such as dc-ac or ac-dc only conversion in a high modulation index as well. In order to enable the four-level π-type converter be employed independently as an inverter or rectifier without any modulation index limitation under the unity power factor condition, more redundant vectors or zero sequence components are required to be selected during the high voltage level (high modulation index) commutation such as 2E to 3E in order to adjust dc-link capacitors voltages. A hybrid-clamped four-level π-type converter proposed in [13] has the ability to resolve this issue by adding two additional switching devices as well as one additional FC in the phase-leg structure. However, there is no any appropriate analysis on this topology. Therefore, in this chapter, a comprehensive analysis about the hybrid clamped four-level π-type converter has been implemented. For hybrid NPC converters, there are some topologies have been investigated such as four-level hybrid NPC converter [139][140]. With the same output voltage level, compare to original FC converters, hybrid NPC converters require less number of FCs in the converter phase-leg which will not occupy the volume as much as the original FC converter does. Compares to normal NPC converters, hybrid NPC converters have the self dc-link NP voltages balancing ability due to the participation of the FC in commutations especially the commutations related to the NPs. Meanwhile, for hybrid clamped multilevel converter topologies, there

are several modulation and control methods for them. Selective harmonic elimination pulse-width modulation (SHE-PWM) has been used for the FC based five-level active NPC converter in [182][183]. The phase-shifted (PS) PWN with zero-sequence signals injection method has been used for a four-level hybrid-clamped converter in [180][184]. In this chapter, a control scheme based on the simple and effective logic flow chart with CB-PWM method is designed for the modulation and control of the hybrid-clamped four-level π-type converter. Due to this feature, the proposed method is very easy to implement. Simulations as well as experimental tests verified the hybrid-clamped four-level π-type converter is able to operate as a single-end converter such as inverter with all three dc-link capacitors voltage and FC voltage balanced without limitation on the modulation index under the unity power factor condition. At the same time, the optimum selection method for the FC has been analysed in this chapter in order to make a trade-off on the additional volume due to additional FCs in each phase-leg. Through the single phase-leg operation test, the FC ripple expression for the single phase-leg operation has been derived for the FC optimum selection.

6.2 Converter Controllability and Switching States

The phase-leg structure of the hybrid-clamped four-level π-type converter is shown in Fig.6.1. This topology is based on the original four-level π-type converter, but with two more switching devices as well as one more FC clamped between two neutral paths of the phase leg structure. This modification will enable the hybrid-clamped four-level π-type converter have plenty of redundant switching states, which make it possible to balance the dc-link NP voltages and FC voltages even at high modulation indices and unity power factor conditions as a single-end converter. Apart from that, all devices in the phase-leg do not have to block the whole dc-link voltage either during the steady state or the commutation period. Therefore, lower voltage rating devices with cheaper price can be adopted.

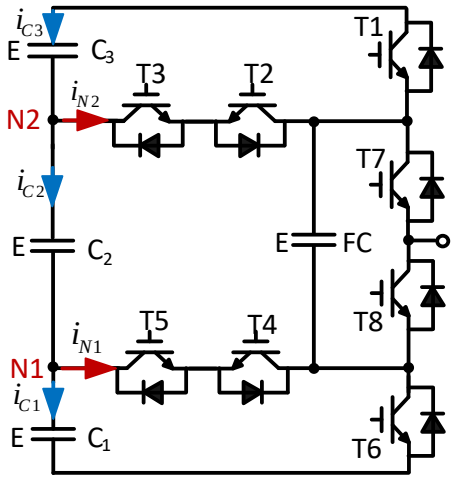


Figure 6.1 Phase-leg of the hybrid-clamped four-level π-type converter

TABLE VI.I COMPARISON OF FOUR-LEVEL CONVERTERS (SINGLE PHASE LEG)

Topology	NO. of the switching states	Single-end operation capability	NO. of switching devices per phase leg	NO. of FCs
Four-level π-type	4	No	6	No
Hybrid-clamped Four-level π-type	8	Yes	8	1
FC four-level converter	6	Yes	6	3
Four-level NPC converter	6	No	6 + 4 clamping diodes	No

Table VI.I compares the four-level π-type converter topology with the hybrid-clamped four-level π-type converter and two other topologies, i.e. FC four-level converters and Four-level NPC converters. As seen, there are in total 8 switching states in the hybrid-clamped four-level π-type converter, which doubles that in the four-level π-type converter. The increase in redundant switching states mainly increases options for the dc-link NP voltage adjustment, which enables the new topology to balance all the capacitors' voltages without the restriction of the modulation index (The detail will be explain in the following). However, the one additional FC in the hybrid-clamped converter phase-leg increases the total system volume to some extent, therefore, the size of FC can be selected with the optimized sized which will be discussed later.

In order to guarantee the uniform step levels at the output phase voltage of this converter topology, dc-link capacitors should ideally share one third of the whole dc-link voltage (E in Fig.6.1), and the FC voltage should be also regulated at one third of the total dc-link voltage. Fig.6.2 presents switching

states and corresponding output voltage levels of a converter phase-leg. There are eight switching states with four output voltage levels and the current can flow in both directions (in and out of the converter).

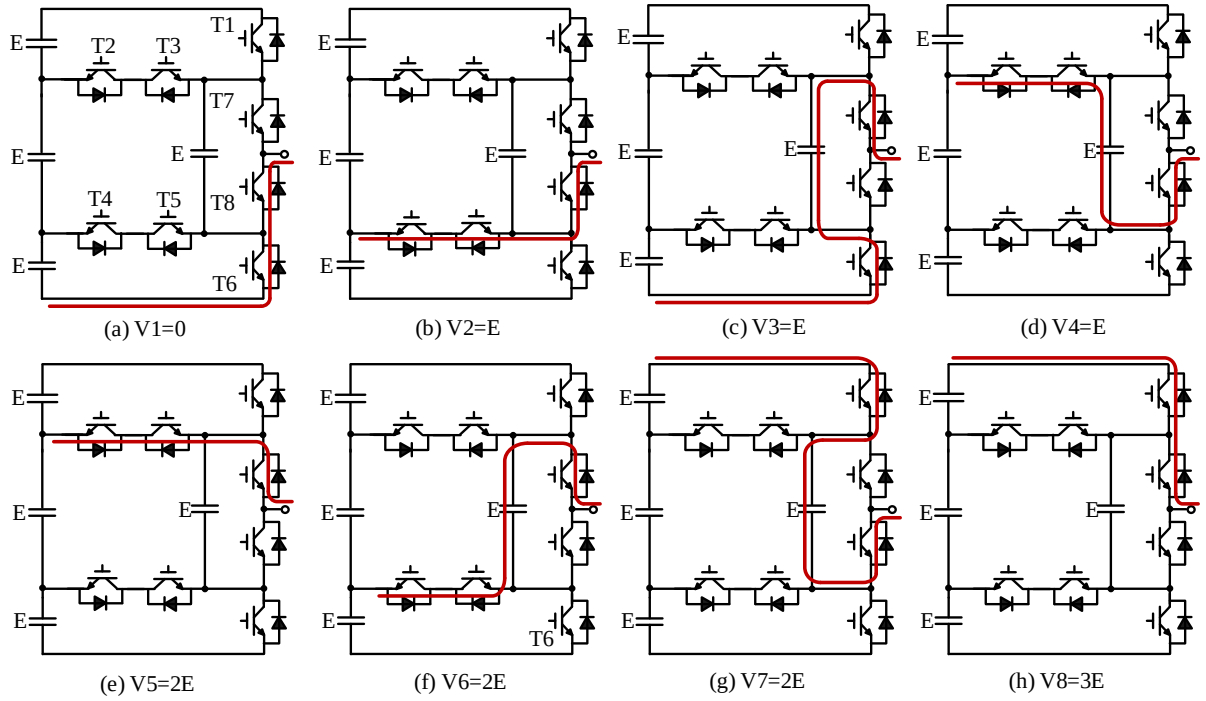


Figure 6.2 Switching states with corresponding output voltage levels

There are four output voltage levels as shown in Fig.6.3. Here, staircase voltages waveforms and sinusoidal current waveforms are used to simplify the analysis. To achieve the NP voltages balancing, the total amount of current flows N1 and N2 should be zero within one fundamental period. Under the zero power factor condition as shown in Fig.6.3 (a), the current flows through N1 and N2 can be zero within one fundamental period by only using the switching states V2, V5, when current commutates to N1 or N2. Under the unity power factor condition as shown in Fig.6.3 (b), only switching states V2, V5 are not enough to balance the charge flows through N1 and N2 because they make the neutral path current flow in a single direction. Switching states such as V4 and V6 (where currents flow via the FC) are required to balance the current flowing through N1 and N2. And V3 and V7 are also required to adjust the FC voltage, as V4 and V6 will affect the FC voltage. Therefore, similar to the analysis in Chapter 5, the unity power factor is the worst case scenario for NP voltages balancing and will be addressed in this chapter as well as in this thesis.

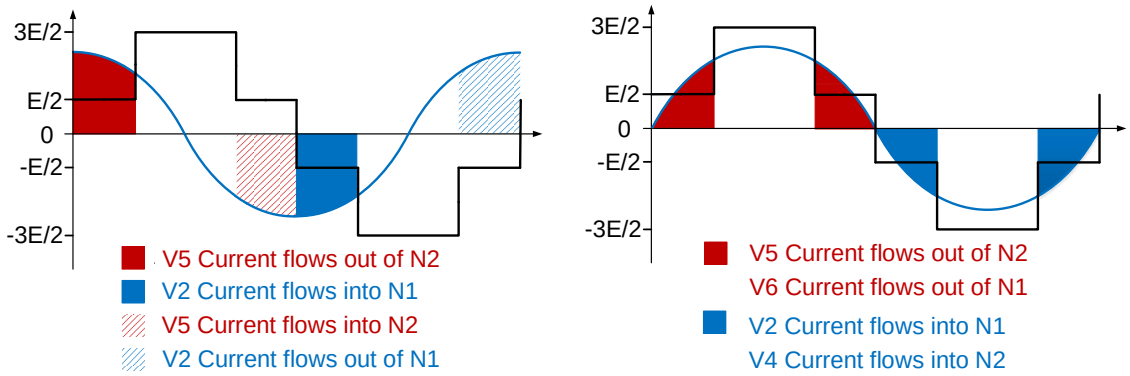


Figure 6.3 Neutral path currents flow conditions (a) power factor=0, (b) power factor=1

For voltage levels 0 and 3E, there is only one switching state corresponding to each of them respectively. For voltage level E and 2E (which involve NPs currents), there are three switching states available to be selected for each of them, which provides more redundant switching states when regulating NP voltages as well as the FC voltage. For example, when the current is flowing out of the inverter during the commutation between 2E and 3E. For 3E, only the switching state V8 can be selected, and it does not affect NP voltages or the FC voltage. For 2E, V5 will allow the current flowing out of N2, charging C3 while discharging C1 and C2; V6 will lead the current flowing out of N1, charging C3, C2 while discharging C1. Therefore, for the same output voltage 2E, appropriate switching states can be selected to let the current flow either through N2 or N1 in order to regulate the dc-link NP voltages for the desired purpose. Similarly, V6 will discharge the FC while V7 will charge the FC, which can be used to actively control the FC voltage under the same output voltage level. This enables this topology to have sufficient redundant switching states to regulate capacitors' voltages even at the high modulation index under the unity power factor condition.

Table VI.II shows the switching devices states corresponding to different switching states.

TABLE VI.II SWITCHING STATES OF THE NEW HYBRID-CLAMPED FOUR-LEVEL Π-TYPE CONVERTER

	T1	T2	T3	T4	T5	T6	T7	T8	Vo	i_{N1}	i_{N2}	i_{fc}
V1	0	0	0	0	0	1	0	1	0	0	0	0
V2	0	0	0	1	1	0	0	1	E	i_o	0	0
V3	0	0	0	0	0	1	1	0	E	0	0	i_o
V4	0	1	1	0	0	0	0	1	E	0	i_o	$-i_o$
V5	0	1	1	0	0	0	1	0	2E	0	i_o	0
V6	0	0	0	1	1	0	1	0	2E	i_o	0	i_o
V7	1	0	0	0	0	0	0	1	2E	0	0	$-i_o$
V8	1	0	0	0	0	0	1	0	3E	0	0	0

(a) $i_{load}>0$

	T1	T2	T3	T4	T5	T6	T7	T8	V_o	i_{N1}	i_{N2}	i_{fc}
V1	0	0	0	0	0	1	0	1	0	0	0	0
V2	0	0	0	1	1	0	0	1	E	i_o	0	0
V3	0	0	0	0	0	1	1	0	E	0	0	$-i_o$
V4	0	1	1	0	0	0	0	1	E	0	i_o	i_o
V5	0	1	1	0	0	0	1	0	2E	0	i_o	0
V6	0	0	0	1	1	0	1	0	2E	i_o	0	$-i_o$
V7	1	0	0	0	0	0	0	1	2E	0	0	i_o
V8	1	0	0	0	0	0	1	0	3E	0	0	0

(b) $i_{load}<0$

It can be found in Table VI.II, the switching group V1,V2; V1,V4; V3,V6; V4,V7; V5,V8; V6,V8, there are over two switching devices performing switching actions, which will increase the switching loss to some extent. This problem will be resolved in following sections.

6.3 DC-link NP voltages balancing control and FC voltage control strategy

The control strategy designed for the hybrid-clamped four-level π-type converter should aim to achieve dc-link NP voltages balancing, and regulate the FC voltage without affecting the output voltage quality at the same time. From the phase-leg structure of this topology in Fig.6.1, each phase-leg contains one

FC, which is independent to other phase-legs if multi-phase system adopted. Therefore, the FC voltage can be regulated by the single phase-leg independently [18]. While three dc-link capacitors are shared by all other phase-legs if multi-phase system employed. Therefore, dc-link NP voltages can be regulated by all phase-legs. Thus, the control of the FC voltage is of a higher priority and the control of dc-link NP voltages is given a relatively lower priority.

As there are sufficient available redundant switching states can be selected to regulate dc-link NP voltages as well as the FC voltage during the modulation. Therefore, for this topology, there are two methods that can be used for dc-link NP voltages and the FC voltage control. The first method is to select appropriate switching states in Fig.6.2 in each phase-leg for a given modulation waveform to regulate the FC voltage and dc-link NP voltages depending on the converter current flow directions as well as the corresponding output voltage levels [13][18][185]. This approach is straightforward and can be employed for each phase independently.

The second method is to select the optimum redundant vectors in SVM [28][38][151][186], or equivalently inject optimum zero-sequence components to fundamental reference waveforms in a CB-PWM [18][36][75]. Each effective redundant vector or zero-sequence component will have different effects on dc-link NP voltages and the FC voltage. Consequently, each redundant vector or zero-sequence component can be evaluated against the control objective, such as minimizes the energy on each dc-link capacitor or keeps the variation of the dc-link capacitor voltage as minimum as possible during each switching period. It should be noted that desired redundant vectors or zero-sequence signals are selected from multi-phase reference signals, thus this process is based on a multi-phase system. Ideally, these two methods should be used together in order to get an overall optimum control effect. However, consider the practical system computation effort as well as the characteristic of the hybrid-clamped four-level π-type converter topology, the first method will be used for the topology modulation and all capacitors' voltages control in this chapter.

a) FC voltage control

The FC voltage should be balanced within each sampling period (or switching period if equals to the sampling period).

Assume the sampling frequency equals to the switching frequency, the variation of the FC voltage

within one switching period can be expressed as

$$\Delta V_{fc}=\frac{1}{C_{fc}}\cdot i_o\cdot d_{fc}\cdot T_s \tag{6.1}$$

where C_{fc} is the capacitance value of the FC. i_o is the converter output current. T_s is the switching period. d_{fc} is the duty cycle which represents the duty cycle of the switching period where the current flowing through the FC. Therefore, d_{fc} can be controlled by adjusting the duty cycle of corresponding switching devices.

As seen in Fig. 6.3 above, only switching states V3, V4, V6, V7 can affect the FC voltage. Meanwhile, V4, V6 affect neutral path currents. In order to simplify the control algorithm, and ensure the system operation stability at the same time, a voltage error tolerance range for the FC voltage can be predefined, e.g. V_{tol}. Then, by comparing the actual FC voltage with the FC reference voltage (E, 1/3 of the total dc-link voltage), only if the difference between the reference voltage and actual FC voltage is beyond the tolerance V_{tol}, the FC voltage control will be activated. Consequently, specific switching states will be selected depending on output current flow directions as well as output phase voltage levels. Due to the coupling between the neutral path current and the FC current in V4 and V6, this predefined tolerance V_{tol} should not be too small. Otherwise, the FC voltage control is always activated due to the high priority. As a result, the neutral path current will be affected by V4, V6, and this may lead to dc-link NP voltages unbalancing. On the other hand, under the unity power factor condition, V_{tol} should not be set too large as well because V4 and V6 will always discharge the FC when regulating the neutral path current, thus the FC voltage will settle around E-V_{tol}. If V_{tol} is too large, the offset -V_{tol} will lead to large error in the FC voltage. Therefore, V_{tol}=1V is used in this chapter.

As mentioned before, the selection of desirable switching states also depends on output phase voltage levels, such as 0, E, 2E, 3E as shown in Fig.6.2. For the single phase-leg structure, a level shifted carrier-based sinusoidal modulation can be adopted as shown in Fig.6.4 (the sinusoidal modulation wave used here is to get the sinusoidal output current if the single phase-leg is employed). Where the corresponding modulation wave can be unified within the range of 0 to 3 similar to the modulation introduced in section 3.2 and section 5.3. Thus, the voltage level is defined as the integer part of the modulation signal while the fractional part defines the PWM duty cycle. Then, corresponding devices can switch on and off according to the interaction between the modulation signal and carrier signals. For example, if i_o>0

(Positive direction is defined as the current flows out of the inverter), the FC voltage is higher than the reference voltage and the modulation signal voltage level is 2, then switching states V6 and V8 will be selected to discharge the FC. The output voltage will switch between 2E and 3E. If the FC voltage error is within the predefined range, no active FC voltage control will be applied.

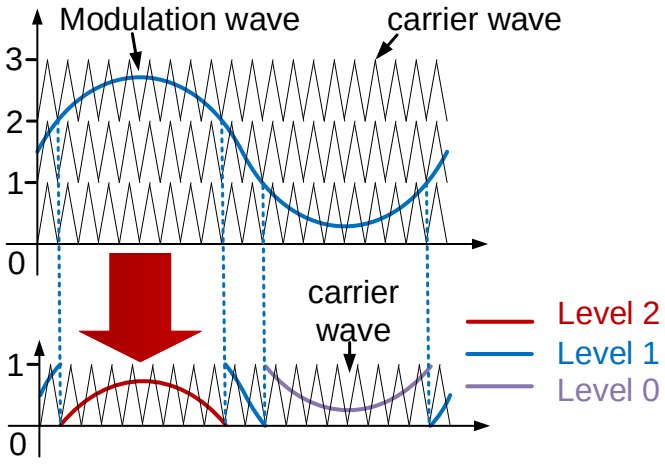


Figure 6.4 Level shifted carrier-based sinusoidal modulation scheme for the hybrid-clamped four-level π-type converter

b) DC-link NP voltages balancing control

As the FC voltage control for the hybrid-clamped four-level π-type converter is given the first priority. When the FC voltage is regulated within the pre-defined range, the dc-link NP voltages balancing control will be activated. The control cost function can be derived by keeping three dc-link capacitors' voltages as close to 1/3 of the total dc-link voltage as possible in each switching period as shown in (6.2) [139]

$$\min V = \sum_{i=1}^{3} \left| V_{dci} + \Delta V_{dci} - \frac{V_{dc}}{3} \right| \tag{6.2}$$

where, V_{dc} is the total dc-link voltage. V_{dc1}, V_{dc2}, V_{dc3} are dc-link three capacitors' voltages, respectively. ΔV_{dci} is the estimated capacitor voltage variation in the next switching period, and can be expressed as (6.3).

$$\Delta V_{dci} = \frac{i_{Ci} \cdot T_s \cdot d}{C} \tag{6.3}$$

where C_i is the capacitance value of each dc-link capacitor. i_{Ci} is the current flowing through each dc-link capacitor. T_s is the switching period. d is the duty cycle when the current flowing through NPs, and can be expressed as (6.4)

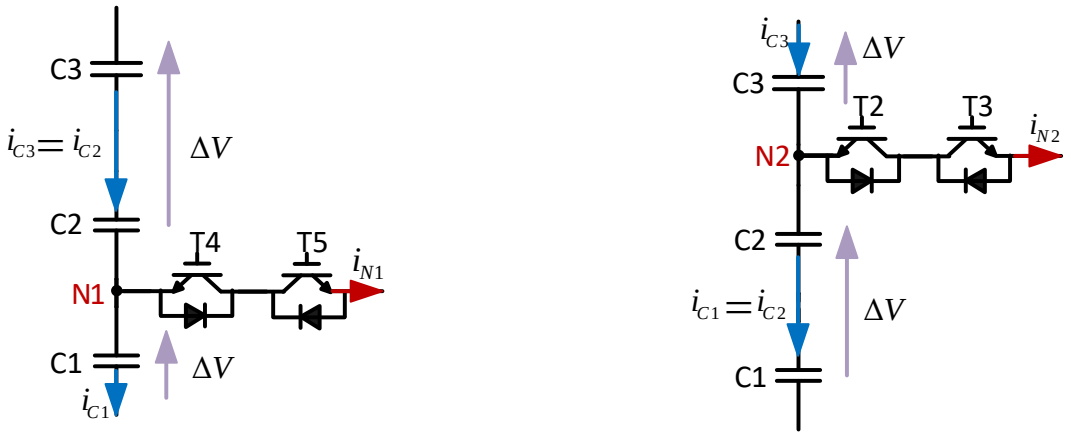
$$d = \begin{cases} frac(u_i) & int(u_i) = 0 \\ 1 & int(u_i) = 1 \\ 1 - frac(u_i) & int(u_i) = 2 \end{cases} \tag{6.4}$$

where, u_i is the modulation signal as shown in Fig.6.4. int(u_i) means the integer part (voltage level) of the modulation signal and frac(u_i) means the fractional part (duty cycle) of the modulation signal.

Desirable switching states will be picked in order to force the output current flowing through either N2 or N1 under the same voltage level in order to minimize the cost function in (6.2). Currents flowing through the neutral paths i_{N1} and i_{N2} can be expressed in (6.5)

$$\begin{cases} i_{N1} = k \cdot i_o \\ i_{N2} = (1-k) \cdot i_o \end{cases} \tag{6.5}$$

where, i_o is the output current. The value of k depends on switching states and determines which NP the current should flow through. If the current flows through N1, k=1, otherwise, k=0.



(a) Current flowing through N1 (b) Current flowing through N2

Figure 6.5 Relationship between dc-link capacitors currents and neutral path currents

According to Fig.6.5, the derivation of the relationship between the capacitor current i_{Cj} in (6.6) and i_{N1}, i_{N2} is the same as introduced in section 5.3 for the original four-level π-type converter. For the transient state in Fig.6.5 (a), the relationship between i_{N1} and i_{C1}, i_{C2} and i_{C3} can be expressed as (6.6a)

$$\begin{cases} i_{C1} = -\frac{2}{3} i_{N1} \\ i_{C2} = \frac{1}{3} i_{N1} \\ i_{C3} = \frac{1}{3} i_{N1} \end{cases} \tag{6.6a}$$

while for the transient state in Fig.6.5 (b), the relationship between i_{N2} and i_{C1}, i_{C2} and i_{C3} can be expressed as (6.6b)

$$\begin{cases} i_{C1} = -\frac{1}{3} i_{N2} \\ i_{C2} = -\frac{1}{3} i_{N2} \\ i_{C3} = \frac{2}{3} i_{N2} \end{cases} \tag{6.6b}$$

Corresponding switching states selection process in order to keep three dc-link capacitors voltage as close to one-third of the total dc-link voltage as possible during each switching period given in (6.2) can be implemented in a simple way according to (6.6). The effect on dc-link capacitors voltages variations from neutral path currents i_{N1} and i_{N2} can be calculated separately. Therefore, expression (6.2) can be divided into (6.7a) and (6.7b)

$$\min V_{N1} = \sum_{i=1}^{3} \left| V_{dci} + \Delta V_{dci} - \frac{V_{dc}}{3} \right| \tag{6.7a}$$

$$\min V_{N2} = \sum_{i=1}^{3} \left| V_{dci} + \Delta V_{dci} - \frac{V_{dc}}{3} \right| \tag{6.7b}$$

where (6.7a) presents the sum of three dc-link capacitors' voltages variations affected only by i_{N1}, and (6.7b) presents the sum of three dc-link capacitors' voltages variations affected only by i_{N2}. If $\min V_{N1} > \min V_{N2}$, it means the effect from i_{N1} leads to a relatively large dc-link capacitor voltage deviation and the desired current in the next switching cycle should flow through N2 to compensate the charging and discharging effect from i_{N1}. Therefore, optimum switching states should make the current flow through N2 and avoid flowing through N1. Vice versa, if $\min V_{N1} \leq \min V_{N2}$, which means the effect from i_{N2} leads to a relatively large dc-link capacitors' voltages deviation, the desired current in the next switching cycle should flow through N1 to compensate the charging and discharging effect from i_{N2}. Then, the optimum switching states should make the current flow through N1 and avoid flowing through N2.

Therefore, for the dc-link NP voltages balancing control, the corresponding duty cycle will be determined first according to the level of the modulation signal as in (6.4). The current flowing through different NPs and dc-link capacitors, which affects the voltage sharing among three capacitors will be evaluated by (6.3) (6.5) (6.6a) and (6.6b). The switching state which leads to the minimum value of the objective in (6.2) will be finally selected, which balances the dc-link NP voltages.

It should be noticed that even dc-link capacitors' voltages have been balanced during each fundamental period, however, if the modulation wave in Fig.6.4 is a purely open loop sinusoidal wave, C1 and C3 will always charge and discharge in every half fundamental period in a single-phase system. There will be voltage ripples at the NPs N1 and N2 and the frequency equals to the fundamental output. These low frequency voltage ripples can be reduced or eliminated in a three-phase system with zero-sequence voltage injection.

In summary, there are four steps to determine the final switching states in each switching period as shown in Fig.6.6, which is an extension of the flow chart in [13]. Firstly, check the output current direction. Secondly, according to the modulation signal, determine which voltage level the inverter is currently working on. Thirdly, compare the FC voltage with the FC reference voltage and check whether the error is within the predefined tolerance range. If the error is beyond the predefined tolerance range, the FC voltage control will be activated and the corresponding switching states will be selected. Fourthly, if the above FC voltage error is within the predefined tolerance range, the dc-link NP voltages balancing control is activated. In practice, the switching actions in Table IV.II need to be reconsidered with the effect of dead-time. Otherwise, 'two-level jump' phenomenon will occur during the operation, which will cause unwanted larger switching loss as well as higher dv/dt on switching devices. A practical 'two-level jump' effect during a 70V dc-link voltage operation without considering the dead-time effect has been demonstrated in Appendix G I.

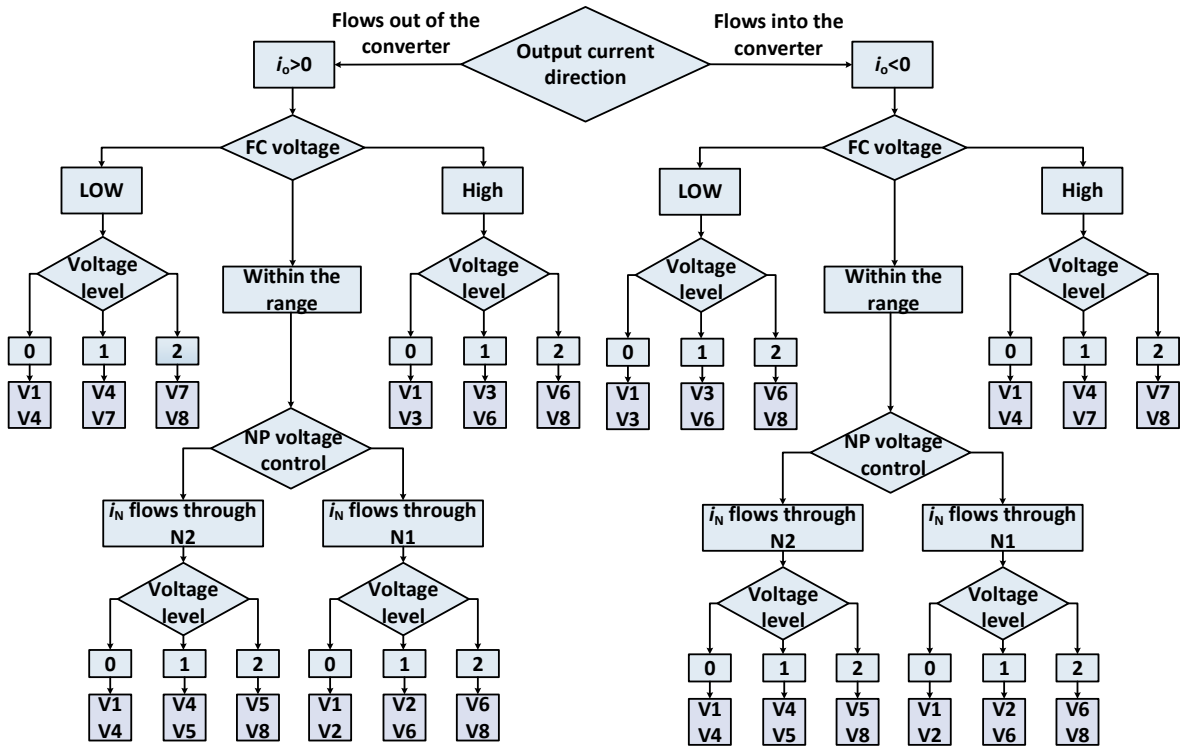
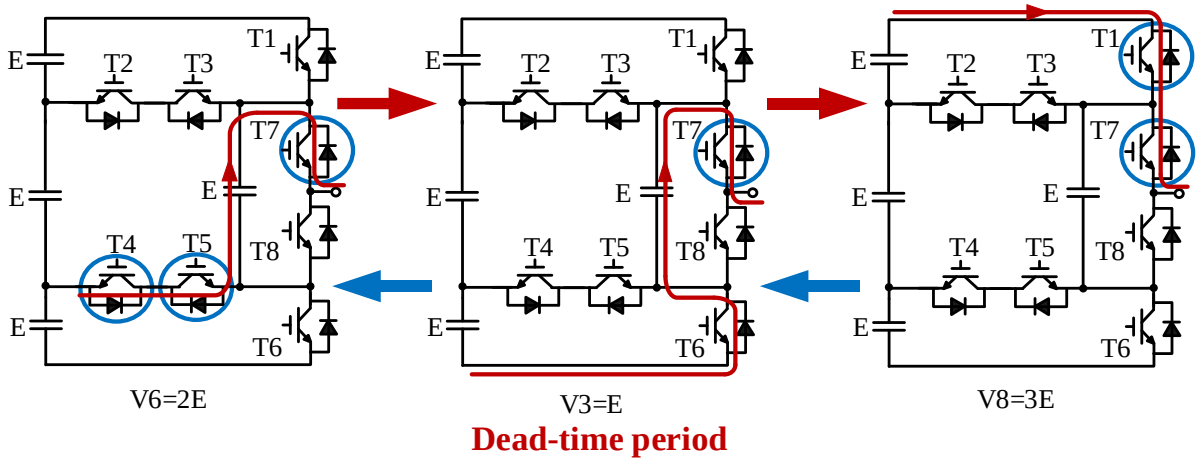


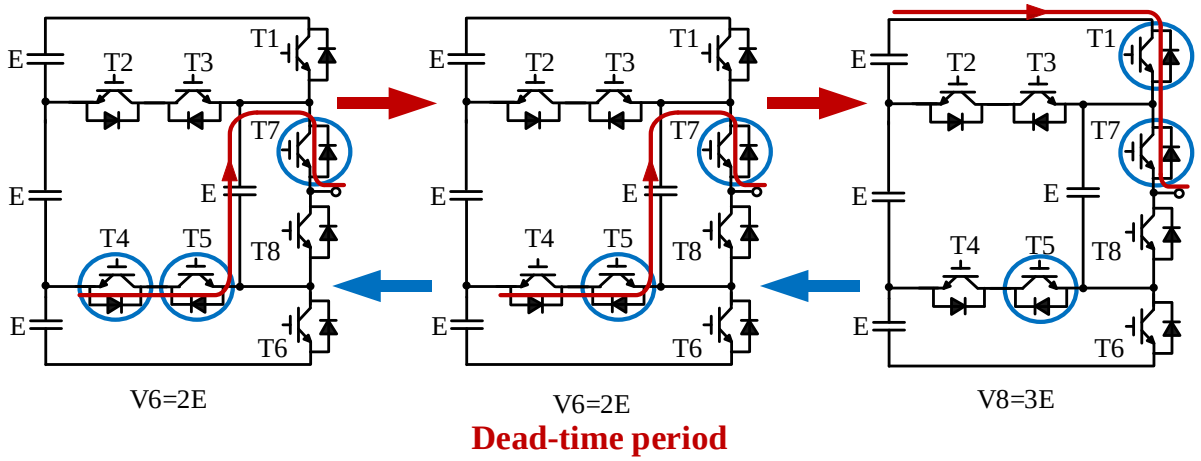
Figure 6.6 Control and modulation flowchart

There're totally six switching states groups situations which will cause the two-level jump. Take the V6 V8 group when the current flows out of the converter for example as shown in Fig.6.7. When the converter in V6 switching state, T4, T5, T7 are in on-state, the current flows through the antiparallel diode of T4, T5, then T7 out of the inverter. And the output voltage is 2E as shown in Fig. 6.7 (a), where the device inside the blue cycle turns on. When the converter in V8 switching state, T1, T7 turn-on, the current flows through T1 and T7 out of the inverter as shown in Fig. 6.7 (a) as well. T7 keeps turn-on during the V6 V8 swithing group as shown in Table VI.II. However, in the practical test, a dead-time has been introduced in the swithcing group in order to prevent the shot-through due to complimentary devices both turn on. Here during the dead-time period, T4, T5, T1 are in turn-off state, only T7 turns on, the current flows through the antiparallel diode of T6, the FC then T7 out of the inverter, the output voltage is E. This switching state during the dead-time period between V6 and V8 becomes V3. This causes the two-level jump as shown in Appendix G.I. To deal with this problem, just keeps T5 always in on-state during the commutation between V6 and V8, thus the swithcing state during the dead-time period will be still V6, then, aviod the two-level jump phenomenon. Meanwhile, by adjusting the switching action in V6, V8 switching group, the number of switching devices performs switching

actions has reduced to two compared to the number in Table VI.II, which reduces the swithcing loss.



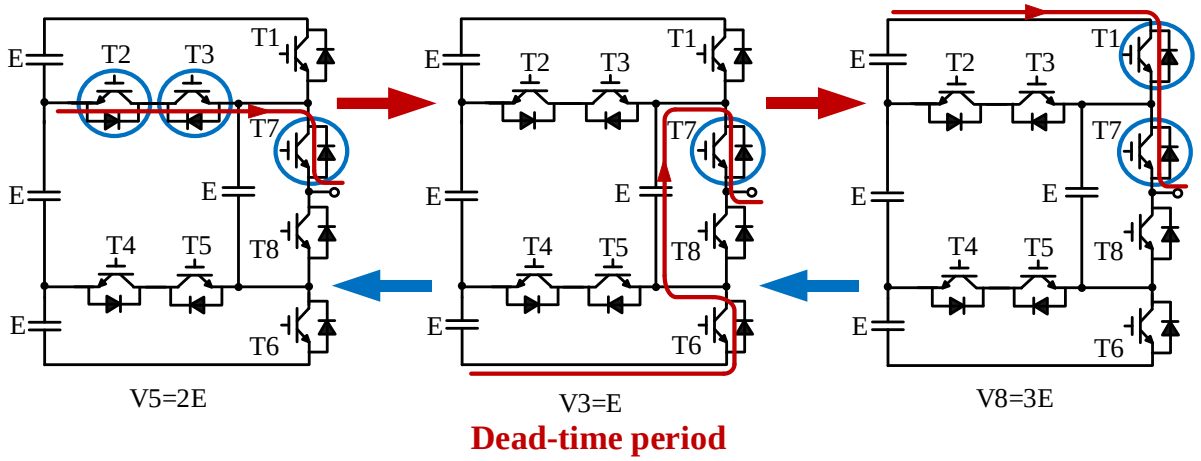
(a) V6 V8 commutation without correction



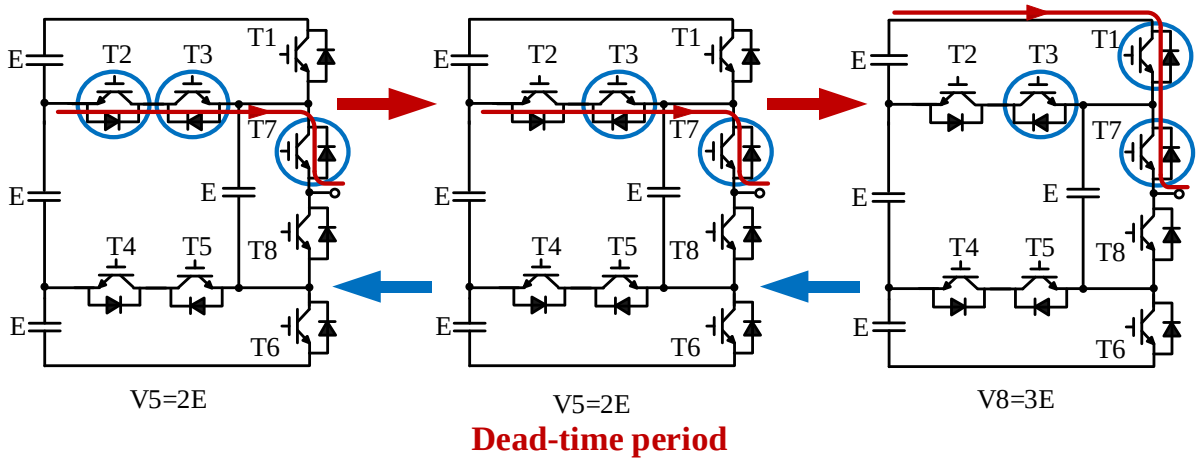
(b) V6 V8 commutation with correction

Figure 6.7 V6, V8 switching states when io>0

Fig.6.8 presents the V5 V8 group when the current flows out of the converter situation. Actually the dead-time effect in this group will not only cause the double-jump phenomenon, but also affect the state of FC voltage as shown in Fig.6.8 (a). During the dead-time in Fig. 6.8 (a), only T7 is in turn-on state, the current flows through the anti-paralle diode of T6, FC, then T7 out of the converter. It makes the inverter output voltage become to E and also discharges the FC which is not desireable during this commutation preocess and will affect the system control performance. The solution is the same, just keep T3 always on during commutation as shown in Fig. 6.8 (b).



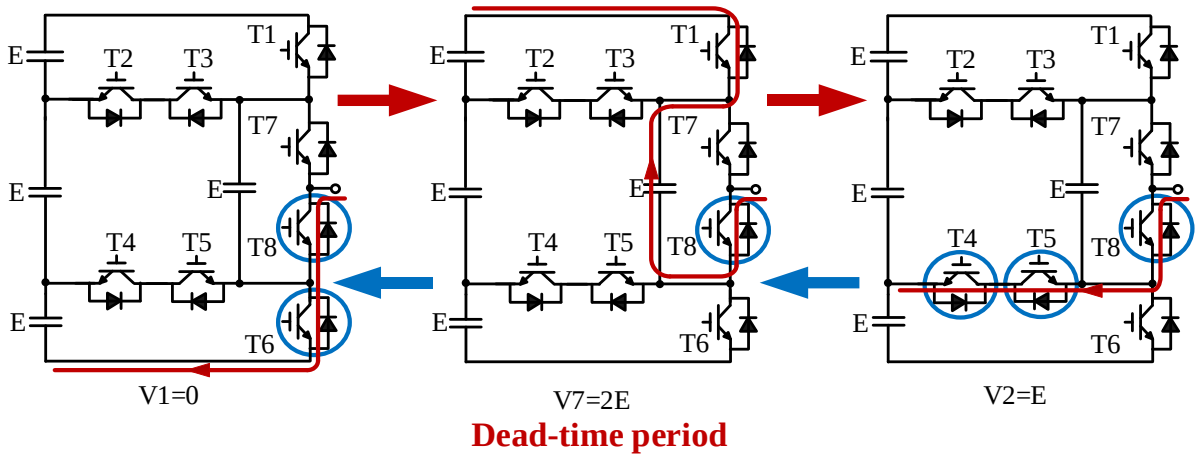
(a) V5 V8 commutation without correction



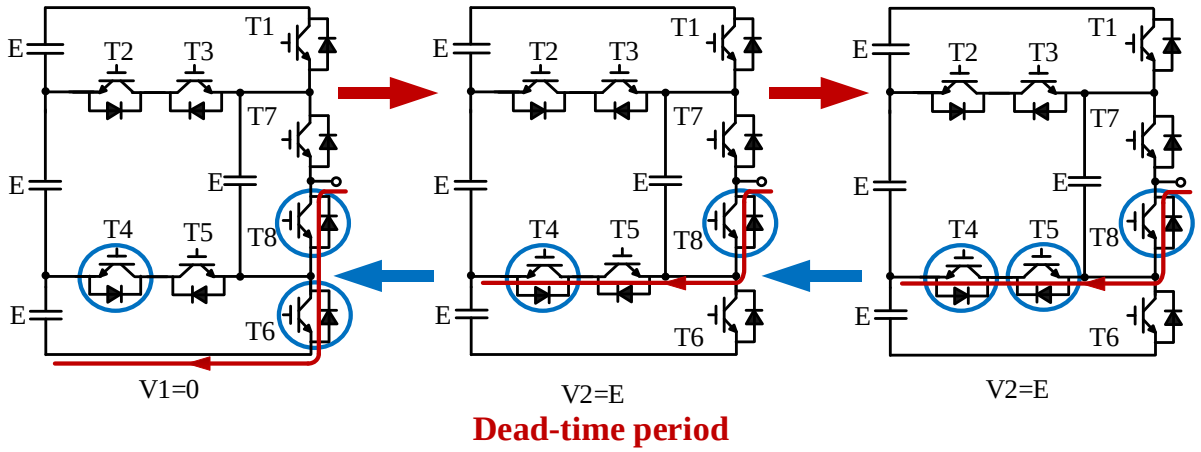
(b) V5 V8 commutation with correction

Figure 6.8 V5, V8 switching states when io>0

For V1 V2 group when the current flows into the converter situation, the solution is keeping T4 always on during the commutation as shown in Fig. 6.9.



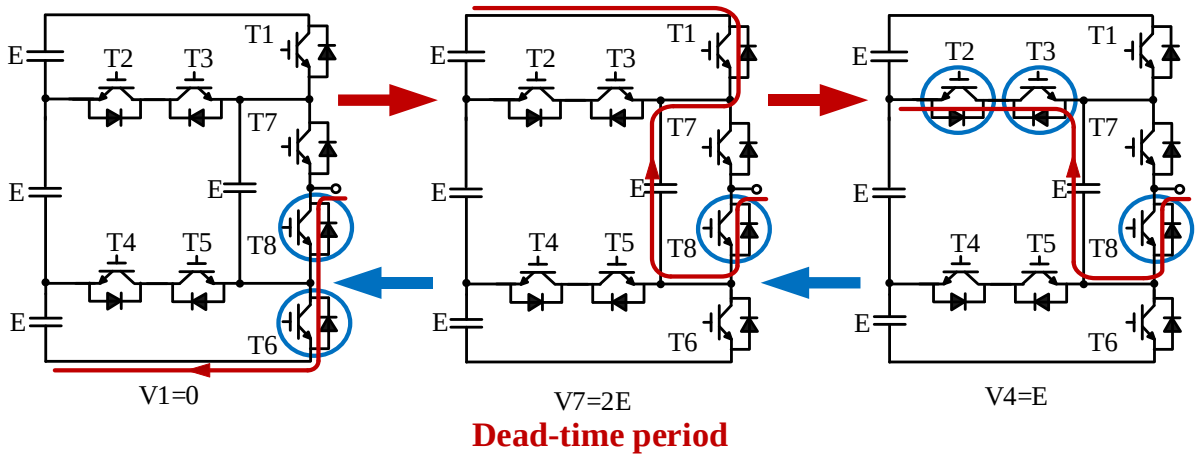
(a) V1 V2 commutation without correction



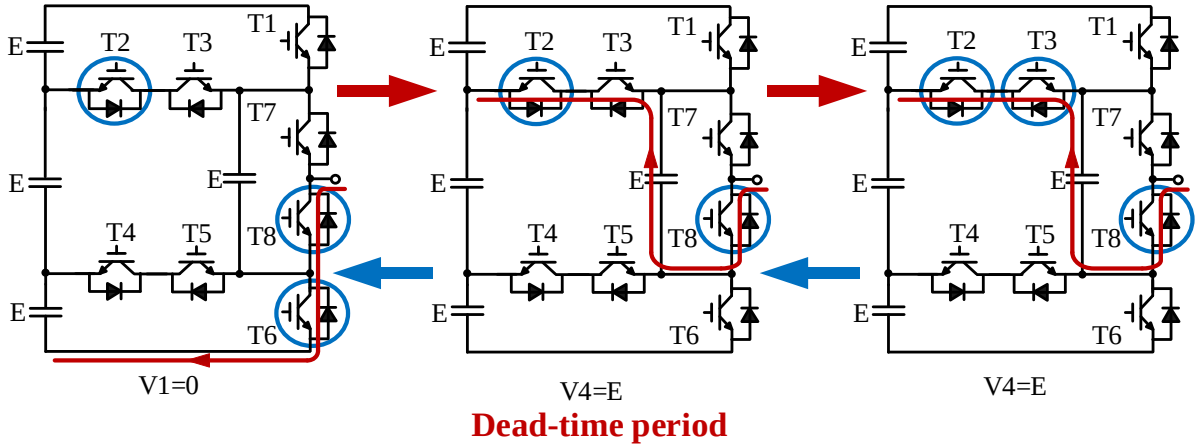
(b) V1 V2 commutation with correction

Figure 6.9 V1, V2 switching states when io<0

For V1 V4 group when the current flows into the converter situation, the solution is keeping T2 always on during the commutation as shown in Fig. 6.10.



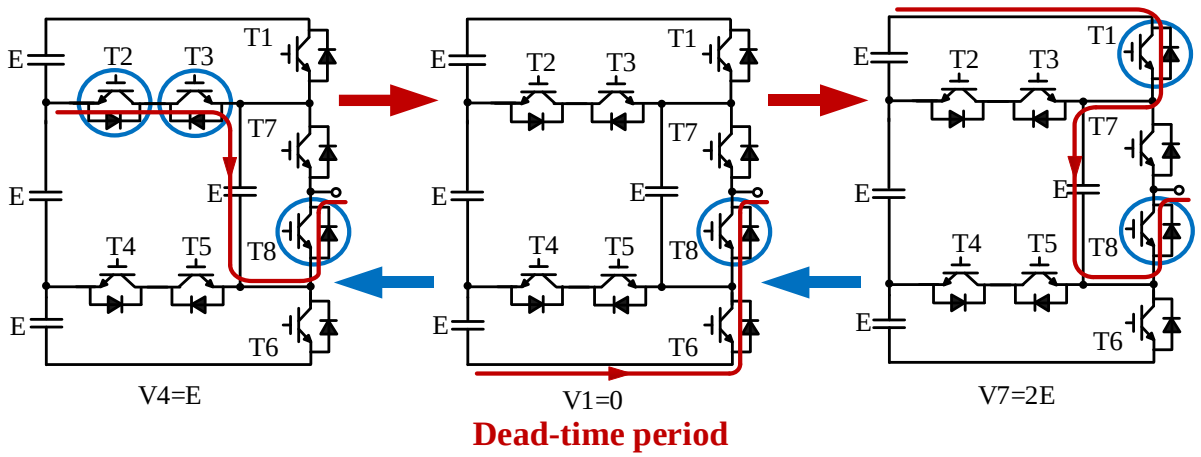
(a) V1 V4 commutation without correction



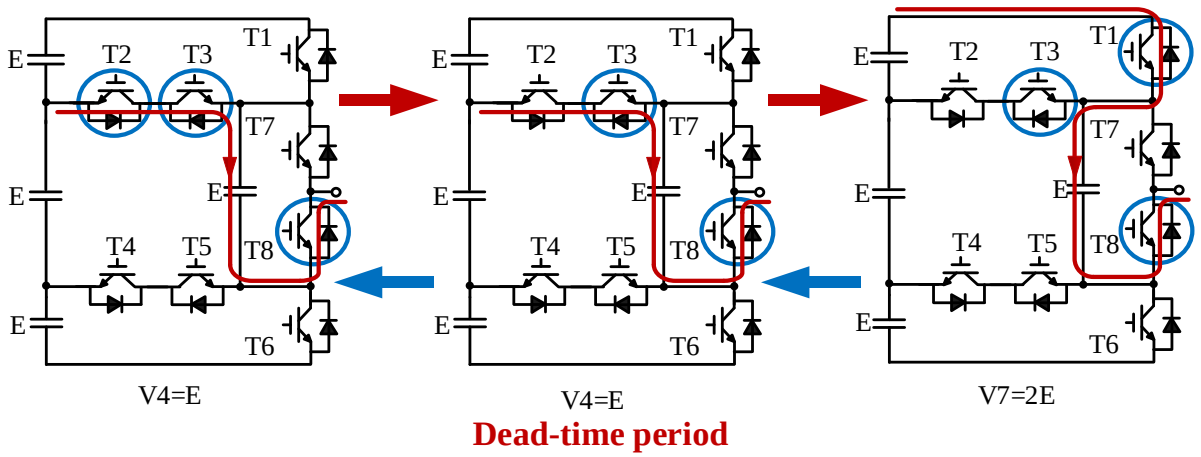
(b) V1 V4 commutation with correction

Figure 6.10 V1, V4 switching states when io<0

For V4 V7 group when the current flows out of the converter situation, the solution is keeping T3 always on during the commutation as shown in Fig. 6.11.



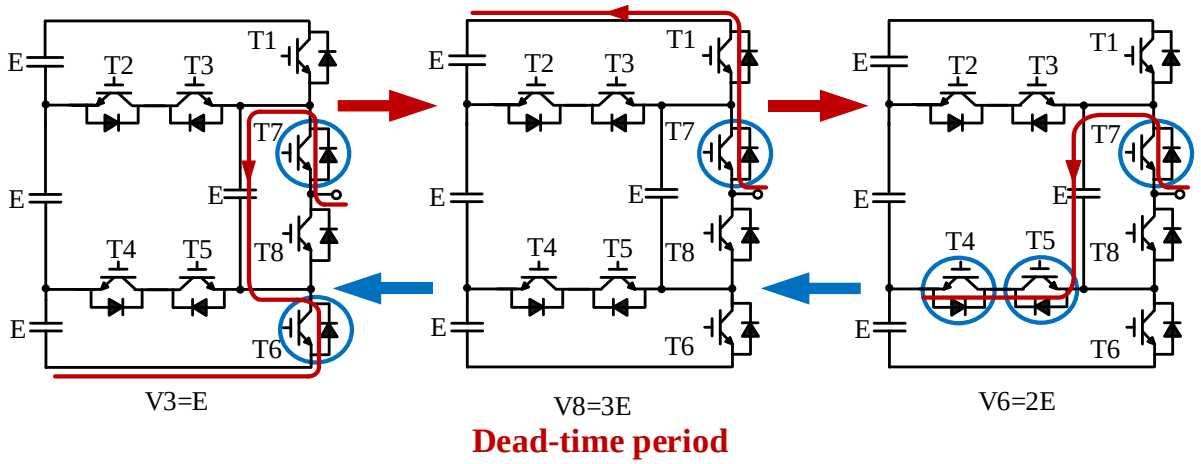
(a) V4 V7 commutation without correction



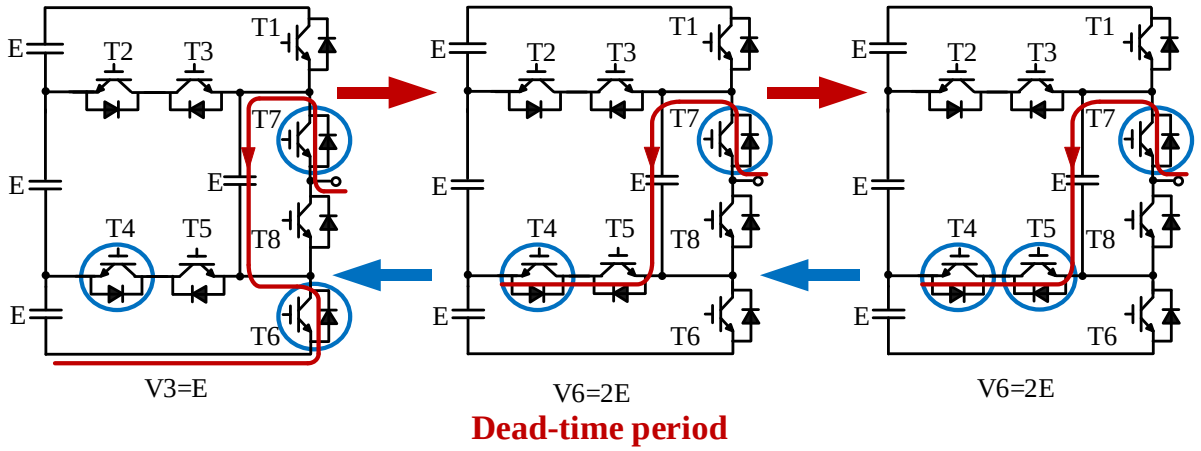
(b) V4 V7 commutation with correction

Figure 6.11 V4, V7 switching states when io>0

For V3 V6 group when the current flows into the converter situation, the solution is keeping T4 always on during the commutation as shown in Fig.6.12.



(a) V3 V6 commutation without correction



(b) V3 V6 commutation with correction

Figure 6.12 V3, V6 switching states when io<0

In summary, with considering the dead-time effect, the modified switching states truth table according to different switching groups is presented in Table VI.III.

TABLE VI.III SWITCHING STATES FOR DIFFERENT SWITCHING GROUPS ACCORDING TO THE VOLTAGE LEVEL WITH THE DEAD-TIME EFFECT ELIMINATION

Group	Switching state	T1	T2	T3	T4	T5	T6	T7	T8	V_o
V1, V2	V1	0	0	0	1	1	0	0	1	0
	V2	0	0	0	1	0	1	0	1	E
V1, V3	V1	0	0	0	0	0	1	1	0	0
	V3	0	0	0	0	0	1	0	1	E
V1, V4	V1	0	1	1	0	0	0	0	1	0
	V4	0	1	0	0	0	1	0	1	E
V2, V6	V2	0	0	0	1	1	0	1	0	E
	V6	0	0	0	1	1	0	0	1	2E
V3, V6	V3	0	0	0	1	1	0	1	0	E
	V6	0	0	0	1	0	1	1	0	2E
V4, V5	V4	0	1	1	0	0	0	1	0	E
	V5	0	1	1	0	0	0	0	1	2E
V4, V7	V4	1	0	1	0	0	0	0	1	E
	V7	0	1	1	0	0	0	0	1	2E
V5, V8	V5	1	0	1	0	0	0	1	0	2E
	V8	0	1	1	0	0	0	1	0	3E
V6, V8	V6	1	0	0	0	1	0	1	0	2E
	V8	0	0	0	1	1	0	1	0	3E
V7, V8	V7	1	0	0	0	0	0	1	0	2E
	V8	1	0	0	0	0	0	0	1	3E

6.4 Simulation

The concept configuration of the proposed single-phase hybrid-clamped four-level π-type converter is shown in Fig.6.13. In order to make sure the successful operation, the phase-leg output has to be returned back to the mid-point of the dc-link. An identical single-phase simulation system has been established in MATLAB/Simulink to verify the proposed FC voltage control and the dc-link NP voltages

balancing control strategy for the hybrid-clamped four-level π-type inverter. The simulation model is shown in Appendix D III.

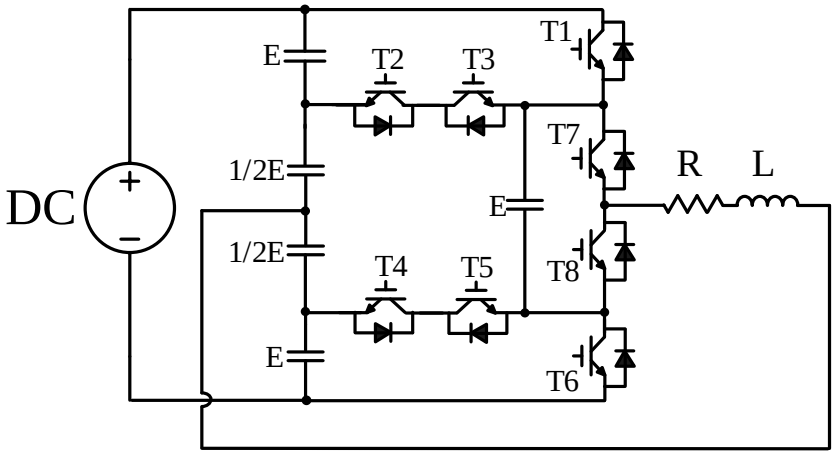


Figure 6.13 Concept configuration of the single-phase hybrid clamped four-level π-type converter

The input dc-link voltage is 300V, modulation index is 0.95. Fundamental frequency is 50 Hz. The inverter supplies power to a single-phase RL load 25Ω, 5mH. Full list of simulation setup and parameters of this single-phase hybrid clamped four-level π-type converter is shown in Table VI.IV and Table VI.V, respectively.

Zero-order Hold is employed in order to imitate the ADC sampling process of the practical circuit. The Internal resistance Ron is selected as the default value 0.01 in order to make it similar to a practical IGBT. The snubber resistance and capacitance are selected as the default. In practical, both dc-link capacitor and FC will be charged to some level but lower than the desired value before the PWM signals applied on them. Therefore, in the simulation system, initial voltages setting for both dc-link capacitor and FC are 80% of the desired value.

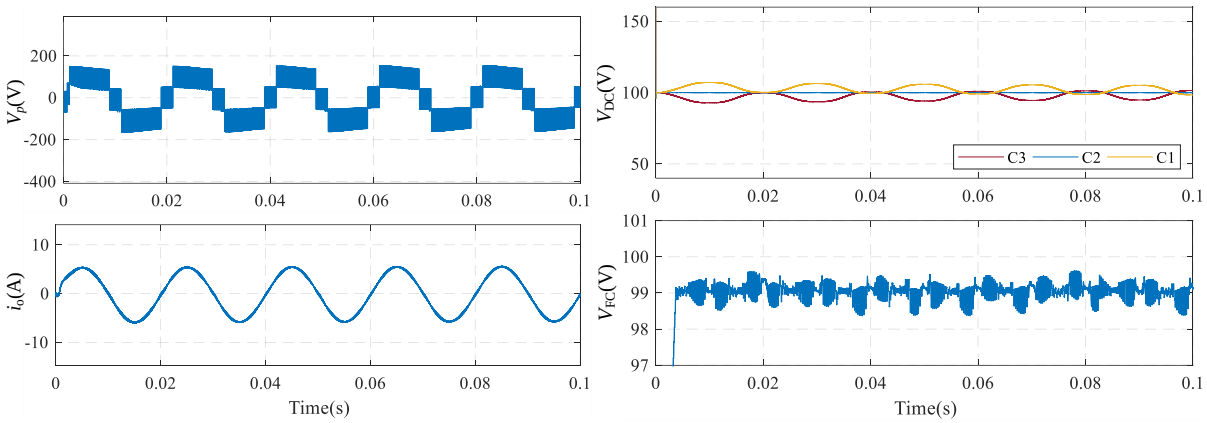
TABLE VI.IV THREE-PHASE SYSTEM SIMULATION PARAMETERS

Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs
Zero-Order Hold sample time	100 μs
Deadtime model	On/Off Delay (On delay, Time delay:2μs)
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, cap initial voltage 100V)
FC model	Series RLC Branch (Branch type: C, cap initial voltage 80V)

TABLE VI.V PARAMETERS OF SINGLE-PHASE HYBRID CLAMPED FOUR-LEVEL Π-TYPE CONVERTER

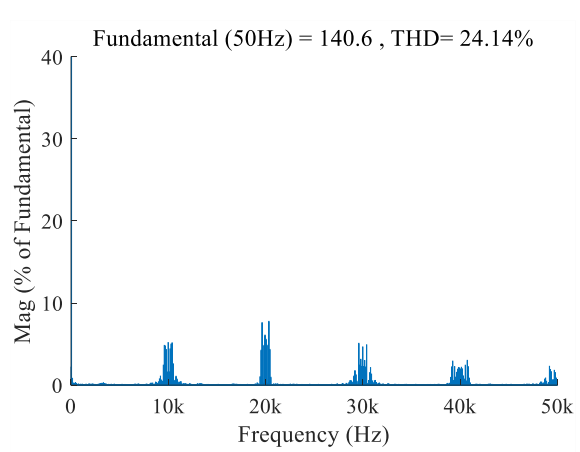
Parameters	Values
DC-link voltage	V_{dc} = 300 V
DC-link capacitors	C1=C2=C3=2000 μF
FC	C_{fc} = 300 μF
FC voltage deviation	V_{tol} =1V
Fundamental frequency	fo = 50 Hz
Load	R = 25 Ω, L = 5 mH
Modulation index	m = 0.95
Dead-time	t_d = 2 μs

Fig.6.14 (a) (b) (c) (d) show output waveforms under the switching frequency f_s=10 kHz. Fig.6.14 (a) upper figure shows the output phase voltage which has four levels, and Fig.6.14 (a) lower figure shows the output current which is sinusoidal as expected. Fig.6.14 (b) shows dc-link capacitors' voltages and the FC voltage which are all well regulated around 100V. Voltage ripples are observed across the upper and lower dc-link capacitors at a fundamental frequency 50 Hz. The FC voltage is actually around 99V, 1V less than the reference value which is expected as introduced in section 6.3 a). Fig.6.14 (c) (d) show the FFT analysis of the output phase voltage and current, respectively. Fig.6.14 (e) (f) (g) (h) show output waveforms under the switching frequency f_s=20 kHz. Fig.6.14 (e) upper figure shows the output phase voltage which has four levels as well, and Fig.6.14 (e) lower figure shows the output current which is sinusoidal as well. Fig.6.14 (f) shows dc-link capacitors' voltages and the FC voltage which are all well regulated around 100V, on-third of the total dc-link voltage, the same as shown in Fig.6.14 (b). The FC voltage ripple can be monitored less than that in Fig.6.14 (b) due to the larger switching frequency. Fig.6.14 (g) (h) show the FFT analysis of the output phase voltage and current, respectively. The THD of current under f_s=20 kHz is less than that of 10 kHz situation due to the lower high switching frequency harmonic contents.

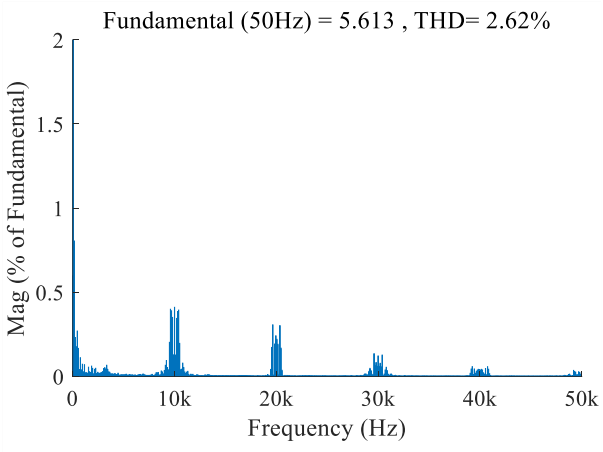


(a) Phase voltage and current (f_s=10 kHz)

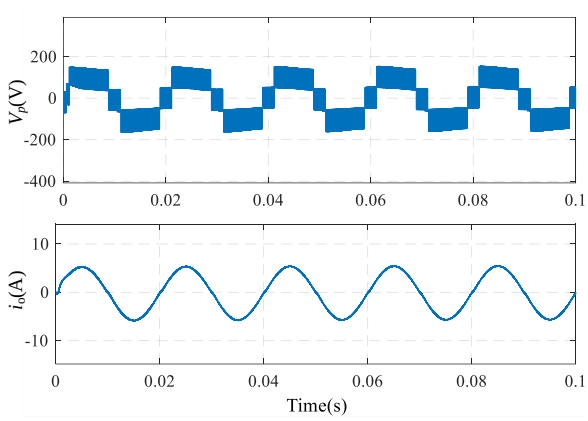
(b) DC-link capacitors' voltages and FC voltage(f_s=10 kHz)



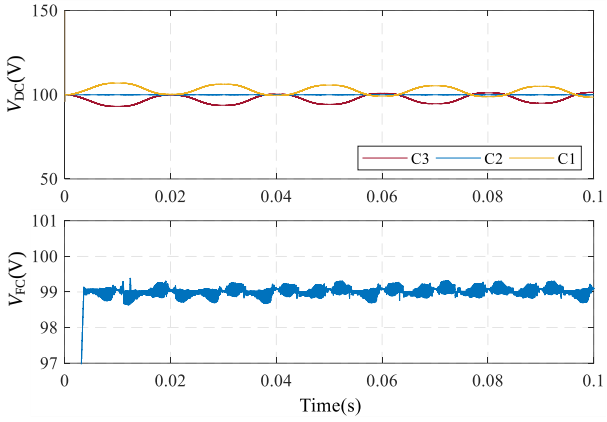
(c) FFT analysis of V_p (f_s=10 kHz)



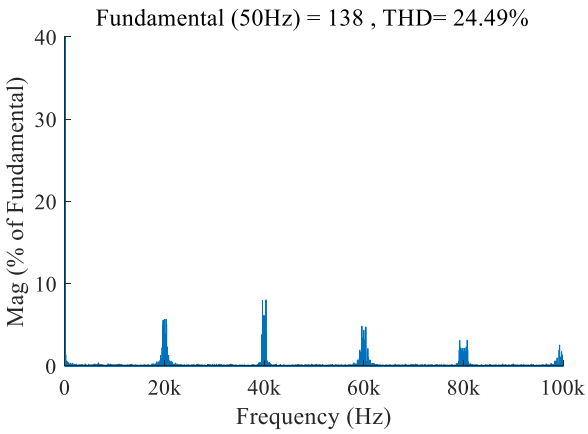
(d) FFT analysis of i_o (f_s=10 kHz)



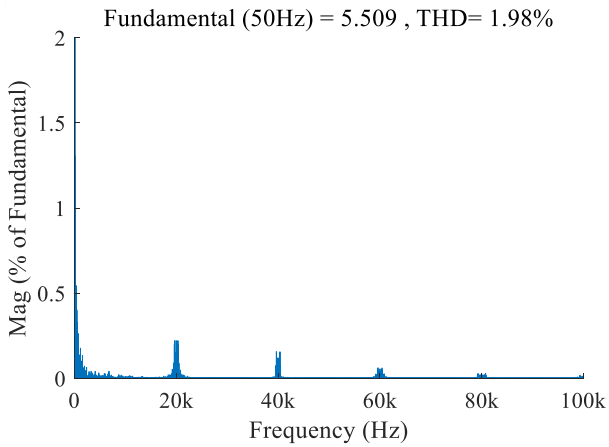
(e) Phase voltage and current (f_s=20 kHz)



(f) DC-link capacitors' voltages and FC voltage (f_s=20 kHz)



(g) FFT analysis of V_p (f_s=20 kHz)



(h) FFT analysis of i_o (f_s=20 kHz)

Figure 6.14 Simulation results of the single-phase hybrid clamped four-level π-type converter

6.5 Prototype and exprimental results

a) Experimental results with the presented control

As mentioned in section 6.1, one characteristic of this topology is the ability to operate as a single phase-leg system with balanced dc-link NP voltages. To verify the proposed control scheme for the hybrid-clamped four-level π-type converter especially the single phase-leg operation, a single-phase prototype has been built with 600V IGBTs (IKW30N60H3) as shown in Fig.6.15. The PCB layout view is shown in Appendix E III. The full list of components for the single-phase hybrid clamped four-level π-type converter is shown in Table VI.VI. The inverter is also controlled by the DSP-FPGA (XILINX SPARTAN XC3S400, and TI TMS320 F2833) control board which has been used in Chapter 4 and Chapter 5. The control codes for DSP and FPGA are shown in Appendix F II.

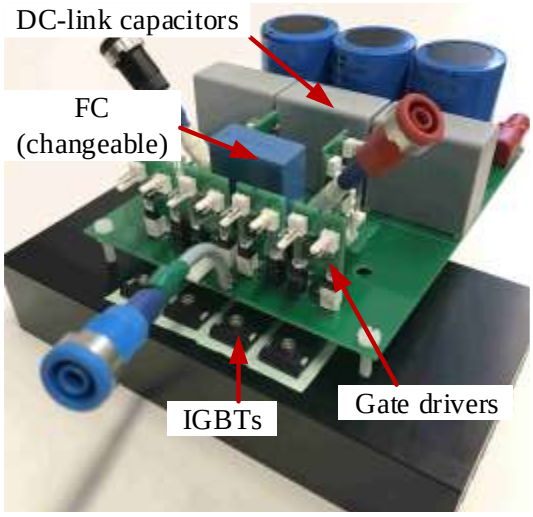


Figure 6.15 Experimental prototype of the hybrid-clamped four-level π-type single-phase inverter

TABLE VI.VI LIST OF COMPONENTS FOR THE SINGLE-PHASE HYBRID CLAMPED FOUR-LEVEL Π-TYPE CONVERTER

dc-link capacitors 1	MAL215990125E3 (1000μF/315V) × 3
dc-link capacitors 2	VISHAY 1848 MKP ((20μF/700V) × 3
dc-link parallel resistors	100kΩ/2W × 3
Switches	IKW30N60H3 (600V) × 8
Gate driver chips	HCPL 0314 × 8
Gate resistors	10Ω (SMD 0806) × 8
Gate driver input resistors	680Ω (SMD 0806) × 8
Gate driver output decoupling caps	0.1μF (SMD 0806) × 8
Heatsink	97CN-01500-A-200

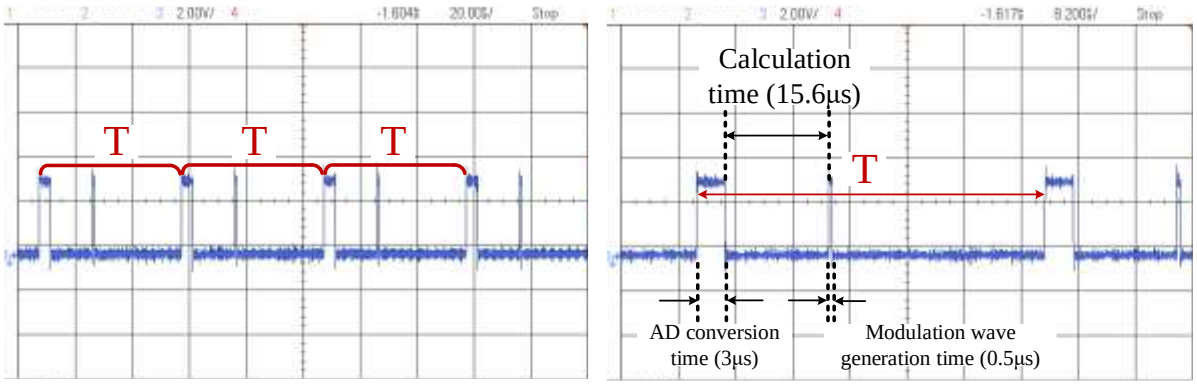
With modified switching states arrangement in Table VI.III, the 300V dc-link voltage test has been performed. Table VI.VII lists the parameters do perform the test.

TABLE VI.VII TEST PARAMETERS FOR SINGLE-PHASE HYBRID CLAMPED-FOUR-LEVEL Π-TYPE CONVERTER

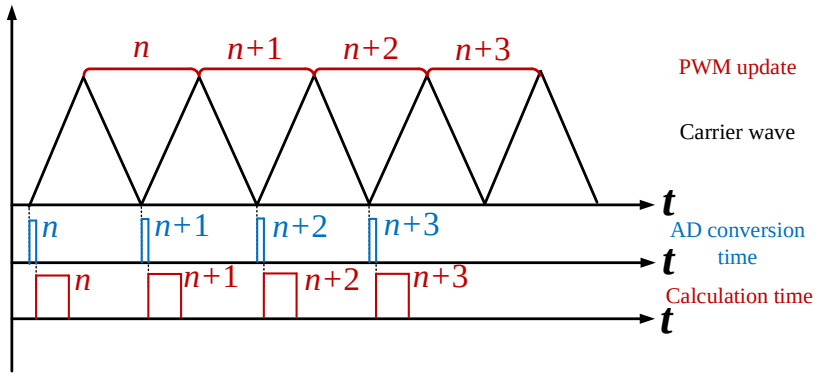
V_{dc}	300V
Load	25Ω, 5mH
Fundamental frequency	50 Hz
FC voltage deviation	V_{tol} =1V
C_{fc}	50μF
C1, C2, C3	2000μF
T1 – T8	IKW30N60H3 (600V)
Modulation index	0.95
Dead-time	2μs

Fig.6.16 presents the execution time of the control algorithm for the signal-phase hybrid clamped four-level π-type converter, the sampling frequency is set to equal to the switching frequency. Put the AD conversion time, calculation time as well as the modulation wave generation time together, the total execution time of the control algorithm is 19.1μs. For a 10 kHz or 20 kHz switching frequency/sampling

frequency, this total execution time is less than the half of the switching period/sampling period. Therefore, the preferred modulation waveform update point can be the mid-point of the carrier wave. For example, as shown in Fig.6.16 (c), if the AD conversion starts at the bottom of the carrier wave, the upcoming peak of the carrier wave can be the modulation wave update point. Basically, with this setting, the time delay between the AD sampling point and the modulation wave update point can be reduced to half of the switching period/sampling period. This can improve the system dynamic response as well as the reliability. One thing should be mentioned here, as the default ADC input filter cutoff frequency equals to 1.29 kHz which is relatively low for the sampling requirement for the FC control. Therefore, it has been changed in order to fix this issue (the detailed technical process and analysis is shown in Appendix G II).



(a) Actual time of each sampling period (b) Zoomed-in actual code execution time

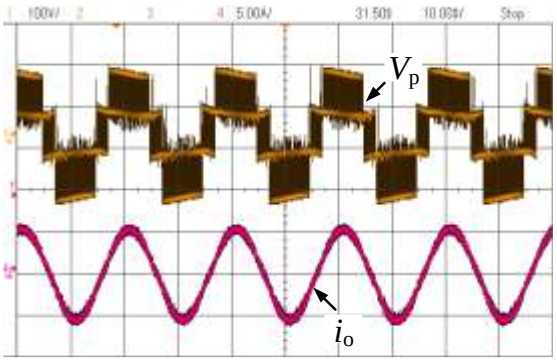


(c) signal delay concept within in the DSP/FPGA control board

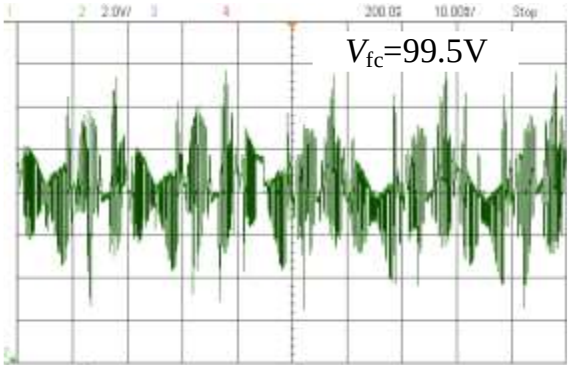
Figure 6.16 Monitored back-to-back system DSP/FPGA code execution time through DAC

Fig.6.17 presents the single-phase hybrid-clamped four-level π-type converter output waveforms under the 10 kHz switching frequency. Fig. 6.17 (a) shows the output phase voltage V_p which is of four levels

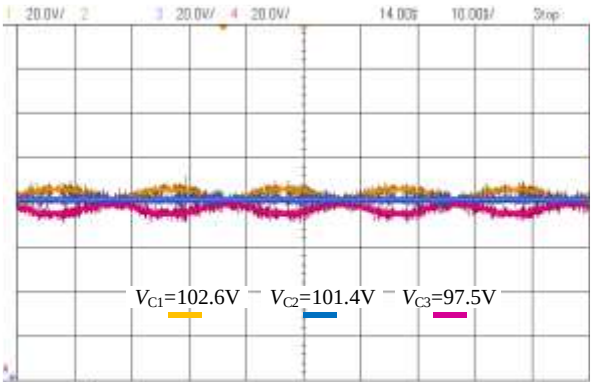
as expected, and the output current i_o is sinusoidal. Fig. 6.17 (b) shows the FC voltage. It is well regulated at around 100V. Due to the relatively small FC value, the high frequency voltage ripple amplitude is about 6V. Fig.6.17 (c) show three dc-link capacitors' voltages. Waveforms have shown these three voltages are well regulated around 100V as well. A low frequency voltage ripple is observed across the upper and lower capacitor at a fundamental frequency 50 Hz. Fig.6.17 (d) shows the FFT analysis of the output current in Fig.6.17 (a),



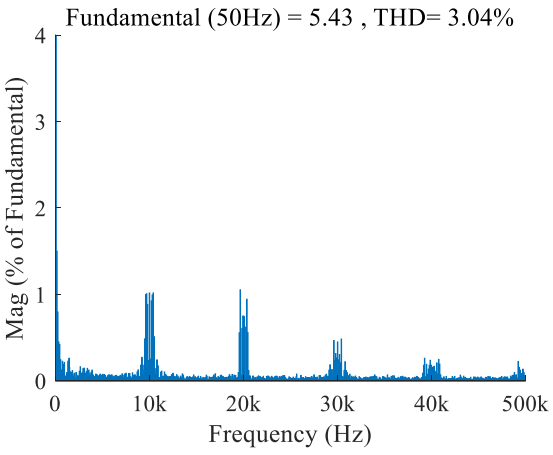
(a) Output phase voltage and current



(b) FC voltage



(c) dc-link capacitors voltages

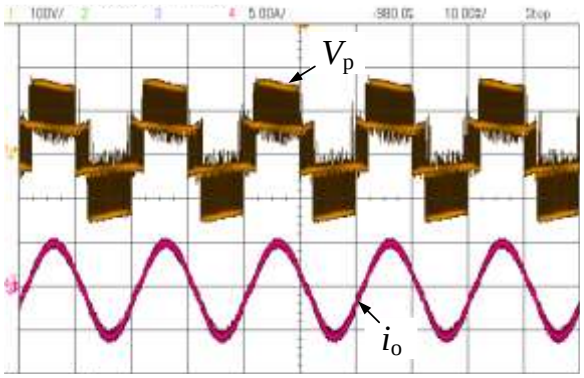


(d) Output current harmonics spectrum

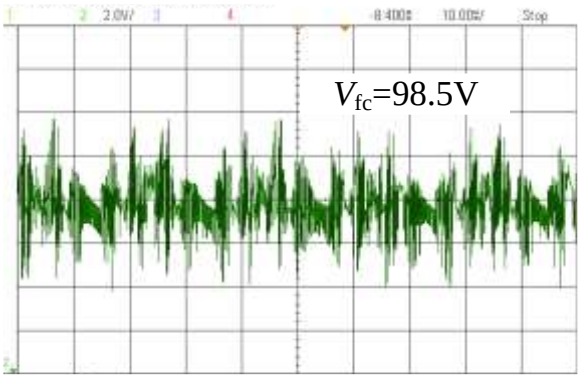
Figure 6.17 Single-phase hybrid clamped four-level π-type converter test waveforms at 10 kHz switching frequency

Fig.6.18 presents the single-phase hybrid clamped four-level π-type converter output waveforms under the 20 kHz switching frequency. Fig. 6.18 (a) shows the output phase voltage V_p which is of four levels as expected, and the output current i_o is sinusoidal. Compare with the current waveform in Fig.6.17 (a), the current waveform in Fig.6.18 (a) is slightly thinner due to the relatively lower high frequency distortion. Fig. 6.18 (b) shows the FC voltage which is well maintained at around 100V. It can be noted,

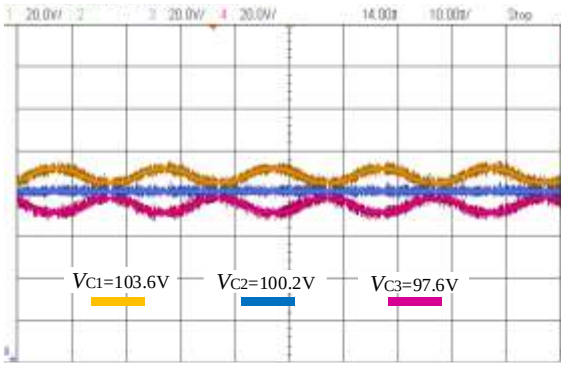
the FC voltage ripple in Fig.6.18 (b) is lower than that in Fig.6.17 (b). Fig.6.18 (c) show dc-link capacitors' voltages as well. All three dc-link capacitors voltages are well regulated around 100V. Voltage ripples are also observed across the upper and lower capacitor at a fundamental frequency 50 Hz. Fig.6.18 (d) presents the FFT analysis of the output current in Fig.6.18 (a), which presents a lower total THD compares to the 10 kHz switching frequency condition.



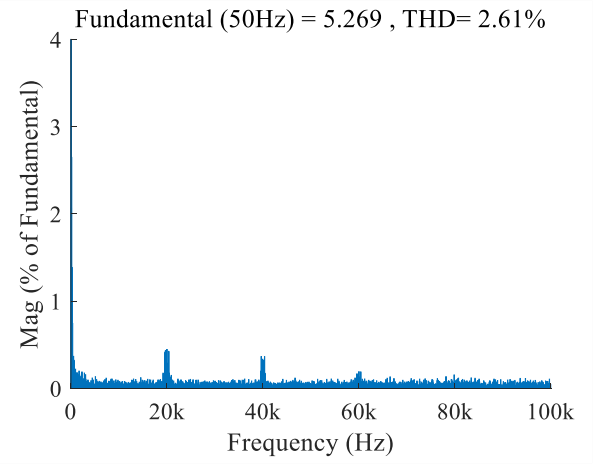
(a) Output phase voltage and current



(b) FC voltage



(c) dc-link capacitors voltages



(d) FFT analysis of output current

Figure 6.18 Single-phase hybrid clamped four-level π-type converter test waveforms at 20 kHz switching frequency

b) FC voltage variation

Through the comparison of FC voltage waveforms under the two switching frequencies10 kHz and 20 kHz conditions, it can be noticed, the higher the switching frequency, the lower the FC voltage ripple. As the current direction of the FC will be modified each individual switching period, thus the voltage

ripple of the FC changes in each individual switching period.

Fig.6.19 presents the zoomed-in simulation FC voltage waveform as well as the corresponding output phase voltage and current of waveforms shown in section 6.4. Under a unity power factor and a high modulation index condition, it can be noticed that the maximum high frequency FC voltage ripple occurs periodically at positions where the red arrows point to. These positions are within the commutation between 0~E or 2E~3E. Taking the switching group V6, V8 in Fig.6.2 above for example, with a unity power factor, V6 discharges the FC, while V8 does not. Meanwhile, for a carrier-based sinusoidal modulation, at the red arrowed position, the amplitude of the current is relatively large, and the time duration of V6 (2E) is much larger than that of V8 (3E). That's the reason why the large FC voltage ripple happens in these positions.

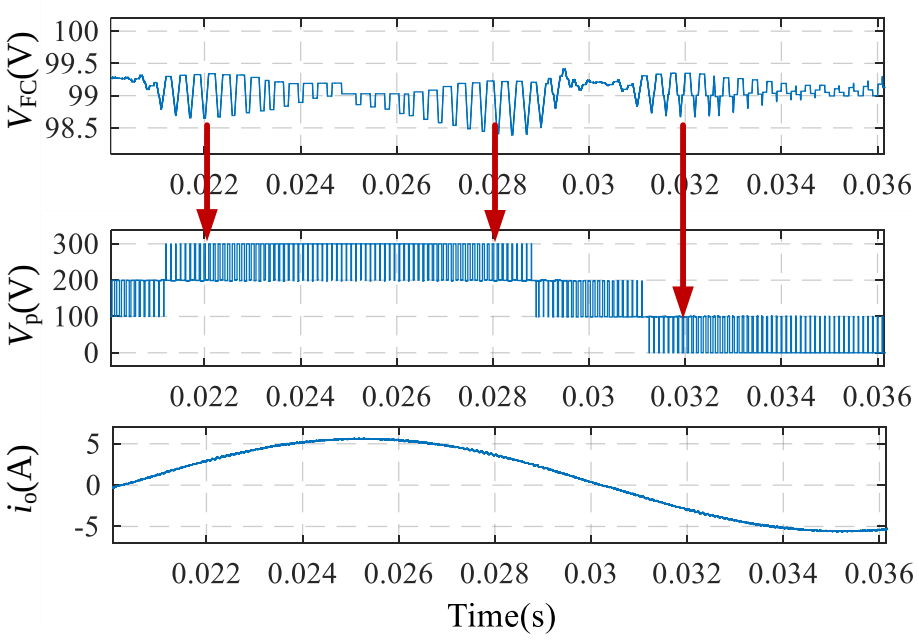
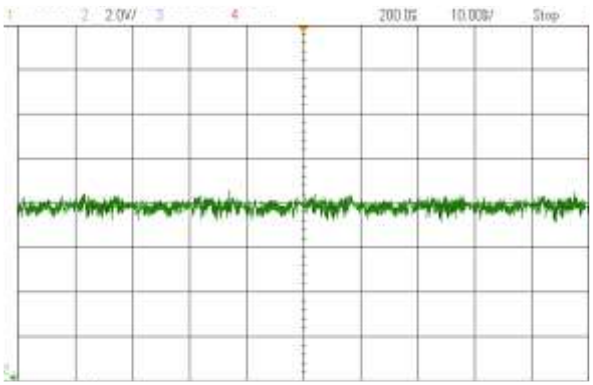
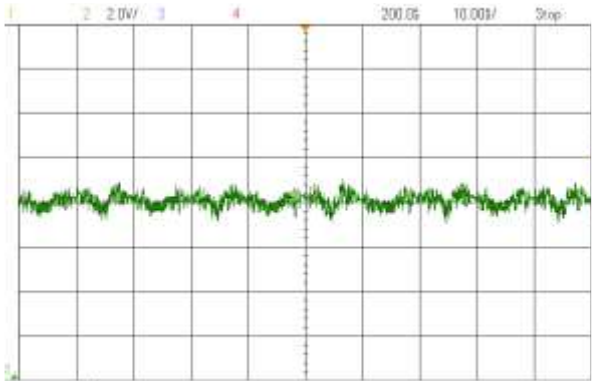


Figure 6.19 Single-phase simulation FC voltage, output phase voltage and current (Zoomed)

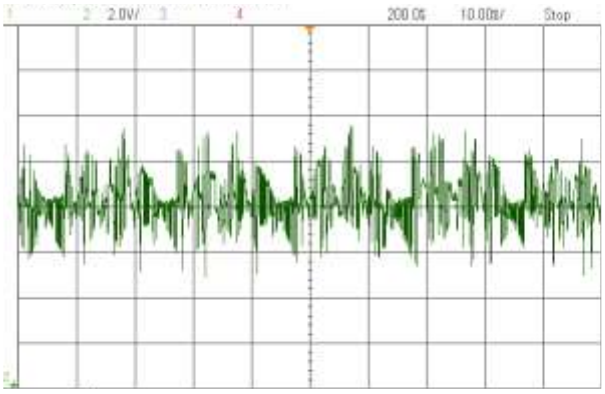
Fig.6.20 presents experimental FC voltage ripples under groups of different conditions, it can be monitored that the FC voltage ripple is proportional to the output current amplitude I_o, and inversely proportional to FC capacitance C_{FC} and the switching frequency f_s.



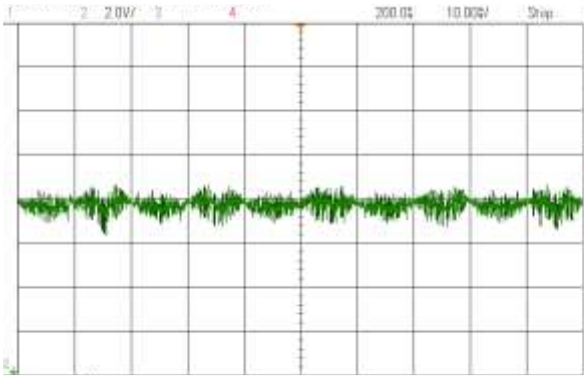
(a) I_o=3.24A, f_s=10 kHz, C_{FC}=300μF



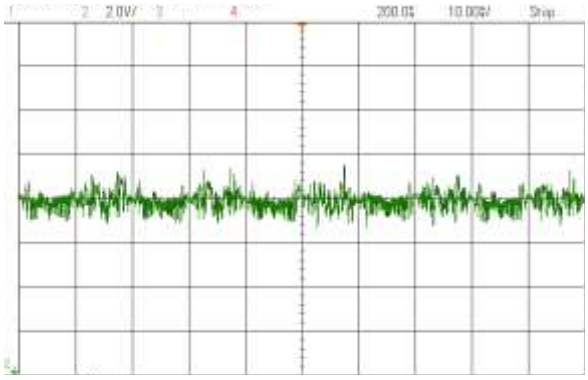
(b) I_o=3.24A, f_s =10 kHz, C_{FC} =200μF



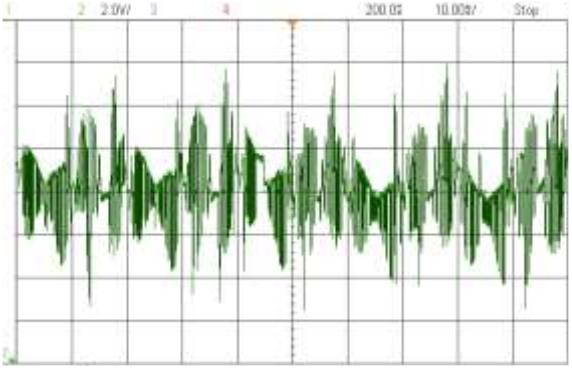
(c) I_o=3.24A, f_s =10 kHz, C_{FC} =50μF



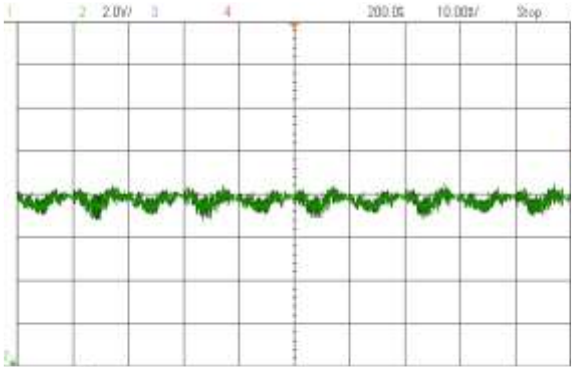
(d) I_o=5.7A, f_s =10 kHz, C_{FC} =300μF



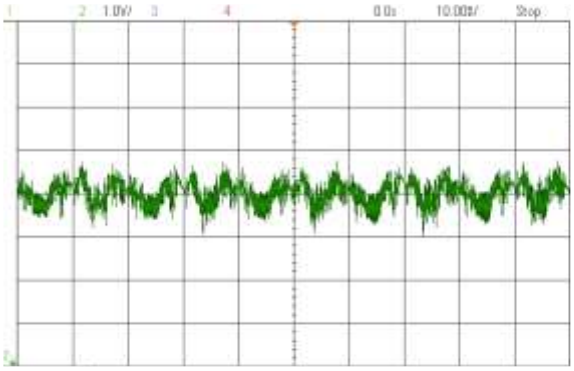
(e) I_o=5.7A, f_s =10 kHz, C_{FC} =200μF



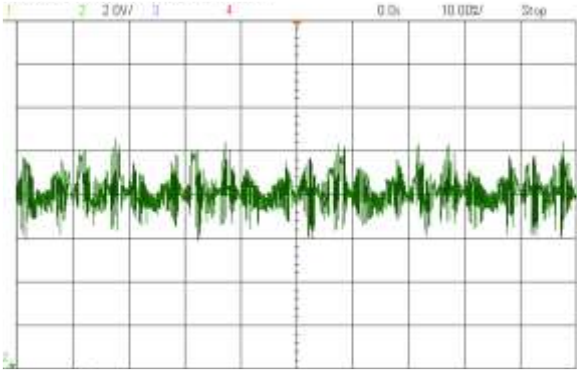
(f) I_o=5.7A, f_s =10 kHz, C_{FC} =50μF



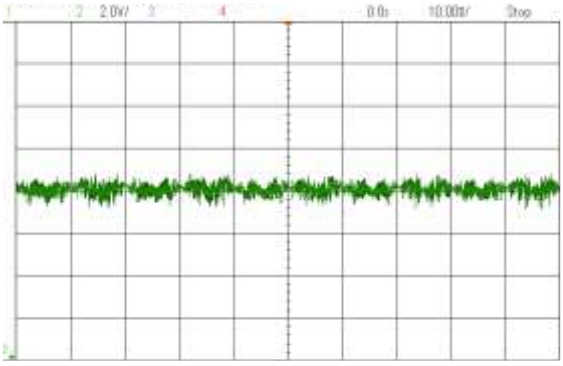
(g) I_o=3.24A, f_s =20 kHz, C_{FC} =300μF



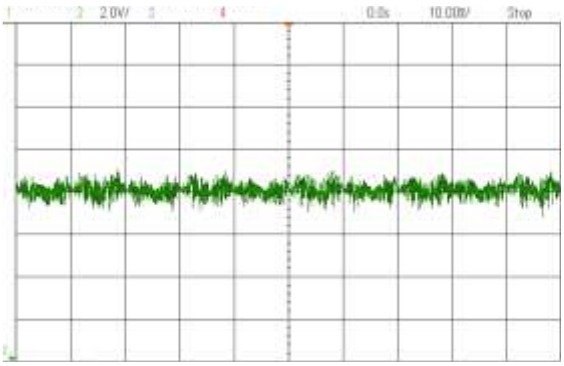
(h) I_o=3.24A, f_s =20 kHz, C_{FC} =200μF



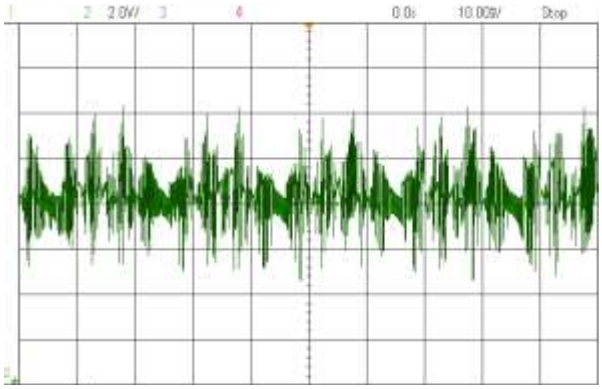
(i) I_o=3.24A, f_s =20 kHz, C_{FC} =50μF



(j) I_o=5.7A, f_s =20 kHz, C_{FC} =300μF



(k) I_o=5.7A, f_s =20 kHz, C_{FC} =200μF



(l) I_o=5.7A, f_s =20 kHz, C_{FC} =50μF

Figure 6.20 Test FC voltage ripples under different conditions

As mentioned in section 6.3, 1/3 of the total dc-link capacitor is set as the reference value for the FC voltage control. As the FC voltage control is of the higher priority than the dc-link NP voltages balancing control, the predefined FC voltage tolerance range has be defined for the purpose that FC voltage regulation control will not always be activated [182]. This method can also be called as the hysteresis band control [182][183] . If there's no such tolerance range, or let's say the criteria is to make FC voltage exactly equals to the idea FC reference voltage point, the FC voltage control will always be activated no matter its voltage higher or lower than this reference point. In this case, as the FC voltage control has the first priority, the system will only implement the FC voltage control. Consequently, there will be no chance for the system to execute the dc-link NPs' voltages balancing control, the voltages on the dc-link capacitors' voltages of the system will eventually drift and become unbalanced. The system becomes unstable. Generally, the FC voltage ripple within some specific range requirement is acceptable, and this predefined tolerance range is chosen by this way in order to further optimize the size of the FC selection according to different requirements, an analytical expression for the FC capacitance should be derived. The FC voltage variation during each switching period is expressed in (6.1). To express the peak voltage ripple on FC, (6.1) can be rewritten as in (6.8).

$$\Delta V_{\mathrm{fc\_p}}=\frac{1}{C_{\mathrm{fc}}}\cdot d_{\mathrm{fc\_p}}\cdot g_{\mathrm{p}}\cdot I_{\mathrm{o}}\cdot T_{\mathrm{s}}$$

$$\Delta V_{\mathrm{fc\_p}}=\frac{k_{\mathrm{p}}}{C_{\mathrm{fc}}}\cdot I_{\mathrm{o}}\cdot T_{\mathrm{s}} \tag{6.8}$$

where I_{o} is the peak load current. $d_{\mathrm{fc\_p}}$ is the proportion of the switching period where the current flowing through the FC causes the maximum FC voltage ripple. g_{p} is the coefficient which represents the corresponding value of the unity load current trigonometric function $\sin(\omega_{\mathrm{o}}t+\varphi)$ when the maximum FC voltage ripple occurs. Among which ω_{o} is the load current fundamental angular speed, and φ is the load power angle. According to the analysis in section 6.5 b) above, maximum FC ripples highlighted by the red arrows in Fig.6.19 are periodically. During these maximum FC ripples, the corresponding instantaneous load current absolute value can be deemed as the same, which means the corresponding value of g_{p} can be deemed as the same as well. Therefore, using $k_{\mathrm{p}}= d_{\mathrm{fc\_p}}* g_{\mathrm{p}}$ to simplify the expression (6.1).

To obtain the value of k_{p}, tests under different FC capacitance values have been carried out. Two

different switching frequencies of 10 kHz and 20 kHz with two different load currents 3.24A, 5.7A (peak value) have been considered. Test results are presented in Table VI.VIII.

TABLE VI.VIII Measured FC voltage ripples data

ΔV_{fc_p}/V		I_o			
		f_s=10 kHz		f_s=20 kHz	
		3.24A	5.7A	3.24A	5.7A
C_{fc}	50μF	2.78	4.76	1.3	2.6
	100μF	1.28	2.32	0.67	1.26
	200μF	0.64	1.16	0.32	0.62
	300μF	0.38	0.78	0.23	0.38
	500μF	0.25	0.46	0.14	0.24

By using the curve fitting technique through Matlab, the FC voltage ripple vs. FC capacitance curve has been plotted in Fig.6.21 by using the measured data in Table VI.VIII. Sequence values of k_p can be derived accordingly as shown in Table VI.IX. Fig. 6.21 presents the peak-to-peak FC voltage ripples percentage vs FC values curves under the different switching frequencies and the different inverter currents. Under the same inverter current, the higher the switching frequency, the lower the FC ripple.

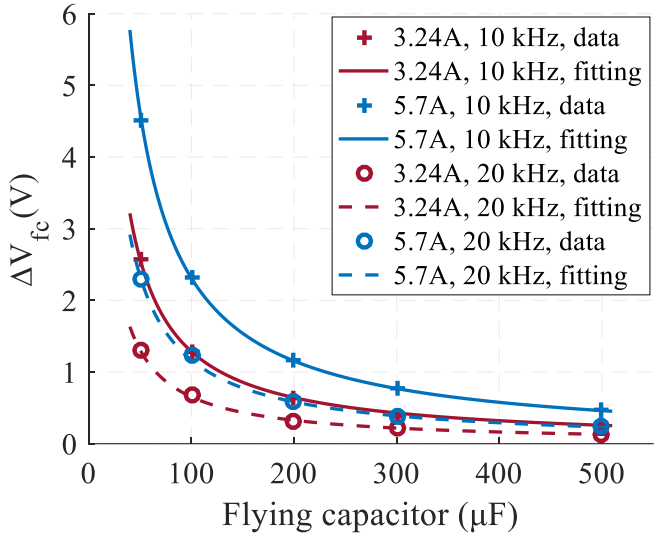


Figure 6.21 Curves of ΔV_{fc_p} vs C_{fc}

TABLE VI.IX SIMULATION AND TEST PARAMETERS

Conditions	k_p
3.24A, 10 kHz	0.398
5.7A, 10 kHz	0.405
3.24A, 20 kHz	0.403
5.7A, 20 kHz	0.409

All four values of k_p derived from tests in Table VI.IX are around 0.4 within a 3% tolerance. Consequently, $k_p = 0.4$ can be used in (6.8) to determine the optimum value of the required capacitance under the single-phase unity power factor operation according to the voltage ripple requirements. This provides a useful guideline for selecting the value and size of the FC for the single-phase hybrid clamped four-level π-type converter.

6.6 Three-phase inverter operation simulation

The operation as well as the control strategy for the single-phase hybrid clamped four-level π-type converter has been investigated and experimental verified. Meanwhile, due to the proposed control strategy for the hybrid-clamped four-level π-type converter is single-phase independent, therefore, the proposed topology can be extended to multi-phase converter with the proposed control scheme. In this section, the three-phase hybrid-clamped four-level π-type inverter system simulation with the proposed FC voltage and dc-link NP voltages balancing control strategy based on the level shifted CB-PWM has been carried out using MATLAB/Simulink with results shown in Fig.6.22 and Fig.6.23. Simulation setup and parameters are summarized in Table VI.X and Table VI.XI, respectively. The simulation model is shown in Appendix D IV.

Zero-order Hold is employed in order to imitate the ADC sampling process of the practical circuit. The Internal resistance Ron is selected as the default value 0.01 in order to make it similar to a practical IGBT. The snubber resistance and capacitance are selected as the default. In practical, both dc-link capacitor and FC will be charged to some level but lower than the desired value before the PWM signals applied on them. Therefore, in the simulation system, initial voltages setting for both dc-link capacitor and FC are 80% of the desired value.

TABLE VI.X THREE-PHASE SYSTEM SIMULATION PARAMETERS

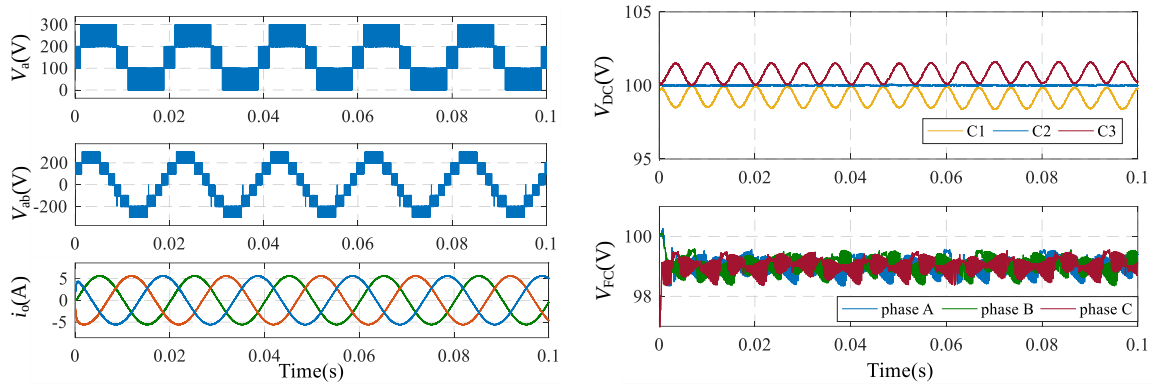
Parameters	Values
Software	Matlab 2017.b
Toolbox	Simulink
Simulation type (Solver)	Discrete
Simulation system sample time	1 μs
Zero-Order Hold sample time	100 μs
IGBT model	IGBT/Diode module
IGBT/Diode module setting	Internal resistance Ron=0.01, Snubber resistance Rs=100000, Snubber capacitance Cs=inf
DC-link cap model	Series RLC Branch (Branch type: C, cap initial voltage 100V)
FC model	Series RLC Branch (Branch type: C, cap initial voltage 80V)

TABLE VI.XI THREE-PHASE SYSTEM SIMULATION PARAMETERS

Parameters	Values
DC-link voltage	V_{dc} = 300 V
DC-link capacitors	C1=C2=C3=2000 μF
FC	C_{fc} = 300 μF
FC voltage deviation	V_{tol} =1V
Carrier frequency	fs = 10 kHz
Fundamental frequency	fo = 50 Hz
Load	R = 25 Ω, L = 5 mH
Modulation index	m = 0.95
Dead-time	t_d = 2 μs

Fig.6.22 (a) shows the three-phase system output phase A phase voltage, phase AB line voltage as well as three-phase output currents with a modulation index 0.95. The phase voltage and line voltage have four voltage levels and seven voltage levels, respectively as expected. The three-phase output currents are sinusoidal. Fig.6.22 (b) upper figure presents three dc-link capacitors voltages waveforms. They are

all controlled at 100V which is 1/3 of the total dc-link voltage. There are voltage ripples at triple the fundamental frequency (150 Hz) on the upper capacitor C3 and the lower capacitor C1 out of phase with each other due to the three-phase system as expected. These voltage ripples can be eliminated by an appropriate zero-sequence components injection. Fig.6.22 (b) bottom figure presents three FC voltage waveforms corresponding to three phase-legs, which are all regulated at 1/3 of the total dc-link voltage. And there is a -1V offset on it as expected.

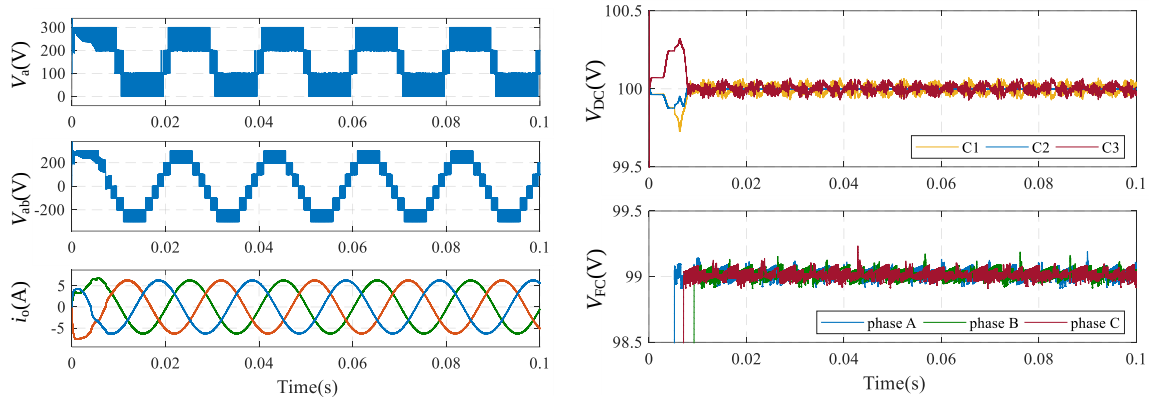


(a) Three-phase system output voltages and currents (b) Three-phase system capacitors voltages

Figure 6.22 Three-phase hybrid clamped four-level π-type converter simulation results

Through the three-phase hybrid clamped four-level π-type converter simulation results presented in Fig.6.22, it verified that the proposed FC voltage and dc-link NP voltages balancing control method can be well operated on the three-phase system. Due to the simulation is based on the pure sinusoidal CB-PWM, there are still low frequency voltage ripples on the dc-link upper and lower capacitors with the frequency equals to 3 times fundamental frequency. These low frequency voltage ripples can be further reduced by the appropriate zero-sequence single injection. At the same time the operation modulation index of the three-phase converter system can be further increased by injecting the zero-sequence single as well. Fig. 6.23 shows operation waveforms of three-phase hybrid clamped four-level π-type converter with the dynamic optimum zero-sequence generation method used in Chapter 5. The simulation parameters are the same as shown in Table VI.X, only changed the modulation index m=1.05. Fig.6.23 (a) presents the phase voltage of phase A, line voltage of phase AB, and three-phase output currents. The system works well, the phase voltage and line voltage have four voltage levels and seven voltage levels, respectively as expected. Three-phase output currents are sinusoidal. Fig.6.23 (b) upper figure presents three dc-link capacitors voltages waveforms. They are also well regulated but with a much less

voltage ripple peak-to-peak 0.1V compares to the voltage ripple 1V shown in Fig.6.22 (a) upper figure. Fig.6.23 (b) bottom figure presents three FC voltage waveforms on three phase-legs, which are also well regulated at 1/3 of the total dc-link voltage.



(a) Three-phase system output voltages and currents (b) Three-phase system capacitors voltages

Figure 6.23 Three-phase hybrid clamped four-level π-type converter simulation results

6.7 Summary of Chapter 6

This chapter investigated the hybrid-clamped four-level π-type converter which is extended based on the original four-level π-type converter investigated in Chapter 3 to 5. With two additional switching devices and one additional FC, this new topology converter is able to operate as a three-phase single-end converter (rectifier or inverter) or even a single-phase converter with dc-link NP voltages balanced at any operation conditions. The worst-case scenario unity power factor with high modulation index condition has been tested with a single-phase hybrid-clamped four-level π-type converter. A 300V dc-link voltage test based on the single phase-leg hybrid clamped four-level π-type converter has verified the proposed hybrid clamped four-level π-type converter topology can operate well with all three dc-link capacitors balanced as well as the FC voltage being controlled at 1/3 the total dc-link voltage (100V) with the proposed control strategy.

Meanwhile, due to the proposed control strategy for the hybrid clamped four-level π-type converter is single-phase independent, the system can be extended to multiple-phase configuration without lose the dc-link NP voltages balancing. A three-phase hybrid-clamped four-level π-type inverter unity power factor operation has been verified by Matlab/Simulink simulation system.

Due to additional FC employed in each phase-leg, the size selection for this FC should be take careful consideration in order to fulfil the system volume requirements for some specific applications such as EV applications. The expression of the relationship between the FC voltage ripple and the FC capacitance under unity power factor condition with sinusoidal modulation has also been obtained according to 300V dc-link voltage single phase-leg experimental results in section 6.5 b). This final expression can be used to optimize the FC size according to the specific power requirement for a single phase-leg operation.

7 Conclusions and future work

7.1 Contributions and conclusions

- **Topology layout configurations and operation output waveforms of the proposed four-level π-type converter have been compared to other popular converters used in low voltage applications. It proved the four-level π-type topology can have less voltage stress on each switching device, less output harmonics, but the converter layout complexity is not significantly increased. It initially verified that compares to the two-level converter, the three-level diode NPC converter and the three-level T-type converter, the proposed topology is qualified to use switching devices with lower voltage rating and lower price, smaller size output filter with the same output harmonics requirements. Which makes it a good candidate for the compact system for low voltage applications.**

  Theoretical analysis has been implemented. With the same dc voltage supply, the four-level π-type converter presents a lower switching voltage on each switching device on the phase-leg compares to the two-level converter, the three-level diode NPC converter and the three-level T-type converter. This feature makes the proposed four-level π-type converter be able to use the switching devices with lower voltage rating and lower price. With respect to the converter configuration complexity, the four-level π-type converter only has two more switching devices compares to the three-level T-type converter but without needs of the clamping diodes. And for a three-phase system, the four-level π-type converter will only require two additional gate driver supplies compares to the two-level converter, and will require even four less gate driver supplies compares to the three-level diode NPC converter. Therefore, the structure complexity of the four-level π-type converter is not an issue. With the Matlab/Simulation model, and by using the same input voltage and power, the numerical comparison among the layout characteristics as well as the open loop operation performance have been implemented. Based on the Matlab/Simulink proves with the traditional level shifted CB-PWM, the four-level π-type converter demonstrates much lower output harmonic contents compares to three-level converters as well as the two-level converter. Harmonic performance has been experimentally verified with the three-phase four-level π-type converter prototype established by IGBT

FGW15N120VD (1200V), IKW30N60H3 (600V) and the three-phase two-level converter prototype based on IGBT FGW15N120VD (1200V). This verified the four-level π-type converter can have the smaller filter size design compares to the other popular converters, which is good for the compact and higher power density applications.

- **Power loss analysis which includes the individual switching device conduction loss and switching loss analysis based on different operation conditions. Based on that, a generalized analytical average power loss model of the four-level π-type converter is established. Based on this proposed model, the converter power loss distribution as well as the system operation efficiency under various modulation indices, power factors and switching frequencies can be mathematically analyzed. Power efficiency calculation as well as the experimental prototype efficiency measurement comparison with the two-level converter are conducted. It proved the four-level π-type converter has much less efficiency drop with the increase of the switching frequency compares to the two-level converter. Calculation and test results also verified the proposed power loss model for the four-level π-type converter is effective and can be used in the estimation of the design in practical.**

  The proposed analytical average power loss analysis provides the analytical average power loss expression as a function of IGBT collector current, power factor angle, input voltage level, modulation index, etc. within the single fundamental period. The analytical power loss investigated in this thesis is based on the pure sinusoidal modulation. If the modulation wave is not sinusoidal such as the modulation waves with the third order harmonics injection, if these modulation waves can be pre-calculated, then they can also be used by changing conduction intervals summarized in TABLE III.I to TABLE III.IV as well as switching intervals summarized in Table III.VII to TABLE III.X. Based on the data from device datasheet, the proposal power loss model is able to provide the quick analysis for the converter system power loss distribution as well as the system efficiency. Through the mathematical analysis based on the proposed power loss model, the four-level π-type converter shows a higher efficiency than two-level and three-level converters at switching frequencies higher than 5 kHz due to the reduced switching loss at high switching frequencies domain. Meanwhile, through the calculation analysis, with same system parameters, switching devices on the four-level π-type

converter are less stressed compare to the other three converter topologies. The experimental case study is based on the 600V dc voltage input, 2.5 kW power level, unity power factor, 0.95 modulation index experimental setup (a sample condition for renewable energy power plant). Experiments are based on the four-level π-type inverter prototype as well as the two-level inverter prototype established with the same IGBTs. Both prototypes operated with the sinusoidal open loop condition in order to get the fair comparison. By comparing calculated efficiencies and measured efficiencies, the experimental results of both the four-level π-type inverter and the two-level inverter match well with their corresponding theoretical calculations. It proved that the proposed average analytical power loss model works well to evaluate the operation efficiency of the four-level π-type converter. And through both the calculation and test results, the power efficiency curve of the four-level π-type converter shows a much more flat tendency with the increase of the switching frequency compares to that of the two-level converter. It verified the lower switching losses of the four-level π-type converter, which makes it a good candidate for the higher power density applications such as renewable energy generation and electric vehicles.

- **DC-link NP voltages balancing control strategy design for the four-level π-type converter in order to make the proposed topology overcome the dc-link NP voltages drift issue ,and ensure the converter is able to operate at stable and reliable conditions. A symmetrical back-to-back four-level π-type converter prototype with the proposed control algorithm has been first implemented under a 300V dc-link input voltage and the unity power factor condition. A controllable region for this back-to-back four-level π-type converter system based on the unity power factor conditions have been first summarized experimentally. It can be used as the design reference in the bidirectional pure active power applications.**

  Implementation of the NP voltage balancing control on the back-to-back configuration of the four-level π-type converter optimum zero-sequence injection based on level shifted CB-PWM based control strategy has been implemented on the three-phase four-level π-type converter to resolve the dc-link NP voltages unbalancing issue during the unity power factor operation. Three groups of experimental operations have been implemented on the three-phase four-level π-type converter prototype to verify the control effect. The first group is based on 50V dc

voltage input, unity output power factor, inverter only system, without dc-link NP voltages balancing control applied. Test results verified, the three-phase four-level π-type converter can not operate with the dc-link NP voltages balanced under the open loop unity power factor condition, regardless the value of the modulation index. The second group is based on 50V dc voltage input, unity output power factor, inverter only system, with the proposed dc-link NP voltages balancing control applied. Test results verified, the proposed control strategy is able to balance the dc-link NP voltages of the three-phase four-level π-type inverter with an upper limit 0.6 for the modulation index under the unity power factor condition. The third group is based on 300V dc voltage input, back-to-back system, grid connects to the rectifier side, RL load connects to the inverter side, unity power factors on both sides, proposed control strategy applied. According to test results, with the same modulation indices on both sides, converter dc-link capacitor voltages balance can be guaranteed on any available value of the modulation indices. However, with the different modulation indices on both side, dc-link NP voltages balancing can not be guaranteed at all modulation indices combinations on both sides. But closer modulation indices on both sides help to balance the voltages as the controllable region for back-to-back four-level π-type converter under unity power factor condition on Fig.5.30. It can be used as the design reference in the bidirectional pure active power applications such as renewable energy boat.

- **Design of the hybrid-clamped four-level π-type converter. This new topology is the one approach to make the original four-level π-type converter be able to operate as a single-end converter (inverter or rectifier) with dc-link capacitors voltages balanced without modulation index and power factor limitation. Converter topology configuration and control have been comprehensively analyzed and experimentally verified.**

  This topology is based on the original four-level π-type converter with two additional switching devices and one additional FC in the phase-leg structure. With the 300V dc voltage input, the unity power factor and the 0.95 modulation index, the single phase-leg hybrid-clamped four-level π-type converter prototype established in section 6.5 works stable with all three dc-link capacitors voltages and FC voltage controlled at 1/3 the total dc-link voltage. Experiments verified the proposed hybrid-clamped four-level π-type converter has the ability to operate as a

single phase-leg with all capacitors voltages balanced with the proposed control and modulation strategy under the worst-case scenario (unity power factor with high modulation index condition). Therefore, this topology can be a potential alternative for the original four-level π-type converter when dc-ac or ac-dc only conversion in high modulation indices applications are required. As the one additional FC employed in each phase-leg, the size selection for this FC should be take careful consideration in order to fulfil the system volume requirements for some specific applications such as EV applications. The expression of the relationship between the FC voltage ripple and the FC capacitance under unity power factor condition with sinusoidal modulation for the singe-leg configuration has been obtained according to the experimental data. The final expression can be used to optimize the FC size according to the required power requirement for the single-phase configuration in order to fulfill the compact size as well as the higher power density requirements for the electrical vehicle applications.

7.2 Future work

- The back-to-back four-level π-type converter with the proposed dc-link NP voltages balancing control method has been successfully verified by experiments with three-phase RL loads. It is interested to verify it with the three-phase motor connected as a load in order to investigate its actual performance as a motor drive. It is also worth to connect motors on both rectifier side as well as the inverter side in order to simulate the generator and motor bi-directional operation, which is a good attempt for the power renewable energy power generation-utilization system. Meanwhile, for the hybrid-clamped four-level π-type converter, it is also worth verifying its performance as an actual motor drive.
- The close loop dc-link NP voltages balancing control method has been verified with the 300V dc-link voltage level. It is worth to investigate the possibility with an increased voltage level such as 600V and even 900V. With the increased voltage level operation, the proposed topology as well as the dc-link NP voltages balancing control method can be adopted as the practical low voltage industrial standard or medium voltage industrial standard.
- It is interested to investigate the new application area for the either the back-to-back four-level π-type converter or the single-end hybrid-clamped four-level π-type converter.

- VV PWM based dc-link NP voltages balancing control strategy is worth to be investigated and applied on the four-level π-type converter in order to make this topology operate as single inverter or rectifier under high power factor and high modulation index condition without the back-to-back configuration or FC. Meanwhile, the operation efficiency is also worth to be investigated.

Appendix

Appendix A. Devices conduction loss and switching loss equation

I. Two-level converter

Conduction loss

$$P_{con,T1} = P_{con,T2} = V_{CE0} \cdot I_{CM} \left(\frac{m \cdot \cos\varphi}{8} + \frac{1}{2\pi} \right) + r_{0T} \cdot I_{CM}^2 \left(\frac{m \cdot \cos\varphi}{3\pi} + \frac{1}{8} \right)$$

$$P_{con,D1} = P_{con,D2} = V_{F0} \cdot I_{CM} \left(-\frac{m \cdot \cos\varphi}{8} + \frac{1}{2\pi} \right) + r_{0D} \cdot I_{CM}^2 \left(-\frac{m \cdot \cos\varphi}{3\pi} + \frac{1}{8} \right)$$

Switching loss

$$P_{sw,T1} = P_{sw,T2} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left(\frac{A_{0T}}{2} + \frac{B_{0T}}{\pi} \cdot I_{CM} + \frac{C_{0T}}{4} \cdot I_{CM}^2 \right)$$

$$P_{rev,D1} = P_{rev,D2} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left(\frac{A_{0D}}{2} + \frac{B_{0D}}{\pi} \cdot I_{CM} + \frac{C_{0D}}{4} \cdot I_{CM}^2 \right)$$

II. Three-level NPC converter

Conduction loss

$$P_{con,T1} = P_{con,T4} = V_{CE0} \cdot I_{CM} \cdot m \left(\frac{\cos\varphi}{4} + \frac{\sin\varphi}{4\pi} - \frac{\varphi \cdot \cos\varphi}{4\pi} \right) + r_{0T} \cdot I_{CM}^2 \cdot m \left(\frac{\cos^2\varphi}{6\pi} + \frac{\cos\varphi}{3\pi} + \frac{1}{6\pi} \right)$$

$$P_{con,T2} = P_{con,T3} = V_{CE0} \cdot I_{CM} \left(\frac{1}{\pi} - \frac{m \cdot \sin\varphi}{4\pi} + \frac{m \cdot \varphi \cdot \cos\varphi}{4\pi} \right) + r_{0T} \cdot I_{CM}^2 \left(-\frac{m \cdot \cos^2\varphi}{6\pi} + \frac{m \cdot \cos\varphi}{3\pi} - \frac{m}{6\pi} + \frac{1}{4} \right)$$

$$P_{con,D1} = P_{con,D2} = P_{con,D3} = P_{con,D4} = V_{F0} \cdot I_{CM} \cdot m \left(\frac{\sin\varphi}{4\pi} - \frac{\varphi \cdot \cos\varphi}{4\pi} \right) + r_{0D} \cdot I_{CM}^2 \cdot m \left(\frac{\cos^2\varphi}{6\pi} - \frac{\cos\varphi}{3\pi} + \frac{1}{6\pi} \right)$$

$$P_{con,D5} = P_{con,D6} = V_{F0} \cdot I_{CM} \left(\frac{1}{\pi} - \frac{m \cdot \cos\varphi}{4} - \frac{m \cdot \sin\varphi}{2\pi} + \frac{m \cdot \varphi \cdot \cos\varphi}{2\pi} \right) + r_{0D} \cdot I_{CM}^2 \left(-\frac{m \cdot \cos^2\varphi}{3\pi} - \frac{m}{3\pi} + \frac{1}{4} \right)$$

Switching loss

$$P_{sw,T1}=P_{sw,T4}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0T}(\frac{1}{2}-\frac{\varphi}{2\pi})+\frac{B_{0T}}{2\pi}\cdot I_{CM}(1+\cos\varphi)+C_{0T}\cdot I_{CM}^2(\frac{1}{4}-\frac{\varphi}{4\pi}+\frac{\cos\varphi\cdot\sin\varphi}{4\pi})\right]$$

$$P_{sw,T2}=P_{sw,T3}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0T}\cdot\frac{\varphi}{2\pi}+\frac{B_{0T}}{2\pi}\cdot I_{CM}(1-\cos\varphi)+\frac{C_{0T}}{4\pi}\cdot I_{CM}^2(\varphi-\cos\varphi\cdot\sin\varphi)\right]$$

$$P_{rev,D1}=P_{rev,D4}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0D}\cdot\frac{\varphi}{2\pi}+\frac{B_{0D}}{2\pi}\cdot I_{CM}(1-\cos\varphi)+\frac{C_{0D}}{4\pi}\cdot I_{CM}^2(\varphi-\cos\varphi\cdot\sin\varphi)\right]$$

$$P_{rev,D2}=P_{rev,D3}=0$$

$$P_{rev,D5}=P_{rev,D6}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0D}(\frac{1}{2}-\frac{\varphi}{2\pi})+\frac{B_{0D}}{2\pi}\cdot I_{CM}(1+\cos\varphi)+C_{0D}\cdot I_{CM}^2(\frac{1}{4}-\frac{\varphi}{4\pi}+\frac{\cos\varphi\cdot\sin\varphi}{4\pi})\right]$$

III. Three-level T-type converter

Conduction loss

$$P_{con,T2}=P_{con,T3}=V_{CE0}\cdot I_{CM}\left(\frac{1}{\pi}-\frac{m\cdot\cos\varphi}{4}-\frac{m\cdot\sin\varphi}{2\pi}+\frac{m\cdot\varphi\cdot\cos\varphi}{2\pi}\right)+r_{0T}\cdot I_{CM}^2\left(-\frac{m\cdot\cos^2\varphi}{3\pi}-\frac{m}{3\pi}+\frac{1}{4}\right)$$

$$P_{con,D1}=P_{con,D4}=V_{F0}\cdot I_{CM}\cdot m\left(\frac{\sin\varphi}{4\pi}-\frac{\varphi\cdot\cos\varphi}{4\pi}\right)+r_{0D}\cdot I_{CM}^2\cdot m\left(\frac{\cos^2\varphi}{6\pi}-\frac{\cos\varphi}{3\pi}+\frac{1}{6\pi}\right)$$

$$P_{con,D2}=P_{con,D3}=V_{F0}\cdot I_{CM}\left(\frac{1}{\pi}-\frac{m\cdot\cos\varphi}{4}-\frac{m\cdot\sin\varphi}{2\pi}+\frac{m\cdot\varphi\cdot\cos\varphi}{2\pi}\right)+r_{0D}\cdot I_{CM}^2\left(-\frac{m\cdot\cos^2\varphi}{3\pi}-\frac{m}{3\pi}+\frac{1}{4}\right)$$

Switching loss

$$P_{sw,T1}=P_{sw,T4}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0T}(\frac{1}{2}-\frac{\varphi}{2\pi})+\frac{B_{0T}}{2\pi}\cdot I_{CM}(1+\cos\varphi)+C_{0T}\cdot I_{CM}^2(\frac{1}{4}-\frac{\varphi}{4\pi}+\frac{\cos\varphi\cdot\sin\varphi}{4\pi})\right]$$

$$P_{sw,T2}=P_{sw,T3}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0T}\cdot\frac{\varphi}{2\pi}+\frac{B_{0T}}{2\pi}\cdot I_{CM}(1-\cos\varphi)+\frac{C_{0T}}{4\pi}\cdot I_{CM}^2(\varphi-\cos\varphi\cdot\sin\varphi)\right]$$

$$P_{rev,D1}=P_{rev,D4}=f_c\cdot\frac{V_c}{V_{base}}\cdot\left[A_{0D}\cdot\frac{\varphi}{2\pi}+\frac{B_{0D}}{2\pi}\cdot I_{CM}(1-\cos\varphi)+\frac{C_{0D}}{4\pi}\cdot I_{CM}^2(\varphi-\cos\varphi\cdot\sin\varphi)\right]$$

$$P_{rev,D2} = P_{rev,D3} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left[A_{0D}(\frac{1}{2} - \frac{\varphi}{2\pi}) + \frac{B_{0D}}{2\pi} \cdot I_{CM}(1+\cos\varphi) + C_{0D} \cdot I_{CM}^2(\frac{1}{4} - \frac{\varphi}{4\pi} + \frac{\cos\varphi \cdot \sin\varphi}{4\pi}) \right]$$

IV. Four-level π-type converter

a) $m \le \frac{1}{3}$

Conduction loss

$$P_{con,T1} = P_{con,T6} = 0$$

$$P_{con,T2} = P_{con,T5} = V_{CE0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{3m \cdot \cos\varphi}{8} \right) + r_{0T} \cdot I_{CM}^2 \left(\frac{1}{8} - \frac{m \cdot \cos\varphi}{\pi} \right)$$

$$P_{con,T3} = P_{con,T4} = V_{CE0} \cdot I_{CM} \left(\frac{1}{2\pi} + \frac{3m \cdot \cos\varphi}{8} \right) + r_{0T} \cdot I_{CM}^2 \left(\frac{1}{8} + \frac{m \cdot \cos\varphi}{\pi} \right)$$

$$P_{con,D1} = P_{con,D6} = 0$$

$$P_{con,D2} = P_{con,D5} = V_{F0} \cdot I_{CM} \left(\frac{1}{2\pi} + \frac{3m \cdot \cos\varphi}{8} \right) + r_{0D} \cdot I_{CM}^2 \left(\frac{1}{8} + \frac{m \cdot \cos\varphi}{\pi} \right)$$

$$P_{con,D3} = P_{con,D4} = V_{F0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{3m \cdot \cos\varphi}{8} \right) + r_{0D} \cdot I_{CM}^2 \left(\frac{1}{8} - \frac{m \cdot \cos\varphi}{\pi} \right)$$

Switching loss

$$P_{sw,T1} = P_{sw,T6} = 0$$

$$P_{sw,T2} = P_{sw,T5} = 0$$

$$P_{sw,T3} = P_{sw,T4} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left(\frac{A_{0T}}{2} + \frac{B_{0T}}{\pi} \cdot I_{CM} + \frac{C_{0T}}{4} \cdot I_{CM}^2 \right)$$

$$P_{rev,D1} = P_{rev,D6} = 0$$

$$P_{rev,D2} = P_{rev,D5} = 0$$

$$P_{rev,D3} = P_{rev,D4} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left(\frac{A_{0D}}{2} + \frac{B_{0D}}{\pi} \cdot I_{CM} + \frac{C_{0D}}{4} \cdot I_{CM}^2 \right)$$

b) $m > \frac{1}{3}, \sin^{-1}\frac{1}{3m} \geq \varphi$

Conduction loss

$$P_{con,T1} = P_{con,T6} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{3m \cdot \cos\varphi}{8} - \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0T} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} - \frac{1}{8} \right)$$

$$P_{con,T2} = P_{con,T5} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0T} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{m \cdot \cos\varphi}{\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} \right)$$

$$P_{con,T3} = P_{con,T4} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{3m \cdot \cos\varphi}{8} + \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{2\pi} \right)$$

$$+ r_{0T} \cdot I_{CM}^2 \left(-\frac{\arcsin(\frac{1}{3m})}{2\pi} + \frac{m \cdot \cos\varphi}{\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{9\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{\pi} + \frac{3}{8} \right)$$

$$P_{con,D1} = P_{con,D6} = 0$$

$$P_{con,D2} = P_{con,D5} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{3m \cdot \cos\varphi}{8} + \frac{\cos\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{2\pi} + \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{2\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(- \frac{\arcsin(\frac{1}{3m})}{2\pi} + \frac{m \cdot \cos\varphi}{\pi} - \frac{m\sqrt{1 - \frac{1}{9m^2}}}{\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{18\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{9\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{\pi} + \frac{3}{8} \right)$$

$$P_{con,D3} = P_{con,D4} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{4\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{m \cdot \cos\varphi}{\pi} + \frac{m\sqrt{1 - \frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1 - \frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{2\pi} \right)$$

Switching loss

$$P_{sw,T1} = P_{sw,T6} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left[A_{0T} \left(\frac{1}{2} - \frac{\arcsin(\frac{1}{3m})}{\pi} \right) + B_{0T} \cdot I_{CM} \cdot \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{\pi} \right.$$

$$\left. + C_{0T} \cdot I_{CM}^2 \left(\frac{1}{4} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \right]$$

$$P_{sw,T2} = P_{sw,T5} = 0$$

$$P_{sw,T3} = P_{sw,T4} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0T} \cdot \dfrac{\arcsin(\dfrac{1}{3m})}{\pi} + B_{0T} \cdot I_{CM} \left(\dfrac{1}{\pi} - \dfrac{\cos\varphi \sqrt{1-\dfrac{1}{9m^2}}}{\pi} \right) \\ + C_{0T} \cdot I_{CM}^2 \left(\dfrac{\arcsin(\dfrac{1}{3m})}{2\pi} + \dfrac{\sqrt{1-\dfrac{1}{9m^2}}}{6\pi \cdot m} + \dfrac{\cos^2\varphi \cdot \sqrt{1-\dfrac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

$$P_{rev,D1} = P_{rev,D6} = 0$$

$$P_{rev,D2} = P_{rev,D5} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \left(\dfrac{1}{2} - \dfrac{\arcsin(\dfrac{1}{3m})}{\pi} \right) + B_{0D} \cdot I_{CM} \cdot \dfrac{\cos\varphi \sqrt{1-\dfrac{1}{9m^2}}}{\pi} \\ + C_{0D} \cdot I_{CM}^2 \left(\dfrac{1}{4} - \dfrac{\arcsin(\dfrac{1}{3m})}{2\pi} - \dfrac{\sqrt{1-\dfrac{1}{9m^2}}}{6\pi \cdot m} + \dfrac{\cos^2\varphi \cdot \sqrt{1-\dfrac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

$$P_{rev,D3} = P_{rev,D4} = f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \cdot \dfrac{\arcsin(\dfrac{1}{3m})}{\pi} + B_{0D} \cdot I_{CM} \left(\dfrac{1}{\pi} - \dfrac{\cos\varphi \sqrt{1-\dfrac{1}{9m^2}}}{\pi} \right) \\ + C_{0D} \cdot I_{CM}^2 \left(\dfrac{\arcsin(\dfrac{1}{3m})}{2\pi} + \dfrac{\sqrt{1-\dfrac{1}{9m^2}}}{6\pi \cdot m} + \dfrac{\cos^2\varphi \cdot \sqrt{1-\dfrac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

c) $m > \frac{1}{3}, \sin^{-1}\frac{1}{3m} < \varphi < \pi - \sin^{-1}\frac{1}{3m}$

Conduction loss

$$P_{con,T1} = P_{con,T6} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{3m \cdot \cos\varphi}{8} - \frac{1}{4\pi} + \frac{3m \cdot \sin\varphi}{8\pi} + \frac{\sin\varphi}{24\pi \cdot m} - \frac{\cos\varphi\sqrt{1-\frac{1}{9m^2}}}{8\pi} - \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+r_{0T} \cdot I_{CM}^2 \left(\frac{\varphi}{8\pi} + \frac{\arcsin(\frac{1}{3m})}{8\pi} + \frac{m \cdot \cos\varphi}{2\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} - \frac{\cos\varphi \cdot \sin\varphi}{8\pi} \right.$$
$$\left. - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} + \frac{\cos\varphi \cdot \sin\varphi}{108\pi \cdot m^2} - \frac{1}{8} \right)$$

$$P_{con,T2} = P_{con,T5} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{3}{4\pi} - \frac{3m \cdot \sin\varphi}{8\pi} - \frac{\sin\varphi}{24\pi \cdot m} - \frac{3\cos\varphi\sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} - \frac{9m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+r_{0T} \cdot I_{CM}^2 \left(\frac{3\varphi}{8\pi} - \frac{\arcsin(\frac{1}{3m})}{8\pi} + \frac{m \cdot \cos\varphi}{2\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} - \frac{3\cos\varphi \cdot \sin\varphi}{8\pi} \right.$$
$$\left. + \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{\cos\varphi \cdot \sin\varphi}{36\pi \cdot m^2} \right)$$

$$P_{con,T3} = P_{con,T4} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{3}{4\pi} - \frac{3m \cdot \cos\varphi}{8} - \frac{3m \cdot \cos\varphi}{8\pi} - \frac{\sin\varphi}{24\pi \cdot m} + \frac{3\cos\varphi\sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} + \frac{9m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+r_{0T} \cdot I_{CM}^2 \left(-\frac{3\varphi}{8\pi} - \frac{\arcsin(\frac{1}{3m})}{8\pi} - \frac{m \cdot \cos\varphi}{2\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} + \frac{3\cos\varphi \cdot \sin\varphi}{8\pi} \right.$$
$$\left. + \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\cos\varphi \cdot \sin\varphi}{36\pi \cdot m^2} + \frac{3}{8} \right)$$

$$P_{con,D1} = P_{con,D6} =$$

$$V_{F0} \cdot I_{CM} \left(-\frac{1}{4\pi} + \frac{3m \cdot \sin\varphi}{8\pi} + \frac{\sin\varphi}{24\pi \cdot m} + \frac{\cos\varphi \sqrt{1-\frac{1}{9m^2}}}{8\pi} - \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} + \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\begin{array}{l} -\frac{\varphi}{8\pi} + \frac{\arcsin(\frac{1}{3m})}{8\pi} - \frac{m \cdot \cos\varphi}{2\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} + \frac{\cos\varphi \cdot \sin\varphi}{8\pi} \\ -\frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\cos\varphi \cdot \sin\varphi}{108\pi \cdot m^2} \end{array} \right)$$

$$P_{con,D2} = P_{con,D5} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{3}{4\pi} - \frac{3m \cdot \cos\varphi}{8} - \frac{3m \cdot \cos\varphi}{8\pi} - \frac{\sin\varphi}{24\pi \cdot m} + \frac{3\cos\varphi \sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} + \frac{9m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\begin{array}{l} -\frac{3\varphi}{8\pi} - \frac{\arcsin(\frac{1}{3m})}{8\pi} - \frac{m \cdot \cos\varphi}{2\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} + \frac{3\cos\varphi \cdot \sin\varphi}{8\pi} \\ +\frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\cos\varphi \cdot \sin\varphi}{36\pi \cdot m^2} + \frac{3}{8} \end{array} \right)$$

$$P_{con,D3} = P_{con,D4} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{3}{4\pi} - \frac{3m \cdot \sin\varphi}{8\pi} - \frac{\sin\varphi}{24\pi \cdot m} - \frac{3\cos\varphi \sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{3m \cdot \varphi \cdot \cos\varphi}{8\pi} - \frac{9m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{8\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\begin{array}{l} \frac{3\varphi}{8\pi} - \frac{\arcsin(\frac{1}{3m})}{8\pi} + \frac{m \cdot \cos\varphi}{2\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{72\pi \cdot m} - \frac{3\cos\varphi \cdot \sin\varphi}{8\pi} \\ +\frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{8\pi} + \frac{\cos\varphi \cdot \sin\varphi}{36\pi \cdot m^2} \end{array} \right)$$

Switching loss

$$P_{sw,T1} = P_{sw,T6} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0T} \left(\frac{1}{2} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\varphi}{2\pi} \right) + B_{0T} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\sin\varphi}{6\pi \cdot m} + \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{2\pi} \right) \\ + C_{0T} \cdot I_{CM}^2 \left(\frac{1}{4} - \frac{\varphi}{4\pi} - \frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{12\pi \cdot m} + \frac{\cos\varphi \sin\varphi}{4\pi} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} - \frac{\cos\varphi \sin\varphi}{18\pi \cdot m^2} \right) \end{array} \right]$$

$$P_{sw,T2} = P_{sw,T5} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0T} \left(\frac{\varphi}{2\pi} - \frac{\arcsin(\frac{1}{3m})}{2\pi} \right) + B_{0T} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\sin\varphi}{6\pi \cdot m} - \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{2\pi} \right) \\ + C_{0T} \cdot I_{CM}^2 \left(\frac{\varphi}{4\pi} - \frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{12\pi \cdot m} - \frac{\cos\varphi \sin\varphi}{4\pi} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\cos\varphi \sin\varphi}{18\pi \cdot m^2} \right) \end{array} \right]$$

$$P_{sw,T3} = P_{sw,T4} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0T} \cdot \frac{\arcsin(\frac{1}{3m})}{\pi} + B_{0T} \cdot I_{CM} \cdot \frac{\sin\varphi}{3\pi \cdot m} \\ + C_{0T} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\sin^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

$$P_{rev,D1} = P_{rev,D6} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \left(\frac{\varphi}{2\pi} - \frac{\arcsin(\frac{1}{3m})}{2\pi} \right) + B_{0D} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\sin\varphi}{6\pi \cdot m} - \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{2\pi} \right) \\ + C_{0D} \cdot I_{CM}^2 \left(\frac{\varphi}{4\pi} - \frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{12\pi \cdot m} - \frac{\cos\varphi \sin\varphi}{4\pi} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\cos\varphi \sin\varphi}{18\pi \cdot m^2} \right) \end{array} \right]$$

$$P_{rev,D2} = P_{rev,D5} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \left(\frac{1}{2} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\varphi}{2\pi} \right) + B_{0D} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\sin\varphi}{6\pi \cdot m} + \frac{\cos\varphi \sqrt{1-\frac{1}{9m^2}}}{2\pi} \right) \\ + C_{0D} \cdot I_{CM}^2 \left(\frac{1}{4} - \frac{\varphi}{4\pi} - \frac{\arcsin(\frac{1}{3m})}{4\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{12\pi \cdot m} + \frac{\cos\varphi \sin\varphi}{4\pi} + \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{6\pi \cdot m} - \frac{\cos\varphi \sin\varphi}{18\pi \cdot m^2} \right) \end{array} \right]$$

$$P_{rev,D3} = P_{rev,D4} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \cdot \frac{\arcsin(\frac{1}{3m})}{\pi} + B_{0D} \cdot I_{CM} \cdot \frac{\sin\varphi}{3\pi \cdot m} \\ + C_{0D} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{6\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

d) $m > \frac{1}{3}, \pi - \sin^{-1}\frac{1}{3m} \le \varphi < \pi$

Conduction loss

$$P_{con,T1} = P_{con,T6} = 0$$

$$P_{con,T2} = P_{con,T5} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{3m \cdot \cos\varphi}{8} + \frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{2\pi} \right)$$

$$+ r_{0T} \cdot I_{CM}^2 \left(\frac{3}{8} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{m \cdot \cos\varphi}{\pi} - \frac{m\sqrt{1-\frac{1}{9m^2}}}{\pi} - \frac{\sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{9\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{\pi} \right)$$

$$P_{con,T3} = P_{con,T4} =$$

$$V_{CE0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0T} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} + \frac{m \cdot \cos\varphi}{\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} \right)$$

$$P_{con,D1} = P_{con,D6} =$$

$$V_{F0} \cdot I_{CM} \left(-\frac{3m \cdot \cos\varphi}{8} + \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} + \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} - \frac{1}{8} \right)$$

$$P_{con,D2} = P_{con,D5} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{4\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{4\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{4\pi} + \frac{m \cdot \cos\varphi}{\pi} + \frac{m\sqrt{1-\frac{1}{9m^2}}}{2\pi} + \frac{\sqrt{1-\frac{1}{9m^2}}}{36\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{18\pi \cdot m} + \frac{m \cdot \cos^2\varphi \cdot \sqrt{1-\frac{1}{9m^2}}}{2\pi} \right)$$

$$P_{con,D3} = P_{con,D4} =$$

$$V_{F0} \cdot I_{CM} \left(\frac{3m \cdot \cos\varphi}{8} + \frac{1}{2\pi} - \frac{\cos\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{2\pi} - \frac{3m \cdot \arcsin(\frac{1}{3m}) \cdot \cos\varphi}{2\pi} \right)$$

$$+ r_{0D} \cdot I_{CM}^2 \left(\frac{3}{8} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{m \cdot \cos\varphi}{\pi} - \frac{m\sqrt{1 - \frac{1}{9m^2}}}{\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{18\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{9\pi \cdot m} - \frac{m \cdot \cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{\pi} \right)$$

Switching loss

$$P_{sw,T1} = P_{sw,T6} = 0$$

$$P_{sw,T2} = P_{sw,T5} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[A_{0T} \left(\frac{1}{2} - \frac{\arcsin(\frac{1}{3m})}{\pi} \right) - B_{0T} \cdot I_{CM} \cdot \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{\pi} + C_{0T} \cdot I_{CM}^2 \left(\frac{1}{4} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \right]$$

$$P_{sw,T3} = P_{sw,T4} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[A_{0T} \cdot \frac{\arcsin(\frac{1}{3m})}{\pi} + B_{0T} \cdot I_{CM} \left(\frac{1}{\pi} + \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{\pi} \right) + C_{0T} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{2\pi} + \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \right]$$

$$P_{rev,D1} = P_{rev,D6} =$$

$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \left(\frac{1}{2} - \frac{\arcsin(\frac{1}{3m})}{\pi} \right) - B_{0D} \cdot I_{CM} \cdot \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{\pi} \\ + C_{0D} \cdot I_{CM}^2 \left(\frac{1}{4} - \frac{\arcsin(\frac{1}{3m})}{2\pi} - \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} + \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

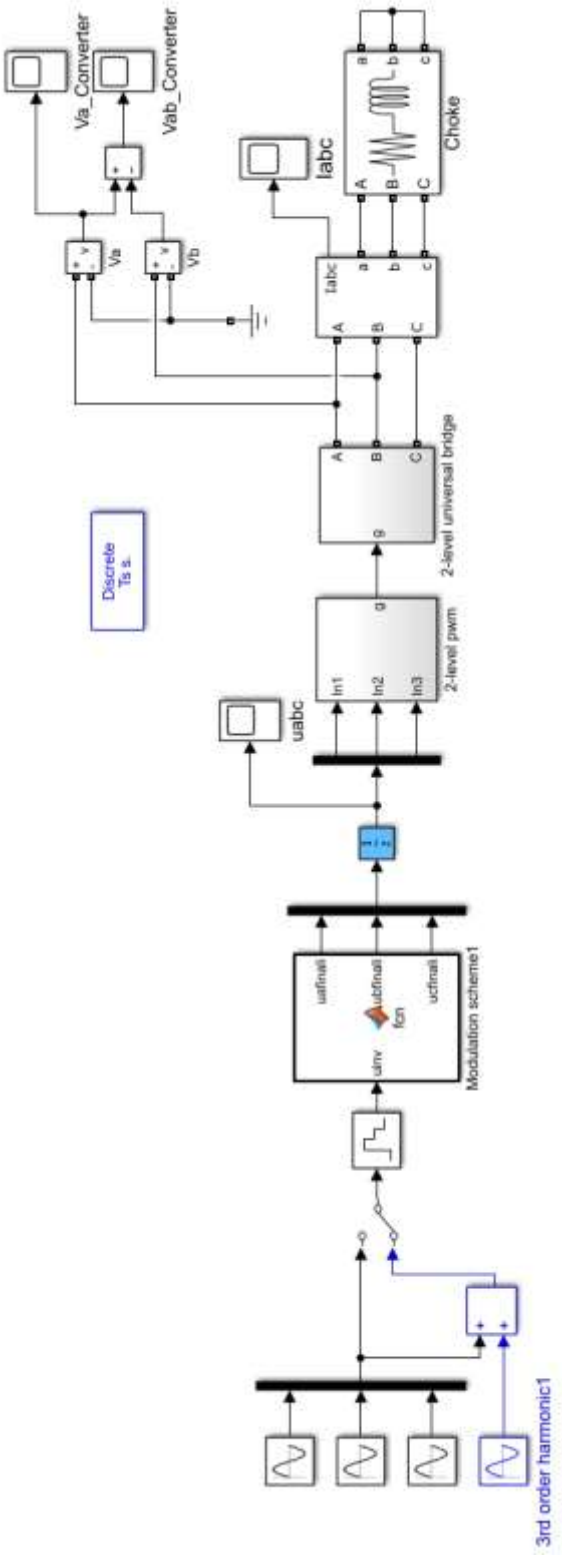
$$P_{rev,D2} = P_{rev,D5} = 0$$

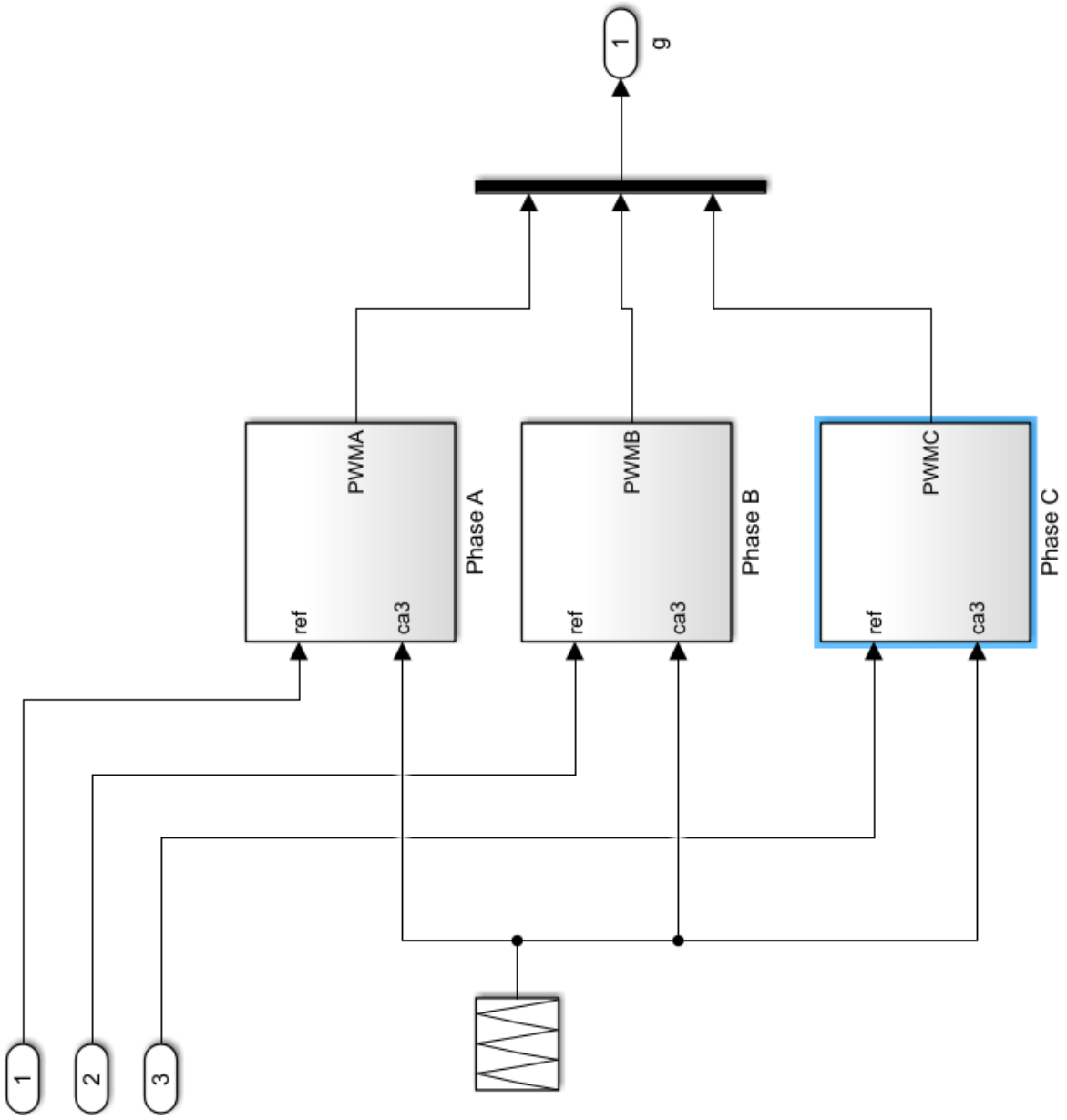
$$P_{rev,D3} = P_{rev,D4} =$$

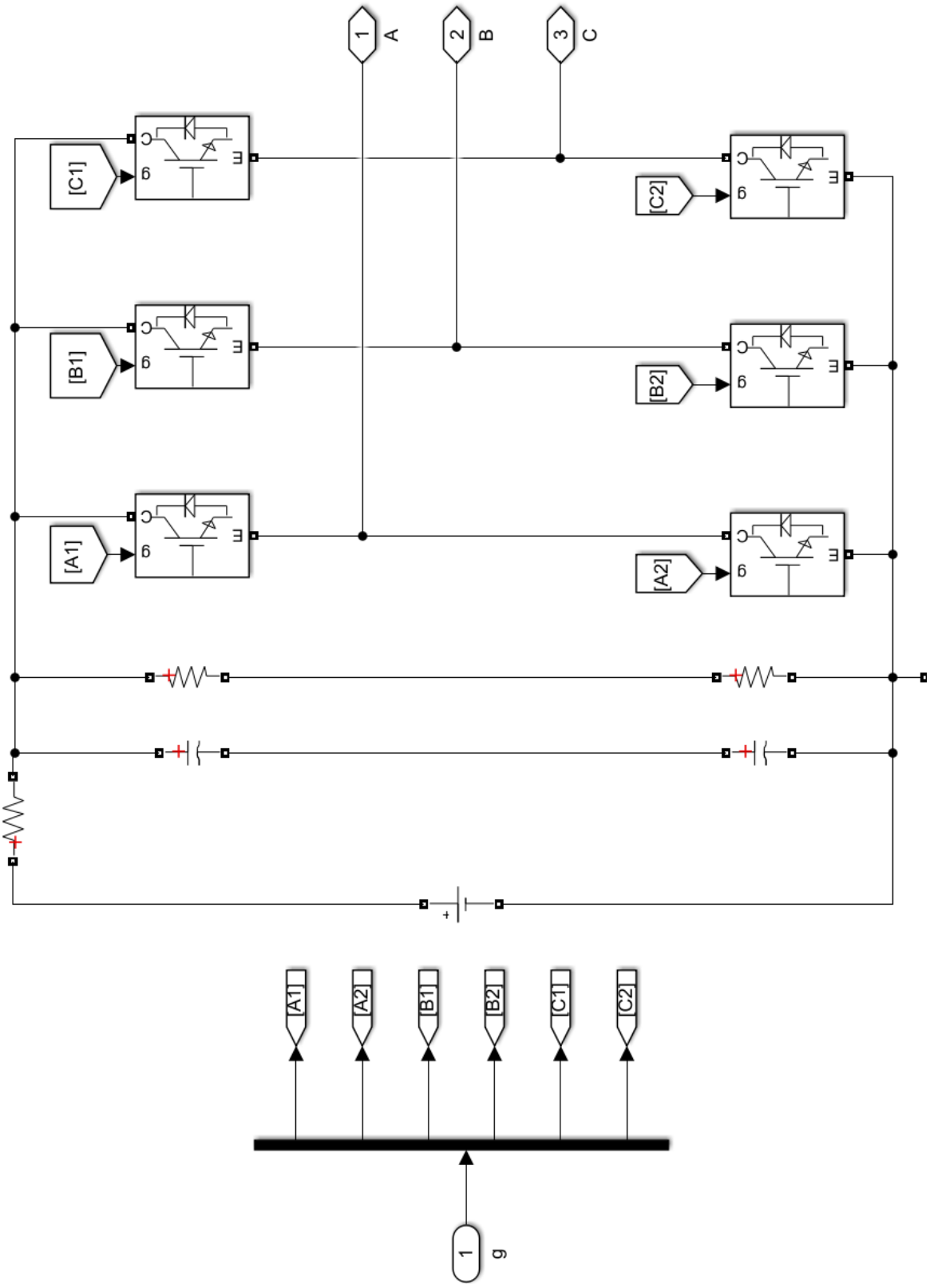
$$f_c \cdot \frac{V_c}{V_{base}} \cdot \left[\begin{array}{l} A_{0D} \cdot \frac{\arcsin(\frac{1}{3m})}{\pi} + B_{0D} \cdot I_{CM} \left(\frac{1}{\pi} + \frac{\cos\varphi \sqrt{1 - \frac{1}{9m^2}}}{\pi} \right) \\ + C_{0D} \cdot I_{CM}^2 \left(\frac{\arcsin(\frac{1}{3m})}{2\pi} + \frac{\sqrt{1 - \frac{1}{9m^2}}}{6\pi \cdot m} - \frac{\cos^2\varphi \cdot \sqrt{1 - \frac{1}{9m^2}}}{3\pi \cdot m} \right) \end{array} \right]$$

Appendix B. MATLAB/Simulink Simulation layout for converter topologies operational verification.

I. Three-phase two-level converter

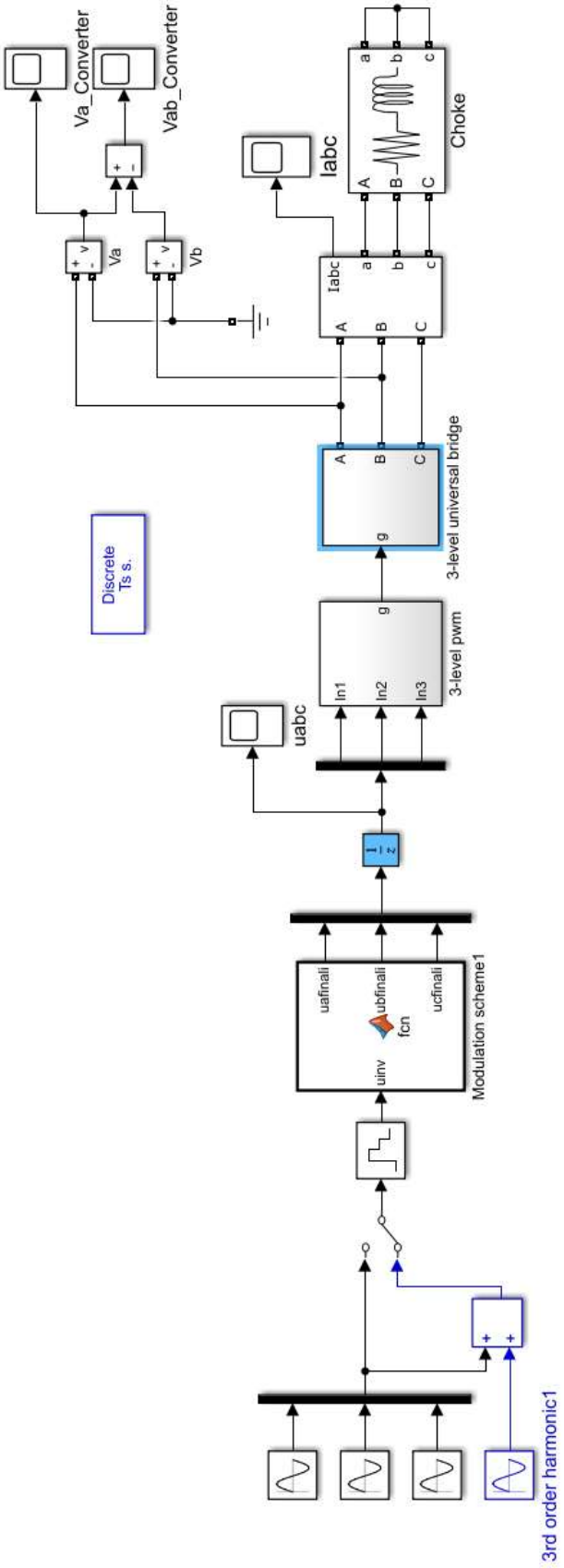


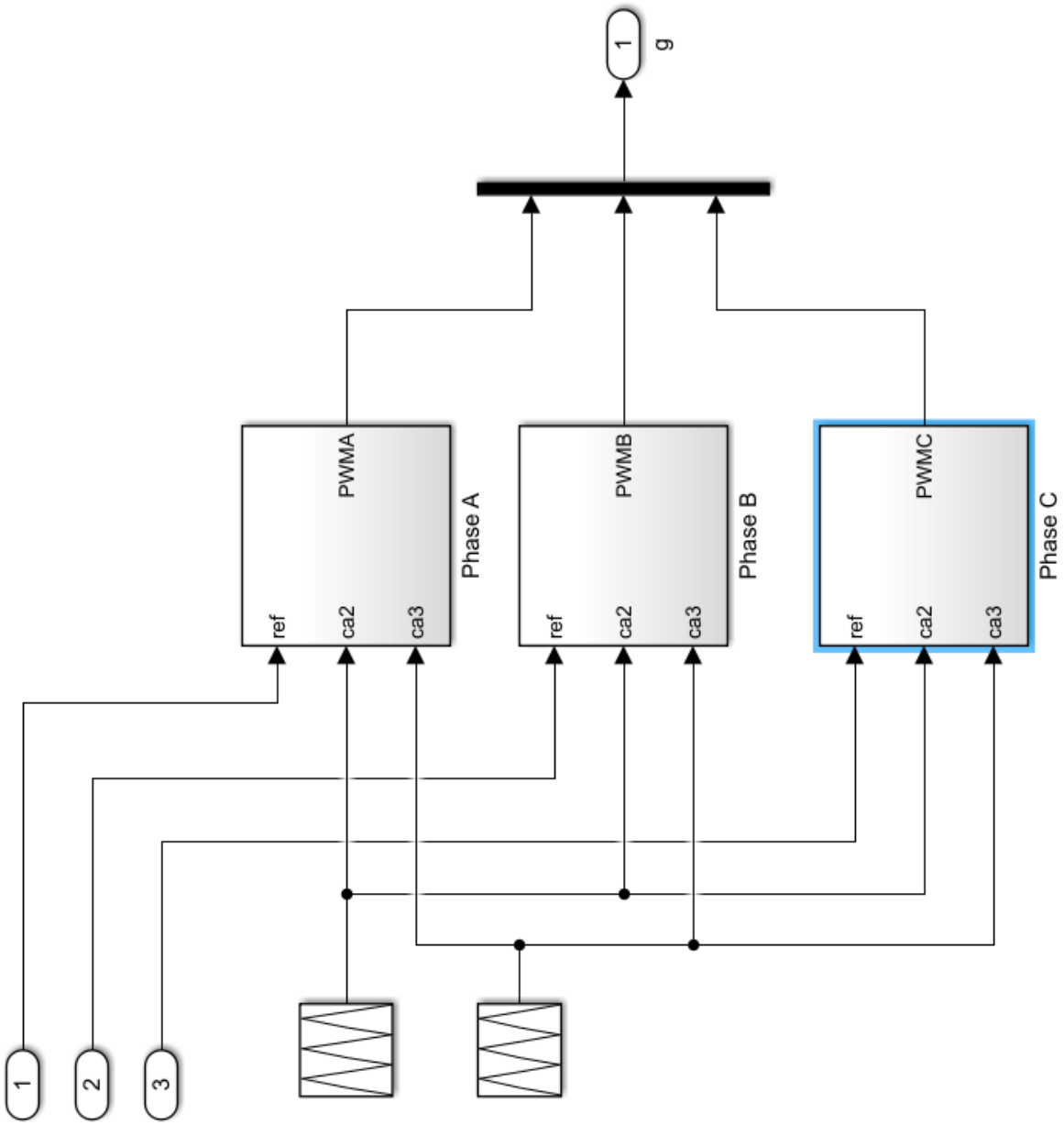

1
g
PWMA
Phase A
ref
ca3
PWMB
Phase B
ref
ca3
PWMC
Phase C
ref
ca3
1
2
3

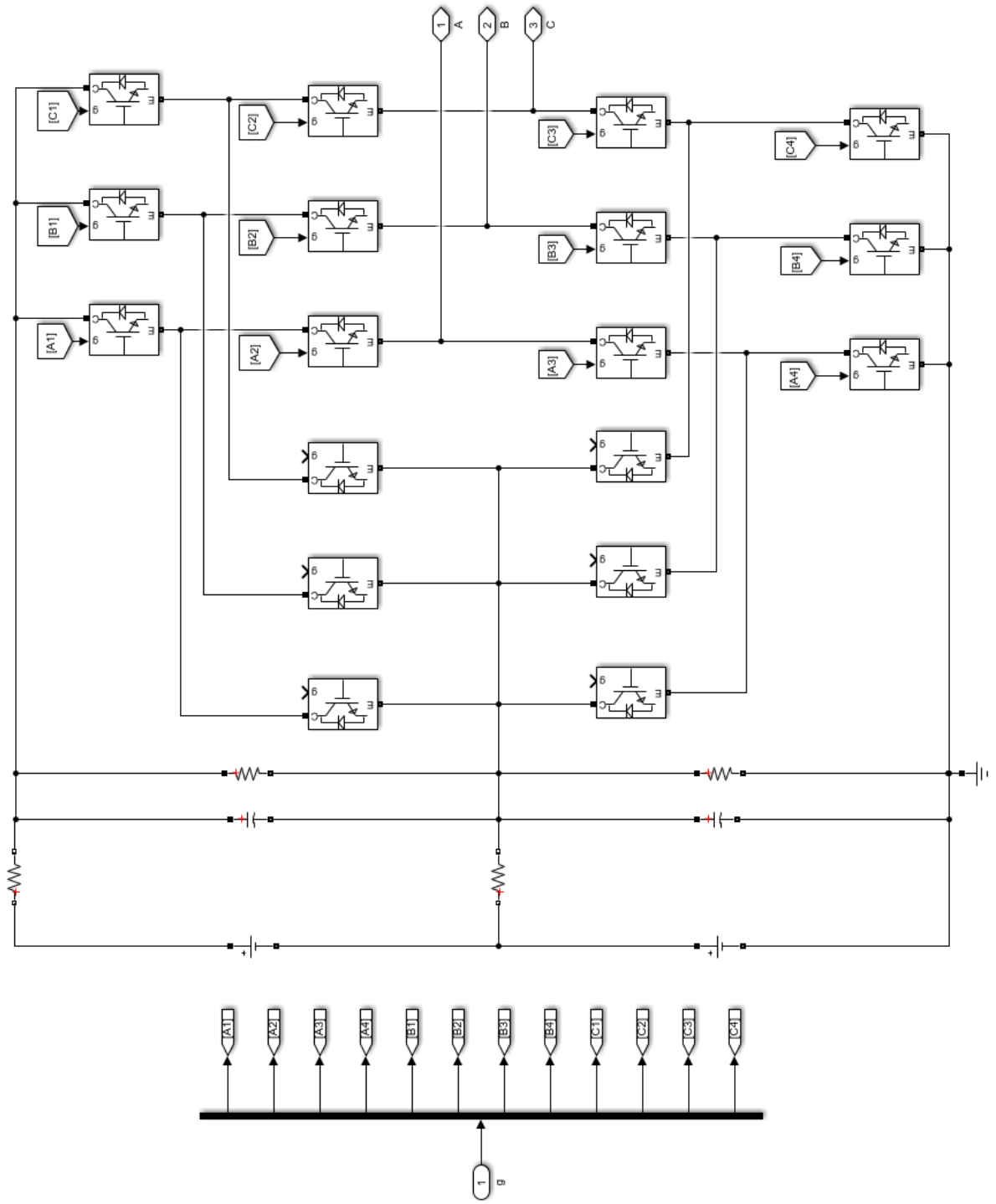

1
A
2
B
3
C
[C1]
[C2]
[B1]
[B2]
[A1]
[A2]
К
Б
Э
+
[A1]
[A2]
[B1]
[B2]
[C1]
[C2]
1
g

```
1    function [uafinali,ubfinali,ucfinali] = fcn(uinv)
2
3
4    uai=uinv(1);    ubi=uinv(2);uci=uinv(3);
5
6
7    uafinali=0.5*uai+0.5;
8    ubfinali=0.5*ubi+0.5;
9    ucfinali=0.5*uci+0.5;
```

II. Three-phase three-level NPC converter

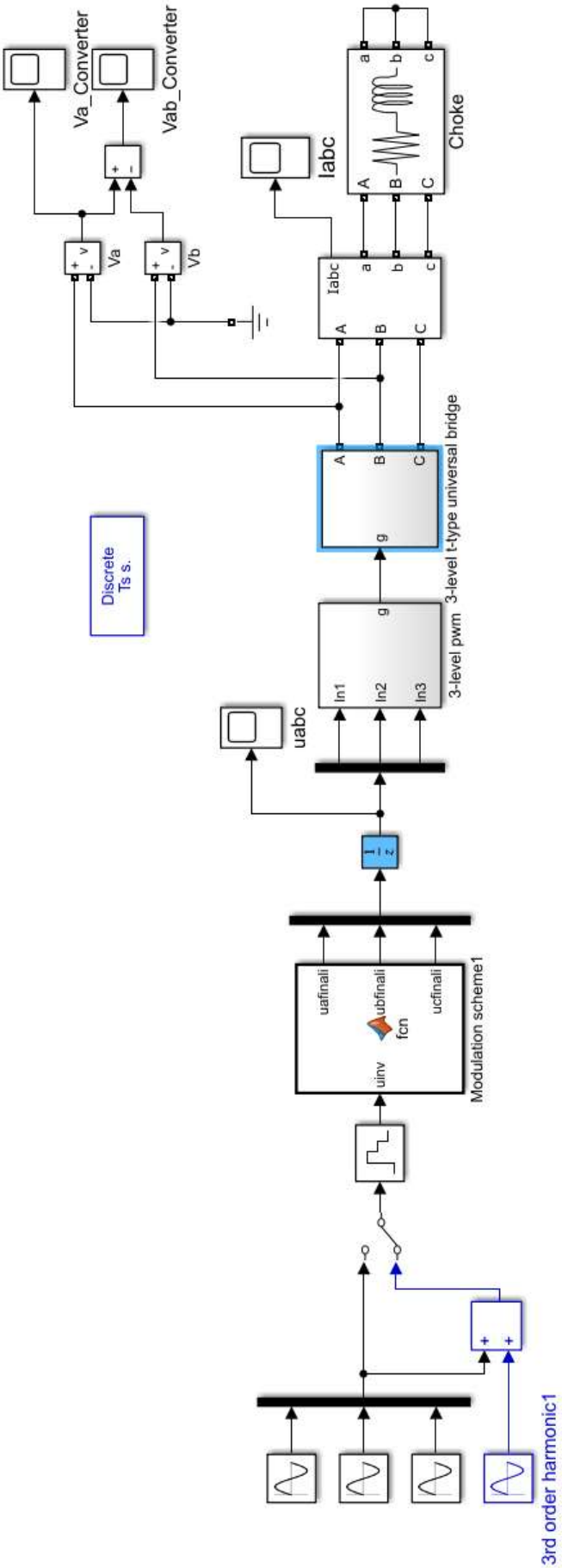


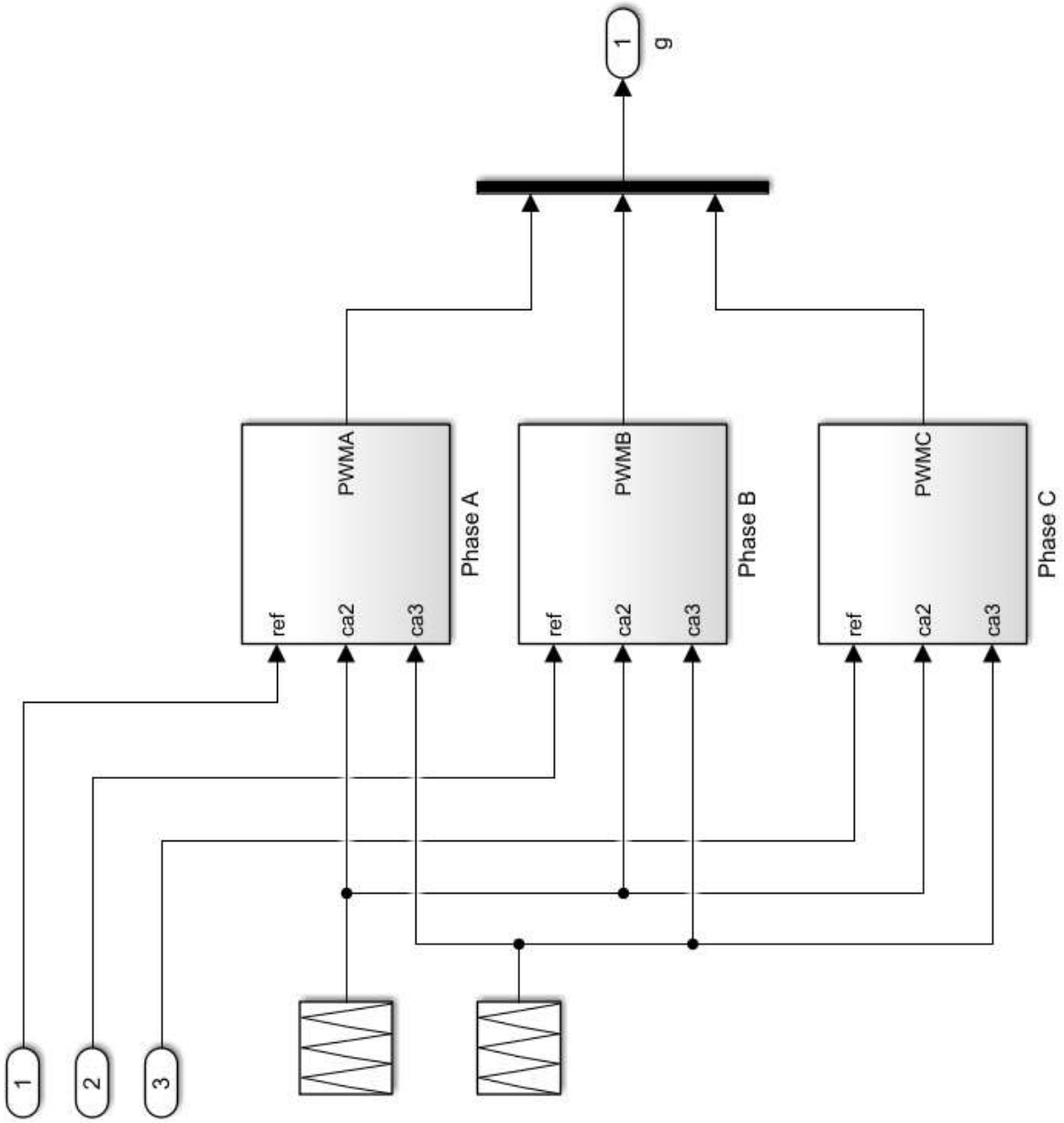

1
g
PWMA
ref
ca2
ca3
Phase A
PWMB
ref
ca2
ca3
Phase B
PWMC
ref
ca2
ca3
Phase C
1
2
3

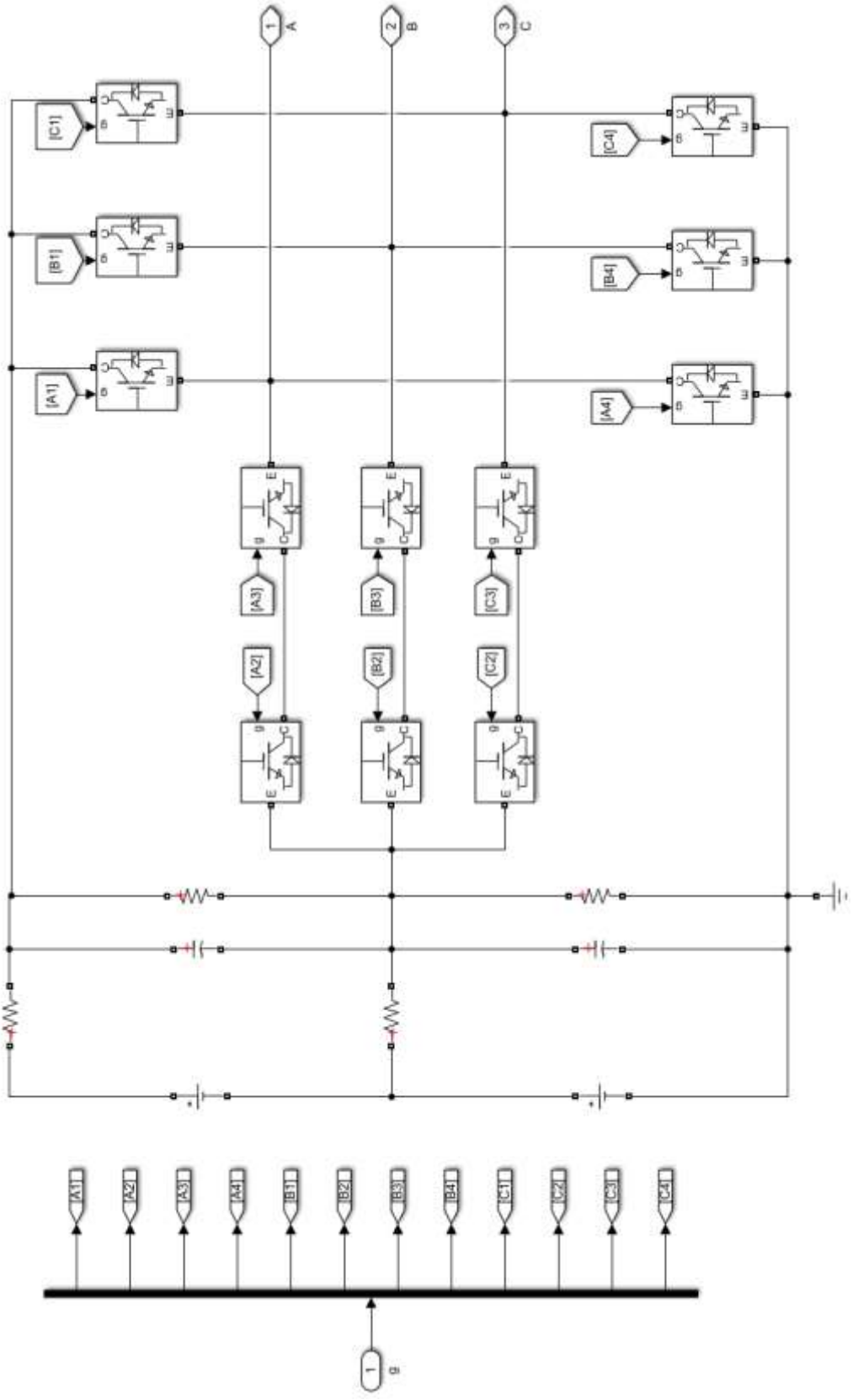

1
A
2
B
3
C
[C1]
[C2]
[C3]
[C4]
[B1]
[B2]
[B3]
[B4]
[A1]
[A2]
[A3]
[A4]
[A1]
[A2]
[A3]
[A4]
[B1]
[B2]
[B3]
[B4]
[C1]
[C2]
[C3]
[C4]
1
g

```
1     function [uafinali,ubfinali,ucfinali] = fcn(uinv)
2
3
4 -   uai=uinv(1);    ubi=uinv(2);uci=uinv(3);
5
6
7 -   uafinali=uai+1;
8 -   ubfinali=ubi+1;    %offset from (-1.5 to 1.5) to (0 to 3)
9 -   ucfinali=uci+1;
```

III. Three-phase three-level T-type converter

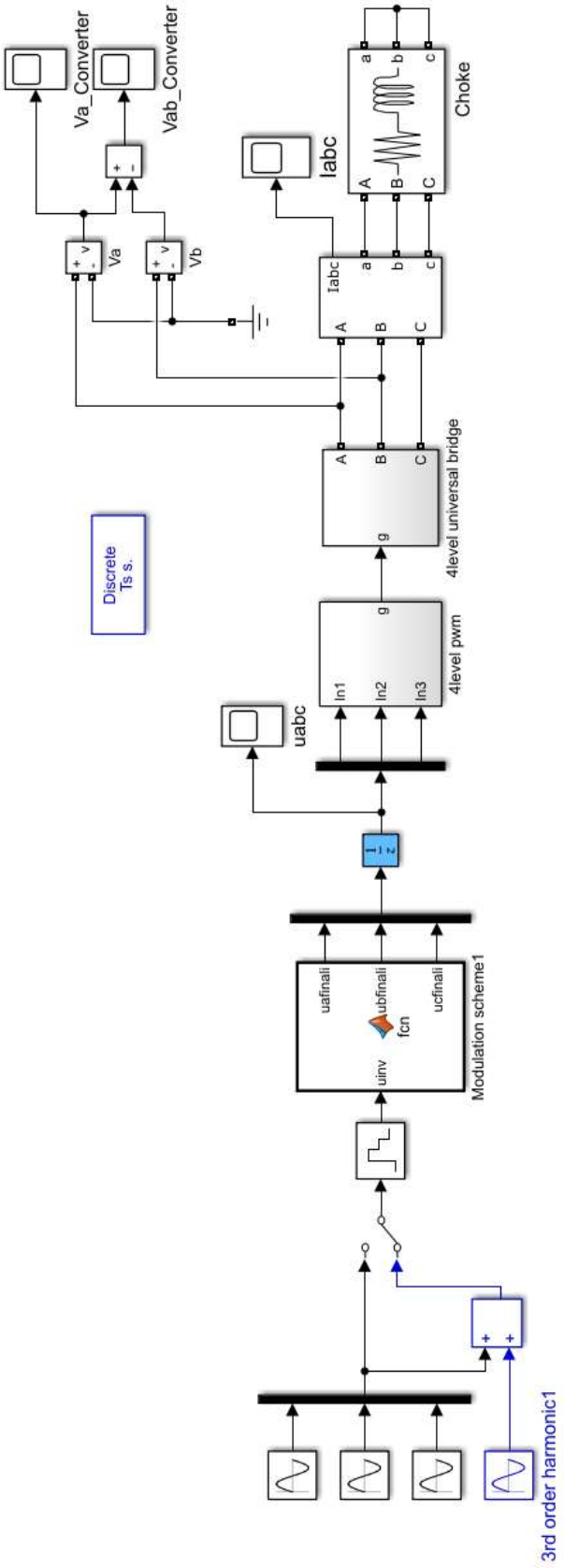

Va_Converter
Vab_Converter
Va
Vb
Iabc
Choke
Discrete
Ts s.
3-level t-type universal bridge
3-level pwm
uabc
uafinali
ubfinali
ucfinali
fcn
uinv
Modulation scheme1
3rd order harmonic1

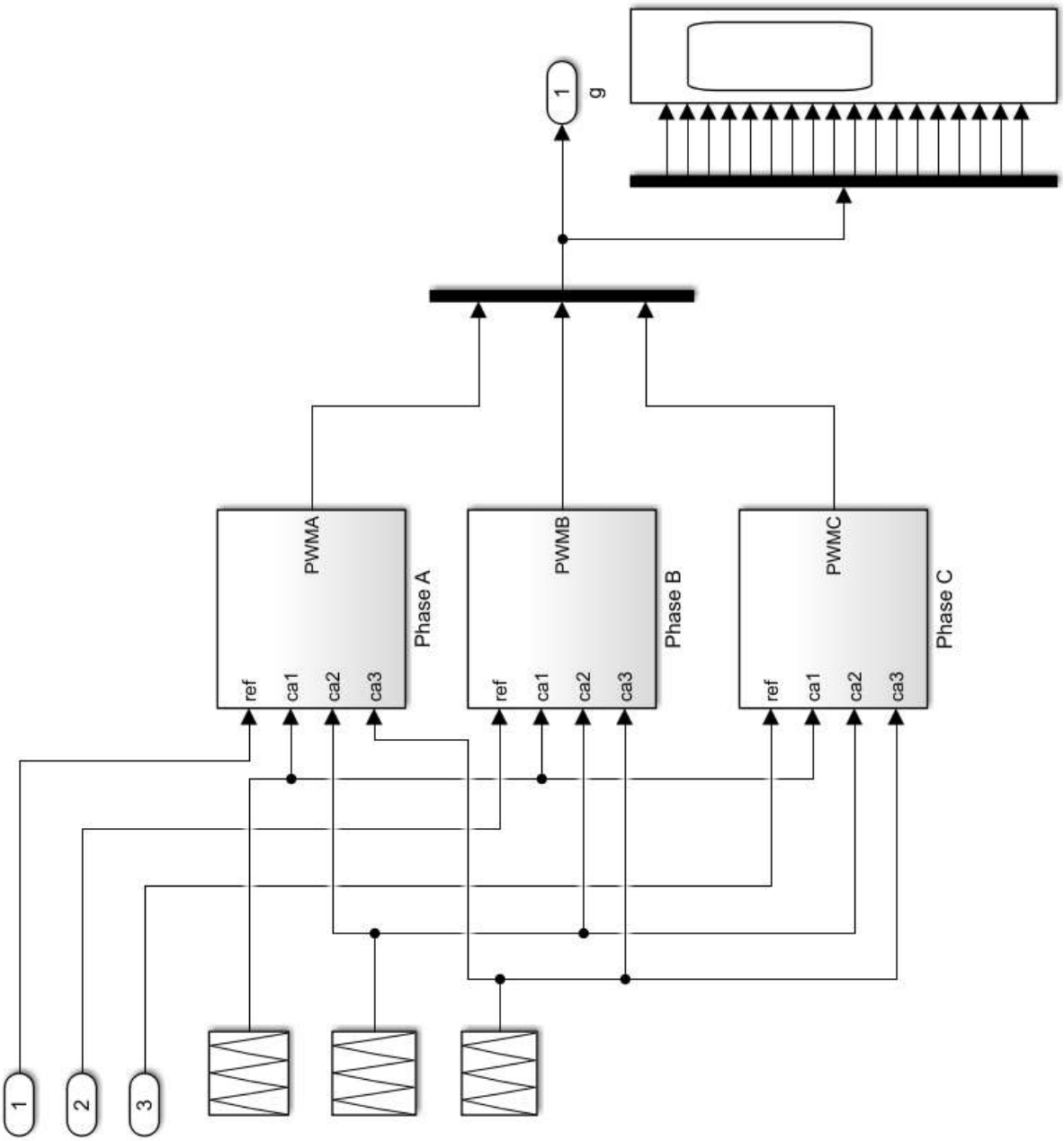

1
g
PWMA
Phase A
ref
ca2
ca3
PWMB
Phase B
ref
ca2
ca3
PWMC
Phase C
ref
ca2
ca3
1
2
3

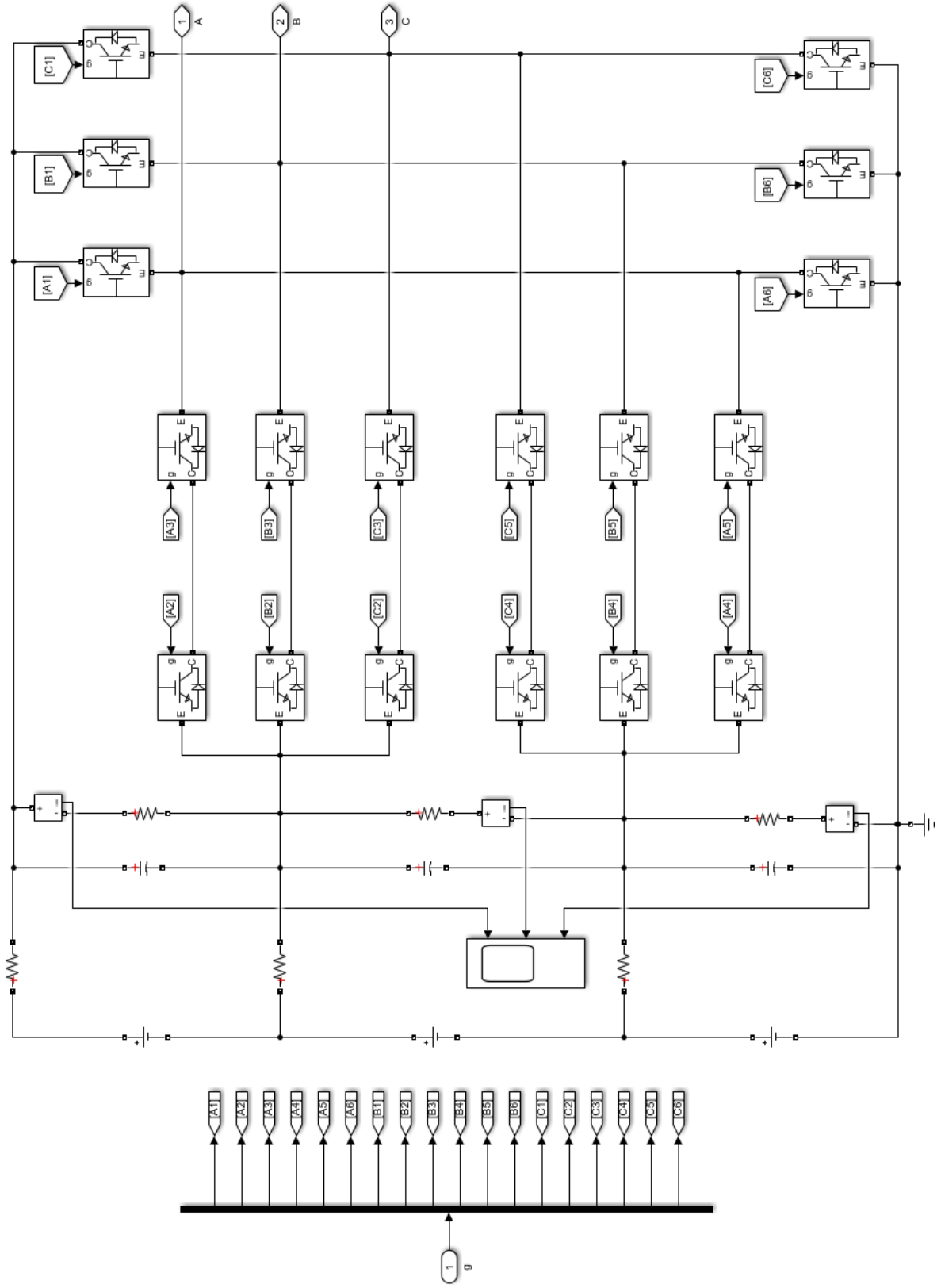

1
A
2
B
3
C
[C1]
[B1]
[A1]
[C4]
[B4]
[A4]
[A3]
[B3]
[C3]
[A2]
[B2]
[C2]
[A1]
[A2]
[A3]
[A4]
[B1]
[B2]
[B3]
[B4]
[C1]
[C2]
[C3]
[C4]
g

```
1     function [uafinali,ubfinali,ucfinali] = fcn(uinv)
2
3
4 -   uai=uinv(1);    ubi=uinv(2);uci=uinv(3);
5
6
7 -   uafinali=uai+1;
8 -   ubfinali=ubi+1;    %offset from (-1.5 to 1.5) to (0 to 3)
9 -   ucfinali=uci+1;
```

IV. Three-phase four-level π-type converter




1
g
PWMA
Phase A
ref
ca1
ca2
ca3
PWMB
Phase B
ref
ca1
ca2
ca3
PWMC
Phase C
ref
ca1
ca2
ca3
1
2
3


1
A
2
B
3
C
[C1]
[B1]
[A1]
[C6]
[B6]
[A6]
[A3]
[B3]
[C3]
[C5]
[B5]
[A5]
[A2]
[B2]
[C2]
[C4]
[B4]
[A4]
[A1]
[A2]
[A3]
[A4]
[A5]
[A6]
[B1]
[B2]
[B3]
[B4]
[B5]
[B6]
[C1]
[C2]
[C3]
[C4]
[C5]
[C6]
1
g

```
1     function [uafinali,ubfinali,ucfinali] = fcn(uinv)
2
3
4 -   uai=uinv(1);   ubi=uinv(2);uci=uinv(3);
5
6
7 -   uafinali=1.5*uai+1.5;
8 -   ubfinali=1.5*ubi+1.5;   %offset from (-1.5 to 1.5) to (0 to 3)
9 -   ucfinali=1.5*uci+1.5;
```

Appendix C. Power loss analysis calculation through MATLAB/Simulink Simulation

I. Power loss distribution of the four-level π-type converter

```
%% IGBT loss with sinusodial modulaton %%
clear all

%   600V IGBT & diode characteristics
UT0=1.17;        % IGBT initial voltage drop 600V
rfT=(4-1.17)/67.5;  % Slope of IGBT V/I curve  600V

UD0=1.02;         % Diode initial voltage drop 600Vvc
rfD=(2.85-1.02)/50;    %12e-3;       % Slope of diode V/I curve 600V

ATon= -3.26e-5;    % curve fitting coefficient turn-on loss
BTon= 2.61e-5;;   % curve fitting coefficient turn-on loss
CTon= 5.36e-7;   % curve fitting coefficient turn-on loss

AToff= -0.708e-5;    % curve fitting coefficient turn-off loss
BToff= 1.84e-5;    % curve fitting coefficient turn-off loss
CToff= 7.63e-8;    % curve fitting coefficient turn-off loss

ADrev= 4.2e-4; % curve fitting diode reverse recovery loss
BDrev= 7.88e-5; % curve fitting diode reverse recovery loss
CDrev= -1.04e-7;% curve fitting diode reverse recovery loss

%   1200V IGBT and diode characteristics
VCEN=3; % rated IGBT voltage drop
VCE0=1; % IGBT threshold voltage
ICN=21.25;    % rated IGBT collector current 300A

VFN=2;  % rated diode voltage drop
VF0=0.9;%1.05;  % diode forward threshold voltage
ICNF=19; % rated Diode current
ri=(VCEN-VCE0)/ICN;
rd=0.057;%(VFN-VF0)/ICNF;

AoTon=2.15e-4;
BoTon=2.6e-5;
CoTon=3.5e-6;

AoToff=0.4e-4;
BoToff=1.007e-4;
CoToff=-1e-6;

AoD=8.00e-4;
BoD=6.8e-5;
CoD=-8.627e-7;

ICM=15; Amplitude of the phase current
VCC1=600;% Dc-link voltage  maybe should choose 1200V
VCC2=400;
Vdc1=600; % real dc-link voltage
Vdc3=(Vdc1)/3;
```

```
m=0.95;   % The modulation index
fc=10e3;    % carrier frequency
y=pi;  % Power factor  0 inverter operation pi rectifier operation
fs=fc;

Pt1_pi=0;
Pt2_pi_1=0;
Pt2_pi_2=0;
Pt3_pi=0;
Pd1_pi=0;
Pd2_pi=0;
Pd3_pi_1=0;
Pd3_pi_2=0;
Pont1_pi=0;
Pont2_pi=0;
Pont3_pi=0;
Pofft1_pi=0;
Pofft2_pi=0;
Pofft3_pi=0;
Prrd1_pi=0;
Prrd2_pi=0;
Prrd3_pi_1=0;
Prrd3_pi_2=0;

Pt1_pi_large=0;
Pt2_pi_large_1=0;
Pt2_pi_large_2=0;
Pt2_pi_large_3=0;
Pt3_pi_large_1=0;
Pt3_pi_large_2=0;
Pt3_pi_large_3=0;
Pd1_pi_large=0;
Pd2_pi_large_1=0;
Pd2_pi_large_2=0;
Pd2_pi_large_3=0;
Pd3_pi_large_1=0;
Pd3_pi_large_2=0;
Pd3_pi_large_3=0;
Pont1_pi_large=0;
Pofft1_pi_large=0;
Pont2_pi_large=0;
Pofft2_pi_large=0;
Pont3_pi_large_1=0;
Pofft3_pi_large_1=0;
Pont3_pi_large_2=0;
Pofft3_pi_large_2=0;
Prrd1_pi_large=0;
Prrd2_pi_large=0;
Prrd3_pi_large_1=0;
Prrd3_pi_large_2=0;
```

```
Prrd3_pi_large_3=0;

Pt1_pi_small=0;
Pt2_pi_small_1=0;
Pt2_pi_small_2=0;
Pt2_pi_small_3=0;
Pt3_pi_small_1=0;
Pt3_pi_small_2=0;
Pd1_pi_small=0;
Pd2_pi_small_1=0;
Pd2_pi_small_2=0;
Pd3_pi_small_1=0;
Pd3_pi_small_2=0;
Pd3_pi_small_3=0;
Pont1_pi_small=0;
Pofft1_pi_small=0;
Pont2_pi_small=0;
Pofft2_pi_small=0;
Pont3_pi_small=0;
Pofft3_pi_small=0;
Prrd1_pi_small=0;
Prrd2_pi_small=0;
Prrd3_pi_small_1=0;
Prrd3_pi_small_2=0;

Pt1_pi_below=0;
Pt2_pi_below_1=0;
Pt2_pi_below_2=0;
Pt2_pi_below_3=0;
Pt2_pi_below_4=0;
Pt3_pi_below_1=0;
Pt3_pi_below_2=0;
Pd1_pi_below=0;
Pd2_pi_below_1=0;
Pd2_pi_below_2=0;
Pd3_pi_below_1=0;
Pd3_pi_below_2=0;
Pd3_pi_below_3=0;
Pd3_pi_below_4=0;
Pont1_pi_below=0;
Pofft1_pi_below=0;
Pont2_pi_below=0;
Pofft2_pi_below=0;
Pont3_pi_below_1=0;
Pofft3_pi_below_1=0;
Pont3_pi_below_2=0;
Pofft3_pi_below_2=0;
Prrd1_pi_below=0;
Prrd2_pi_below=0;
Prrd3_pi_below_1=0;
```

```
Prrd3_pi_below_2=0;
Prrd3_pi_below_3=0;

for x=0:asin(1/(3*m))/100:asin(1/(3*m))
    Pt2_pi_small_1=Pt2_pi_small_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_1=Pd3_pi_small_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_1=Prrd3_pi_small_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_1=Pt2_pi_below_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_1=Pd3_pi_below_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_1=Prrd3_pi_below_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);
%      plot(x,(1/2)+(3/2)*m*sin(x),'o')
%      hold on
end

for x=asin(1/(3*m)):(y-asin(1/(3*m)))/100:y
    Pt2_pi_small_2=Pt2_pi_small_2+((y-asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_small=Pd1_pi_small+((y-asin(1/(3*m)))/100)*(VF0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_2=Pd3_pi_small_2+((y-asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_small=Pont2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft2_pi_small=Pofft2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_small=Prrd1_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))+CoD*
(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(3/2)-(3/2)*m*sin(x),'o',x,(-1/2)+(3/2)*m*sin(x),'+')
%     hold on
end

for x=0:y/100:y
    Pt2_pi_1=Pt2_pi_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs(1/2+(3/2)*m*sin(x))/
(2*pi);
    Pd3_pi_1=Pd3_pi_1+(y/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Prrd3_pi_1=Prrd3_pi_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/
(2*pi);
    Pt2_pi_large_1=Pt2_pi_large_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Pd3_pi_large_1=Pd3_pi_large_1+(y/100)*(UD0-rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Prrd3_pi_large_1=Prrd3_pi_large_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*
```

```
(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on

end

for x=y:(asin(1/(3*m))-y)/100:asin(1/(3*m))
    Pt3_pi_large_1=Pt3_pi_large_1+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_1=Pd2_pi_large_1+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_large_1=Pont3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_1=Pofft3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on

end

for x=y:(pi-asin(1/(3*m))-y)/100:pi-asin(1/(3*m))
    Pt1_pi_small=Pt1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_small_1=Pt3_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_1=Pd2_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_small=Pont1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_small=Pofft1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_small=Prrd2_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(3/2)-(3/2)*m*sin(x),'o',x,(-1/2)+(3/2)*m*sin(x),'+')
%     hold on
end

for x=asin(1/(3*m)):(pi-2*asin(1/(3*m)))/100:pi-asin(1/(3*m))
    Pt1_pi_large=Pt1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_large_2=Pt3_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_2=Pd2_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_large=Pont1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_large=Pofft1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
```

```
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_large=Prrd2_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_2=Pt2_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_below=Pd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*(VP0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_2=Pd3_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_below=Pont2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft2_pi_below=Pofft2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_below=Prrd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))
+CoD*(ICM*sin(x-y))^2)/(2*pi);
%     plot(x,(3/2)-(3/2)*m*sin(x),'o',x,abs((-1/2)+(3/2)*m*sin(x)),'+')
%     hold on
end

for x=pi-asin(1/(3*m)):(y-pi+asin(1/(3*m)))/100:y
    Pt2_pi_below_3=Pt2_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_3=Pd3_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_2=Prrd3_pi_below_2+((y-pi+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on

end

for x=pi-asin(1/(3*m)):2*asin(1/(3*m))/100:pi+asin(1/(3*m))
    Pt3_pi_small_2=Pt3_pi_small_2+(2*asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_2=Pd2_pi_small_2+(2*asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_small=Pont3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*
(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_small=Pofft3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=pi-asin(1/(3*m)):(y+asin(1/(3*m)))/100:pi+y
    Pt3_pi_large_3=Pt3_pi_large_3+((y+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_3=Pd2_pi_large_3+((y+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
```

```
    Pont3_pi_large_2=Pont3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_2=Pofft3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=y:pi/100:pi+y
    Pt3_pi=Pt3_pi+(pi/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Pd2_pi=Pd2_pi+(pi/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Pont3_pi=Pont3_pi+(pi/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi=Pofft3_pi+(pi/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/
(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=y:(pi+asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt3_pi_below_1=Pt3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_below_1=Pd2_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_1=Pont3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_below_1=Pofft3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs
(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=pi+y:(asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt2_pi_large_2=Pt2_pi_large_2+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_2=Pd3_pi_large_2+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_2=Prrd3_pi_large_2+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-
y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=2*pi-asin(1/(3*m)):(asin(1/(3*m))-pi+y)/100:pi+y
    Pt3_pi_below_2=Pt3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
```

```
    Pd2_pi_below_2=Pd2_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_2=Pont3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_below_2=Pofft3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=2*pi-asin(1/(3*m)):asin(1/(3*m))/100:2*pi
    Pt2_pi_large_3=Pt2_pi_large_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_3=Pd3_pi_large_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_3=Prrd3_pi_large_3+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_small_3=Pt2_pi_small_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_3=Pd3_pi_small_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_2=Prrd3_pi_small_2+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,ADrev-BDrev*ICM*sin(x-y)+CDrev*(ICM*sin(x-y))^2,'o')%,x,sin(x-y),'+')
%     hold on

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=pi+y:(pi-y)/100:2*pi
    Pt2_pi_2=Pt2_pi_2+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_2=Pd3_pi_2+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_2=Prrd3_pi_2+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

%     plot(x,(1/2)+(3/2)*m*sin(x),'o')
%     hold on
end

for x=pi+y:(pi-y)/100:2*pi
    Pt2_pi_below_4=Pt2_pi_below_4+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_4=Pd3_pi_below_4+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_3=Prrd3_pi_below_3+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
```

```
end

Pt2_pi=Pt2_pi_1+Pt2_pi_2;
Pd3_pi=Pd3_pi_1+Pd3_pi_2;
Prrd3_pi=Prrd3_pi_1+Prrd3_pi_2;
Pt2_pi_large=Pt2_pi_large_1+Pt2_pi_large_2+Pt2_pi_large_3;
Pt3_pi_large=Pt3_pi_large_1+Pt3_pi_large_2+Pt3_pi_large_3;
Pd2_pi_large=Pd2_pi_large_1+Pd2_pi_large_2+Pd2_pi_large_3;
Pd3_pi_large=Pd3_pi_large_1+Pd3_pi_large_2+Pd3_pi_large_3;
Pont3_pi_large=Pont3_pi_large_1+Pont3_pi_large_2;
Pofft3_pi_large=Pofft3_pi_large_1+Pofft3_pi_large_2;
Prrd3_pi_large=Prrd3_pi_large_1+Prrd3_pi_large_2+Prrd3_pi_large_3;
Pt2_pi_small=Pt2_pi_small_1+Pt2_pi_small_2+Pt2_pi_small_3;
Pt3_pi_small=Pt3_pi_small_1+Pt3_pi_small_2;
Pd2_pi_small=Pd2_pi_small_1+Pd2_pi_small_2;
Pd3_pi_small=Pd3_pi_small_1+Pd3_pi_small_2+Pd3_pi_small_3;
Prrd3_pi_small=Prrd3_pi_small_1+Prrd3_pi_small_2;
Pt2_pi_below=Pt2_pi_below_1+Pt2_pi_below_2+Pt2_pi_below_3+Pt2_pi_below_4;
Pt3_pi_below=Pt3_pi_below_1+Pt3_pi_below_2;
Pd2_pi_below=Pd2_pi_below_1+Pd2_pi_below_2;
Pd3_pi_below=Pd3_pi_below_1+Pd3_pi_below_2+Pd3_pi_below_3+Pd3_pi_below_4;
Pont3_pi_below=Pont3_pi_below_1+Pont3_pi_below_2;
Pofft3_pi_below=Pofft3_pi_below_1+Pofft3_pi_below_2;
Prrd3_pi_below=Prrd3_pi_below_1+Prrd3_pi_below_2+Prrd3_pi_below_3;


  if m<=(1/3)
      Y=[
             Pt1_pi Pont1_pi+Pofft1_pi
             Pt2_pi Pont2_pi+Pofft2_pi
             Pt3_pi Pont3_pi+Pofft3_pi
             Pd1_pi Prrd1_pi
             Pd2_pi Prrd2_pi
             Pd3_pi Prrd3_pi
             ]

          bar(Y,'stacked')
          title('Loss distribution')
          xlabel('4 level pi type')     %m<=1/3
          ylabel('Devices loss(W)')
          set(gca,'YGrid','on')
          set(gca,'XTickLabel',{'T1','T2','T3','D1','D2','D3'})
          legend('Con loss','Sw loss')
  elseif asin(1/(3*m))>=y
       Y=[
             Pt1_pi_large Pont1_pi_large+Pofft1_pi_large
             Pt2_pi_large Pont2_pi_large+Pofft2_pi_large
             Pt3_pi_large Pont3_pi_large+Pofft3_pi_large
             Pd1_pi_large Prrd1_pi_large
             Pd2_pi_large Prrd2_pi_large
```

```
            Pd3_pi_large Prrd3_pi_large
            ]

        bar(Y,'stacked')
        title('Loss distribution')
        xlabel('4 level pi type')%m>1/3, arcsin(1/(3*m))>=y
        ylabel('Devices loss(W)')
        set(gca,'YGrid','on')
        set(gca,'XTickLabel',{'T1','T2','T3','D1','D2','D3'})
        legend('Con loss','Sw loss')
        Pcon_4levelpi=6*(Pont1_pi_large+Pont2_pi_large+Pont3_pi_large+Pofft1_pi_large+Pofft2_pi_large+Pofft3_pi_large+Prrd1_pi_large+Prrd2_pi_large+Prrd3_pi_large+Pt1_pi_large+Pt2_pi_large+Pt3_pi_large+Pd1_pi_large+Pd2_pi_large+Pd3_pi_large)
  elseif (pi-asin(1/(3*m)))>y
      Y=[
            Pt1_pi_small Pont1_pi_small+Pofft1_pi_small
            Pt2_pi_small Pont2_pi_small+Pofft2_pi_small
            Pt3_pi_small Pont3_pi_small+Pofft3_pi_small
            Pd1_pi_small Prrd1_pi_small
            Pd2_pi_small Prrd2_pi_small
            Pd3_pi_small Prrd3_pi_small
            ]

        bar(Y,'stacked')
 %       title('Loss distribution')
 %       xlabel('4 level pi type')%m>1/3, arcsin(1/(3*m))<y<(pi-asin(1/(3*m)))
        ylabel('Devices loss(W)')
        set(gca,'YGrid','on')
        set(gca,'XTickLabel',{'T1','T2','T3','D1','D2','D3'})
        legend('Con loss','Sw loss')
  else
      Y=[
            Pt1_pi_below Pont1_pi_below+Pofft1_pi_below
            Pt2_pi_below Pont2_pi_below+Pofft2_pi_below
            Pt3_pi_below Pont3_pi_below+Pofft3_pi_below
            Pd1_pi_below Prrd1_pi_below
            Pd2_pi_below Prrd2_pi_below
            Pd3_pi_below Prrd3_pi_below
            ]

        bar(Y,'stacked')
        title('Loss distribution')
        xlabel('4 level pi type') %m>1/3, (pi-arcsin(1/(3*m)))<=y
        ylabel('Devices loss(W)')
        set(gca,'YGrid','on')
        set(gca,'XTickLabel',{'T1','T2','T3','D1','D2','D3'})
        legend('Con loss','Sw loss')
  end
```

II. Power loss vs power factor angle curve of the four-level π-type converter

```
%% IGBT loss with sinusodial modulaton %%
clear all

%   600V IGBT & diode characteristics
UT0=1.17;         % IGBT initial voltage drop 600V
rfT=(4-1.17)/67.5;  % Slope of IGBT V/I curve  600V

UD0=1.02;          % Diode initial voltage drop 600Vvc
rfD=(2.85-1.02)/50;    %12e-3;       % Slope of diode V/I curve 600V

ATon= -3.26e-5;    % curve fitting coefficient turn-on loss
BTon= 2.61e-5;;   % curve fitting coefficient turn-on loss
CTon= 5.36e-7;   % curve fitting coefficient turn-on loss

AToff= -0.708e-5;    % curve fitting coefficient turn-off loss
BToff= 1.84e-5;    % curve fitting coefficient turn-off loss
CToff= 7.63e-8;    % curve fitting coefficient turn-off loss

ADrev= 4.2e-4; % curve fitting diode reverse recovery loss
BDrev= 7.88e-5; % curve fitting diode reverse recovery loss
CDrev= -1.04e-7;% curve fitting diode reverse recovery loss

%   1200V IGBT and diode characteristics
VCEN=3; % rated IGBT voltage drop
VCE0=1; % IGBT threshold voltage
ICN=21.25;    % rated IGBT collector current 300A

VFN=2;  % rated diode voltage drop
VF0=0.9;%1.05;  % diode forward threshold voltage
ICNF=19; % rated Diode current
ri=(VCEN-VCE0)/ICN;
rd=0.057;%(VFN-VF0)/ICNF;

AoTon=2.15e-4;
BoTon=2.6e-5;
CoTon=3.5e-6;

AoToff=0.4e-4;
BoToff=1.007e-4;
CoToff=-1e-6;

AoD=8.00e-4;
BoD=6.8e-5;

ICM=15; % Amplitude of the phase current
VCC1=600;% Dc-link voltage  maybe should choose 1200V
VCC2=400;
Vdc1=600; % real dc-link voltage
Vdc3=(Vdc1)/3;
m=0.95;    % The modulation index
```

```
fc=10e3;    % carrier frequency
fs=fc;
i=1;
for y=0:0.2:pi;  % Power factor  0 inverter operation pi rectifier operation

Pt1_pi=0;
Pt2_pi_1=0;
Pt2_pi_2=0;
Pt3_pi=0;
Pd1_pi=0;
Pd2_pi=0;
Pd3_pi_1=0;
Pd3_pi_2=0;
Pont1_pi=0;
Pont2_pi=0;
Pont3_pi=0;
Pofft1_pi=0;
Pofft2_pi=0;
Pofft3_pi=0;
Prrd1_pi=0;
Prrd2_pi=0;
Prrd3_pi_1=0;
Prrd3_pi_2=0;

Pt1_pi_large=0;
Pt2_pi_large_1=0;
Pt2_pi_large_2=0;
Pt2_pi_large_3=0;
Pt3_pi_large_1=0;
Pt3_pi_large_2=0;
Pt3_pi_large_3=0;
Pd1_pi_large=0;
Pd2_pi_large_1=0;
Pd2_pi_large_2=0;
Pd2_pi_large_3=0;
Pd3_pi_large_1=0;
Pd3_pi_large_2=0;
Pd3_pi_large_3=0;
Pont1_pi_large=0;
Pofft1_pi_large=0;
Pont2_pi_large=0;
Pofft2_pi_large=0;
Pont3_pi_large_1=0;
Pofft3_pi_large_1=0;
Pont3_pi_large_2=0;
Pofft3_pi_large_2=0;
Prrd1_pi_large=0;
Prrd2_pi_large=0;
Prrd3_pi_large_1=0;
Prrd3_pi_large_2=0;
```

```
Prrd3_pi_large_3=0;

Pt1_pi_small=0;
Pt2_pi_small_1=0;
Pt2_pi_small_2=0;
Pt2_pi_small_3=0;
Pt3_pi_small_1=0;
Pt3_pi_small_2=0;
Pd1_pi_small=0;
Pd2_pi_small_1=0;
Pd2_pi_small_2=0;
Pd3_pi_small_1=0;
Pd3_pi_small_2=0;
Pd3_pi_small_3=0;
Pont1_pi_small=0;
Pofft1_pi_small=0;
Pont2_pi_small=0;
Pofft2_pi_small=0;
Pont3_pi_small=0;
Pofft3_pi_small=0;
Prrd1_pi_small=0;
Prrd2_pi_small=0;
Prrd3_pi_small_1=0;
Prrd3_pi_small_2=0;

Pt1_pi_below=0;
Pt2_pi_below_1=0;
Pt2_pi_below_2=0;
Pt2_pi_below_3=0;
Pt2_pi_below_4=0;
Pt3_pi_below_1=0;
Pt3_pi_below_2=0;
Pd1_pi_below=0;
Pd2_pi_below_1=0;
Pd2_pi_below_2=0;
Pd3_pi_below_1=0;
Pd3_pi_below_2=0;
Pd3_pi_below_3=0;
Pd3_pi_below_4=0;
Pont1_pi_below=0;
Pofft1_pi_below=0;
Pont2_pi_below=0;
Pofft2_pi_below=0;
Pont3_pi_below_1=0;
Pofft3_pi_below_1=0;
Pont3_pi_below_2=0;
Pofft3_pi_below_2=0;
Prrd1_pi_below=0;
Prrd2_pi_below=0;
Prrd3_pi_below_1=0;
```

```
Prrd3_pi_below_2=0;
Prrd3_pi_below_3=0;

for x=0:asin(1/(3*m))/100:asin(1/(3*m))
    Pt2_pi_small_1=Pt2_pi_small_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_1=Pd3_pi_small_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_1=Prrd3_pi_small_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_1=Pt2_pi_below_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_1=Pd3_pi_below_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_1=Prrd3_pi_below_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=asin(1/(3*m)):(y-asin(1/(3*m)))/100:y
    Pt2_pi_small_2=Pt2_pi_small_2+((y-asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_small=Pd1_pi_small+((y-asin(1/(3*m)))/100)*(VF0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_2=Pd3_pi_small_2+((y-asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_small=Pont2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft2_pi_small=Pofft2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_small=Prrd1_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))+CoD*
(ICM*sin(x-y))^2)/(2*pi);

end

for x=0:y/100:y
    Pt2_pi_1=Pt2_pi_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs(1/2+(3/2)*m*sin(x))/
(2*pi);
    Pd3_pi_1=Pd3_pi_1+(y/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Prrd3_pi_1=Prrd3_pi_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/
(2*pi);
    Pt2_pi_large_1=Pt2_pi_large_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Pd3_pi_large_1=Pd3_pi_large_1+(y/100)*(UD0-rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Prrd3_pi_large_1=Prrd3_pi_large_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*
(ICM*sin(x-y))^2)/(2*pi);

end
```

```
for x=y:(asin(1/(3*m))-y)/100:asin(1/(3*m))
    Pt3_pi_large_1=Pt3_pi_large_1+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_1=Pd2_pi_large_1+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_large_1=Pont3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_1=Pofft3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=y:(pi-asin(1/(3*m))-y)/100:pi-asin(1/(3*m))
    Pt1_pi_small=Pt1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_small_1=Pt3_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_1=Pd2_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_small=Pont1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_small=Pofft1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_small=Prrd2_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=asin(1/(3*m)):(pi-2*asin(1/(3*m)))/100:pi-asin(1/(3*m))
    Pt1_pi_large=Pt1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_large_2=Pt3_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_2=Pd2_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_large=Pont1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_large=Pofft1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_large=Prrd2_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_2=Pt2_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_below=Pd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*(VF0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_2=Pd3_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_below=Pont2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
```

```
    Pofft2_pi_below=Pofft2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_below=Prrd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))+CoD*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):(y-pi+asin(1/(3*m)))/100:y
    Pt2_pi_below_3=Pt2_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_3=Pd3_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_2=Prrd3_pi_below_2+((y-pi+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):2*asin(1/(3*m))/100:pi+asin(1/(3*m))
    Pt3_pi_small_2=Pt3_pi_small_2+(2*asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_2=Pd2_pi_small_2+(2*asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_small=Pont3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_small=Pofft3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):(y+asin(1/(3*m)))/100:pi+y
    Pt3_pi_large_3=Pt3_pi_large_3+((y+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_3=Pd2_pi_large_3+((y+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_large_2=Pont3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_2=Pofft3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=y:pi/100:pi+y
    Pt3_pi=Pt3_pi+(pi/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi=Pd2_pi+(pi/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi=Pont3_pi+(pi/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi=Pofft3_pi+(pi/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
```

```
end

for x=y:(pi+asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt3_pi_below_1=Pt3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_below_1=Pd2_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_1=Pont3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_below_1=Pofft3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi+y:(asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt2_pi_large_2=Pt2_pi_large_2+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_2=Pd3_pi_large_2+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_2=Prrd3_pi_large_2+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=2*pi-asin(1/(3*m)):(asin(1/(3*m))-pi+y)/100:pi+y
    Pt3_pi_below_2=Pt3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_below_2=Pd2_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_2=Pont3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_below_2=Pofft3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=2*pi-asin(1/(3*m)):asin(1/(3*m))/100:2*pi
    Pt2_pi_large_3=Pt2_pi_large_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_3=Pd3_pi_large_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_3=Prrd3_pi_large_3+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_small_3=Pt2_pi_small_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_3=Pd3_pi_small_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_2=Prrd3_pi_small_2+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
```

```
end

for x=pi+y:(pi-y)/100:2*pi
    Pt2_pi_2=Pt2_pi_2+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin
(x))/(2*pi);
    Pd3_pi_2=Pd3_pi_2+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin
(x))/(2*pi);
    Prrd3_pi_2=Prrd3_pi_2+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))
^2)/(2*pi);

end

for x=pi+y:(pi-y)/100:2*pi
    Pt2_pi_below_4=Pt2_pi_below_4+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+
(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_4=Pd3_pi_below_4+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+
(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_3=Prrd3_pi_below_3+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*
(ICM*sin(x-y))^2)/(2*pi);
end

Pt2_pi=Pt2_pi_1+Pt2_pi_2;
Pd3_pi=Pd3_pi_1+Pd3_pi_2;
Prrd3_pi=Prrd3_pi_1+Prrd3_pi_2;
Pt2_pi_large=Pt2_pi_large_1+Pt2_pi_large_2+Pt2_pi_large_3;
Pt3_pi_large=Pt3_pi_large_1+Pt3_pi_large_2+Pt3_pi_large_3;
Pd2_pi_large=Pd2_pi_large_1+Pd2_pi_large_2+Pd2_pi_large_3;
Pd3_pi_large=Pd3_pi_large_1+Pd3_pi_large_2+Pd3_pi_large_3;
Pont3_pi_large=Pont3_pi_large_1+Pont3_pi_large_2;
Pofft3_pi_large=Pofft3_pi_large_1+Pofft3_pi_large_2;
Prrd3_pi_large=Prrd3_pi_large_1+Prrd3_pi_large_2+Prrd3_pi_large_3;
Pt2_pi_small=Pt2_pi_small_1+Pt2_pi_small_2+Pt2_pi_small_3;
Pt3_pi_small=Pt3_pi_small_1+Pt3_pi_small_2;
Pd2_pi_small=Pd2_pi_small_1+Pd2_pi_small_2;
Pd3_pi_small=Pd3_pi_small_1+Pd3_pi_small_2+Pd3_pi_small_3;
Prrd3_pi_small=Prrd3_pi_small_1+Prrd3_pi_small_2;
Pt2_pi_below=Pt2_pi_below_1+Pt2_pi_below_2+Pt2_pi_below_3+Pt2_pi_below_4;
Pt3_pi_below=Pt3_pi_below_1+Pt3_pi_below_2;
Pd2_pi_below=Pd2_pi_below_1+Pd2_pi_below_2;
Pd3_pi_below=Pd3_pi_below_1+Pd3_pi_below_2+Pd3_pi_below_3+Pd3_pi_below_4;
Pont3_pi_below=Pont3_pi_below_1+Pont3_pi_below_2;
Pofft3_pi_below=Pofft3_pi_below_1+Pofft3_pi_below_2;
Prrd3_pi_below=Prrd3_pi_below_1+Prrd3_pi_below_2+Prrd3_pi_below_3;


  if m<=(1/3)
       PT1_pi(i)=Pt1_pi+Pont1_pi+Pofft1_pi;
       PT2_pi(i)=Pt2_pi+Pont2_pi+Pofft2_pi;
       PT3_pi(i)=Pt3_pi+Pont3_pi+Pofft3_pi;
       PD1_pi(i)=Pd1_pi+Prrd1_pi;
```

```
        PD2_pi(i)=Pd2_pi+Prrd2_pi;
        PD3_pi(i)=Pd3_pi+Prrd3_pi;
    elseif asin(1/(3*m))>=y
        PT1_pi(i)=Pt1_pi_large+Pont1_pi_large+Pofft1_pi_large;
        PT2_pi(i)=Pt2_pi_large+Pont2_pi_large+Pofft2_pi_large;
        PT3_pi(i)=Pt3_pi_large+Pont3_pi_large+Pofft3_pi_large;
        PD1_pi(i)=Pd1_pi_large+Prrd1_pi_large;
        PD2_pi(i)=Pd2_pi_large+Prrd2_pi_large;
        PD3_pi(i)=Pd3_pi_large+Prrd3_pi_large;
    elseif (pi-asin(1/(3*m)))>y
        PT1_pi(i)=Pt1_pi_small+Pont1_pi_small+Pofft1_pi_small;
        PT2_pi(i)=Pt2_pi_small+Pont2_pi_small+Pofft2_pi_small;
        PT3_pi(i)=Pt3_pi_small+Pont3_pi_small+Pofft3_pi_small;
        PD1_pi(i)=Pd1_pi_small+Prrd1_pi_small;
        PD2_pi(i)=Pd2_pi_small+Prrd2_pi_small;
        PD3_pi(i)=Pd3_pi_small+Prrd3_pi_small;
    else
        PT1_pi(i)=Pt1_pi_below+Pont1_pi_below+Pofft1_pi_below;
        PT2_pi(i)=Pt2_pi_below+Pont2_pi_below+Pofft2_pi_below;
        PT3_pi(i)=Pt3_pi_below+Pont3_pi_below+Pofft3_pi_below;
        PD1_pi(i)=Pd1_pi_below+Prrd1_pi_below;
        PD2_pi(i)=Pd2_pi_below+Prrd2_pi_below;
        PD3_pi(i)=Pd3_pi_below+Prrd3_pi_below;
    end
    i=i+1;
end

y=0:0.2:pi;
plot(y,PT1_pi,'m');hold on;
plot(y,PT2_pi,'r');hold on;
plot(y,PT3_pi,'g');hold on;
plot(y,PD1_pi,'c');hold on;
plot(y,PD2_pi,'k');hold on;
plot(y,PD3_pi,'b');hold on;
xlabel('power factor angle(rad)')
ylabel('Device loss(W)')
legend('T1(T6)','T2(T5)','T3(T4)','D1(D6)','D2(D5)','D3(D4)')
CoD=-8.627e-7;
```

III. Converter topologies efficiencies comparison

```
%% IGBT loss with sinusodial modulaton %%
clear all

%   600V IGBT & diode characteristics
UT0=1.17;        % IGBT initial voltage drop 600V
rfT=(4-1.17)/67.5;  % Slope of IGBT V/I curve  600V

UD0=1.02;         % Diode initial voltage drop 600Vvc
rfD=(2.85-1.02)/50;    %12e-3;       % Slope of diode V/I curve 600V

ATon= -3.26e-5;    % curve fitting coefficient turn-on loss
BTon= 2.61e-5;;  % curve fitting coefficient turn-on loss
CTon= 5.36e-7;  % curve fitting coefficient turn-on loss

ATOff= -0.708e-5;    % curve fitting coefficient turn-off loss
BTOff= 1.84e-5;    % curve fitting coefficient turn-off loss
CTOff= 7.63e-8;    % curve fitting coefficient turn-off loss

ADrev= 4.2e-4; % curve fitting diode reverse recovery loss
BDrev= 7.88e-5; % curve fitting diode reverse recovery loss
CDrev= -1.04e-7;% curve fitting diode reverse recovery loss

%   1200V IGBT and diode characteristics
VCEN=3; % rated IGBT voltage drop
VCE0=1; % IGBT threshold voltage
ICN=21.25;    % rated IGBT collector current 300A

VFN=2;  % rated diode voltage drop
VF0=0.9;%1.05;  % diode forward threshold voltage
ICNF=19; % rated Diode current
ri=(VCEN-VCE0)/ICN;
rd=0.057;%(VFN-VF0)/ICNF;

AoTon=2.15e-4;
BoTon=2.6e-5;
CoTon=3.5e-6;

AoToff=0.4e-4;
BoToff=1.007e-4;
CoToff=-1e-6;

AoD=8.00e-4;
BoD=6.8e-5;
CoD=-8.627e-7;

ICM=15;  % Amplitude of the phase current
VCC1=600;% Dc-link voltage  maybe should choose 1200V
VCC2=400;
Vdc1=600; % real dc-link voltage
Vdc2=(Vdc1)/2;
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Vdc3=(Vdc1)/3;
m=0.95;   % The modulation index
y=0;  % Power factor  0 inverter operation pi rectifier operation

i=1;
for fc=0:10:100e3;    % carrier frequency

    fs=fc;

    % Conduction loss
    Pi=((ri*cos(y)*ICM^2)/(3*pi) + (VCE0*cos(y)*ICM)/8)*m + (ri*ICM^2)/8 + (VCE0*ICM)/(2*pi);    % One IGBT conduction loss of 2-level converter
    Pd=(- (rd*cos(y)*ICM^2)/(3*pi) - (VF0*cos(y)*ICM)/8)*m + (rd*ICM^2)/8 + (VF0*ICM)/(2*pi);    % Diode conduction loss of 2-level converter
    Pt1_t=(VCE0*ICM*(cos(y)/4 + sin(y)/(4*pi) - (y*cos(y))/(4*pi)) + ICM^2*ri*(cos(y)^2/(6*pi) + cos(y)/(3*pi) + 1/(6*pi)))*m;  % One IGBT conduction loss of 3-level t-type converter
    Pd1_t=(ICM^2*rd*(cos(y)^2/(6*pi) - cos(y)/(3*pi) + 1/(6*pi)) + VF0*ICM*(sin(y)/(4*pi) - (y*cos(y))/(4*pi)))*m;  % Diode conduction loss of 3-level t-type converter
    Pt2_t=(-UT0*ICM*(cos(y)/4 + sin(y)/(2*pi) - (y*cos(y))/(2*pi)) - ICM^2*rfT*(cos(y)^2/(3*pi) + 1/(3*pi)))*m + (rfT*ICM^2)/4 + (UT0*ICM)/pi;
    Pd2_t=(-UD0*ICM*(cos(y)/4 + sin(y)/(2*pi) - (y*cos(y))/(2*pi)) - ICM^2*rfD*(cos(y)^2/(3*pi) + 1/(3*pi)))*m + (rfD*ICM^2)/4 + (UD0*ICM)/pi;
    Pt1_npc=(UT0*ICM*(cos(y)/4 + sin(y)/(4*pi) - (y*cos(y))/(4*pi)) + ICM^2*rfT*(cos(y)^2/(6*pi) + cos(y)/(3*pi) + 1/(6*pi)))*m;  % One IGBT conduction loss of 3-level npc converter
    Pd1_npc=(ICM^2*rfD*(cos(y)^2/(6*pi) - cos(y)/(3*pi) + 1/(6*pi)) + UD0*ICM*(sin(y)/(4*pi) - (y*cos(y))/(4*pi)))*m;  % Diode conduction loss of 3-level npc converter
    Pt2_npc=(-ICM^2*rfT*(cos(y)^2/(6*pi) - cos(y)/(3*pi) + 1/(6*pi)) - UT0*ICM*(sin(y)/(4*pi) - (y*cos(y))/(4*pi)))*m + (rfT*ICM^2)/4 + (UT0*ICM)/pi;
    Pd2_npc=(ICM^2*rfD*(cos(y)^2/(6*pi) - cos(y)/(3*pi) + 1/(6*pi)) + UD0*ICM*(sin(y)/(4*pi) - (y*cos(y))/(4*pi)))*m;
    Pd5_npc=(-UD0*ICM*(cos(y)/4 + sin(y)/(2*pi) - (y*cos(y))/(2*pi)) - ICM^2*rfD*(cos(y)^2/(3*pi) + 1/(3*pi)))*m + (rfD*ICM^2)/4 + (UD0*ICM)/pi;

    % Switching loss
    % IGBT turn-on loss
    Pon=fc*Vdc1/VCC1*(AoTon/2+BoTon/pi*ICM+CoTon/4*ICM^2);
    Pont1_t=fs*Vdc2/VCC1*((1/2 - y/(2*pi))*AoTon + (1/(2*pi) + cos(y)/(2*pi))*BoTon*ICM + ((cos(y)*sin(y))/(4*pi) - y/(4*pi) + 1/4)*CoTon*ICM^2);
    Pont2_t=fs*Vdc2/VCC2*((y/(2*pi))*ATon + (1/(2*pi) - cos(y)/(2*pi))*BTon*ICM + (y/(4*pi) - (cos(y)*sin(y))/(4*pi))*CTon*ICM^2);
    Pont1_npc=fs*Vdc2/VCC2*((1/2 - y/(2*pi))*ATon + (1/(2*pi) + cos(y)/(2*pi))*BTon*ICM + ((cos(y)*sin(y))/(4*pi) - y/(4*pi) + 1/4)*CTon*ICM^2);
    Pont2_npc=fs*Vdc2/VCC2*((y/(2*pi))*ATon + (1/(2*pi) - cos(y)/(2*pi))*BTon*ICM + (y/(4*pi) - (cos(y)*sin(y))/(4*pi))*CTon*ICM^2);

    % IGBT turn-off loss
    Poff=fc*Vdc1/VCC1*(AoToff/2+BoToff/pi*ICM+CoToff/4*ICM^2);
    Pofft1_t=fs*Vdc2/VCC1*((1/2 - y/(2*pi))*AoToff + (1/(2*pi) + cos(y)/(2*pi))*BoToff*ICM + ((cos(y)*sin(y))/(4*pi) - y/(4*pi) + 1/4)*CoToff*ICM^2);
    Pofft2_t=fs*Vdc2/VCC2*((y/(2*pi))*AToff + (1/(2*pi) - cos(y)/(2*pi))*BToff*ICM + (y/(4*pi) - (cos
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(y)*sin(y))/(4*pi))*CToff*ICM^2);
    Pofft1_npc=fs*Vdc2/VCC2*((1/2 - y/(2*pi))*AToff + (1/(2*pi) + cos(y)/(2*pi))*BToff*ICM + ((cos(y)
*sin(y))/(4*pi) - y/(4*pi) + 1/4)*CToff*ICM^2);
    Pofft2_npc=fs*Vdc2/VCC2*((y/(2*pi))*AToff + (1/(2*pi) - cos(y)/(2*pi))*BToff*ICM + (y/(4*pi) - (cos
(y)*sin(y))/(4*pi))*CToff*ICM^2);

    % Diode reverse recovery losses
    Prr=fc*Vdc1/VCC1*(AoD/2+BoD/pi*ICM+CoD/4*ICM^2);
    Prrd1_t=fs*Vdc2/VCC1*((y/(2*pi))*AoD + (1/(2*pi) - cos(y)/(2*pi))*BoD*ICM + (y/(4*pi) - (cos(y)*sin
(y))/(4*pi))*CoD*ICM^2);
    Prrd2_t=fs*Vdc2/VCC2*((1/2 - y/(2*pi))*ADrev + (1/(2*pi) + cos(y)/(2*pi))*BDrev*ICM + ((cos(y)*sin
(y))/(4*pi) - y/(4*pi) + 1/4)*CDrev*ICM^2);
    Prrd1_npc=fs*Vdc2/VCC2*((y/(2*pi))*ADrev + (1/(2*pi) - cos(y)/(2*pi))*BDrev*ICM + (y/(4*pi) - (cos
(y)*sin(y))/(4*pi))*CDrev*ICM^2);
    Prrd2_npc=0;
    Prrd5_npc=fs*Vdc2/VCC2*((1/2 - y/(2*pi))*ADrev + (1/(2*pi) + cos(y)/(2*pi))*BDrev*ICM + ((cos(y)
*sin(y))/(4*pi) - y/(4*pi) + 1/4)*CDrev*ICM^2);

Pt1_pi=0;
Pt2_pi_1=0;
Pt2_pi_2=0;
Pt3_pi=0;
Pd1_pi=0;
Pd2_pi=0;
Pd3_pi_1=0;
Pd3_pi_2=0;
Pont1_pi=0;
Pont2_pi=0;
Pont3_pi=0;
Pofft1_pi=0;
Pofft2_pi=0;
Pofft3_pi=0;
Prrd1_pi=0;
Prrd2_pi=0;
Prrd3_pi_1=0;
Prrd3_pi_2=0;

Pt1_pi_large=0;
Pt2_pi_large_1=0;
Pt2_pi_large_2=0;
Pt2_pi_large_3=0;
Pt3_pi_large_1=0;
Pt3_pi_large_2=0;
Pt3_pi_large_3=0;
Pd1_pi_large=0;
Pd2_pi_large_1=0;
Pd2_pi_large_2=0;
Pd2_pi_large_3=0;
Pd3_pi_large_1=0;
Pd3_pi_large_2=0;
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Pd3_pi_large_3=0;
Pont1_pi_large=0;
Pofft1_pi_large=0;
Pont2_pi_large=0;
Pofft2_pi_large=0;
Pont3_pi_large_1=0;
Pofft3_pi_large_1=0;
Pont3_pi_large_2=0;
Pofft3_pi_large_2=0;
Prrd1_pi_large=0;
Prrd2_pi_large=0;
Prrd3_pi_large_1=0;
Prrd3_pi_large_2=0;
Prrd3_pi_large_3=0;

Pt1_pi_small=0;
Pt2_pi_small_1=0;
Pt2_pi_small_2=0;
Pt2_pi_small_3=0;
Pt3_pi_small_1=0;
Pt3_pi_small_2=0;
Pd1_pi_small=0;
Pd2_pi_small_1=0;
Pd2_pi_small_2=0;
Pd3_pi_small_1=0;
Pd3_pi_small_2=0;
Pd3_pi_small_3=0;
Pont1_pi_small=0;
Pofft1_pi_small=0;
Pont2_pi_small=0;
Pofft2_pi_small=0;
Pont3_pi_small=0;
Pofft3_pi_small=0;
Prrd1_pi_small=0;
Prrd2_pi_small=0;
Prrd3_pi_small_1=0;
Prrd3_pi_small_2=0;

Pt1_pi_below=0;
Pt2_pi_below_1=0;
Pt2_pi_below_2=0;
Pt2_pi_below_3=0;
Pt2_pi_below_4=0;
Pt3_pi_below_1=0;
Pt3_pi_below_2=0;
Pd1_pi_below=0;
Pd2_pi_below_1=0;
Pd2_pi_below_2=0;
Pd3_pi_below_1=0;
Pd3_pi_below_2=0;
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Pd3_pi_below_3=0;
Pd3_pi_below_4=0;
Pont1_pi_below=0;
Pofft1_pi_below=0;
Pont2_pi_below=0;
Pofft2_pi_below=0;
Pont3_pi_below_1=0;
Pofft3_pi_below_1=0;
Pont3_pi_below_2=0;
Pofft3_pi_below_2=0;
Prrd1_pi_below=0;
Prrd2_pi_below=0;
Prrd3_pi_below_1=0;
Prrd3_pi_below_2=0;
Prrd3_pi_below_3=0;

for x=0:asin(1/(3*m))/100:asin(1/(3*m))
    Pt2_pi_small_1=Pt2_pi_small_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_1=Pd3_pi_small_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_1=Prrd3_pi_small_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_1=Pt2_pi_below_1+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_1=Pd3_pi_below_1+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_1=Prrd3_pi_below_1+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=asin(1/(3*m)):(y-asin(1/(3*m)))/100:y
    Pt2_pi_small_2=Pt2_pi_small_2+((y-asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_small=Pd1_pi_small+((y-asin(1/(3*m)))/100)*(VF0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_2=Pd3_pi_small_2+((y-asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_small=Pont2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft2_pi_small=Pofft2_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_small=Prrd1_pi_small+((y-asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))+CoD*
(ICM*sin(x-y))^2)/(2*pi);

end

for x=0:y/100:y
    Pt2_pi_1=Pt2_pi_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs(1/2+(3/2)*m*sin(x))/
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(2*pi);
    Pd3_pi_1=Pd3_pi_1+(y/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Prrd3_pi_1=Prrd3_pi_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))^2)/
(2*pi);
    Pt2_pi_large_1=Pt2_pi_large_1+(y/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Pd3_pi_large_1=Pd3_pi_large_1+(y/100)*(UD0-rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)
*m*sin(x))/(2*pi);
    Prrd3_pi_large_1=Prrd3_pi_large_1+(y/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*
(ICM*sin(x-y))^2)/(2*pi);

end

for x=y:(asin(1/(3*m))-y)/100:asin(1/(3*m))
    Pt3_pi_large_1=Pt3_pi_large_1+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_1=Pd2_pi_large_1+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_large_1=Pont3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_1=Pofft3_pi_large_1+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=y:(pi-asin(1/(3*m))-y)/100:pi-asin(1/(3*m))
    Pt1_pi_small=Pt1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_small_1=Pt3_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_1=Pd2_pi_small_1+abs((pi-asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_small=Pont1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_small=Pofft1_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_small=Prrd2_pi_small+abs((pi-asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=asin(1/(3*m)):(pi-2*asin(1/(3*m)))/100:pi-asin(1/(3*m))
    Pt1_pi_large=Pt1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*(VCE0+ri*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pt3_pi_large_2=Pt3_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_2=Pd2_pi_large_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont1_pi_large=Pont1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoTon+BoTon*ICM*abs(sin
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(x-y))+CoTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft1_pi_large=Pofft1_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoToff+BoToff*ICM*abs
(sin(x-y))+CoToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd2_pi_large=Prrd2_pi_large+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_below_2=Pt2_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pd1_pi_below=Pd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*(VF0+rd*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((-1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_2=Pd3_pi_below_2+abs((pi-2*asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin
(x-y))*abs((3/2)-(3/2)*m*sin(x))/(2*pi);
    Pont2_pi_below=Pont2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft2_pi_below=Pofft2_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);
    Prrd1_pi_below=Prrd1_pi_below+abs((pi-2*asin(1/(3*m)))/100)*fs*Vdc3/VCC1*(AoD+BoD*ICM*abs(sin(x-y))
+CoD*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):(y-pi+asin(1/(3*m)))/100:y
    Pt2_pi_below_3=Pt2_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_3=Pd3_pi_below_3+((y-pi+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_2=Prrd3_pi_below_2+((y-pi+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin
(x-y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):2*asin(1/(3*m))/100:pi+asin(1/(3*m))
    Pt3_pi_small_2=Pt3_pi_small_2+(2*asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_small_2=Pd2_pi_small_2+(2*asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_small=Pont3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*
(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_small=Pofft3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi-asin(1/(3*m)):(y+asin(1/(3*m)))/100:pi+y
    Pt3_pi_large_3=Pt3_pi_large_3+((y+asin(1/(3*m)))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_large_3=Pd2_pi_large_3+((y+asin(1/(3*m)))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_large_2=Pont3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))
+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_large_2=Pofft3_pi_large_2+((y+asin(1/(3*m)))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin
```
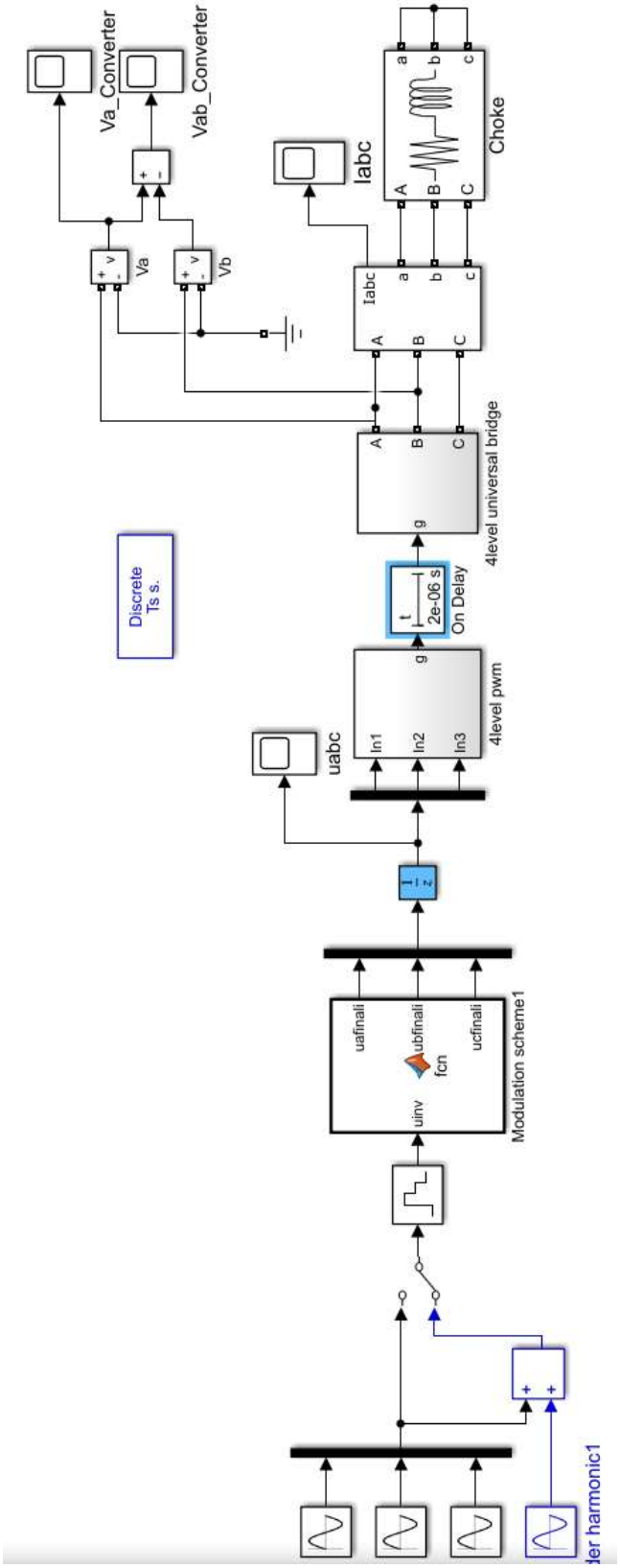

```
(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=y:pi/100:pi+y
    Pt3_pi=Pt3_pi+(pi/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Pd2_pi=Pd2_pi+(pi/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin(x))/
(2*pi);
    Pont3_pi=Pont3_pi+(pi/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi=Pofft3_pi+(pi/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))+CToff*(ICM*sin(x-y))^2)/
(2*pi);

end

for x=y:(pi+asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt3_pi_below_1=Pt3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_below_1=Pd2_pi_below_1+((pi+asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_1=Pont3_pi_below_1+((pi+asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi+y:(asin(1/(3*m))-y)/100:pi+asin(1/(3*m))
    Pt2_pi_large_2=Pt2_pi_large_2+((asin(1/(3*m))-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_2=Pd3_pi_large_2+((asin(1/(3*m))-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))
*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_2=Prrd3_pi_large_2+((asin(1/(3*m))-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-
y))+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_small=Pofft3_pi_small+(2*asin(1/(3*m))/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs(sin(x-y))
+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=2*pi-asin(1/(3*m)):(asin(1/(3*m))-pi+y)/100:pi+y
    Pt3_pi_below_2=Pt3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd2_pi_below_2=Pd2_pi_below_2+((asin(1/(3*m))-pi+y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-
y))*abs((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pont3_pi_below_2=Pont3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(ATon+BTon*ICM*abs(sin(x-
y))+CTon*(ICM*sin(x-y))^2)/(2*pi);
    Pofft3_pi_below_2=Pofft3_pi_below_2+((asin(1/(3*m))-pi+y)/100)*fs*Vdc3/VCC2*(AToff+BToff*ICM*abs
(sin(x-y))+CToff*(ICM*sin(x-y))^2)/(2*pi);

end

for x=2*pi-asin(1/(3*m)):asin(1/(3*m))/100:2*pi
```

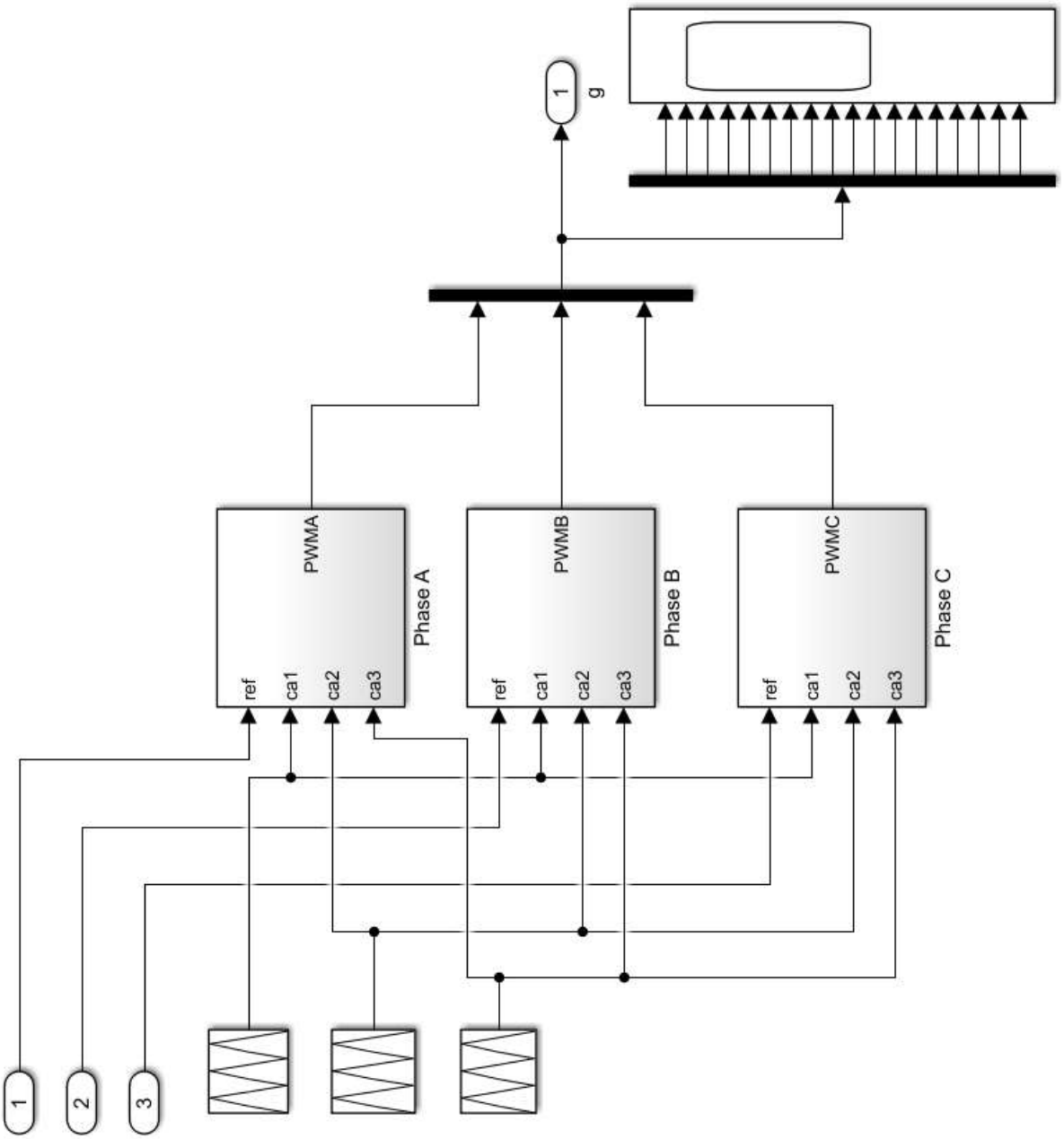
```
    Pt2_pi_large_3=Pt2_pi_large_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_large_3=Pd3_pi_large_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_large_3=Prrd3_pi_large_3+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);
    Pt2_pi_small_3=Pt2_pi_small_3+(asin(1/(3*m))/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_small_3=Pd3_pi_small_3+(asin(1/(3*m))/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs
((1/2)+(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_small_2=Prrd3_pi_small_2+(asin(1/(3*m))/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))
+CDrev*(ICM*sin(x-y))^2)/(2*pi);

end

for x=pi+y:(pi-y)/100:2*pi
    Pt2_pi_2=Pt2_pi_2+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin
(x))/(2*pi);
    Pd3_pi_2=Pd3_pi_2+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+(3/2)*m*sin
(x))/(2*pi);
    Prrd3_pi_2=Prrd3_pi_2+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*(ICM*sin(x-y))
^2)/(2*pi);
    Pt2_pi_below_4=Pt2_pi_below_4+((pi-y)/100)*(UT0+rfT*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+
(3/2)*m*sin(x))/(2*pi);
    Pd3_pi_below_4=Pd3_pi_below_4+((pi-y)/100)*(UD0+rfD*ICM*abs(sin(x-y)))*ICM*abs(sin(x-y))*abs((1/2)+
(3/2)*m*sin(x))/(2*pi);
    Prrd3_pi_below_3=Prrd3_pi_below_3+((pi-y)/100)*fs*Vdc3/VCC2*(ADrev+BDrev*ICM*abs(sin(x-y))+CDrev*
(ICM*sin(x-y))^2)/(2*pi);
end


Pt2_pi=Pt2_pi_1+Pt2_pi_2;
Pd3_pi=Pd3_pi_1+Pd3_pi_2;
Prrd3_pi=Prrd3_pi_1+Prrd3_pi_2;
Pt2_pi_large=Pt2_pi_large_1+Pt2_pi_large_2+Pt2_pi_large_3;
Pt3_pi_large=Pt3_pi_large_1+Pt3_pi_large_2+Pt3_pi_large_3;
Pd2_pi_large=Pd2_pi_large_1+Pd2_pi_large_2+Pd2_pi_large_3;
Pd3_pi_large=Pd3_pi_large_1+Pd3_pi_large_2+Pd3_pi_large_3;
Pont3_pi_large=Pont3_pi_large_1+Pont3_pi_large_2;
Pofft3_pi_large=Pofft3_pi_large_1+Pofft3_pi_large_2;
Prrd3_pi_large=Prrd3_pi_large_1+Prrd3_pi_large_2+Prrd3_pi_large_3;
Pt2_pi_small=Pt2_pi_small_1+Pt2_pi_small_2+Pt2_pi_small_3;
Pt3_pi_small=Pt3_pi_small_1+Pt3_pi_small_2;
Pd2_pi_small=Pd2_pi_small_1+Pd2_pi_small_2;
Pd3_pi_small=Pd3_pi_small_1+Pd3_pi_small_2+Pd3_pi_small_3;
Prrd3_pi_small=Prrd3_pi_small_1+Prrd3_pi_small_2;
Pt2_pi_below=Pt2_pi_below_1+Pt2_pi_below_2+Pt2_pi_below_3+Pt2_pi_below_4;
Pt3_pi_below=Pt3_pi_below_1+Pt3_pi_below_2;
Pd2_pi_below=Pd2_pi_below_1+Pd2_pi_below_2;
Pd3_pi_below=Pd3_pi_below_1+Pd3_pi_below_2+Pd3_pi_below_3+Pd3_pi_below_4;
```

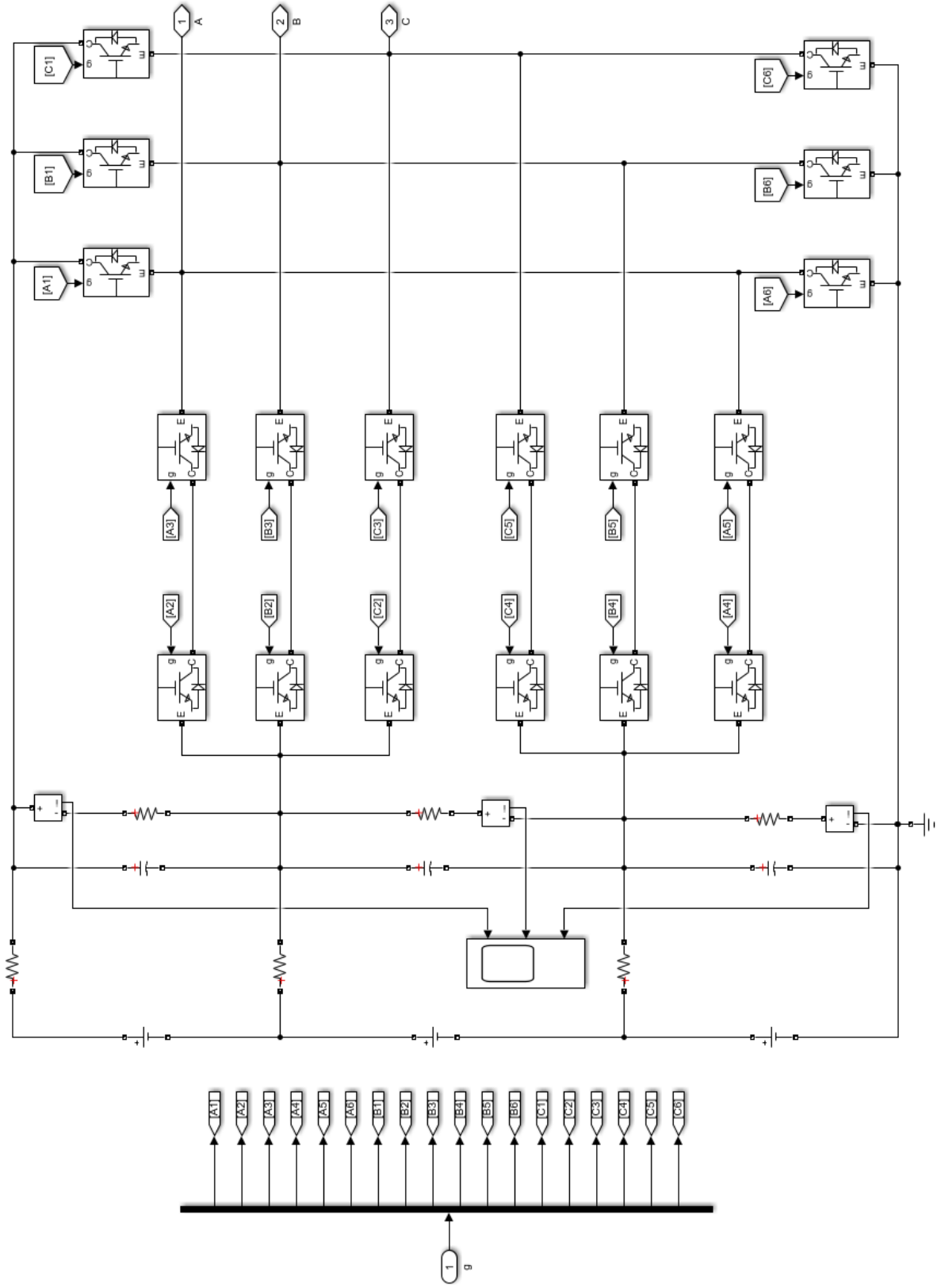
```
Pont3_pi_below=Pont3_pi_below_1+Pont3_pi_below_2;
Pofft3_pi_below=Pofft3_pi_below_1+Pofft3_pi_below_2;
Prrd3_pi_below=Prrd3_pi_below_1+Prrd3_pi_below_2+Prrd3_pi_below_3;

    % efficiency calculation
    Pcon_2level(i)=6*(Pon+Poff+Prr+Pi+Pd);
    Pcon_3levelt(i)=6*(Pont1_t+Pont2_t+Pofft1_t+Pofft2_t+Prrd1_t+Prrd2_t+Pt1_t+Pt2_t+Pd1_t+Pd2_t);
    Pcon_3levelnpc(i)=6* ↙
(Pont1_npc+Pont2_npc+Pofft1_npc+Pofft2_npc+Prrd1_npc+Prrd2_npc+Prrd5_npc+Pt1_npc+Pt2_npc+Pd1_npc+Pd2_np ↙
c+Pd5_npc);
    P_2level=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
    P_3levelt=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
    P_3levelnpc=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
    efficiency_2level(i)=P_2level/(P_2level+Pcon_2level(i));
    efficiency_3levelt(i)=P_3levelt/(P_3levelt+Pcon_3levelt(i));
    efficiency_3levelnpc(i)=P_3levelnpc/(P_3levelnpc+Pcon_3levelnpc(i));

  if m<=(1/3)
      Pcon_4levelpi(i)=6* ↙
(Pont1_pi+Pont2_pi+Pont3_pi+Pofft1_pi+Pofft2_pi+Pofft3_pi+Prrd1_pi+Prrd2_pi+Prrd3_pi+Pt1_pi+Pt2_pi+Pt3_ ↙
pi+Pd1_pi+Pd2_pi+Pd3_pi);
      P_4levelpi=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
      efficiency_4levelpi(i)=P_4levelpi/(Pcon_4levelpi(i)+P_4levelpi);
  elseif asin(1/(3*m))>=y
       Pcon_4levelpi(i)=6* ↙
(Pont1_pi_large+Pont2_pi_large+Pont3_pi_large+Pofft1_pi_large+Pofft2_pi_large+Pofft3_pi_large+Prrd1_pi_ ↙
large+Prrd2_pi_large+Prrd3_pi_large+Pt1_pi_large+Pt2_pi_large+Pt3_pi_large+Pd1_pi_large+Pd2_pi_large+Pd ↙
3_pi_large);
      P_4levelpi=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
      efficiency_4levelpi(i)=P_4levelpi/(Pcon_4levelpi(i)+P_4levelpi);
  elseif (pi-asin(1/(3*m)))>y
      Pcon_4levelpi(i)=6* ↙
(Pont1_pi_small+Pont2_pi_small+Pont3_pi_small+Pofft1_pi_small+Pofft2_pi_small+Pofft3_pi_small+Prrd1_pi_ ↙
small+Prrd2_pi_small+Prrd3_pi_small+Pt1_pi_small+Pt2_pi_small+Pt3_pi_small+Pd1_pi_small+Pd2_pi_small+Pd ↙
3_pi_small);
      P_4levelpi=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
      efficiency_4levelpi(i)=P_4levelpi/(Pcon_4levelpi(i)+P_4levelpi);
  else
      Pcon_4levelpi(i)=6* ↙
(Pont1_pi_below+Pont2_pi_below+Pont3_pi_below+Pofft1_pi_below+Pofft2_pi_below+Pofft3_pi_below+Prrd1_pi_ ↙
below+Prrd2_pi_below+Prrd3_pi_below+Pt1_pi_below+Pt2_pi_below+Pt3_pi_below+Pd1_pi_below+Pd2_pi_below+Pd ↙
3_pi_below);
      P_4levelpi=sqrt(3)*ICM/sqrt(2)*Vdc1/sqrt(2)*0.866*m*abs(cos(y));
      efficiency_4levelpi(i)=P_4levelpi/(Pcon_4levelpi(i)+P_4levelpi);
  end
    i=i+1;
end

fc=0:10:100e3;
plot(fc/1e3,efficiency_2level*100,'r',fc/1e3,efficiency_3levelt*100,'b',fc/1e3, ↙
```

```
efficiency_3levelnpc*100, 'g',fc/1e3,efficiency_4levelpi*100, 'k')
scatter(o,q)
scatter(g,h)
hold on
title('Converter efficiency variation with switching frequency' )
xlabel('Switching frequency(kHz)' )
ylabel('Converter efficiency(%)' )
legend('2 level','3 level T-type','3 level npc','4 level pi-type')
grid on
```

IV. Simulation models of four-level π-type converter to validate the effect on dc-link parallel resistors.



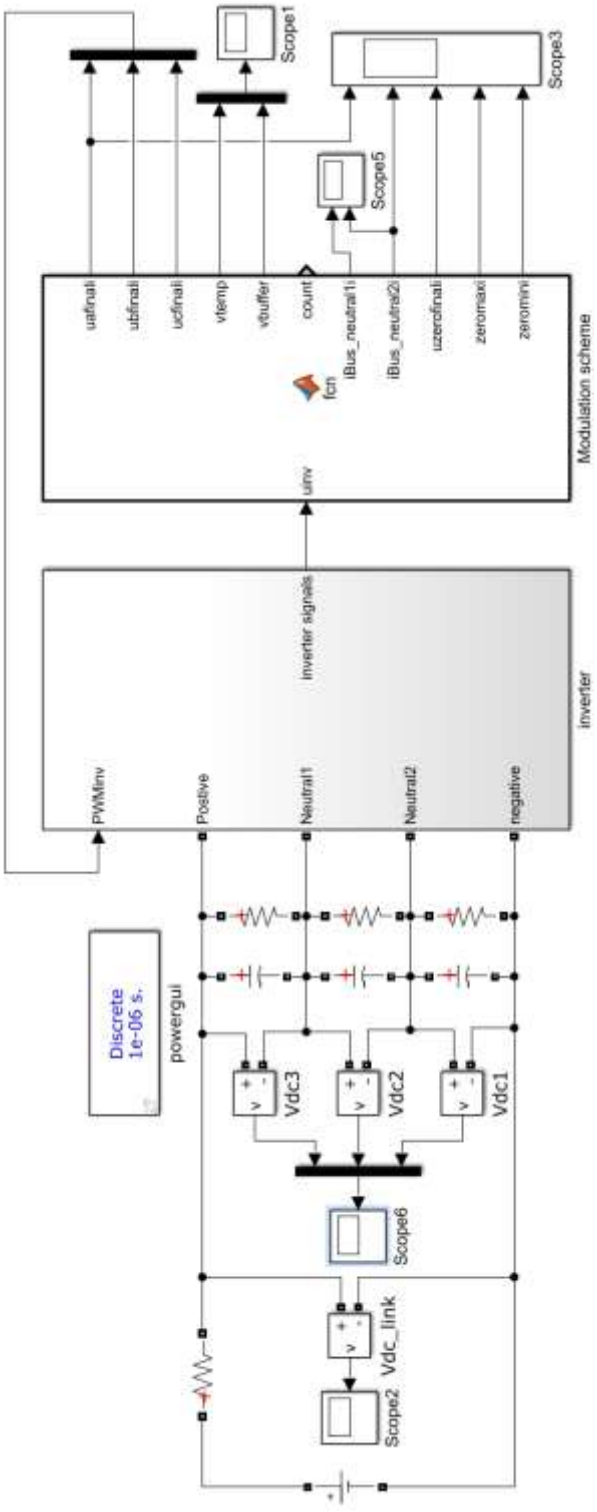

1
g
PWMA
Phase A
ref
ca1
ca2
ca3
PWMB
Phase B
ref
ca1
ca2
ca3
PWMC
Phase C
ref
ca1
ca2
ca3
1
2
3

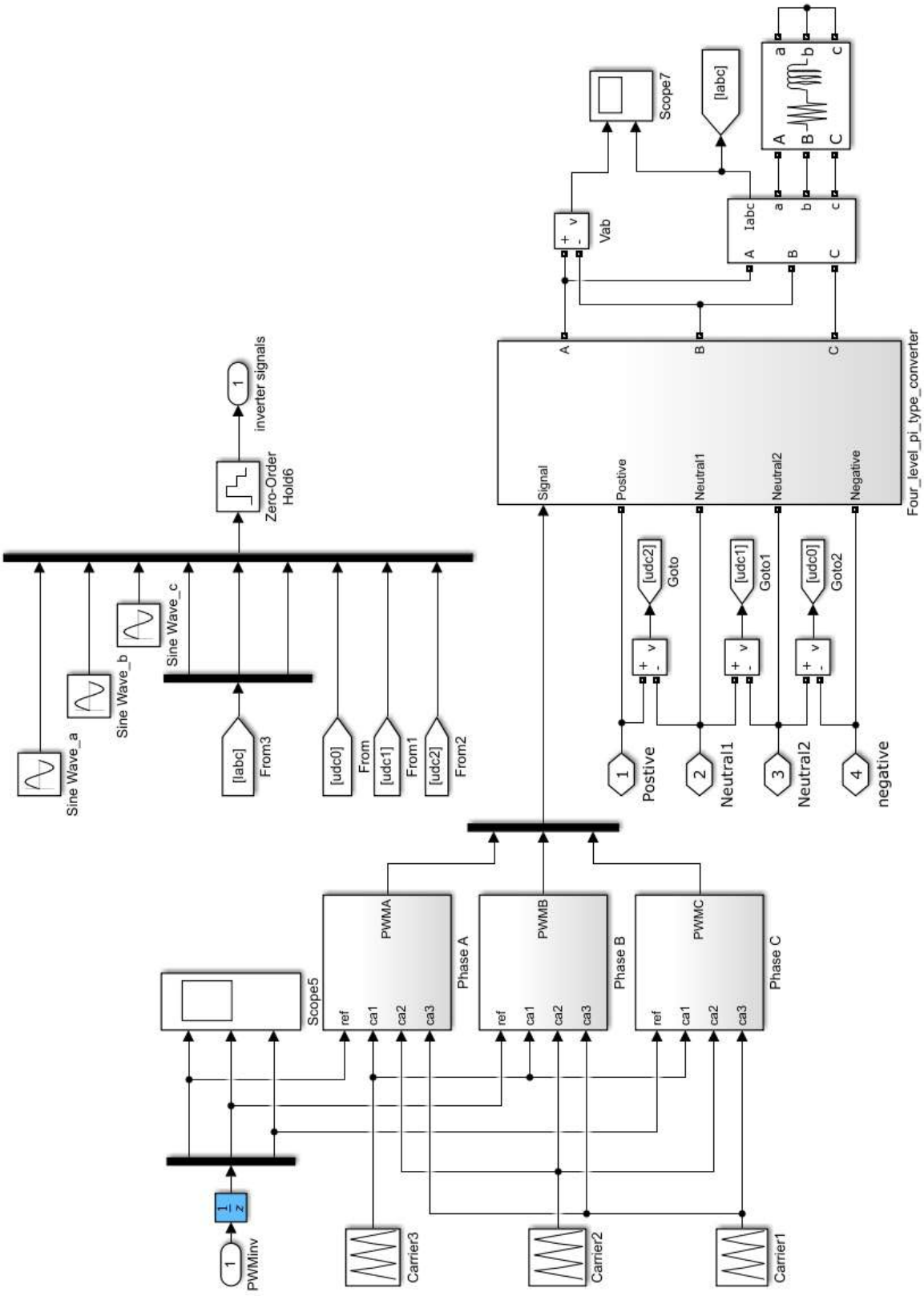

1
A
2
B
3
C
[C1]
[B1]
[A1]
[C6]
[B6]
[A6]
[A3]
[B3]
[C3]
[C5]
[B5]
[A5]
[A2]
[B2]
[C2]
[C4]
[B4]
[A4]
[A1]
[A2]
[A3]
[A4]
[A5]
[A6]
[B1]
[B2]
[B3]
[B4]
[B5]
[B6]
[C1]
[C2]
[C3]
[C4]
[C5]
[C6]
1
g

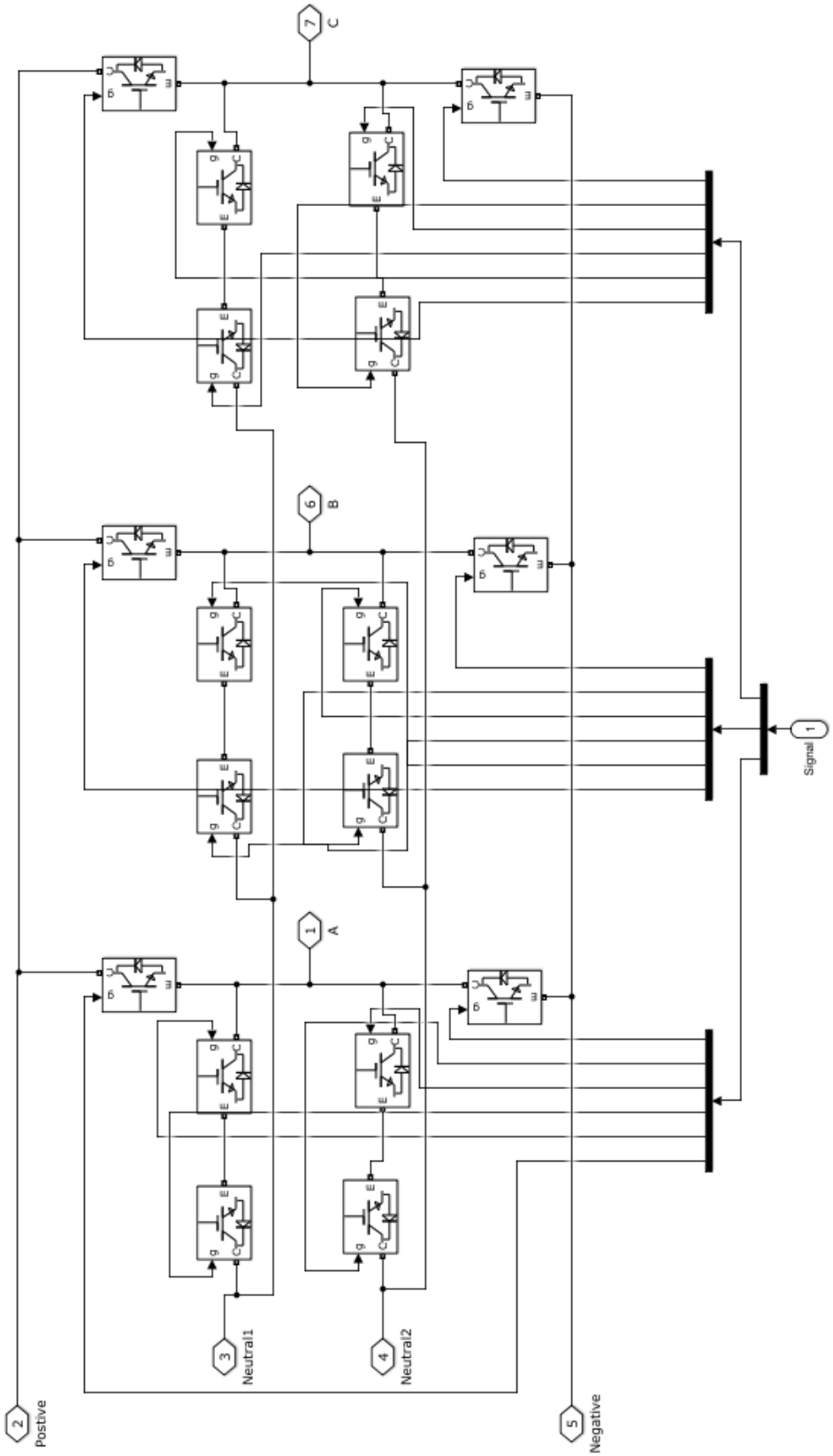
```
1     function [uafinali,ubfinali,ucfinali] = fcn(uinv)
2
3
4 -   uai=uinv(1);   ubi=uinv(2);uci=uinv(3);
5
6
7 -   uafinali=1.5*uai+1.5;
8 -   ubfinali=1.5*ubi+1.5;   %offset from (-1.5 to 1.5) to (0 to 3)
9 -   ucfinali=1.5*uci+1.5;
```

Appendix D. MATLAB/Simulink Simulation layout for the dc-link NP voltage balancing control

I. Four-level π-type converter (single-end inverter)



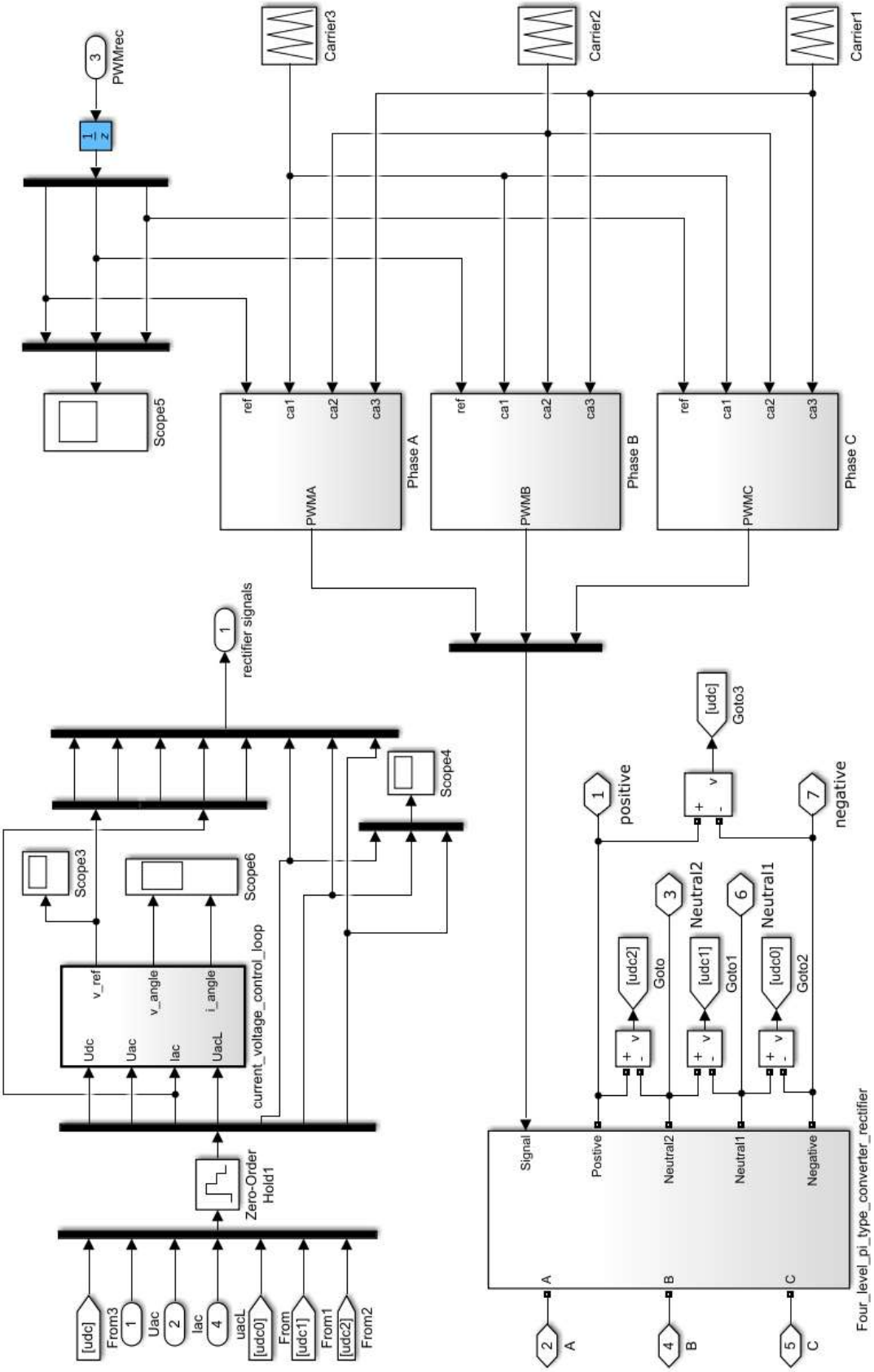

Sine Wave_a
Sine Wave_b
Sine Wave_c
[Iabc]
From3
[udc0]
From
[udc1]
From1
[udc2]
From2
Zero-Order Hold6
1
inverter signals
Scope7
[Iabc]
Vab
Iabc
a
b
c
A
B
C
Four_level_pi_type_converter
Signal
Postive
Neutral1
Neutral2
Negative
[udc2]
Goto
[udc1]
Goto1
[udc0]
Goto2
1
Postive
2
Neutral1
3
Neutral2
4
negative
Scope5
PWMA
PWMB
PWMC
Phase A
Phase B
Phase C
ref
ca1
ca2
ca3
1
z
PWMinv
Carrier3
Carrier2
Carrier1

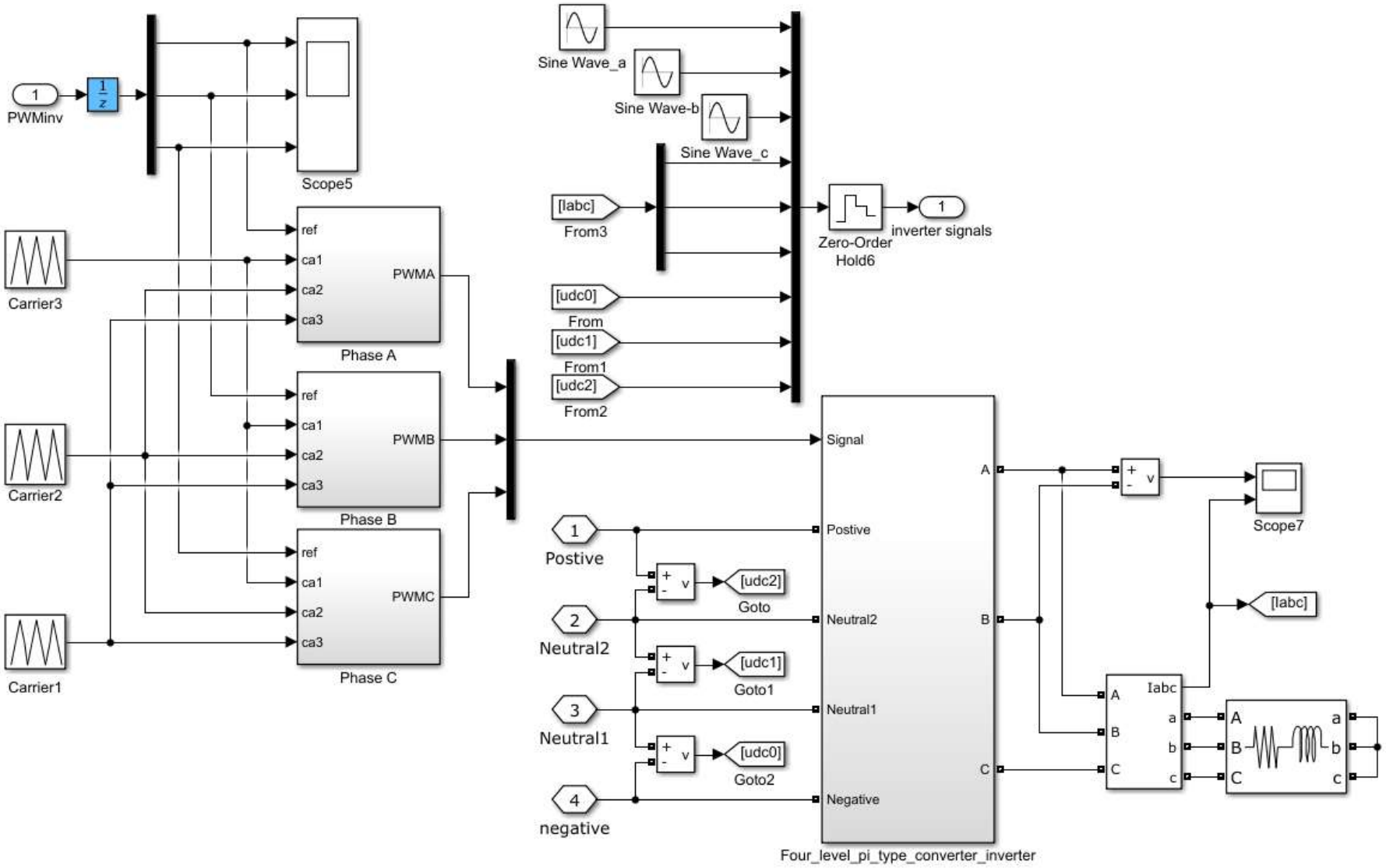

7
C
6
B
1
A
Signal
1
2
Postive
3
Neutral1
4
Neutral2
5
Negative

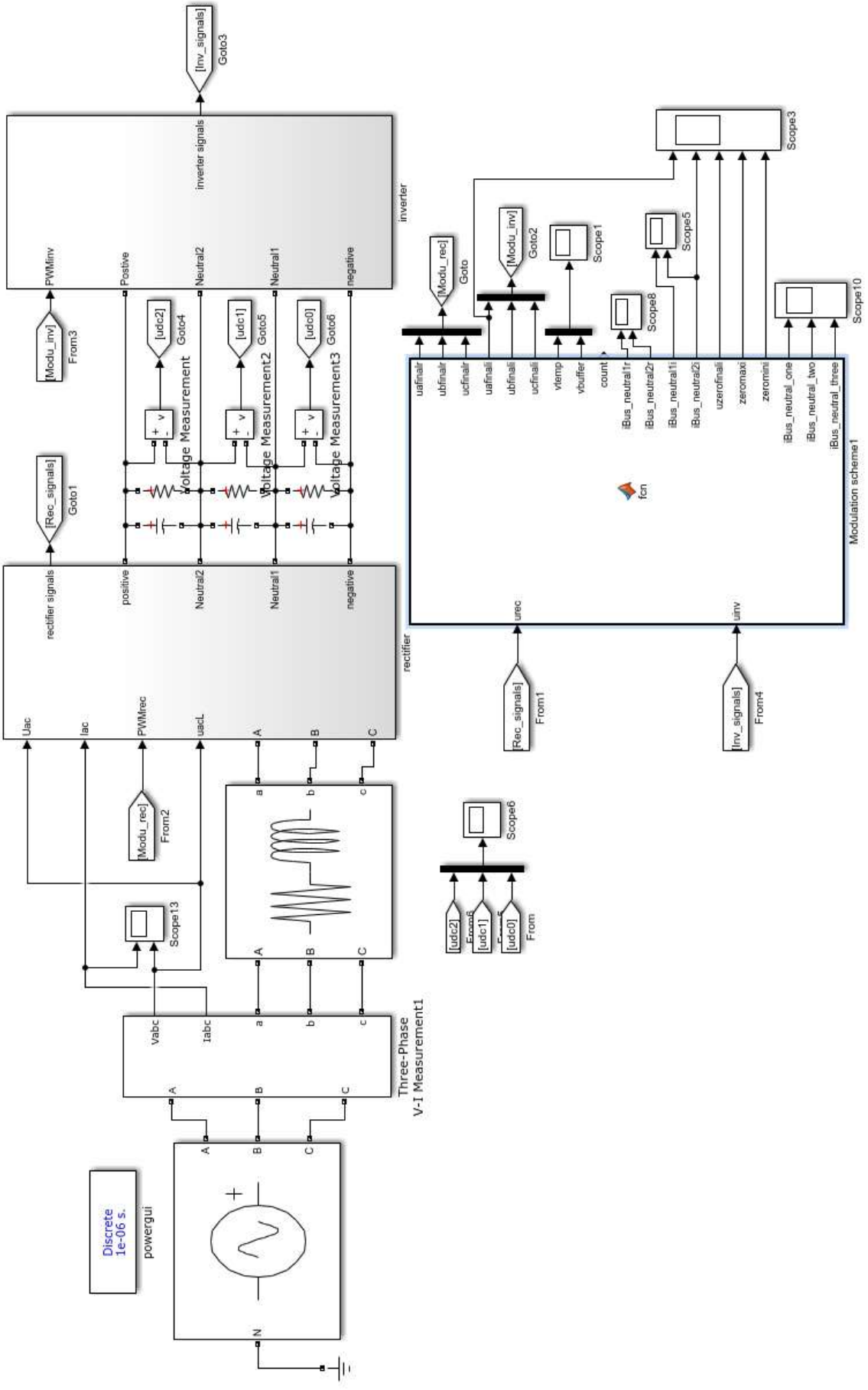
```
    function [uafinali,ubfinali,ucfinali,vtemp, vbuffer, count,iBus_neutral1i, iBus_neutral2i, ↙
uzerofinali, zeromaxi, zeromini] = fcn(uinv)

 udc0=uinv(7); udc1=uinv(8); udc2=uinv(9);
 uai=uinv(1);   ubi=uinv(2);uci=uinv(3);
 iai=uinv(4);  ibi=uinv(5); ici=uinv(6);

 utotal=udc0+udc1+udc2;
 uzerofinali=0;
 iBus_neutral1i=0;
 iBus_neutral2i=0;
 vbuffer=0;
 vtemp=0;
 count=0;

 uai=1.5*uai+1.5;
 ubi=1.5*ubi+1.5;    %offset from (-1.5 to 1.5) to (0 to 3)
 uci=1.5*uci+1.5;

 zeromaxi=3-max([uai,ubi,uci]);
 zeromini=-min([uai,ubi,uci]);

  step=0.05;%(zeromaxi-zeromini)/5;%2^-4; %0.01;

    for zeroseqi=zeromini:step:zeromaxi

      uanewi=uai+zeroseqi;
      ubnewi=ubi+zeroseqi;
      ucnewi=uci+zeroseqi;

        lai = floor(uanewi);
        lbi = floor(ubnewi);
        lci = floor(ucnewi);

        tai = uanewi - lai;
        tbi = ubnewi - lbi;
        tci = ucnewi - lci;

        iBus_neutral2i = iai*(tai*(lai == 1) +(1.0 - tai)*(lai == 2))+ ibi*(tbi*(lbi == 1) + (1.0 - ↙
tbi)*(lbi == 2))+ ici*(tci*(lci == 1) + (1.0 - tci)*(lci == 2));
        iBus_neutral1i = iai*(tai*(lai == 0) +(1.0 - tai)*(lai == 1))+ ibi*(tbi*(lbi == 0) + (1.0 - ↙
tbi)*(lbi == 1))+ ici*(tci*(lci == 0) + (1.0 - tci)*(lci == 1));

        iBus_neutral_three = iBus_neutral2i*2/3+iBus_neutral1i*1/3;        % for upper capacitor ↙
//inverter mode
        iBus_neutral_two = -iBus_neutral2i*1/3+iBus_neutral1i*1/3;         % for middle capacitor
        iBus_neutral_one = -iBus_neutral2i*1/3-iBus_neutral1i*2/3;     % for lower capacitor

        vtemp1 = (udc0-1/3*utotal)*iBus_neutral_one;      % capacitor voltage compared with Vdc/3  lower
        vtemp2 = (udc1-1/3*utotal)*iBus_neutral_two;      % middle capacitor
```

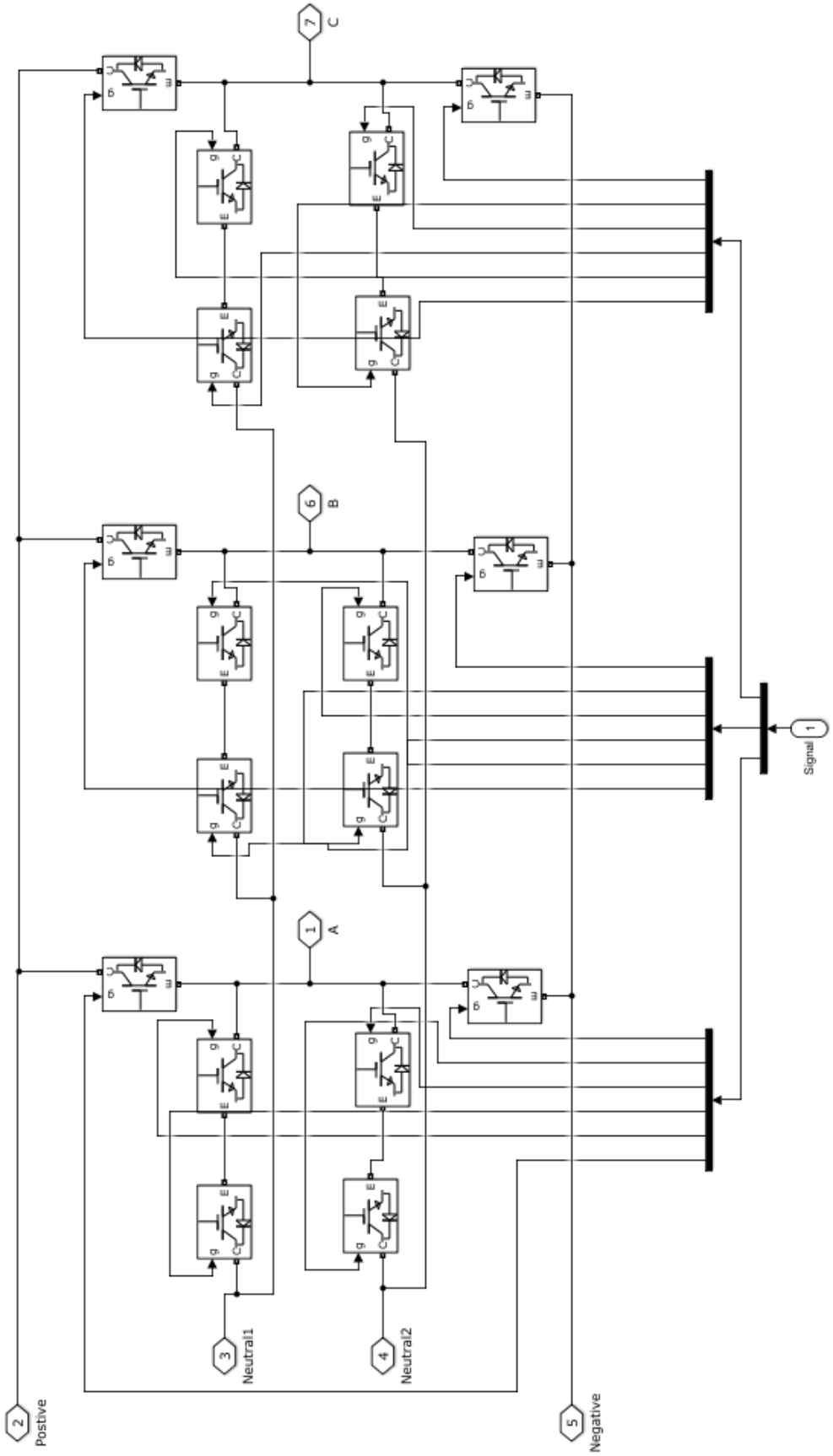
```
        vtemp3 = (udc2-1/3*utotal)*iBus_neutral_three;    % upper capacitor

        vtemp = vtemp1+vtemp2+vtemp3;

      if (abs(count)<1e-5)
                vbuffer=vtemp;
                uzerofinali = zeroseqi;
                count=1;
        end

              if (vtemp <= vbuffer)
                vbuffer = vtemp;
                uzerofinali = zeroseqi;
                count=2;
              end
end
     uafinali=uai+uzerofinali;
     ubfinali=ubi+uzerofinali;
     ucfinali=uci+uzerofinali;
```

II. Four-level π-type converter (back-to-back configuration)




1
PWMinv
1/z
Scope5
Carrier3
Carrier2
Carrier1
ref
ca1
ca2
ca3
PWMA
PWMB
PWMC
Phase A
Phase B
Phase C
Sine Wave_a
Sine Wave-b
Sine Wave_c
[Iabc]
From3
[udc0]
From
[udc1]
From1
[udc2]
From2
Zero-Order
Hold6
1
inverter signals
Signal
Postive
Neutral2
Neutral1
Negative
A
B
C
1
Postive
2
Neutral2
3
Neutral1
4
negative
[udc2]
Goto
[udc1]
Goto1
[udc0]
Goto2
Four_level_pi_type_converter_inverter
Scope7
[Iabc]
Iabc
a
b
c


Discrete
1e-06 s.
powergui
A
B
C
N
vabc
iabc
a
b
c
Three-Phase
V-I Measurement1
Uac
Iac
PWMrec
uacL
rectifier signals
positive
Neutral2
Neutral1
negative
rectifier
[Rec_signals]
Goto1
[Modu_rec]
From2
Scope13
[udc2]
Goto4
[udc1]
Goto5
[udc0]
Goto6
Voltage Measurement
Voltage Measurement2
Voltage Measurement3
[Modu_inv]
From3
PWMinv
Postive
Neutral2
Neutral1
negative
inverter signals
inverter
[Inv_signals]
Goto3
[Modu_rec]
Goto
[Modu_inv]
Goto2
Scope1
Scope3
Scope5
Scope8
Scope10
uafinalr
ubfinalr
ucfinalr
uafinali
ubfinali
ucfinali
vtemp
vbuffer
count
iBus_neutral1r
iBus_neutral2r
iBus_neutral1i
iBus_neutral2i
uzerofinali
zeromaxi
zeromini
iBus_neutral_one
iBus_neutral_two
iBus_neutral_three
fcn
Modulation scheme1
urec
uinv
[Rec_signals]
From1
[Inv_signals]
From4
Scope6
[udc2]
[udc1]
[udc0]
From

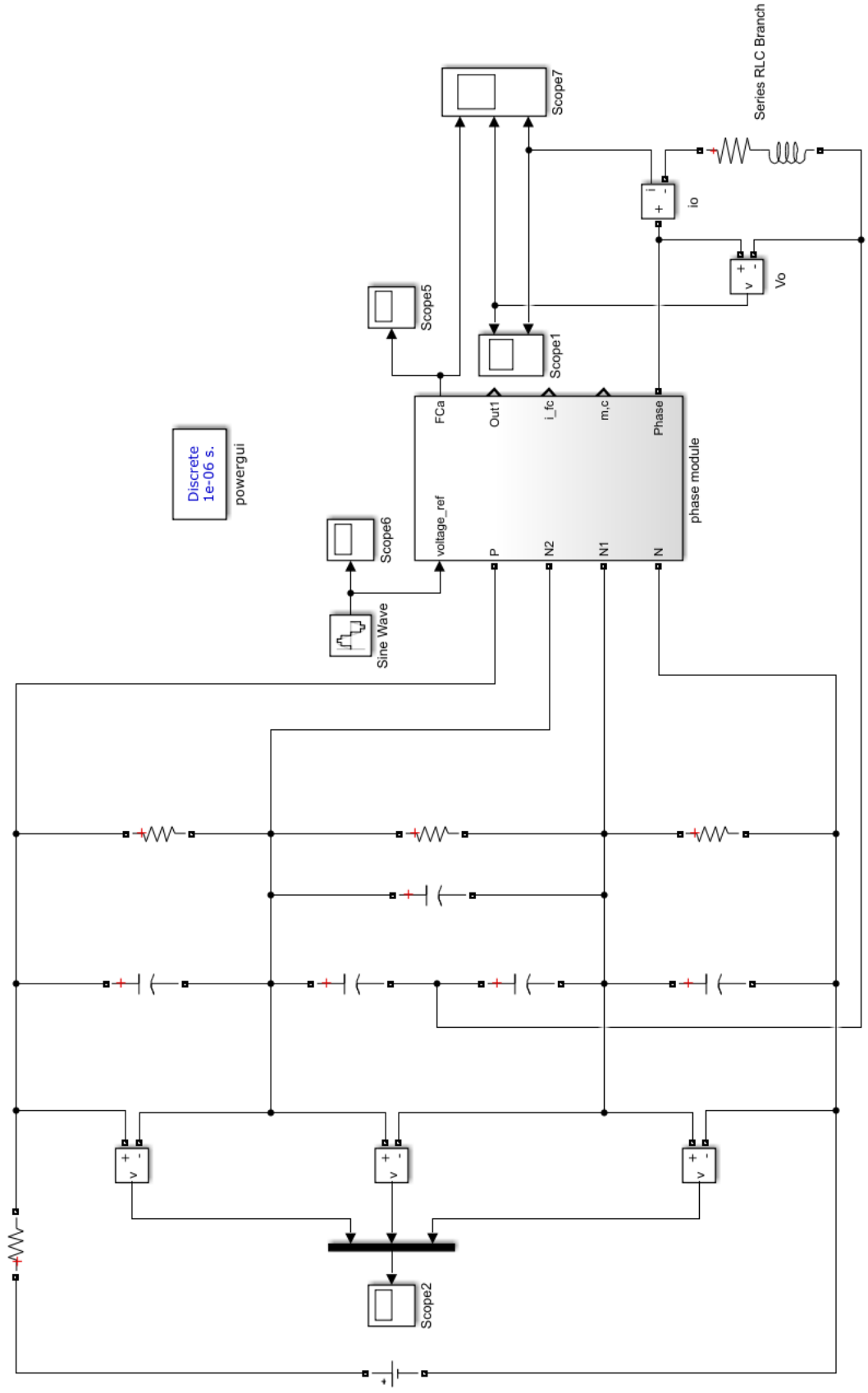

7
C
6
B
1
A
Signal
1
2
Postive
3
Neutral1
4
Neutral2
5
Negative

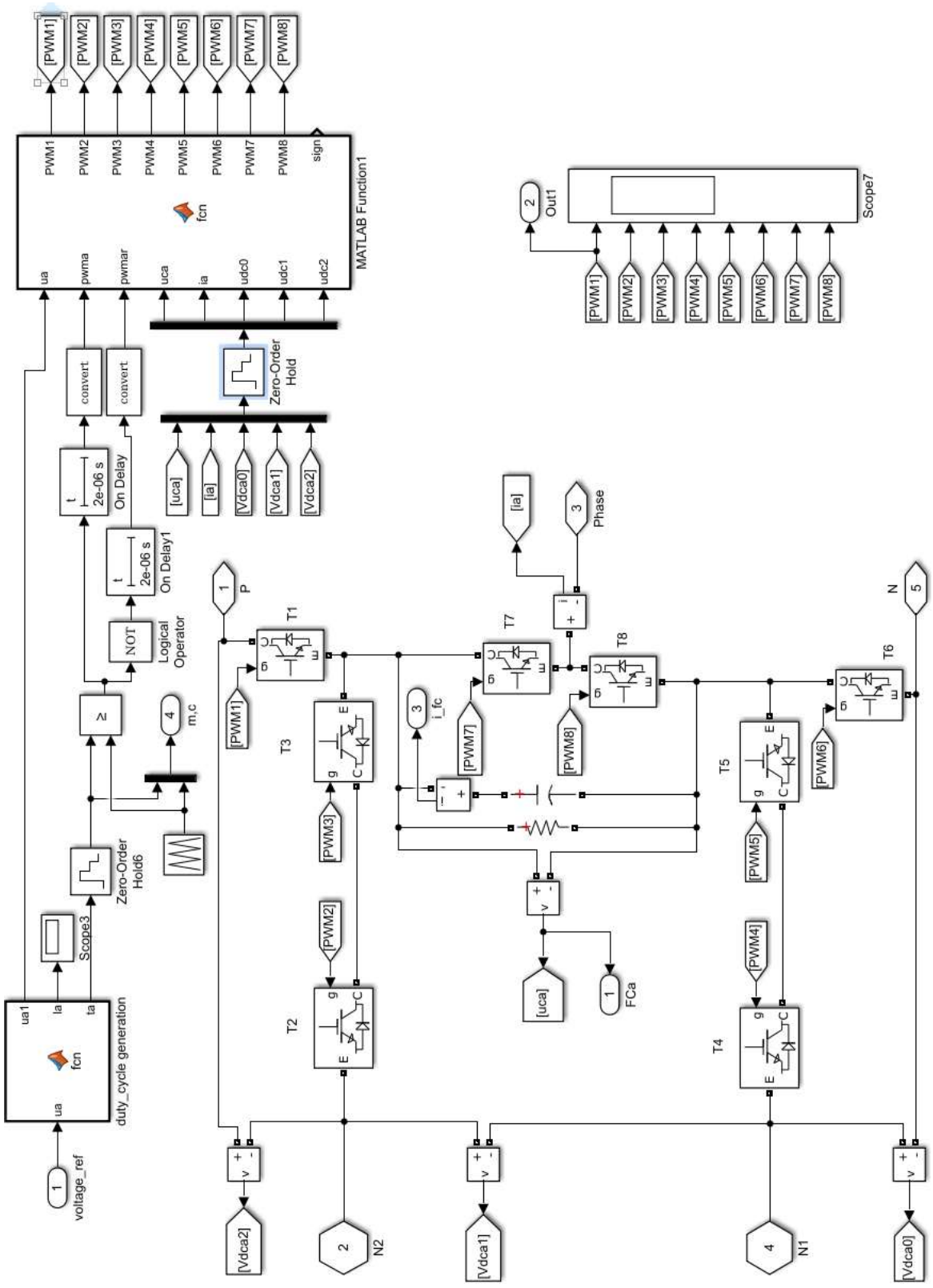
```
function [uafinalr,ubfinalr,ucfinalr,uafinali,ubfinali,ucfinali,vtemp,vbuffer, count,iBus_neutral1r,
iBus_neutral2r, iBus_neutral1i, iBus_neutral2i, uzerofinali, zeromaxi, zeromini, iBus_neutral_one,
iBus_neutral_two, iBus_neutral_three] = fcn(urec,uinv)

valfar=urec(1);   vbetar=urec(2);
iar=urec(3);  ibr=urec(4); icr=urec(5);
udc0=urec(6); udc1=urec(7); udc2=urec(8);

uai=uinv(1);   ubi=uinv(2);uci=uinv(3);
iai=uinv(4);  ibi=uinv(5); ici=uinv(6);

utotal=udc0+udc1+udc2;
uafinalr=0;
ubfinalr=0;
ucfinalr=0;
zeromaxi=0;
zeromini=0;
uzerofinali=0;
uzerofinalr=0;
iBus_neutral1r=0;
iBus_neutral2r=0;
iBus_neutral1i=0;
iBus_neutral2i=0;
iBus_neutral_one=0;
iBus_neutral_two=0;
iBus_neutral_three=0;
Vm1=300*0.866*0.97/sqrt(3);
sucflag=0;
vbuffer=0;
vtemp=0;

   count=0;
   RootofUsr=sqrt(valfar^2+vbetar^2);

  if (RootofUsr>Vm1) % //limit the amplitude
    valfar=valfar/RootofUsr*Vm1;
    vbetar=vbetar/RootofUsr*Vm1;
  end

uar=valfar;
ubr=-0.5*valfar+sqrt(3)/2*vbetar;
ucr=-0.5*valfar-sqrt(3)/2*vbetar;

 vbase=utotal/3;

uar=uar*2/vbase/2;
ubr=ubr*2/vbase/2;
ucr=ucr*2/vbase/2;

uar=uar+1.5;
```

```
ubr=ubr+1.5;
ucr=ucr+1.5;

uai=1.5*uai+1.5;
ubi=1.5*ubi+1.5;    %offset from (-1.5 to 1.5) to (0 to 3)
uci=1.5*uci+1.5;

zeromaxr=3-max([uar,ubr,ucr]);
zerominr=-min([uar,ubr,ucr]);

zeromaxi=3-max([uai,ubi,uci]);
zeromini=-min([uai,ubi,uci]);

 step=0.2;%(zeromaxi-zeromini)/5

 for zeroseqr=zerominr:step:zeromaxr

   for zeroseqi=zeromini:step:zeromaxi

     uanewr=uar+zeroseqr;
     ubnewr=ubr+zeroseqr;
     ucnewr=ucr+zeroseqr;

     uanewi=uai+zeroseqi;
     ubnewi=ubi+zeroseqi;
     ucnewi=uci+zeroseqi;

       lar = floor(uanewr);
       lbr = floor(ubnewr);
       lcr = floor(ucnewr);

       tar = uanewr - lar;
       tbr = ubnewr - lbr;
       tcr = ucnewr - lcr;

       iBus_neutral2r = iar*(tar*(lar == 1) +(1.0 - tar)*(lar == 2))+ ibr*(tbr*(lbr == 1) + (1.0 -
tbr)*(lbr == 2))+ icr*(tcr*(lcr == 1) + (1.0 - tcr)*(lcr == 2));    % higher neutral
       iBus_neutral1r = iar*(tar*(lar == 0) +(1.0 - tar)*(lar == 1))+ ibr*(tbr*(lbr == 0) + (1.0 -
tbr)*(lbr == 1))+ icr*(tcr*(lcr == 0) + (1.0 - tcr)*(lcr == 1));    % lower neutral

       lai = floor(uanewi);
       lbi = floor(ubnewi);
       lci = floor(ucnewi);

       tai = uanewi - lai;
       tbi = ubnewi - lbi;
       tci = ucnewi - lci;

       iBus_neutral2i = iai*(tai*(lai == 1) +(1.0 - tai)*(lai == 2))+ ibi*(tbi*(lbi == 1) + (1.0 -
tbi)*(lbi == 2))+ ici*(tci*(lci == 1) + (1.0 - tci)*(lci == 2));
```

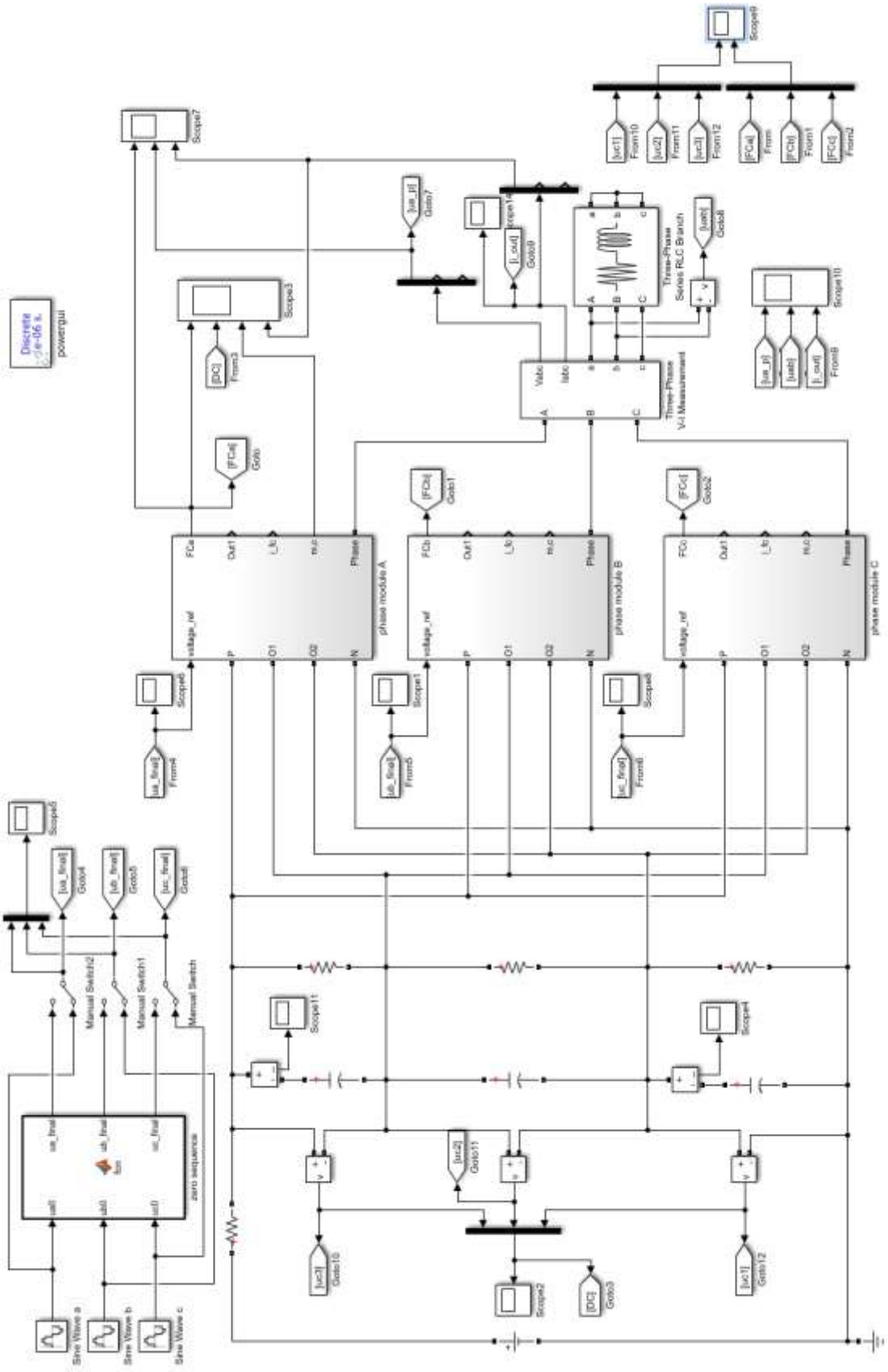
```
        iBus_neutral1i = iai*(tai*(lai == 0) +(1.0 - tai)*(lai == 1))+ ibi*(tbi*(lbi == 0) + (1.0 -
tbi)*(lbi == 1))+ ici*(tci*(lci == 0) + (1.0 - tci)*(lci == 1));

        iBus_neutral_threer = -iBus_neutral2r*2/3-iBus_neutral1r*1/3;        % for upper capacitor
rectifier
        iBus_neutral_twor = iBus_neutral2r*1/3-iBus_neutral1r*1/3;         % for middle capacitor
        iBus_neutral_oner = iBus_neutral2r*1/3+iBus_neutral1r*2/3;     % for lower capacitor

        iBus_neutral_threei = iBus_neutral2i*2/3+iBus_neutral1i*1/3;        % for upper capacitor
//inverter mode
        iBus_neutral_twoi = -iBus_neutral2i*1/3+iBus_neutral1i*1/3;         % for middle capacitor
        iBus_neutral_onei = -iBus_neutral2i*1/3-iBus_neutral1i*2/3;     % for lower capacitor

         iBus_neutral_one = iBus_neutral_oner+iBus_neutral_onei;
         iBus_neutral_two = iBus_neutral_twor+iBus_neutral_twoi;
         iBus_neutral_three = iBus_neutral_threer+iBus_neutral_threei;

        vtemp1 = (udc0-1/3*utotal)*iBus_neutral_one;      % capacitor voltage compared with Vdc/3  lower
        vtemp2 = (udc1-1/3*utotal)*iBus_neutral_two;      % middle capacitor
        vtemp3 = (udc2-1/3*utotal)*iBus_neutral_three;    % upper capacitor

        vtemp = vtemp1+vtemp2+vtemp3;
          if(count <1e-5)
                vbuffer=vtemp;
                uzerofinali = zeroseqi;
                uzerofinalr = zeroseqr;
                count=1;
            end

              if (vtemp <= vbuffer)
                vbuffer = vtemp;
                uzerofinali = zeroseqi;
                uzerofinalr = zeroseqr;
                count=2;
              end
    end
  end
      uafinalr=uar+uzerofinalr;
      ubfinalr=ubr+uzerofinalr;
      ucfinalr=ucr+uzerofinalr;

      uafinali=uai+uzerofinali;
      ubfinali=ubi+uzerofinali;
      ucfinali=uci+uzerofinali;
```

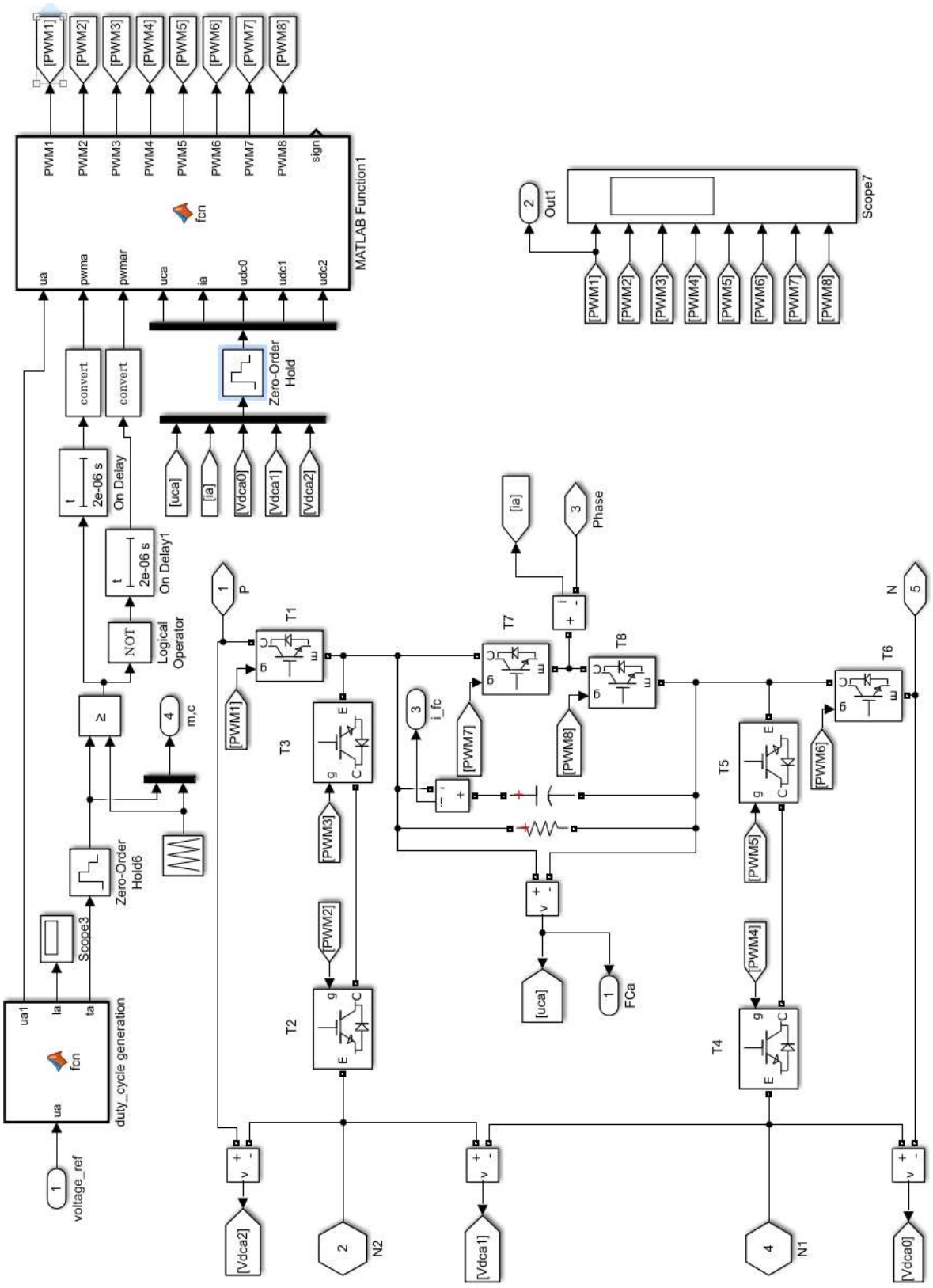
III. Hybrid-clamped four-level π-type converter (single-phase)




[PWM1]
[PWM2]
[PWM3]
[PWM4]
[PWM5]
[PWM6]
[PWM7]
[PWM8]
MATLAB Function1
fcn
ua
pwma
pwmar
uca
ia
udc0
udc1
udc2
sign
Zero-Order Hold
[uca]
[ia]
[Vdca0]
[Vdca1]
[Vdca2]
convert
convert
On Delay
On Delay1
2e-06 s
NOT
Logical Operator
Zero-Order Hold6
Scope3
duty_cycle generation
ua1
la
ta
voltage_ref
Out1
Scope7
Phase
m,c
i_fc
FCa
P
N
N1
N2
T1
T2
T3
T4
T5
T6
T7
T8

IV. Hybrid-clamped four-level π-type converter (three-phase)




[PWM1]
[PWM2]
[PWM3]
[PWM4]
[PWM5]
[PWM6]
[PWM7]
[PWM8]
MATLAB Function1
ua
pwma
pwmar
uca
ia
udc0
udc1
udc2
sign
fcn
Zero-Order Hold
convert
On Delay
On Delay1
2e-06 s
NOT
Logical Operator
Zero-Order Hold6
Scope3
duty_cycle generation
voltage_ref
Scope7
Out1
[uca]
[ia]
[Vdca0]
[Vdca1]
[Vdca2]
Phase
P
N
m,c
i_fc
FCa
N1
N2
T1
T2
T3
T4
T5
T6
T7
T8

```
function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8, sign] = fcn(ua,pwma,pwmar,uca,ia,udc0,udc1,
udc2)
%#codegen

% input uca, ucb, ucc  flying capacitor voltage
% Vdc1, Vdc2 neutral point voltage, vdc1 is the lower capacitor voltage,
% vdc2 is the upper capacitor voltage
% ia, ib, ic output current
% ua, ub, uc reference voltage

% note dc-link voltage set at 600V, flying capacitor voltage set at
% 600/3=200V

capref=(udc0+udc1+udc2)/3;
tolerance=1;

sign=0;
if abs(capref-uca)>1
    sign=1;
else
    sign=0;
end

la=floor(ua);
ta=ua-la;    % output to generate PWM

 utotal=udc0+udc1+udc2;
 fs=10e3;  % switching frequency
%  Rbase=Vbase/Ibase;  % impedence base
 Cap=1.0/(fs*2e-3);    % /*capacitor value 2200uF*/

        PWM1=0;
        PWM2=0;
        PWM3=0;
        PWM4=0;
        PWM5=0;
        PWM6=0;
        PWM7=0;
        PWM8=0;

% inner capacitor balancing Phase A
if ia>0                  % current flowing out
    if (uca-capref)>tolerance    % capacitor voltage is higher
        if la==0          % V1, V3
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v3fcn(pwma,pwmar);
        elseif la==1      % V3, V6
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v3v6fcn(pwma,pwmar);
        elseif la==2       %V6, V8
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v6v8fcn(pwma,pwmar);
        else
```

```
        end
    elseif(uca-capref)<-tolerance   % capacitor voltage is lower
        if la==0              % V1, V4;
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v4fcn(pwma,pwmar);
        elseif la==1          % V4, V7
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v7fcn(pwma,pwmar);
        elseif la==2          % V7, V8
           [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v7v8fcn(pwma,pwmar);
        else
        end
    else                    % capacitor voltage is within the range, neutral point balancing

        if la==0

        iBus_neutral1=ia*ta;  % current flowing out of the lower neutral

        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*ta;  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V1, V4
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v4fcn(pwma,pwmar);
           else                      % choose the lower neutral V1, V2
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v2fcn(pwma,pwmar);
           end

        elseif la==1

        iBus_neutral1=ia*1;  % current flowing out of the lower neutral
```

```
        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);  % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);  % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);  % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*1;  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);  % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);  % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);  % upper capacitor

        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V4, V5
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v5fcn(pwma,pwmar);
           else                      % choose the lower neutral V2, V6
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v2v6fcn(pwma,pwmar);
           end

        elseif la==2
        iBus_neutral1=ia*(1-ta);  % current flowing out of the lower neutral

        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);  % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);  % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);  % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*(1-ta);  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
```

```
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);  % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);  % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);  % upper capacitor

        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V5, V8
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v5v8fcn(pwma,pwmar);
           else                      % choose the lower neutral V6, V8
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v6v8fcn(pwma,pwmar);
           end
        else
        end
    end

elseif ia<=0            % current flowing into
    if (uca-capref)>tolerance   % capacitor voltage is higher
            if la==0    % v1, v4
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v4fcn(pwma,pwmar);
            elseif la==1  % v4, v7
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v7fcn(pwma,pwmar);
            elseif la==2 % v7, v8
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v7v8fcn(pwma,pwmar);
            else
            end
    elseif(uca-capref)<-tolerance   % capacitor voltage is lower
        if la==0    % v1, v3
        [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v3fcn(pwma,pwmar);
        elseif la==1 % v3, v6
        [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v3v6fcn(pwma,pwmar);
        elseif la==2 % v6, v8
        [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v6v8fcn(pwma,pwmar);
        else
        end
    else                % capacitor voltage is within the range, neutral point balancing

         if la==0

        iBus_neutral1=ia*ta;  % current flowing out of the lower neutral

        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);  % capacitor voltage compared with Vdc/3 ↙
lower
```

```
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*ta;  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V1, V4
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v4fcn(pwma,pwmar);
           else                      % choose the lower neutral V1, V2
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v2fcn(pwma,pwmar);
           end

        elseif la==1

        iBus_neutral1=ia*1;  % current flowing out of the lower neutral

        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*1;  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor
```

```
        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V4, V5
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v5fcn(pwma,pwmar);
           else                      % choose the lower neutral V2, V6
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v2v6fcn(pwma,pwmar);
           end

        elseif la==2
        iBus_neutral1=ia*(1-ta);  % current flowing out of the lower neutral

        iBus_neutral_three =iBus_neutral1*1/3;       % for upper capacitor
        iBus_neutral_two = iBus_neutral1*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral1*2/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp = vtemp1+vtemp2+vtemp3;

        iBus_neutral2=ia*(1-ta);  % current flowing out of the upper neutral
        iBus_neutral_three = iBus_neutral2*2/3;       % for upper capacitor
        iBus_neutral_two = -iBus_neutral2*1/3;        % for middle capacitor
        iBus_neutral_one = -iBus_neutral2*1/3;        % for lower capacitor

        vtemp1 = abs(udc0-1/3*utotal+ iBus_neutral_one*Cap);   % capacitor voltage compared with Vdc/3 ↙
lower
        vtemp2 = abs(udc1-1/3*utotal+ iBus_neutral_two*Cap);   % middle capacitor
        vtemp3 = abs(udc2-1/3*utotal+ iBus_neutral_three*Cap);   % upper capacitor

        % 1/3 of the total capacitor
        vtemp_second = vtemp1+vtemp2+vtemp3;

           if vtemp>vtemp_second     % choose the upper neutral V5, V8
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v5v8fcn(pwma,pwmar);
           else                      % choose the lower neutral V6, V8
            [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v6v8fcn(pwma,pwmar);
           end
        else
        end
    end

end

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v2fcn(pwma,pwmar)    % V1,V2
```

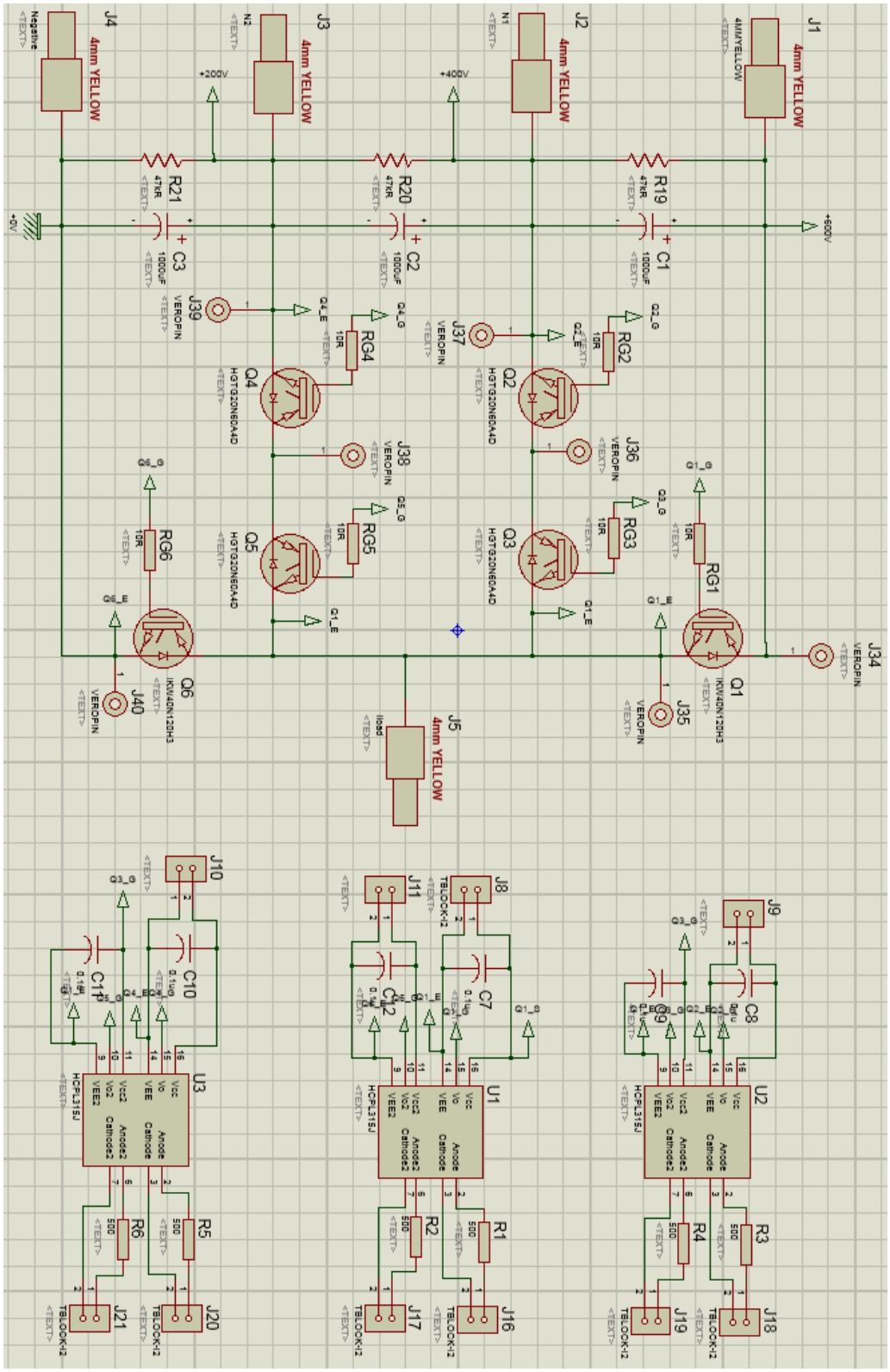
```
            PWM1=0;
            PWM2=0;
            PWM3=0;
          %  PWM4=pwma;
            PWM4=1;
            PWM5=pwma;
            PWM6=pwmar;
            PWM7=0;
            PWM8=1;


function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v3fcn(pwma,pwmar)    % V1,V3
            PWM1=0;
            PWM2=0;
            PWM3=0;
            PWM4=0;
            PWM5=0;
            PWM6=1;
            PWM7=pwma;
            PWM8=pwmar;
function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v1v4fcn(pwma,pwmar)    % V1,V4
            PWM1=0;
          %  PWM2=pwma;
            PWM2=1;
            PWM3=pwma;
            PWM4=0;
            PWM5=0;
            PWM6=pwmar;
            PWM7=0;
            PWM8=1;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v2v6fcn(pwma,pwmar)    % V2,V6
            PWM1=0;
            PWM2=0;
            PWM3=0;
            PWM4=1;
            PWM5=1;
            PWM6=0;
            PWM7=pwma;
            PWM8=pwmar;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v3v6fcn(pwma,pwmar)    % V3,V6
            PWM1=0;
            PWM2=0;
            PWM3=0;
          %  PWM4=pwma;
            PWM4=1;
            PWM5=pwma;
            PWM6=pwmar;
            PWM7=1;
```

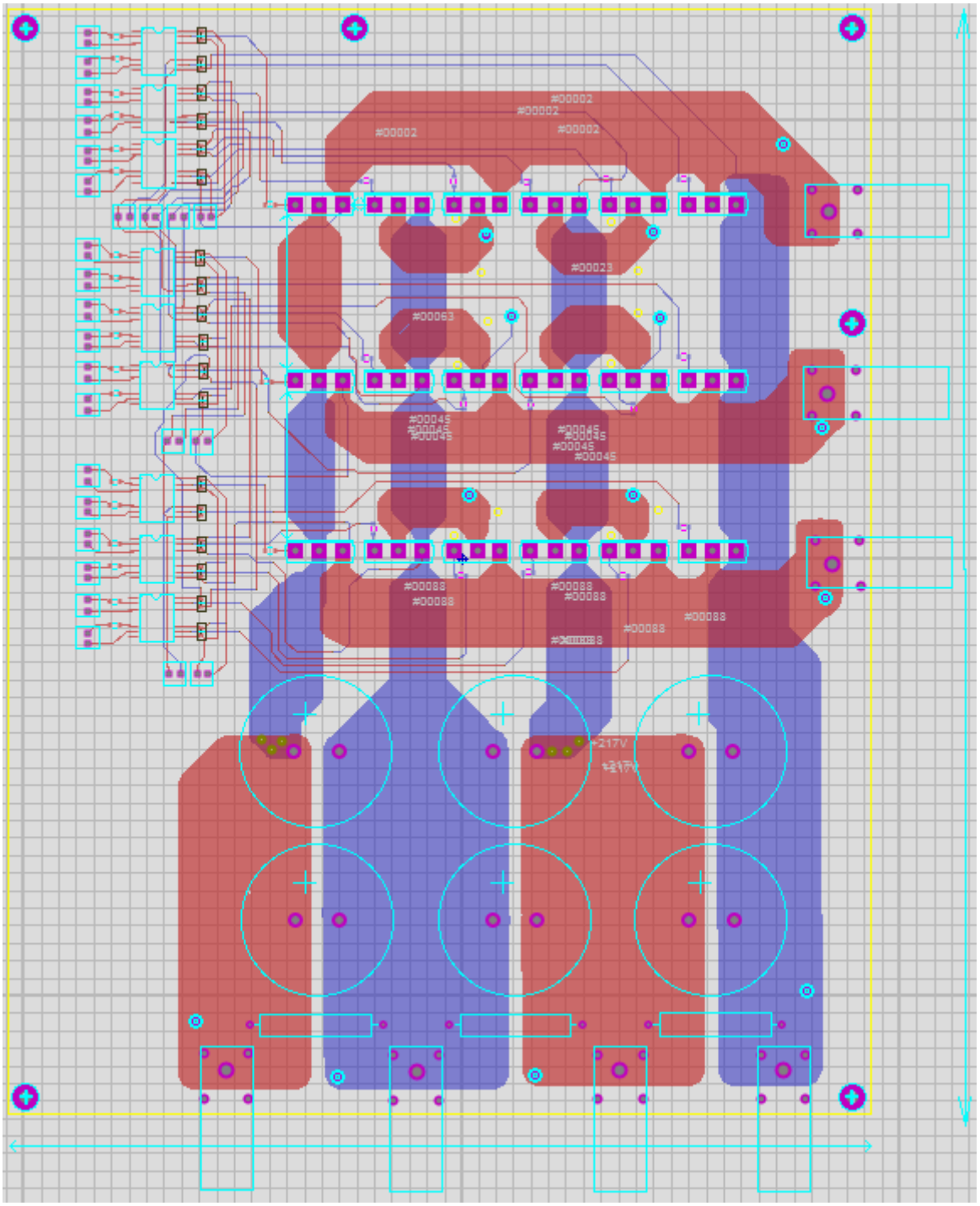
```
            PWM8=0;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v5fcn(pwma,pwmar)    % V4,V5
        PWM1=0;
        PWM2=1;
        PWM3=1;
        PWM4=0;
        PWM5=0;
        PWM6=0;
        PWM7=pwma;
        PWM8=pwmar;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v4v7fcn(pwma,pwmar)    % V4,V7
            PWM1=pwma;
            PWM2=pwmar;
          %   PWM3=pwmar;
            PWM3=1;
            PWM4=0;
            PWM5=0;
            PWM6=0;
            PWM7=0;
            PWM8=1;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v5v8fcn(pwma,pwmar)    % V5,V8
         PWM1=pwma;
         PWM2=pwmar;
        %  PWM3=pwmar;
         PWM3=1;
         PWM4=0;
         PWM5=0;
         PWM6=0;
         PWM7=1;
         PWM8=0;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v6v8fcn(pwma,pwmar)    % V6,V8
            PWM1=pwma;
            PWM2=0;
            PWM3=0;
            PWM4=pwmar;
          %  PWM5=pwmar;
            PWM5=1;
            PWM6=0;
            PWM7=1;
            PWM8=0;

function [PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8]=v7v8fcn(pwma,pwmar)    % V7,V8
        PWM1=1;
        PWM2=0;
        PWM3=0;
        PWM4=0;
```

```
PWM5=0;
PWM6=0;
PWM7=pwma;
PWM8=pwmar;
```

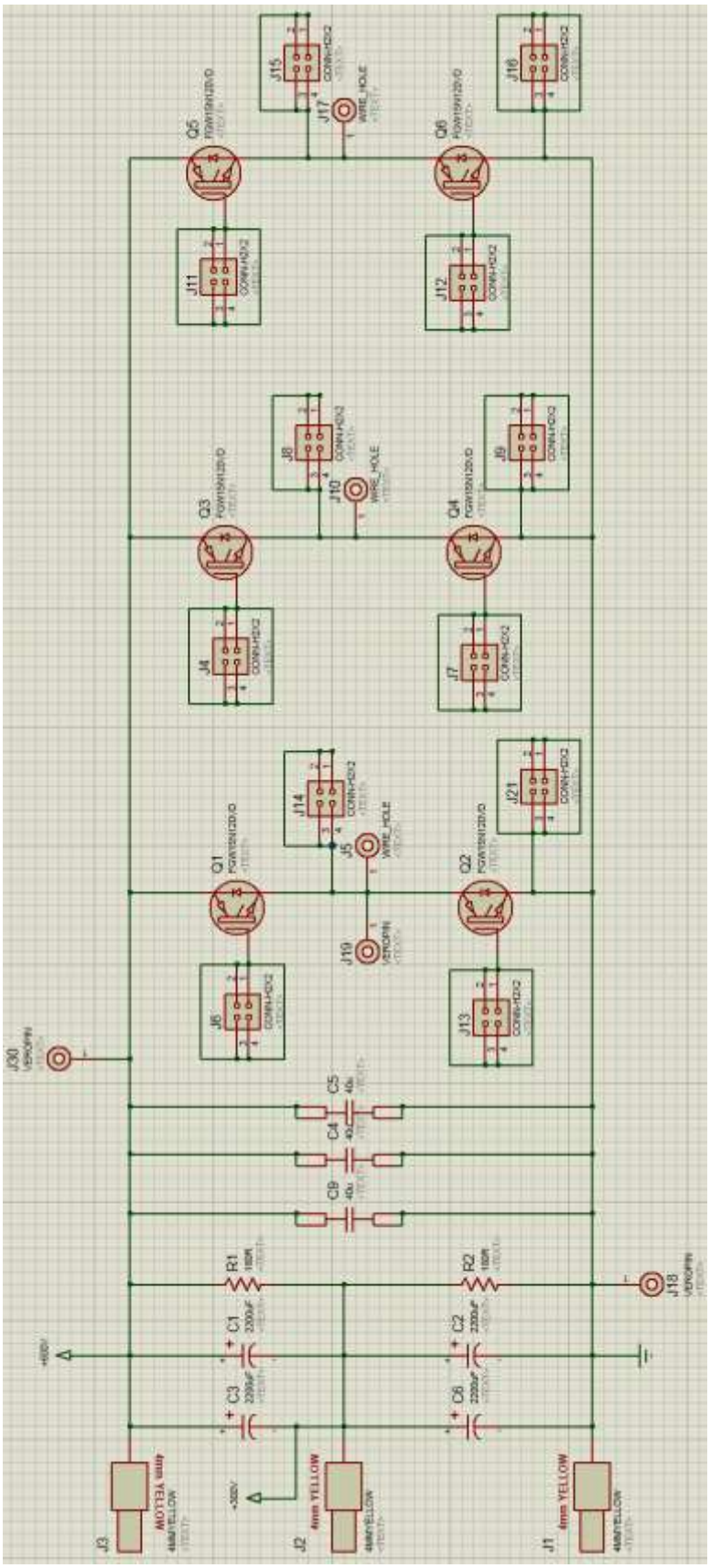
Appendix E. Prototype schematic and PCB layouts

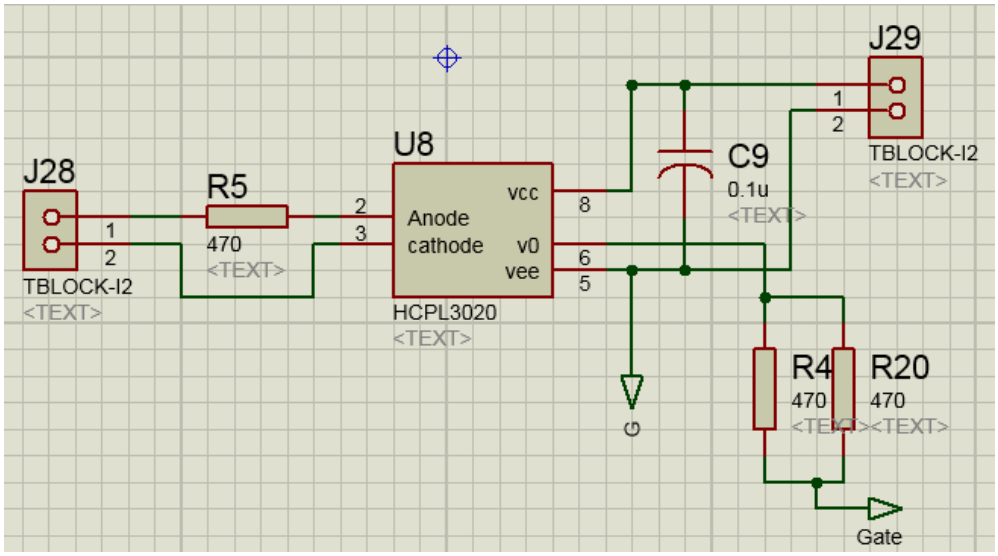
I. Four-level π-type converter

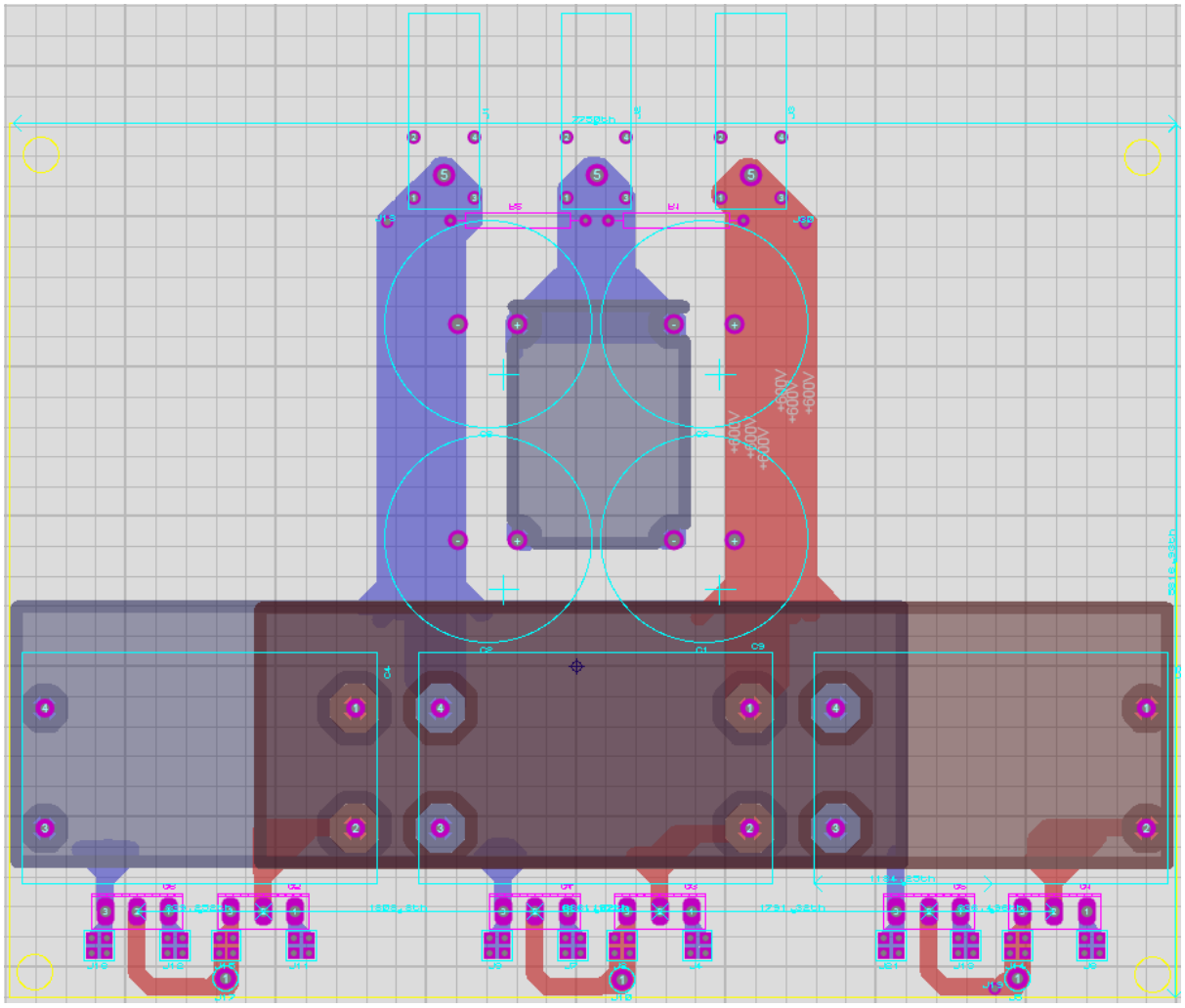


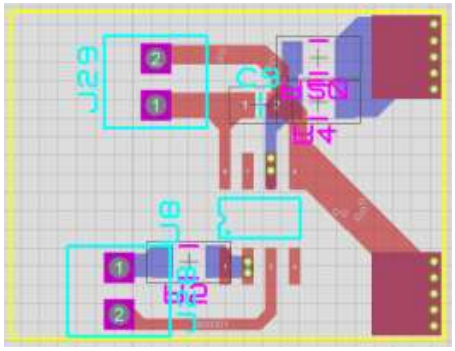

#00002
#00002
#00002
#00002
#00023
#00063
#00045
#00045
#00045
#00045
#00045
#00045
#00088
#00088
#00088
#00088
#00088
+217V

II. Two-level converter

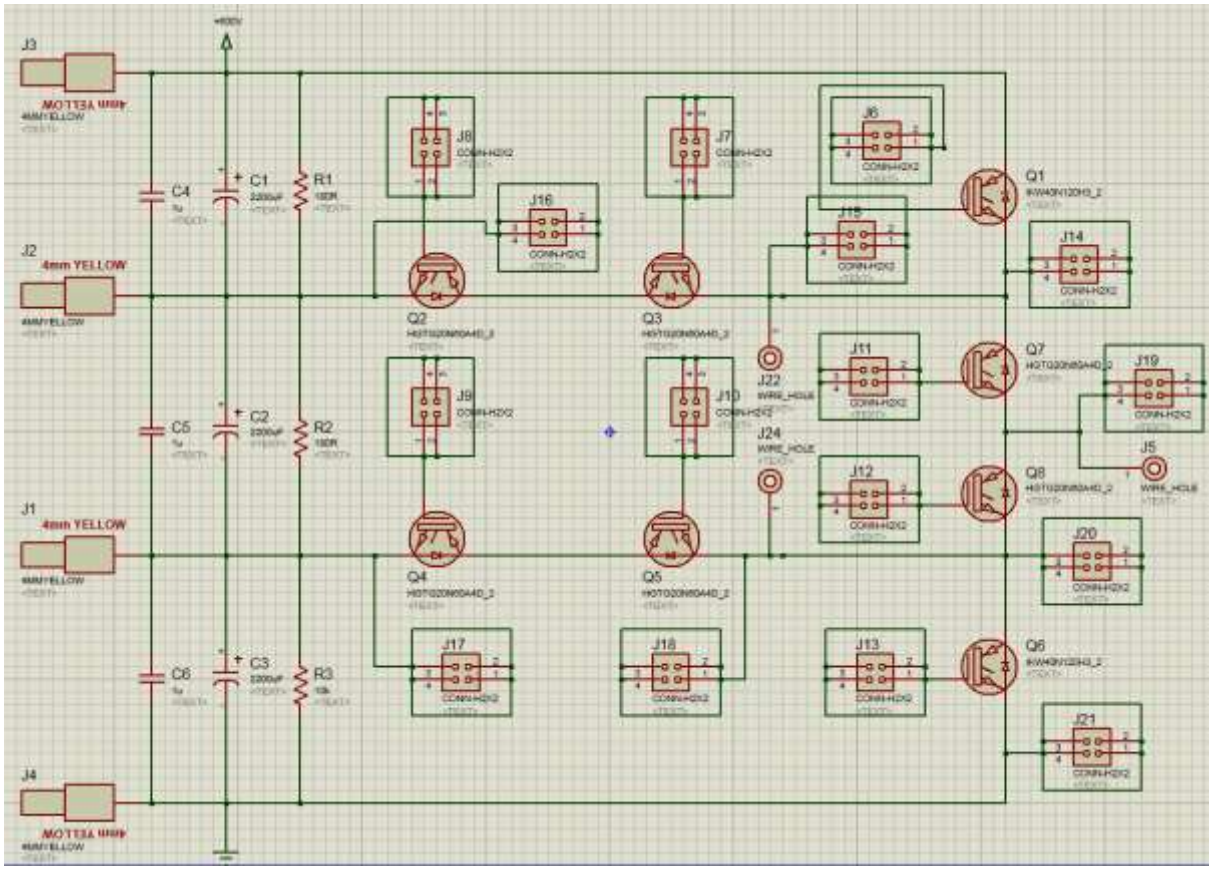


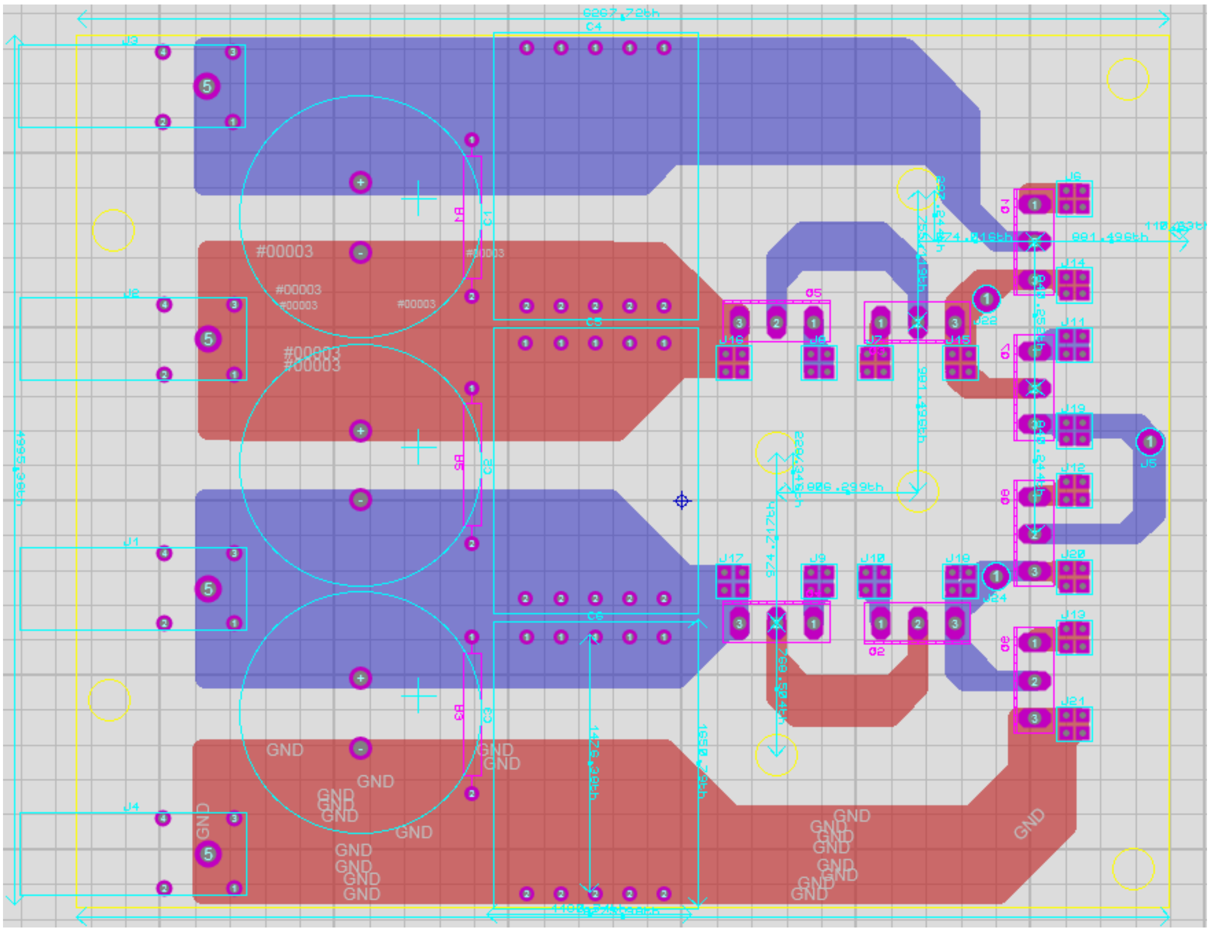

J29
1
2
TBLOCK-I2
<TEXT>
J28
1
2
TBLOCK-I2
<TEXT>
R5
470
<TEXT>
2
3
U8
Anode
cathode
vcc
v0
vee
8
6
5
HCPL3020
<TEXT>
C9
0.1u
<TEXT>
R4
470
R20
470
<TEXT><TEXT>
Gate

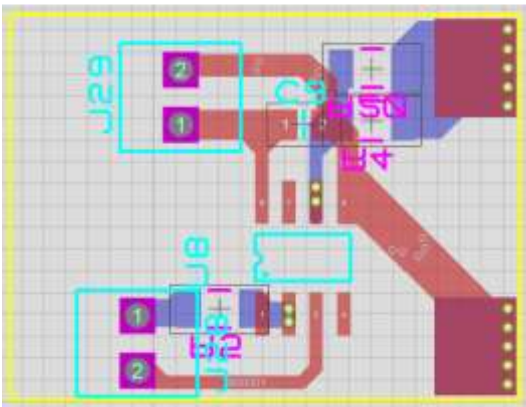




III. Hybrid clamped four-level π-type converter







Appendix F. DSP/FPGA control board related information

I. Code for NP voltages balancing control code for four-level π-type converter (back-to-back configuration)

```
//###########################################################################
// $TI Release: DSP2833x Header Files V1.01 $
// $Release Date: 7-21, 2010 $
//###########################################################################

#include "DSP2833x_Device.h"     // DSP2833x Headerfile Include File
#include "DSP2833x_Examples.h"   // DSP2833x Examples Include File
#include "IQmathLib.h"
#include "PVControl.h"
#include "AD7656_data_Pro.h"
#include "3hclarke.h"
#include "park.h"
#include "ipark.h"
#include "pid_reg3.h"
#include "Xian_Xiang.h"
#include <math.h>
#include <stdio.h>
#include <stdlib.h>
#include <limits.h>
////////////// Interrupt function definiation/////////////
   interrupt void PWM_INT(void);      //carrier wave underflow interrupt
   interrupt void AD_Sample(void);   //AD sampling interrupt

  ///////////////globe variables definition//////////////
   Uint32  EPwmTimerIntCount;//interrupt count

   volatile Uint16 EnableFlag=FALSE;//enable program operation

   int Data_re; //read FPGA data

            float udc1=0;
            float udc2=0;
            float udc3=0;
            float iai=0;
            float ibi=0;
            float ici=0;
            float uai=0;
            float ubi=0;
            float uci=0;
            float uafinali=0;
            float ubfinali=0;
            float ucfinali=0;
            float udc=0;
            float j=0;
            float zeromaxi=0;
            float zeromini=0;
            float maxui=0;
            float minui=0;
            float uanewi=0, ubnewi=0, ucnewi=0;
            int lai=0, lbi=0, lci=0;
            float tai=0, tbi=0, tci=0;
            float ibus_neutral2i=0, ibus_neutral1i=0;
            float ibus_neutral_threei=0, ibus_neutral_twoi=0, ibus_neutral_onei=0;
            float vtemp3=0, vtemp2=0, vtemp1=0;
            float ubuffer = 0;
            float vtemp = 0;
            float uzerofinali = 0;
            int countseq = 0;
            float iar=0;
```

```
60            float ibr=0;
61            float icr=0;
62            float uar=0;
63            float ubr=0;
64            float ucr=0;
65            float uafinalr=0;
66            float ubfinalr=0;
67            float ucfinalr=0;
68             float i=0;
69             float zeromaxr=0;
70             float zerominr=0;
71             float maxur=0;
72             float minur=0;
73             float uanewr=0, ubnewr=0, ucnewr=0;
74             int lar=0, lbr=0, lcr=0;
75             float tar=0, tbr=0, tcr=0;
76             float ibus_neutral2r=0, ibus_neutral1r=0;
77             float ibus_neutral_threer=0, ibus_neutral_twor=0,
   ibus_neutral_oner=0;
78             float uzerofinalr=0;
79             float Angle=0;
80             float ubase=0;
81             float mr=0;
82             float Angle1=0;
83             float uarr=0, ubrr=0, ucrr=0;
84             float Ut=0;
85             float Utmax;
86
87            float ibus_neutral_three=0, ibus_neutral_two=0, ibus_neutral_one=0;
88            float w=2*3.141592654*50;
89            float L=0.005;
90
91//////////////functin definition//////////////
92   CLARKE3H clark1=CLARKE3H_DEFAULTS;  // 3-phase rectifier currents clark
   transformation
93   CLARKE3H clark2=CLARKE3H_DEFAULTS; // 3-phase grid voltage clark transformation
94
95   PARK park1=PARK_DEFAULTS; // 3-phase grid voltage park transformation
96   PARK park2=PARK_DEFAULTS; // 3-phase rectifier currents park transformation
97
98   IPARK ipark1=IPARK_DEFAULTS; // reverse park transformation
99   IPARK ipark2=IPARK_DEFAULTS;
100   XIANXIANG xianxiang=Xian_Xiang_DEFAULTS; //line voltage transfer to phase
   voltage
101
102   PIDREG3 pid1_vdc=PIDREG3_DEFAULTS;//Vdc voltage loop PI configuration
103   PIDREG3 pid1_id=PIDREG3_DEFAULTS;//d-axis current loop PI configuration
104   PIDREG3 pid1_iq=PIDREG3_DEFAULTS;//q-axis current loop PI configuration
105   PIDREG3 pid_Ud1=PIDREG3_DEFAULTS; //Phase lock loop PI configuration
106
107//////////////address pointer//////////////
108   unsigned int * AD_CONVST   = (unsigned int *) 0x4e00;   //AD7656 converion
   initial
109   unsigned int * EN_PWM_int   = (unsigned int *) 0x4f0a;  //enable PWM interrupt
110   unsigned int * DIS_PWM_int   = (unsigned int *) 0x4f0c; //disable PWM interupt
111   unsigned int * TR_FPGA     = (unsigned int *) 0x4ff0;   //data from DSP to FPGA
112   unsigned int * RE_FPGA     = (unsigned int *) 0x4fc0;   //data from FPGA to DSP
113   unsigned int * A_Compare_value  = (unsigned int *) 0x4f03; //inverter phase A
   modualtion signal
```

```
114    unsigned int * B_Compare_value  = (unsigned int *) 0x4f06; //inverter phase B
   modualtion signal
115    unsigned int * C_Compare_value  = (unsigned int *) 0x4f09; //inverter phase C
   modualtion signal
116    unsigned int * RA_Compare_value  = (unsigned int *) 0x4f11; //rectifier phase A
   modualtion signal
117    unsigned int * RB_Compare_value  = (unsigned int *) 0x4f16; //rectifier phase B
   modualtion signal
118    unsigned int * RC_Compare_value  = (unsigned int *) 0x4f12; //rectifier phase C
   modualtion signal
119    unsigned int * EN_Pulse  = (unsigned int *) 0x4fa1; //enable PWM output
120    unsigned int * DIS_Pulse  = (unsigned int *) 0x4fa6; //disable PWM output
121    unsigned int * DA_VOUT1  = (unsigned int *) 0x4d00; //DA5725 analog channel1
122    unsigned int * DA_VOUT2  = (unsigned int *) 0x4d04; //DA5725 analog channel2
123    unsigned int * DA_VOUT3  = (unsigned int *) 0x4d08; //DA5725 analog channel3
124    unsigned int * DA_VOUT4  = (unsigned int *) 0x4d0c; //DA5725 analog channel4
125
126     float sin_a=0;
127     float sin_b=0;
128     float sin_c=0;
129     int sin_i=0;
130     float m=1.1;
131     int amp=2500;
132
133     //Vdc and Iload limits for Vdc = 300 V
134             float Vdc_limit = 135.0;
135             float Iload_limit = 21;
136             AD7656_Pro bosen_ad = AD7656_Pro_DEFAULTS;  //The structure found in
   the AD7656_data_Pro header file is called and given the name apollo_ad.
137                                                          //Then it is made equal
   to the AD7656_Pro_DEFAULTS structure that contains the gain and offset information
   for each variable in the aforementioned structure.
138
139 int ii=0;
140 int hh=0;
141
142 //////////////main function//////////////
143 void main(void)
144 {
145 // Initialize System Control:
146 // PLL, WatchDog, enable Peripheral Clocks
147 // This example function is found in the DSP2833x_SysCtrl.c file.
148     InitSysCtrl();
149
150 // Initalize GPIO:
151    InitScicGpio();
152 // illustrates how to set the GPIO to it's default state.
153 // InitGpio();  // Skipped for this example
154
155 // For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
156 // These functions are in the DSP2833x_EPwm.c file
157    InitEPwmGpio();
158
159 // Clear all interrupts and initialize PIE vector table:
160 // Disable CPU interrupts
161    DINT;
162
163 // Initialize the PIE control registers to their default state.
164 // The default state is all PIE interrupts disabled and flags/// are cleared.
```

```
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();
////////////////////////////////////
   InitXintf();

   //MemCopy(&RamfuncsLoadStart, &RamfuncsLoadEnd, &RamfuncsRunStart);

// Call Flash Initialization to setup flash waitstates
// This function must reside in RAM
   //InitFlash();  //initialize FLASH

   scic_fifo_init();       // Initialize the SCI FIFO

   scic_echoback_init();  // Initalize SCI for echoback

   RS485GpioSet();      //RS485 receive/send control port

// initialize interrupt
   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.XINT2 = &PWM_INT;
   PieVectTable.XINT1 = &AD_Sample;
   EDIS;    // This is needed to disable write to EALLOW protected registers

   EPwmTimerIntCount = 0;  //interrupt count

// configure external interrupt 1 (XINT1), for AD sampling
   EALLOW;
   GpioCtrlRegs.GPAMUX2.bit.GPIO16 = 0;
   GpioCtrlRegs.GPADIR.bit.GPIO16 = 0;
   GpioCtrlRegs.GPAQSEL2.bit.GPIO16 = 2;     // XINT1 Qual using 6 samples
   GpioCtrlRegs.GPACTRL.bit.QUALPRD2 = 0x0a;// sampling period 20*SYSCLKOUT
   GpioIntRegs.GPIOXINT1SEL.bit.GPIOSEL = 16;
   XIntruptRegs.XINT1CR.bit.POLARITY = 0;  //interrupt on falling edge
   XIntruptRegs.XINT1CR.bit.ENABLE = 1;    //enable XINT1
   EDIS;

   IER |= M_INT1;        //enable CPU interrupt 1
   PieCtrlRegs.PIEIER1.bit.INTx5= 1; //enable PIE interrupt 1

// configure external interrupt 2 (XINT2), for triangle wave underflow interrupt
   EALLOW;
   GpioCtrlRegs.GPAMUX2.bit.GPIO17 = 0;
   GpioCtrlRegs.GPADIR.bit.GPIO17 = 0;
   GpioCtrlRegs.GPAQSEL2.bit.GPIO17 = 2;     // XINT2 Qual using 6 samples
   GpioCtrlRegs.GPACTRL.bit.QUALPRD2 = 0x0a;// sampling period 20*SYSCLKOUT
   GpioIntRegs.GPIOXINT2SEL.bit.GPIOSEL = 17;
   XIntruptRegs.XINT2CR.bit.POLARITY = 1;  //interrupt on rising edge
```

```
224    XIntruptRegs.XINT2CR.bit.ENABLE = 1;     //enable XINT2
225    EDIS;
226
227    IER |= M_INT1;         //enable CPU interrupt 1
228    PieCtrlRegs.PIEIER1.bit.INTx4= 1;  //enable PIE interrupt 2
229
230    EALLOW;
231    GpioCtrlRegs.GPBMUX2.bit.GPIO61 = 0;
232    GpioCtrlRegs.GPBDIR.bit.GPIO61 = 1;
233    EDIS;
234
235    pid1_vdc.Kp=_IQ(0.358);//kp=0.358
236    pid1_vdc.Ki=_IQ(36);//ki=36.0527
237    pid1_vdc.Kd=_IQ(0);
238    pid1_vdc.Kc=_IQ(0);
239    pid1_vdc.OutMax=_IQ(10); //pi_vdc output saturate value
240    pid1_vdc.OutMin=_IQ(-20);
241    pid1_vdc.OutMax1=_IQ(10); //ui and up variable saturate value
242    pid1_vdc.OutMin1=_IQ(-20);
243    pid1_vdc.Tc=_IQ(0.00014);
244 //  pid1_vdc.Ref=_IQ(150);
245
246    pid1_id.Kp=_IQ(9);//kp=3.241
247    pid1_id.Ki=_IQ(66);//ki=64
248    pid1_id.Kd=_IQ(0);
249    pid1_id.Kc=_IQ(0);
250    pid1_id.OutMax=_IQ(70);  //
251    pid1_id.OutMin=_IQ(-150);
252    pid1_id.OutMax1=_IQ(70);  //
253    pid1_id.OutMin1=_IQ(-150);
254    pid1_id.Tc=_IQ(0.00014);
255
256    pid1_iq.Kp=_IQ(9);//kp=3.241
257    pid1_iq.Ki=_IQ(66);//ki=64
258    pid1_iq.Kd=_IQ(0);
259    pid1_iq.Kc=_IQ(0);
260    pid1_iq.OutMax=_IQ(70);   //
261    pid1_iq.OutMin=_IQ(-150);
262    pid1_iq.OutMax1=_IQ(70);   //
263    pid1_iq.OutMin1=_IQ(-150);
264    pid1_iq.Tc=_IQ(0.00014);
265
266    pid_Ud1.Kp=_IQ(10);
267    pid_Ud1.Ki=_IQ(0.5);
268    pid_Ud1.Kd=_IQ(0);
269    pid_Ud1.Kc=_IQ(0);
270    pid_Ud1.OutMax=_IQ(10000);
271    pid_Ud1.OutMin=_IQ(-150);
272    pid_Ud1.OutMax1=_IQ(10000);
273    pid_Ud1.OutMin1=_IQ(-150);
274    pid_Ud1.Tc=_IQ(0.0001);
275
276    * EN_PWM_int = 0;       // enbale triangle wave underflow interrupt
277    * EN_Pulse  = 0;
278
279// enable globe interrupt and real time debug interrupt
280    EINT;   // enable globe interrupt INTM
281    ERTM;   // real time debug interrupt DBGM
282
```

```
283 // infinite loop, waiting for interrupt
284    for(;;)
285    {
286
287 ii++;
288 if(ii>=1000)
289 {
290   ii=0;
291 }
292
293    }
294
295 }//end of main
296
297 interrupt void PWM_INT(void)
298 {
299
300 //  GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
301
302        * AD_CONVST=0;          //activate AD conversion
303        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
304
305 }
306
307  interrupt void AD_Sample(void)
308 {
309     // GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
310      //This interrupt starts when the AD7656 is done converting. This is interrupt
    XINT1.
311
312
313         // read =  * RE_FPGA;  // for determining if the XINTF is working
314
315
316         //The function defined in the AD7656_data_Pro source file is called here.
    This function needs to tap into the stucture and the defines found in the
    corresponding header file.
317                                    //The structure and the defines were named
    apollo_ad here, in the main source file.
318                                    //This is where the ADC conversion results are
    read by the DSP and manipulated in the main program, to get a reading of the
    sensed magnitudes.
319        sin_a=m*sin(sin_i*0.005*6.283185306);
320        sin_b=m*sin(sin_i*0.005*6.283185306-2.0944);  //four-level pi-type
321        sin_c=m*sin(sin_i*0.005*6.283185306+2.0944);
322
323   sin_i++;
324   if(sin_i>=200){sin_i=0;}//fundamental period 50ms
325
326 bosen_ad.pro(&bosen_ad);
327        udc1=bosen_ad.Vdc_linka;
328        udc2=bosen_ad.Vdc_linkb;
329        udc3=bosen_ad.Vdc_linkc;
330        udc = udc1 + udc2 + udc3;
331
332        iai=bosen_ad.I_loada;
333        ibi=bosen_ad.I_loadb;
334        ici=bosen_ad.I_loadc;
335
```

```
336        iar=bosen_ad.I_chokear;
337        ibr=bosen_ad.I_chokebr;
338        icr=bosen_ad.I_chokecr;
339
340        if ( bosen_ad.Vdc_linka >= Vdc_limit || bosen_ad.Vdc_linkb >= Vdc_limit ||
   bosen_ad.Vdc_linkc >= Vdc_limit || bosen_ad.I_loada >= Iload_limit||
   bosen_ad.I_loadb >= Iload_limit|| bosen_ad.I_loadc >= Iload_limit ||
   bosen_ad.I_chokear >= Iload_limit || bosen_ad.I_chokebr >= Iload_limit ||
   bosen_ad.I_chokecr >= Iload_limit )
341                                {
342                                    * DIS_Pulse = 1;  //The DIS_PULSE acts on the
   compare_en variable at the FPGA side, which in turn enables or disables the
   generation of the PWM signals.
343                                }
344        //Overload and overvoltage protection.
345                  //The contents of the adresses DIS_Pulse and EN_Pulse don't
   matter; only the fact that they are used in the if command. That's because the
   FPGA reads the actual address on the address bus of the XINTF.
346
347
348        xianxiang.Uab=2*0.2237 * bosen_ad.Vgrid_ab;
349        xianxiang.Ubc=2*0.2237 * bosen_ad.Vgrid_bc;
350        xianxiang.Uca=2*0.2237 * bosen_ad.Vgrid_ca;
351        xianxiang.calc(&xianxiang);
352
353        clark2.As=xianxiang.Ua;
354        clark2.Bs=xianxiang.Ub;
355        clark2.Cs=xianxiang.Uc;
356        clark2.calc(&clark2);
357
358        pid_Ud1.Ref=0;
359        pid_Ud1.Fdb=park1.Qs;
360        pid_Ud1.calc(&pid_Ud1);
361        Wt=-pid_Ud1.Out+_IQ(314.1592654);//pay attention of the sign before
   pid_ud1.Out
362        Ang=Ang+_IQmpy(Wt,_IQ(0.0001));
363        if(Ang>_IQ(3.141592654))
364          {Ang-=_IQ(6.283185308);}
365        else if(Ang<_IQ(-3.141592654))
366          {Ang+=_IQ(6.283185308);}
367        Grid_Ang=Ang;
368
369        Angle=Grid_Ang;
370
371//        * DA_VOUT2 = (unsigned int) (((Angle*0.125)+0.5) * 2457);
372        park1.Alpha=clark2.Alpha;
373        park1.Beta=clark2.Beta;
374        park1.Angle=Angle;
375        park1.calc(&park1);
376
377        clark1.As=iar;
378        clark1.Bs=ibr;
379        clark1.Cs=icr;
380        clark1.calc(&clark1);
381
382        park2.Alpha=clark1.Alpha;
383        park2.Beta=clark1.Beta;
384        park2.Angle=Angle;
385        park2.calc(&park2);
```

```
//       * DA_VOUT3 = (unsigned int) (((Angle*0.125)+0.5) * 2457);
       pid1_vdc.Ref= _IQ(150);
       pid1_vdc.Fdb=udc;
       pid1_vdc.calc(&pid1_vdc);

       pid1_id.Ref=pid1_vdc.Out;
       pid1_id.Fdb=park2.Ds;
       pid1_id.calc(&pid1_id);

       pid1_iq.Ref= _IQ(0);
       pid1_iq.Fdb=park2.Qs;
       pid1_iq.calc(&pid1_iq);

       ipark1.Ds= -pid1_id.Out + (park2.Qs *w*L) + park1.Ds;
       ipark1.Qs= -pid1_iq.Out - (park2.Ds *w*L);
       ipark1.Angle=Angle;
       ipark1.calc(&ipark1);

       uar= ipark1.Alpha;
       ubr= -0.5*ipark1.Alpha+0.866*ipark1.Beta;
       ucr= -0.5*ipark1.Alpha-0.866*ipark1.Beta;

       uar=0.01*uar +1.5;
       ubr=0.01*ubr +1.5;
       ucr=0.01*ucr +1.5;

    uai = sin_a*1.5 +1.5;
    ubi = sin_b*1.5 +1.5;
    uci = sin_c*1.5 +1.5;

    if ((uar)>(ubr)) {
        if((uar)>(ucr)){
            maxur = uar;
        }
        else{
            maxur = ucr;
        }
    }
    else if ((ubr)>(ucr)) {
        maxur = ubr;
    }
    else {
        maxur = ucr;
    }

    if ((uar)<(ubr)) {
        if((uar)<(ucr)){
            minur = uar;
        }
        else{
            minur = ucr;
        }
    }
    else if ((ubr)<(ucr)) {
        minur = ubr;
    }
    else {
        minur = ucr;
    }
```

```
445
446
447     if ((uai)>(ubi)) {
448         if((uai)>(uci)){
449             maxui = uai;
450         }
451         else{
452             maxui = uci;
453         }
454     }
455     else if ((ubi)>(uci)) {
456         maxui = ubi;
457     }
458     else {
459         maxui = uci;
460     }
461
462     if ((uai)<(ubi)) {
463         if((uai)<(uci)){
464             minui = uai;
465         }
466         else{
467             minui = uci;
468         }
469     }
470     else if ((ubi)<(uci)) {
471         minui = ubi;
472     }
473     else {
474         minui = uci;
475     }
476
477     zeromaxr = 3-maxur;
478     zerominr = -minur;
479
480     zeromaxi = 3-maxui;
481     zeromini = -minui;
482
483 //  GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
484     for (i = zerominr ; i<= zeromaxr ;i = i + (zeromaxr-zerominr)*0.4) {
485         for (j = zeromini ; j<= zeromaxi ;j = j + (zeromaxi-zeromini)*0.5) {
486
487         uanewr = uar + i;
488         ubnewr = ubr + i;
489         ucnewr = ucr + i;
490
491         uanewi = uai + j;
492         ubnewi = ubi + j;
493         ucnewi = uci + j;
494
495         lar = floor(uanewr);
496         lbr = floor(ubnewr);
497         lcr = floor(ucnewr);
498
499         tar = uanewr - lar;
500         tbr = ubnewr - lbr;
501         tcr = ucnewr - lcr;
502
503         ibus_neutral2r = iar * (tar * (lar == 1) + (1 - tar) * (lar == 2))+ ibr *
```

```
   (tbr * (lbr == 1) + (1 - tbr) * (lbr == 2))+ icr * (tcr * (lcr == 1) + (1 - tcr) *
   (lcr == 2));
504        ibus_neutral1r = iar * (tar * (lar == 0) + (1 - tar) * (lar == 1))+ ibr *
   (tbr * (lbr == 0) + (1 - tbr) * (lbr == 1))+ icr * (tcr * (lcr == 0) + (1 - tcr) *
   (lcr == 1));
505
506        lai = floor(uanewi);
507        lbi = floor(ubnewi);
508        lci = floor(ucnewi);
509
510        tai = uanewi - lai;
511        tbi = ubnewi - lbi;
512        tci = ucnewi - lci;
513
514        ibus_neutral2i = iai * (tai * (lai == 1) + (1 - tai) * (lai == 2))+ ibi *
   (tbi * (lbi == 1) + (1 - tbi) * (lbi == 2))+ ici * (tci * (lci == 1) + (1 - tci) *
   (lci == 2));
515        ibus_neutral1i = iai * (tai * (lai == 0) + (1 - tai) * (lai == 1))+ ibi *
   (tbi * (lbi == 0) + (1 - tbi) * (lbi == 1))+ ici * (tci * (lci == 0) + (1 - tci) *
   (lci == 1));
516
517        ibus_neutral_three = (-ibus_neutral2r *2*0.3333 - ibus_neutral1r
   *1*0.3333)+(ibus_neutral2i *2*0.3333 + ibus_neutral1i *1*0.3333);
518        ibus_neutral_two = (ibus_neutral2r *1*0.3333 - ibus_neutral1r
   *1*0.3333)+(-ibus_neutral2i *1*0.3333 + ibus_neutral1i *1*0.3333);
519        ibus_neutral_one = (ibus_neutral2r *1*0.3333 + ibus_neutral1r
   *2*0.3333)+(-ibus_neutral2i *1*0.3333 - ibus_neutral1i *2*0.3333);
520
521        vtemp = (udc1 - 0.3333 * udc) * ibus_neutral_one + (udc2 - 0.3333 * udc) *
   ibus_neutral_two + (udc3 - 0.3333 * udc) * ibus_neutral_three;
522
523        if (vtemp <= 0) {
524            ubuffer = vtemp;
525            uzerofinali = j;
526            uzerofinalr = i;
527        }
528        if (vtemp <= ubuffer) {
529            ubuffer = vtemp;
530            uzerofinali = j;
531            uzerofinalr = i;
532        }
533
534  }
535 }
536
537    uafinali = uai + uzerofinali;
538    ubfinali = ubi + uzerofinali;
539    ucfinali = uci + uzerofinali;
540
541    uafinalr = uar + uzerofinalr;
542    ubfinalr = ubr + uzerofinalr;
543    ucfinalr = ucr + uzerofinalr;
544
545    * A_Compare_value =(unsigned int)(uafinali * amp);
546    * B_Compare_value =(unsigned int)(ubfinali * amp);
547    * C_Compare_value =(unsigned int)(ucfinali * amp);
548
549    * RA_Compare_value =(unsigned int)(uafinalr * amp);
550    * RB_Compare_value =(unsigned int)(ubfinalr * amp);
```

```
551     * RC_Compare_value =(unsigned int)(ucfinalr * amp);
552
553  // GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
554
555     * DA_VOUT4 = (unsigned int) (((uafinalr*0.125)) * 2457);
556     * DA_VOUT3 = (unsigned int) (((uar*0.125)) * 2457);
557     * DA_VOUT1 = (unsigned int) (((uzerofinalr*0.125)+0.5) * 2457);
558
559     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
560     return;
561
562 }
563 //===========================================================================
564 // No more.
565 //===========================================================================
566
567
568
```

```
  1  `timescale 1ns / 1ps
  2  //////////////////////////////////////////////////////////////////////////////////
  3  // Company:
  4  // Engineer:
  5  //
  6  // Create Date:    10:36:57 08/31/2011
  7  // Design Name:    lixiaoqiang
  8  // Module Name:    AD_TEST
  9  // Project Name:
 10  // Target Devices:
 11  // Tool versions:
 12  // Description:
 13  //
 14  // Dependencies:
 15  //
 16  // Revision:
 17  // Revision 0.01 - File Created
 18  // Additional Comments: XZCS0
 19  //
 20  //////////////////////////////////////////////////////////////////////////////////
 21  module Top_control(DB,ADDB,XZCS0,XRD,XWE0,ADC_CONVST,ADC_BUSY1,ADC_BUSY2,
 22                     ADC_CS1,ADC_CS2,ADC_RD,RESET_H,clk,XINT1,XINT2,
 23                     DA_CS,DA_WR,DA_LDAC,RESET_L,
 24  //                 pwm1,pwm2,pwm3,pwm4,pwm5,pwm6,
 25                     pwm1,pwm2,pwm3,pwm4,pwm5,pwm6,pwm7,pwm8,pwm9,pwm10,pwm11,pwm12,
    pwm13,pwm14,pwm15,pwm16,pwm17,pwm18,
 26                     pwm19,pwm20,pwm21,pwm22,pwm23,pwm24,pwm25,pwm26,pwm27,pwm28,pwm29,
    pwm30,pwm31,pwm32,pwm33,pwm34,pwm35,pwm36,
 27  //                 Drive_fault1,Drive_fault2,Drive_fault3,
 28  //                 Drive_fault4,Drive_fault5,Drive_fault6,
 29  //
    Contactor_control,Contactor_switch,Stop_button,Run_led,Fault_led,Power_led
 30                     );
 31  ////////////////////input_output define/////////////////////////
 32        input XZCS0;       //DSP side 0 zone select signal(low active)
 33        input XRD;         //DSP side 0 zone read signal(low active)
 34        input XWE0;        //DSP side 0 zone write signal(low active)
 35        input ADC_BUSY1,ADC_BUSY2;         //AD7656_1/2/3 busy signal
 36        input clk;         //FPGA 50M Hz clock
 37  //    input
    Drive_fault1,Drive_fault2,Drive_fault3,Drive_fault4,Drive_fault5,Drive_fault6;//IGB
    T driver fault protection signal
 38        input [19:0] ADDB;       //DSP side 20 bit address bus
 39        input Stop_button;       //stop button
 40  //    input Contactor_switch;   //
 41        output ADC_CONVST;       //AD7656_1/2/3 convert signal
 42        output ADC_CS1, ADC_CS2;           // AD7656_1/2/3 chip select signal
 43        output ADC_RD;           //AD7656_1/2/3 read signal
 44        output RESET_H;          //AD7656_1/2/3 reset signal
 45        output XINT1;            //interrupt for AD7656_1/2/3
 46        output XINT2;            //interrupt for SVPWM
 47        inout [15:0] DB;         //16 bit data bus
 48        output pwm1,pwm2,pwm3,pwm4,pwm5,pwm6,pwm7,pwm8,pwm9,pwm10,pwm11,pwm12,pwm13,
    pwm14,pwm15,pwm16,pwm17,pwm18;//Pulse output pins
 49        output pwm19,pwm20,pwm21,pwm22,pwm23,pwm24,pwm25,pwm26,pwm27,pwm28,pwm29,
```

```
      pwm30,pwm31,pwm32,pwm33,pwm34,pwm35,pwm36;
  50          output DA_CS;              //DA5725 chip select
  51          output DA_WR;              //DA5725 write data signal
  52          output DA_LDAC;            //DA5725 convert signal
  53          output RESET_L;            //DA5725 reset signal
  54    //    output Contactor_control; //contactor control signal(1:on,0:off)
  55    //    output Run_led,Fault_led,Power_led; //led for run,fault,power
  56    ////////////////////variable && data style define ////////////////////////////
  57
  58    //////////DATA BUS Tristate define////////////////////
  59          wire signed [15:0] DB;   //define DB as 16 bit signed data style
  60          wire signed [15:0] input_of_DB;      //DB input reg
  61          wire signed [15:0] output_of_DB;     //DB output reg
  62          reg out_en;    //input or output enable signal for tristate (1:output
      ,0:input)
  63          reg signed [15:0] R_FPGA, T_FPGA,Data_output;   //R_FPGA: DSP =>FPGA
      T_FPGA: DSP<=FPGA
  64
  65    //////////PWM define//////////////////////////
  66          wire A_1,A_2,A_3,A_4,A_5,A_6,B_1,B_2,B_3,B_4,B_5,B_6,C_1,C_2,C_3,C_4,C_5,C_6;
  67          wire RA_1,RA_2,RA_3,RA_4,RA_5,RA_6,RB_1,RB_2,RB_3,RB_4,RB_5,RB_6,RC_1,RC_2,
      RC_3,RC_4,RC_5,RC_6;
  68          wire [15:0] counter;
  69          reg [15:0] A_Compare,B_Compare,C_Compare,RA_Compare,RB_Compare,RC_Compare;
  70          reg [15:0] A_Com,B_Com,C_Com,RA_Com,RB_Com,RC_Com;
  71          reg compare_en;
  72          reg over_flag;
  73          reg XINT2_en;           //PWM interrupt enable:1, disable:0
  74
  75    ////////////////////main code zone//////////////////////////////////////////////
  76
  77    //////////initial zone//////////////////////////////////
  78          initial
  79             begin
  80                out_en = 1'b0;
  81                R_FPGA = 'd0;
  82                T_FPGA = 'd0;
  83                Data_output = 'd0;
  84    //          IGBT_Fault = 'd0;
  85    //          IGBT_count = 'd0;
  86    //          Contactor_output = 'd0;
  87                A_Com= 'd0; B_Com= 'd0; C_Com= 'd0;
  88                RA_Com= 'd0; RB_Com= 'd0; RC_Com= 'd0;
  89    //          A_Compare= 'd15000; B_Compare= 'd15000; C_Compare= 'd15000;
  90                A_Compare= 'd0; B_Compare= 'd0; C_Compare= 'd0;
  91                RA_Compare= 'd0; RB_Compare= 'd0; RC_Compare= 'd0;
  92                over_flag= 'd0;
  93                XINT2_en='d0;
  94                compare_en='d0;
  95             end
  96
  97    //////////DATA BUS Tristate control////////////////////
  98          assign input_of_DB = DB;
  99          assign DB = (out_en==1'b1)? output_of_DB : 16'hzzzz ;
--100
```

```
101   /////////DSP <==> FPGA Communication//////////////////
102         always @(posedge clk)
103            begin
104                  if((ADDB==20'h4fc0)/* || (ADDB==20'h4f55) || (ADDB==20'h4f44)*/)  //
105                  //this three address for AD7656_1/2/3 ,FPGA need AD data for
      calculating,so set the port as input_port
106                     out_en <= 1'b1;           //DB output control port
107                  else
108                     out_en <= 1'b0;          //DB input control port
109            end
110
111   ////////////////////////////////////////
112
113   assign output_of_DB=T_FPGA;   //FPGA upload data to DSP
114
115   /////DSP write to FPGA ///////////////////
116            always @(XWE0)
117            if(XWE0==1'b0 && ADDB==20'h4ff0 && XZCS0==1'b0)
118               begin
119                  R_FPGA <= input_of_DB;
120               end
121   /////DSP read FPGA /////
122            always @(XRD)
123            if(XRD==1'b0 && ADDB==20'h4fc0 && XZCS0==1'b0)//&& ADDB==20'h4fc0
124                  T_FPGA =  16'h0000;
      ////////////////////////Change_Here//////////////////////////////
125            else
126               if(XRD==1'b0 && ADDB==20'h4f55 && XZCS0==1'b0)
127                  T_FPGA = IGBT_Fault;
128               else
129                  if(XRD==1'b0 && ADDB==20'h4f44 && XZCS0==1'b0)
130                     T_FPGA = Contactor_output;
131
132   ////AD7656////
133         AD7656 ADC_control(
134            .clk(clk),.ADDB(ADDB),.XZCS0(XZCS0),.XRD(XRD),
135            .ADC_CONVST(ADC_CONVST),.ADC_BUSY1(ADC_BUSY1),
136            .ADC_BUSY2(ADC_BUSY2),
137            .ADC_CS1(ADC_CS1),.ADC_CS2(ADC_CS2),
138            .ADC_RD(ADC_RD),.RESET_H(RESET_H),.XINT1(XINT1)
139                           );
140
141   //////DA5725////
142         DA5725 DAC_control(
143            .clk(clk),
144            .XWE0(XWE0),
145            .XZCS0(XZCS0),
146            .ADDB(ADDB),
147            .DA_CS(DA_CS),
148            .DA_WR(DA_WR),
149            .DA_LDAC(DA_LDAC),
150            .RESET_L(RESET_L)
151                           );
152
153   //////PWM produce///////
```

```
154   ////enable triangle wave overflow interrup
155         always @(posedge clk)
156            begin
157             if(ADDB==20'h4f0a && XZCS0==1'b0)
158                   XINT2_en='d1;
159             if(ADDB==20'h4f0c && XZCS0==1'b0)
160                   XINT2_en='d0;
161            end
162   ////read modulation wave signals from DSP
163         always @(XWE0)
164             if(XWE0==1'b0 && ADDB==20'h4f11 && XZCS0==1'b0)
165                  begin
166                     RA_Com <= input_of_DB;
167                  end
168
169         always @(XWE0)
170             if(XWE0==1'b0 && ADDB==20'h4f16 && XZCS0==1'b0)
171                  RB_Com <= input_of_DB;
172
173         always @(XWE0)
174             if(XWE0==1'b0 && ADDB==20'h4f12 && XZCS0==1'b0)
175                  begin
176                     RC_Com <= input_of_DB;
177                     over_flag <= 'd1;
178                  end
179               else
180                  over_flag <= 'd0;
181
182         always @(XWE0)
183             if(XWE0==1'b0 && ADDB==20'h4f03 && XZCS0==1'b0)
184                  begin
185                     A_Com <= input_of_DB;
186                  end
187
188         always @(XWE0)
189             if(XWE0==1'b0 && ADDB==20'h4f06 && XZCS0==1'b0)
190                  B_Com <= input_of_DB;
191
192         always @(XWE0)
193             if(XWE0==1'b0 && ADDB==20'h4f09 && XZCS0==1'b0)
194                  begin
195                     C_Com <= input_of_DB;
196                     over_flag <= 'd1;
197                  end
198               else
199                  over_flag <= 'd0;
200
201   ////PWM comparator, generate PWM signals
202         PWM_Generate PWM(
203            .clk(clk),
204            .A_Compare(A_Compare),
205            .B_Compare(B_Compare),
206            .C_Compare(C_Compare),
207            .RA_Compare(RA_Compare),
208            .RB_Compare(RB_Compare),
```

```
209             .RC_Compare(RC_Compare),
210             .counter(counter),
211             .A_1(A_1),.A_2(A_2),.A_3(A_3),.A_4(A_4),.A_5(A_5),.A_6(A_6),.B_1(B_1),.
        B_2(B_2),.B_3(B_3),.B_4(B_4),.B_5(B_5),.B_6(B_6),.C_1(C_1),.C_2(C_2),.C_3(C_3),.
        C_4(C_4),.C_5(C_5),.C_6(C_6),
212             .RA_1(RA_1),.RA_2(RA_2),.RA_3(RA_3),.RA_4(RA_4),.RA_5(RA_5),.RA_6(RA_6),.
        RB_1(RB_1),.RB_2(RB_2),.RB_3(RB_3),.RB_4(RB_4),.RB_5(RB_5),.RB_6(RB_6),.RC_1(RC_1
        ),.RC_2(RC_2),.RC_3(RC_3),.RC_4(RC_4),.RC_5(RC_5),.RC_6(RC_6),
213             .XINT2(XINT2),
214             .XINT2_en(XINT2_en),
215             .compare_en(compare_en)
216                         );
217
218     ////Upon finishing received modulation wave signals, send them to PWM comparator,
        generate PWM signals
219           always @(posedge clk)
220              if(counter == 'd2500)
221                 begin
222                    A_Compare <=A_Com;
223                    B_Compare <=B_Com;
224                    C_Compare <=C_Com;
225                    RA_Compare <=RA_Com;
226                    RB_Compare <=RB_Com;
227                    RC_Compare <=RC_Com;
228                 end
229
230     ////enable/disable PWM output
231           //assign en_signal = (~XWE0 | fault_flag1 | fault_flag2 | fault_flag3 |
        fault_flag4 | fault_flag5 | fault_flag6);
232           always @(posedge clk)
233               if((ADDB==20'h4fa6 && XZCS0==1'b0))
234                         compare_en = 'd0;             //disable PWM output
235                 else
236                 begin
237                    if(ADDB==20'h4fa1 && XZCS0==1'b0)
238                       compare_en = 'd1;               //enable PWM output
239                 end
240
241     ////PWM output
242           assign pwm1 = A_1;
243           assign pwm2 = A_2;
244           assign pwm3 = A_3;
245           assign pwm4 = A_4;
246           assign pwm5 = A_5;
247           assign pwm6 = A_6;
248           assign pwm7 = B_1;
249           assign pwm8 = B_2;
250           assign pwm9 = B_3;
251           assign pwm10 = B_4;
252           assign pwm11 = B_5;
253           assign pwm12 = B_6;
254           assign pwm13 = C_1;
255           assign pwm14 = C_2;
256           assign pwm15 = C_3;
257           assign pwm16 = C_4;
```

```
258         assign pwm17 = C_5;
259         assign pwm18 = C_6;
260         assign pwm19 = RA_1;
261         assign pwm20 = RA_2;
262         assign pwm21 = RA_3;
263         assign pwm22 = RA_4;
264         assign pwm23 = RA_5;
265         assign pwm24 = RA_6;
266         assign pwm25 = RB_1;
267         assign pwm26 = RB_2;
268         assign pwm27 = RB_3;
269         assign pwm28 = RB_4;
270         assign pwm29 = RB_5;
271         assign pwm30 = RB_6;
272         assign pwm31 = RC_1;
273         assign pwm32 = RC_2;
274         assign pwm33 = RC_3;
275         assign pwm34 = RC_4;
276         assign pwm35 = RC_5;
277         assign pwm36 = RC_6;
278
279   endmodule
280
```

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    17:01:09 10/25/2011
7   // Design Name:
8   // Module Name:    PWM_Generate
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21    module PWM_Generate(clk,A_Compare,B_Compare,C_Compare,counter,
22                        RA_Compare,RB_Compare,RC_Compare,
23  //                      A_up,A_down,B_up,B_down,C_up,C_down,
24                        A_1,A_2,A_3,A_4,A_5,A_6,B_1,B_2,B_3,B_4,B_5,B_6,C_1,C_2,C_3,C_4
    ,C_5,C_6,
25                        RA_1,RA_2,RA_3,RA_4,RA_5,RA_6,RB_1,RB_2,RB_3,RB_4,RB_5,RB_6,
    RC_1,RC_2,RC_3,RC_4,RC_5,RC_6,
26                        XINT2,XINT2_en,compare_en
27                       );
28  ////////////////////input_output define/////////////////////////
29        input clk;
30        input [15:0] A_Compare,B_Compare,C_Compare,RA_Compare,RB_Compare,RC_Compare;
31        output counter;
32  //    output A_up,A_down,B_up,B_down,C_up,C_down;
33        output A_1,A_2,A_3,A_4,A_5,A_6,B_1,B_2,B_3,B_4,B_5,B_6,C_1,C_2,C_3,C_4,C_5,
    C_6;
34        output RA_1,RA_2,RA_3,RA_4,RA_5,RA_6,RB_1,RB_2,RB_3,RB_4,RB_5,RB_6,RC_1,RC_2
    ,RC_3,RC_4,RC_5,RC_6;
35        output XINT2;                                  //counter=0 triangle wave
    overflow interrupt
36        input XINT2_en;                               //enable XINT2 output
37        input compare_en;
38  ////////////////////variable && data style define//////////////////////
39  //    parameter PRD = 16'd12500;           //fs=2kHz, IGBT switch period
    PRD=Ts*fm/2=0.0005*50000000/2=12500
40  //    parameter PRD = 16'd5000;           //fs=5kHz, IGBT switch period
    PRD=Ts*fm/2=0.0002*50000000/2=5000
41        parameter PRD = 16'd2500;           //fs=10kHz, IGBT switch period
    PRD=Ts*fm/2=0.0001*50000000/2=2500
42  //    parameter PRD = 16'd1250;            //fs=20kHz, IGBT switch period
    PRD=Ts*fm/2=(1/20000)*50000000/2=1250
43  //    parameter PRD = 16'd834;             //fs=30kHz, IGBT switch period
    PRD=Ts*fm/2=(1/30000)*50000000/2=833
44  //    parameter PRD = 16'd625;             //fs=40kHz, IGBT switch period
PRD=Ts*fm/2=(1/40000)*50000000/2=625
```

```
45    //    parameter PRD = 16'd500;              //fs=50kHz, IGBT switch period
      PRD=Ts*fm/2=(1/50000)*50000000/2=500
46          reg [15:0] counter;                  //produce the triangle wave
47          reg symbol_flag;                     //signed bit of up/down 1:up 0:down
48    //    reg A_up,A_down,B_up,B_down,C_up,C_down;
49          reg A_1,A_2,A_3,A_4,A_5,A_6,B_1,B_2,B_3,B_4,B_5,B_6,C_1,C_2,C_3,C_4,C_5,C_6;
50          reg RA_1,RA_2,RA_3,RA_4,RA_5,RA_6,RB_1,RB_2,RB_3,RB_4,RB_5,RB_6,RC_1,RC_2,
      RC_3,RC_4,RC_5,RC_6;
51    //    reg [1:0] flag_a,flag_b,flag_c;
52    //    reg [7:0] count_a,count_b,count_c,count_a1,count_b1,count_c1;
53          reg [7:0] count_a1,count_a2,count_a3,count_a4,count_a5,count_a6,count_b1,
      count_b2,count_b3,count_b4,count_b5,count_b6,count_c1,count_c2,count_c3,count_c4,
      count_c5,count_c6;
54          reg [7:0] count_ra1,count_ra2,count_ra3,count_ra4,count_ra5,count_ra6,
      count_rb1,count_rb2,count_rb3,count_rb4,count_rb5,count_rb6,count_rc1,count_rc2,
      count_rc3,count_rc4,count_rc5,count_rc6;
55          reg XINT2_flag;
56    //////////initial zone//////////////////////////////
57          initial
58             begin
59                symbol_flag = 1'b1;
60                counter = 16'd0;
61                A_1 = 'b0;
62                A_2 = 'b0;
63                A_3 = 'b0;
64                A_4 = 'b0;
65                A_5 = 'b0;
66                A_6 = 'b0;
67                B_1 = 'b0;
68                B_2 = 'b0;
69                B_3 = 'b0;
70                B_4 = 'b0;
71                A_5 = 'b0;
72                B_6 = 'b0;
73                C_1 = 'b0;
74                C_2 = 'b0;
75                C_3 = 'b0;
76                C_4 = 'b0;
77                C_5 = 'b0;
78                C_6 = 'b0;
79                RA_1 = 'b0;
80                RA_2 = 'b0;
81                RA_3 = 'b0;
82                RA_4 = 'b0;
83                RA_5 = 'b0;
84                RA_6 = 'b0;
85                RB_1 = 'b0;
86                RB_2 = 'b0;
87                RB_3 = 'b0;
88                RB_4 = 'b0;
89                RA_5 = 'b0;
90                RB_6 = 'b0;
91                RC_1 = 'b0;
92                RC_2 = 'b0;
93                RC_3 = 'b0;
```

```
 94              RC_4 = 'b0;
 95              RC_5 = 'b0;
 96              RC_6 = 'b0;
 97              count_a1 = 'd0; count_a2 = 'd0; count_a3 = 'd0; count_a4 = 'd0;
    count_a5 = 'd0; count_a6 = 'd0;
 98              count_b1 = 'd0; count_b2 = 'd0; count_b3 = 'd0; count_b4 = 'd0;
    count_b5 = 'd0; count_b6 = 'd0;
 99              count_c1 = 'd0; count_c2 = 'd0; count_c3 = 'd0; count_c4 = 'd0;
    count_c5 = 'd0; count_c6 = 'd0;
100             count_ra1 = 'd0; count_ra2 = 'd0; count_ra3 = 'd0; count_ra4 = 'd0;
    count_ra5 = 'd0; count_ra6 = 'd0;
101             count_rb1 = 'd0; count_rb2 = 'd0; count_rb3 = 'd0; count_rb4 = 'd0;
    count_rb5 = 'd0; count_rb6 = 'd0;
102             count_rc1 = 'd0; count_rc2 = 'd0; count_rc3 = 'd0; count_rc4 = 'd0;
    count_rc5 = 'd0; count_rc6 = 'd0;
103             XINT2_flag = 1'b0;
104         end
105 ////////////////////main code zone//////////////////////////////////////////////
106
107 ///////generator triangle//////
108       always @(posedge clk)
109          if(symbol_flag == 1'b1)
110             if(counter < PRD)
111                counter = counter + 'd1;
112             else
113                begin
114                   counter = PRD - 'd1;
115                   symbol_flag = 1'b0;
116                   XINT2_flag = 1'b0;
117                end
118          else
119             if(counter > 16'd0)
120                begin
121                   counter = counter - 'd1;
122                   if(counter == 'd0)
123                      XINT2_flag = 1'b1;
124                end
125             else
126                begin
127                   counter = 'd1;
128                   symbol_flag = 1'b1;
129                end
130
131 ///////ÖÐ¶ÏÂö³åÊ¹ÄÜ/////
132       assign XINT2 = (XINT2_en==1'b1)? XINT2_flag : 1'b1 ;
133
134 ///////generator pulse//////
135
136 //Rectifier side//////
137 //A_phase
138 always @(posedge clk)
139          if(compare_en == 'd0)
140             begin
141                RA_1<='d0;
142                RA_2<='d0;
```

```
143                 RA_3<='d0;
144                 RA_4<='d0;
145                 RA_5<='d0;
146                 RA_6<='d0;
147              end
148           else
149              begin
150                 if(RA_Compare>(2*PRD))
151                    begin
152                       RA_3<='d1;
153                       RA_4<='d0;
154                       RA_5<='d1;
155                       RA_6<='d0;
156                       if(counter>(RA_Compare-(2*PRD)))
157                         begin
158                            count_ra1<= 'd0;
159                            RA_1<='d0;
160                            if(count_ra2 == 'd100)
161                               RA_2<='d1;
162                            else
163                               count_ra2<=count_ra2+'d1;
164                         end
165                       else
166                         begin
167                            count_ra2<= 'd0;
168                            RA_2<='d0;
169                            if(count_ra1 == 'd100)
170                               RA_1<='d1;
171                            else
172                               count_ra1<=count_ra1+'d1;
173                         end
174                    end
175                  else if(RA_Compare>PRD)
176                     begin
177                        RA_1<='d0;
178                        RA_2<='d1;
179                        RA_5<='d1;
180                        RA_6<='d0;
181                        if(counter>(RA_Compare-PRD))
182                          begin
183                             count_ra3<= 'd0;
184                             RA_3<='d0;
185                             if(count_ra4 == 'd100)
186                                RA_4<='d1;
187                             else
188                                count_ra4<=count_ra4+'d1;
189                          end
190                        else
191                          begin
192                             count_ra4<= 'd0;
193                             RA_4<='d0;
194                             if(count_ra3 == 'd100)
195                                RA_3<='d1;
196                             else
197                                count_ra3<=count_ra3+'d1;
```

```
198                             end
199                         end
200                     else
201                         begin
202                             RA_1<='d0;
203                             RA_2<='d1;
204                             RA_3<='d0;
205                             RA_4<='d1;
206                             if(counter>RA_Compare)
207                               begin
208                                  count_ra5<= 'd0;
209                                  RA_5<='d0;
210                                  if(count_ra6 == 'd100)
211                                     RA_6<='d1;
212                                  else
213                                     count_ra6<=count_ra6+'d1;
214                               end
215                             else
216                               begin
217                                  count_ra6<= 'd0;
218                                  RA_6<='d0;
219                                  if(count_ra5 == 'd100)
220                                     RA_5<='d1;
221                                  else
222                                     count_ra5<=count_ra5+'d1;
223                               end
224                         end
225                 end
226
227
228   ////B_phase
229   always @(posedge clk)
230             if(compare_en == 'd0)
231                begin
232                   RB_1<='d0;
233                   RB_2<='d0;
234                   RB_3<='d0;
235                   RB_4<='d0;
236                   RB_5<='d0;
237                   RB_6<='d0;
238                end
239             else
240                begin
241                   if(RB_Compare>(2*PRD))
242                      begin
243                         RB_3<='d1;
244                         RB_4<='d0;
245                         RB_5<='d1;
246                         RB_6<='d0;
247                         if(counter>(RB_Compare-(2*PRD)))
248                           begin
249   //                         RB_1<='d0;
250   //                         RB_2<='d1;
251                               count_rb1<= 'd0;
252                               RB_1<='d0;
```

```
253                             if(count_rb2 == 'd100)
254                                RB_2<='d1;
255                             else
256                                count_rb2<=count_rb2+'d1;
257                          end
258                       else
259                          begin
260   //                        RB_1<='d1;
261   //                        RB_2<='d0;
262                             count_rb2<= 'd0;
263                             RB_2<='d0;
264                             if(count_rb1 == 'd100)
265                                RB_1<='d1;
266                             else
267                                count_rb1<=count_rb1+'d1;
268                          end
269                    end
270                 else if(RB_Compare>PRD)
271                    begin
272                       RB_1<='d0;
273                       RB_2<='d1;
274                       RB_5<='d1;
275                       RB_6<='d0;
276                       if(counter>(RB_Compare-PRD))
277                          begin
278   //                        RB_3<='d0;
279   //                        RB_4<='d1;
280                             count_rb3<= 'd0;
281                             RB_3<='d0;
282                             if(count_rb4 == 'd100)
283                                RB_4<='d1;
284                             else
285                                count_rb4<=count_rb4+'d1;
286                          end
287                       else
288                          begin
289   //                        RB_3<='d1;
290   //                        RB_4<='d0;
291                             count_rb4<= 'd0;
292                             RB_4<='d0;
293                             if(count_rb3 == 'd100)
294                                RB_3<='d1;
295                             else
296                                count_rb3<=count_rb3+'d1;
297                          end
298                    end
299                 else
300                    begin
301                       RB_1<='d0;
302                       RB_2<='d1;
303                       RB_3<='d0;
304                       RB_4<='d1;
305                       if(counter>RB_Compare)
306                          begin
307   //                        RB_5<='d0;
```

```
308   //                          RB_6<='d1;
309                               count_rb5<= 'd0;
310                               RB_5<='d0;
311                               if(count_rb6 == 'd100)
312                                  RB_6<='d1;
313                               else
314                                  count_rb6<=count_rb6+'d1;
315                            end
316                         else
317                            begin
318   //                          RB_5<='d1;
319   //                          RB_6<='d0;
320                               count_rb6<= 'd0;
321                               RB_6<='d0;
322                               if(count_rb5 == 'd100)
323                                  RB_5<='d1;
324                               else
325                                  count_rb5<=count_rb5+'d1;
326                            end
327                      end
328                end
329
330
331   ////C_phase
332   always @(posedge clk)
333            if(compare_en == 'd0)
334               begin
335                  RC_1<='d0;
336                  RC_2<='d0;
337                  RC_3<='d0;
338                  RC_4<='d0;
339                  RC_5<='d0;
340                  RC_6<='d0;
341               end
342            else
343               begin
344                  if(RC_Compare>(2*PRD))
345                     begin
346                        RC_3<='d1;
347                        RC_4<='d0;
348                        RC_5<='d1;
349                        RC_6<='d0;
350                        if(counter>(RC_Compare-(2*PRD)))
351                          begin
352   //                        RC_1<='d0;
353   //                        RC_2<='d1;
354                              count_rc1<= 'd0;
355                              RC_1<='d0;
356                              if(count_rc2 == 'd100)
357                                 RC_2<='d1;
358                              else
359                                 count_rc2<=count_rc2+'d1;
360                          end
361                        else
362                          begin
```

```
363   //                          RC_1<='d1;
364   //                          RC_2<='d0;
365                               count_rc2<= 'd0;
366                               RC_2<='d0;
367                               if(count_rc1 == 'd100)
368                                  RC_1<='d1;
369                               else
370                                  count_rc1<=count_rc1+'d1;
371                            end
372                      end
373                   else if(RC_Compare>PRD)
374                      begin
375                         RC_1<='d0;
376                         RC_2<='d1;
377                         RC_5<='d1;
378                         RC_6<='d0;
379                         if(counter>(RC_Compare-PRD))
380                           begin
381   //                         RC_3<='d0;
382   //                         RC_4<='d1;
383                               count_rc3<= 'd0;
384                               RC_3<='d0;
385                               if(count_rc4 == 'd100)
386                                  RC_4<='d1;
387                               else
388                                  count_rc4<=count_rc4+'d1;
389                           end
390                         else
391                           begin
392   //                         RC_3<='d1;
393   //                         RC_4<='d0;
394                               count_rc4<= 'd0;
395                               RC_4<='d0;
396                               if(count_rc3 == 'd100)
397                                  RC_3<='d1;
398                               else
399                                  count_rc3<=count_rc3+'d1;
400                           end
401                      end
402                   else
403                      begin
404                         RC_1<='d0;
405                         RC_2<='d1;
406                         RC_3<='d0;
407                         RC_4<='d1;
408                         if(counter>RC_Compare)
409                           begin
410   //                         RC_5<='d0;
411   //                         RC_6<='d1;
412                               count_rc5<= 'd0;
413                               RC_5<='d0;
414                               if(count_rc6 == 'd100)
415                                  RC_6<='d1;
416                               else
417                                  count_rc6<=count_rc6+'d1;
```

```
418                             end
419                           else
420                             begin
421   //                           RC_5<='d1;
422   //                           RC_6<='d0;
423                               count_rc6<= 'd0;
424                               RC_6<='d0;
425                               if(count_rc5 == 'd100)
426                                  RC_5<='d1;
427                               else
428                                  count_rc5<=count_rc5+'d1;
429                             end
430                       end
431                 end
432
433
434   //Inverter side///////
435   //A_phase
436   always @(posedge clk)
437            if(compare_en == 'd0)
438               begin
439                  A_1<='d0;
440                  A_2<='d0;
441                  A_3<='d0;
442                  A_4<='d0;
443                  A_5<='d0;
444                  A_6<='d0;
445               end
446            else
447               begin
448                  if(A_Compare>(2*PRD))
449                     begin
450                        A_3<='d1;
451                        A_4<='d0;
452                        A_5<='d1;
453                        A_6<='d0;
454                        if(counter>(A_Compare-(2*PRD)))
455                          begin
456                             count_a1<= 'd0;
457                             A_1<='d0;
458                             if(count_a2 == 'd100)
459                                A_2<='d1;
460                             else
461                                count_a2<=count_a2+'d1;
462                          end
463                        else
464                          begin
465                             count_a2<= 'd0;
466                             A_2<='d0;
467                             if(count_a1 == 'd100)
468                                A_1<='d1;
469                             else
470                                count_a1<=count_a1+'d1;
471                          end
472                     end
```

```
473                 else if(A_Compare>PRD)
474                    begin
475                       A_1<='d0;
476                       A_2<='d1;
477                       A_5<='d1;
478                       A_6<='d0;
479                       if(counter>(A_Compare-PRD))
480                         begin
481                            count_a3<= 'd0;
482                            A_3<='d0;
483                            if(count_a4 == 'd100)
484                               A_4<='d1;
485                            else
486                               count_a4<=count_a4+'d1;
487                         end
488                       else
489                         begin
490                            count_a4<= 'd0;
491                            A_4<='d0;
492                            if(count_a3 == 'd100)
493                               A_3<='d1;
494                            else
495                               count_a3<=count_a3+'d1;
496                         end
497                    end
498                 else
499                    begin
500                       A_1<='d0;
501                       A_2<='d1;
502                       A_3<='d0;
503                       A_4<='d1;
504                       if(counter>A_Compare)
505                         begin
506                            count_a5<= 'd0;
507                            A_5<='d0;
508                            if(count_a6 == 'd100)
509                               A_6<='d1;
510                            else
511                               count_a6<=count_a6+'d1;
512                         end
513                       else
514                         begin
515                            count_a6<= 'd0;
516                            A_6<='d0;
517                            if(count_a5 == 'd100)
518                               A_5<='d1;
519                            else
520                               count_a5<=count_a5+'d1;
521                         end
522                    end
523              end
524
525
526
527
```

```
528   //B_phase
529   always @(posedge clk)
530             if(compare_en == 'd0)
531                begin
532                   B_1<='d0;
533                   B_2<='d0;
534                   B_3<='d0;
535                   B_4<='d0;
536                   B_5<='d0;
537                   B_6<='d0;
538                end
539             else
540                begin
541                   if(B_Compare>(2*PRD))
542                      begin
543                         B_3<='d1;
544                         B_4<='d0;
545                         B_5<='d1;
546                         B_6<='d0;
547                         if(counter>(B_Compare-(2*PRD)))
548                           begin
549   //                         B_1<='d0;
550   //                         B_2<='d1;
551                               count_b1<= 'd0;
552                               B_1<='d0;
553                               if(count_b2 == 'd100)
554                                  B_2<='d1;
555                               else
556                                  count_b2<=count_b2+'d1;
557                           end
558                         else
559                           begin
560   //                         B_1<='d1;
561   //                         B_2<='d0;
562                               count_b2<= 'd0;
563                               B_2<='d0;
564                               if(count_b1 == 'd100)
565                                  B_1<='d1;
566                               else
567                                  count_b1<=count_b1+'d1;
568                           end
569                      end
570                   else if(B_Compare>PRD)
571                      begin
572                         B_1<='d0;
573                         B_2<='d1;
574                         B_5<='d1;
575                         B_6<='d0;
576                         if(counter>(B_Compare-PRD))
577                           begin
578   //                         B_3<='d0;
579   //                         B_4<='d1;
580                               count_b3<= 'd0;
581                               B_3<='d0;
582                               if(count_b4 == 'd100)
```

```
583                                 B_4<='d1;
584                              else
585                                 count_b4<=count_b4+'d1;
586                           end
587                        else
588                           begin
589   //                         B_3<='d1;
590   //                         B_4<='d0;
591                              count_b4<= 'd0;
592                              B_4<='d0;
593                              if(count_b3 == 'd100)
594                                 B_3<='d1;
595                              else
596                                 count_b3<=count_b3+'d1;
597                           end
598                     end
599                  else
600                     begin
601                        B_1<='d0;
602                        B_2<='d1;
603                        B_3<='d0;
604                        B_4<='d1;
605                        if(counter>B_Compare)
606                           begin
607   //                         B_5<='d0;
608   //                         B_6<='d1;
609                              count_b5<= 'd0;
610                              B_5<='d0;
611                              if(count_b6 == 'd100)
612                                 B_6<='d1;
613                              else
614                                 count_b6<=count_b6+'d1;
615                           end
616                        else
617                           begin
618   //                         B_5<='d1;
619   //                         B_6<='d0;
620                              count_b6<= 'd0;
621                              B_6<='d0;
622                              if(count_b5 == 'd100)
623                                 B_5<='d1;
624                              else
625                                 count_b5<=count_b5+'d1;
626                           end
627                     end
628               end
629
630
631   //C_phase
632   always @(posedge clk)
633            if(compare_en == 'd0)
634               begin
635                  C_1<='d0;
636                  C_2<='d0;
637                  C_3<='d0;
```

```
638                 C_4<='d0;
639                 C_5<='d0;
640                 C_6<='d0;
641              end
642           else
643              begin
644                 if(C_Compare>(2*PRD))
645                    begin
646                       C_3<='d1;
647                       C_4<='d0;
648                       C_5<='d1;
649                       C_6<='d0;
650                       if(counter>(C_Compare-(2*PRD)))
651                         begin
652   //                       C_1<='d0;
653   //                       C_2<='d1;
654                            count_c1<= 'd0;
655                            C_1<='d0;
656                            if(count_c2 == 'd100)
657                               C_2<='d1;
658                            else
659                               count_c2<=count_c2+'d1;
660                         end
661                       else
662                         begin
663   //                       C_1<='d1;
664   //                       C_2<='d0;
665                            count_c2<= 'd0;
666                            C_2<='d0;
667                            if(count_c1 == 'd100)
668                               C_1<='d1;
669                            else
670                               count_c1<=count_c1+'d1;
671                         end
672                    end
673                 else if(C_Compare>PRD)
674                    begin
675                       C_1<='d0;
676                       C_2<='d1;
677                       C_5<='d1;
678                       C_6<='d0;
679                       if(counter>(C_Compare-PRD))
680                         begin
681   //                       C_3<='d0;
682   //                       C_4<='d1;
683                            count_c3<= 'd0;
684                            C_3<='d0;
685                            if(count_c4 == 'd100)
686                               C_4<='d1;
687                            else
688                               count_c4<=count_c4+'d1;
689                         end
690                       else
691                         begin
692   //                       C_3<='d1;
```

```
693   //                          C_4<='d0;
694                               count_c4<= 'd0;
695                               C_4<='d0;
696                               if(count_c3 == 'd100)
697                                  C_3<='d1;
698                               else
699                                  count_c3<=count_c3+'d1;
700                            end
701                      end
702                   else
703                      begin
704                         C_1<='d0;
705                         C_2<='d1;
706                         C_3<='d0;
707                         C_4<='d1;
708                         if(counter>C_Compare)
709                           begin
710   //                         C_5<='d0;
711   //                         C_6<='d1;
712                               count_c5<= 'd0;
713                               C_5<='d0;
714                               if(count_c6 == 'd100)
715                                  C_6<='d1;
716                               else
717                                  count_c6<=count_c6+'d1;
718                            end
719                         else
720                           begin
721   //                         C_5<='d1;
722   //                         C_6<='d0;
723                               count_c6<= 'd0;
724                               C_6<='d0;
725                               if(count_c5 == 'd100)
726                                  C_5<='d1;
727                               else
728                                  count_c5<=count_c5+'d1;
729                            end
730                      end
731                end
732
733
734   endmodule
735
```

II. Code for NP voltage and FC voltage balancing control code for hybrid clamped four-level π-type converter

```
//###########################################################################
// $TI Release: DSP2833x Header Files V1.01 $
// $Release Date: 7-21, 2010 $
//###########################################################################

#include "DSP2833x_Device.h"     // DSP2833x Headerfile Include File
#include "DSP2833x_Examples.h"   // DSP2833x Examples Include File
#include "IQmathLib.h"
#include "PVControl.h"
#include "AD7656_data_Pro.h"
#include "3hclarke.h"
#include "park.h"
#include "ipark.h"
#include "pid_reg3.h"
#include "Xian_Xiang.h"
#include <math.h>
#include <stdio.h>
#include <stdlib.h>
#include <limits.h>
/////////////// Interrupt function definiation///////////////
   interrupt void PWM_INT(void);      //carrier wave underflow interrupt
   interrupt void AD_Sample(void);   //AD sampling interrupt

   volatile Uint16 EnableFlag=FALSE;//enable program operation

   ///////////////globe variables definition///////////////
   long delay_count=0;  //delay count
   int Data_re; //saving FPGA uploaded data

            float udc1=0;
            float udc2=0;
            float udc3=0;
            float iai=0;
            float uai=0;
            float udc=0;
            int lai=0, lbi=0, lci=0;
            float tai=0, tbi=0, tci=0;
            float ibus_neutral2i=0, ibus_neutral1i=0;
            float ibus_neutral_threei=0, ibus_neutral_twoi=0, ibus_neutral_onei=0;
            float vtemp3=0, vtemp2=0, vtemp1=0;
            float ubuffer = 0;
            float vtemp = 0;
            float vtemp_second = 0;
            float uzerofinali = 0;
            int countseq = 0;

            float ibus_neutral_three=0, ibus_neutral_two=0, ibus_neutral_one=0;
            float w=2*3.141592654*50;
            float L=0.005;
            float ufc=0;
            float capref=0;
            float tolerance=1;
            float cap=/*0.02475*/0.04950495; //1/[(2020e-6)*(10e3)]

///////////////address pointer///////////////
   unsigned int * AD_CONVST   = (unsigned int *) 0x4e00;   //AD7656 conversion
  start
   unsigned int * EN_PWM_int   = (unsigned int *) 0x4f0a;  //Enable PWM interrupt
   unsigned int * DIS_PWM_int   = (unsigned int *) 0x4f0c; //Disable PWM interrupt
```

```
59    unsigned int * TR_FPGA     = (unsigned int *) 0x4ff0;   //DSP send data to FPGA
60    unsigned int * RE_FPGA     = (unsigned int *) 0x4fc0;   //FPGA upload data to
  DSP
61    unsigned int * A_Compare_value  = (unsigned int *) 0x4f03; //Phase A modulation
  signal
62    unsigned int * B_Compare_value  = (unsigned int *) 0x4f06; //Phase B modulation
  signal
63    unsigned int * C_Compare_value  = (unsigned int *) 0x4f09; //Phase C modulation
  signal
64    unsigned int * EN_Pulse  = (unsigned int *) 0x4fa1; //Enable pulse output
65    unsigned int * DIS_Pulse  = (unsigned int *) 0x4fa6; //Disable pulse output
66    unsigned int * DA_VOUT1  = (unsigned int *) 0x4d00; //DA5725 analog channel
  address 1
67    unsigned int * DA_VOUT2  = (unsigned int *) 0x4d04; //DA5725 analog channel
  address 2
68    unsigned int * DA_VOUT3  = (unsigned int *) 0x4d08; //DA5725 analog channel
  address 3
69    unsigned int * DA_VOUT4  = (unsigned int *) 0x4d0c; //DA5725 analog channel
  address 4
70
71    unsigned int * SW_V13 = (unsigned int*) 0x4f11;
72    unsigned int * SW_V36 = (unsigned int*) 0x4f16;
73    unsigned int * SW_V68 = (unsigned int*) 0x4fb6;
74    unsigned int * SW_V14 = (unsigned int*) 0x4fb1;
75    unsigned int * SW_V47 = (unsigned int*) 0x4fbc;
76    unsigned int * SW_V78 = (unsigned int*) 0x4fba;
77    unsigned int * SW_V12 = (unsigned int*) 0x4fac;
78    unsigned int * SW_V45 = (unsigned int*) 0x4faa;
79    unsigned int * SW_V26 = (unsigned int*) 0x4f12;
80    unsigned int * SW_V58 = (unsigned int*) 0x4fe1;
81    unsigned int * DIS_SW_V13 = (unsigned int*) 0x4f22;
82    unsigned int * DIS_SW_V36 = (unsigned int*) 0x4f33;
83    unsigned int * DIS_SW_V68 = (unsigned int*) 0x4f66;
84    unsigned int * DIS_SW_V14 = (unsigned int*) 0x4f77;
85    unsigned int * DIS_SW_V47 = (unsigned int*) 0x4f88;
86    unsigned int * DIS_SW_V78 = (unsigned int*) 0x4f99;
87    unsigned int * DIS_SW_V12 = (unsigned int*) 0x4f21;
88    unsigned int * DIS_SW_V45 = (unsigned int*) 0x4f31;
89    unsigned int * DIS_SW_V26 = (unsigned int*) 0x4f41;
90    unsigned int * DIS_SW_V58 = (unsigned int*) 0x4f51;
91
92     float sin_a=0;
93     float sin_b=0;
94     float sin_c=0;
95     int sin_i=0;
96     float m=0.95;
97     int amp=2500;
98 //Vdc and Iload limits for Vdc = 600 V for now.
99             float Vdc_limit = 130.0;
100            float Iload_limit = 12.0;
101            float Vfc_limit = 110.0;
102            AD7656_Pro bosen_ad = AD7656_Pro_DEFAULTS;  //The structure found in
   the AD7656_data_Pro header file is called and given the name apollo_ad.
103                                                         //Then it is made equal
   to the AD7656_Pro_DEFAULTS structure that contains the gain and offset information
   for each variable in the aforementioned structure.
104
105 int ii=0;
106 int hh=0;
```

```
107
108 //////////////main function//////////////
109 void main(void)
110 {
111 // Initialize System Control:
112 // PLL, WatchDog, enable Peripheral Clocks
113 // This example function is found in the DSP2833x_SysCtrl.c file.
114     InitSysCtrl();
115
116 // Initalize GPIO:
117    InitScicGpio();
118 // illustrates how to set the GPIO to it's default state.
119 // InitGpio();  // Skipped for this example
120
121 // For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
122 // These functions are in the DSP2833x_EPwm.c file
123    InitEPwmGpio();
124
125 // Clear all interrupts and initialize PIE vector table:
126 // Disable CPU interrupts
127    DINT;
128
129 // Initialize the PIE control registers to their default state.
130 // The default state is all PIE interrupts disabled and flags/// are cleared.
131 // This function is found in the DSP2833x_PieCtrl.c file.
132    InitPieCtrl();
133
134 // Disable CPU interrupts and clear all CPU interrupt flags:
135    IER = 0x0000;
136    IFR = 0x0000;
137
138 // Initialize the PIE vector table with pointers to the shell Interrupt
139 // Service Routines (ISR).
140 // This will populate the entire table, even if the interrupt
141 // is not used in this example.  This is useful for debug purposes.
142 // The shell ISR routines are found in DSP2833x_DefaultIsr.c.
143 // This function is found in DSP2833x_PieVect.c.
144    InitPieVectTable();
145 ////////////////////////////////////
146    InitXintf();
147
148    //MemCopy(&RamfuncsLoadStart, &RamfuncsLoadEnd, &RamfuncsRunStart);
149
150 // Call Flash Initialization to setup flash waitstates
151 // This function must reside in RAM
152    //InitFlash();  //initialize FLASH
153
154    scic_fifo_init();       // Initialize the SCI FIFO
155
156    scic_echoback_init();  // Initalize SCI for echoback
157
158    RS485GpioSet();      //RS485 receive/send control port
159
160 // interrupt initialization
161    EALLOW;  // This is needed to write to EALLOW protected registers
162    PieVectTable.XINT2 = &PWM_INT;
163    PieVectTable.XINT1 = &AD_Sample;
164    EDIS;    // This is needed to disable write to EALLOW protected registers
165
```

```
166    EPwmTimerIntCount = 0;  //interrupt count
167
168 // arrange XINT1, for AD sampling
169    EALLOW;
170    GpioCtrlRegs.GPAMUX2.bit.GPIO16 = 0;
171    GpioCtrlRegs.GPADIR.bit.GPIO16 = 0;
172    GpioCtrlRegs.GPAQSEL2.bit.GPIO16 = 2;     // XINT1 Qual using 6 samples
173    GpioCtrlRegs.GPACTRL.bit.QUALPRD2 = 0x0a;// each sampling period 20*SYSCLKOUT
174    GpioIntRegs.GPIOXINT1SEL.bit.GPIOSEL = 16;
175    XIntruptRegs.XINT1CR.bit.POLARITY = 0;  //interrupt generated on a falling edge
176    XIntruptRegs.XINT1CR.bit.ENABLE = 1;    //enable XINT1
177    EDIS;
178
179    IER |= M_INT1;        //enable CPU interrupt 1
180    PieCtrlRegs.PIEIER1.bit.INTx5= 1; //enable PIE interrupt 1
181
182
183 // Arrange XINT2, for triangle wave overflow interrupt
184    EALLOW;
185    GpioCtrlRegs.GPAMUX2.bit.GPIO17 = 0;
186    GpioCtrlRegs.GPADIR.bit.GPIO17 = 0;
187    GpioCtrlRegs.GPAQSEL2.bit.GPIO17 = 2;     // XINT2 Qual using 6 samples
188    GpioCtrlRegs.GPACTRL.bit.QUALPRD2 = 0x0a;// each sampling period 20*SYSCLKOUT
189    GpioIntRegs.GPIOXINT2SEL.bit.GPIOSEL = 17;
190    XIntruptRegs.XINT2CR.bit.POLARITY = 1;  //interrupt genereated on a rising edge
191    XIntruptRegs.XINT2CR.bit.ENABLE = 1;    //enable XINT2
192
193    IER |= M_INT1;        //enable CPU interrupt1
194    PieCtrlRegs.PIEIER1.bit.INTx4= 1;  //Enable PIE interrupt2
195
196 EALLOW;
197 GpioCtrlRegs.GPBMUX2.bit.GPIO61 = 0;
198 GpioCtrlRegs.GPBDIR.bit.GPIO61 = 1;
199 EDIS;
200
201    * EN_PWM_int = 0;       // enable triangle wave overflow interrupt
202    * EN_Pulse  = 0;
203
204 // Enable global interrupts and higher priority real-time debug events
205    EINT;   // Enable global interrupt INTM
206    ERTM;   // Enable Global realtime interrupt DBGM
207
208
209 // infinite loop, wait for interrupt (optional)
210    for(;;)
211    {
212
213 ii++;
214 if(ii>=500)
215 {
216   ii=0;
217 }
218
219    }
220
221 }//end of main
222
223 interrupt void PWM_INT(void)
224 {
```

```
225
226 GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
227        * AD_CONVST=0;          //activate AD conversion
228        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
229
230 }
231
232  interrupt void AD_Sample(void)
233 {
234
235      GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
236 //   test--;
237      //This interrupt starts when the AD7656 is done converting. This is interrupt
    XINT1.
238
239
240 //       read =  * RE_FPGA;  // for determining if the XINTF is working
241
242 //   * DA_VOUT1 = (unsigned int) (1 * 2457);
243         //The function defined in the AD7656_data_Pro source file is called here.
    This function needs to tap into the stucture and the defines found in the
    corresponding header file.
244                                      //The structure and the defines were named
    apollo_ad here, in the main source file.
245                                      //This is where the ADC conversion results are
    read by the DSP and manipulated in the main program, to get a reading of the
    sensed magnitudes.
246
247 bosen_ad.pro(&bosen_ad);
248 sin_a=m*sin(sin_i*0.005*6.283185306);
249
250 sin_i++;
251 if(sin_i>=200){sin_i=0;}//fundamental period 50ms
252
253        udc1 = bosen_ad.Vdc_linka; //lower
254        udc2 = bosen_ad.Vdc_linkb; //middle
255        udc3 = bosen_ad.Vdc_linkc; //upper
256        udc = udc1 + udc2 + udc3;
257
258        ufc = bosen_ad.Vfc;
259        capref = 0.333333*udc;
260        iai=bosen_ad.I_loada;
261
262         uai = sin_a*1.5 +1.5;
263
264         lai = floor(uai);
265
266         tai = uai - lai;
267
268         * A_Compare_value =(unsigned int)(uai * amp);
269 //          * DA_VOUT1 = (unsigned int) (tai * 2500);
270         if (iai>=0.0) {
271             if ((ufc-capref)>tolerance) {
272                 if (lai==0) {
273                     * SW_V13 = 0;
274                     * DIS_SW_V36 = 0;
275                     * DIS_SW_V68 = 0;
276                     * DIS_SW_V14 = 0;
277                     * DIS_SW_V47 = 0;
```

```
278                     * DIS_SW_V78 = 0;
279                     * DIS_SW_V12 = 0;
280                     * DIS_SW_V45 = 0;
281                     * DIS_SW_V26 = 0;
282                     * DIS_SW_V58 = 0;
283 
284                 }
285                 else if (lai==1) {
286 
287                     * DIS_SW_V13 = 0;
288                     * SW_V36 = 0;
289                     * DIS_SW_V68 = 0;
290                     * DIS_SW_V14 = 0;
291                     * DIS_SW_V47 = 0;
292                     * DIS_SW_V78 = 0;
293                     * DIS_SW_V12 = 0;
294                     * DIS_SW_V45 = 0;
295                     * DIS_SW_V26 = 0;
296                     * DIS_SW_V58 = 0;
297 
298                 }
299                 else if (lai==2) {
300 
301                     * DIS_SW_V13 = 0;
302                     * DIS_SW_V36 = 0;
303                     * SW_V68 = 0;
304                     * DIS_SW_V14 = 0;
305                     * DIS_SW_V47 = 0;
306                     * DIS_SW_V78 = 0;
307                     * DIS_SW_V12 = 0;
308                     * DIS_SW_V45 = 0;
309                     * DIS_SW_V26 = 0;
310                     * DIS_SW_V58 = 0;
311 
312                 }
313 //              else{}
314             }
315             else if ((ufc-capref)<(-tolerance)) {
316                 if (lai==0) {
317 
318                     * DIS_SW_V13 = 0;
319                     * DIS_SW_V36 = 0;
320                     * DIS_SW_V68 = 0;
321                     * SW_V14 = 0;
322                     * DIS_SW_V47 = 0;
323                     * DIS_SW_V78 = 0;
324                     * DIS_SW_V12 = 0;
325                     * DIS_SW_V45 = 0;
326                     * DIS_SW_V26 = 0;
327                     * DIS_SW_V58 = 0;
328 
329                 }
330                 else if (lai==1) {
331 
332                     * DIS_SW_V13 = 0;
333                     * DIS_SW_V36 = 0;
334                     * DIS_SW_V68 = 0;
335                     * DIS_SW_V14 = 0;
336                     * SW_V47 = 0;
```

```
337                     * DIS_SW_V78 = 0;
338                     * DIS_SW_V12 = 0;
339                     * DIS_SW_V45 = 0;
340                     * DIS_SW_V26 = 0;
341                     * DIS_SW_V58 = 0;
342 
343                 }
344                 else if (lai==2) {
345 
346                     * DIS_SW_V13 = 0;
347                     * DIS_SW_V36 = 0;
348                     * DIS_SW_V68 = 0;
349                     * DIS_SW_V14 = 0;
350                     * DIS_SW_V47 = 0;
351                     * SW_V78 = 0;
352                     * DIS_SW_V12 = 0;
353                     * DIS_SW_V45 = 0;
354                     * DIS_SW_V26 = 0;
355                     * DIS_SW_V58 = 0;
356 
357                 }
358 //              else{}
359             }
360             else
361                 if (lai==0) {
362                     ibus_neutral1i = iai * tai; //lower neutral point
363                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
364                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
365                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
366 
367                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
368                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
369                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
370 
371                     vtemp = vtemp1 + vtemp2 + vtemp3;
372 
373                     ibus_neutral2i = iai * tai;  //upper neutral point
374                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
375                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
376                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
377 
378                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
379                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
380                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
381 
382                     vtemp_second = vtemp1 + vtemp2 + vtemp3;
383                     if (vtemp>vtemp_second) {
384 
385                         * DIS_SW_V13 = 0;
386                         * DIS_SW_V36 = 0;
387                         * DIS_SW_V68 = 0;
388                         * SW_V14 = 0;
389                         * DIS_SW_V47 = 0;
390                         * DIS_SW_V78 = 0;
391                         * DIS_SW_V12 = 0;
392                         * DIS_SW_V45 = 0;
393                         * DIS_SW_V26 = 0;
```

```
394                         * DIS_SW_V58 = 0;
395
396                     }
397                     else {
398
399                         * DIS_SW_V13 = 0;
400                         * DIS_SW_V36 = 0;
401                         * DIS_SW_V68 = 0;
402                         * DIS_SW_V14 = 0;
403                         * DIS_SW_V47 = 0;
404                         * DIS_SW_V78 = 0;
405                         * SW_V12 = 0;
406                         * DIS_SW_V45 = 0;
407                         * DIS_SW_V26 = 0;
408                         * DIS_SW_V58 = 0;
409
410                     }
411                 }
412                 else if (lai==1) {
413                     ibus_neutral1i = iai * 1;
414                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
415                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
416                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
417
418                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
419                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
420                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
421
422                     vtemp = vtemp1 + vtemp2 + vtemp3;
423
424                     ibus_neutral2i = iai * 1;
425                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
426                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
427                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
428
429                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
430                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
431                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
432
433                     vtemp_second = vtemp1 + vtemp2 + vtemp3;
434                     if (vtemp>vtemp_second) {
435
436                         * DIS_SW_V13 = 0;
437                         * DIS_SW_V36 = 0;
438                         * DIS_SW_V68 = 0;
439                         * DIS_SW_V14 = 0;
440                         * DIS_SW_V47 = 0;
441                         * DIS_SW_V78 = 0;
442                         * DIS_SW_V12 = 0;
443                         * SW_V45 = 0;
444                         * DIS_SW_V26 = 0;
445                         * DIS_SW_V58 = 0;
446
447                     }
448                     else {
449
450                         * DIS_SW_V13 = 0;
```

```
451                         * DIS_SW_V36 = 0;
452                         * DIS_SW_V68 = 0;
453                         * DIS_SW_V14 = 0;
454                         * DIS_SW_V47 = 0;
455                         * DIS_SW_V78 = 0;
456                         * DIS_SW_V12 = 0;
457                         * DIS_SW_V45 = 0;
458                         * SW_V26 = 0;
459                         * DIS_SW_V58 = 0;
460 
461                     }
462                 }
463                 else if (lai==2) {
464                     ibus_neutral1i = iai * (1-tai);
465                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
466                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
467                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
468 
469                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
470                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
471                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
472 
473                     vtemp = vtemp1 + vtemp2 + vtemp3;
474 
475                     ibus_neutral2i = iai * (1-tai);
476                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
477                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
478                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
479 
480                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
481                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
482                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
483 
484                     vtemp_second = vtemp1 + vtemp2 + vtemp3;
485                     if (vtemp>vtemp_second) {
486 
487                         * DIS_SW_V13 = 0;
488                         * DIS_SW_V36 = 0;
489                         * DIS_SW_V68 = 0;
490                         * DIS_SW_V14 = 0;
491                         * DIS_SW_V47 = 0;
492                         * DIS_SW_V78 = 0;
493                         * DIS_SW_V12 = 0;
494                         * DIS_SW_V45 = 0;
495                         * DIS_SW_V26 = 0;
496                         * SW_V58 = 0;
497 
498                     }
499                     else {
500 
501                         * DIS_SW_V13 = 0;
502                         * DIS_SW_V36 = 0;
503                         * SW_V68 = 0;
504                         * DIS_SW_V14 = 0;
505                         * DIS_SW_V47 = 0;
506                         * DIS_SW_V78 = 0;
507                         * DIS_SW_V12 = 0;
```

```
508                         * DIS_SW_V45 = 0;
509                         * DIS_SW_V26 = 0;
510                         * DIS_SW_V58 = 0;
511 
512                     }
513                 }
514 //              else{}
515         }
516         else if (iai < 0.0) {
517             if ((ufc-capref)>tolerance) {
518                 if (lai==0) {
519 
520                     * DIS_SW_V13 = 0;
521                     * DIS_SW_V36 = 0;
522                     * DIS_SW_V68 = 0;
523                     * SW_V14 = 0;
524                     * DIS_SW_V47 = 0;
525                     * DIS_SW_V78 = 0;
526                     * DIS_SW_V12 = 0;
527                     * DIS_SW_V45 = 0;
528                     * DIS_SW_V26 = 0;
529                     * DIS_SW_V58 = 0;
530 
531                 }
532                 else if (lai==1) {
533 
534                     * DIS_SW_V13 = 0;
535                     * DIS_SW_V36 = 0;
536                     * DIS_SW_V68 = 0;
537                     * DIS_SW_V14 = 0;
538                     * SW_V47 = 0;
539                     * DIS_SW_V78 = 0;
540                     * DIS_SW_V12 = 0;
541                     * DIS_SW_V45 = 0;
542                     * DIS_SW_V26 = 0;
543                     * DIS_SW_V58 = 0;
544 
545                 }
546                 else if (lai==2) {
547 
548                     * DIS_SW_V13 = 0;
549                     * DIS_SW_V36 = 0;
550                     * DIS_SW_V68 = 0;
551                     * DIS_SW_V14 = 0;
552                     * DIS_SW_V47 = 0;
553                     * SW_V78 = 0;
554                     * DIS_SW_V12 = 0;
555                     * DIS_SW_V45 = 0;
556                     * DIS_SW_V26 = 0;
557                     * DIS_SW_V58 = 0;
558 
559                 }
560 //              else{}
561             }
562             else if ((ufc-capref)<(-tolerance)) {
563                 if (lai==0) {
564 
565                     * SW_V13 = 0;
566                     * DIS_SW_V36 = 0;
```

```
567                     * DIS_SW_V68 = 0;
568                     * DIS_SW_V14 = 0;
569                     * DIS_SW_V47 = 0;
570                     * DIS_SW_V78 = 0;
571                     * DIS_SW_V12 = 0;
572                     * DIS_SW_V45 = 0;
573                     * DIS_SW_V26 = 0;
574                     * DIS_SW_V58 = 0;
575 
576                 }
577                 else if (lai==1) {
578 
579                     * DIS_SW_V13 = 0;
580                     * SW_V36 = 0;
581                     * DIS_SW_V68 = 0;
582                     * DIS_SW_V14 = 0;
583                     * DIS_SW_V47 = 0;
584                     * DIS_SW_V78 = 0;
585                     * DIS_SW_V12 = 0;
586                     * DIS_SW_V45 = 0;
587                     * DIS_SW_V26 = 0;
588                     * DIS_SW_V58 = 0;
589 
590                 }
591                 else if (lai==2) {
592 
593                     * DIS_SW_V13 = 0;
594                     * DIS_SW_V36 = 0;
595                     * SW_V68 = 0;
596                     * DIS_SW_V14 = 0;
597                     * DIS_SW_V47 = 0;
598                     * DIS_SW_V78 = 0;
599                     * DIS_SW_V12 = 0;
600                     * DIS_SW_V45 = 0;
601                     * DIS_SW_V26 = 0;
602                     * DIS_SW_V58 = 0;
603 
604                 }
605 //              else{}
606             }
607             else
608                 if (lai==0) {
609                     ibus_neutral1i = iai * tai;
610                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
611                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
612                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
613 
614                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
615                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
616                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
617 
618                     vtemp = vtemp1 + vtemp2 + vtemp3;
619 
620                     ibus_neutral2i = iai * tai;
621                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
622                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
623                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
624 
```

```
625                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
626                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
627                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
628
629                     vtemp_second = vtemp1 + vtemp2 + vtemp3;
630                     if (vtemp>vtemp_second) {
631
632                         * DIS_SW_V13 = 0;
633                         * DIS_SW_V36 = 0;
634                         * DIS_SW_V68 = 0;
635                         * SW_V14 = 0;
636                         * DIS_SW_V47 = 0;
637                         * DIS_SW_V78 = 0;
638                         * DIS_SW_V12 = 0;
639                         * DIS_SW_V45 = 0;
640                         * DIS_SW_V26 = 0;
641                         * DIS_SW_V58 = 0;
642
643                     }
644                     else {
645
646                         * DIS_SW_V13 = 0;
647                         * DIS_SW_V36 = 0;
648                         * DIS_SW_V68 = 0;
649                         * DIS_SW_V14 = 0;
650                         * DIS_SW_V47 = 0;
651                         * DIS_SW_V78 = 0;
652                         * SW_V12 = 0;
653                         * DIS_SW_V45 = 0;
654                         * DIS_SW_V26 = 0;
655                         * DIS_SW_V58 = 0;
656
657                     }
658                 }
659                 else if (lai==1) {
660                     ibus_neutral1i = iai * 1;
661                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
662                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
663                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
664
665                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
666                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
667                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
668
669                     vtemp = /*2.2*sin(sin_i*0.005*6.283185306-2);*/vtemp1 + vtemp2
    + vtemp3;
670
671                     ibus_neutral2i = iai * 1;
672                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
673                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
674                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
675
676                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
677                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
678                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
679
```

```
680                     vtemp_second = /*1.2*sin(sin_i*0.005*6.283185306+2);*/vtemp1 +
    vtemp2 + vtemp3;
681                     if (vtemp>vtemp_second) {
682 
683                         * DIS_SW_V13 = 0;
684                         * DIS_SW_V36 = 0;
685                         * DIS_SW_V68 = 0;
686                         * DIS_SW_V14 = 0;
687                         * DIS_SW_V47 = 0;
688                         * DIS_SW_V78 = 0;
689                         * DIS_SW_V12 = 0;
690                         * SW_V45 = 0;
691                         * DIS_SW_V26 = 0;
692                         * DIS_SW_V58 = 0;
693 
694                     }
695                     else {
696 
697                         * DIS_SW_V13 = 0;
698                         * DIS_SW_V36 = 0;
699                         * DIS_SW_V68 = 0;
700                         * DIS_SW_V14 = 0;
701                         * DIS_SW_V47 = 0;
702                         * DIS_SW_V78 = 0;
703                         * DIS_SW_V12 = 0;
704                         * DIS_SW_V45 = 0;
705                         * SW_V26 = 0;
706                         * DIS_SW_V58 = 0;
707 
708                     }
709                 }
710                 else if (lai==2) {
711                     ibus_neutral1i = iai * (1-tai);
712                     ibus_neutral_threei = ibus_neutral1i *1.0*0.3333;
713                     ibus_neutral_twoi = ibus_neutral1i *1.0*0.3333;
714                     ibus_neutral_onei = (- ibus_neutral1i *2.0*0.3333);
715 
716                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
717                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
718                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
719 
720                     vtemp = vtemp1 + vtemp2 + vtemp3;
721 
722                     ibus_neutral2i = iai * (1-tai);
723                     ibus_neutral_threei = ibus_neutral2i *2.0*0.3333;
724                     ibus_neutral_twoi = (- ibus_neutral2i *1.0*0.3333);
725                     ibus_neutral_onei = (- ibus_neutral2i *1.0*0.3333);
726 
727                     vtemp1 = fabs(udc1 - 0.3333 * udc + ibus_neutral_onei * cap);
728                     vtemp2 = fabs(udc2 - 0.3333 * udc + ibus_neutral_twoi * cap);
729                     vtemp3 = fabs(udc3 - 0.3333 * udc + ibus_neutral_threei *
    cap);
730 
731                     vtemp_second = vtemp1 + vtemp2 + vtemp3;
732                     if (vtemp>vtemp_second) {
733 
734                         * DIS_SW_V13 = 0;
735                         * DIS_SW_V36 = 0;
```

```
736                         * DIS_SW_V68 = 0;
737                         * DIS_SW_V14 = 0;
738                         * DIS_SW_V47 = 0;
739                         * DIS_SW_V78 = 0;
740                         * DIS_SW_V12 = 0;
741                         * DIS_SW_V45 = 0;
742                         * DIS_SW_V26 = 0;
743                         * SW_V58 = 0;
744
745                     }
746                     else {
747
748                         * DIS_SW_V13 = 0;
749                         * DIS_SW_V36 = 0;
750                         * SW_V68 = 0;
751                         * DIS_SW_V14 = 0;
752                         * DIS_SW_V47 = 0;
753                         * DIS_SW_V78 = 0;
754                         * DIS_SW_V12 = 0;
755                         * DIS_SW_V45 = 0;
756                         * DIS_SW_V26 = 0;
757                         * DIS_SW_V58 = 0;
758
759                     }
760                 }
761 //                else{}
762         }
763
764         if ( bosen_ad.Vdc_linka >= Vdc_limit || bosen_ad.Vdc_linkb >= Vdc_limit ||
    bosen_ad.Vdc_linkc >= Vdc_limit || bosen_ad.I_loada >= Iload_limit|| bosen_ad.Vfc
    >= Vfc_limit)
765                         {
766                             * DIS_Pulse = 1;  //The DIS_PULSE acts on the
    compare_en variable at the FPGA side, which in turn enables or disables the
    generation of the PWM signals.
767                         }
768
769
770     GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
771
772     GpioDataRegs.GPBTOGGLE.bit.GPIO61 = 1;
773     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
774     return;
775
776 }
777
778
779
780
781
782 //===========================================================================
783 // No more.
784 //===========================================================================
785
786
787
```

```
    1   `timescale 1ns / 1ps
    2   //////////////////////////////////////////////////////////////////////////////////
    3   // Company:
    4   // Engineer:
    5   //
    6   // Create Date:    10:36:57 08/31/2011
    7   // Design Name:    lixiaoqiang
    8   // Module Name:    AD_TEST
    9   // Project Name:
   10   // Target Devices:
   11   // Tool versions:
   12   // Description:
   13   //
   14   // Dependencies:
   15   //
   16   // Revision:
   17   // Revision 0.01 - File Created
   18   // Additional Comments: XZCS0
   19   //
   20   //////////////////////////////////////////////////////////////////////////////////
   21   module Top_control(DB,ADDB,XZCS0,XRD,XWE0,ADC_CONVST,ADC_BUSY1,ADC_BUSY2,
   22                      ADC_CS1,ADC_CS2,ADC_RD,RESET_H,clk,XINT1,XINT2,
   23                      DA_CS,DA_WR,DA_LDAC,RESET_L,
   24                      pwm1,pwm2,pwm3,pwm4,pwm5,pwm6,pwm7,pwm8,
        /*pwm9,pwm10,pwm11,pwm12,pwm13,pwm14,pwm15,pwm16,pwm17,pwm18,
   25
        pwm19,pwm20,pwm21,pwm22,pwm23,pwm24,pwm25,pwm26,pwm27,pwm28,pwm29,pwm30,pwm31,pwm32
        ,pwm33,pwm34,pwm35,pwm36,*/
   26   //                   Drive_fault1,Drive_fault2,Drive_fault3,
   27   //                   Drive_fault4,Drive_fault5,Drive_fault6,
   28   //
        Contactor_control,Contactor_switch,Stop_button,Run_led,Fault_led,Power_led
   29                        );
   30   ////////////////////input_output define/////////////////////////
   31         input XZCS0;        //DSP side 0 zone select signal(low active)
   32         input XRD;          //DSP side 0 zone read signal(low active)
   33         input XWE0;         //DSP side 0 zone write signal(low active)
   34         input ADC_BUSY1,ADC_BUSY2;          //AD7656_1/2/3 busy signal
   35         input clk;          //FPGA 50M Hz clock
   36   //    input
        Drive_fault1,Drive_fault2,Drive_fault3,Drive_fault4,Drive_fault5,Drive_fault6;//IGB
        T driver fault protection signal
   37         input [19:0] ADDB;        //DSP side 20 bit address bus
   38         input Stop_button;        //stop button
   39   //    input Contactor_switch;   //contactor switch
   40         output ADC_CONVST;        //AD7656_1/2/3 convert signal
   41         output ADC_CS1, ADC_CS2;            // AD7656_1/2/3 chip select signal
   42         output ADC_RD;            //AD7656_1/2/3 read signal
   43         output RESET_H;           //AD7656_1/2/3 reset signal
   44         output XINT1;             //interrupt for AD7656_1/2/3
   45         output XINT2;             //interrupt for SVPWM
   46         inout [15:0] DB;          //16 bit data bus
   47         output pwm1,pwm2,pwm3,pwm4,pwm5,pwm6,pwm7,pwm8
        /*,pwm9,pwm10,pwm11,pwm12,pwm13,pwm14,pwm15,pwm16,pwm17,pwm18*/;//PWN output pins
   48   //    output
```

```
      pwm19,pwm20,pwm21,pwm22,pwm23,pwm24,pwm25,pwm26,pwm27,pwm28,pwm29,pwm30,pwm31,pwm32
      ,pwm33,pwm34,pwm35,pwm36;
 49         output DA_CS;              //DA5725 chip select
 50         output DA_WR;              //DA5725 write data signal
 51         output DA_LDAC;            //DA5725 convert signal
 52         output RESET_L;            //DA5725 reset signal
 53   //    output Contactor_control; //contactor control signal(1:on,0:off)
 54   //    output Run_led,Fault_led,Power_led; //led for run,fault,power
 55   ////////////////////variable && data style define ////////////////////////////
 56
 57   //////////DATA BUS Tristate define////////////////////
 58         wire signed [15:0] DB;   //define DB as 16 bit signed data style
 59         wire signed [15:0] input_of_DB;      //DB input reg
 60         wire signed [15:0] output_of_DB;     //DB output reg
 61         reg out_en;    //input or output enable signal for tristate (1:output
      ,0:input)
 62         reg signed [15:0] R_FPGA, T_FPGA,Data_output;   //R_FPGA: DSP =>FPGA
      T_FPGA: DSP<=FPGA
 63
 64   //////////PWM pin define//////////////////////////
 65         wire A_1,A_2,A_3,A_4,A_5,A_6,A_7,A_8;
 66         wire [15:0] counter;
 67         reg [15:0] A_Compare
      /*,B_Compare,C_Compare*//*,RA_Compare,RB_Compare,RC_Compare*/;
 68         reg [15:0] A_Com/*,B_Com,C_Com*//*,RA_Com,RB_Com,RC_Com*/;
 69   //      reg SW_V13,SW_V36,SW_V68,SW_V14,SW_V47,SW_V78,SW_V12,SW_V45,SW_V26,SW_V58;
 70         reg compare_en;
 71         reg over_flag;
 72         reg XINT2_en;           //PWM interrupt enable output, 0: disable, 1: enable
 73
 74   ////////////////////main code zone//////////////////////////////////////////////
 75
 76   //////////initial zone//////////////////////////////
 77         initial
 78            begin
 79               out_en = 1'b0;
 80               R_FPGA = 'd0;
 81               T_FPGA = 'd0;
 82               Data_output = 'd0;
 83   //          IGBT_Fault = 'd0;
 84   //          IGBT_count = 'd0;
 85   //          Contactor_output = 'd0;
 86               A_Com= 'd0; /*B_Com= 'd0; C_Com= 'd0;*/
 87   //          A_Compare= 'd15000; B_Compare= 'd15000; C_Compare= 'd15000;
 88               A_Compare= 'd0; /*B_Compare= 'd0; C_Compare= 'd0;*/
 89   //            SW_V13= 'd0; SW_V36= 'd0; SW_V68= 'd0; SW_V14= 'd0; SW_V47= 'd0;
      SW_V78= 'd0; SW_V12= 'd0; SW_V45= 'd0; SW_V26= 'd0; SW_V58= 'd0;
 90               over_flag= 'd0;
 91               XINT2_en='d0;
 92               compare_en='d0;
 93   //          Contactor_control = 'd0; Run_led ='d0; Fault_led ='d0; Power_led ='d1;
 94            end
 95
 96   //////////DATA BUS Tristate control////////////////////
 97         assign input_of_DB = DB;
```

```
   98         assign DB = (out_en==1'b1)? output_of_DB : 16'hzzzz ;
   99
  100   /////////DSP <==> FPGA Communication//////////////////
  101         always @(posedge clk)
  102            begin
  103                  if((ADDB==20'h4fc0))
  104                  //this three address for AD7656_1/2/3 ,FPGA need AD data for
      calculating,so set the port as input_port
  105                     out_en <= 1'b1;           //DB output control port
  106                  else
  107                     out_en <= 1'b0;          //DB input control port
  108            end
  109
  110   ////////////////////////////////////////
  111
  112   assign output_of_DB=T_FPGA;   //FPGA uploads DSP data
  113
  114   /////DSP write to FPGA ///////////////////
  115            always @(XWE0)
  116            if(XWE0==1'b0 && ADDB==20'h4ff0 && XZCS0==1'b0)
  117               begin
  118                  R_FPGA <= input_of_DB;
  119               end
  120   /////DSP read FPGA /////
  121            always @(XRD)
  122            if(XRD==1'b0 && ADDB==20'h4fc0 && XZCS0==1'b0)//&& ADDB==20'h4fc0
  123                  T_FPGA =  16'h0000;
      ////////////////////Change_Here//////////////////////////
  124   //        else
  125   //           if(XRD==1'b0 && ADDB==20'h4f55 && XZCS0==1'b0)
  126   //              T_FPGA = IGBT_Fault;
  127   //           else
  128   //              if(XRD==1'b0 && ADDB==20'h4f44 && XZCS0==1'b0)
  129   //                 T_FPGA = Contactor_output;
  130
  131   ////AD7565////
  132         AD7656 ADC_control(
  133            .clk(clk),.ADDB(ADDB),.XZCS0(XZCS0),.XRD(XRD),
  134            .ADC_CONVST(ADC_CONVST),.ADC_BUSY1(ADC_BUSY1),
  135            .ADC_BUSY2(ADC_BUSY2),
  136            .ADC_CS1(ADC_CS1),.ADC_CS2(ADC_CS2),
  137            .ADC_RD(ADC_RD),.RESET_H(RESET_H),.XINT1(XINT1)
  138                           );
  139
  140   //////DAC5725/////
  141         DA5725 DAC_control(
  142            .clk(clk),
  143            .XWE0(XWE0),
  144            .XZCS0(XZCS0),
  145            .ADDB(ADDB),
  146            .DA_CS(DA_CS),
  147            .DA_WR(DA_WR),
  148            .DA_LDAC(DA_LDAC),
  149            .RESET_L(RESET_L)
  150                           );
```

```
151
152   //////PWM produce///////
153   ////enable triangle wave under flow interrupt
154         always @(posedge clk)
155            begin
156             if(ADDB==20'h4f0a && XZCS0==1'b0)
157                   XINT2_en='d1;
158             if(ADDB==20'h4f0c && XZCS0==1'b0)
159                   XINT2_en='d0;
160            end
161   ////read modulation wave signals from DSP for comparison
162
163         always @(XWE0)
164             if(XWE0==1'b0 && ADDB==20'h4f03 && XZCS0==1'b0)
165                  begin
166                     A_Com <= input_of_DB;
167                     over_flag <= 'd1;
168                  end
169             else
170                  over_flag <= 'd0;
171
172   ////generate PWM signals
173         PWM_Generate PWM(
174            .clk(clk),
175            .A_Compare(A_Compare),
176            .ADDB(ADDB),
177            .XZCS0(XZCS0),
178            .counter(counter),
179            .A_1(A_1),.A_2(A_2),.A_3(A_3),.A_4(A_4),.A_5(A_5),.A_6(A_6),.A_7(A_7),.
       A_8(A_8),
180            .SW_V13(SW_V13),.SW_V36(SW_V36),.SW_V68(SW_V68),.SW_V14(SW_V14),.SW_V47(
       SW_V47),.SW_V78(SW_V78),.SW_V12(SW_V12),.SW_V45(SW_V45),.SW_V26(SW_V26),.SW_V58(
       SW_V58),
181            .XINT2(XINT2),
182            .XINT2_en(XINT2_en),
183            .compare_en(compare_en)
184                       );
185
186   ////When three comparison values received, send to PWM comparitor to generator PWM
187         always @(posedge clk)
188            if(counter == 'd2500)
189               begin
190                  A_Compare <=A_Com;
191               end
192
193   ////enable/disable PWM output
194         //assign en_signal = (~XWE0 | fault_flag1 | fault_flag2 | fault_flag3 |
       fault_flag4 | fault_flag5 | fault_flag6);
195         always @(posedge clk)
196             if((ADDB==20'h4fa6 && XZCS0==1'b0))
197                        compare_en = 'd0;             //disable PWM output
198             else
199               begin
200                  if(ADDB==20'h4fa1 && XZCS0==1'b0)
201                     compare_en = 'd1;               //enable PWM output
```

```
202                 end
203
204     ////PWM output
205           assign pwm1 = A_1;
206           assign pwm2 = A_2;
207           assign pwm3 = A_3;
208           assign pwm4 = A_4;
209           assign pwm5 = A_5;
210           assign pwm6 = A_6;
211           assign pwm7 = A_7;
212           assign pwm8 = A_8;
213
214     endmodule
215
```

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    17:01:09 10/25/2011
7   // Design Name:
8   // Module Name:    PWM_Generate
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21    module PWM_Generate(clk,A_Compare,/*B_Compare,C_Compare,*/counter,
22                        XZCS0,ADDB,
23                      A_1,A_2,A_3,A_4,A_5,A_6,A_7,A_8,
24                      SW_V13,SW_V36,SW_V68,SW_V14,SW_V47,SW_V78,SW_V12,SW_V45,SW_V26,
    SW_V58,
25                      XINT2,XINT2_en,compare_en
26                     );
27  ////////////////////input_output define//////////////////////
28        input clk;
29        input [15:0] A_Compare;
30        output counter;
31        input [19:0] ADDB;
32        input XZCS0;
33        output A_1,A_2,A_3,A_4,A_5,A_6,A_7,A_8;
34        output SW_V13,SW_V36,SW_V68,SW_V14,SW_V47,SW_V78,SW_V12,SW_V45,SW_V26,SW_V58;
35        output XINT2;                                    //counter=0 triangle wave
    overflow interrupt
36        input XINT2_en;                                 //enable XINT2 output
37        input compare_en;
38  ////////////////////variable && data style define//////////////////////
39  //    parameter PRD = 16'd12500;           //fs=2kHz, IGBT switch period
    PRD=Ts*fm/2=0.0005*50000000/2=12500
40  //    parameter PRD = 16'd5000;           //fs=5kHz, IGBT switch period
    PRD=Ts*fm/2=0.0002*50000000/2=5000
41        parameter PRD = 16'd2500;           //fs=10kHz, IGBT switch period
    PRD=Ts*fm/2=0.0001*50000000/2=2500
42  //    parameter PRD = 16'd1250;            //fs=20kHz, IGBT switch period
    PRD=Ts*fm/2=(1/20000)*50000000/2=1250
43  //    parameter PRD = 16'd833;             //fs=30kHz, IGBT switch period
    PRD=Ts*fm/2=(1/30000)*50000000/2=833
44  //    parameter PRD = 16'd625;             //fs=40kHz, IGBT switch period
    PRD=Ts*fm/2=(1/40000)*50000000/2=625
45  //    parameter PRD = 16'd500;             //fs=50kHz, IGBT switch period
    PRD=Ts*fm/2=(1/50000)*50000000/2=500
46        reg [15:0] counter;                  //produce the triangle wave
```

```
47          reg symbol_flag;                    //signed bit of up/down 1:up 0:down
48          reg A_1,A_2,A_3,A_4,A_5,A_6,A_7,A_8;
49    //    reg [1:0] flag_a,flag_b,flag_c;
50          reg SW_V13,SW_V36,SW_V68,SW_V14,SW_V47,SW_V78,SW_V12,SW_V45,SW_V26,SW_V58;
51          reg [7:0] count_a1,count_a2,count_a3,count_a4,count_a5,count_a6,count_a7,
      count_a8;
52          reg XINT2_flag;
53    //////////initial zone////////////////////////////////
54          initial
55             begin
56                symbol_flag = 1'b1;
57                counter = 16'd0;
58                A_1 = 'b0;
59                A_2 = 'b0;
60                A_3 = 'b0;
61                A_4 = 'b0;
62                A_5 = 'b0;
63                A_6 = 'b0;
64                A_7 = 'b0;
65                A_8 = 'b0;
66                SW_V13 = 'b0;
67                SW_V36 = 'b0;
68                SW_V68 = 'b0;
69                SW_V14 = 'b0;
70                SW_V47 = 'b0;
71                SW_V78 = 'b0;
72                SW_V12 = 'b0;
73                SW_V45 = 'b0;
74                SW_V26 = 'b0;
75                SW_V58 = 'b0;
76                count_a1 = 'd0; count_a2 = 'd0; count_a3 = 'd0; count_a4 = 'd0;
      count_a5 = 'd0; count_a6 = 'd0; count_a7 = 'd0; count_a8 = 'd0;
77                XINT2_flag = 1'b0;
78             end
79    ////////////////////main code zone//////////////////////////////////////////////
80
81          always @(posedge clk)
82              if(ADDB==20'h4f11 && XZCS0==1'b0)
83                    begin
84                    SW_V13 = 'b1;
85                    end
86              else
87                    begin
88                    if(ADDB==20'h4f22 && XZCS0==1'b0)
89                    SW_V13 = 'b0;
90                    end
91          always @(posedge clk)
92              if(ADDB==20'h4f16 && XZCS0==1'b0)
93                    begin     SW_V36 = 'b1;   end
94              else
95                    begin
96                    if(ADDB==20'h4f33 && XZCS0==1'b0)
97                    SW_V36 = 'b0;
98                    end
99          always @(posedge clk)
```

```
100             if(ADDB==20'h4fb6 && XZCS0==1'b0)
101                   begin
102                   SW_V68 = 'b1;
103                   end
104             else
105                   begin
106                   if(ADDB==20'h4f66 && XZCS0==1'b0)
107                   SW_V68 = 'b0;
108                   end
109         always @(posedge clk)
110             if(ADDB==20'h4fb1 && XZCS0==1'b0)
111                   begin     SW_V14 = 'b1;   end
112             else
113                   begin
114                   if(ADDB==20'h4f77 && XZCS0==1'b0)
115                   SW_V14 = 'b0;
116                   end
117         always @(posedge clk)
118             if(ADDB==20'h4fbc && XZCS0==1'b0)
119                   begin     SW_V47 = 'b1;   end
120             else
121                   begin
122                   if(ADDB==20'h4f88 && XZCS0==1'b0)
123                   SW_V47 = 'b0;
124                   end
125         always @(posedge clk)
126             if(ADDB==20'h4fba && XZCS0==1'b0)
127                   begin     SW_V78 = 'b1;   end
128             else
129                   begin
130                   if(ADDB==20'h4f99 && XZCS0==1'b0)
131                   SW_V78 = 'b0;
132                   end
133         always @(posedge clk)
134             if(ADDB==20'h4fac && XZCS0==1'b0)
135                   begin     SW_V12 = 'b1;   end
136             else
137                   begin
138                   if(ADDB==20'h4f21 && XZCS0==1'b0)
139                   SW_V12 = 'b0;
140                   end
141         always @(posedge clk)
142             if(ADDB==20'h4faa && XZCS0==1'b0)
143                   begin     SW_V45 = 'b1;   end
144             else
145                   begin
146                   if(ADDB==20'h4f31 && XZCS0==1'b0)
147                   SW_V45 = 'b0;
148                   end
149         always @(posedge clk)
150             if(ADDB==20'h4f12 && XZCS0==1'b0)
151                   begin     SW_V26 = 'b1;   end
152             else
153                   begin
154                   if(ADDB==20'h4f41 && XZCS0==1'b0)
```

```
155                   SW_V26 = 'b0;
156                   end
157           always @(posedge clk)
158               if(ADDB==20'h4fe1 && XZCS0==1'b0)
159                     begin     SW_V58 = 'b1;   end
160               else
161                     begin
162                     if(ADDB==20'h4f51 && XZCS0==1'b0)
163                     SW_V58 = 'b0;
164                     end
165
166     ///////generator triangle//////
167           always @(posedge clk)
168              if(symbol_flag == 1'b1)
169                 if(counter < PRD)
170                    counter = counter + 'd1;
171                 else
172                    begin
173                       counter = PRD - 'd1;
174                       symbol_flag = 1'b0;
175                       XINT2_flag = 1'b0;
176                    end
177              else
178                 if(counter > 16'd0)
179                    begin
180                       counter = counter - 'd1;
181                       if(counter == 'd0)
182                          XINT2_flag = 1'b1;
183                    end
184                 else
185                    begin
186                       counter = 'd1;
187                       symbol_flag = 1'b1;
188                    end
189
190     ///////enable interrupt pulse/////
191           assign XINT2 = (XINT2_en==1'b1)? XINT2_flag : 1'b1 ;
192
193     ///////generator pulse//////
194
195     //Inverter side///////
196     //A_phase
197
198           always @(posedge clk)
199              if(compare_en == 'd0)
200                 begin
201                    A_1<='d0;
202                    A_2<='d0;
203                    A_3<='d0;
204                    A_4<='d0;
205                    A_5<='d0;
206                    A_6<='d0;
207                    A_7<='d0;
208                    A_8<='d0;
209                 end
```

```
210             else
211                begin
212                   if(SW_V68 == 'd1)
213                       begin
214                          A_2<='d0;
215                          A_3<='d0;
216                          A_5<='d1;
217                          A_6<='d0;
218                          A_7<='d1;
219                          A_8<='d0;
220                          if(counter>(A_Compare-2*PRD)/*A_Compare*/)
221                            begin
222                               count_a1<= 'd0;
223                               A_1<='d0;
224                               if(count_a4 == 'd100)
225                                  A_4<='d1;
226    //                            A_5<='d1;
227                               else
228                                  count_a4<=count_a4+'d1;
229                            end
230                          else if(counter<(A_Compare-2*PRD)/*A_Compare*/)
231                            begin
232                               count_a4<= 'd0;
233                               A_4<='d0;
234    //                         A_5<='d0;
235                               if(count_a1 == 'd100)
236                                  A_1<='d1;
237                               else
238                                  count_a1<=count_a1+'d1;
239                            end
240                          else
241                            begin
242                               count_a1<= 'd0;
243                               A_1<='d0;
244                               count_a4<= 'd0;
245                               A_4<='d0;
246                            end
247                       end
248                    else if(SW_V13 == 'd1)
249                       begin
250                          A_1<='d0;
251                          A_2<='d0;
252                          A_3<='d0;
253                          A_4<='d0;
254                          A_5<='d0;
255                          A_6<='d1;
256                          if(counter>A_Compare)
257                            begin
258                               count_a7<= 'd0;
259                               A_7<='d0;
260                               if(count_a8 == 'd100)
261                                  A_8<='d1;
262                               else
263                                  count_a8<=count_a8+'d1;
264                            end
```

```
265                         else if(counter<A_Compare)
266                           begin
267                              count_a8<= 'd0;
268                              A_8<='d0;
269                              if(count_a7 == 'd100)
270                                 A_7<='d1;
271                              else
272                                 count_a7<=count_a7+'d1;
273                           end
274                         else
275                           begin
276                              count_a7<= 'd0;
277                              A_7<='d0;
278                              count_a8<= 'd0;
279                              A_8<='d0;
280                           end
281                     end
282                   else if(SW_V36 == 'd1)
283                     begin
284                        A_1<='d0;
285                        A_2<='d0;
286                        A_3<='d0;
287                        A_4<='d1;
288                        A_7<='d1;
289                        A_8<='d0;
290                        if(counter>(A_Compare-PRD)/*A_Compare*/)
291                          begin
292      //                     count_a4<= 'd0;
293      //                     A_4<='d0;
294                             count_a5<= 'd0;
295                             A_5<='d0;
296                             if(count_a6 == 'd100)
297                                A_6<='d1;
298                             else
299                                count_a6<=count_a6+'d1;
300                          end
301                        else if(counter<(A_Compare-PRD)/*A_Compare*/)
302                          begin
303                             count_a6<= 'd0;
304                             A_6<='d0;
305                             if((count_a5 == 'd100) /*|| (count_a5 == 'd100)*/)
306   //                           A_4<='d1;
307                                A_5<='d1;
308                             else
309                                count_a5<=count_a5+'d1;
310                          end
311                        else
312                          begin
313                             count_a5<= 'd0;
314                             A_5<='d0;
315                             count_a6<= 'd0;
316                             A_6<='d0;
317                          end
318                     end
319                   else if(SW_V14 == 'd1)
```

```
320                     begin
321                        A_1<='d0;
322                        A_2<='d1;
323                        A_4<='d0;
324                        A_5<='d0;
325                        A_7<='d0;
326                        A_8<='d1;
327                        if(counter>A_Compare)
328                          begin
329                             count_a3<= 'd0;
330   //                        A_2<='d0;
331                             A_3<='d0;
332                             if(count_a6 == 'd100)
333                                A_6<='d1;
334                             else
335                                count_a6<=count_a6+'d1;
336                          end
337                        else if(counter<A_Compare)
338                          begin
339                             count_a6<= 'd0;
340                             A_6<='d0;
341                             if(count_a3 == 'd100)
342   //                           A_2<='d1;
343                                A_3<='d1;
344                             else
345                                count_a3<=count_a3+'d1;
346                          end
347                       else
348                         begin
349                            count_a3<= 'd0;
350                            A_3<='d0;
351                            count_a6<= 'd0;
352                            A_6<='d0;
353                         end
354                     end
355                  else if(SW_V47 == 'd1)
356                     begin
357                        A_3<='d1;
358                        A_4<='d0;
359                        A_5<='d0;
360                        A_6<='d0;
361                        A_7<='d0;
362                        A_8<='d1;
363                        if(counter>(A_Compare-PRD)/*A_Compare*/)
364                          begin
365                             count_a1<= 'd0;
366                             A_1<='d0;
367                             if(count_a2 == 'd100)
368                                A_2<='d1;
369   //                        A_3<='d1;
370                             else
371                                count_a2<=count_a2+'d1;
372                          end
373                        else if(counter<(A_Compare-PRD)/*A_Compare*/)
374                          begin
```

```
375                              count_a2<= 'd0;
376                              A_2<='d0;
377   //                         A_3<='d0;
378                              if(count_a1 == 'd100)
379                                 A_1<='d1;
380                              else
381                                 count_a1<=count_a1+'d1;
382                           end
383                        else
384                          begin
385                             count_a1<= 'd0;
386                             A_1<='d0;
387                             count_a2<= 'd0;
388                             A_2<='d0;
389                          end
390                     end
391                  else if(SW_V78 == 'd1)
392                     begin
393                        A_1<='d1;
394                        A_2<='d0;
395                        A_3<='d0;
396                        A_4<='d0;
397                        A_5<='d0;
398                        A_6<='d0;
399                        if(counter>(A_Compare-2*PRD)/*A_Compare*/)
400                          begin
401                             count_a7<= 'd0;
402                             A_7<='d0;
403                             if(count_a8 == 'd100)
404                                A_8<='d1;
405                             else
406                                count_a8<=count_a8+'d1;
407                          end
408                        else if(counter<(A_Compare-2*PRD)/*A_Compare*/)
409                          begin
410                             count_a8<= 'd0;
411                             A_8<='d0;
412                             if(count_a7 == 'd100)
413                                A_7<='d1;
414                             else
415                                count_a7<=count_a7+'d1;
416                          end
417                        else
418                          begin
419                             count_a7<= 'd0;
420                             A_7<='d0;
421                             count_a8<= 'd0;
422                             A_8<='d0;
423                          end
424                     end
425                  else if(SW_V12 == 'd1)
426                     begin
427                        A_1<='d0;
428                        A_2<='d0;
429                        A_3<='d0;
```

```
430                         A_4<='d1;
431                         A_7<='d0;
432                         A_8<='d1;
433                         if(counter>A_Compare)
434                           begin
435                              count_a5<= 'd0;
436   //                         A_4<='d0;
437                              A_5<='d0;
438                              if(count_a6 == 'd100)
439                                 A_6<='d1;
440                              else
441                                 count_a6<=count_a6+'d1;
442                           end
443                         else if(counter<A_Compare)
444                           begin
445                              count_a6<= 'd0;
446                              A_6<='d0;
447                              if(count_a5 == 'd100)
448   //                            A_4<='d1;
449                                 A_5<='d1;
450                              else
451                                 count_a5<=count_a5+'d1;
452                           end
453                        else
454                          begin
455                             count_a5<= 'd0;
456                             A_5<='d0;
457                             count_a6<= 'd0;
458                             A_6<='d0;
459                          end
460                     end
461                  else if(SW_V45 == 'd1)
462                     begin
463                        A_1<='d0;
464                        A_2<='d1;
465                        A_3<='d1;
466                        A_4<='d0;
467                        A_5<='d0;
468                        A_6<='d0;
469                        if(counter>(A_Compare-PRD)/*A_Compare*/)
470                          begin
471                             count_a7<= 'd0;
472                             A_7<='d0;
473                             if(count_a8 == 'd100)
474                                A_8<='d1;
475                             else
476                                count_a8<=count_a8+'d1;
477                          end
478                        else if(counter<(A_Compare-PRD)/*A_Compare*/)
479                          begin
480                             count_a8<= 'd0;
481                             A_8<='d0;
482                             if(count_a7 == 'd100)
483                                A_7<='d1;
484                             else
```

```
485                                 count_a7<=count_a7+'d1;
486                             end
487                           else
488                             begin
489                                count_a7<= 'd0;
490                                A_7<='d0;
491                                count_a8<= 'd0;
492                                A_8<='d0;
493                             end
494                       end
495                     else if(SW_V26 == 'd1)
496                       begin
497                          A_1<='d0;
498                          A_2<='d0;
499                          A_3<='d0;
500                          A_4<='d1;
501                          A_5<='d1;
502                          A_6<='d0;
503                          if(counter>(A_Compare-PRD)/*A_Compare*/)
504                            begin
505                               count_a7<= 'd0;
506                               A_7<='d0;
507                               if(count_a8 == 'd100)
508                                  A_8<='d1;
509                               else
510                                  count_a8<=count_a8+'d1;
511                            end
512                          else if(counter<(A_Compare-PRD)/*A_Compare*/)
513                            begin
514                               count_a8<= 'd0;
515                               A_8<='d0;
516                               if(count_a7 == 'd100)
517                                  A_7<='d1;
518                               else
519                                  count_a7<=count_a7+'d1;
520                            end
521                          else
522                            begin
523                               count_a7<= 'd0;
524                               A_7<='d0;
525                               count_a8<= 'd0;
526                               A_8<='d0;
527                            end
528                       end
529                     else if(SW_V58 == 'd1)
530                       begin
531                          A_3<='d1;
532                          A_4<='d0;
533                          A_5<='d0;
534                          A_6<='d0;
535                          A_7<='d1;
536                          A_8<='d0;
537                          if(counter>(A_Compare-2*PRD)/*A_Compare*/)
538                            begin
539                               count_a1<= 'd0;
```

```
540                                 A_1<='d0;
541                                 if(count_a2 == 'd100)
542                                    A_2<='d1;
543   //                               A_3<='d1;
544                                 else
545                                    count_a2<=count_a2+'d1;
546                               end
547                             else if(counter<(A_Compare-2*PRD)/*A_Compare*/)
548                               begin
549                                  count_a2<= 'd0;
550                                  A_2<='d0;
551   //                             A_3<='d0;
552                                  if(count_a1 == 'd100)
553                                     A_1<='d1;
554                                  else
555                                     count_a1<=count_a1+'d1;
556                               end
557                             else
558                               begin
559                                  count_a1<= 'd0;
560                                  A_1<='d0;
561                                  count_a2<= 'd0;
562                                  A_2<='d0;
563                               end
564                         end
565                 end
566
567   endmodule
568
```

III. Code execution principle of the DSP/FPGA control board

Fig.A.E.1 presents the general operation flow diagram of the employed DSP/FPGA control board. First, DSP gives an order that XINT2 has been enabled. Where XINT2 actives the interrupt AD conversion progress which synchronizes with the triangular carrier wave each sampling period. During the AD converter process, DSP gives an order to initialize the AD conversion in ADC chip. AD 7656 will begin the AD signals conversion. After the 3μs AD conversion finishes, a BUSY signal will enable the XINT1. Where XINT1 actives the interrupt called "AD sampling interrupt", in which most of the control algorithm and codes are executed based on the variables get from the AD conversion in the last step. After all the included control algorithm and codes execution, the modulation wave will be updated accordingly. Finally, the updated modulation wave will be transferred to the FPGA through the DB(data bus) to compare with the carrier wave then generate the PWN signals.

The feature of this control board is that the FPGA only focuses on the carrier wave generation and PWM output (through the comparison of the carrier wave and the modulation wave). While the DSP only focuses on the calculation.

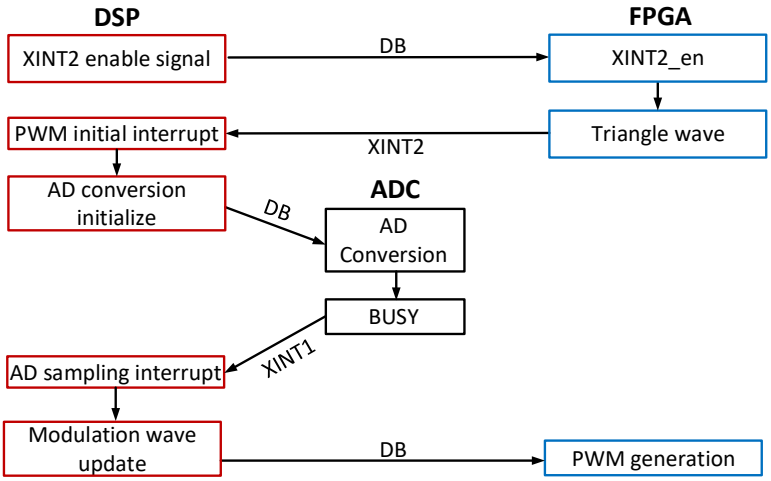
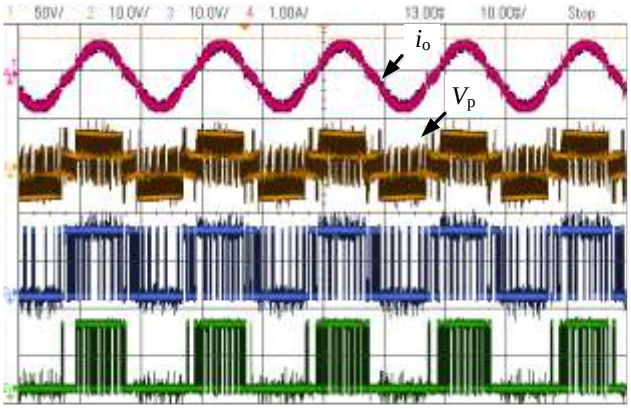


Fig.A.E.1 operation flow chart of the DSP/FPGA board

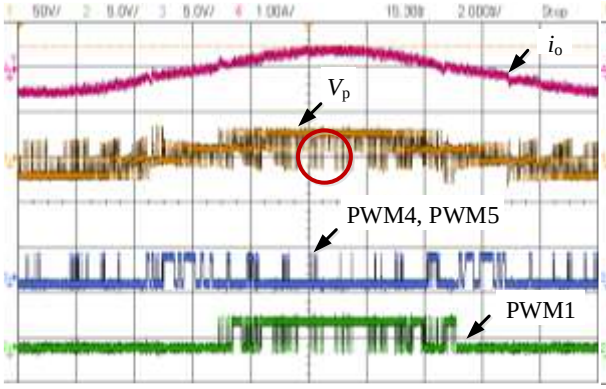
Appendix G. Hybrid four-level π-type converter supplementary information

I. Two-level jump phenomenon in the hybrid four-level π-type converter operation

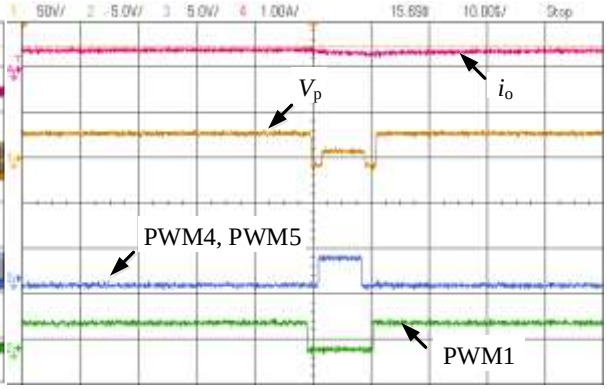
An initial test of the hybrid four-level π-type single-phase converter under the 70V dc-link voltage condition has been taken as a trail. Due to this test did not consider the deadtime effect, there're two-level jump (eg. From E jumps to 3E directly) phenomenons in the phase voltage waveform as shown in Fig.A.F.I. As the desirable operation requires the output voltage only jumps between the adjacent voltage levels, for example from E to 2E then from 2E to 3E. The two-level jump will cause a larger voltage stress on the individual switching device, consequently increases the switching loss as well as the output harmonic contents.



(a) Output current and phase voltage



(b) V6 V8 switching states outputs



(c) V6 V8 switching states outputs (zoomed)

Fig.A.F.I Initial test on single-phase hybrid four-level π-type converter without considering the dead-time effect

II. ADC input filter modification and its effect on FC voltage control

The FC in the hybrid four-level π-type converter should be served as a high frequency charging/discharging capacitor. As mentioned in chapter 5, ideally, within one switching cycle, switching states should be selected flexibly to charge or discharge the FC for a given current direction. Therefore, sampling as well as the control delay for the FC voltage control should be as small as possible. In practical implementation, in order to reduce the high frequency noise, each sampled variable has to be filtered by the analogue filter before entering into the ADC. Fig. A.F.II presents the schematic layout of the second-order high pass filter with the default setting before the input of the ADC on the adopted DSP/FPGA control board in this thesis.

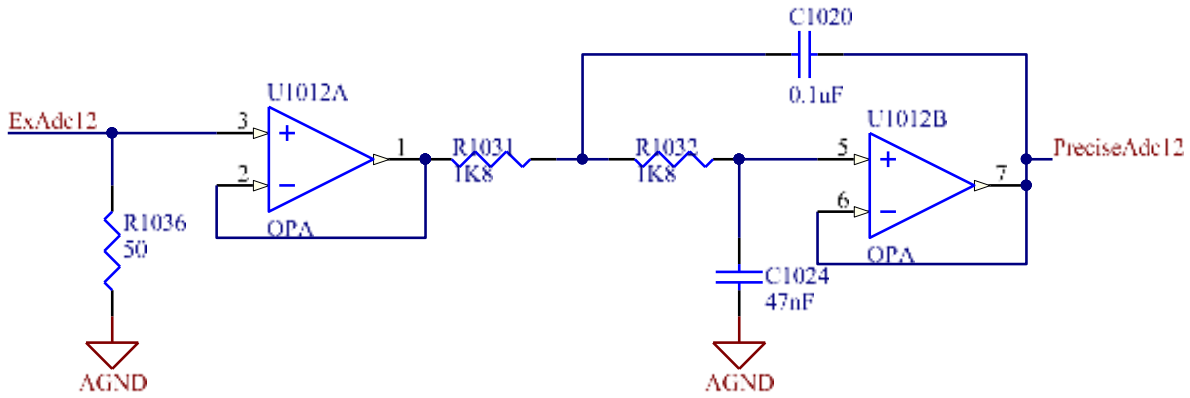
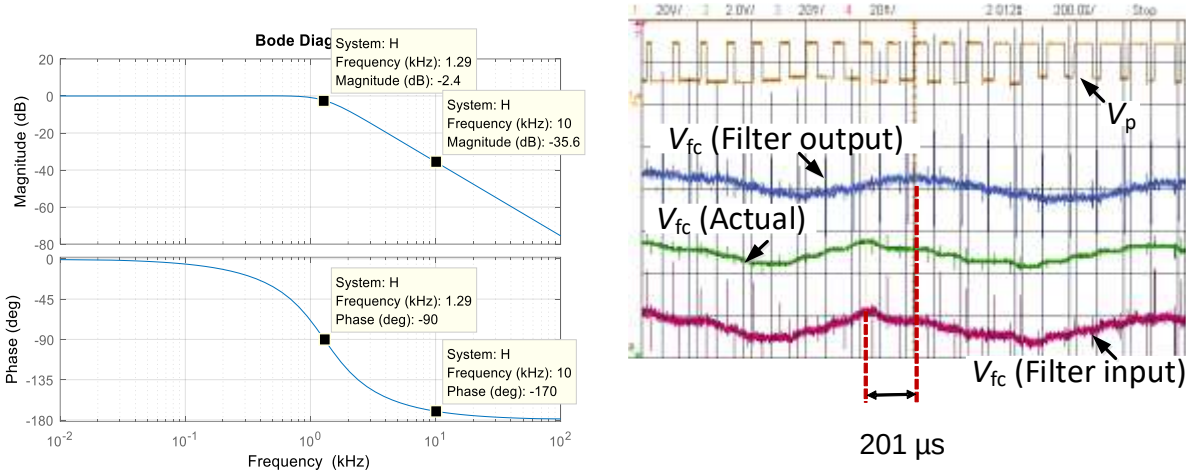
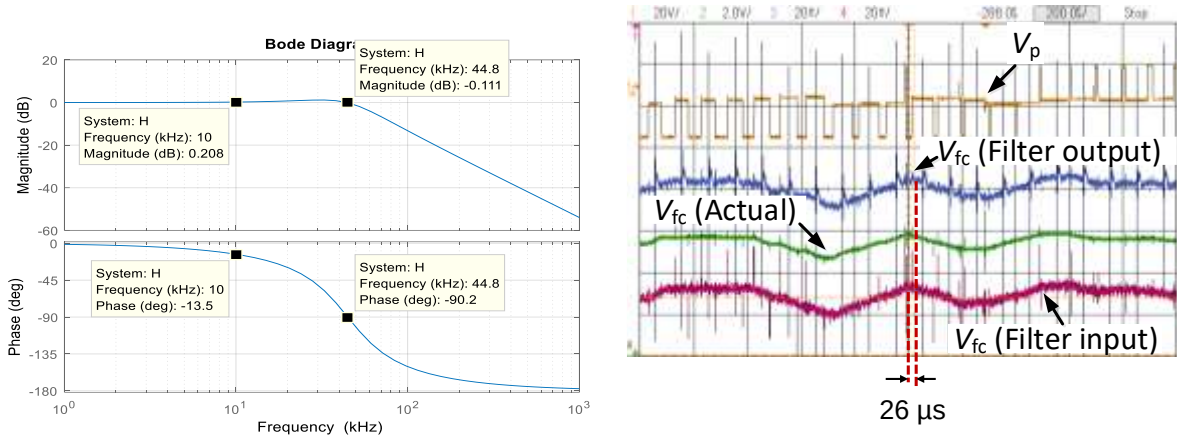


Fig. A.F.II Schematic layout of the ADC input filter with the default setting

With the setting in Fig. A.F.II, the cutoff frequency of the low pass filter is 1.29 kHz as shown in Fig. A.F.III (a). Fig. A.F.III (b) shows the actual FC voltage waveforms (green) compares with the FC waveform signal that ADC achieved after the filter (blue). There is a 201μs delay between them due to the original ADC input filter setting. This delay will cause some inaccurate switching actions related to the FC voltage control (high speed control). Some point which requires a discharging switching action may result a charging switching action due to the sampling signal delay. This will affect the optimum selection of the FC size. Therefore, some modifications have been made on the ADC filter. Replace C1 with 3.9nF capacitor, and C2 with 1nF capacitor, the cutoff frequency of the new filter setting is 44.774 kHz as shown in Fig. A.F.III (c). Consequently, the actual delay between FC voltage and the ADC captured signal has been reduced to 26 μs as shown in Fig. A.F.III (d). This new setting can make the FC voltage control more accurate and make it possible to optimize the FC size.



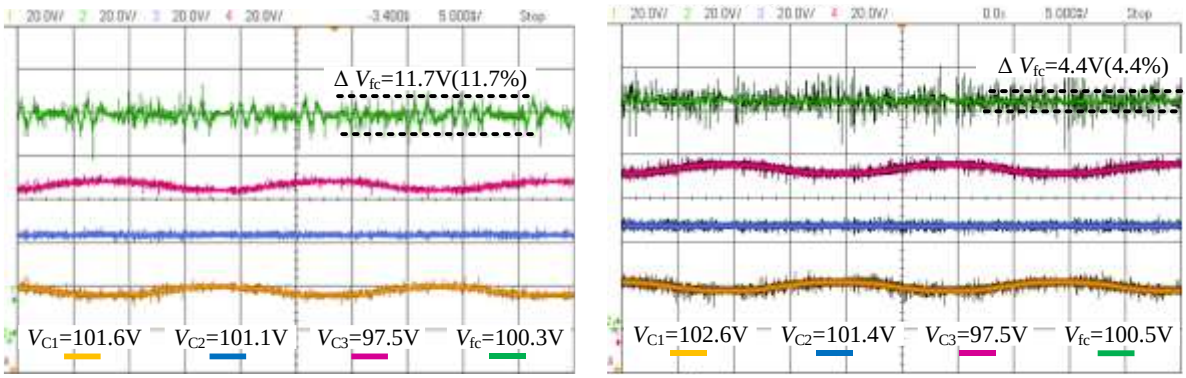
(a) C_1=100nF, C_2=47nF, f_c=1.289 kHz, Q=0.7293



(b) C_1=3.9nF, C_2=1nF, f_c=44.773 kHz, Q=0.987

Fig. A.F.III Comparison between (a) the original ADC input filter setting and (b) the modified one

Fig. A.F.IV presents the comparison of the FC voltage waveforms of the actual operation of the single-phase hybrid four-level π-type converter between the original ADC input filter setting (Fig.A.F.IV (a)) and the modified ADC input filter setting(Fig.A.F.IV (b)). It is obvious, that the voltage ripple on the FC voltage has reduced from 11.7% to 4.4% under when C_{FC}=50µF and I_o=5.7A. This is due to the time delay between the actual FC voltage and the ADC captured signal has been significantly reduced, consequently, the mis-switching actions have been prevented.



(a) (b)

Fig. A.F.IV FC voltages comparison between (a) the original ADC filter setting and (b) the modified ADC filter setting

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