Buffer optimization for wide-bandgap RF and Power devices

Buffer Behaviour, Kink Effect, Charge Transport and Future Devices

By

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Abstract

The core of high performance and reliable operation of wide bandgap devices lie in the design of buffer layers. This thesis is primarily focused on the impact of the buffer on the operation of AlGaN/GaN HEMTs, devoted to both RF GaN on Silicon Carbide (SiC) and power switching GaN on Silicon devices. The demand for higher power is increasing which requires improvement at the material and device level. Nominally undoped GaN is usually slightly n-type due to Nitrogen vacancies and impurities such as Oxygen acting as donors. A dopant such as Iron (Fe) and Carbon is used to make the buffer more insulating. Fe, an acceptor with the energy of 0.72 eV below the conduction band, sits on the Nitrogen site and has been quite successful in achieving an insulating buffer resulting in good RF performance. Carbon, on the other hand, is a better choice for the power industry which requires high breakdown voltages and has been able to deliver resistivity as high as 10^{13} Ω.cm. However, Carbon is a deep acceptor when on the Nitrogen site (C_N) with an acceptor trap level 0.9 eV above the valence band making the buffer p-type. A p-type buffer underneath the 2DEG forms a vertical p-n junction which can make the buffer float and act as a reservoir for time-dependent charge storage. A background level of Carbon will inherently be incorporated during GaN growth due to the presence of organic carrier gases in MOCVD. It is the role of this background Carbon in Fe doped buffer layers and its subsequent consequences, which forms the crux of this thesis.

Wafers with all parameters identical but for the background Carbon level has been subjected to DC, Pulse I-V, transient and breakdown studies yielding valuable information about conduction mechanism in the buffer. Kink effect, which is a hysteresis in the output characteristics of a transistor, is shown to be strongly dependent on background Carbon density. An explanation based on a "leaky dielectric" model of a floating semi-insulating GaN buffer together with conventional Fe and C deep-level defects has been tested and applied successfully. The proposed model is a more realistic approach in comparison to two other models reported in past which are based on unusual deep level defect properties and cannot be explained by conventional defect models. The proposed insight into the mechanism for kink offers a route to its control and suppression. Positive and negative magnitude drain current transient signals with 0.9 eV activation energy have been seen, corresponding to changes in the occupation of Carbon acceptors located in different regions of the GaN buffer. The observation of such signals from a single trap type also raise questions on conventional interpretations of these transients based on the bulk 1-D deep-level transient spectroscopy (DLTS) models for GaN devices with floating regions.

These wafers showed very different Pulse I-V behaviour which can be explained based on their buffer doping; however, under RF IV measurement they appeared identical. This absence of correlation between Pulsed and RF IV brings into question the applicability of Pulsed I-V measurements alone as a tool for extracting nonlinear device models in the case of GaN HEMTs, which is a widespread practice. Drain injected breakdown study on these wafers resulted in the identification of the two-step process, one initiated by a leakage path between the source and drain and other due to electron punch-through current. Simulations and Electroluminescence studies under operation confirmed impact ionization, with its impact being much smaller compared to punch through.

Effect of Carbon doping on buffer behaviour for GaN on Silicon devices aimed for power applications has also been evaluated, using stepped and ramped substrate bias. For the first time, experimental evidence of lateral charge spreading beyond the active area of the device and its impact on neighbouring devices has been explained. The lateral charge spreading beyond the active area can be a concern for wafer level reliability or system integration.

The last two Chapters introduces two possible next-generation RF transistors. GaN on diamond transistors with ultra-thin GaN and diamond as a heat sink has been shown with excellent thermal and electrical performance. As an alternative, a new wideband gap material Gallium Oxide (β-Ga_2O_3), which could be a choice for future RF device has been evaluated using Pulse I-V and large signal RF. These devices show minimal surface and buffer trapping, yielding a record RF performance. However, poor thermal conductivity is the performance limiting factor, which if countered well can lead to a promising material for future devices.

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AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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- **Manikant Singh**, M. Casbon, M.J. Uren , J. Pomeroy , S. Dalcanale, S. Karboyan, P. Tasker, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki,and M. Kuball, "Pulsed Large Signal RF Performance of Field-Plated $Ga_2\ O_3$ MOSFETs" *IEEE Electron Device Letters*, Vol. 39, No. 10, October 2018, DOI 10.1109/LED.2018.2865832.

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- **Manikant Singh**, M.J. Uren, S. Karboyan, H. Chandrasekar, T. Martin, and M. Kuball, "Misinterpretation of Drain Transient Spectroscopy in GaN HEMTs: Explanation using a floating buffer model" *Digest CS Mantech*, Minneapolis, MN, USA, 2019.

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- **Manikant Singh**, M. Casbon, C. Middleton, S. Karboyan, J. Pomeroy, M.J. Uren and M.Kuball, "Ultra-thin GaN-on-Diamond with excellent RF and thermal performance" *United Kingdom Nitrides Consortium UKNC, Glasgow, Jan. 2019.*

- **Manikant Singh**, M.J. Uren, H. Chandrasekar, S. Karboyan, T. Martin, and M. Kuball, "Multiple drain-current-transient responses from the same trap: explanation using floating buffer model" *International Workshop on Nitride Semiconductors, Kanazawa, Japan,2018.* ***Invited talk***

- **Manikant Singh**, M.A. Casbon, M.J. Uren, J.W. Pomeroy, P.J. Tasker, M.H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki and M. Kuball, "Pulse and Large Signal RF Performance of β-Ga_2O_3 MOSFETs" *Electronic Materials Conference, Santa Barbara, CA,2018.*

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- **Manikant Singh**, M.J. Uren, T. Martin, S. Karboyan and M. Kuball, "Kink" in AlGaN/GaN-HEMTs: Floating Buffer Model, *United Kingdom Nitrides Consortium UKNC, Manchester, Jan.2018.*

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- **Manikant Singh**, J. Pomeroy, M. Casbon, T. Moule, S. Dalcanale, S. Karboyan, M.J. Uren, P. Tasker, M.H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki and M. Kuball, "Record large signal RF performance for β-Ga_2O_3 MOSFETs" *United Kingdom Nitrides Consortium UKNC, Glasgow, Jan.2019.* ***Best Poster award.***
- **Manikant Singh**, T. Martin, M.J. Uren and M. Kuball, "Kink" in AlGaN/GaN-HEMTs: Impact on Devices and Demonstration of Suppression, *International Conference of Nitride Semiconductors ICNS 11, Strasbourg, France, 2017.*

CHAPTER 1

INTRODUCTION

Human life today revolves around technology, the majority of which is driven by electronics. Discovery of the transistor by Shockley, Bardeen and Brattain in 1947 single handedly revolutionised the electronics industry [1] [2]. Constant demands for improvement has led to rapid developments in terms of efficiency and power capabilities of electronic switching devices. However, with increasing electronic industry improvements and population, the energy demands are rising rapidly as well. One estimate put the worldwide electricity consumption to be double by 2035 [3]. Ironically 25% of all the electricity produced is lost, primarily due to inefficient load technologies and poor power electronics [4]. Majority of these power converters have primarily been based on Silicon due to maturity in CMOS process and development of device design from three terminal transistor to HV insulated-gate bipolar transistor (high voltage IGBT). They have been used extensively in power supply, motor drives and HV traction lines. However, the ever-increasing demand for higher power, switching speeds, compact systems and better efficiency, resulted in the quest for new materials.

Lot of work has been put into an understanding of new materials especially with a higher bandgap than Silicon. Silicon Carbide (SiC) and Gallium Nitride (GaN) were two apparent choices, primarily because of their higher bandgap. Fig.1.1 shows a comparison for SiC and GaN with Silicon based on several parameters [5]. For high power one of the critical parameters is material breakdown strength. As seen, compared to Silicon, GaN has 10 times higher breakdown field, meaning devices made out of GaN can withstand 10 times more voltage than a Silicon device with the same physical dimension. This makes GaN the obvious choice not only for higher power but for compact systems size as well. Combining high electric breakdown with high mobility (1150 for bulk and 2000 cm^2/V.s for a 2D electron gas) further makes GaN ideal for fast switching and high voltage. In terms of material properties, SiC has better thermal conductivity than GaN;

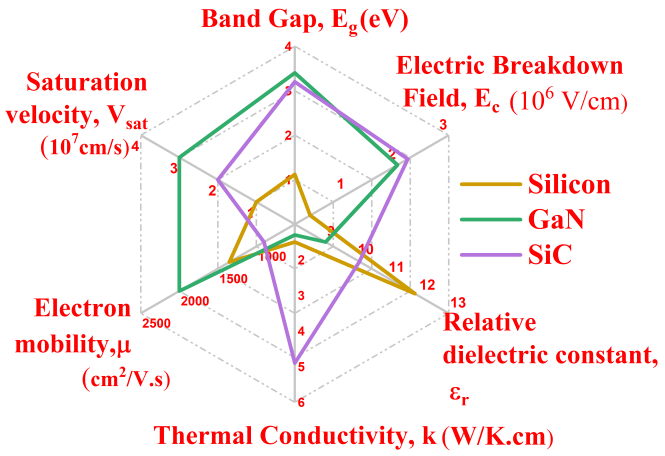

Figure 1.1: The spider diagram showing the critical material properties comparing Silicon, GaN and SiC compiled based on values reported in [5].

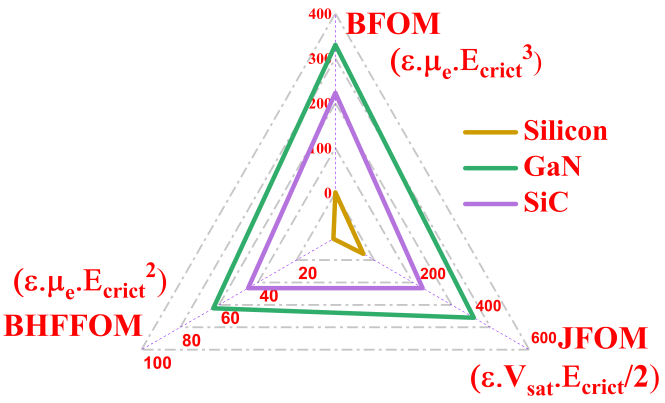

Figure 1.2: The spider diagram showing the comparison for different FOM's for Silicon, GaN and SiC [5].

however, this has been improved by integration of GaN on non-native substrates such as SiC, making use of its excellent thermal conductivity. Several application-specific figures of merit have been proposed in order to evaluate the suitability of different materials. Baliga Figure of Merit (BFOM) which is the product of dielectric constant, mobility and critical electric field defines the resistive losses, defining the ultimate power handling capability of the material. Similarly, Johnson Figure of Merit (JFOM) which is a product of saturation velocity and critical electric field represents the frequency and power handling capability of the material. There is another Baliga Figure of Merit for a high-frequency (BHFFOM) devices which compares mobility with the square of the critical electric field defining switching losses in the material. GaN is better

on all the FOMs as compared to Silicon for high-power, high-frequency applications as shown in Fig.1.2. An additional advantage is the ability of GaN to form heretostructures which will further increase mobility, making GaN the preferred choice against Silicon and SiC.

Despite all the above advantages in terms of the material properties of GaN, it has been a long journey for the commercialisation of GaN transistors. Lack of available technology to grow large area GaN substrates and the high costs involved in focused research efforts on the heteroepitaxy of GaN thin films on foreign substrates, gave rise to a large defect density in these films. In 1968, Maruska and Tietjen demonstrated the first reports on substantial area Gallium Nitride material on Sapphire substrates [6]. The majority of GaN films grown during that period showed high electron concentration even without any intentional doping; however, to create a p-n junction a suitable p-type dopant had to be found. In 1989, *Akasaki et al.* used Magnesium as a dopant to show the first p-type GaN films [7]. Later *Nakamura et al.* by use of high-temperature annealing in Nitrogen ambient showed much improved p-type conducting GaN films [8]. In the meantime, *Amano et al.* further improved the material quality of GaN on Sapphire substrates using a low temperature AlN nucleation layers [9]. These discoveries were game changers in what led to the development of blue LEDs enabling ultimately white LEDs. All three of them were awarded the Nobel prize in 2014 for their immense contributions to the area. Developments of good epitaxial layers also led to the discovery of two-dimensional electron gas in AlGaN/GaN heterojunction. The roadmap since the first discovery of AlGaN/GaN HEMT till the present date is shown in Fig.1.3.

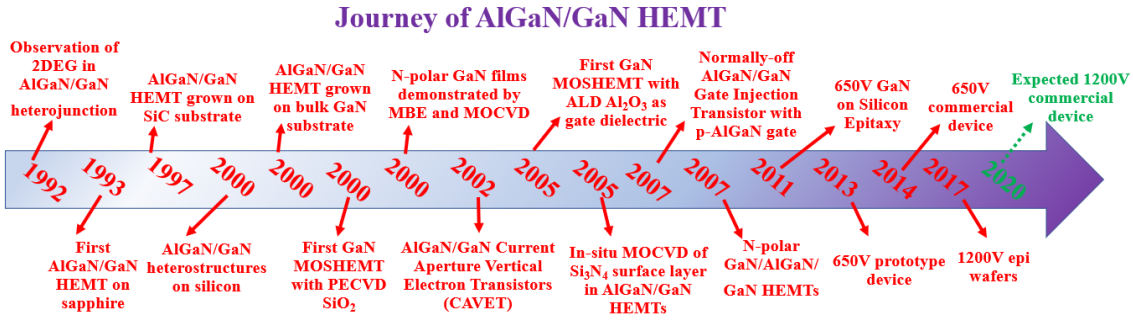

Figure 1.3: Evolution of AlGaN/GaN HEMT over the years [10], [11].

Khan et al. demonstrated 2DEG formation in AlGaN/GaN grown using low-pressure MOCVD for the first time, followed soon by the creation of first AlGaN/GaN HEMT transistor on Sapphire [12]. Due to poor thermal conductivity soon Sapphire was replaced with SiC which had a much better thermal conductivity (4.9 W/cm.K) and lattice mismatch (3.5%). Due to its superiority in terms of lattice mismatch, it resulted in the average dislocation density of 10^{-8} cm^{-2} for GaN epitaxy grown on SiC making it the obvious choice for state of the art GaN devices for high performance which is true even today [13]. However, the lack of large area substrate and higher cost led to look out for a new substrate such as Silicon. Silicon had an added advantage

of mature device processing capabilities and a vast pool of electronic components which could make the system integration much more straightforward. Even with inferior lattice mismatch (17%) and thermal conductivity compared to SiC it soon became the obvious choice of substrates for power switching simply because of it being the cheapest of all available substrates. *Kaiser et al.* demonstrated the first AlGaN/GaN HEMT on Silicon (111) substrate containing an AlN high-temperature buffer layer [14]. Though GaN HEMT on Silicon has been demonstrated, the significant thermal expansion coefficient mismatch (52%) created tensile strain in the epitaxy leading to large wafer bow and cracks making device processing difficult. This issue was resolved using a combination of AlN and GaN layers as the stress mitigation layer countering the tensile and compressive stress during the growth and upon the cool down. Since then several approaches have been demonstrated leading to smaller bow and better quality of films [15] [16].

Device design has improved along with epitaxial growth, with the implementation of field plate, better gate design and passivation techniques. Field plates are aimed to work as additional gate regions, aiding in distributing the potential drop across the whole gate-drain gap, maximising the device breakdown capabilities and is used extensively in GaN high power transistors. Several gate technologies such as tri-gate and recessed gate have been used to achieve positive threshold voltage making normally off devices which usually are depletion-mode due to the presence of spontaneous and piezoelectric polarization [17] [18].

Even though present AlGaN/GaN HEMTs are dominating high power and switching market, device reliability is still a concern. With high voltage operation, the defects induced during the growth or defects within the crystals, or in the dielectric used during fabrication can act as a site for degradation. Most of the surface related effects have been optimised by the use of better gate design, improved field plate and passivation schemes; however, the buffer still remains as a focus of research. The GaN buffer which acts as a back barrier constraining 2DEG to remain at AlGaN/GaN interface and withstand high off-state source-drain leakage is often doped with deep level traps such as Iron (Fe) and Carbon (C). For RF applications, Fe doping is used with a density of $\sim 10^{18}\ cm^{-3}$ in the bulk of the GaN to suppress off-state bulk leakage. It turns out that this choice has the benefit of largely suppressing bulk current-collapse [19]. For the case of power devices, Fe doping cannot deliver sufficiently high off-state drain leakage or breakdown voltage (this is partly because it's trap energy level is too shallow); hence the use of Carbon. Typically density of around $10^{19}\ cm^{-3}$ is used to give lower off-state leakage and higher increased breakdown voltages [20]. Although these doping schemes do their job in improving the device performance, their role is not entirely understood yet. For example, Carbon doping does deliver a highly insulating buffer and high breakdown voltage; it is also highly vulnerable to current-collapse (CC). CC defines the state where a device on-resistance significantly increases after been held in the off state. This recovery process can take anywhere between milli seconds to more than 1000 seconds which is undesirable for safe device operation. Carbon is also inevitably present in the MOCVD during growth and even a small concentration of background Carbon

along with Fe can cause trapping during device operation.

It is this area of doping in buffer layer of GaN HEMTs which is the main focus of study in this thesis. The second Chapter of the thesis explains the theory and background required for an understanding of AlGaN/GaN HEMT. This Chapter discusses the formation of 2DEG, working of the transistor, different doping schemes and several reliability issues of present day GaN HEMTs. The next three Chapters (Chapter 4, 5 and 6) discuss different reliability issues for primarily Fe doped AlGaN/GaN HEMT on SiC. The two identical GaN-on-SiC wafers processed with identical layer structures incorporating nominally identical Fe doping to suppress punch-through, but with different growth conditions resulting in bulk Carbon levels of 3x10^{17} and 2x10^{16} cm^{-3}. The high Carbon density wafer showed a kink in the output characteristics, whereas the low Carbon density wafer showed no kink. It is these two wafers which have been used for the study reported in this thesis for Chapters 4, 5 and 6. In Chapter 4, a new floating buffer model to explain "kink", an undesirable hysteresis in the output characteristics of AlGaN/GaN HEMTs observed at low drain bias, has been reported. Presence of unintentionally incorporated background Carbon (C) can make the intentionally Iron (Fe) doped buffer p-type, allowing it to float electrically. The supply of holes to charge the buffer arises due to a band-to-band trap-assisted leakage path rather than via impact ionization, which will be a dominating factor at higher fields. Simulations of the kink show that it can be enabled and modified by small changes in the concentration of background Carbon that are well below the Fe density. The measurements on two wafers with different background Carbon having dramatically different kink behaviour are entirely consistent with the simulated model. Chapter 5 reports the usability of Pulsed I-V technique as a tool for accurately extracting nonlinear models. DC and Pulsed I-V performed on the exact two wafers (as in Chapter 3) showed dramatic dispersion in knee region suggesting different trapping behaviours. However, under radio frequency (RF) I-V waveform measurements, utilizing active harmonic load-pull they showed identical RF knee. Both wafers gave 4 W/mm RF power at 1 GHz, and ~70% power added efficiency (PAE). The absence of correlation between Pulsed I-V and RF measurements raises a question about the applicability of Pulsed I-V measurements alone as a tool for extracting nonlinear device models in the case of GaN HEMTs. Further, in Chapter 6, breakdown (BD) study using a drain current injection technique has been reported. Simultaneous measurements of the drain, source and gate currents allows the direct evidence of high source current injection under off-state condition through the buffer, surprisingly giving higher measured source current than gate current indicating the leakage through the buffer. Electron punch-through from the source side under high current injection has been assigned as the reason for the breakdown. Electroluminescence imaging and spectroscopy has been performed to understand the localisation of charge within the device and simulations has been used to validate the experimental study. Chapter 7 reports on lateral charge spreading for Carbon doped GaN on Silicon aimed for power applications. Substrate ramp measurement technique used for evaluating charge storage in buffer, shows area dependence, suggesting that lateral charge

spreading has occurred beyond the active physical area of the device. This has been measured experimentally for the first-time, showing effect of lateral charge spreading as wide as up to 2 mm much beyond the physical area of the device and with longer recovery times. Charge spreading beyond active area can be a severe concern for wafer level reliability or system integration when different devices share the same epitaxy. Next generation of GaN RF devices are studied in Chapter 8. This work evaluates the impact of thinning GaN buffers on the performance of GaN-on-Diamond devices. In spite of thinning of buffer, the electrical performance has remained intact while Diamond has aided the thermal performance. We demonstrate minimal trapping and excellent large signal RF performance at 1 GHz for ultra-thin GaN-on-Diamond technology. These results demonstrate successful integration of ultra-thin GaN-on-Diamond bringing Diamond closer to the active region of the device, making it thermally efficient without compromising electrical switching performance. Obtained electrical and thermal results puts this work among the state-of-the-art GaN RF devices. Chapter 9 explores a new wide bandgap material β-Ga_2O_3. A brief literature review followed by Pulsed I-V evaluation and large signal RF measurement on β-Ga_2O_3 MOSFET is presented. Good pulse performance with minimal trapping is shown with record RF performance at 1 GHz; however, both DC and RF performance are severely limited due to poor thermal conductivity. Given this is a relatively new material and still evolving, a lot of these issues can be resolved as the technology becomes mature in future. The overall conclusions are reported at the end as Chapter 10.

CHAPTER 2

THEORETICAL BACKGROUND

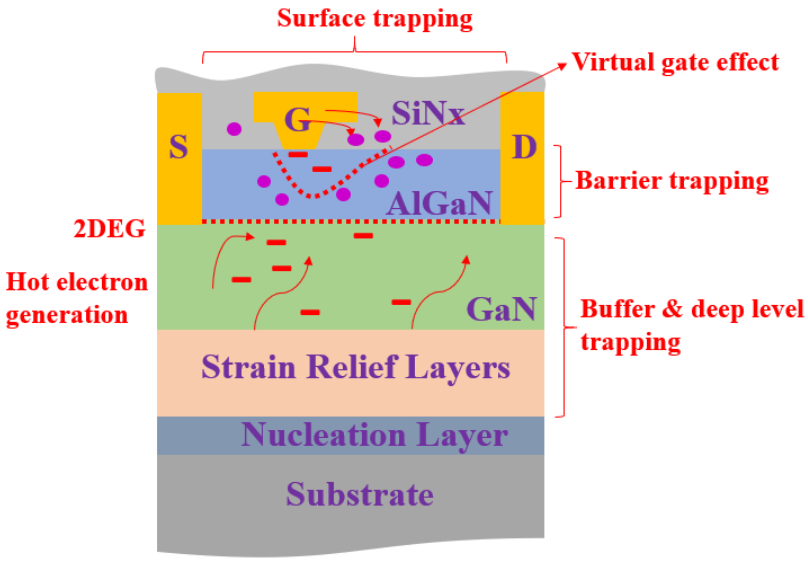

Figure 2.1: Schematic of AlGaN/GaN HEMT highlighting several issues associated with it.

This chapter explains materials properties, polarization in heterostructures and details in particular about AlGaN/GaN High Electron Mobility Transistor (HEMT). Method and challenges involved in HEMT epitaxial growth and device fabrication is discussed. Outline for merits and needs of good switching device is discussed explaining the suitability of AlGaN/GaN HEMT as a most promising candidate. Key current challenges such as trapping, breakdown and leakages are explained along with examples from recent advancement in terms of handling them. This chapter with all the details as shown in the schematic in Fig.2.1 is aimed

to provide the theoretical basis for experimental chapters to follow which discuss these issues in more detail.

2.1 Material properties

2.1.1 GaN Crystal structure

Group III-nitrides like AlN, GaN, and InN can crystallise into either wurtzite, zinc-blende or rock salt crystal structures. GaN crystallises in the cubic zincblende or hexagonal wurtzite primitive cells and produces a rock-salt structure only under high pressure. However, of all three at ambient conditions, the wurtzite structure as shown in Fig.2.2 (a) is the thermodynamically more stable phase than zinc blende with a calculated 13 meV/cation lower total crystal energy [21]. The majority of work throughout the thesis is also focused on the wurtzite structure.

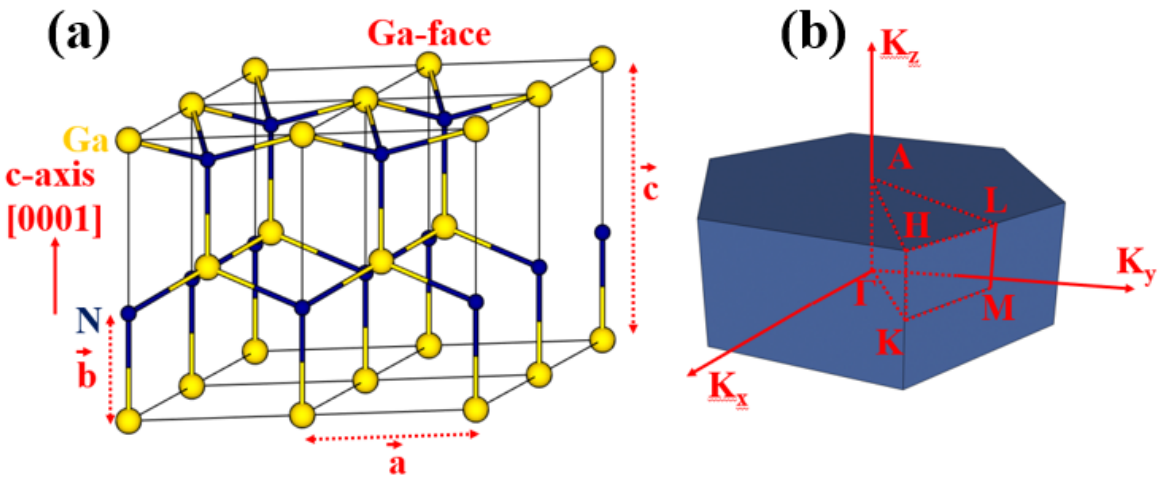

Figure 2.2: (a) Schematic wurtzite crystal structure of GaN in real space; (b) Brillouin zone of a hexagonal crystal with selected symmetry points, with k_x, k_y, and k_z as components of the wave vector k [22][23].

The wurtzite structure consists of two interpenetrating hexagonal close-packed lattices of either Ga or N atoms which are shifted concerning each other ideally by 5/8 along the c-axis [24]. The unit cell of the wurtzite lattice is hexagonal with a basis of two Gallium (Ga) and two Nitrogen (N) atoms. This structure is non-centrosymmetric meaning there is no inversion symmetry in this lattice along the c-axis, represented by vector pointing from a Ga atom to the neighbouring N atom [25]. The material grown along [0001] directions is called Ga-polar with vector pointing from Ga to N. Whereas N polar is grown in the opposite directions eventually turning out as mirror image to Ga polar structure with identical atom on same plane and side of the bond. Hence, wurtzite GaN crystals have two distinct faces, (0001) plane depicts the Ga face, while (000_1) corresponds to the N face, referring to the atomic sheet terminating the crystal.

The surface properties in terms of chemical behaviour and thermal stability are strongly affected depending on whether the structure is Ga or N polar. Most of the high-quality growth is done using Ga-face since N-face material growth has proved to be challenging. The lack of inversion symmetry also gives GaN an intrinsic polarization providing different surface chemistry and adatom mobilities for different crystalline faces [26].

The first Brillouin zone of the wurtzite structure which corresponds to the Wigner-Seitz cell of the reciprocal lattice is a hexagonal prism as illustrated in Fig.2.2(b). The Γ point denotes the centre of the Brillouin zone with the reciprocal lattice vector k =0. Here, k represents the wave vector and k_x, k_y, k_z denote the axes of the Cartesian coordinate system in the momentum space [22][23].

The band structure of GaN, calculated via the empirical pseudo potential method [27], is shown in Fig.2.3. The diagram shows energy band values for points along the Wigner-Seitz cell, i.e. varying k. With the minimum of the conduction band, Ec and the maximum of the valence band Ev coinciding at the centre of the Brillouin zone, which is also located in the middle of the band structure the Γ-point making GaN a direct bandgap material. The combination of direct bandgap and gap of 3.4 eV makes GaN useful material properties such as high hardness (10.2 GPa), high thermal conductivity (230 W/mK at room temperature) and high breakdown field (~5x10^6 V/cm). Making it the preferred choice of electronic and optoelectronic devices [28].

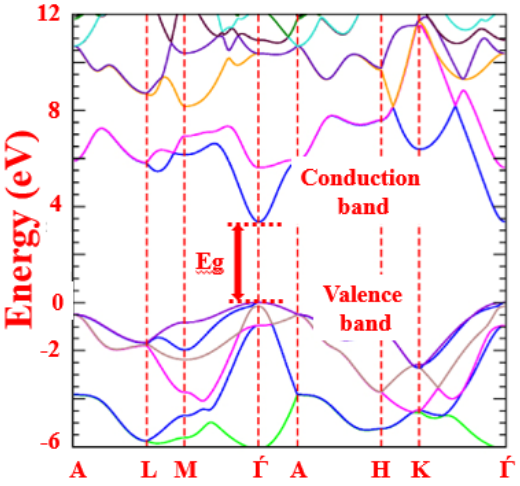

Figure 2.3: The electronic band structure of Wurtzite GaN calculated using the lempirical pseudo potential method [27].

2.1.2 Polarization effects in Nitrides

Nitrogen, the smallest and the most electronegative Group V element together with Gallium and its different electronegativity induces a polar behaviour in each Gallium-Nitride crystal. The

polarization exists for nitride semiconductors in both the zincblende and wurtzite phases. There are two types of polarization:

- Spontaneous Polarization (P_{SP}).
- Piezoelectric Polarization (P_{PZ}).

In case of absence of an external electric field, the total polarization is given by:

$$P_{total} = P_{SP} + P_{PZ} + P_{ext} \tag{2.1}$$

1. ***Spontaneous Polarization (P_{SP}):*** P_{SP} represents the intrinsic polarisation field of an unstrained crystal. The polarization properties are strongly connected to the unit cell symmetry of the crystal. Electrons involved in the nitrogen covalent bond will be strongly attracted by the Coulomb potential of the N atomic nucleus due to lack of electrons occupying the outer orbitals. This strong ionicity of metal-nitrogen bonds along with the absence of inversion symmetry results in macroscopic polarization along the [0001] direction and is called spontaneous polarization [29].

2. ***Piezoelectric Polarization (P_{PZ}):*** Most of the layers grown are often under strain due to lattice mismatch with the underlying layers. In the presence of any stress applied to the lattice, the ideal lattice parameters (c_0,a_0) will change. This additional polarization due to strain-induced distortion of the crystal lattice is called piezoelectric polarization [30]. The piezoelectric polarization field described by Hooke's law, P_{PZ}, is expressed as:

   $$P_i^{pz} = \sum_j e_{ij}\epsilon_{ij} \tag{2.2}$$

   Where piezoelectric constants are e_{ij} and deformation of a crystal ϵ_j. The equation shows that the polarization tensor of the material is linearly dependent on macroscopic polarization which is induced due to changes in the dipole moment along the [0001] axis by applied strain. The two different types of stress applied on Nitride crystal will be as shown in Fig2.4:

   - **Bi axial compressive stress**: For bi axial stress, the total polarizations will decrease given the piezoelectric and spontaneous polarizations will act in opposite directions as shown in Fig.2.4(b).
   - **Tensile stress**: In case of tensile stress, the total polarizations will increase because spontaneous polarizations and Piezoelectric Polarization will act parallel (same) to each other Fig.2.4(c).

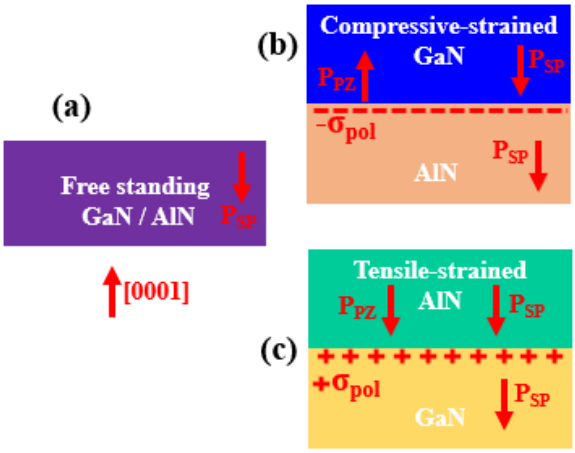

Figure 2.4: The directions of the spontaneous and piezoelectric polarization vectors for an undoped GaN and AlN under free standing (a), compressive strain (b) and under tensile strain (c) is shown.

2.1.3 Polarization in Heterostructure

Heterostructures are composed of two or more semiconductors with different energy gaps, leading to a discontinuity of conduction and valence band at the interface and therefore to a band offset. In the case of GaN, the incorporation of AlN into the material creates the alloy AlGaN, whose bandgap can be varied according by changing Aluminum (Al) concentration in the alloy. The bandgap energy can then be expressed.

$$E_g(x) = xE_g(AlN) + (1-x)E_g(GaN) - bx(1-x) \tag{2.3}$$

x here represents mole fraction for AlN, E_g (AlN)= 6.2 eV and for GaN= 3.4 eV, b is the bowing parameter [31]. The band gap of GaN is narrower in comparison to that of AlN. Any abrupt change via incorporation of Al into GaN will result in abrupt band offset at the semiconductor heterointerface which will be a step-like function. It is this difference in the polarizations across the heterointerface which is responsible for creation of interface charge accumulation which is called as the Two-Dimensional Electrons Gas (2DEG) as shown in Fig.2.5. Along with creation of 2DEG this difference also affects the band structure creating charge depletion regions.

For the two strain cases shown in Fig.2.4 (b) and (c) the formation of 2DEG will be:

AlN strained on GaN: In this case, both the difference in spontaneous and piezoelectric polarization lies in the same direction, leading to an increase in total polarisation at the interface. This leads to the formation of a two-dimensional electron gas (2DEG) in GaN by rearrangement of free carriers. The corresponding band diagrams is shown in Fig.2.6.

GaN strained on AlN: Conversely, when GaN is compressively strained on an AlN buffer layer, the polarization difference has opposite signs which leads to decrease in total polarization

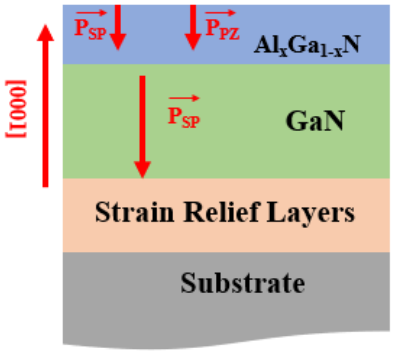

Figure 2.5: The directions of the spontaneous and piezoelectric polarization vectors AlGaN/GaN HEMT under tensile stress.

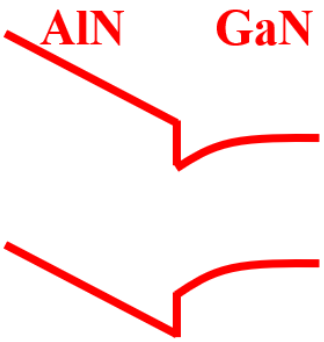

Figure 2.6: Potential profile for AlN strained on GaN.

and hence creation of depletion region in the GaN.

2.1.4 Polarization in AlGaN/GaN case

Now consider a Ga-face AlGaN/GaN structure, based on the Fig.2.7 below there is a difference in the lattice constant which we know causes a lattice mismatch at the heterointerface resulting in biaxial tensile strain in the AlGaN layer [32]. From previous explanation we know under tensile stress, the polarization fields in the AlGaN and GaN layers are parallel and pointing towards the substrate as shown in Fig.2.4. These combined polarizations, in turn, induce an excess of free-moving electrons in the Gallium Nitride. The electrons concentrate near the polarization region, hard against the Aluminum Gallium Nitride but without straying into it because the material's higher bandgap acts as a barrier. This leads into formation of a two-dimensional "gas" (2DEG) of charge-carrying electrons on the GaN side of the heterojunction, close to the boundary with the Aluminum as shown in Fig.2.8 [33]. The induced polarisation sheet charge density σ

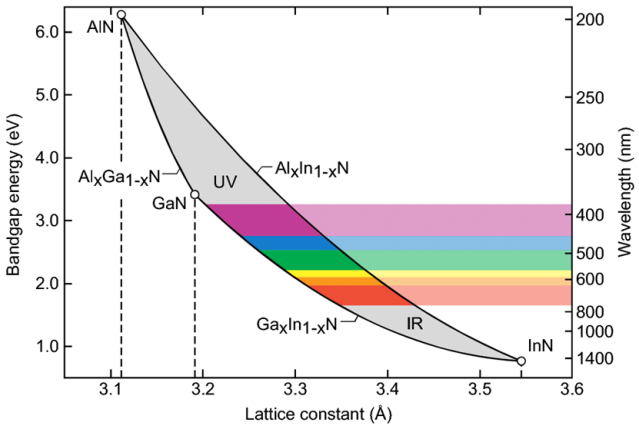

Figure 2.7: Lattice constant vs bandgap for GaN, AlN and AlGaN is shown [32].

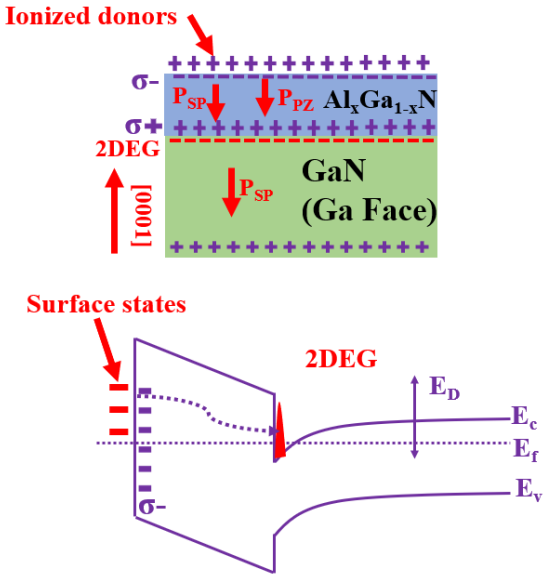

Figure 2.8: Band diagram and schematic of polarization charge at AlGaN/GaN HEMT induced by polarization along with schematic.

created AlGaN-GaN interface of the grown heterostructures along the c-axis (GaN) [34], shown in Fig.2.2 (a), can expressed as:

$$|\sigma| = |P_{SP-AlGaN} + P_{PE-AlGaN} - P_{SP-GaN}| \tag{2.4}$$

The surface states shown in Fig.2.8 are the source of the electrons in the 2DEG. Consider an undoped AlGaN with a surface state at an energy E_D below the conduction band edge and it is a donor like state meaning it is neutral when occupied and positive when empty. It is this donor states which pins the fermi level E_F at the surface. Typically there are up to $10^{13}\ cm^{-2}$ of positively charged donors on the surface.

2.2 AlGaN/GaN HEMT:

2.2.1 Epitaxy

Figure 2.9 shows example of an AlGaN/GaN HEMT stack, typical GaN HEMT epitaxy consists of a substrate, a Nucleation layer, Strain relief layer, GaN buffer layer, AlGaN Barrier layer and the top capping layer (GaN /SiNx). Majority of these epitaxies are grown using Metal chemical vapour deposition (MOCVD) or Molecular beam epitaxy (MBE). Role and challenges in each of these layers are as follows:

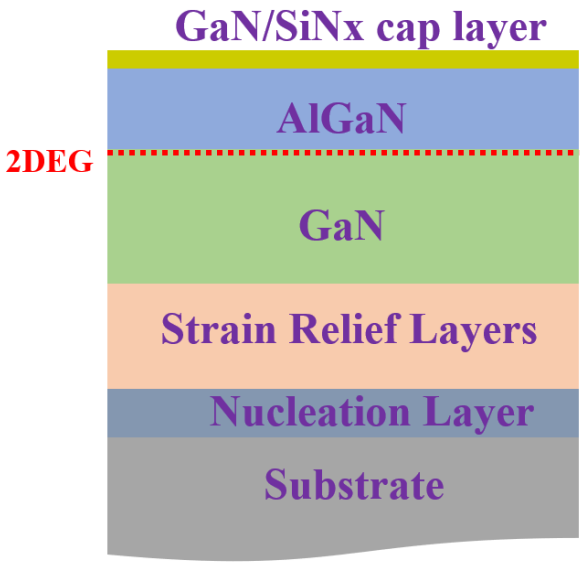

Figure 2.9: Shows example of an AlGaN/GaN HEMT stack, it consists of a substrate, a Nucleation layer, Strain relief layer, GaN buffer layer, AlGaN Barrier layer and the top capping layer (GaN /SiNx).

2.2.2 Substrate

Lack of native large area GaN substrates and the expensive cost involved has forced most of the growth on to non-native substrates. Several factors are considered in order to choose suitable substrate such as lattice mismatch, thermal conductivity, large area availability, cost, thermal expansion coefficient and ease of integration. The thermal expansion coefficient is one of the important parameters since most of the growth is done at elevated temperate which incurs strain in the material which upon cool down will either increase or decrease making it harder to obtain flat wafer surface required for processing. The table 2.1 shows comparison of most of the suitable candidates based on the suitable parameters mentioned before.

Based on table using lattice mismatch as parameter, SiC appears most suitable candidate among the foreign candidates however, the cost involved is the major problem. Currently majority

Properties	GaN	Silicon	SiC	Sapphire	Diamond
Bandgap (eV)	3.42	1.11	3.26	9.9	5.45
Thermal conductivity at 300K $k(W/cm-K)$	2	1.5	4.9	0.35	180
Lattice mismatch with GaN (%)	0	17	3.5	14	89
Thermal expansion coefficient (x10^{-6} K^{-1})	5.5	2.6	4.46	7.5	1.0
Substrate size	30	300	150	150	10
Substrate cost	Very high	Very low	High	Medium	Extremely high

Table 2.1: Comparison of different material and their suitability for growth of GaN [31].

of RF and power devices are based on GaN on SiC substrates specially in the field of low RF loss power amplifiers. Diamond among all offers best thermal conductivity but poor lattice mismatch, lack of large area substrates and cost makes the integration harder. Poor thermal conductivity of sapphire also makes it unsuitable for high power applications [35]. Silicon even with low thermal conductivity and lattice mismatch has been most favourable choice of substrates primarily due to large area substrates available and low cost. The mature semiconductor process based around silicon also makes the integration of devices in future much easier. However, for RF device the conducting substrate can be a problem as it can couple to the channel incurring in loss. This is main reason for the use of SiC substrate for most of RF devices.

Growth of GaN on silicon is performed using metal organic chemical vapour deposition (MOCVD) system or Molecular beam epitaxy (MBE). For manufacturing and ease of production, MOCVD process is preferred. The lattice and thermal mismatch between GaN and Silicon makes this much harder process to achieve. Before any growth, the silicon wafer is treated around 1000°C under hydrogen ambience to get rid of the native oxide from the surface [36].

2.2.3 Nucleation and Strain relief layer

Lattice mismatch between the substrate and the material will incur defects such as dislocations in large number as shown in Fig.2.10 (a) and (b). The dislocations percolates till the top as the material grows and later can act as path for leakages or trap sites putting device reliability at risk. The one way to reduce the dislocation is to grow suitable nucleation layer which can aid the growth. AlN is choice for growth of GaN on silicon, it also helps in preventing the melt back etching risk at higher temperatures between GaN and silicon [37] [38].

For GaN grown on SiC substrate this isn't a big problem primarily due to good lattice match between them. A typical stack on SiC includes nucleation layer mostly AlGaN followed by GaN buffer layer.

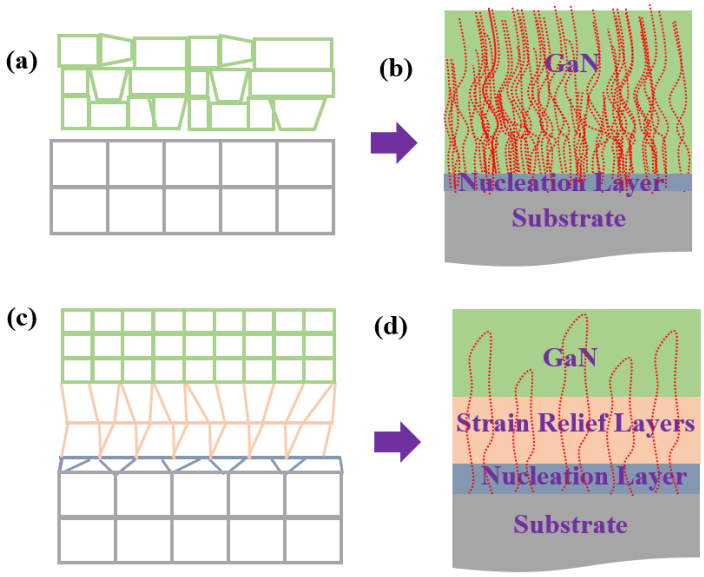

Figure 2.10: (a) Representation of lattice mismatch between GaN and substrate, (b) shows dislocation defects which will incur during the growth. (c) shows the use of nucleation and strain relief layer in countering the stress and help in reduction of dislocations as shown in (d).

The case for GaN on silicon is very different due to large lattice mismatch between them as seen in Table.2.1. To counter defects from lattice mismatch and thermal expansion coefficients stress engineering is performed by adding growth of strain relief layer or the transition layers shown in Fig.2.10 (c) and (d). Typically, these layers are graded AlGaN composition layer in different ways such as step graded, super lattices, linear graded or the slow growth process [37]. Each of these growth method offers its own advantages. The composition of AlGaN aids in reducing the dislocation density and the smaller lattice constant counters the stress in GaN during cool down process after high temperature growth.

2.2.4 Buffer layer

A semi-insulating or high resistivity GaN layer is grown to ensure proper drain-source current saturation, complete channel pinch-off, low leakages between adjacent devices. A thick GaN can also aid in achieving higher buffer breakdown voltages [31]. GaN on SiC aimed for RF device requires an insulating GaN layer to increase the breakdown (V_{BD}). The V_{BD} is defined by the subthreshold (I_{subth}) a current at which measured drain current goes beyond 0.1% of maximum drain current. Higher I_{subth} can lead to effects such as punch through. If the Fermi level in the buffer is closer to conduction band than under high off state conditions electrons can travel through the buffer bypassing the gate. This effects is defined as punch through, typically short channel devices are more prone to this effect [39]. Making buffer more insulating and confining the potential under the channel by adding extrinsic dopants is one of the ways to avoid punch

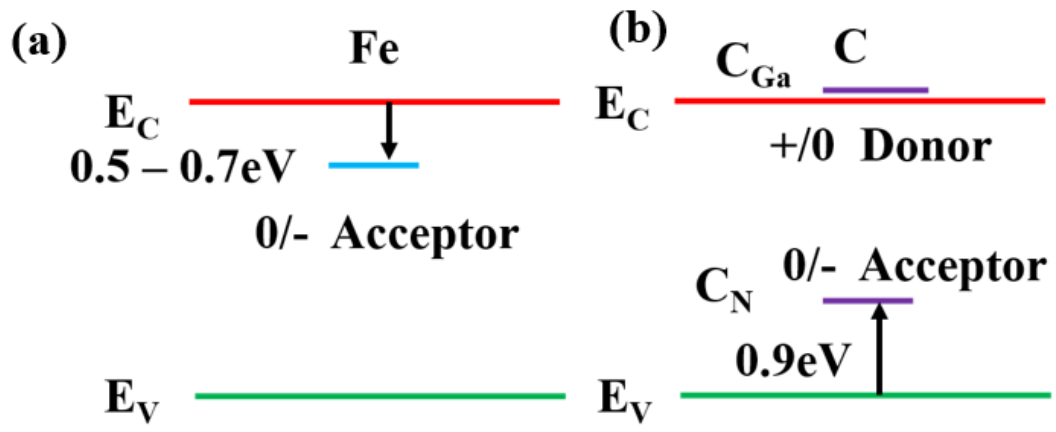

Figure 2.11: Band profiles for Iron (a) and Carbon (b) doped in GaN HEMTs.

through [40][39]. Most of the present day GaN on SiC RF devices uses Iron (Fe) as dopant. Fe with an energy of 0.72 eV below the conduction band sits on the nitrogen site making the buffer n-type due to Fe pinning of the fermi level (E_F) in the upper half of the gap as shown in Fig.2.11 (a) making electrons as majority carriers [19]. Use of Fe has resulted in excellent record RF performance however, there still are some challenges in terms of reliability which will be discussed later in this Chapter [41]. Power devices made on GaN on Silicon has different requirements. Breakdown voltages required are much higher and creates the need for making GaN buffer more insulating. Carbon is one of the preferred dopant choices with density above $10^{18}\ cm^{-3}$ for power primarily because it has better insulating properties much higher than Fe doped buffer. Based on reported literature carbon is a deep acceptor which on the nitrogen site (C_N) has an acceptor trap level 0.9 eV above the valence band and make the buffer p-type with majority of transport being through holes as shown in Fig.2.11 (b) [42]. Although this high insulating GaN:C does help in increasing the breakdown it also brings in issues such as current collapse or dynamic R_{ON}. This will be discussed later in this chapter.

2.2.5 AlGaN Barrier layer

The barrier layer typically is AlGaN which is wider bandgap than the buffer layer. It is the difference in bandgap energies between AlGaN and underneath GaN which leads to band bending and creation of two-dimensional conductive channel (2DEG). This makes the layer most critical in the HEMT structure. The quality of this layer depends on specific mole fraction, composition and thickness of the layer.

2.2.6 Capping layer

Usually a thin GaN layer (1-2 nm) is deposited on top of the barrier layer to prevent the epitaxial surface from oxidation and produce a much smoother surface. It acts as an encapsulation of the high density of surface donor traps on the ungated surface which are essential to the operation of the GaN HEMT device since their positive charge ultimately supplies and matches the negative 2DEG charge. Without the typical $10^{13}\ cm^{-2}$ of ionized surface donors, there would be no free electrons and the device would not conduct [43]. It also aids in reducing the surface leakage and surface trapping. In recent times insitu SiN_x capping layer have been also used with much better surface and leakage performance [44].

2.3 AlGaN/GaN HEMT:

2.3.1 HEMT Device

With the epitaxy growth completed with good quality material and desired wafer bow next step is device fabrication. Typical example of AlGaN/GaN HEMT stack after the fabrication process is shown in Fig.2.12. Three areas, ohmic contact process for source and drain contact, device isolation MESA or implant process and schottky contacts for gate have been discussed here in detail.

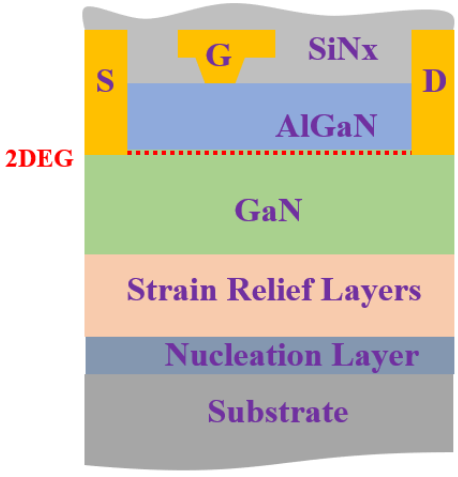

Figure 2.12: Shows typical AlGaN/GaN HEMT device structure.

2.3.2 Ohmic Contacts

To obtain contacts with 2DEG which is at AlGaN (barrier) and GaN Buffer interface, it requires special metallization process to form ohmic contacts. Ideally these contacts need to have the lowest possible contacts resistance (R_c). The lower the R_c, the lower the access resistance to

the 2DEG enabling smaller gate-drain resistance. This adds as an advantage by increasing the intrinsic transconductance (g_m) enabling higher cut off frequency (f_t) and maximum frequency (f_{max}). Lower contact resistance aids in achieving higher Id_{Max} and lower on-resistance, both of these are always desirable.

Process: Conventional FET devices use low work function metals to form ohmic contact; however, in case of GaN its difficult to find low enough work function metal to yield a low enough barrier height. A GaN HEMT device typically have ohmic contacts which consists of a four-metal stack Ti/Al/Ni/Au [99] annealed at high temperature to diffuse in and make contact with 2DEG. Each of these metal plays a specific role enabling lower R_c.

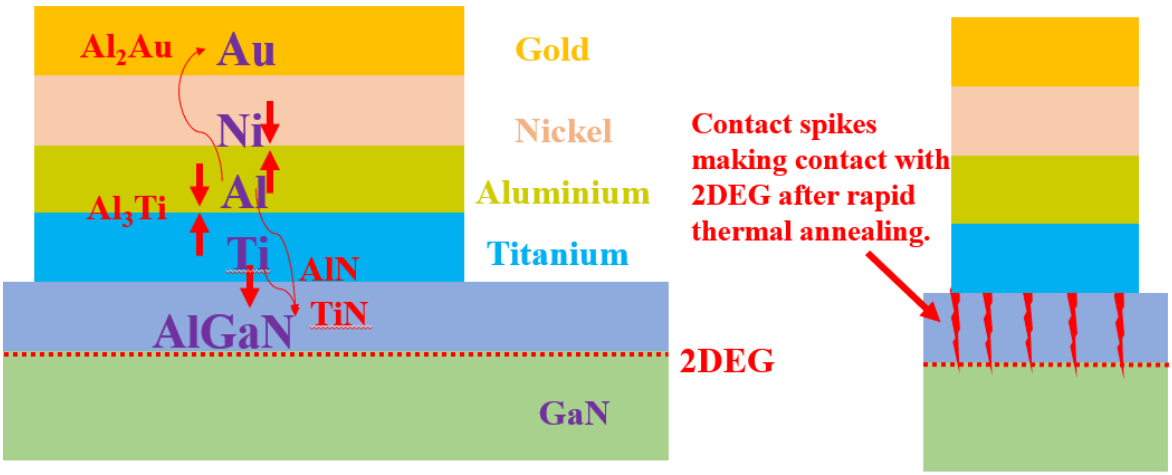

Figure 2.13: Shows stack of four metals used for ohmic contact process with each layer forming different alloys allowing lower contact resistance, after the rapid thermal annealing process the metal diffuse in and make contacts with the 2DEG.

Titanium (Ti): To react with N in AlGaN and GaN layer to form TiN which has a lower work function as shown in Fig.2.13, lowering the SBH and therefore helping in contact formation [45]. There also have been arguments about Ti extracting N out of the GaN. This leaves a high density of N vacancies (donors) near the interface pinning the Fermi level creating tunnel junction across the barrier responsible for an Ohmic contact behaviour [46].

Aluminium (Al): Al in the metallization scheme is known to improve the contact resistance by reacting with Ti and forming Al_3Ti layer to prevent any further oxidation as shown in Fig.2.13. Some reports also suggest the formation of AlN resulting in N vacancies, which yields a heavily doped interface underneath the contact creating a doped region and tunnel junctions. The other reason for Aluminium presence is also to decrease the aggressive Ti-GaN reaction [11] [45].

Nickel (Ni): Nickel is to prevent the in diffusion of top Au and out-diffusion of Aluminium.

Gold (Au): Au is deposited as the final metal layer to exclude oxidation of the contact during high annealing temperature and to improve the Ohmic contacts conductivity [47].

A range of different metal thickness, their mole fraction and rapid thermal annealing temperature is used to obtain lower R_c. Recently there have been reports of the regrown method with highly doped regions have been used and R_c as low as 0.08 Ω.mm has been achieved repeatedly [48]. Transmission line method TLM, discussed in Chapter-3 is used to determine the R_c.

2.3.3 Device isolation

Device isolation is key step in the fabrication of HEMT devices. Due to growth the 2DEG is present across the entire area, it is this areas which is isolated by etching the material until the 2DEG is removed leaving islands of area with 2DEG and no 2DEG areas. The depth of mesa isolation has to be done concerning the position of 2DEG. Presence of 2DEG all over the wafer requires isolation between the contacts and devices. Good etching requires smooth sidewalls, selective etching and low damage. The role of etching is essential since side wall damages can lead to excessive gate leakage current and degradation of the breakdown voltage of the device [49][50].

Process: Common method to achieve this is by using a dry process using ion etch (RIE) and inductively coupled plasma (ICP). Combination of the chlorine-based gas proper mixture and optimum RF power, pressure, flow rate and DC bias allows smooth etch profiles. Several reports have shown excellent etch profiles and lower leakages.

Most of the commercial device manufacturing today uses ion implant process with different ion species (N+, O+, Ar+, Fe+ and Zn+) for AlGaN/GaN HEMTs to obtain device isolation by choosing optimum incident energies and dose concentration [51][52]. This part of HEMT fabrication is mostly optimised and standard now.

2.3.4 Schottky contacts

Schottky contacts are an important part for HEMT devices and correspond to the gate contacts of the device controlling the 2DEG. An ideal Schottky gate contact enables low leakage current, high breakdown, low gate resistance and good thermal stability. Ideal contact is defined by barrier height ϕ_b, ideality factor n, serial resistance R_s and breakdown voltage V_{br}. In metal semiconductor terms barrier height is defined as the energy difference between the semiconductor conduction-band edge at the interface and the Fermi level in the metal. It is an important parameter controlling electron current across the interface and the depletion width and is determined by the difference between the electron affinities for the metal and the semiconductor as shown in Fig.2.14.

For a doped heterostructure electrons need elevated energy to tunnel through the barrier with aid of thermionic emission. However, for an undoped structure it can cross the barrier with help of thermionic emission. For high doped case the depletion region is thin enough for electrons to tunnel through the barrier. All these parameters are extracted from IV characteristic. In forward

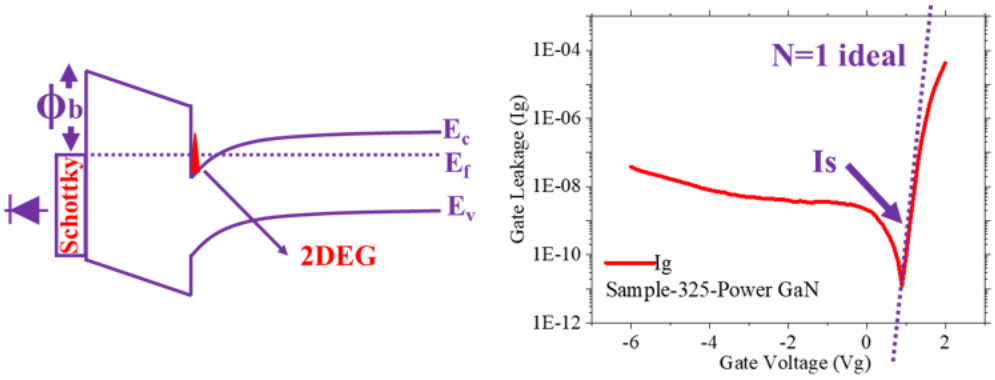

Figure 2.14: Shows band profile of schottky gate contact for AlGaN/GaN HEMT at zero gate bias and gate leakage measured on typical HEMT showing off state leakage of 10^{-7}A.

bias voltage region for applied voltage higher than 3kT/q the current is defined by equation [53]:

$$I = I_s exp \frac{q(V - IR_s)}{nkT}[A] \tag{2.5}$$

Where the saturation current I_s is given by:

$$Is = ART^2 exp \frac{q\phi_b}{kT} \tag{2.6}$$

where A is the device area, R is Richardson constant, the barrier height ϕ_b will be given by the equation 2.7, where I_s is extrapolated from Y-axis intersection in IV curve.

$$\phi_b = \frac{kT}{q} ln \frac{ART^2}{I_s} \tag{2.7}$$

Example of gate schottky leakage current is shown here in Fig.2.14 showing leakage current of the order of 10^{-7}A. Commonly used Schottky metal in case of AlGaN/GaN HEMT is a Ni/Au alloy which will have a barrier height of around 0.5 eV [54]. Ti/Al alternatives exist for an Au-free process which is necessity sometimes in silicon foundries [55] [56].

2.3.5 Passivation

This is shield of the HEMT device protecting it from trapping, moisture, surface contamination and surface leakage. Typically silicon nitride (SiN_x) is used as a passivation layer. It's most important task however, is to suppress any lateral conduction by hopping of electrons between these interface traps which can lead to issues such as current collapse (discussed later in this chapter). Most common passivation layer is Si_3N_4, SiO_2 or sometimes Al_2O_3 and can be formed by three methods:

(a) Plasma enhanced chemical vapour deposition (PECVD) at about 300-400°. This was until recently the normal choice for RF devices but has a high hydrogen content of as much

as 20% which makes it a poor diffusion barrier for moisture [57] and degrades its hot electron reliability. **(b)** Insitu Si_3N_4 can also be grown during the epitaxial growth using MOCVD. It has the advantage of preventing any contamination of the GaN cap/Si_3N_4 interface during processing. This approach has been used by, for instance, ON Semiconductor [58]. **(c)** Low pressure chemical vapour deposition (LPCVD) Si_3N_4 deposited at ~ 800° has a very low hydrogen content and is far denser than PECVD material. As a result it has excellent diffusion barrier properties, is thermally stable, and has much reduced electron trapping [59]. This approach has been used by Nexperia.

2.4 AlGaN/GaN HEMT Operation

In this section, the main parameters of the HEMT device will be explained. Some basic terms, important for the evaluation of HEMT performance will be discussed as well.

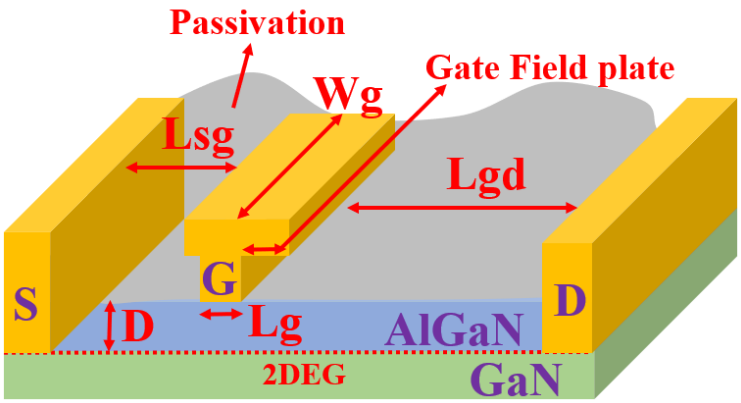

Figure 2.15: Shows schematic of an AlGaN/GaN HEMT device with its various dimensions and parts illustrated.

2.4.1 DC performance

The drain current flowing through the device is directly proportional to the gate width (W_g). Example of output characteristics of a transistor is shown in Fig.2.16(a) showing I_d-V_{ds} measured at V_{gs} varying from -3 V to 1 V. The current flowing between the drain and source or the rate at which the 2DEG charge moves across the gate contacts can be written as:

$$I_D = q n_s v_{eff} W g \tag{2.8}$$

where n_s is the 2DEG charge density, v_{eff} is the effective velocity of the electrons in the channel, and W_g is the gate width [53]. In an ideal transistor, the length of the device is much larger than the thickness of the AlGaN barrier, so the current flows between the ohmics and

it is modulated by the voltage applied at the gate. The modified drain current, I_D then can be represented as a function of n2D(x) and V(x) in the lateral direction.

$$I_D = W_g q n_{2D}(x) \mu \frac{\partial V(x)}{\partial (x)} \tag{2.9}$$

Where, μ is the channel electron mobility, and Wg is the gate width. Integrating from the source side of the gate edge (x =0) to drain side of gate edge (x = L_g), the I_D is obtained as

$$I_D = \frac{\epsilon \mu W g}{(d + \Delta d L g)} \left\{ (V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right\} \tag{2.10}$$

where the drain-to-source voltage is defined as V_{ds}, d is the thickness of the AlGaN Schottky barrier layer, Δd is the effective distance of the 2DEG from the heterointerface, and V_g is the gate bias. Transfer characteristics: Fig2.16 (b) shows example of a transfer curve measured with V_{gs}

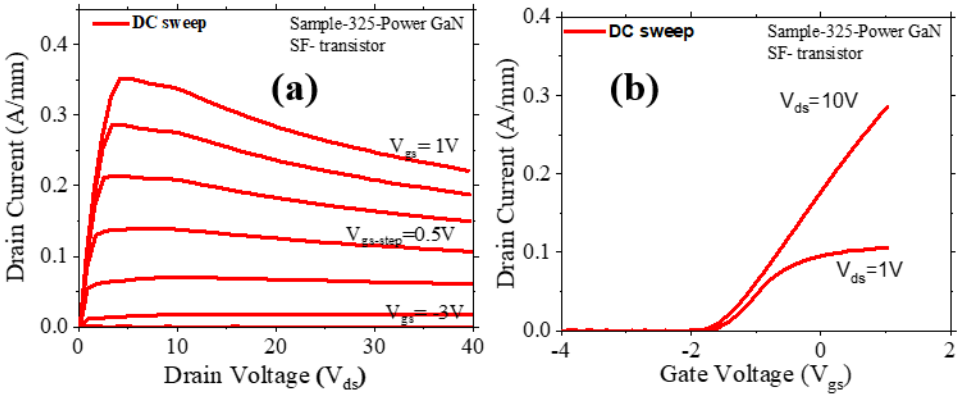

Figure 2.16: Shows DC output characteristics with V_{gs} varying from -3 V to 1 V, (b) shows transfer curve measured by sweeping V_{gs} from -4 V to +1 V at V_{ds}= 1 V and 10 V.

varying from -3 V to +1 V. In case of HEMT, it is the Schottky barrier gate potential which dictates the channel control. The intrinsic gain of the HEMT is defined by measured transconductance, g_m. The g_m is basically the effectiveness of the gate in modulating the drain current and is defined as:

$$g_m = \frac{\delta I_D}{\delta V_{gs}} \tag{2.11}$$

The transconductance (g_m) of the device is one of the important parameter of device evaluation for an RF applications. It is related with gains and high-frequency properties of the device. The transconductance in the saturated regime is given by:

$$g_m = \frac{\epsilon_{AlGaN} V_{sat} W}{d_{AlGaN} + \Delta d} \tag{2.12}$$

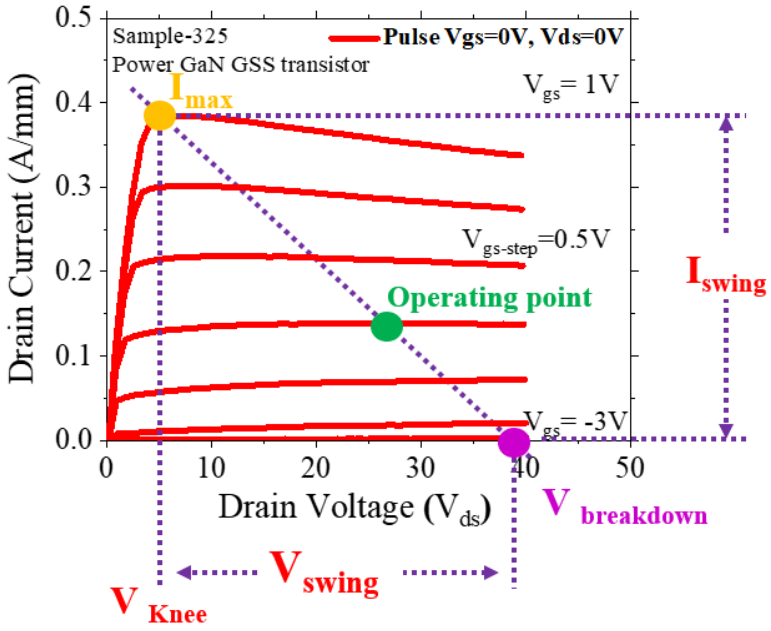

Figure 2.17: Shows DC output characteristics with V_{gs} varying from -3V to 1V, with RF load line indicating important point on the IV plane for RF operation such as V_{knee},$V_{breakdown}$, V_{swing} and I_{swing}.

2.4.2 GaN HEMT for RF switching

The output characteristics depicted in Fig.2.17 show the so-called knee-voltage V_{knee} at the transition from the linear regime (V_{ds} < V_{knee}) of $I_{ds}(V_{ds})$ to the saturation regime (V_{ds} > V_{knee}). During an RF operation, the linear or the knee region is most important since based on the class of operation the device is operated along a dynamic load line. The device connected through load resistor (R_l) is operated at bias range typically around 10-30 V with maximum bias during OFF state being not more than 100V. This means the breakdown voltage ($V_{breakdown}$) requirement for these types of devices need not be very high; however; a stable V_{knee} is a must. For a good amplifier, the aim, therefore, is to maximize the current available from the device and the voltage swing (V_{swing}), the large voltage swing possible without the breakdown) it can sustain to obtain maximum power, as shown in Fig.2.17. Where (I_{max}) is the maximum drain current, ($V_{breakdown}$) is the drain breakdown voltage and (V_{knee}) is the knee voltage as shown in Fig.2.17. This dynamic swing from OFF to the linear region means devices go through different regions on the IV plane as shown Fig.2.18. Bias during OFF state can go up to 100's volts leading into high field region to Semi ON-state of the high field and high current; this makes device vulnerable to trapping in a buffer or in the surface which could lead to dispersion from the original knee.

The maximum voltage swing a device can withstand is defined by V_{knee} - $V_{breakdown}$. A low knee voltage is obtained when the access resistances and the ohmic contact resistances are

minimized and hence the reason why the constant focus has been put on to decreasing the R_c further. The access resistance is lowered by maximizing the $n_s.\mu$ product and has been ongoing research to optimize the epitaxy. The high electron mobility μ while maintaining a high channel charge n_s observed in GaN HEMT becomes an advantage making it a good candidate for power amplifier device compared to most of the wide bandgap (WBG) materials available. The table 2.2 compares list WBG material available for power amplifier application. Combining high mobility and 2DEG density observed in GaN HEMT leads to lower channel resistance resulting in low on-resistance. Saturation velocity of 2.5x10^7 cm/s ensures high current densities which provide higher output and enable higher frequency. 10 times higher critical electric field than silicon will provide higher breakdown allowing large drain bias operation providing higher power density with higher output impedance per unit RF. These reasons combined together explains why GaN HEMT can be most obvious choice for power amplifier applications [60] [31].

2.4.3 GaN HEMT for Power switching

As power switch most important requirement is breakdown strength which for GaN is 10 times higher than silicon meaning the 10 times higher voltage can be applied to GaN device for same dimension silicon device. The specific on resistance of GaN device is twice smaller compared to silicon device with same voltage rating with added advantage of smaller device area [61]. These advantages when compared to other materials in the table above makes GaN the ultimate choice.

For power switching the device is switched from very high OFF state bias typically in the

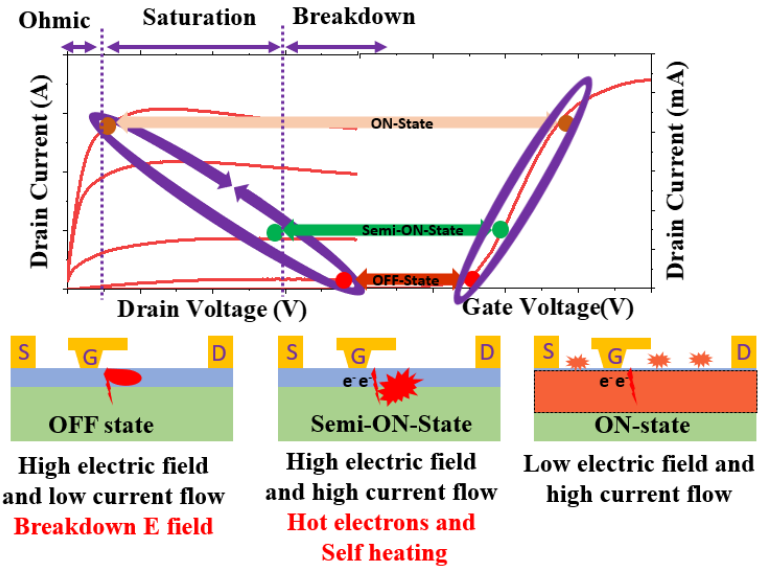

Figure 2.18: Shows different field and current areas during switching in devices from on sate, semi on state to off state, each of these state has different combination of current and field. The schematic below represents the combination of current and field for each state.

Properties	GaN	Silicon	SiC	AlN
Bandgap (eV)	3.42	1.1	3.26	6.1
n_i (cm^3K)	2.0x10^{-13}	1.5 x10^{10}	8.2 x10^{-9}	~ 10^{-31}
ϵ_r	9	11.8	10	8.4
μ_n (cm^2/V.s)	2000	1350	700	1100
V_{sat} (10^7 cm/s)	2.5	1.0	2	1.8
E_{crit} (MV/cm)	3.3	0.3	3	11.7
Θ (W/cm.K)	2.0	1.5	4.5	4.5

Table 2.2: Comparison of physical properties of important semiconductors for switching applications [31].

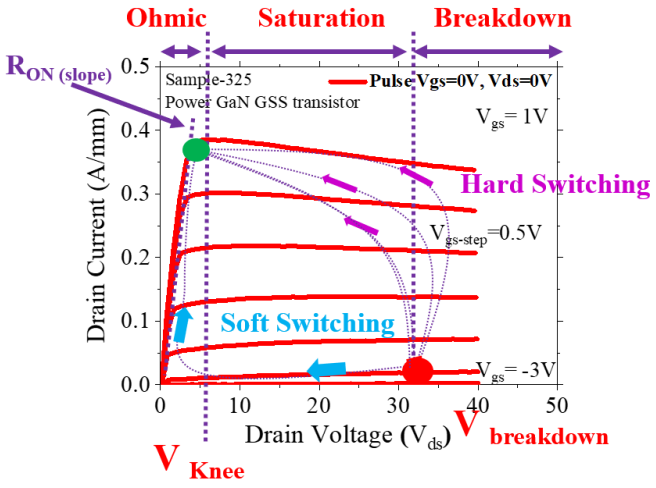

Figure 2.19: Shows ohmic, saturation and breakdown regions over IV plane, hard and soft switching path ways is indicated along with V_{knee} for a typical GaN HEMT IV plot.

range of 100's of V (can be as high as up to 600-1200V, very high field region) to ON state (low field region) as shown in the Fig.2.19. As a figure of merit low ON resistance is desired with fast switching transitions time during the operation. The switching is done in two ways, hard and soft switching [31]. During hard switching device switches from low electric field to high electric field ending up in ON state while in soft switching the path goes through V_{gs}= 0V bias point making it less catastrophic. Based on combination of field and current the region of device switching can be marked as shown in Fig.2.18. The presence of high current and high electrical field during high OFF-state can lead to significant trapping, self-heating and generation of hot electrons especially during hard switching mode. A good HEMT device must show higher breakdown voltage ($V_{breakdown}$), lower leakage, small ON-resistance and fast transitions time with the lower loss. The complexity of making the buffer insulating and presence of inherent defects in the epitaxy makes GaN HEMT more challenging. The reliability issues later in the chapter explains several trapping and buffer challenges for GaN power switch.

2.5 Issues with GaN HEMT

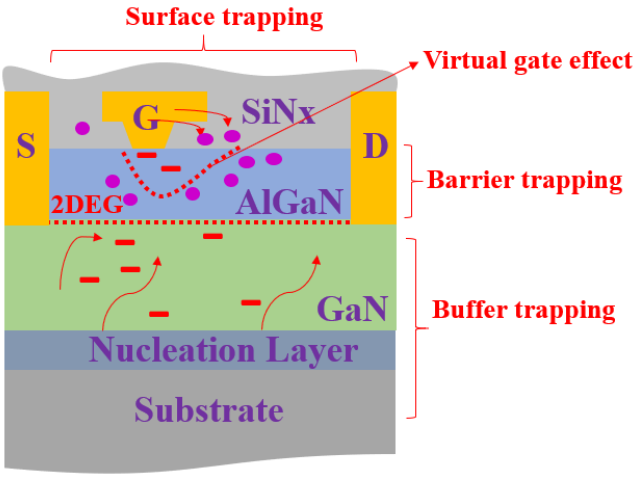

Figure 2.20: Shows different issues surrounding AlGaN/GaN HEMT which could possibly be the area of improvement.

Despite serious development in term of better buffer design, growth optimization, better device fabrication and improved understanding of device design there is still plenty of area of concern for GaN HEMT ranging from buffer trapping, virtual gate effect and surface trapping as shown in Fig.2.20. This section discusses these issues, their impact on performance and possible suggestions for improvement. The key issues in GaN HEMT discussed here are:

2.5.1 Trapping in GaN HEMT

GaN like most of the semiconductors can have defects, a lack of crystal perfection in the material. The electrical behaviour of these defects can be described as trap states located in the bandgap or generation-recombination centres. Shallow defects are called those whose levels lie in close vicinity of band edges (few tens of milli-electron volts (meV) from the respective band edges), while deep defects have electron states lying further from the bands. The reason they are called traps because they are not in dynamic equilibrium with the system of electrons in the conduction and valence bands. These trap states may be empty or occupied by electrons, which has an impact on the charge they carry. Trap states in the upper part of the band gap (closer to the conduction band) are acceptor-like, neutral when empty and negatively charged when occupied. Trap states in the lower part (below the neutral level) of the band gap (closer to the valence band) are donor-like, positively charged when empty and neutral when occupied [53]. The charge state of these deep levels does not respond to the high-frequency signals applied to the device during dynamic switching; hence electrons can get "trapped" in them.

2.5.2 An example of trapping

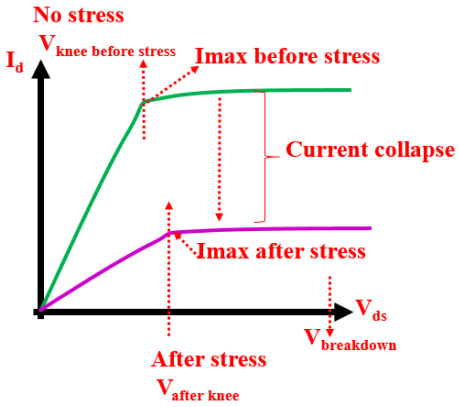

Figure 2.21: Shows impact of trapping on IV, the reduction in V_{knee} and I_{max} after stress shows the role of trapping.

We have understood that GaN HEMT during various switching process goes through a different field of stress and any trap sites during such switching can lead to dispersion. For example, based on DC IV measurements of an RF GaN switch performance the power estimated from the device is extracted using:

$$Power_{max} = \frac{(I_{max} - I_{min}).(V_{max} - V_{beforeknee})}{8} \tag{2.13}$$

During dynamic switching, the device is subjected to a combination of high field and current regions making it vulnerable to trapping. These traps can affect the V_{knee} of the device by creating a potential barrier that obstructs the flow of channel current. Trapping of these electrons means depleted 2DEG density at the channel. This will cause a dynamic shift in threshold voltage of the device (meaning decrease in V_{knee}, saturation current) or increase in ON-Resistance. This change in V_{knee} will significantly change the obtained power during RF operation, and the obtained power will be expressed as:

$$Power_{max} = \frac{(I_{max} - I_{min}).(V_{max} - V_{afterknee})}{8} \tag{2.14}$$

This difference in DC and RF power estimation is called DC-RF dispersion or knee walkout or the current collapse (CC). The trap location causing DC-to-RF dispersion can be on the surface, gate-drain access region, in the vicinity of the gate or the semi-insulating GaN buffer underneath the channel. The origin of traps can be a consequence of several factors, e.g. defects, dislocations, the presence of impurities, fabrication challenges or the device geometry [31].

2.5.3 Surface Trapping

Surface traps can be classified as electron traps or hole traps depending on whether the trap state achieves equilibrium with the system of electrons in the conduction band or valence band.

The most common impact of surface traps is current collapse or knee walkout as discussed before. It is the result of electron capture and emission from surface donor traps, with the electrons flowing across the surface from the gate corner as shown in Fig.2.22.

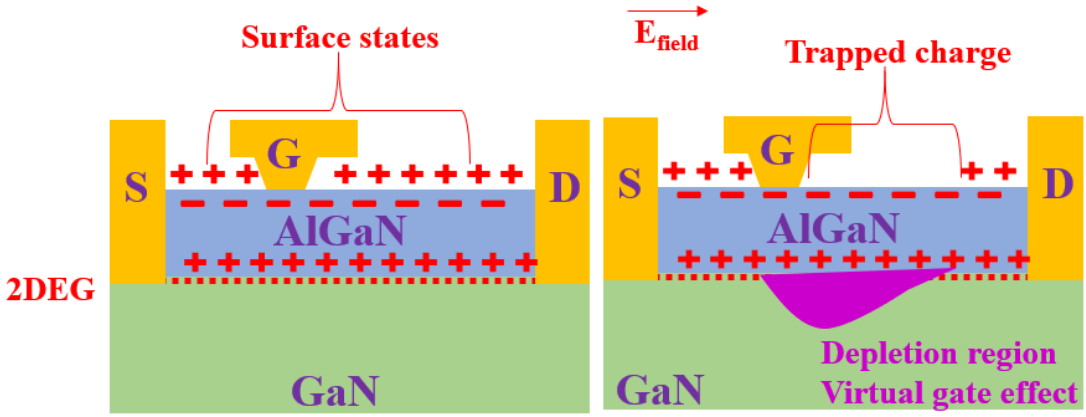

Figure 2.22: Shows schematic for surface states and upon electric field impact the trapping leading to creation of depletion region ending up as virtual gate effect.

Fig.2.22 shows a schematic representation of the hopping process that occurs as electrons flow from the gate corner across the surface to reside in the surface donors due to the high electric field located at the drain edge of the gate. This hopping process is highly non-linear in the electric field, occurring by a Poole-Frenkel mechanism, so the charge will only flow a short distance from the gate corner where the electric field is highest. On the removal of the field when the device is returned to the linear region, the built-in field induced by the trapped charge itself will slowly return most of the charge to the gate. This surface charged region near the gate corner is referred to as a "virtual gate" [62].

The impact of this charge is shown in the pulse IV plots of Fig.2.23. Here the black lines are pulsed from an unbiased steady state condition of V_{gs}=0 V, V_{ds}=0 V condition, so there is no virtual gate charge, and the red dashed lines are pulsed from the gate off state bias representing gate stress with V_{gs}= -6 V, V_{ds}= 0 V and the green line are drain biased off-state with V_{gs}= -6 V, V_{ds}= 40 V where a virtual gate will have formed. In most cases, pulse IV is used to characterize these traps by choosing specific biasing conditions. The pulse length in all these measurements are 200ns with 1ms pulse length, this is to avoid any self heating effects.

For surface CC a dramatic fall in the current handling in the device knee region with off state stress as seen in Fig.2.23. The mechanism for the severe impact on the knee region is related to the virtual gate locally reducing the carrier concentration in the 2DEG under the virtual gate as seen in Fig.2.22, which reduces its current carrying capacity. The presence of this depletion region leads to the formation of two gate bias controls, the actual gate bias applied and the virtual gate control (controlled surface state traps). Further details can be found in [63]. Surface current collapse strongly reduces output power and degrades efficiency for an RF device. This effect

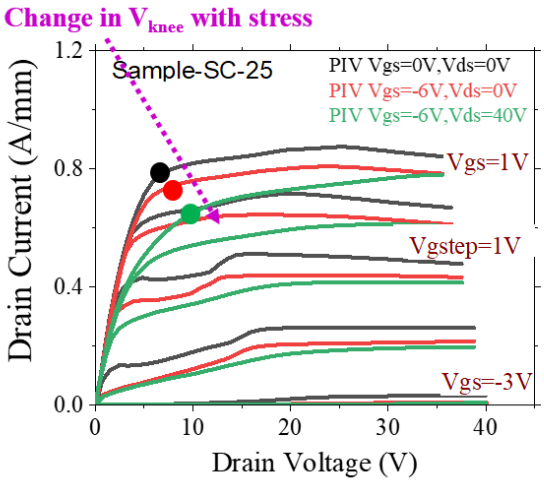

Figure 2.23: Shows impact of different OFF-state stress conditions on the knee walkout, steady state V_{gs}=0 V, V_{ds}=0 V shown in black, gate stress V_{gs}= -6 V, V_{ds}= 0 V shown in red and gate-drain stress V_{gs}= -6 V, V_{ds}= 40 V shown in green. The locus of knee for each plot is marked with dot showing the change in V_{knee} with increase in OFF-state stress.

also occurs for power switching. Therefore, this effect is equally undesirable for both types of switching operations. It is important to note that surface donors are essential in all GaN devices, so suppression of current surface collapse must concentrate on suppressing the lateral conduction of electrons from the gate to the traps, and not on the suppression of the traps. Since this lateral conduction process is strongly field accelerated, the primary control is achieved by limiting the electric field at the gate corner. This field control is undertaken in all devices by a combination of sloped gate corner, field plates and good passivation. With good device design and manufacture, surface current-collapse is no longer a serious issue in current devices [63].

2.5.4 Buffer trapping

Buffer trapping in RF device: In order to suppress punch through and short channel effects, GaN on SiC RF uses Iron (Fe) as dopant. The key parameter that controls the short-channel effects is the density of deep acceptor states in the GaN. The depletion region under the gate during high negative OFF state is strongly affected by the intrinsic or extrinsic acceptor density. Therefore adding high negative acceptor charge density in the depletion region confines the electrons at the surface. By adding an extrinsic acceptor such as Fe helps in keeping the electrons confined at the surface and resulting in good pinch off behaviour. However, current collapse has still been observed in most of Fe doped buffers specially under high drain bias during OFF state and has been assigned to the same acceptors. The Fe doped buffer being weakly n-type supports geometrically determined negative space charge under the gate which screens the field associated with large drain biases and the transient behaviour of these charge leads to CC. Uren

et al. also predicted that the presence of Carbon (always present during the growth) during Fe doping can pin the Fermi level into the lower half making the buffer p-type [19]. This forms an P-N junction between the 2DEG and the buffer making the buffer to float and act as a reservoir for time-dependent charge storage. This not only makes the CC worse but also brings in issues such as kink which has been explained in detail in this thesis.

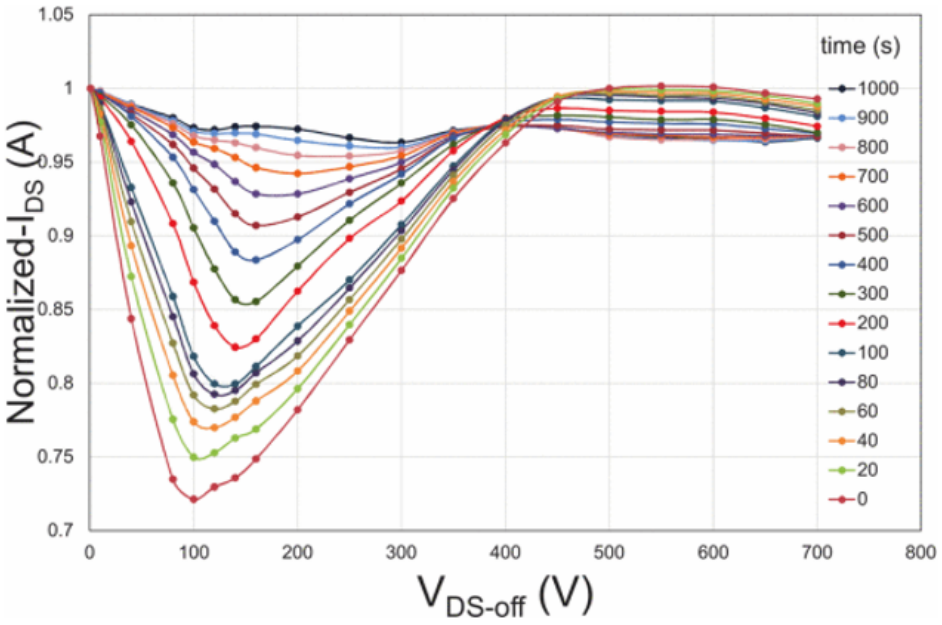

Figure 2.24: Shows example of bulk dynamic RON in a GaN MISHEMT following 1000s bias stress at room temperature.The curves show measurements of R_{ON} at times between 20 and 100s following switching to the on-state [64].

Buffer trapping in Power device: Compared to surface current-collapse, buffer related current-collapse or dynamic R_{ON} is a very serious problem for GaN power devices. Buffer is the most important part of the HEMT structure making important contribution not only in defect-free growth process but also in saturation velocity and charge carrier mobility. Fig.2.24 shows an example of dynamic R_{ON} in an ON Semiconductor MISHEMT device, illustrating the complex behaviour that can be observed [64]. Many technologies from different sources display a worst case for dynamic R_{ON} at a voltage well below the maximum operating voltage, and in this case, a 30% increase in R_{ON} was observed at 100 V which improves later showing almost no dynamic R_{ON} at its maximum specified voltage of 650 V. Here the timescale for recovery after switching to the on-state is in the order of 1000s [64]. The timescale for trapping in the off-state is also typically in the same range [65]. Early power devices on carbon doped epitaxy showed R_{ON} increasing linearly following off-state stress, and in the absence of a full understanding of the mechanism responsible for the wafer to wafer, variation progress was slow in developing a route to suppression [66].

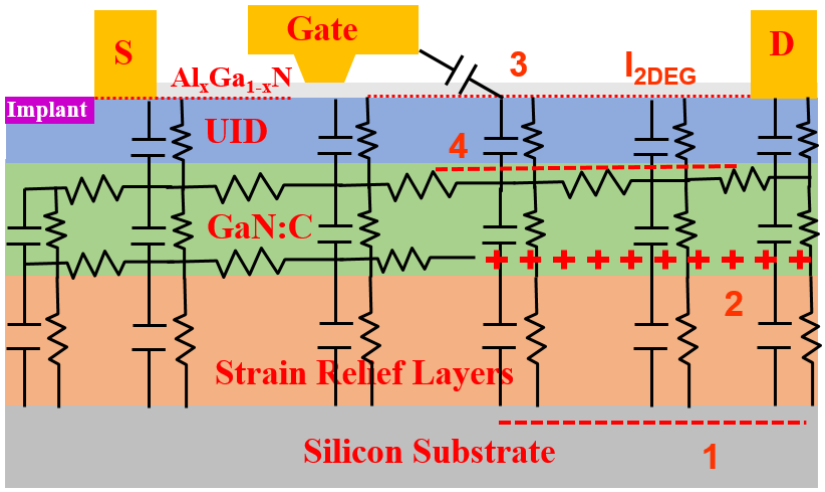

Figure 2.25: Shows equivalent circuit representation of the power transistor showing the leakage resistance and capacitive components. The location of charged regions resulting from applied drain bias are indicated with numbers 1-4 [67].

Uren *et al.* developed a model to explain the variability of the dynamic R_{ON} based on the energy level of the carbon deep level trap and the impact of threading dislocations [19], [68] [67]. Earlier in this chapter it was shown that Fe with an energy of 0.72 eV below the conduction band making it an n-type buffer. Carbon on other hand on the nitrogen site (C_N) makes the buffer p-type. With an absence of any external field makes the buffer dominated by carbon making it behave as p-type. This makes the highly resistive GaN buffer isolated from the 2DEG by forming a P-N junction making buffer float and act as a reservoir for time-dependent charge storage. Using these buffer understandings an equivalent circuit representation of a typical GaN power FET buffer is shown in Fig.2.25. The main layers forming the buffer are an undoped GaN layer, a carbon doped GaN layer and a highly resistive blocking strain relief layer containing AlGaN. The carbon doped GaN is very weakly p-type and the majority carriers are holes. However, the density of free holes is extremely low so that its resistivity even for heavy doping is found to be as high as 10^{14} Ω.cm. The p-type carbon doped GaN layer is isolated from the 2DEG by a reverse biased P-N junction, meaning that the layer can float and holes can flow laterally within this layer, which because of its high resistivity, occurs on a timescale of hundreds of seconds. The GaN:C layer act as a back gate to control and modify the conductivity of the 2DEG and variations in its potential can result in severe dynamic R_{ON}. The reason why this problem of a floating GaN:C layer does not occur in all devices is that the P-N junction between the 2DEG and the GaN:C layer is actually slightly leaky along defects such as screw dislocations, allowing the potential of the GaN:C to follow that of the 2DEG and preventing back-gating. When a high drain bias is applied, slow leakage within the epitaxial layers will result in positive and negative charged regions in the locations shown in the Fig.2.25 and which can be used to explain the maximum in dynamic R_{ON} as shown in Fig.2.24 [52]. This model has successfully explained many of the

observations including the timescale for the behaviour, the maximum in dynamic R_{ON} at 100 V, and the huge variability seen between epitaxies. This model has important and unexpected consequences. It is essential to have vertical leakage in these devices to suppress the dynamic R_{ON}. Suppression of dynamic R_{ON} is always a trade-off with leakage. It has been demonstrated now by several manufacturers that this balance can be achieved; however it is certainly not straightforward. The trap density is not important in determining dynamic R_{ON}. This is because there are always more than enough traps to store the charge, and it is the leakage path to the traps that determine the dynamics of the process.

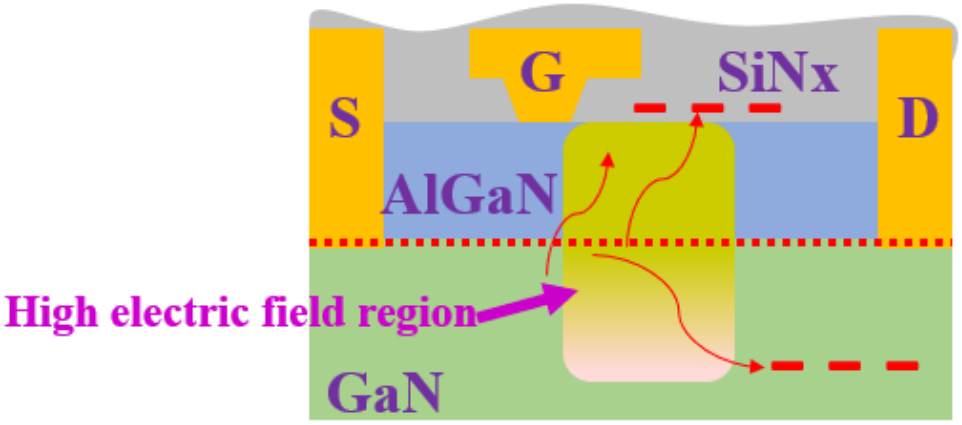

Figure 2.26: Shows cross section of AlGaN/GaN HEMT with high field region being created under certain biasing condition. With high fields, the electrons can gain higher energy, this may lead to overcoming the barrier getting trapped on the surface or the barrier.

2.5.5 Breakdown issues in GaN HEMT

The main attraction for GaN HEMTs has been high power devices which often requires capabilities to sustain high electric fields especially under OFF state during the operation and minimizing on state voltage drop to obtain minimum power dissipation. High electric fields can induce electronic trapping and increase their impact on output characteristics, which may lead to the breakdown of the device eventually. Particularly OFF state stressing, i.e. the prolonged high voltage operation in a pinch off has been seen to be detrimental to devices. These high field regions as shown in Fig.2.26 are often observed at the gate edges and within the interior of the device structure and lead to several pathways to breakdown limiting high voltage capability in GaN HEMT [69]. Few major ones are discussed below:

Breakdown due to leakage through the gate, barrier layer: Zanoni *et al.* in a review mentioned several modifications required to obtain improvements in breakdown qualities [70]. Leakage through the barrier and passivation layer were investigated using step stress mea-

surement technique along with a combination of electroluminescence. They suggested use of an unstrained GaN cap layer or in-situ SiN_x passivation layer which can delay surface degradation. In recent times better passivation techniques and barrier qualities have significantly improved the gate leakage issues in the devices [71].

Breakdown through buffer layer in Power devices: Most power devices are made on conducting substrates. In the scenario of high voltage operation, the electric field across the channel area and the buffer increases significantly, and with the occurrence of high vertical leakage, the conduction through the buffer or even the substrate (conductive silicon/n-type SiC) can take place. The other parameter for achieving high breakdown is gate-drain L_{GD} scaling which can define the breakdown condition. However, under high field conditions, the drain current can rise rapidly mainly due to electron flow from the gate terminal possibly assisted by the electron's injection across the Schottky barrier under high field stress.

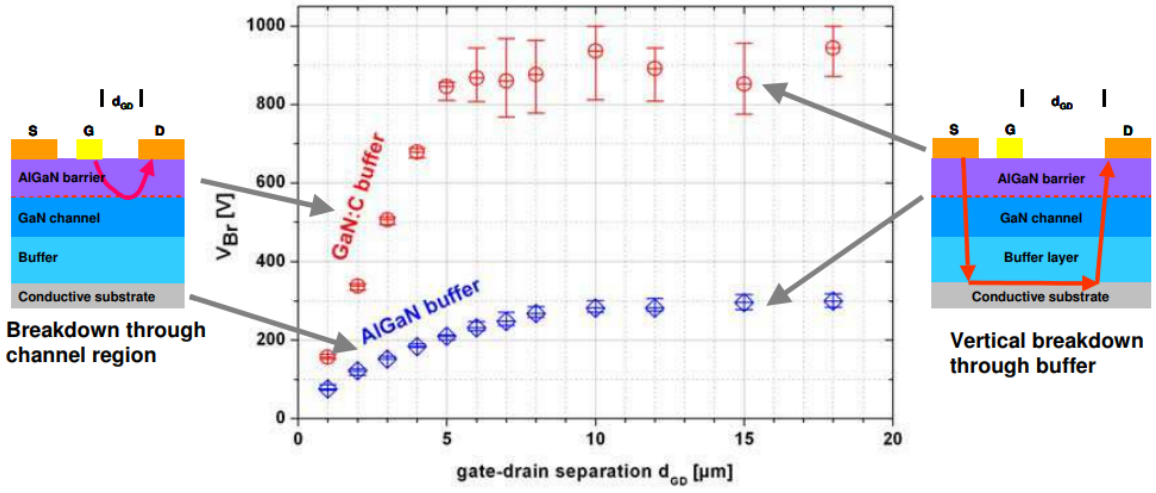

Figure 2.27: Shows breakdown dependence on gate-drain distance for two different buffer designs, for one the path is through channel while for second it goes through buffer all the way back to drain [72].

Wuerfl *et al.* using detailed DC measurements showed that the gate current is no longer synchronous to the drain current at breakdown condition; instead the drain current increases at breakdown condition without significantly influencing the gate current [72]. For the saturated regions, this means that the breakdown current is now bypassing the gate control region. Detailed investigations have shown that breakdown is now characterized by a current flow originating for instance from the source contacts of the devices down to the substrate and back to the drain terminal as indicated in the Fig.2.27. They also showed using a range of gate to drain distance (D_{GD}), the critical field for breakdown can be shifted to higher drain voltage as seen in the Fig.2.27. Figure shows an example of the median value of device breakdown in dependence on gate-to-drain distance (D_{GD}) for different buffer designs. The insets on the left and right side are highlighting the proposed breakdown mechanisms in the respective regions of the IV-

characteristic. However, there are some cases, the drain current splits into the source and gate current and has been studied in detail in chapter-6 in this thesis. Since most of the field crowding takes place near the gate edge use of adequate field plate design can significantly improve the breakdown conditions.

Breakdown induced by punch-through effect in RF devices: Uren *et al.* demonstrated that AlGaN/GaN single heterojunction HFETs are vulnerable to short-channel effects [39]. Using a two-dimensional finite-element simulation, they suggested to eliminate punch-through, the GaN buffer layer in short-channel devices must be designed not only to insulate the device, but also to confine carriers in the channel. They recommended the use of a sufficiently high density of deep acceptors to be incorporated into the GaN buffer.

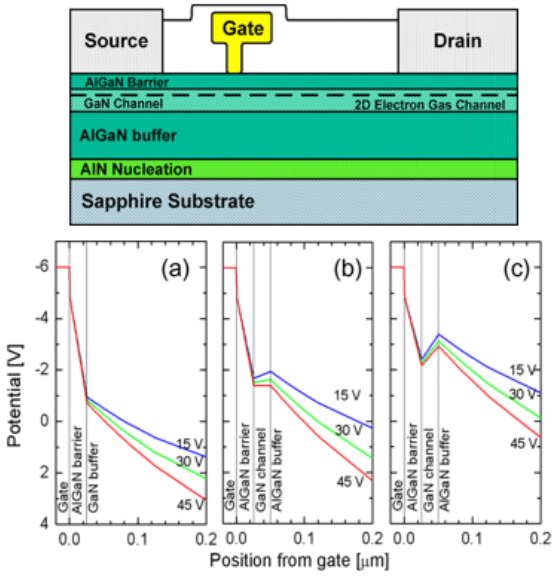

Figure 2.28: Shows planar gate HEMT structure with linearly graded AlGaN layer, the bottom is simulation potential profile for three different Cross section (a) GaN buffer layer, (b) $Al_{0.05}$ $Ga_{0.95}$N buffer and (c) $Al_{0.1}$ $Ga_{0.9}$N buffer layer, for all three case bias is V_g= -6 V and V_d = 15, 30 and 45 V [40].

Later Bahat-Treidel *et al.* demonstrated the use of a wide band-gap buffer layer replacing the traditional GaN buffer layer [40]. The introduction of a linearly graded AlGaN buffer layer as shown in Fig.2.28 leads to better confinement of the electrons in the GaN channel, accompanied by a reduction in I_{ds} max and an increase of V_t. Using low maximum Al concentrations (5%) in the buffer layer, DH HEMTs could prevent the buffer-layer punch through and reduce the sub threshold drain leakage current, thus significantly increase the device $V_{breakdown}$.

2.6 Gallium oxide (Ga_2O_3)

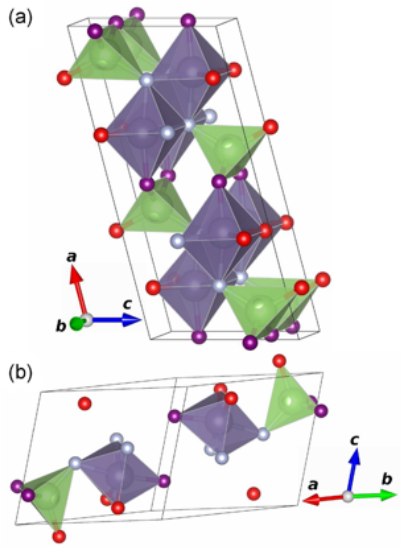

Figure 2.29: Shows the atomic unit cell of β-Ga_2O_3. The two inequivalent Ga (large spheres) and the three inequivalent O (smaller spheres) sites are indicated with a different color. (b) The primitive unit cell, using the same coloring scheme [73].

So far in chapter GaN and its issues have been discussed, this chapter explores new wide bandgap material called Gallium oxide (Ga_2O_3) which could be an alternative choice for future RF device, Fig.2.29 shows atomic unit cell of β-Ga_2O_3 [73]. A comprehensive review of material growth and device development has been presented along with a study on exploring its capabilities as an RF device. Later in the thesis β-Ga_2O_3 MOSFET detailed electrical study is presented showing good pulse performance with minimal trapping which makes these results encouraging given this is a relatively new technology with process and material still evolving, however, the DC and RF performance has been found to be severely limited due to poor thermal conductivity.

2.6.1 Introduction

Great emphasis has been put towards reducing energy consumption for better health and economic interests which has led to rapid advancements in power electronics. It is believed that over 25% of the worldwide annual energy consumption can be saved if widespread adoption of highly efficient power electronics technologies can be realised [74]. Dominant silicon based commercial power electronics devices such as IGBTs, thyristors, MOSFETs are approaching theoretical limits due to fundamental material properties. Wide bandgap (WBG) devices excel at delivering higher achievable junction temperatures and thinner drift regions (because of the associated higher critical electric field values) which can result in much lower on-resistance than is possible in Silicon [75]. The relative electric field permittivity (ϵ_r) has an important influence

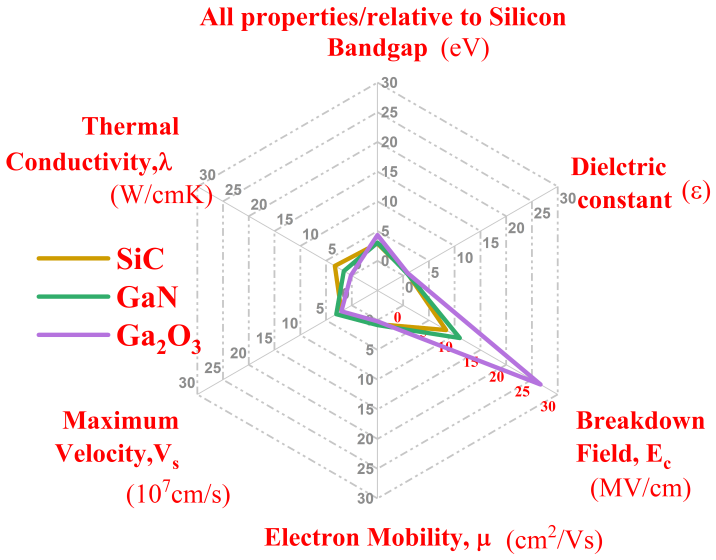

Figure 2.30: Shows spider chart for comparison of β-Ga_2O_3 with GaN and SiC based on several parameters with relative to silicon.

on the value of interelectrode capacitances. Low capacitance implies higher switching speeds and low switching losses which aid severely in RF performance [74]. Due to larger bandgap and high E_{crit} (maximum electric field that the material can support before the avalanche breakdown) Silicon Carbide (SiC) and Gallium Nitride (GaN) have been two primary front-runners for WBG devices. The ability to grow large area epitaxy have allowed them to be commercially viable. However, the poor thermal conductivity and the difficulty in making them semi-insulating due to issues such as growth and doping has kept the doors open for other materials.

In recent time lot of new ultra-wide bandgap (UWBG) materials such as Aluminium Nitride (AlN), Boron Nitride (BN) and Gallium Oxide (Ga_2O_3) have merged Fig.2.32(a). Ga_2O_3 with largest bandgap (4.9eV) among transparent conductive substrate and with good controllability of N-type conductivity over a wide range through Si or Sn doping and tuneable resistivity in the extremely wide range of 10^{-3}-10^{12} Ω cm has gained a lot of attraction [76][77]. Ga_2O_3 single crystals exhibit five polymorphs denoted by α, β, γ, δ, and ϵ. Monoclinic β-Ga_2 O_3 is the thermodynamically stable form with lattice constants of a = 12.2 Å, b = 3.0 Å, and c = 5.8 Å (shown in Fig.2.29). The β-polytype with the monoclinic β-gallia structure is the most stable and the only crystal structure available for Ga_2O_3 melt growth, whereas the other phases are metastable [78]. A comparison of Ga_2O_3 with SiC and GaN on based on several parameters is shown in Fig. 2.31.

In order to make good power device, low ON resistance is key parameters and one of the standard figure of merit (FOM) for power device evaluation is Baliga's figure of merit (BFOM),

	Silicon	GaN	SiC	Diamond	β-Ga_2O_3
E_c (eV)	1.1	3.4	3.3	5.5	4.9
μ ($cm^2/V.s$)	1400	1200	1000	2000	300
ϵ_{REL}	11.8	9	9.7	5.5	10
V_{SAT} (10^7cm/s)	1.0	2.5	2.0	1.0	1.1
λ (W/m.k)	150	130	370	2000	10,30
BFOM($\mu\epsilon {E_c}^3$)	1	870	340	24661	3444

Table 2.3: Comparison of power semiconductor materials and associated unipolar FET figures of merit [79].

which is defined as:

$$BFOM = \epsilon \mu E_c^3 \tag{2.15}$$

where ϵ is the dielectric constant, μ the carrier mobility, and E_c the critical electric field at the onset of breakdown. BFOM defines the material parameters to minimize conduction losses, β-Ga_2O_3 is calculated to be at least four times larger than those of 4H-SiC and GaN. Fig.2.32(b) shows the theoretical limits of on-resistances as a function of the breakdown voltage for the semiconductors, as calculated from the parameters in Table 2.3 [80][81]. These estimates indicate the great potential of Ga_2O_3 for high-power and high-voltage device applications.

Similarly Johnson figure of merit (JFOM) which define a good RF device is given by [82]:

$$JFOM = \frac{1}{2\pi}(2\pi L_G f_T)\frac{2V_{BD}}{\alpha L_G} = \frac{2}{\alpha} f_t V_{BD} \tag{2.16}$$

where L_G is the gate length, V_{sat} is the saturation velocity and E_{BD} is the electric field,ft is the cutoff frequency, where α is an adjustable parameter that relates the voltage drop across the gate to the total voltage applied to the device and can be calcualted by:

$$V_{BD} = \alpha \frac{E_{BD} L_G}{2} \tag{2.17}$$

The effective mass of electrons in β-Ga_2O_3 is 0.28 m0 and LO phonon energy (~ 44 meV) is low however if bulk electron saturation velocity v_{sat} ~ 1.5x10^7 cm/s is assumed than it can outperform GaN in terms of RF operation[83]. The Baliga and Johnson FOM good numbers for β-Ga_2O_3 makes it promising material for future power and RF applications. A comparison of Ga_2O_3 with SiC and GaN on basis of different figure of merit is shown in Fig. 2.30.

2.6.2 Growth

2.6.2.1 Bulk crystals

Important conditions for high-quality epitaxial growth is the absence of impurities and structural impurities like dislocations, point defects, stacking faults and has often lead to growth on native

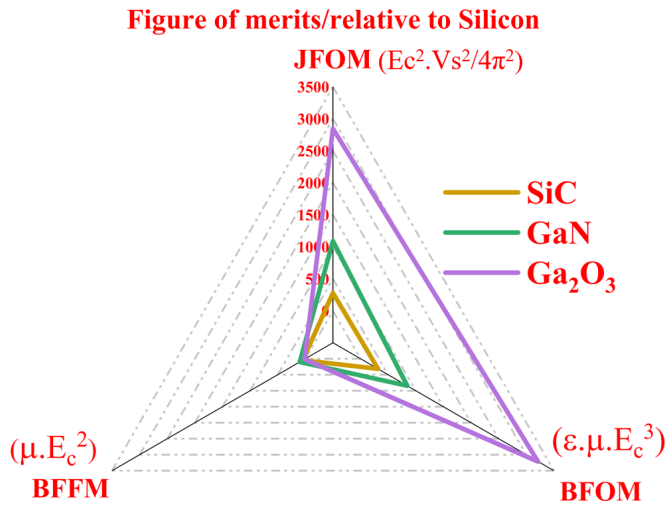

Figure 2.31: Shows comparison of different Figure of Merits for β-Ga_2O_3 relative to Silicon.

substrates. Efforts were put in for large size single crystal Ga_2O_3 bulk wafers. Initial efforts were made by float zone (FZ) but an inability to grow larger crystal than 25mm diameter was limiting factor [78]. Tomm *et al.* [85] were first to demonstrate Ga_2O_3 crystals using the Czochralski (CZ) method; however; it was Galazka *et al.* [80] who demonstrated 2 inch Diameter β-Ga_2O_3 good quality single crystals with rocking curve FWHM on the (100) plane was about 100" for a 20-22 mm diameter crystal. For a 2-inch crystal they could measure much lower values such as 46" on the as-cleaved (100), however, melt thermodynamics requiring higher oxygen concentration

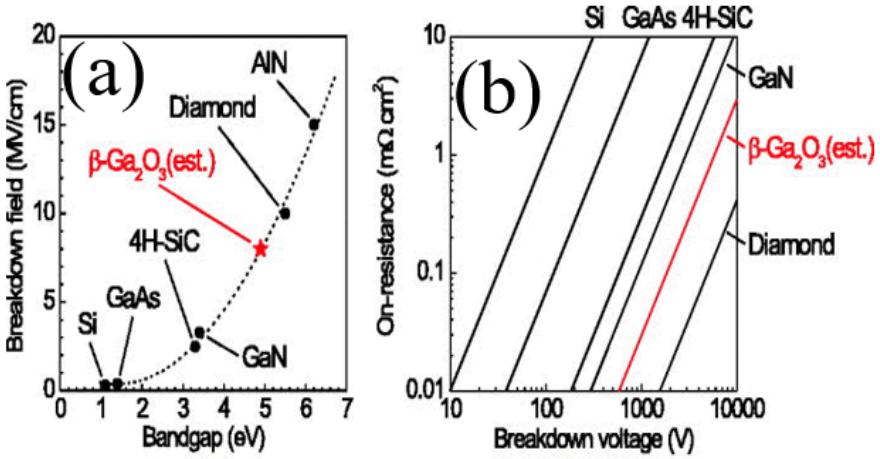

Figure 2.32: (a) Shows bandgap dependence of the breakdown field and (b) theoretical limits of on-resistances as a function of breakdown voltage for major semiconductors and β-Ga_2O_3 [84].

motivated others for exploring different growth methods. Edge-defined film fed growth (EFG) a well-established melt grown method used for sapphire wafers was brought into use [86]. Kuramata *et al.* [82] reported the growth of large and high quality β-Ga_2O_3 single crystals by the EFG process. Residual impurities, doping controllability, and crystal defects were investigated, and the results show that β-Ga_2O_3 single crystals can be fabricated with sufficient quality for semiconductor device applications. They could also show the effect of thermal annealing on the electrical properties and clarified the method of stabilising the donor concentration. The first-time size up to 4 inches in diameter was fabricated and now based on ease of growing large area bulk substrates up to 6 inches are easily available and sold by Tamura Corporation (as shown in Fig. 2.33).

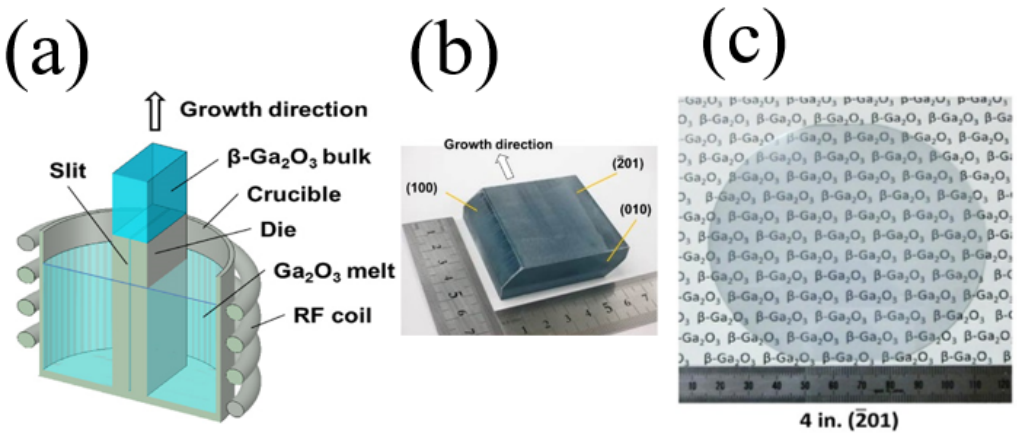

Figure 2.33: (a) Shows schematic drawing of the EFG process, (b) the Ga_2O_3 melt moves up to the top of the die through the slit by capillary action. (b) shows β-Ga_2O_3 bulk crystal, which has been cut perpendicular to the [010] direction and shaped into a flat hexagonal prism. (c) shows substrates with 4 inch in diameter with a surface orientation of (201) [87].

2.6.2.2 Epitaxial growth

Molecular beam epitaxy (MBE): Availability of bulk crystals opened up the epitaxial thin film growth research with successful demonstration of thin films grown by various systems like molecular beam epitaxy (MBE) [89], halide vapour phase epitaxy (HVPE) [90][91], metal organic chemical vapor deposition (MOCVD) [91][92] and mist chemical vapor deposition (Mist-CVD) [93][94]. Out of most of these MBE has been most used growth method so far for Ga_2O_3 films. Several initial reports of Ga_2O_3 using RF-plasma assisted MBE can be found, and these films had atomically flat surfaces because of the step-flow growth mode. Higashiwaki *et al.* [80] demonstrated molecular-beam epitaxy(MBE) grown Sn-doped n-type Ga_2O_3 layer with a thickness of 300 nm on an Mg-doped semi-insulating-Ga_2O_3(010) substrate fabricated by the

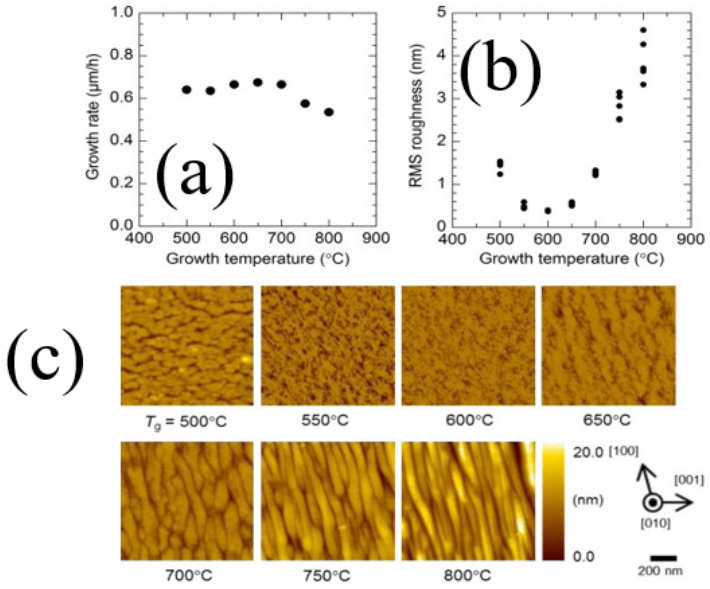

Figure 2.34: schematic growth rates of Ga_2O_3 epitaxial films as a function of Tg showing a decrease in growth rate beyond 700°C. Surface RMS roughnesses of Ga_2O_3 epitaxial films as a function of Tg, the sample grown at 500°C had a rough surface covered with small grains resulting from three-dimensional growth. In contrast, the samples were grown at Tg= 550-650°C had a smooth surface. Multi-atomic steps along the [100] direction that was due to step bunching growth were observed in the samples grown at Tg>700°C, and the trend became worse with increasing Tg [88].

floating zone (FZ) method which was relatively easy method to start with, but it also meant that typical crystals are limited to roughly 10 mm in diameter by 50 mm in length. Ga and Sn fluxes were supplied by evaporation of Ga metal and SnO_2 powder heated in normal Knudsen cells. A gas mixture of ozone and oxygen was used as the oxygen source. The substrate temperature was 700°C, and the growth rate of Ga_2O_3 was 0.6 μl/h. However, there was a major problem with the MBE growth on the (100) plane in that the growth rate was only a few tens of nanometers per hour and doping was difficult. Sn the most common dopant is usually employed as a donor dopant in MBE growth of n-Ga_2O_3 thin films; however, Sn atoms tend to segregate on the growing surface without being incorporated into the epitaxial film. Sasaki *et al.* [88] in their work investigated the relation between the growth rate and the Ga_2O_3 substrate orientation and succeeded in increasing the growth rate to several micrometres per hour by changing the orientation from (100) to (010). Furthermore, the use of Ga_2O_3 (010) substrates enabled them to precisely control the N-type conductivity of the MBE-grown Ga_2O_3 films by using the correct temperature for Sn doping. They obtained an atomically smooth and flat surface for the samples grown in the range of Tg= 550-650°C (as shown in Fig.2.34). Although they had a doping delay in

the initial stage of growth in the sample grown at Tg= 600°C , they optimised it later reducing the temperature to 570°C . They could demonstrate high-crystal quality Ga_2O_3 epitaxial films with a smooth surface and uniform doping profile over a narrow temperature range of 550-570°C. This optimised MBE growth temperature of Sn-doped β-Ga_2O_3 homoepitaxial films enabled them to have better control their structural and electrical properties.

Later Kaun *et al.* [95] demonstrated successful coherent growth of β-$(AlGa_2)/O_3/Ga_2O_3$ heterostructures using RF-plasma MBE. Cross-sectional transmission electron microscopy of an $(Al_{0.15}\ Ga_{0.85})O_3/Ga_2O_3$ superlattice revealed abrupt layer interfaces and high alloy homogeneity. These results indicate a large possibility of band engineering in Ga_2O_3-based material system which could lead to high-performance electrical devices based on the heterostructures.

MOCVD: The other possible method of MOCVD has also been used for growth of $Ga_2\ O_3$ thin films with several reports claiming good quality films [91][96] however, stacking faults were often observed as the main crystallographic defects. Poor control of electrical conductivity due to the low activation efficiency of donor dopants and limited N-type Sn doping concentrations on the order of $\sim 10^{18}\ cm^{-3}$ or more has raised some concerns from the power device community. Possible reasons for these issues include compensation by Ga vacancies and Sn incorporation at electrically inactive sites [78]. The exact mechanism is still unclear, and presently there is a lot of ongoing research activity.

2.6.3 Challenges

2.6.3.1 Doping

The n-type conductivity is commonly attributed to oxygen vacancies which are ionised and form donors. The conductivity of the Ga_2O_3 crystals grown by the float zone method can be controlled by changing the gas ambient or by doping. The conductivity of Ga_2O_3 crystals could be controlled from 10^{-9} to $38\Omega^{-1}\ cm^{-1}$ by changing the oxygen content in the growth atmosphere. Because of the strong correlation between the conductivity of Ga_2O_3 crystals and oxygen partial pressure in growth or annealing environments, n-type conductivity was commonly attributed to the presence of oxygen vacancies. However, this assumption has been questioned by Varley *et al.* [97] who performed first-principle calculations based on the hybrid functional theory of various impurities and oxygen vacancies in Ga_2O_3. According to these calculations, oxygen vacancy acts as a deep donor with ionisation energy of more than 1 eV and thus cannot contribute to N-type conductivity. Doping with other elements also affects the electrical conductivity and free electron concentration of Ga_2O_3 crystals. For example, group IV elements such as Si, Ge and Sn substituting on the Ga site or group VII elements such as Cl and F substituting on the Oxygen site act as shallow donors. Sn and Si have remained most preferred dopant however there have been few reports with Fe and Mg as other dopants.

2.6.3.2 Thermal Properties

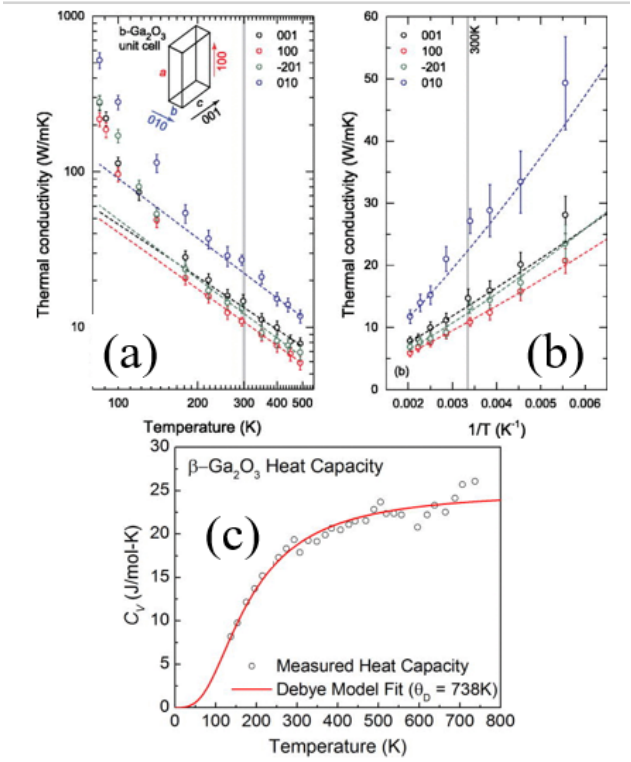

Figure 2.35: Shown here is temperature-dependent thermal conductivity of β-Ga_2O_3 measured along different crystal directions. (a) Shows the thermal conductivity and temperature are on the log scale. The inset shows a schematic of the unit cell of the β-Ga_2O_3 crystal. (b) Shows a linear plot of thermal conductivity against 1/T to highlight the dependence on temperature and the high-temperature 1/Tm fits more clearly. (c) Shows measured heat capacity of β-Ga_2O_3 as a function of temperature. The solid line is the Debye model fit from which the Debye temperature is obtained [98].

With advancement in growth and decent material properties makes Ga_2O_3 good candidate for devices; however, it takes a hit due to its poor thermal conductivity. Its thermal conductivity is about half of that of sapphire and one order of magnitude smaller than that of GaN. Because of the crystalline anisotropy, the thermal conductivity in β-Ga_2O_3 is very different along different crystal directions. The thermal conductivity is the highest along the [010] direction and lowest along the [100] direction at all temperatures used in the measurements. Guo *et al.* [98] measured the temperature-dependent thermal conductivity along four different crystal directions in the temperature range of 80-495K using the time domain thermoreflectance method. At room temperature, the [010] direction has the highest thermal conductivity of 27 W/mK while that along [100] direction has the lowest value of 10.9 W/mK (as shown in Fig.2.35). This also opens a lot of areas for research to design better thermal systems as has been done for GaN and other materials.

2.6.4 Devices

In order to make Power or an RF device three basic important capabilities are required: (a) Ohmic process (for Source-drain contacts). (b) Schottky process (for gate control). (c) Etching (to isolate the devices).

2.6.4.1 Ohmic contacts in β-Ga_2O_3

In order to achieve the predicted operation using β-Ga_2 O_3 transistor based on material property it is essential to achieve low contact resistance (R_c). Low R_c requires good ohmic contacts for which proper choice of metal or highly doped semiconductor coupled with good annealing process is required. Thermionic field emission theory defines characteristic energy of a metal-semiconductor contacts, E_{oo} (eV) as:

$$E_{oo} = \frac{qh}{4\pi}\sqrt{\frac{N}{\epsilon_o \epsilon_r \frac{m}{m_o}}} \tag{2.18}$$

Where q is the electron charge, h is the planks constant, N is the doping density, m is the tunnelling effective mass, ϵ_o is the permittivity of the semiconductor and ϵ_r is the permittivity of free space. Since E_{oo} is inversely proportional to the probability of an electron tunnelling through a metal semiconductor contact meaning the higher the value of E_{oo}, the more likely contact will be ohmic due to the domination of the tunnelling process [99]. Based on published data in the absence of any surface states the contacts on β-Ga_2O_3 would have ohmic behaviour if the doping density » 10^{20} Cm^{-3} (E_{oo}/kt»1) [99]. The job of making ohmic contacts on materials like GaN has been partially easy due to low barrier height possible by defect assisted metal nitride alloy formation during high-temperature annealing process. In terms of β-Ga_2O_3 Silicon implant has been used to form $N+$ regions annealed using RTA at 900-1000°C for best results.

This is followed by Titanium (Ti) and gold (Au) deposition and sometimes second anneal is used to obtain low R_c and values as low as 4.6x10^{-6} Ω cm^2 have been achieved already [100]. Some reports have observed thinning of the Ti metal after anneal using SEM suggesting interfacial reaction and not just the work function responsible for ohmic behaviour however, this area is still evolving [101].

2.6.4.2 Schottky contacts in β-Ga_2O_3

As seen earlier in Fig.2.32(b), E_{critic} of 8 MV/cm is expected from β-Ga_2O_3 which makes it a prime candidate for vertical devices. Since most important criteria for them is specific ON resistance during forward conduction. In an ideal case:

$$R_{on} = \frac{4V_B^2}{\epsilon \mu E_c^2} \tag{2.19}$$

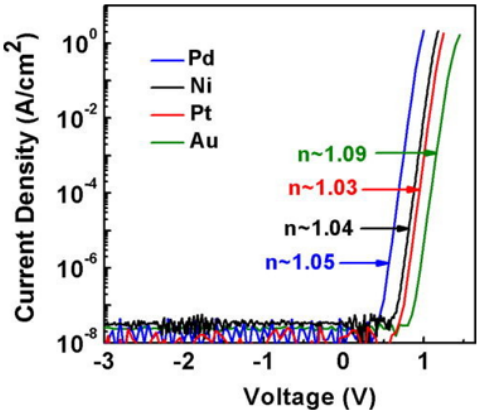

Figure 2.36: Shown here is J-V curve of pd, Ni, Pt, Au SBDs on [010] β-Ga_2O_3. Near ideality factor can be observed for most of the metal used [102].

Where μ is the mobility, E_c is the critical field for breakdown. Advantages of vertical β-Ga_2O_3 device: Low R_{on} possible at higher critical E_c so it can handle higher current and voltage.Metal contact to doped semiconductors are naturally rectifying due to presence of schottky barrier to charge the metal-semiconductor interface. Under forward bias the current density is given by:

$$J = J_s\left(\frac{qV}{e^{nkT}-1}\right) \tag{2.20}$$

And saturation current is given by

$$J = A^*T^2 e\frac{-\phi_B}{kT} \tag{2.21}$$

Where V is the applied bias, n is the ideality factor, A^* is the effect Richardson constant, and T is the temperature, q is the charge of an electron, k is the Boltzmann constant and ϕ is Schottky barrier height [99].

The ideality factor can be obtained from IV plot:

$$n = \frac{q}{kT}\frac{dV}{lnJ} \tag{2.22}$$

And the Schottky barrier height a be calculated as:

$$\phi_B = \frac{kT}{q}ln\frac{A^*T^2}{J_s} \tag{2.23}$$

$$A^* = \frac{4\pi m^* k^2}{h^3} \tag{2.24}$$

Where m is the effective electron mass and h is the Planck constant which for β-Ga_2O_3 is 41.1Acm^{-2} K^{-2} using m=0.342m_o.

Ti/Au has been most common Schottky contact. As shown in Fig. 2.36, for Pd, Ni, Pt and Au near unity ideality factor of 0.09, 1.03, 1.04 and 1.05 has been achieved so far as seen in Fig.2.36.

2.6.4.3 Etching in β-Ga_2O_3

The main technique for etching of β-Ga_2O_3 has been dry etching so far primary because of its advantage over wet etching in providing anisotropy in etch rate. Different methods from ion milling to plasma etch, and reactive ion etching has been widely used. During the process, the sample is masked using photo resist or sometimes even using dielectric such as SiO_2. Most of the literature available on etching has been done on inductively coupled plasma (ICP) with an etch rate from 120 Å/min to 1600 Å/min has been achieved with almost vertical side walls, few of the etching methods reported have been summarized here 2.4. Several reports of damage during plasma etch has been reported and this still remains an evolving area.

Growth method	Etch method	Etch rate (Å min^{-1})	Etch chemistry
MOCVD	ICP	350	SF_6/Ar
Bulk EFG	RIE	120	Cl_2/BCl_3
Bulk EFG (-201)	ICP	800	BCl_3/Ar
Bulk EFG	RIE	160	SF_6
Bulk (-201 EFG)	ICP	1600	BCl_3/Ar

Table 2.4: Summary of selected etching process used in Ga_2O_3 [103][104][105][106][107].

2.6.4.4 FETs: RF devices

High voltage β-Ga_2O_3 MOSFET operation has already made large strides including high electric field strength greater than GaN or SiC theoretical limit and blocking voltages 750 V and both types enhancement and depletion-mode devices. With measured mobility as high as 100 cm^2/V.s, an opportunity exists for β-Ga_2 O_3 transistors to operate as an amplifier. This could have circuit level implications such as monolithic or heterogeneous device integration of high-efficiency RF amplifiers, RF switches, and power switches capable of GHz switching speeds. Ga_2O_3 is expected to achieve significantly reduced parasitic switching losses through scaling [108]. Green *et al.* [109] showed first RF device with the most recent process combined with the ohmic cap layer and gate-recess process on a device with L_{SD}, G_D, L_G, and W of 3.8 μm, 1.6 μm, 0.7 μm, and 1x100 μm respectively. The channel and cap layer were grown by MOVPE at 180 nm and 25 nm and doped by Si at 1x10^{18} cm^{-3} and 1x10^{19} cm^{-3} respectively. Approximately 90 nm of channel material remained after the gate recess etch. The cap layer was not optimized resulting in Rc = 3.3 Ω.mm. The channel μ = 96 cm^2/V.s resulted in R_{SH} = 4850 Ω/sq. A 20 nm ALD Al_2 O_3 gate dielectric was used. Based on small-signal measurements of several devices with W = 1x100 μm with V_{DS} = 10 V and V_{GS} biased at gm-peak a Gain > 10 dB was observed at 1 GHz with f_T > 3 GHz and fmax approaching 10 GHz (as shown in Fig.2.37). Class-A load-pull data at 800 MHz with Pout = 0.23 W/mm with V_{DQ} = 25 V was reported.

Overall this chapter present summary of material properties, formation of 2DEG in heterostructures which serves the base for understanding the device. The device fabrication process

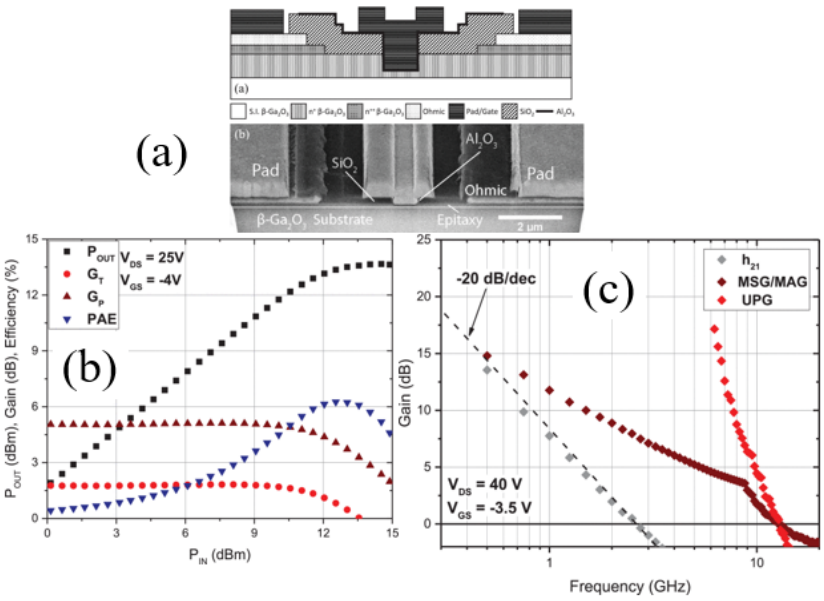

Figure 2.37: (a) Shows device cross-section schematic is shown for the β-Ga_2O_3 MOSFET under test with a focused ion beam (FIB) cross-sectional image of the device. This is the bottom finger of the 2x50 μm split-finger device. (b) Shows 800 MHz Class-A power sweep of a 2x50 /mum β-Ga_2O_3 gate recessed MOSFET. (c) Shows forward current gain (h21), maximum stable gain/maximum available gain (MSG/MAG), and unilateral power gain (UPG) calculated from the scattering parameters (S-parameters) and plotted as a function of frequency. A cut off frequency (f_T) and maximum oscillating frequency (f_{MAX}) were measured to be 2.7 GHz and 12.9 GHz, respectively (V_{DS}= 40 V) [109].

and working is explained highlighting two device type: GaN on SiC for RF and GaN on silicon for power which are the two types of devices discussed in this thesis. Buffer doping and its consequence on reliability of device for both sample type are explained in detail. Last part of the chapter covers literature review about Gallium oxide and its challenges.

CHAPTER 3

TEST STRUCTURES AND EXPERIMENTAL TECHNIQUES

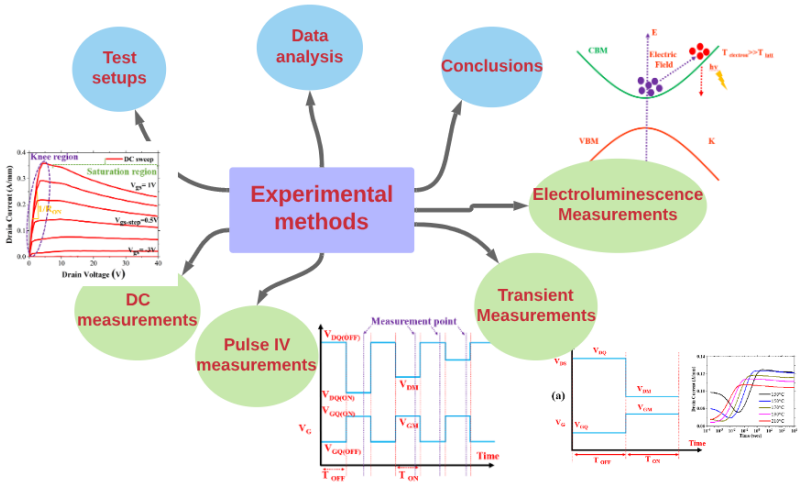

Figure 3.1: Shows overview of topics explained in this chapter.

To solve any scientific problem it requires a great deal of planning, use of proper testing equipment's and data analysis to make a conclusion as shown in steps above in Fig.3.1. This chapter explains in detail the experimental techniques and analysis method used throughout the thesis in various chapters. Some of the techniques are developed during the course of the study and has been mentioned in the chapter. Reference to existing techniques and methods from published work has been made accordingly.

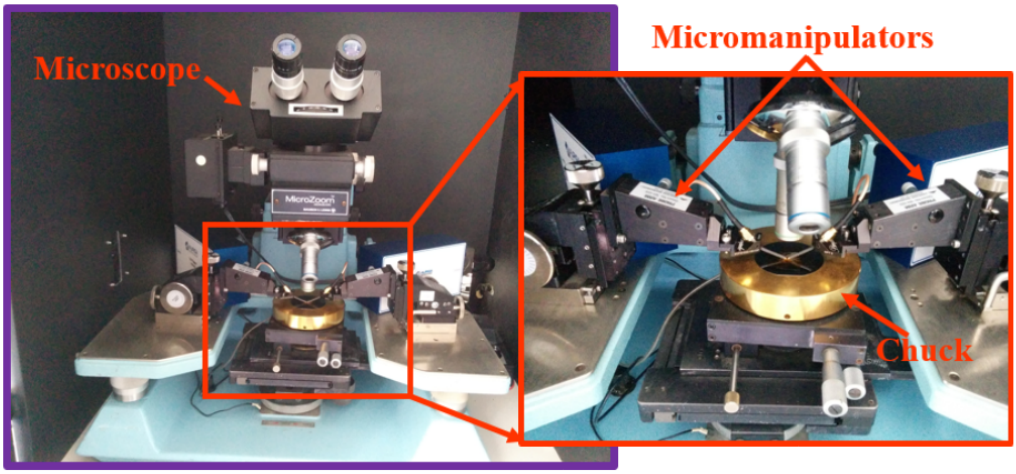

Figure 3.2: A probe station is shown which consists of chuck, microscope and micro manipulators to adjust the probe allowing to make contact with the device.

3.1 Test setup

All the measurements reported in this thesis has been performed on the wafer using a probe station coupled with source measuring units (SMU).

1. ***Probe station:*** A probe station comprises manually controlled stage also called a chuck on which the wafer or the sample rests during the experiment held via vacuum as shown in Fig.3.2. They can be round or square and vary in size from 4 to 6 inches and are made up of material such as tungsten, aluminum or steel. During measurements, it is electrically grounded; however, if required substrate bias can be applied using triaxial connectors. To vary the measurement temperature conditions a thermal chuck can be used which has water cooled PID controlled closed loop system allowing temperature range of 25°C to 200°C. Manual micro-positioners each with independent x, y and z movements and with triaxial connectors are used to make contacts with the device. Microscope with multiple objectives sits on top of the probe station allowing visuals of the device.

2. ***Measuring instrument:*** A source measuring unit (SMU) is used which has both sourcing and measuring capabilities. SMU offers a four-quadrant, precision source, which means it can source current or voltage depending on the settings and load it can go from maximum positive output to maximum negative output without changing test leads. The input resistance of SMU is very high (around 100 TΩ) which helps to minimise circuit loading when making voltage measurements from high impedance sources. It offers very low and precise current measurement sensitivity typically as low as 10pA. Most of the measurements reported in this thesis are performed using Keithley SMU which are controlled using LabView or Test script builder (TSB) software.

3.2 DC measurements

DC measurements can be used to avail a lot of information about the HEMT device ranging from leakages to contact resistance. By making use of source, drain (ohmic) and gate (Schottky) contacts multiple device parameters can be extracted such as:

- Pinch off voltage
- Maximum Drain current
- Mobility
- Transconductance

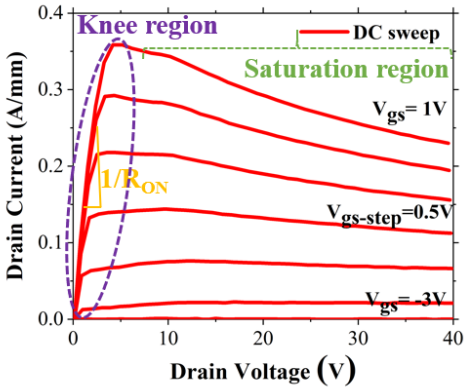

Figure 3.3: DC measurements of GaN HEMT is shown with V_{GS} varying from -3 up to 1 V with 0.5 V steps. Different regions observed in the characteristics are marked.

3.2.1 DC performance

Fig.3.3 shows a typical example of on wafer GaN HEMT DC output and transfer characteristics measured using an SMU. As seen the gate bias (V_{GS}) is varied from -3V to V_{GS}=1V with 0.5V V_{GS} step showing maximum measured drain current (I_{DSS} of 0.38A/mm shown in Fig.3.3. The entire characteristics can be divided into three different regions,linear, knee and the saturation region.The knee regions indicates the maximum achievable ID_{MAX} while the saturation shows the self heating in the device (negative conductance). Using physical dimensions and measured drain, important current parameters such as mobility and threshold voltage (V_{TH}) can be extracted using the equation here:

$$I_D = \frac{W_G.\mu.C_{GS}}{L_{DS}}\left[(V_{GS}-V_{TH})V_{DS}-\frac{V_{DS}^2}{2}\right] \tag{3.1}$$

Where μ is mobility, W_G is gate width, L_{DS} is source-drain distance, C_{GS} is gate capacitance, and V_{TH} is threshold voltage. ON resistance (R_{ON}) can also be extracted using the inverse of the

slope from output characteristics in the linear region. The sweep rate during DC sweep is also important and can reveal important information about the trapping/de-trapping and has been discussed in detail in the next chapter (Kink in GaN HEMTs).

The transfer characteristics of the device illustrate drain current dependence on gate voltage for different drain voltages as shown in Fig.3.4. Transconductance (g_m) is an important parameter for microwave applications and can be extracted from a transistor transfer characteristic. g_m is related to the gain of the device and represents the effectiveness of gate modulating the drain current (I_D).

(3.2)
$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

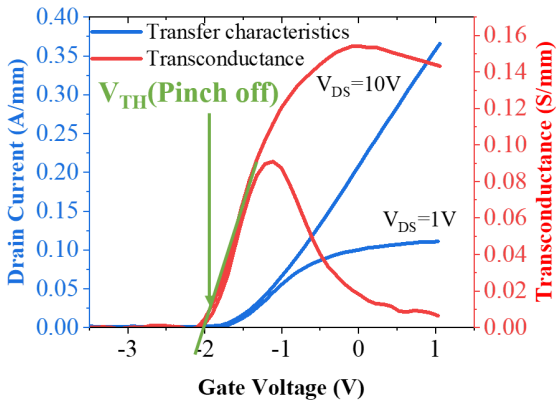

Figure 3.4: DC transfer characteristics of GaN HEMT measured at V_{DS} =1 V and 10 V with V_{GS} varying from -4 V up to 1 V with 0.2 V steps is shown. The transconductance (g_m) of the measured device is plotted on the the other Y axis as well.

From the intercept of transconductance linear fit with x-axis, the threshold voltage (V_{TH}) or the pinch off voltage is defined. The transconductance (g_m) mostly depends on device contacts, barrier thickness and source to drain distance which can be measured experimentally as well.

3.2.2 Contact Resistance

Based on the structure shown in Fig.3.5(a) there are three main resistors, two contact resistance (R_C) and one sheet resistance. Transmission line method (TLM) is used to measure contact resistance of the structure as shown in Fig.3.5(b). In this process resistors of several different lengths but with all other details same are measured, and the total resistance of each of them are plotted against the distance. In the limit of zero length, the residual resistance is twice the contact resistance and is found from the graph by extrapolating back to zero with the x-axis as shown in Fig.3.5(c). With three resistors components and assuming that voltmeter resistance is

larger than the probe resistance the total resistance R_T can be expressed in the form of equation below [110].

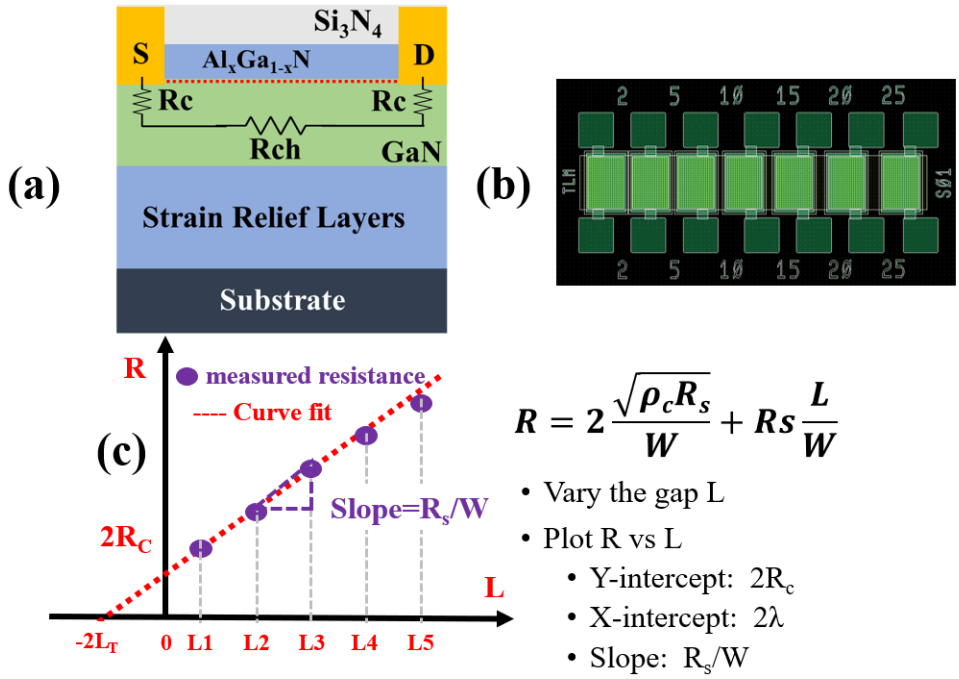

Figure 3.5: Shows the schematic with three main resistance sources, two R_C and one R_{sheet} (a), the multiple contacts TLM arrangements (b) and the plot with measured resistance plotted for various length and the fitting (c).

$$R_T = \frac{V}{I} = 2.R_C + R_{Sheet} \tag{3.3}$$

The sheet resistance the third component shown in the schematic can also be extracted from the slope.

$$slope = \frac{R_{sheet}}{W} \tag{3.4}$$

Since the devices used have planar geometry, the flow of current across the device is not uniform specially around the contact edges. Majority of the current flowing in to the contact are crowed at the edge (most of current takes this path) while far off from the edge has much lower current as shown in the Fig.3.6. It has been shown that this current crowding at the edge drops off in an exponential fashion with a characteristic length of L_T, which is known as the transfer length (L_T) or the effective length of the contact. Transfer length can be obtained from the above curve by extrapolating back to the horizontal axis, where the intercept = -2L_T and the equation expressed here:

$$R_T = \frac{R_{sheet}}{W}(L + 2L_T) \tag{3.5}$$

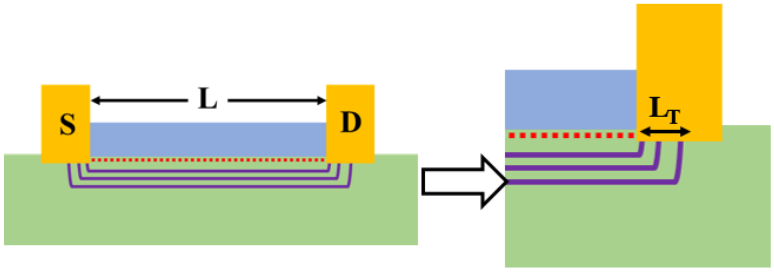

Figure 3.6: The figure here shows the current crowding taking place around the edge of the contacts and representing the transfer length.

3.2.3 Test structures for leakages

Multiple layer stack makes HEMT a complex structure and therefore makes understanding of leakages through the structure more important. By using special test structures, several leakages path can be identified such as:

- Surface Leakage
- Buffer leakage (lateral and vertical)
- Substrate leakage

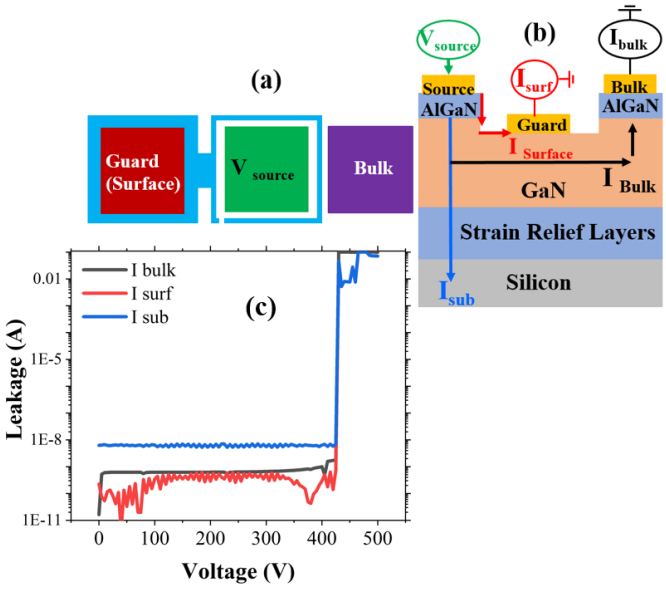

Figure 3.7: Shows the schematic of the test structure (a), the schematics of the measurement connections on the test structure (b) and the measured leakages using the structure (c).

A top view and a schematic cross-section of the structure are shown in Fig.3.7 (a). It consists of two ohmic pads on top of the AlGaN layer (labeled as source and bulk contacts) separated by a mesa area. The third pad is connected to a guard ring around the isolated source pad and sits directly on top of the etched GaN layer as shown Fig.3.7(b). This pad is used to monitor any surface leakage path along the GaN surface as shown in the schematic. The bulk contact will measure any lateral leakage within the bulk of the epitaxy, and Isub will measure the vertical leakage to the Substrate. The surface leakage is shown in Fig.3.7 and it is in the order of 10^{-10} A being much lower than the lateral bulk leakage of about 1nA when biasing the source pad up to 500 V as shown in Fig.3.7 (c). It is quite clear that bulk lateral leakage exceeds surface leakage. The vertical substrate buffer leakage to the substrate is an order of magnitude higher at 10^{-8} A.

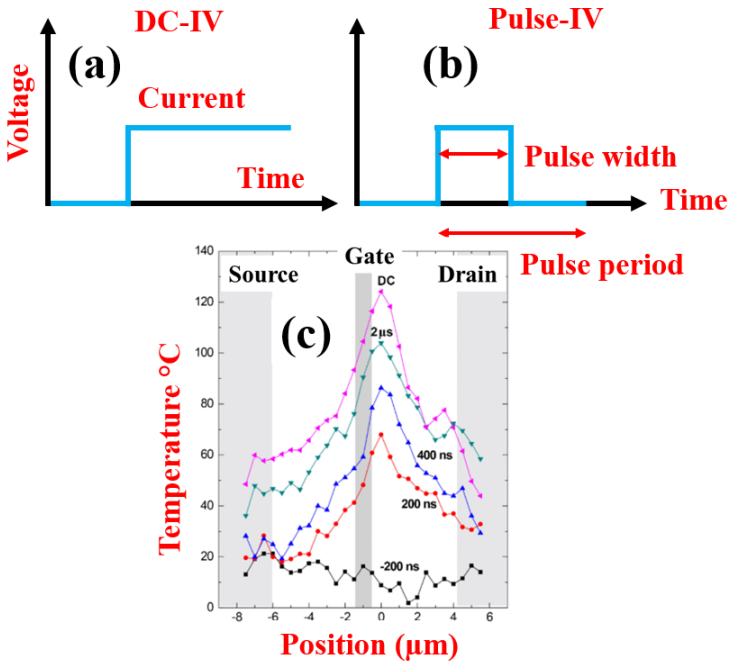

Figure 3.8: Schematic showing DC IV (a) and Pulse IV (b) measurement technique (c) typical example of device heating in GaN HEMT device is shown [111].

3.3 Pulse IV Measurements

Most of the information obtained from DC is about the performance during static operating conditions. DC-IV measurements are continuous measurements which are more prone to heating and not much information can be extracted about the trapping. Step pulse IV measurements can be utilised to investigate two key aspects: self-heating and trapping effects as shown in Fig.3.8. Based on choice of material and its associated thermal time constant a specific pulse length and pulse period is used to avoid any self-heating. All the pulse measurements in this thesis have been performed using Auriga pulse kit (Model 4850).

Method: In this method voltage signals of square pulse is used for gate and drain bias from a steady state quiescent bias point (Q point) to obtain the value of current at the end of pulsed length and then the device stays again at Q point for the rest of the pulse duration until the next voltage pulse is applied. The schematic of the pulse is shown in Fig.3.9.

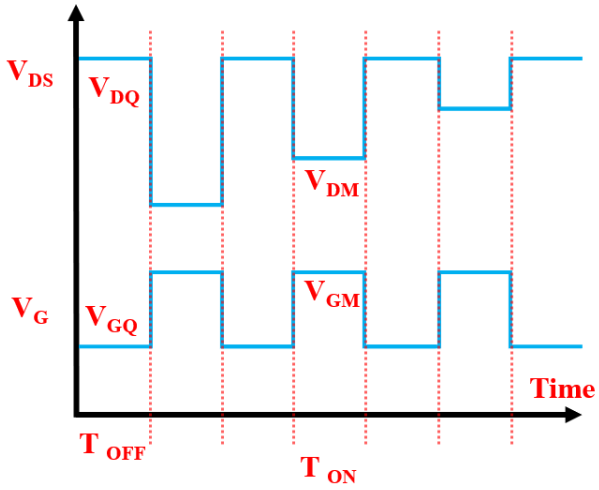

Figure 3.9: Example of Pulse IV setup showing gate and drain voltage step change with respect to time. The ON and OFF duration is defined as T_{ON} and T_{OFF}.

3.3.1 Self heating

The pulse length was typically set to 200 ns with a pulse period of 1ms while sometimes during the large drain bias range pulse length of 1us has been used. The main purpose of using small pulse length is to avoid any self-heating during the pulse IV. To understand the self-heating, Pulse IV from measurements from steady state Q point (V_{GS}=0V, V_{DS}=0V) is compared with DC IV measurements. The use of shorter pulse length doesn't allow sufficient time for the device to heat which is inevitable during DC sweep. An example of DC-IV and Pulse IV measured with 1μs pulse length and 1ms pulse period showing the evidence of self-heating during DC IV is show in in Fig.3.10. A temperature profile measured between the source and drain contact of a single-finger, 125μm-wide AlGaN/GaN HEMT on a SiC substrate, operated at 20 W/mm is shown for a range of times after switch-ON similar to as shown in (Fig.3.8(c). Heating at the gate edge can be observed with increasing ON times [111].

3.3.2 Trapping effects

Trapping effects can be understood by using double pulse measurements which applies both gate and drain pulses with separately specified quiescent voltages for drain and gate. While gate-pulsed measurements were used to probe the contribution of mainly surface states on current output, applying both gate and drain voltage in pulses includes the probing the surface and also

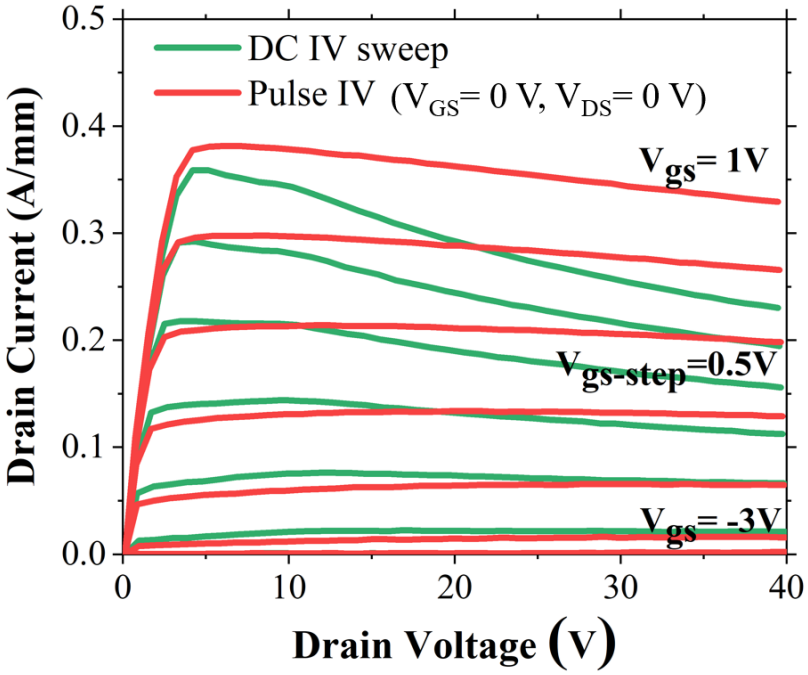

Figure 3.10: DC and Pulse IV output characteristics is overlaid showing drop in current during DC measurements due to self heating.

activate barrier traps underneath the gate as well traps found in the drain access region or the buffer layer. The Q points are chosen such that device stays in an off-state allowing electrons to be depleted under or in the vicinity of the area under probe with some being trapped. The measured current output under these Q point stress conditions, when compared with steady state, reveals information about the trap states and the quality of surface or buffer, the schematic of choices for different Q points in shown in Fig.3.11.

This is a quick and reliable method which allows one to investigate the changes in important parameters such as drain current (I_{DSS}), on resistance (R_{ON}), transconductance (g_m) and threshold voltage (V_{TH}) induced by the capture of carriers at trap-states within the HEMT structure without having any thermal effects. An example of Pulse IV with different gate and gate-drain stress is shown in Fig.3.12 without any dispersion in knee indicating good surface and buffer qualities. To insure good contact during the pulse measurements and to minimise any parasitic capacitance RF GSG picoprobes by GGB Industries connected to microprobe holders using extremely short cables were used in this set-up.

3.4 Transient Measurements

Although Pulse IV provides a quick assessment of device behaviour, the measured current is only applied for a small duration. To gain insight into the kinetics of involved charge (de)trapping mechanisms, and the subsequent identification of involved deep-levels transient measurements

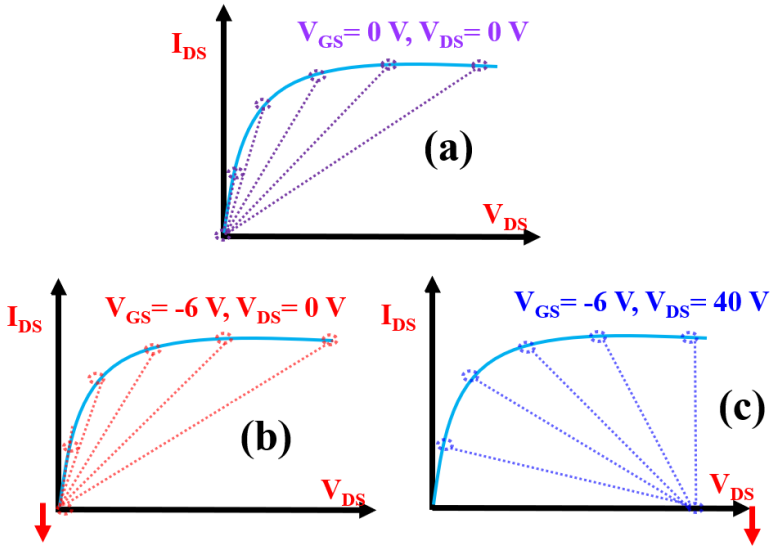

Figure 3.11: Pulse IV schematic for different quiescent point (a) V_{GS}= 0 V, V_{GS}= 0 V (steady state), (b) V_{GS}= -6 V, V_{GS}= 0 V (gate stress) and (c) V_{GS}= -6 V, V_{GS}= 40 V (gate-drain stress) is shown.

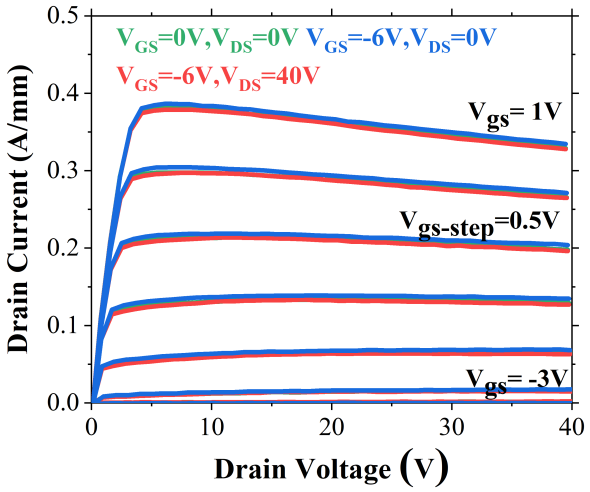

Figure 3.12: Pulse IV with different quiescent point V_{GS}= 0 V, V_{GS}= 0 V (steady state), V_{GS}= -6 V,V_{GS}= 0 V (gate stress) and V_{GS}= -6 V,V_{GS}= 40 V (gate-drain stress) is shown with minimum dispersion in knee region.

been used. Drain current transient provides information regarding trapping/detrapping time constants typically for long measurement intervals. During the measurement, the device is kept under off state or the trapping state for the given amount of duration and immediately switched to on state or low-field linear region with current being monitored over time typically over hundreds of seconds. Bisi *et.al* [112] has recently shown an interesting study about the choice of transient

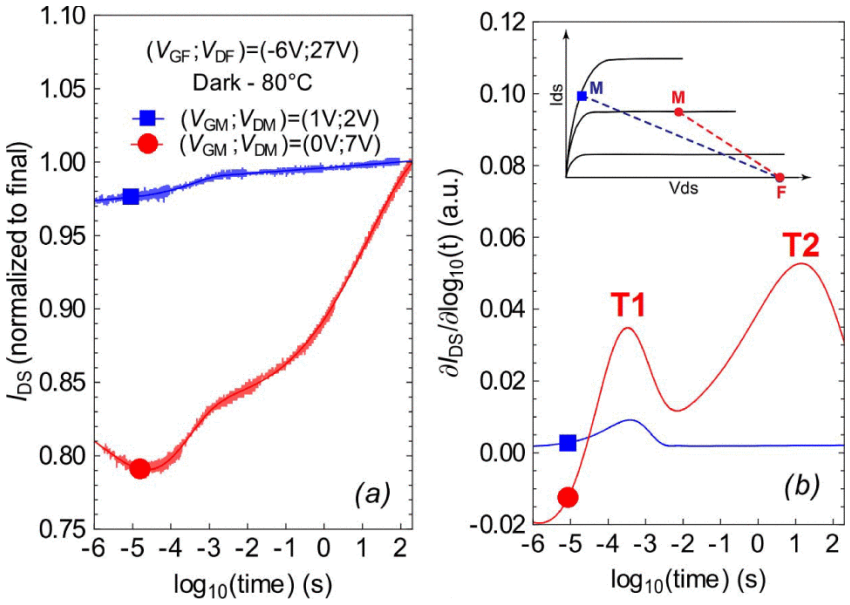

Figure 3.13: (a) Drain current transients performed in the linear and saturation regions, and (b) related differential signals recorded in linear region detect only a weak emission process, while those recorded in saturation region reveal much higher current collapse and the presence of two emission processes labeled T1 and T2 [112].

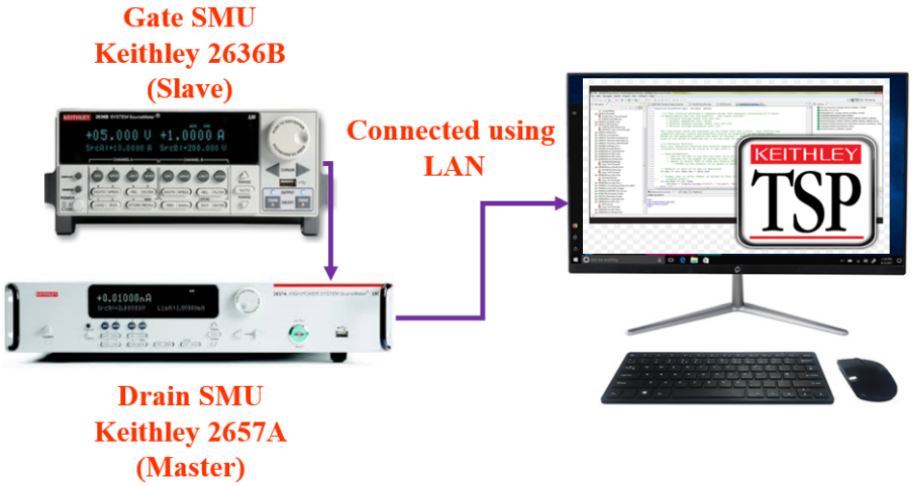

Figure 3.14: Schematic of developed transient test setup is shown here. It involves two keithley system integrated using test scrip builder software interface.

being measured in the linear and saturation region having a significant impact on the results: for the specific case-study, the transient recorded in linear region detected only a weak emission process (blue curve in Fig.3.13 (a)), while that recorded in saturation region (red curve in Fig.3.13 (a)) revealed remarkable current collapse, and the presence of two distinct current recovery processes, whose peaks in the derivative spectrum in logarithmic time scale (Fig.3.13 (b)) have

been labelled respectively "T1" and "T2". This result is very well correlated with that obtained with pulsed measurements, which indicate that current collapse is mainly caused by threshold voltage shift, hence manifesting itself predominantly in the saturation region. What worth to be learnt from this experiment is that to obtain meaningful and exhaustive deep-level spectroscopy, the measurement bias should lie in the current-voltage region in which the device under test suffers from the most prominent current-dispersion effects.

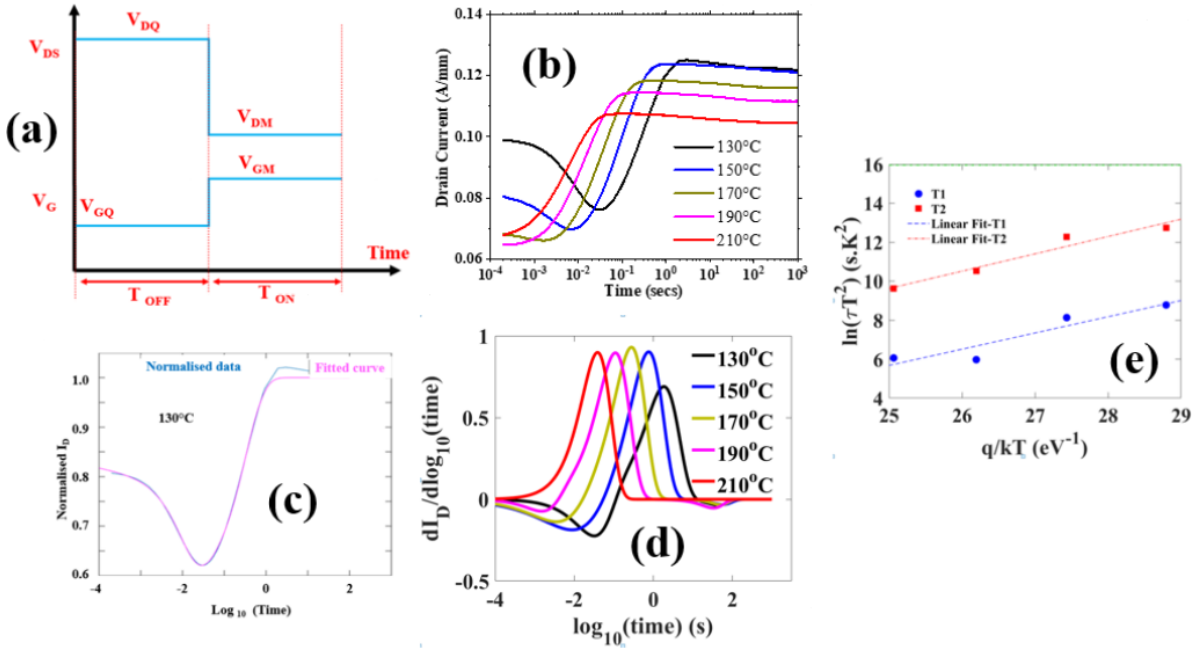

Figure 3.15: Transient measurement schematic is shown in (a), (b) shows measured example over five different temperature range, the fit has been performed on one of the measured transient, (d) shows the derivative plot for all the transient measured and (e) shows the Arrhenius plot used to extract the activation energy (measurements shown here are performed on wafer A used in Chapter 4).

Similar approach has been taken during most of the work done in this thesis with transient recovery condition has been chosen with the specific condition of impact. To be able to choose any trapping conditions and recovery on state conditions with different time intervals a custom software was developed during the study. A current transient kit which is capable of transients from 1 μs to any arbitrary length of time with logarithmically spaced data interval has been developed schematic of which is shown in Fig.3.14. Two different kits 2657A high voltage kit and Keithley 2636B dual channel SMU has been integrated through LAN to enable high-speed data transfer rate. Both the instrument has been synchronized using an oscilloscope to being able to perform switching of V_{GS} and V_{DS} precisely at the same time. Bringing these two instrument also allows pulsing from wide bias points across a range from few mV to up to 3 KV. Test script builder has been used to control the software, and a program was written from scratch to allow to

smooth data accusation. Although Keithley 2657A is capable of going up to 1μs pulse the 2636B has limited capability of 100μs. These rise and fall times has been measured using oscilloscope under range of different biasing conditions with the transient setup to ensure the setup has no ringing or error in rise and fall time.

A specific biased stress point is chosen which is applied for given amount of duration after which bias is switched to measured condition and data is recorded for 1000's of seconds. Based on the data obtained and the trapping time constant we further repeated measurement at different temperature, and their fit to a stretched multiexponential function enables the extraction of apparent trap activation energy using Arrhenius plot, the steps involved are shown in the Fig 3.15. The fitting functions most commonly used is:

$$I_{DS}(t) = I_{DS},final - \sum_{i}^{N} A_i e^{\left(-\frac{t}{\tau_i}\right)^{\beta_i}} \tag{3.6}$$

where the fitting parameters A_i, τ_i and $beta_i$ are respectively the amplitude, the typical time constant and the non-exponential stretching-factor of the N detected charge emission ($A_i > 0$) or capture ($A_i < 0$) processes (N typically ranges between 2 and 4 depending on the analyzed samples) [112]. After successful implementation of fitting functions the peak values are identified and plotted with $\ln(\tau T^2)$kT vs. q/kT which gives trap energy from the slope while the the cross-section is extracted from the y-intercept.

3.5 Back Bias Measurements

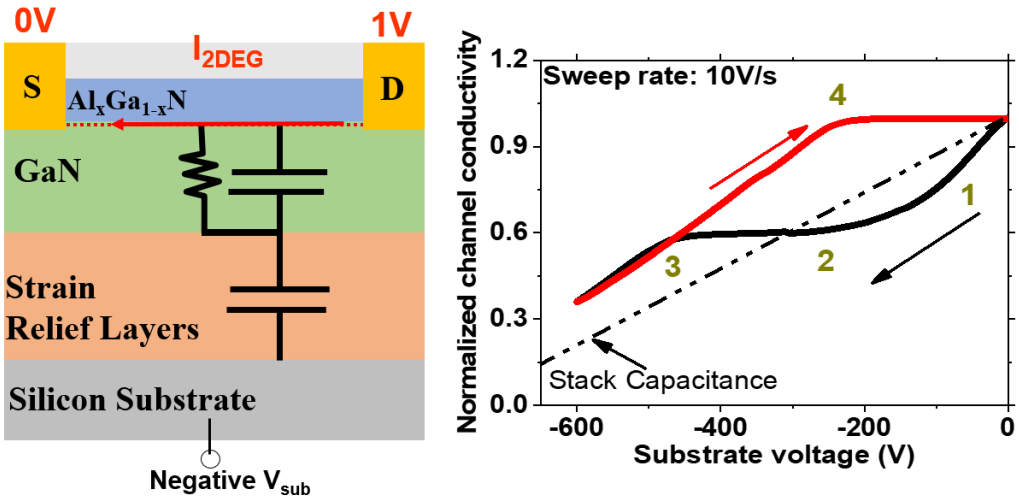

Figure 3.16: Back bias measurement schematic is shown along with measurement example on a TLM contact showing positive charge storage based on the deviation from the calculated stack capacitance.

It's a measurement technique based on using silicon as a back gate to control the channel conductivity in-order to evaluate the charge storage. A small bias of 1 V is applied on the drain to monitor the channel conductivity while substrate bias is ramped up to -600 V (a typical value for epitaxy used for power devices), the ramped voltage generates a vertical displacement current which gives information about transport in the layer. With the channel remaining on while the substrate is ramped, makes this technique surface insensitive and give information primarily about the buffer. Information related to the type of charge storage can also been extracted by comparing the ramp with theoretically calculated stack capacitance [67]. A example of back bias measurement preformed on a TLM contact is shown in Fig.3.16, the stack capacitance is shown with the dotted line. The positive charge storage in the expitaxy can be seen at end of the measurement.

3.6 Electroluminescence Measurements

Electroluminescence (EL) is an emission of light in response to an applied electric field. An electrically excited process results as the radiative recombination of excited electrons leading to a non-equilibrium carrier concentration in electronic bands or states of a defect structure, induced by electrical excitation. In GaN HEMTs, a broad EL signal is typically observed during high

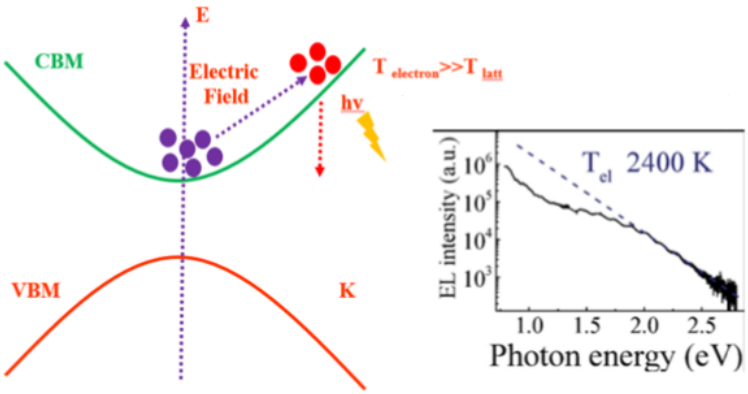

Figure 3.17: Scattering mechanism during high electric field leading to hot electron generation causing the light emission is represented in this figure. The high energy tail observed in EL spectrum follows a Maxwell-Boltzmann distribution [113].

field operation and can be attributed to hot electron generation in the high electric field region of the device. A high electric field between gate and drain due to a high bias accelerating the channel electrons, which then gain kinetic energy initiating the excitation into a higher energy state within the conduction band as represented in Fig.3.17. This is followed by light emission where the emitted spectrum is characteristic for the kinetic energy of hot electrons. The high energy tail observed in EL spectrum (seen in Fig.3.17) follows a Maxwell-Boltzmann distribution:

$$I_{EL}\alpha\left[\frac{1}{\kappa_B(T_{el}-T_i)}\right]^{\frac{3}{2}}\sqrt{E_{Ph}}.exp\left[-\frac{E_{Ph}}{\kappa_B(T_{el}-T_i)}\right] \tag{3.7}$$

with the EL intensity I_{EL}, the photon energy E_{Ph}, and the Boltzmann constant kB. T_{el} and T_l denote the hot electron and lattice temperature, respectively.

Shigekawa *et al.* in [114] and [115] pointed out that EL in GaN HEMTs is not due to band-to-band recombination, while it is generated by hot electrons accelerated by the longitudinal electric field present in the channel. Radiation is hence emitted through Bremsstrahlung process, due to the deceleration of electrons at charged centers.

Since the EL distribution is directly correlated to hot electrons following the electric field in the device channel, the EL profile enables the analysis of the electric field distribution. The maximum EL emission is observed at the peak electric field location in the device, the ratio of EL intensity I_{EL} and drain current I_D follows:

$$\frac{I_{EL}}{I_D}\alpha exp\left(\frac{C}{V_{DS}-V_{knee}}\right) \tag{3.8}$$

where C is a constant. This correlation makes EL analysis an important tool of understanding the field profile specially during high voltage operation.

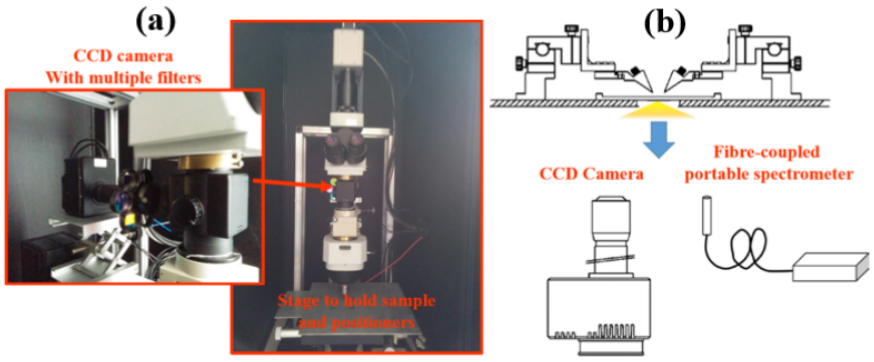

Figure 3.18: EL set up used for imaging from top side (a), (b) shows the setup used for backside illumination coupled with spectrometer and CCD camera [116].

In this thesis detail study of breakdown in GaN HEMTs has been done using EL kit. Two setup have been used: one with top side camera mount to study the EL image, the second was used along with spectrometer from the back side as shown in Fig.3.18 [116]. EL imaging has been carried out with 50x objective and a Hamamatsu digital charge-coupled device (CCD) camera, while the spectra were recorded with a broad-spectrum fiber coupled to a compact spectrometer (Maya 2000-Ocean optics QEPro) sensitive in the range 200-1100 nm. Standard positioners and keithley SMU has been connected in order to bias the device for various operating points. The

oscillations or bump observed in the tail of EL spectra recently has been shown to be related to GaN and SiN_x with a simple exponential response or related to other discrete transition layers as seen in Fig.3.17 [113].

CHAPTER 4

"KINK" IN ALGAN/GAN-HEMTS: FLOATING BUFFER MODEL

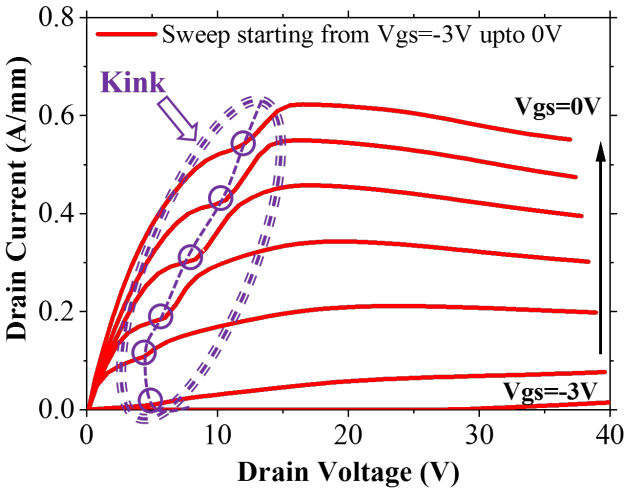

Figure 4.1: DC output characteristics of a GaN HEMT showing onset of kink

Kink, a hysteresis in the output characteristics of transistor has been observed in many generations of devices ranging from silicon MOSFETs, GaAs MESFETs, GaAs and InP HEMTs and AlGaN/GaN HEMTs technology. Several observations have been reported including drain, gate bias dependence, reduction of drain electric field and source potential barrier, issues related to surface or buffer trapping, impact ionization and strong light-sensitivity.

This work focuses on reporting on a new floating buffer model explaining kink effect observed primarily in Fe-doped AlGaN/GaN HEMTs at low drain bias. Using two identical wafers with the only difference being the carbon buffer doping it is shown that unintentionally doped background carbon can make the GaN buffer p-type allowing it to electrically float. It is further shown that

reverse bias trap-assisted leakage across the junction between the 2DEG and the p-type buffer can provide a mechanism for hole injection and buffer discharging at just a few volts above the knee, explaining the "kink" bias dependence and hysteresis at low drain bias, previously this has been assigned due to impact ionization. Using simulations and experimental measurements, it is shown that HEMTs with different background carbon can have dramatically different kink behavior consistent with the model. Drain current transient studies performed shows positive and negative magnitude signals with 0.9 eV activation energy which corresponds to changes in occupation of carbon acceptors located in different regions of the GaN buffer, this has been often ascribed as electron and hole traps in the past. The observation of such signals from a single trap calls into question conventional interpretations of these transients based on bulk 1D DLTS models for GaN devices with floating regions. In this work all the measurements and experimental analysis were carried out by myself while the simulations were performed by Prof M J Uren. All reported simulations graphs and cross sections were generated by me. The model was developed together. All the sample used in this work are provided by IQE, Cardiff and were processed at FBH under the project funded by ESA. This chapter has significant content reproduced from my published work [117], with permission from IEEE. Additional measurements have been added and all the figures have been reproduced with some reused after permission from IEEE.

4.1 Introduction

The kink effect is a hysteretic instability of FET drain current which is observed during a slow drain bias sweep. The current shows a small step increase a few volts above the knee region on the forward sweep, with little or no reduction on the return sweep as shown in Fig.4.1. It has been observed in all generations of FETs, irrespective of the material system, whenever the substrate or surface is able to store charge and achieve a potential which diverges from the ground. In partially depleted SOI MOSFETs or SOS MOSFETs [118], the floating conducting Si buffer is charged by a hole current from impact ionization leading to the charging of the floating p-type body region. In GaAs FETs, the buffer is semi-insulating and can store impact ionization derived charge in deep trap states back-biasing the 2DEG and causing a kink [119]. Kink has also been observed in GaN HEMTs at both cryogenic [120] and room temperatures, with surface related traps originally assigned as the cause [121], although this explanation became untenable as it was unchanged as passivation schemes improved. Another theory attributed kink in GaN HEMTs to impact ionization [122]. However, the fact that the kink is often seen just a few volts (as little as 2-3 V) above the knee makes it implausible for the carriers to have sufficient energy to cause impact ionization and provide a supply of holes. As a result, several models have been suggested based on unusual defect properties. Meneghesso *et al.* [123] proposed that a strongly field dependent de-trapping process from deep acceptor states. They argued that

kink is originated by a buildup (at low drain bias) and subsequent release (at high drain bias) of negative charge, resulting in a shift of pinch-off voltage toward more negative voltages which leads into a sudden increase in drain current. Since kink is correlated to pinch-off voltage shifts, these traps responsible should be located under the gate, either in the AlGaN barrier or in the GaN buffer. These states were linked to the epitaxy rather than being processing-related and showed a complex light sensitivity which was related to yellow cathodoluminescence [124]. Their model matched well explaining the presence of deep traps in the GaN buffer and would also explain both the spectrally resolved photo stimulation experiments and the slow negative charge buildup. On the other hand, Wang *et al.* [125] found that in their devices there was no kink in the very first bias sweep, contrary to the observations in [123] [124], and that the kink magnitude increased with maximum drain voltage [125]. They proposed a different model suggesting that kink could be induced by hot electron trapping and field-assisted de-trapping via donor-like traps in the GaN buffer layer or in the vicinity of the gate. They extracted an activation energy of the traps responsible for the kink effect and found it to be 589 ± 67 meV from temperature-dependent transient measurements. Both these models required strongly field dependent capture cross-sections and trapping/de-trapping processes based on unusual deep level defect properties which cannot be explained by conventional defect models. Furthermore, these defects are not compatible with Poole-Frenkel barrier lowering or conventional deep-levels with sometimes contradicting arguments.

In this work, an alternative explanation of kink effect in GaN HEMTs on silicon carbide (SiC) using conventional deep-levels is provided. Lot of work has been done on improving the buffer qualities in order to make buffer semi-insulating however recent studies has suggested that dopant also brings in several difficulties with them. Uren *et al.* [19] explained the effect of background carbon presence in Fe doped GaN and showed how Fe which is common dopant for RF GaN HEMTs to make the buffer semi-insulating and suppress off-state leakage and ideally expected to be weakly n-type converts to p-type with presence of even small amount of carbon impurity if they exceed the density of any intrinsic donor states [19]. These p-type buffers on an insulating substrate such as SiC are isolated from the 2DEG by a P-N junction and hence can float allowing them to develop a charge and back-gate potential relative to the 2DEG resulting in bias-history dependent instabilities. In contrast, n-type buffer devices would show well-behaved characteristics without the strong hysteric effects characteristic of the floating p-type buffer. Since then extensive work on carbon doped GaN-on-Si power switching devices has shown that the buffer is indeed p-type and floating [67]. GaN-on-Si power devices all use a structure which has an AlGaN top barrier, an undoped GaN channel layer, a carbon doped GaN layer with a carbon density of $\sim 10^{19} cm^{-3}$, a superlattice or step-graded AlGaN layer, AlN nucleation layer on Si substrate. These devices despite delivering 600V operation and excellent R_{ON} have been found to be highly susceptible to a dynamic R_{ON} instability where R_{ON} increases after off-state bias, only recovering after up to 1000s. Huge variation is seen between apparently similar technologies

[126]. This effect has now been successfully explained by a model of the epitaxy which treats the carbon doped semi-insulating epitaxy as a set of "leaky dielectric" layers [67]. Small leakages within and between layers charge the geometric capacitances leading to long time-constants for charging and discharge as shown in Fig.4.2. This model has been able to explain the complex

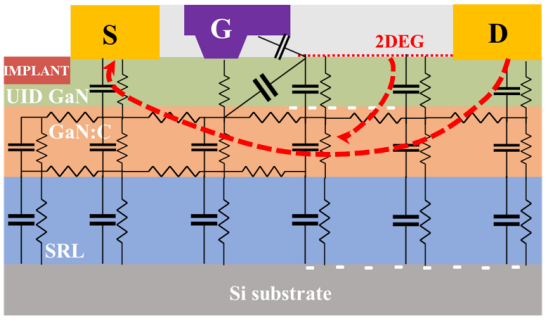

Figure 4.2: Leakage paths and geometric capacitances in a semi-insulating buffer, arrow shows flow of hole current.

drain bias dependence of dynamic R_{ON}, and the resurf-induced high breakdown voltage that the technology can achieve.

Here it is shown how the "leaky dielectric" principles established to explain dynamic R_{ON} in power devices can also be used to explain the kink effect. Kink strong dependence on growth conditions which impact carbon concentration is shown. This work gives an explanation for occurrence of kink in iron-doped (Fe) AlGaN/GaN HEMTs based on a "leaky dielectric" model of a floating semi-insulating p-type GaN buffer [67], together with conventional deep-level defect behavior. The supply of holes to charge the buffer then arises primarily due to band-to-band trap-assisted leakage paths rather than via impact ionization. Simulations of the hysteresis associated with the kink show that it can be enabled and modified by small changes in the concentration of background carbon that are well below the Fe density. It also demonstrates that conventional interpretations of drain current transient spectroscopy can be flawed in devices with a floating p-type GaN buffer.

4.2 Sample details and measurements

Two wafers were grown using MOCVD with nominally identical layer structure of AlGaN barrier, GaN buffer and AlGaN nucleation layer on insulating Silicon carbide (SiC). Secondary ion mass spectrometry (SIMS) measurements were undertaken on similar wafers as shown [127] [128]. Both wafers incorporated a conventional Fe doping profile in the GaN bulk to suppress short-channel effects, having a peak density of $3x10^{16}cm^{-3}$ which decreased exponentially towards the surface as shown in Fig.4.3. Both wafers had a 0.2μm GaN channel region with unintentionally incorporated carbon density of $5x10^{16}cm^{-3}$, but different growth conditions in the lower part of

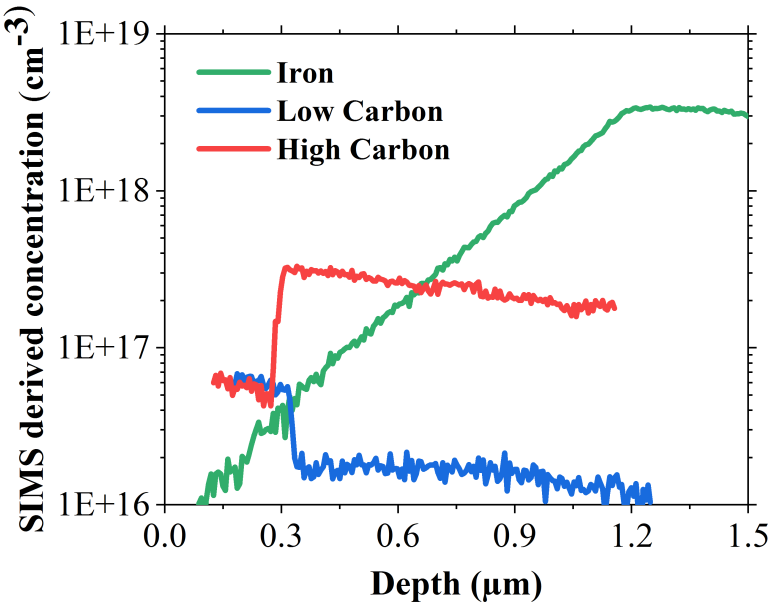

Figure 4.3: Doping density profiles of Fe and C for wafers A and B measured using SIMS.

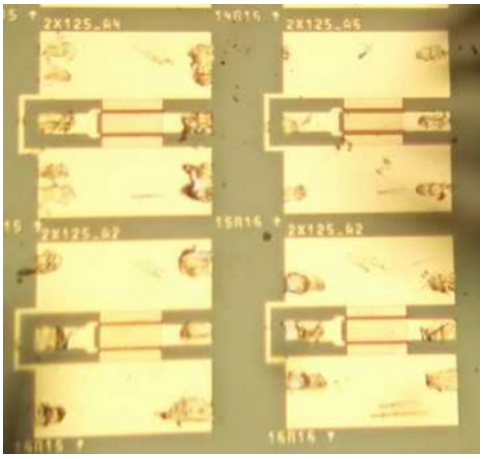

Figure 4.4: Array of 2 finger 2x125 μm AlGaN/GaN HEMT transistor used for this study.

the GaN layer resulted in different carbon profiles. wafer-A had $3\pm1x10^{17}cm^{-3}$ carbon and wafer-B had $2x10^{16}cm^{-3}$ carbon. Oxygen and silicon were below the SIMS background of $5x10^{15}cm^{-3}$.

Both wafers have been processed at BeMitec, supplied by IQE and funded by ESA. AlGaN/GaN HEMTs with a width of 2x125μm, a gate length of 0.25μm, source-drain spacing of 4μm, and source-gate spacing of 1μm were fabricated using Ti/Al/Ni/Au and Ni/Au for Ohmic and Schottky contact respectively, and with identical silicon nitride passivation as shown in Fig.4.4. Repeatability has been demonstrated by processing a further pair of wafers grown with the same conditions, with essentially identical results. Fig.4.5(a), 4.5(b), shows the result of a DC $I_D - V_{DS}$

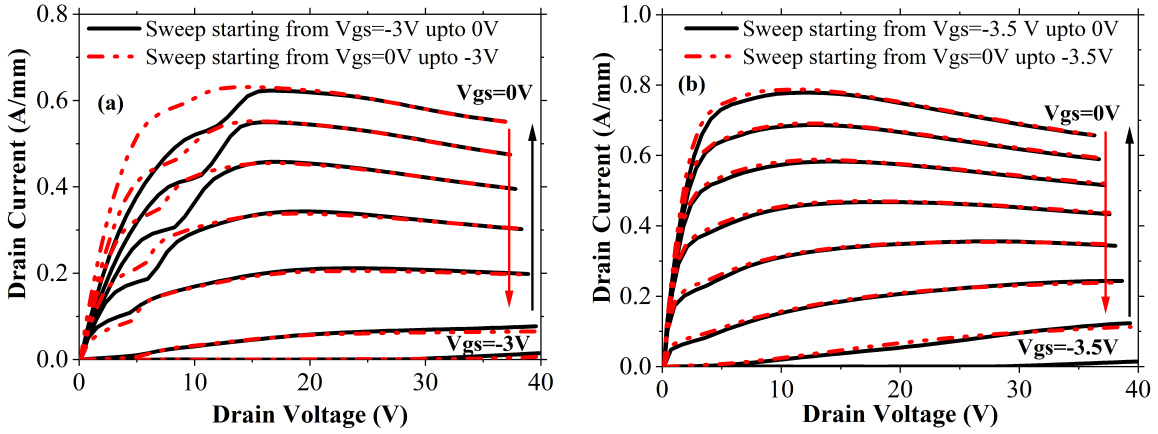

Figure 4.5: DC output characteristics of wafer-A (a) and wafer-B (b) showing the difference between V_{GS} stepping from -3 to 0 V and stepping from 0 to -3.5 V in the steps of 0.5 V. V_{DS} is swept from 0 up to 40 V.

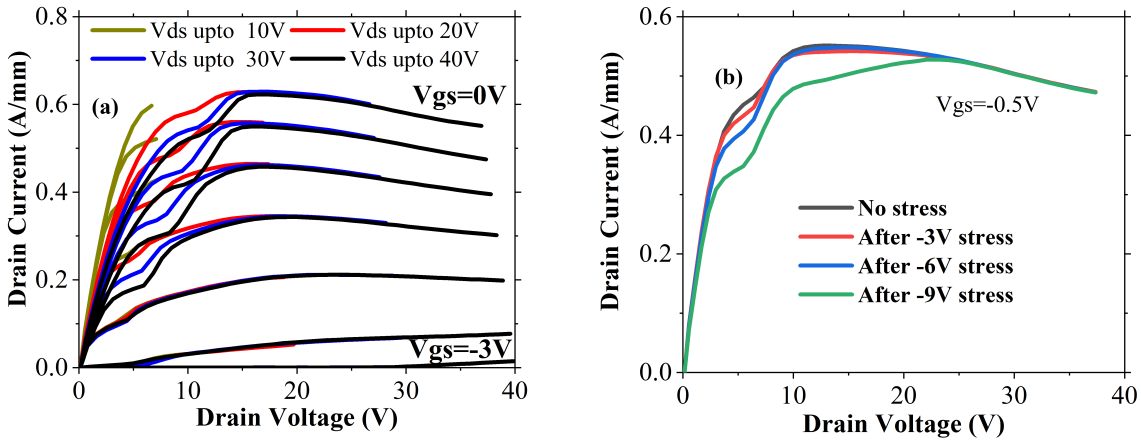

Figure 4.6: (a) DC output characteristics of wafer-A showing the drain bias dependence on kink for different V_{DS} maximum sweep for 10 V, 20 V, 30 V and 40 V. (b) shows the gate bias stress dependence on kink for gate stress ranging from No-stress, -3 V, -6 V and -9 V V_{GS} stress.

measurement at a sweep rate of 1 V/s demonstrating the effect of stepped gate voltage sweep direction. wafer-A showed a strong kink effect, with hysteresis observable at V_{DS} below the kink that is sweep history dependent. It has been reported that the first forward sweep can be kink free [125] however, in this case, a small kink is observable at V_{GS}=0 for wafer-A, with a much lower magnitude than subsequent sweeps Fig.4.5(a). The kink has been seen $\sim 3-5V$ above the knee in all cases and has been found to increase in magnitude with increasing maximum drain bias. As shown in Fig.4.6 (a) different drain bias source for wafer-A varying from V_{DS} =10 V, 20 V, 30 V and 40 V showing an increase in the magnitude of kink with increasing bias. Above the kink, all signs of hysteresis are suppressed. These observations are broadly similar to prior reports [122].

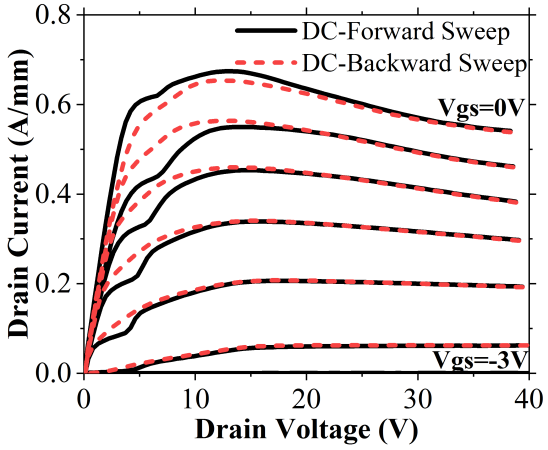

Figure 4.7: V_{DS}= 0 V to 40 V forward DC output characteristics of wafer-A showing kink while reverse DC output characteristics varying from V_{DS}= 40 V to 0 V showing no kink. The V_{GS} sweep direction is from -3 V till 0 V with steps of 0.5V. The V_{GS} is varied from -3 V to 0 V with 0.5 V step size.

Kink is also found to be dependent on OFF-state gate bias stress as shown in Fig.4.6(b). Before every V_{DS} sweep an off state gate stress (at V_{GS}= -3 V, V_{GS}= -6 V and V_{GS}= -9 V) have been applied and the higher the applied off state stress the bigger the magnitude of kink has been observed. The off state V_{GS} stress time has been kept equal to V_{DS} sweep time. This is in contrast to what has been reported earlier [125]. Kink has been also found to be absent if the drain bias is swept in reverse direction as shown in Fig.4.7 where V_{DS} is swept from 40 V to 0 V showing kink free behavior while the forward sweep shows kink.

By contrast, for wafer-B the kink and its associated hysteresis has been found almost entirely suppressed as shown in Fig.4.5(b) and did not show a significant dependence on the maximum drain or gate off-state stress voltage in the sweep as seen in Fig.4.8(a) and (b). Compared with wafer-A, there has been no difference between forward and reverse V_{DS} sweep for wafer-B. During both the sweeps kink has been found absent as shown in Fig.4.9. In all these DC measurements slower sweep ramp rate has been used with the purpose of showing kink clearly since it occurs pronounced at slower ramp rate, as the ramp rate is increased its magnitude reduces but stretches out which relates to associated time constants.

Temperature dependence of kink has also been measured at three different temperature 30°C, 60°C and 120°C for both the wafers as shown in Fig.4.10. Magnitude of kink tends to keep getting smaller with elevated temperatures, at 60°C much smaller kink was observed compared to 30°C and around 120°C it completely disappeared. For wafer-B not much change in magnitude of kink was observed.

To understand associated time constant drain current transients have been performed using a custom developed program (chapter-3, section 3.4). Fig.4.11 shows pulsing from 20 to 4 V V_{DS} which corresponds to the situation kink is observed, and it is then ramped to 20 V then step

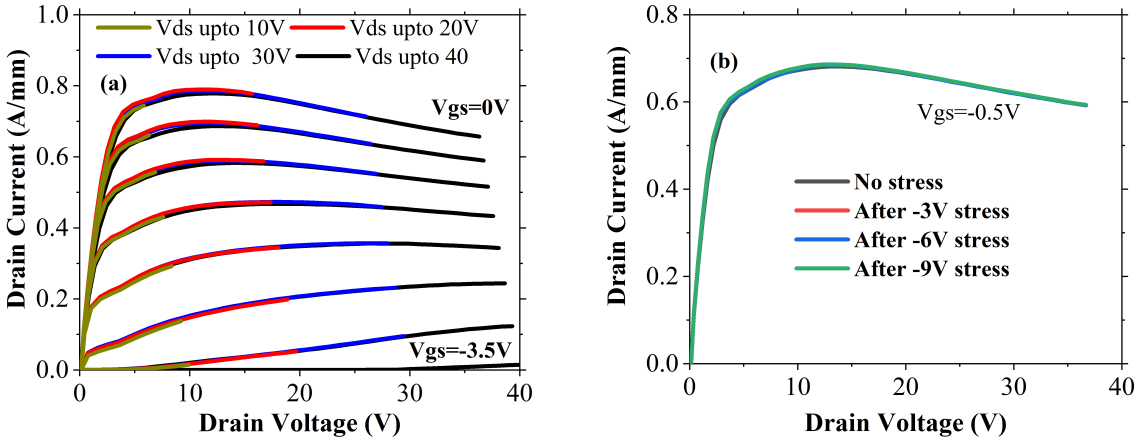

Figure 4.8: (a) DC output characteristics of wafer-B showing the minimum effect of drain bias dependence on kink for different V_{DS} maximum sweep for 10 V, 20 V, 30 V and 40 V. (b) shows almost no gate bias stress dependence for gate stress ranging from No-stress, -3 V, -6 V and -9 V V_{GS}stress on kink.

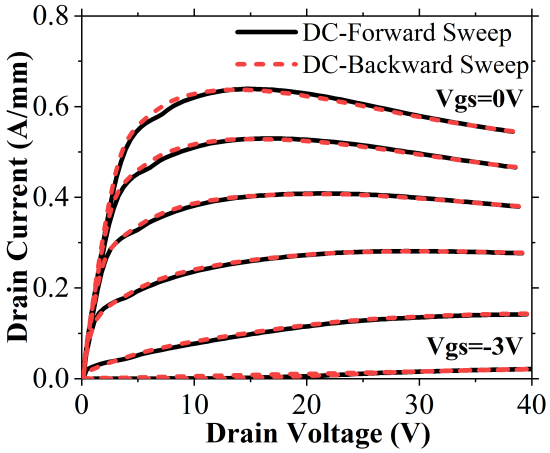

Figure 4.9: V_{DS}= 0 V to 40 V forward DC output characteristics of wafer-B showing no kink while reverse DC output characteristics also remained unchanged with both sweep showing no kink.

back to 0 V. This ramp down is to probe the dynamics after corresponding to the recovery of the IV characteristic below the kink. Drain current transient measurements are a commonly used technique to characterize trap dynamics and has been used extensively in HEMT devices to obtain trap (details of this experiment set up and process has been explained in Chapter-3, section 3.4.).

In this work range of temperatures varying from 25°C to 130°C has used to extract the activation energy as shown in Fig.4.11. A minimum of five temperatures have been used to calculate activation energies as summarized by Bisi et al. [14]. For wafer-B at lower temperature a relatively simple behavior has been observed, displaying a recovery consistent with electron

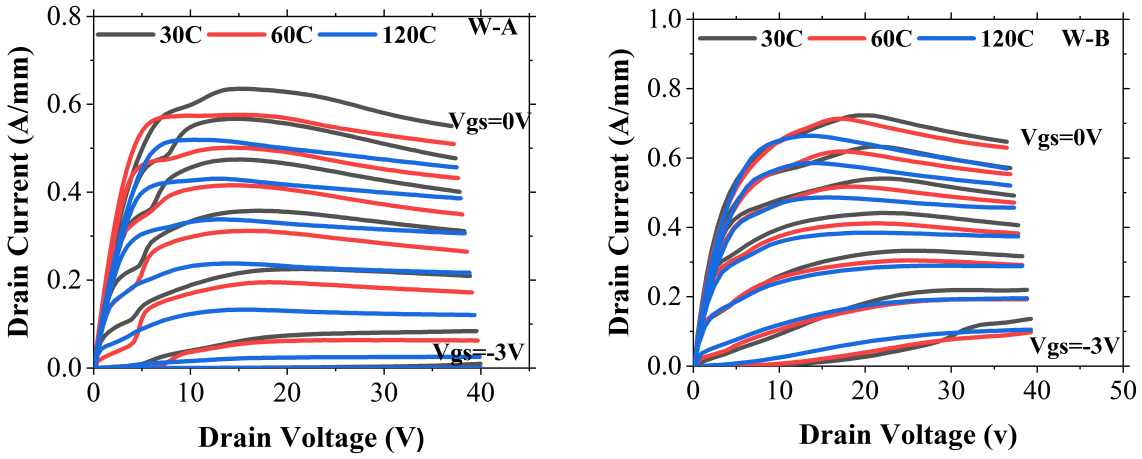

Figure 4.10: DC output characteristics measured for both wafers with V_{DS} varying from 0 V to 40 V and V_{GS} from -3 V to 0 V with steps of 0.5 V for 30°C, 60°C and 120°C.

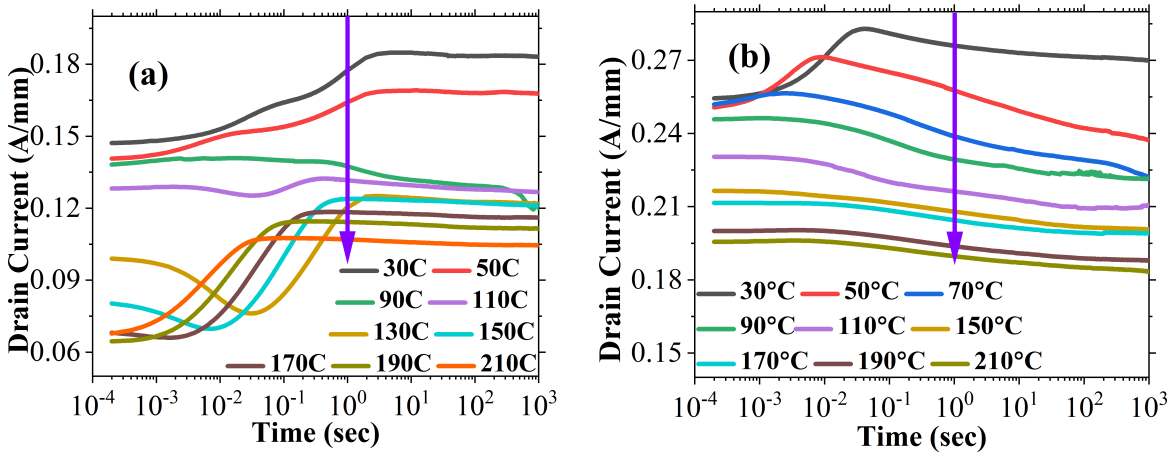

Figure 4.11: Drain current transients measured in the kink region at the indicated temperatures from 30°C to 210°C at $V_{GS} = -1.7V$ and after V_{DS} is stepped from 20 to 4 V for wafer-A (a) and wafer-B (b).

de-trapping with a single time constant (T1) of ~ 10^{-2} at less than 100°C as shown in Fig.4.12. A $\frac{\partial I}{\partial log}$ plot for these temperatures and extracted activation energy of 0.55 eV as shown in Fig.4.13 (a)and (b) has been found comparable with the measured values reported for Fe-doped devices [129], [130]. The behavior is further shown being superimposed on a background of slow drift at higher temperatures. By contrast, wafer-A shows more complex behavior. Below 100°C, wafer-A shows two time constants, one for lower temperature range at ~ 10^{-2} (T1) and second at ~ $1s$ (T2) as shown below in Fig.4.14. A $\frac{\partial I}{\partial log}$ plot for these temperatures are shown in Fig.4.16 (a) with two process T1 and T2. Extracted activation energy of 0.59 eV (similar to wafer-B) has been observed for T1 process while T2 had no temperature dependence. At elevated temperatures >100°C, a

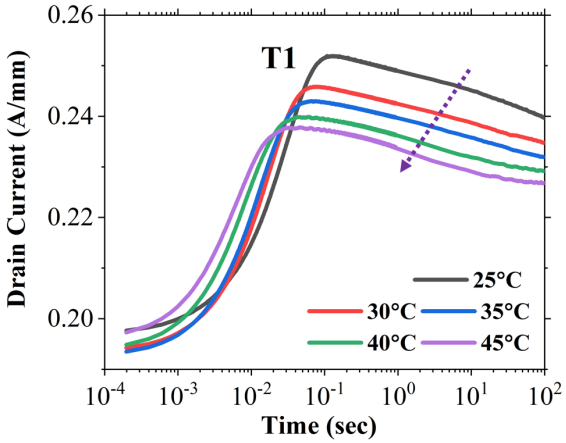

Figure 4.12: Drain current transients measured in the kink region at the indicated temperatures from 25°C to 45°C at $V_{GS} = -1.7V$ and after V_{DS} is stepped from 20 to 4 V showing T1 process for wafer-B.

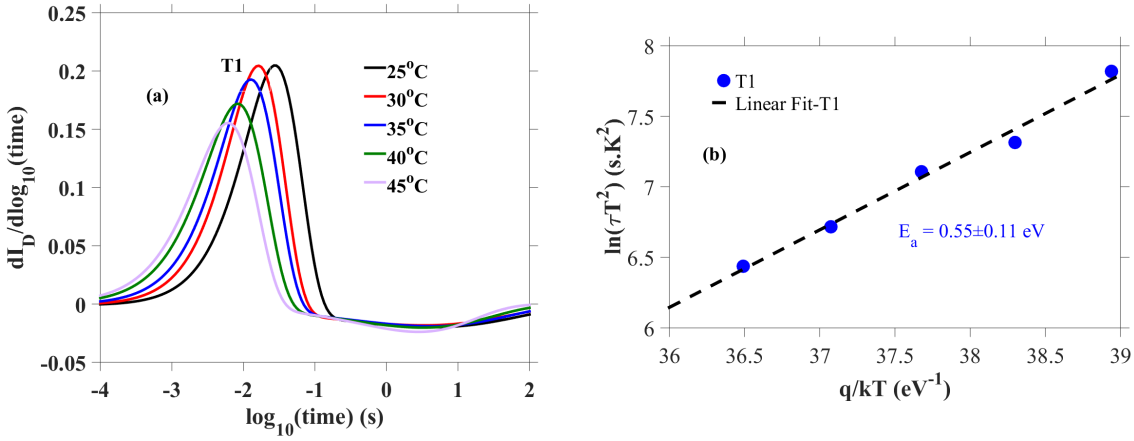

Figure 4.13: Differential extracted from measured transients at low temperature range from 25°C to 45°C at $V_{GS} = -1.7V$ and after V_{DS} is stepped from 20 to 4 V for wafer-B (a) and (b) extracted Arrhenius plot with activation energy of 0.55 eV.

new regime is observed with overlapping positive and negative going transients. As shown in Fig.4.17 is transients varying at temperature from 130°C to 210°C for wafer-A. A $\frac{\partial I}{\partial log}$ plot for these temperatures are shown in Fig.4.17 (a) with two process T3 and T4. The positive going component having an activation energy of roughly ~0.9 eV and the negative going one having a similar value but with larger error Fig.4.18 (b).

At room temperature, it is clear that there is a reasonable consistency between the transient and sweep measurements. wafer-B shows a little kink because its recovery after high drain bias stress is faster than the effective time constant of the voltage sweep, whereas wafer-A longer recovery time makes the kink visible. In both cases for the sweeps, charge trapping occurs rapidly at higher drain bias, which is then neutralized more slowly below the kink.

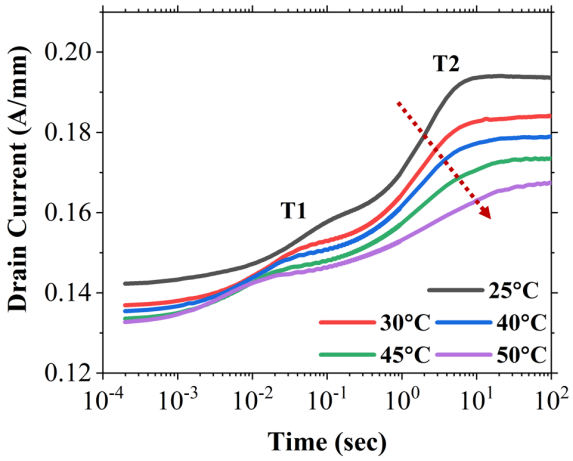

Figure 4.14: Drain current transients measured in the kink region at the indicated temperatures from 25°C to 50°C at $V_{GS} = -1.7V$ and after V_{DS} is stepped from 20 to 4 V for wafer-A.

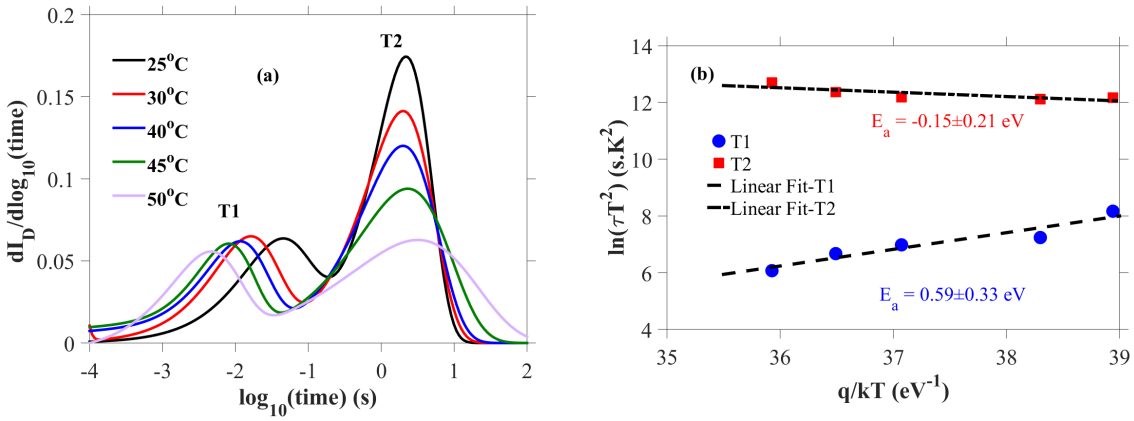

Figure 4.15: Differential extracted from measured transients at low temperature range from 25°C to 50°C showing two different process T1 and T2 for wafer-A (a) and (b) extracted Arrhenius plot with activation energy of 0.59 eV.

In order to determine where within the device the changes in current observed in the drain current transients were occurring, the transient measurements of the distribution of channel resistance were undertaken. The ON-resistance has been taken as $R_{ON} = R_S + R_D$, where R_S and R_D are the access resistances on either side of the gate. Using the gate as a potential probe a small probe voltage of −100mV to +100mV has been applied on the drain (nominal V_{DS} = 0 V), and R_S and R_D were measured within 2s following a stress at 4 or 20 V, as shown in Table 4.1. wafer-A, shows a decrease in R_S and an increase in R_D after stress, whereas for wafer-B increase in R_D and no change in R_S has been observed. The observed difference in R_S and R_D is an important observation and has not been used before in order to interpret the transient measurements. Its also important to note that there is a reduction in R_S, which is normally

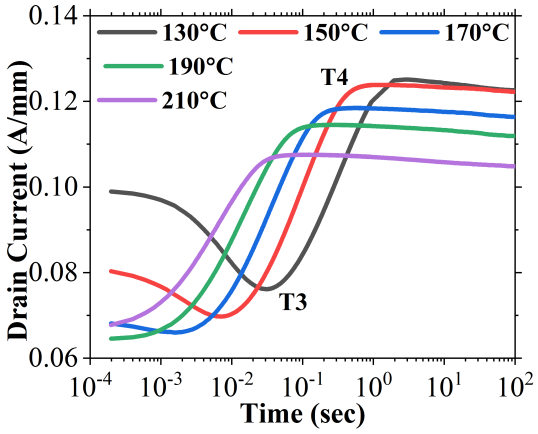

Figure 4.16: Drain current transients measured in the kink region at the indicated temperatures from 130°C to 210°C at $V_{GS} = -1.7V$ and after V_{DS} is stepped from 20 to 4 V for wafer-A.

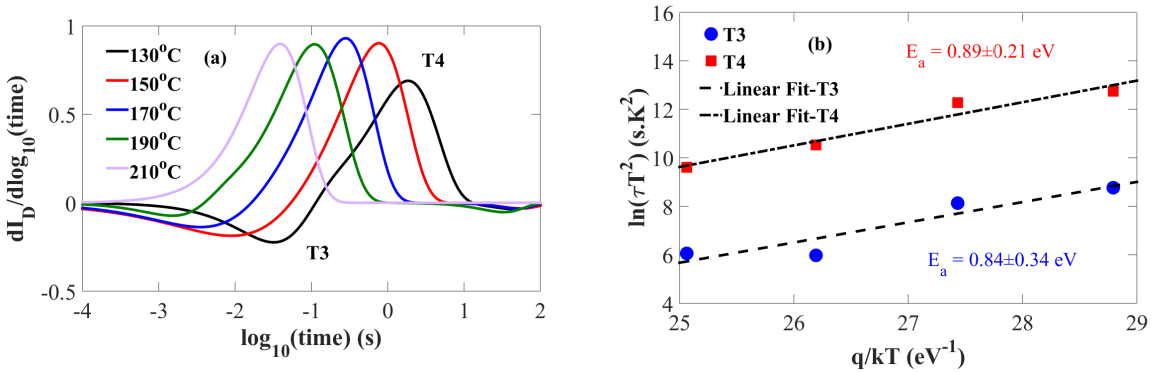

Figure 4.17: Differential extracted from measured transients at high temperature range from 130°C to 210°C showing positive (T4) and negative (T3) process for wafer-A (a) and (b) extracted Arrhenius plot with activation energy of ~ $0.9eV$.

hidden by the larger change in R_D.

		R_S (Ω·mm)	R_D (Ω·mm)
wafer-A	No stress	0.40	2.5
	4V stress	0.36	2.7
	20 V stress	0.28	3.2
wafer-B	No stress	0.33	2.0
	4 V stress	0.33	2.3
	2 0V stress	0.34	3.4

Table 4.1: Summary of source resistance R_S and drain resistance R_D measured for both wafers for no stress and after V_{DS}= 4 V and 20 V stresses.

4.3 Model and Discussion

The GaN buffer in a HEMT is normally doped with a deep level dopant like Fe or C in order to make it semi-insulating. The buffer, in this case, is Fe doped which has an acceptor trap level $0.5-0.7$ eV below the conduction band (C_B) [131] and is normally assumed to be n-type due to Fe pinning of the Fermi level (E_F) in the upper half of the gap as shown in Fig.4.18, preventing the buffer from floating. However, as pointed out in [19], [132] unintentionally incorporated doping (UID) with carbon can convert it to p-type. Carbon on the Nitrogen site (C_N) has an acceptor trap level 0.9 eV above the valence band (V_B) [133] as shown in Fig.4.18. Fe and C_N are both deep acceptors, and in the absence of any external field, the Fermi level will lie near the lowest energy level (C_N), with acceptors above the Fermi level being neutral (Fe). The degree of compensation

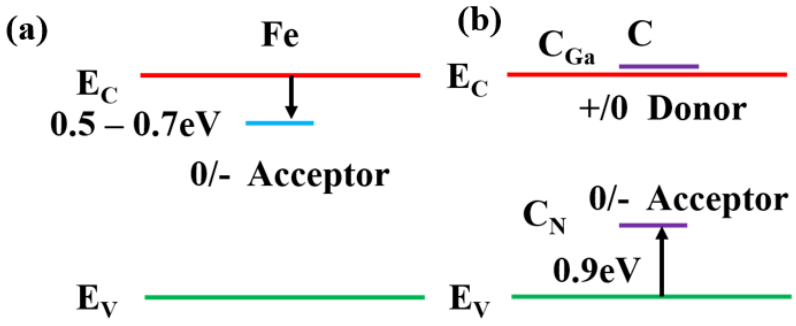

Figure 4.18: Band profiles for Iron (Fe) and Carbon (C) doped in GaN HEMTs.

by donors is critical in determining the N or p-type nature of the GaN but is normally unknown. The Fermi level will switch between close to the Fe trap level and close to the (C_N) level, a shift of ~ 1.8 eV, when the donor density is greater than or less than the (C_N) density respectively. There are several literature reports of related effects. Raman measurements of commercial Fe doped devices fabricated by Cree (CGHV1J006D) suggested that the bulk GaN was indeed p-type [134]. In that case, the SIMS background carbon density was $10^{17} cm^{-3}$ with an unknown donor density which presumably must have been less than that value. Scanning probe measurements in carbon-doped GaN have shown that the material can change from p-type at high C density to n-type at low density [135]. Koller *et al.* [136] measured the built-in voltage in a P-N diode and showed that high C density material is p-type.

The consequence of high carbon doping making the material p-type is that the highly resistive GaN buffer will be isolated from the 2DEG by a P-N junction. Hence the buffer can float and act as a reservoir for time-dependent charge storage. It is argued here that this can be the origin of the kink effect, with the buffer reaching a bias history dependent potential at low bias below the kink and coming into equilibrium with the 2DEG at higher drain bias above the kink as a result of field dependent leakage across the P-N junction.

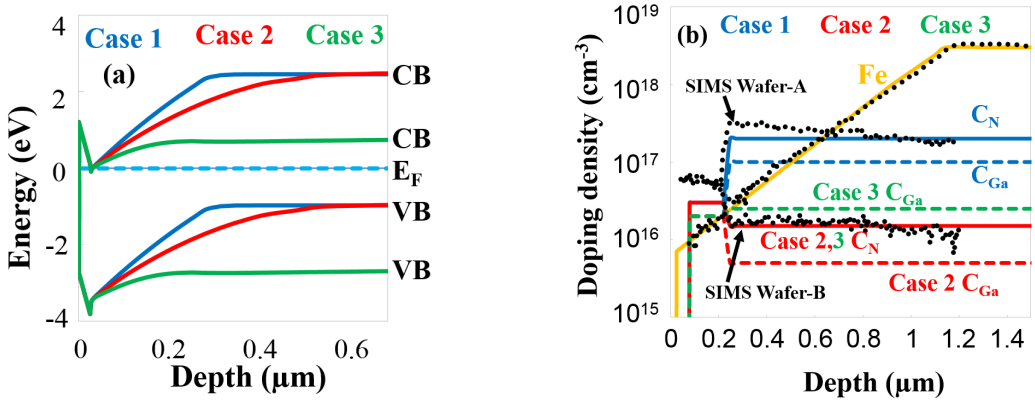

Figure 4.19: (a) Simulated unbiased band profiles on the buffer in this work for a vertical cut line through the gate. (b) Doping density profiles as in Table 4.2 with overlaid measured SIMS profiles of Fe and C for similar wafers to A and B (shown in black dotted line)

To understand the effect of UID carbon on the HEMT, a Fe doped GaN device with L_{SD}= 3.75 μm and L_G= 0.25 μm has been simulated with Silvaco Atlas for a wide range of compensation ratio and donor densities [137]. Three illustrative GaN buffer doping combinations are shown in Table 4.2 and the resulting band diagrams and doping profiles are shown in Fig.4.19 (a) and (b). Case 1 corresponds to wafer-A with $3x10^{17}cm^{-3}$ carbon, where the compensation ratio of carbon on the Ga (donor) and N (acceptor) sites, C_{Ga}/C_N, has been set at 0.5 consistent with what is inferred for power devices and making the layer p-type [67], [138]. Case 2 and 3 correspond to the carbon profile of wafer-B with $1.5x10^{16}cm^{-3}C_N$ and two assumptions for the unknown intrinsic donor density. Case 2 corresponds to a low donor density of $5x10^{15}cm^{-3}$ and hence the layer is dominated by the C_N and is also p-type, whereas Case 3 has a higher donor density of $2.5x10^{16}cm^{-3}$ which exceeds the C_N density and hence is n-type. In all cases the 0.2 μm thick channel region was fully depleted and doped with $3x10^{16}$ C_N and $2x10^{16}cm^{-3}$ C_{Ga} making it semi-insulating (lightly p-type). No doping was incorporated in the 5 nm below the 2DEG to improve simulator convergence.The capture cross-section for Fe has been set to $10^{-13}cm^2$, a high value since Fe can capture via its excited states [132], [139] and C_N to $10^{-15}cm^2$.

	Case-I (wafer-A)	Case-II (wafer-B)	Case-III (wafer-B)
Fe acceptor (E_c-0.7 eV)(cm^{-3})	7x10^{15} at 2DEG increasing exponentially with depth to 3x10^{18} at 1.1μm		
C_N acceptor (E_V+0.9 eV)(cm^{-3})	2x10^{17}	1.5x10^{16}	1.5x10^{16}
C_{Ga} and intrinsic donors (E_C-0.03 eV)(cm^{-3})	1x10^{17}	0.5x10^{16}	2.5x10^{16}

Table 4.2: GaN Buffer profiles used in this work for simulation.

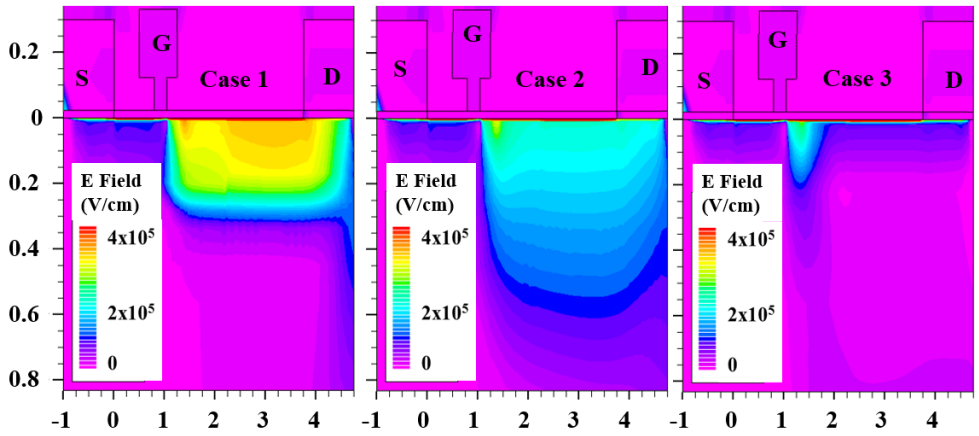

Figure 4.20: Vertical electrical field profile for the buffers of Table 4.2 at V_{DS}= 10 V and V_{GS}= 0 V. Cases 1 and 2, where the buffer is p-type, show a field of as much as 4x10^5 V/cm over the entire gate to drain gap, while for the n-type buffer of case 3, the low field is predicted except at the gate edge.

A key issue in the simulation of these devices is the requirement to include leakage paths through the reverse-biased depletion regions below the 2DEG. It is known from GaN LEDs and vertical PIN diodes that the reverse bias leakage occurs by a trap-assisted band-to-band hopping process associated with threading dislocations [140], [141], which occurs at a low field far below that which is required for impact ionization. In GaN-on-Si devices [136], it has been shown by substrate ramps that there is a leakage through the UID GaN layer from the 2DEG to the p-type GaN:C buffer for the field polarity corresponding to positive drain bias [142]. Sufficient leakage to positively charge the buffer occurred in a few seconds for a field as low as $2x10^5$ V/cm at room temperature. Hence it is reasonable to expect a hole current to flow into the buffer as soon as the field in the channel exceeds a few times 10^5 V/cm. Fig.4.20 shows the simulated vertical electrical field at $V_{DS} = 10V$. Case 3 which is n-type shows low field since there is no significant voltage drop between the 2DEG and the buffer. However, cases 1 and 2, where the buffer is p-type, show a field of as much as $4x10^5$ V/cm over the entire gate to drain gap suggesting that this does indeed provide a plausible explanation for hole leakage into the buffer at a bias consistent with the bias where a kink is observed. There is no built-in model for leakage in a reverse biased GaN P-N junction in the simulator, and hence a simple approximation which has been used successfully to simulate current-collapse in GaN power devices has been employed [67]. This uses a P++ shorting region located under the source and drain contacts, which provides a path for holes to flow into the semi-insulating buffer. It is well established that such leakage paths are often present under ohmic contacts [143]. This simulation approach requires holes to flow from the P++ region at the drain to the gate region in order to impact the threshold voltage and thus results in unrealistically long time-constants at room temperature. Nevertheless, it does allow

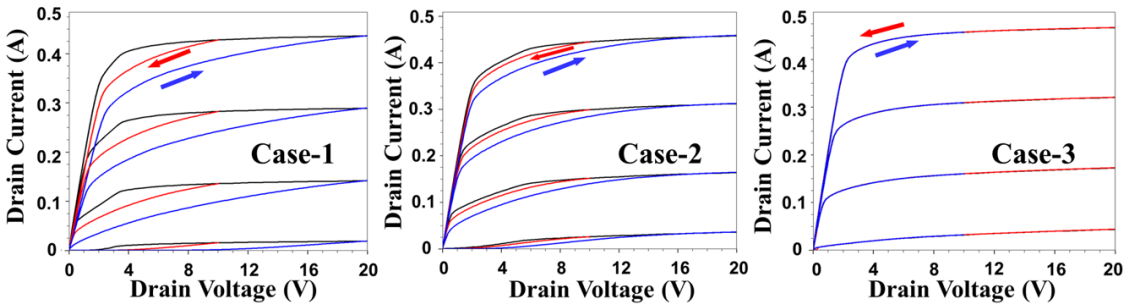

Figure 4.21: Overlaid simulated output characteristics for the buffers of Table 4.2 with V_{GS}= 0 to -2 V in 0.5 V steps. Black line: static (equilibrium) sweep. Blue line: static bias of V_{DS}= 20 V, immediately followed by 10 V/s up-sweep from 0 to 20 V. Red line: static bias of 10 V followed by a 10 V/s down-sweep to 0 V.

the buffer potential to be sensitive to the drain bias, gives an indication of how buffer potential can affect the channel current by a back-gating mechanism and seems to capture the behavior for T>100°C as discussed later.

A simulation of the slow sweep leading to hysteresis is shown in Fig.4.21, where a static IV characteristic is compared with two types of 10 V/s sweep. The assumption here is that leakage into the buffer will occur at $V_{DS} \geq 10V$ allowing the buffer to come into quasi-equilibrium with the drain bias during a slow sweep at all biases above 10 V. Hence a sweep at 10 V/s from the static case at $V_{DS} = 10V$ down to 0 V corresponds to the backwards-sweep shown in Fig.4.5(a). The forward-sweep of Fig.4.5 (a) is simulated by starting with a static simulation at $V_{DS} = 20V$ followed by a step to 0 V in 10 ns, followed by a slow sweep at 10 V/s up to 20 V. The simulation captures the hysteresis in I_D below the kink associated with the charge stored at high drain bias. However, it will not capture the kink itself which would be caused by the onset of leakage between the 2DEG and the buffer, effectively pinning its potential to that in the 2DEG. For the n-type buffer (Case 3), no deviation from the static sweep is observed for the 10 V/s sweeps, whereas for the p-type buffers of Cases 1 and 2 there is a significant hysteresis (reduction) in current apparent in the knee region for the forward-sweep compared to the backward-sweep case. For Case 1, the static sweep exceeds both forward and backward-sweeps. These simulations clearly show how a kink could arise if a non-Ohmic leakage path were present. Charge distributions stored in the buffer cannot change easily at low bias if the buffer is floating but will be able to come into equilibrium at a few volts above the knee once hole charge can flow into the buffer.

To understand more clearly the origin of the complex transient behavior seen in Fig.4.11, drain current transients in the kink region have been simulated for a bias step from 0 V to 4 V (corresponding to initial sweep) and for 20 V to 4 V (subsequent sweep) as shown in Fig.4.22. For the three cases considered here, on step-down Fig.4.22 (a) there is a recovery apparent at

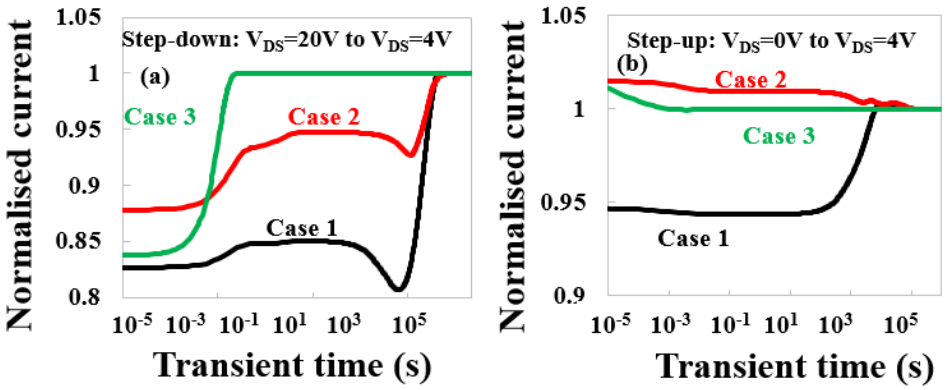

Figure 4.22: Normalized drain current transients for the buffers of Table 4.2(a) following step-down from V_{DS}= 20 to 4 V and (b) step-up from V_{DS}= 0 to 4 V, with V_{GS}= -1.5 V in all cases.

~ 10 ms corresponding to neutralization of charge stored in ionized Fe acceptors under the gate, a time scale too short to be observed in the slow sweep simulations of Fig.4.21. This Fe-related response arises even for the p-type Cases 1 and 2 since the Fermi energy must always cross the Fe trap level within the channel depletion layer. This is followed by negative and positive magnitude long time constant processes for Cases 1 and 2, as can also be observed for >100°C in the current transient measurement for wafer-A (see Fig.4.11(a)). A conventional interpretation of such negative and positive drain current transients would ascribe them to electron and hole traps respectively [112]. However, this cannot be the case in the simulation since the donors are always ionized and only changes in occupation of the C_N acceptor occurs. Another important observation to understand is an "acceptor" and a "donor" response at 0.9 eV also shows similar apparent capture cross-section of $4.6x10^{-16}$ and $1.7x10^{-16}cm^2$ extracted by extrapolation to the y-axis in the Arrhenius plot. These capture cross sections need to be taken carefully because that relies on the assumption of a 1D model with a low resistance ohmic contact to the edge of a depletion region. In present structure there is a semi-insulating buffer and a 2D transport path to the depletion region, and in the regime where the activation energy are extracted, it is shown that the transport is mostly limited by activation within the ohmic region of the buffer and not by activation within the depletion region. This is why two different time constants for the same trap [144] can be distinguished, which would conventionally be interpreted as having two cross-sections.

For Case 3 there is no barrier preventing electrons from flowing into the n-type buffer and hence no additional transients are observed on step-down. Fig.4.11a is representative of the case I where the bulk of the buffer is p-type. There is a small contribution from ionized Fe located near the 2DEG at ~ 10ms which is present for step-down (V_{DS} switched from 20 V to V_{DS}= 4 V), and

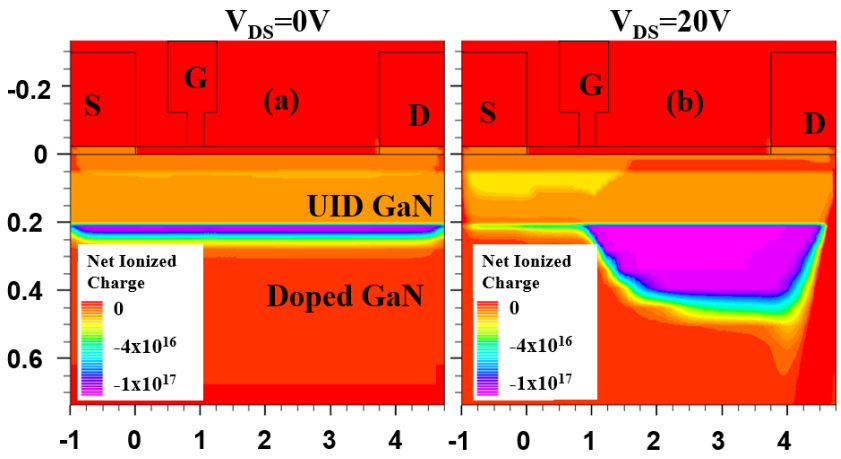

Figure 4.23: Simulated net ionized charge densities for Case 1 with a different bias, (a) V_{GS}= 0 V and V_{DS} = 0 V. (b) V_{GS} = 0 V and V_{DS}= 20 V.

which arises because the Fermi energy must always cross-the Fe trap level within the surface depletion layer. The time constants in Fig.4.11a and Fig.4.21a are similar at room temperature for this contribution since the transport path from the 2DEG to the trap is exactly the same in the real device and in the simulation ie vertical.

Net ionized charge density for Case 1 with and without drain bias are shown in Fig.4.23 to help explain the mechanism of positive and negative magnitude contributions seen in Figs.4.11(a) and 4.22(a). Fig.4.23(a) for $V_{DS} = 0V$ shows that the depletion charge of ionized C_N is constant from source to drain except in the vicinity of the P++ shorting regions at the outer edges of the contacts. However, for positive drain bias, a small hole current starts to flow through the highly resistive buffer, forward biasing the depletion region in the source-gate gap and reverse biasing the depletion region in the gate-drain gap as can be seen for Fig.4.23(b). This reduces the negative charge below the channel near the source and increases it near the drain, so R_S is reduced, and R_D increased. This is exactly what has been measured for wafer-A as shown in Table4.2. The reduction in R_S is excellent supporting evidence for the attribution of wafer-A as p-type with a high C_N density. The absence of any change in R_S in wafer-B is consistent with its low C_N density. There is insufficient depletion charge to cause a significant change in R_S. Fig.4.24 shows the ionized charge for case 3 with (b) and without drain bias (a). When unbiased, there is a depletion region of constant width which extends from source to drain just like case-1 and 2. GaN Buffer, in this case, is Fe doped and hence n-type. Since there is a resistive contact between the GaN buffer and the 2DEG which means under the bias, there is no significant voltage drop between the 2DEG and the buffer in the gate-drain gap and only a relatively small geometrically defined negatively charged region of ionized Fe acceptors located under the gate edge can be seen in Fig4.24 (b). This stored charge distribution only results in an increase in R_D and no change in

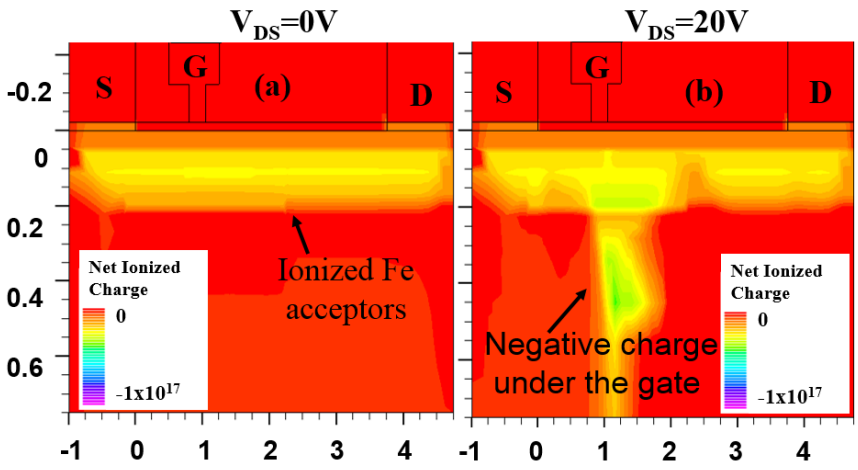

Figure 4.24: Simulated net ionized charge densities for Case 3 with a different bias, (a) V_{GS}= 0 V and V_{DS} = 0 V. (b) V_{GS} = 0 V and V_{DS}= 20 V.

R_S, as has also seen for wafer-B in Table.4.1.

Further confirmation of no significant voltage drop between the 2DEG and the buffer in the gate-drain gap under bias for case 3 can be seen in Fig.4.25. For case 1 holes flow through the semi-insulating buffer producing a resistive potential divider between drain and source which back biases the 2DEG between drain and gate and produces a negatively charged depletion region of ionized C_N as seen before in Fig.4.23(b). This all suggests that the positive and negative magnitude buffer time constants seen in Fig.4.11(a) and simulated in Fig.4.22(a) are all due to the same C_N acceptors but located in different parts of the device. The positive going transient is associated with relaxation of negatively charged C_N acceptors located under the gate, whereas

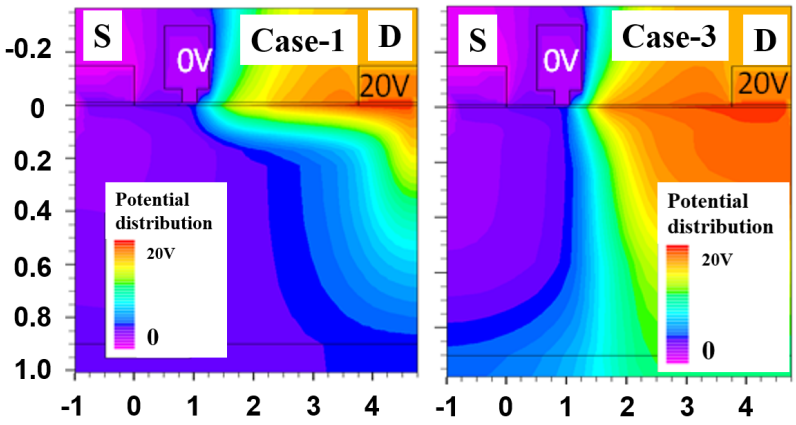

Figure 4.25: Potential distributions for Case 1 and 3 at V_{DS}= 20 V.

the negative component is due to ionization of neutral C_N acceptors in the source-gate depletion region. (There will also be a relaxation of charged acceptors in the gate-drain gap, however, this will have little impact on I_D above the knee since the device is saturated at $V_{DS} = 4V$.) Clearly, the real situation for wafer-A in Fig.4.11(a) is more complex, however above 100°C it is consistent with the simulation, with GaN transport dominated by bulk resistive conduction via holes thermally activated to the V_B, thus explaining the observed 0.9 eV activation energy. It is shown that two time constants (and hence apparent capture cross-sections) from the same trap has previously been observed in related measurements and simulations for a p-type floating buffer [144], although in that case, both contributions had the same sign. Below 100°C, the GaN buffer is more resistive and the behavior would be consistent with the hopping transport between the 2DEG and acceptors dominating, perhaps explaining the widely observed 0.5-0.6 eV activation energy [129], [112], [145].

There have been conflicting reports on the occurrence of the kink on the initial forward sweep [123], [125]. Fig.4.22(b) shows how this can arise depending on the background carbon concentration. It shows the change in current as V_{DS} is stepped from 0 V to $V_{DS} = 4V$ and corresponds to the first sweep from unbiased equilibrium to a bias below the kink but above the knee and hence in saturation. The high C_N density Case 1 shows a normalized increase in current of 6% mostly associated with a reduction in R_S. A reduction in R_S in saturation will reduce the voltage drop between source and gate and hence effectively result in a shift in gate bias in the intrinsic transistor which increases the current. This can be seen with a 17% increase in current when stepping from 20 V to 4 V Fig.4.22(a) where the reduction in resistance under the gate exceeds the effect of the increase in R_S.

By contrast, the low carbon density Case 2 shows minimal change for initial step-up (Fig.4.22(b)). This is because there is a correspondingly lower source region depletion charge and so there is an insignificant effect on R_S and hence would show no kink. wafer-A, which has the high carbon density, shows a small kink on the initial sweep in Fig.4.4(a), consistent with this prediction. wafer-B shows minimal kink and is consistent with an n-type buffer meaning that there is a background concentration of donors greater than $2x10^{16}cm^{-3}$ whose origin is not known. As shown in Fig.4.6(b) it is observed that the drain voltage for the kink is gate bias dependent. This can be explained using the model since the drain voltage for the kink will be a function of the electric field distribution and that will be linked to the gate bias. However, in order to quantify that dependence, one would need to have a measure of the non-linear conduction of the leakage path between the 2DEG and the buffer. At present state, that information isn't available and this could be an extension of this work.

4.4 Conclusion

Kink effect in Fe doped devices, a hysteresis in drain current in the knee region of GaN HEMTs, is explained using a floating buffer model. To observe kink and hysteresis, two effects must be present: the presence of a background substitutional carbon impurity which makes the bulk of the GaN buffer p-type, and band-to-band trap-assisted-leakage of holes from the 2DEG into the buffer at moderate electric fields. Both these requirements are likely to be met in Fe doped MOCVD epitaxy explaining its relatively frequent observation. It is shown that kink is also often observed in carbon-doped power devices as a result of essentially the same mechanism. The magnitude of the kink and its precise time dependence is strongly dependent on the carbon concentration and its degree of self-compensation, the density of background donors, and the exact band-to-band leakage path, helping to explain why even apparently identically grown epitaxy can result in different kink behavior. Depending on the carbon density, a kink can be either present or suppressed during the initial sweep providing an explanation for the reported difference in behavior in the literature [123], [125]. Suppression of the kink effect would require a detailed control of native defects and unintentional dopant's as well as parasitic leakage paths and will constitute a challenge for the community.

It is shown that floating p-type buffers can result in transient behavior which is dependent on the transport path to the trap state rather than just the trap properties themselves. This results in positive and negative sign transients from the same trap, having the same activation energy but located in different parts of the device. Conventionally this would be interpreted as a "electron" and an "hole" trap having different capture cross-section. This calls into question some simplistic interpretations of drain current transient spectroscopy based on classical DLTS which assume the availability of a bath of majority carriers.

CHAPTER 5

EVALUATION OF PULSE I-V AS THE BASIS FOR NON-LINEAR MODELS FOR GAN-BASED HFETS

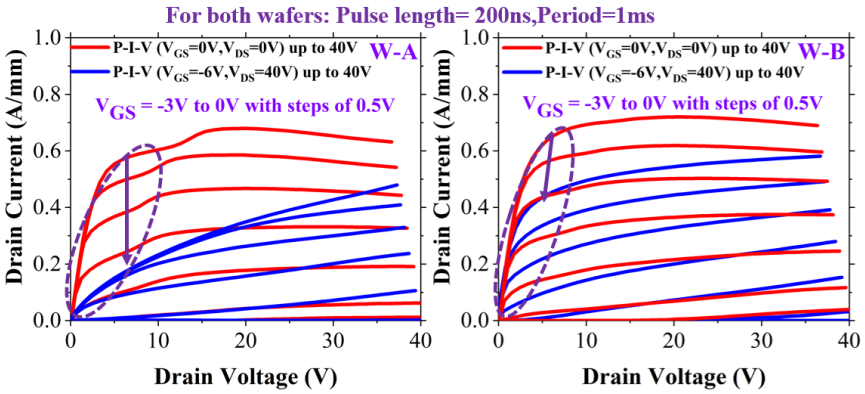

Figure 5.1: Difference in knee walkout observed during pulse output characteristics with 200 ns pulse length and 1ms pulse period of 2x125 μm device on two identical structure (with only differences in buffer doping), red represents steady state (V_{GSQ} = 0 V and V_{DSQ} = 0 V) and blue shows impact of gate-drain stress (V_{GSQ} = -6 V and V_{DSQ}= 40 V). Wafer-A shows much larger knee walkout compared to wafer-B.

In previous chapter two identical layer structure wafers with the only difference in buffer doping were studied using DC I-V and transients supported by simulations to explain "kink" effect. This chapter evaluates the same two wafers and examines the applicability of pulsed I-V measurements (Pulse I-V) as a tool for accurately extracting non-linear GaN-based HFET models. A series of I-V measurements were performed under DC and pulsed conditions demonstrating a dramatic difference in current collapse (knee walkout) as shown above in Fig.5.1

suggesting different trapping behavior in both wafers. This difference would suggest that they would show different RF performance, however when RF I-V waveform measurements at 1GHz, utilizing active harmonic load-pull, were used to study the impact of these traps on RF performance, both wafers gave good overall RF performance with no significant difference observed. This absence of correlation between Pulse I-V measurement results and RF performance raises a question about the applicability of Pulse I-V measurements alone as a tool for extracting non-linear device models in the case of GaN HFETs. This chapter has significant content reproduced from my co-author published work [146], with permission from IEEE. Same samples as used in the previous chapter has been used here. RF measurements and its understanding were contributed by the team from Cardiff university. Most of the measurements reported are performed by me and the ones not are mentioned specifically in each case. All figures have been reproduced with permission from IEEE.

5.1 Introduction

Due to the unique material properties of GaN, particularly high electron mobility, high breakdown field strength and high thermal conductivity, GaN-based transistors have found increasing market penetration in the field of radio frequency (RF) systems. However, despite recent improvements in the growth and fabrication process for the successful realization of high-performance devices, the lack of a complete understanding of the measured shortfall in the performance of GaN-based HFETs still stands as an obstacle to full utilization of these devices in commercial applications. One of the main issues affecting the reliability and dynamic performance is the presence and impact of charge trapping [147]. A full understanding of the many trapping phenomena and their effect on the electrical performance of GaN devices remains a major challenge. It has been observed that the trapping processes can induce a so-called "current collapse", a recoverable decrease in the drain current when operated with large gate-drain voltage swings [148]. Binari *et al.* [149] suggested that the compromised microwave power performance and the current collapse of the DC and pulse device characteristics are related to the presence of traps at the surface and in the GaN buffer layer. Several established models [150][151] have been used to describe the nonlinear behavior of HFETs and MESFET devices. However, these models generally do not consider the trapping effect on the RF performance. For the experimental investigations of the traps the pulsed I-V measurement method (Pulse I-V) is widely utilized and is often used to extract modified device models that aim to take into consideration the charge trapping effects when predicting the transistor's RF behavior [152][153][154][155][156][157]. Initially applied to GaAs based devices, the application of these modeling concepts has now become a major focus in the development of nonlinear large-signal RF GaN HFET models. In recent years, many empirical and compact physical models have been reported, aimed at predicting the performance of the GaN HFET devices [158][159][160][161][162][163][164][165][166][167]. Most of these models again

rely on Pulse I-V measurements as a model extraction and validation tool when including the trapping effects. For instance, Tarazi *et al.* [166][167] suggested that a trap model is crucial to fit DC I-V characteristics and accurately predict large signal performance of GaN HFET devices. They used Pulse I-V measurements to acquire the fitting parameters of the trap controlling voltage in the modified nonlinear device model. In another work Huang *et al.* [165] proposed a new 13-element drain current source model validated by measured Pulse I-V data with various quiescent biases and power dissipation.

This work investigates the impact of traps in AlGaN/GaN HFETs with and without "kink effect" [123][125] and having differing "knee walkout" in Pulse I-V measurements as shown in Fig. 5.1 (as explained in the previous chapter "kink effect" is a hysteresis very commonly observed in the knee region but which is normally assumed to have no impact on RF performance). An RF I-V Waveform measurement system, utilizing active harmonic Load-Pull is also used to investigate the impact of these traps under RF conditions (RF I-V). A comparative analysis of the behavior and impact of the traps under Pulse I-V and RF is reported. It is found that the measured "kink-effect" in DC I-V, and "knee-walkout" in Pulse I-V, does not necessarily provide a valid prediction of the "knee walkout" observed under RF excitation.

5.2 Sample details and measurements

Two AlGaN/GaN epi-layers were grown by metal organic chemical vapor deposition (MOCVD) on 4-inch silicon carbide wafers used in previous chapter to investigate "kink" effect has been used for this study. Wafer-A exhibited significant "kink" in the knee region while wafer-B showed almost no kink under DC conditions. 2x125 μm device has been used for this study with a source-drain spacing of 4 μm and a gate length of 0.25 μm. Details on the epitaxy, drain current transient measurements, and on the kink effect mechanism has already been discussed in the previous chapter. A series of I-V measurements were performed under DC and pulsed conditions to study the carrier trapping and their effect on current collapse (knee walkout) and the kink effect. A Keithley source measurement system was used for DC measurements and current transients were performed using custom built TSB software controlling multiple SMU, while a dynamic pulsed current-voltage analysis system (AU4850) was used for Pulse I-V measurements.

In the case of Pulse I-V measurement, a conventional simultaneous pulse (gate and drain lag) setup was adopted with soft switching. The device was held at a quiescent bias point and the drain current versus the drain voltage curves were measured with pulse length of 200 ns and pulse period of 1ms as shown in Fig.5.2. The same V_{GS} sweep direction for all Pulse I-V measurements has been have in order to maintain the consistency. Advanced double pulse approaches to measure the impact of trapping [25] could have been used but would only have accentuated the differences observed between the wafers. As shown in Fig.5.3 set of four quiescent bias points were used for this investigation each with defined purpose mentioned below as follows:

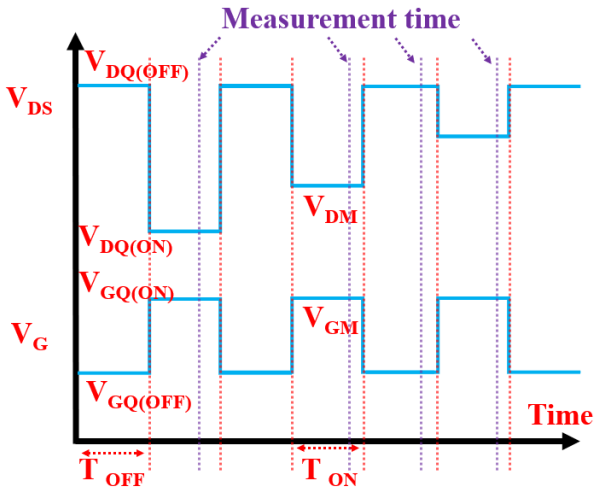

Figure 5.2: Schematic of pulse waveform used for Pulse I-V measurements is shown, for all the study in this chapter 200 ns pulse length and 1ms pulse period is used, the longer duration pulse period ensures that the device reaches steady-state quiescent condition.

- V_{GSQ}= 0 V, V_{DSQ}= 0 V steady state designed to minimize self heating and trapping;
- V_{GSQ}= -6 V, V_{DSQ}= 0 V designed to highlight trapping under the gate region (gate-lag effect;
- V_{GSQ}= -6 V, V_{DSQ}= 40 V designed to highlight trapping under the gate-drain region (drain-lag effect), with no self-heating;
- V_{GSQ}= -1.7 V, V_{DSQ}= 10 V to 28 V designed to highlight trapping under class B operation (emulation of saturated RF performance).

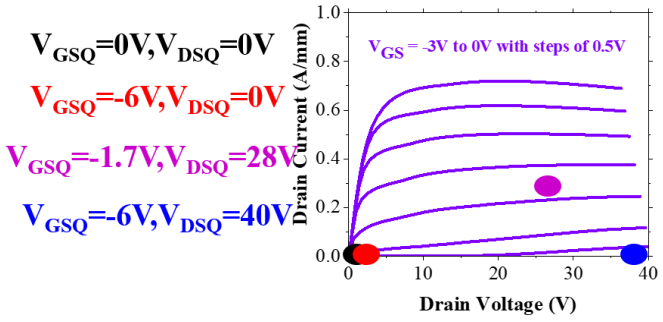

Figure 5.3: Different quiescent point represented over I-V plane of a transistor output characteristics.

Along with output, the transfer characteristics were also obtained based on the same above-mentioned pulse stress conditions at V_{DS}= 1 V with V_{GS} sweep from -6 V to = +1 V to gain insight

into V_{th} shift or change in transconductance upon different stress. A set of different pulse length variation from 200 ns, 500 ns and 1μs has also been performed to understand self-heating and its associated trap time constants. To gain insight into de-trapping time constant current transients were performed using TSB setup. At same quiescent bias points mentioned above these devices were stressed for 1000 seconds followed by immediate change over to ON state at V_{GS}= 0 V and V_{DS}= 1 V with recovery monitored over 1000 seconds.

A large signal RF I-V Waveform Engineering system architecture based on a VTD SWAP-X402 receiver that was developed at Cardiff University [168][169] has been used for the RF analysis in this work. An integrated external modulator with high-speed RF switches (1 GHz) has been used to provide the RF pulsing unit and a high-speed FET switch is used to modulate the drain under DC when needed. The ability to independently switch the RF and DC drain bias between pulse and CW without making any changes to the sampling regime delivers comparability between different measurement conditions; therefore, any measured changes can safely be ascribed to the device under test. In this study, the devices are analyzed under class B operational mode that delivers high power added efficiency (PAE). A resistive load is applied at the fundamental frequency with a short circuit at higher harmonics. The quiescent bias current is initially set to a low level, which rises as the RF drive is increased. The result is a nominally sinusoidal RF drain voltage, V_{DS}(t), waveform and a half wave rectified RF drain current, id(t), waveform that flows primarily when the voltage is at a minimum resulting in improved efficiency. These RF I-V waveforms were measured over a range of fundamental load impedance and at five different DC drain bias points (10 V, 15 V, 20 V, 25 V and 28 V) for 5 different devices on each wafer.

It is important to note that no irreversible degradation was observed in any of the measurements or as a result of bias conditions applied during the experiments. Hence the differences in buffer doping did not lead to degradation as has been observed previously [170].

5.3 Result and Discussion

5.3.1 Pulse I-V measurements (Pulse I-V)

The presence of trapping can be identified from the analysis of the DC and pulsed I-V characteristics, starting from several quiescent bias points. Fig.5.4 shows the output characteristics of both wafers under DC and Pulse I-V measurements at static condition (V_{GSQ}= 0 V, V_{DSQ}= 0 V). It can be noticed that there was a fall in the DC I-V curves at high I_D, V_{DS} for both wafers. This drop in the drain current is not trap related but can be associated with thermal effects since they are absent in Pulse I-V. As already noted, wafer-A showed significant kink especially during the DC sweep with wafer-B showing only a small kink.

1. ***Pulse I-V fast trapping at high drain bias:*** For wafer-A, the Pulse I-V measurements showed an increase in ON-resistance from 4 Ω·mm to 6.25 Ω·mm when pulsed from (V_{GSQ}=

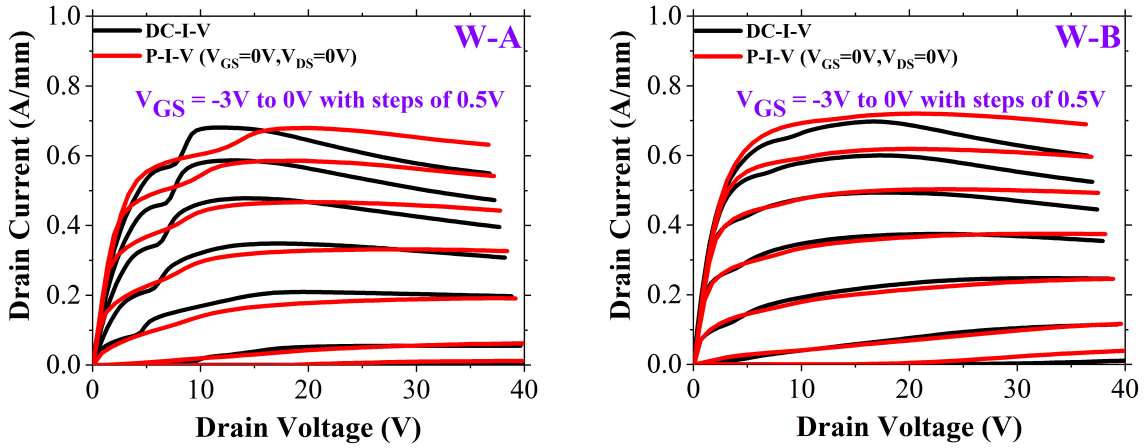

Figure 5.4: DC and Pulse Output characteristics of 2 x 125 μm device during DC I-V sweep (black) and Pulse I-V with steady state condition of V_{GSQ}= 0 V, V_{DSQ}= 0 V (red), with 200 ns pulse length and 1ms pulse period. For both case V_{GS} vary from -3 V up to 0 V in steps of 0.5 V while V_{DS} vary from 0 V up to 40 V.

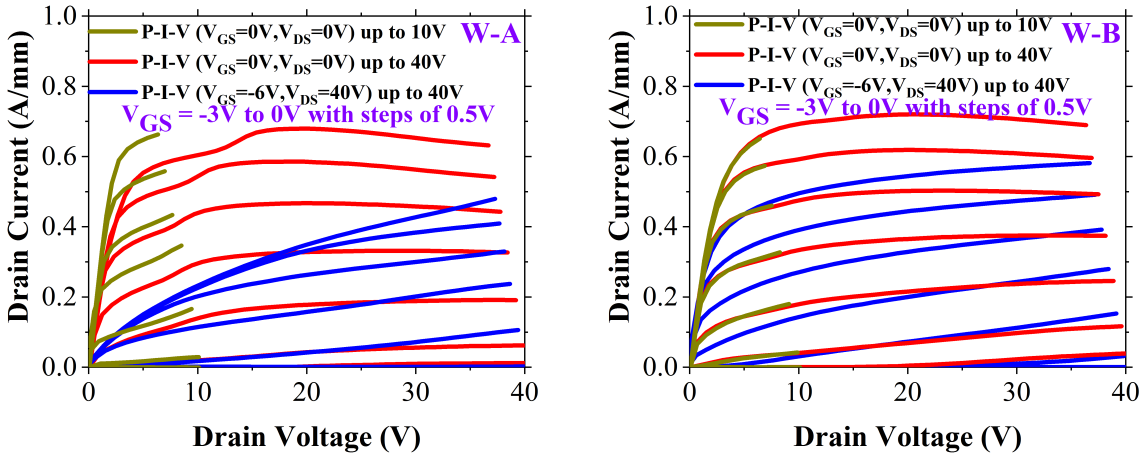

Figure 5.5: Pulse Output characteristics for both wafers with different stress conditions are shown here. Gold color represents V_{GSQ}= 0 V, V_{DSQ}= 0 V up to V_{DS} 10 V max, Red represents V_{GSQ}= 0 V, V_{DSQ}= 0 V up to V_{DS} 40 V max while blue represents gate-drain stress with V_{GSQ}= -6 V, V_{DSQ}= 40 V. For all cases 200 ns pulse length and 1ms pulse period was maintained.

0 V, V_{GDQ}= 0 V) up to V_{DS}= 40 V compared to pulsing only up to V_{DS}= 10 V as seen in Fig.5.5. This demonstrates that rapid trapping in acceptor traps occurs on a timescale less than the 200 ns pulse length at the highest drain voltage. In contrast, wafer-B showed no change in the current with respect to drain stress during Pulse I-V sweep when the maximum pulse voltage changed between 10 V and 40 V. This implies that for this wafer, trapping occurs on a timescale longer than 200 ns at 40 V.

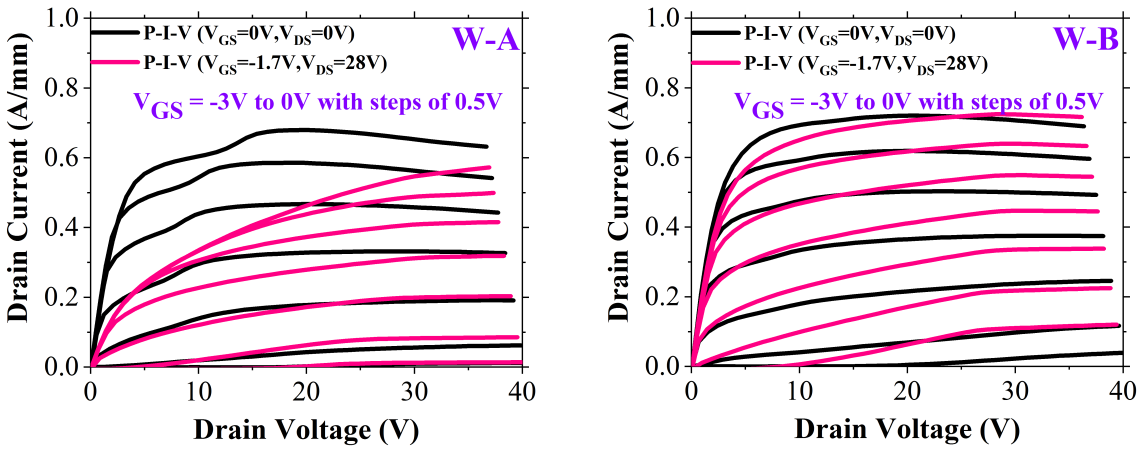

Figure 5.6: Pulse output characteristics for both wafers under RF operating conditions stress are shown here. Black color represents V_{GSQ}= 0 V, V_{DSQ}= 0 V up to V_{DS} 40 V max and magenta represents V_{GSQ}= -1.7 V, V_{DSQ}= 28 V up to V_{DS} 40 V max. For all cases 200 ns pulse length and 1ms pulser period was maintained.

2. ***Pulse I-V Gate lag:*** When comparing the devices pulsed to 40 V from static conditions of (V_{GSQ}= 0 V, V_{DSQ}= 0 V) and Gate stress (V_{GSQ}= -6 V, V_{DSQ}= 0 V) very little difference has been noticed with overlaid output curves for both wafers suggesting that that the drain bias has the most prominent effect on the traps, not the gate.

3. ***Pulse I-V Gate and drain lag:*** The presence of knee walkout and current collapse under drain and gate stress conditions in both wafer-A and wafer-B is clearly seen when static conditions of (V_{GSQ}= 0 V, V_{DSQ}= 0 V) is compared with biased at (V_{GSQ}= -6 V, V_{DSQ}= 40 V) (gate and drain lag). However, the severity of this knee walkout and current collapse is much larger in wafer-A than that observed for wafer-B as clearly seen in Fig.5.5.

4. ***Pulse I-V under RF operating conditions:*** In this study, the devices are analyzed under class B operational mode since they deliver high power added efficiency (PAE) under this mode. In order to replicate exact bias condition for Pulse I-V and RF we have used bias condition of V_{GSQ}= -1.7 V, V_{DSQ}= 28 V with same pulse conditions of 1us as before. These quiescent points corresponded to the DC bias current (I_{DSQ}) that produced maximum output power in the RF measurement. Fig.5.6 shows comparison of shows (V_{GSQ}= -1.7 V, V_{DSQ}= 28 V) with steady state and difference between both wafers can be seen.

   Wafer-A again shows much stronger current collapse while minimal change is observed in case for wafer-B. With observation that wafer-A shows drain bias dependent trap, multiple drain bias stress point varying from 10 V, 15 V, 20 V and 28 V at same V_{GS} has been used showing a direct dependence shown later in the Chapter.

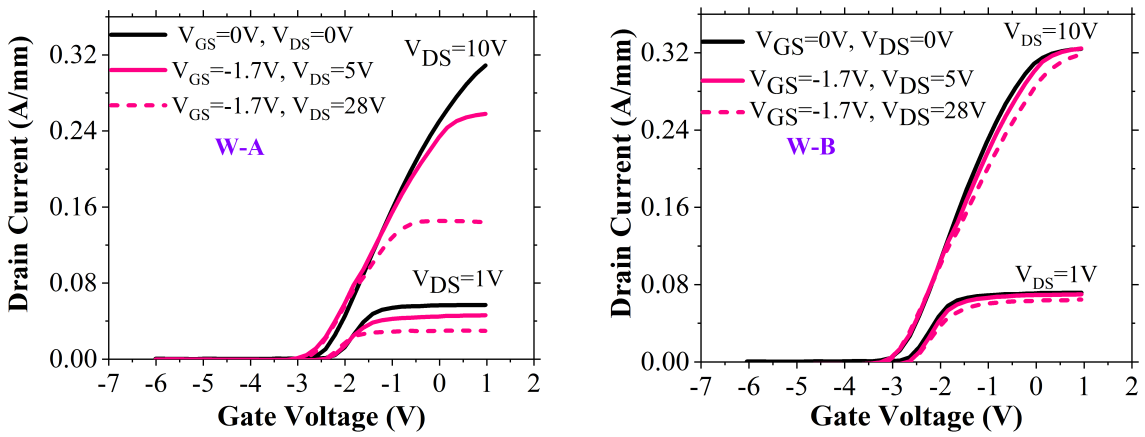

Figure 5.7: Transfer characteristics under RF operating Pulse I-V conditions for both wafer at two different V_{GSQ}= -1.7 V, V_{DSQ}= 5 V and V_{GSQ}= -1.7 V, V_{DSQ}= 28 V are compared with steady state V_{GSQ}= 0 V, V_{DSQ}= 0 V conditions measured for two different V_{DS}= 1 V and 10 V.

5. ***Effect of stress on transfer characteristics:*** If there were any traps in the vicinity of gate or near by it should have resulted in the charge being trapped in the depletion region formed upon high negative stress on gate resulting in V_{th} shift. Similarly, the effect of drain bias would have an effect on the access resistance resulting as change in transconductance g_m. Transfer characteristics measured for both wafers at V_{DS}= 1 V and compared under exact same pulse conditions are shown in Fig.5.7. In case for wafer-B no change in g_m is observed however, wafer-A shows significant change which gets severe with higher drain stress. This further confirms the role of trapping under high drain bias observed before shown in and Fig.5.10. With no shift in V_{th} in either case, confirms no trapping under the gate however, large drop in saturation current for wafer-A indicates an increase in R_d i.e. trapping in drain access region.

6. ***Effect of different stress time during Pulse I-V operation:*** Based on the above reported measured for all the Pulse I-V measurements, we observe current collapse for wafer-A in all case and minimal effect on wafer-B. To understand these traps trap time constant Pulse I-V at different pulse length was performed ranging from ranging from 200 ns, 500 ns and 1 μs as shown in Fig.5.8. No apparent change in knee walkout behavior was observed as compared to observed between two wafers with 1us pulse length. This highlights the fact that trapping time is faster than 200 ns for wafer-A.

7. ***Current transients using Pulse I-V operating conditions:*** To further gain insight into de-trapping recovery time using the same bias conditions current transients were performed as shown in Fig.5.9. Device were stressed at RF biased points for 1000 seconds and immediate change over to on-state at V_{GS}= -1.7 V and V_{DS}= 1 V and recovery was monitored for 1000 seconds as shown in Fig.5.9. Drain dependence is more severe on wafer-A

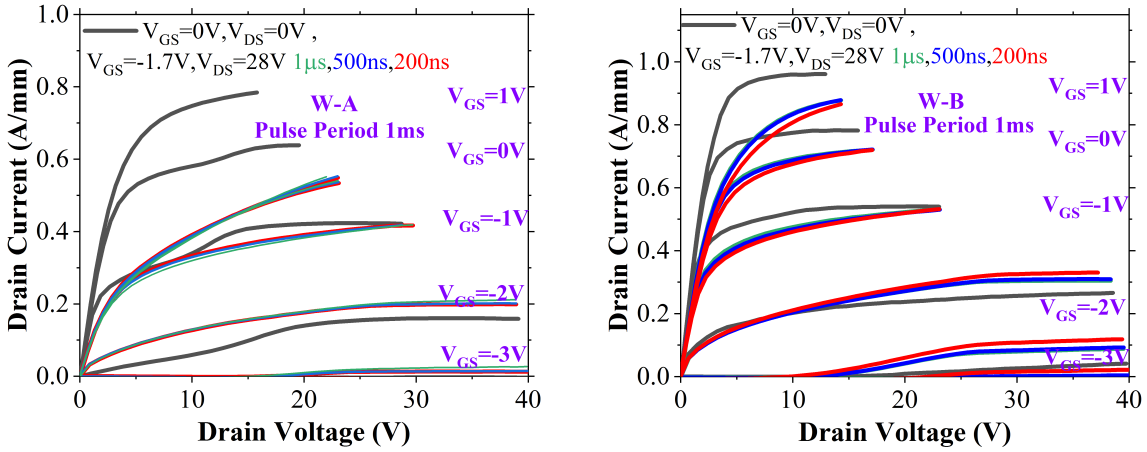

Figure 5.8: Pulse I-V for both wafers under Pulse I-V RF operating conditions at V_{GSQ}= -1.7 V, V_{DSQ}= 28 V for three different pulse length 200 ns, 500 ns and 1 μs with pulse period being 1ms in all cases are compared with steady state conditions of V_{GSQ}= 0 V, V_{DSQ}= 0 V.

while wafer-B has smaller dependence however, both wafers showed longer recovery times. wafer-A shows three different time constants when compared to Wafer B which shows two time constant but much faster recovery. No apparent difference during the transient has been observed which makes the Pulse I-V so distinct between them.

Typical way of analyzing obtained DC, Pulse I-V and transients data is to use them in different ways to extract a trap model for an AlGaN/GaN HEMT, which is used in the fit of a nonlinear device model as suggested by Tarazi *et al.* [166][167]. They suggested using parameters such as trap controlling voltage extracted from Pulse I-V and using trap

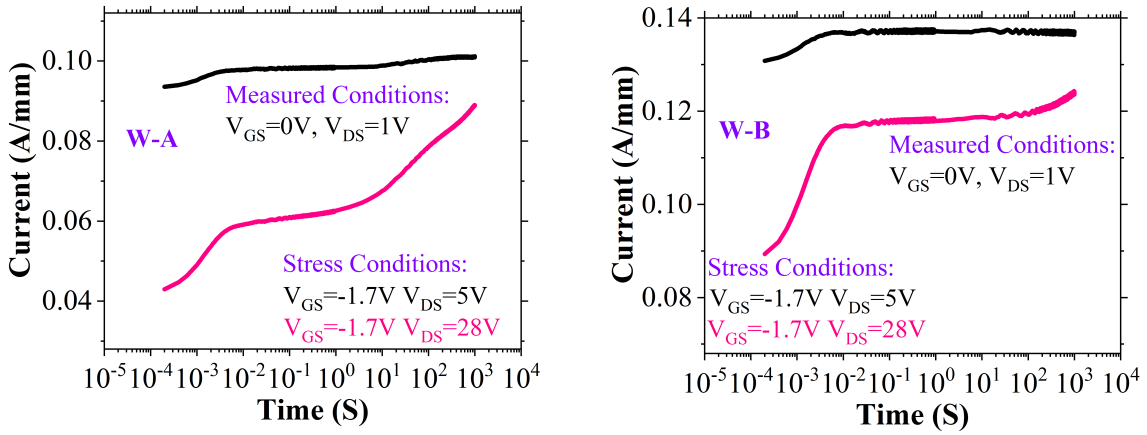

Figure 5.9: Current transients measured at V_{GSQ}= -1.7 V, V_{DSQ}= 1 after 1000 stress at V_{GSQ}= -1.7 V, V_{DSQ}= 5 V and V_{GSQ}= -1.7 V, V_{DSQ}= 28 V are shown. Both wafers shows longer time constant however, wafer-A shows severe dependence on drain bias stress.

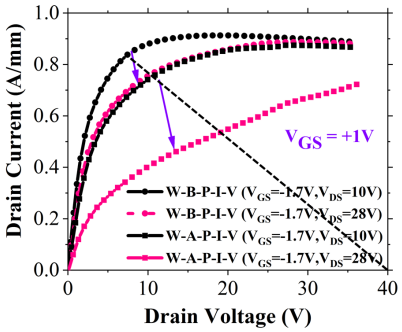

Figure 5.10: Pulse I-V for both wafers under RF operating conditions stress at two different V_{DS}= 10 V and 28 V are shown here. Black color represents wafer B with two different stress V_{GSQ}= -1.7 V, V_{DSQ}= 10 V and V_{GSQ}= -1.7 V, V_{DSQ}= 28 V. Magenta represents wafer-A with same two stress conditions. For all cases 200 ns pulse length and 1ms pulser period was maintained and V_{GS} was kept fixed at +1 V.

time constants from transients, one could simulate transients of the nonlinear model with the trap model included. By using range of drain bias quiescent during Pulse I-V trap potential can be extracted with the difference between current level dividing by steady state transconductance giving steady state trap potential. Based on observations on these two wafers if were used to extract model coefficients for use in a non-linear model modified to account for trapping [158][159][160][161][162][163][164][165][166][167], two different models would be generated, and the predicted RF performance of the wafers would be very different. However, it will now be shown that the measured RF performance of these wafers is very similar and contradicts this expectation.

5.3.2 Large Signal RF performance

To investigate the severity of the knee walkout and current collapse under RF conditions, the measured RF I-V waveforms are transformed into RF dynamic load lines plots, $i_{(d)}$t plotted versus v_{ds}(t). Here the input gate voltage swings between +1 and -6 V corresponding to full saturation. These RF I-V waveform measurements were performed at five different DC drain biases over a range of fundamental load impedances for the devices on both wafers, producing the results shown in Fig.5.11 referred to as an "RF I-V fan diagram" [171][26].

The summary shown in Fig.5.10 here shows comparison of the self-biased class B operating point in saturation under RF bias conditions (V_{GSQ}= -1.7 V, V_{DSQ}= 28 V) with static bias conditions (V_{GSQ}= 0 V, V_{DSQ}= 0 V) for both the wafers for range of V_{DSQ} bias points.

The "RF I-V fan diagrams" highlight that there is no dramatic difference between the two wafers in contrast to what was seen for Pulse I-V in Fig.5.6. There is also no pinch off or buffer leakage issue observable at high drain bias with either of the wafers. In Fig.5.11, it can be noticed that the "knee" of the RF curves, high current/low voltage boundary observed in the $i_{(d)}t$ versus

$V_{ds}(t)$ plots, of each load impedance sweep softens and moves to the right with increasing DC drain bias voltage indicating that there is still a V_{DS} bias dependent knee walkout. Based on

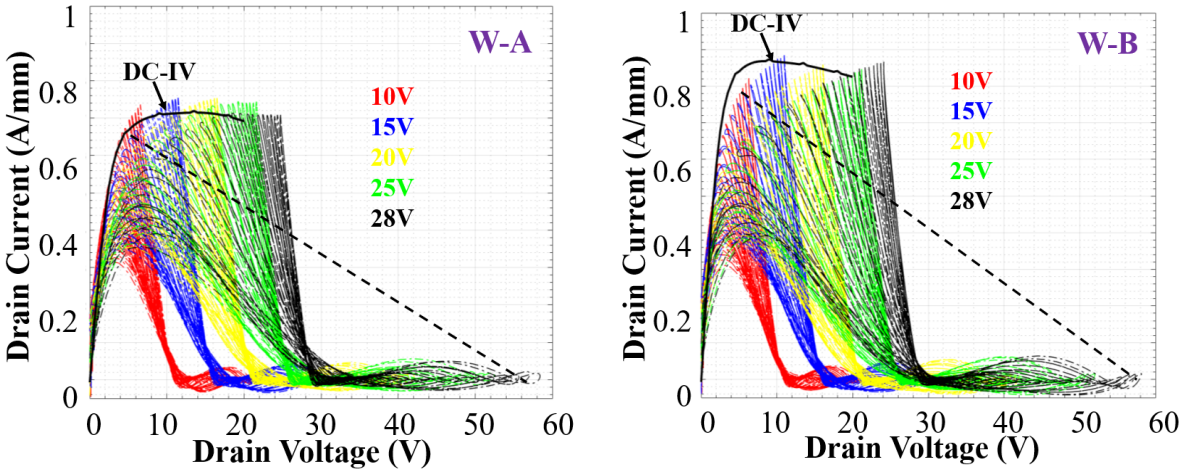

Figure 5.11: RF I-V fan diagrams for both wafers measured at V_{DSQ} = 10 V (red), V_{DSQ}= 15 V (blue), V_{DSQ}= 20 V (yellow), V_{DSQ}= 25 V (green), and V_{DSQ}= 28 V (black), device identifying the RF knee walkout with increasing drain bias. Reference DC I-V at VGS = +1 V (black solid line). This measurement was performed by the research team at Cardiff University as part of research collaboration.

comparison between "knee" of the RF curves seen in Fig.5.11 and Pulse I-V measured under same conditions as seen in Fig.5.10 contrasting observations can be made. Fig.5.10 shows the V_{GS}= +1 V characteristics corresponding to the highest RF input voltage in Fig.5.11. In Fig.5.10, it is clearly evident that wafer-A, exhibits much larger knee walkout and current collapse than wafer-B with increasing drain bias, extending the observation seen in Fig.5.6 to a wider range of operating conditions.

Fig.5.12 shows a plot of the knee voltage against the drain bias voltage. There is no agreed definition of knee voltage, so here the knee voltage for the Pulse I-V data is extracted along the load line presented in Fig.5.6, while the knee voltage for the RF I-V data is extracted along the same load line as presented in Fig.5.11. It is observed that both wafers (under RF conditions) show very similar knee walkout effect with increasing DC drain bias voltage in clear contradiction to the observations made under Pulse I-V where wafer-A showed much more severe knee walkout than wafer-B.

Similar to RF I-V data the maximum output power and maximum power added efficiency (PAE) measured for both wafers for the same P_{IN} in saturation doesn't show significant difference as shown in Fig.5.13 and Fig.5.14. At last 10 devices on both wafers were measured to assess uniformity. Wafer-A at V_{DS}= 28 V gave P_{max}= 29.4 dBm with 0.5 dBm variation between measured devices while PAE max of 68% with 3% variation was measured between devices. For wafer-B gave P_{max}= 32 dBm with 1 dBm variation between measured devices while PAE max

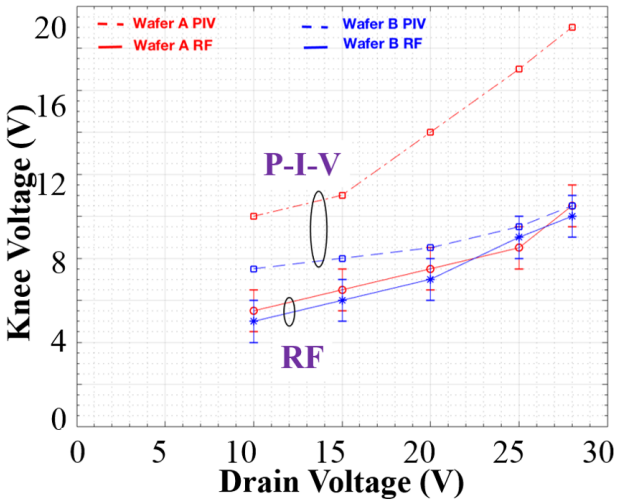

Figure 5.12: Shows a plot of the knee voltage against the drain bias voltage extracted based on load line from Pulse I-V Fig.5.6 and RF load line shows in Fig.5.11. This measurement was performed by Research team at Cardiff university as part of research collaboration.

of 72% with 4% variation was measured between devices. The wafers show very comparable behavior, with the higher power shown by wafer-B entirely explained by the higher maximum drain current measured under DC and is not attributable to any difference in trapping.

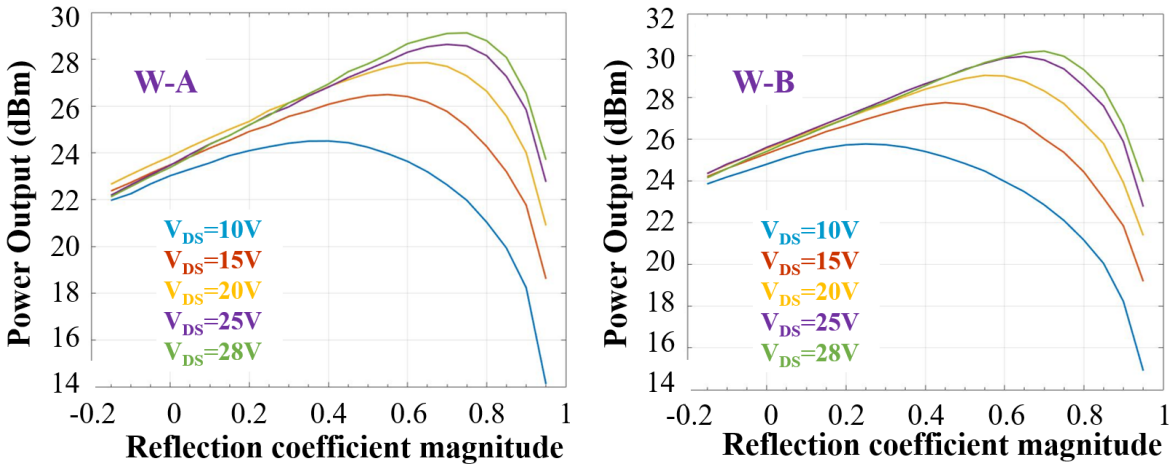

Figure 5.13: Shows RF power output for both wafers measured for varying V_{DS} at 10,15,20,25 and 28 V for both wafers at 1 GHz. This measurement was performed by the research team at Cardiff university as part of research collaboration.

Effect of temperature on device performance: Just to rule out any effect of temperature in all cases the wafer was held on a room temperature chuck. The Pulse I-V and RF measurements were undertaken at the same operating point of V_{GQ}= -1.7 V and V_{DQ}=10, 15, 20, 25 and 28 V in order to try and ensure that the devices had the same self-heating. Of course, the Pulse I-V

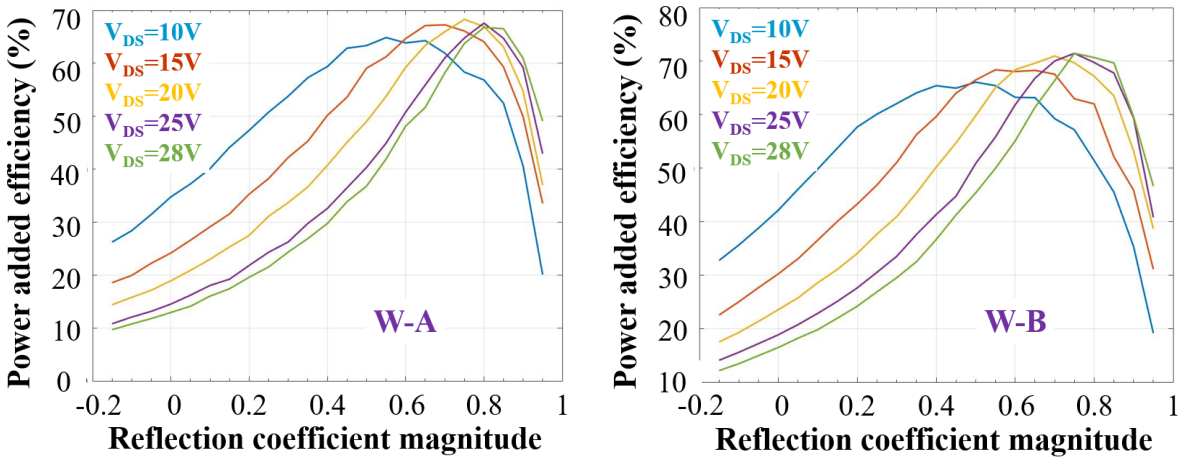

Figure 5.14: Shows Power added efficiency for both wafers measured for varying V_{DS} at 10, 15, 20, 25 and 28 V at 1 GHz. This measurement was performed by Research team at Cardiff university as part of research collaboration.

measurement will not have the benefit of RF-cooling so will be undertaken at a somewhat higher temperature. However, the temperature difference between Pulse I-V and RF would be the same for both wafers since they have almost the same PAE.

Effect of illumination on device performance Casbon *et al.* [168] have shown that illuminating the device with a 3 eV (below bandgap) laser will greatly impact the knee walkout and the current slump. To understand the role of trapping we repeated these measurements using a light source with a Xe lamp with a wide spectrum of 250-1100 nm spectrally filtered by a prism monochromator which was controlled using lab view. Illumination in all cases was maintained constant throughout the experiment. When a 3 eV laser was used, an improvement in the knee

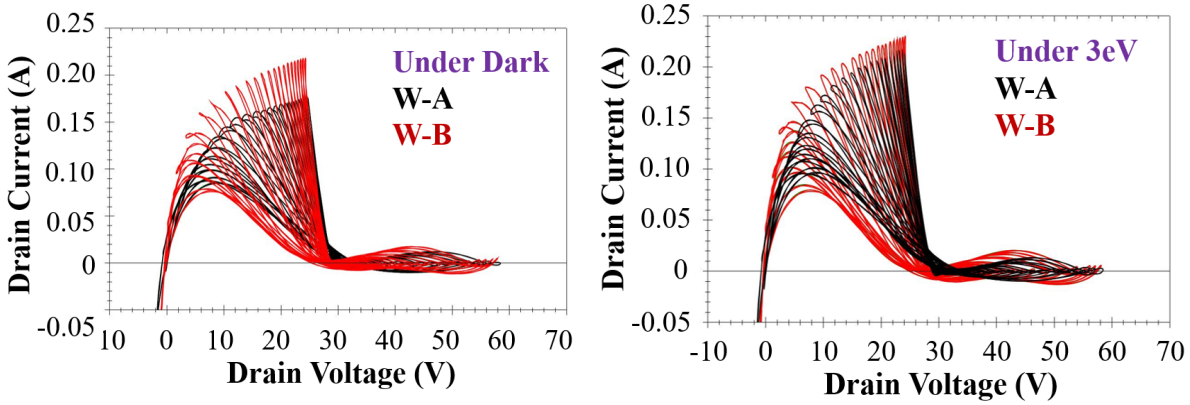

Figure 5.15: RF I-V fan diagrams for both wafers, wafer-A (black), wafer-B (red) measured at V_{DSQ}= 28 V under dark and under 3 eV illumination. This measurement was performed by Research team at Cardiff University as part of research collaboration.

walkout and current collapse was observed; following a similar trend to previously reported work. Both wafers showed an increased drain current when measured under 3 eV laser illumination as shown in Fig.5.15. This improvement in the knee walkout and the current collapse also led to an increase in both the maximum output power (Pmax) and the maximum power added efficiency (PAE max) at V_{DS}= 28 V when illuminated with 3 eV laser. These measurements also complement when Pulse I-V was repeated under 3 eV illumination.

Based on all the observations and trials it appears that the key difference between these wafers is shown in Fig.5.5. wafer-A showed rapid trapping on a timescale shorter than the typically used 200 ns pulse length and that led to a strongly distorted Pulse I-V characteristic. This was then unrepresentative of the 1 GHz RF waveform which had a characteristic timescale much shorter than the trapping time. By contrast, Pulse I-V measurements on wafer-B accurately represented the RF waveforms because both responded faster than the trapping time. Another possible explanation could be wafer-A which shows fast trapping time at higher bias gets de-trapped on the way back which will be the case in RF. With sine wave on input having continuous up and down pattern will causes a pattern on the output, signifying every up is preceded and followed by a down. This would mean any trapping occurring at high drain bias will be de-trapped on the way back during the same run. This won't be the case during Pulse I-V where V_{DS} is swept with respect to assigned time spent on any given V_{GDSQ}, which allows only trapping as shown in Fig.5.16.

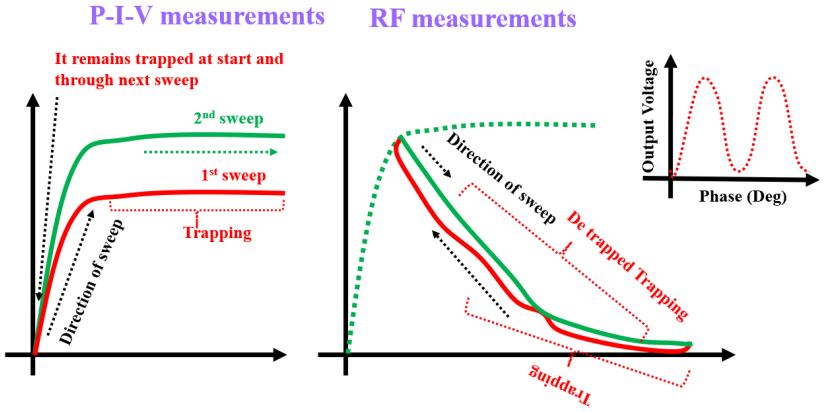

Figure 5.16: Shows basic IV waveform used for Pulse I-V and RF measurements. Due to sequence and direction of IV during pulse all the trapped electronics remains trapped before and during start of next sweep however, under RF due to sinusoidal waveform it is exposed to trap and de-trap process as shown above.

5.4 Conclusion

Two HEMT wafers with different growth characteristics resulted in quite distinct DC and Pulse I-V behavior. Only one showed a kink effect, and also showed much stronger knee walkout in

Pulse I-V. The conventional interpretation of this behavior would suggest a dramatic difference in RF performance. However large signal RF measurements showed no significant difference in output power or efficiency between the wafers. Hence, while Pulse I-V measurements can be a very useful tool for identifying charge trapping, it can fall short in predicting the impact of traps under RF conditions.

In conclusion, great caution must be taken when utilizing Pulse I-V measurements to extract RF device model coefficients aimed at including trapping effects in GaN-based HEMTs. While it may well be possible to formulate a pulsed I-V measurement regime which correctly predicts the RF performance, this is likely to vary with process changes. Thus, appropriate large signal RF I-V waveform measurements are an essential additional requirement, if one is to develop robust non-linear RF device models that include traps.

CHAPTER 6

UNDERSTANDING DRAIN INJECTED BREAKDOWN MECHANISMS IN CARBON DOPED GAN ON SIC HEMT

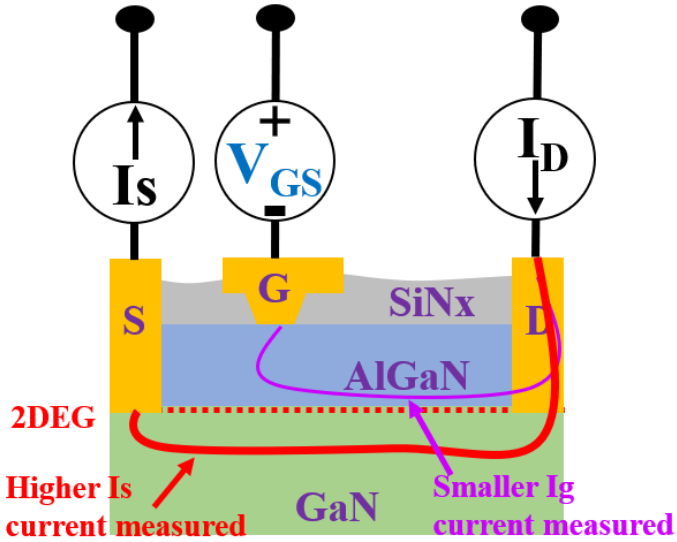

Figure 6.1: Schematic of drain current injection technique to measure breakdown investigating leakage path through the epitaxy.

Chapter 4 and 5 discussed the kink effect and pulse IV analysis on GaN-on-SiC wafers primarily made for RF operation. In this chapter breakdown (BD) study using drain current injection technique for GaN on silicon carbide substrate will be shown. Simultaneous measurements of the drain, source and gate current allows us to present the direct evidence of high source current injection under off-state condition through the buffer, surprisingly

giving higher measured source current than gate current indicating the presence of leakage through the buffer as shown in schematic above Fig.6.1. Electroluminescence has been performed to understand the localization of charge within the device and simulations has been used to further validate the experimental study. All measurements in this chapter are preformed on sample-IQE-wafer-A-norstel (GMX21-21-420-353). Simulation work shown in this chapter are contributed by Mark Yang.

6.1 Introduction

Large bandgap enables GaN to withstand high breakdown fields which with high saturation velocity makes it suitable for high power/voltage application. Recent advancement in epitaxy and device processing has enabled excellent performance during RF for AlGaN/GaN high electron mobility transistors (HEMT). High power fast switching also makes these devices vulnerable to breakdown (BD) which is defined as conditions at which a sudden increase in measured current/voltage is observed. Several BD mechanisms have been suggested taking part in the different region of the device. Uren *et al.* showed that the increase in drain current at high drain voltages (and in pinch-off conditions) can be ascribed to punch-through effects, i.e. the flow of current within the bulk of the GaN layer [172]. Using a two-dimensional finite-element simulation they demonstrated that like other types of field-effect devices AlGaN/GaN single heterojunction are vulnerable to short-channel effects and suggested using high density of deep acceptors to be incorporated in GaN buffer to make it more insulating and confine the carriers in the channel which over the years has been achieved by use of Iron (Fe) and Carbon. In another model, Tan *et al.* suggested surface-hopping mechanisms and attributed the breakdown at high drain voltages to a thermal runaway process, which occurs when a certain power threshold is reached by surface current conduction, however, the current generation of devices shows much-improved surface morphology which suppresses that effect [173]. Recently Killat *et al.* studied the impact ionization processes in special test structures consisting of AlGaN/GaN HEMTs with an InGaN back barrier [174]. They demonstrated that such structures emit electroluminescence (EL) peak at the InGaN bandgap energy when operated as transistors. They suggested that this EL peak originates from the recombination of electrons and holes generated by impact ionization.

Most of the conventional breakdown measurements involved irreversible damage to the device or degradation until Alamo *et al.* first reported current controlled breakdown method and called it drain-current injection technique which enabled a study of the physics of breakdown in HFET's [175]. In this method source (I_S) is kept grounded and current (I_D) is injected into the drain of the on-state device. The gate voltage (V_G) is then ramped down to shut the device off leading to a rise in the drain-source voltage to a peak. This peak represents an unambiguous definition of three-terminal breakdown voltage (BDV). This unique technique gives the advantage of avoiding repetitive scanning and reduced the risk of burnout in unstable and fragile devices. Using this

technique Wang *et al.* suggested that the source injection through the buffer can also induce impact ionization and cause a premature three terminal breakdown in conventional AlGaN/GaN HEMTs [176]. However, no direct evidence of an increase in source current injection or any electroluminescence study has been reported so far confirming the role of impact ionization.

In this work, we present the BD study using current injection technique for GaN on silicon carbide substrate showing breakdown characteristics. Simultaneous measurements of the drain, source and gate current allows us to present the direct evidence of high source current injection under off-state condition through the buffer. There seems to be two process involved: (i) at the gate depletion region there is leakage path between the gate and the source, (ii) at higher negative off state punch through current dominates and it triggers the impact ionization near drain side of the gate edge. Electroluminescence measurement have been performed under the same biasing conditions to gain insight. Atlas device simulation is used to replicate the measurement scenario and suggests that it is source injection in these devices which initiate breakdown process. This study provides further insights into the breakdown mechanisms for AlGaN/GaN HEMTs which is critical for making this device reliable for commercial applications.

6.2 Sample and Measurements

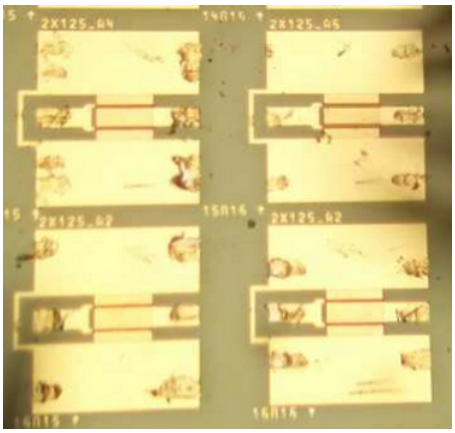

Figure 6.2: Shows the device used for breakdown (BD) study.

MOCVD grown structure of AlGaN barrier, GaN buffer and AlGaN nucleation layer on insulating SiC has been used for this study. The exact same Wafer-A used in kink study explained in chapter-4 has been used here, the device schematic used for this measurement can be seen in Fig.6.2 [177]. The device used for the study has a width of 2x125 μm, a gate length of 0.25 μm, the source-drain spacing of 4 μm, and source-gate spacing of 1 μm has been fabricated using Ti/Al/Ni/Au and Ni/Au for Ohmic and Schottky contact respectively, and with silicon nitride as a passivation layer. The device used here have been fabricated at FBH Berlin under the project funded by ESA. DC I_D-V_D measurements up to 40 V drain bias with 1V/sec sweep rate are shown

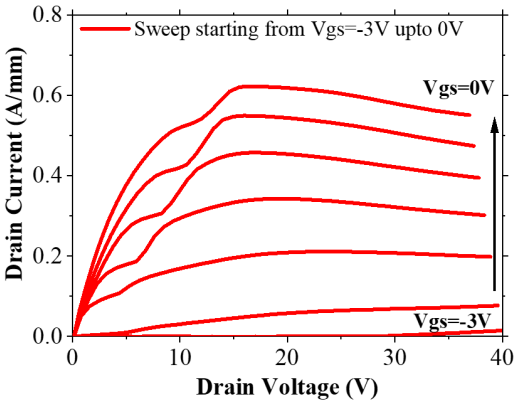

Figure 6.3: Shows DC output characteristics of AlGaN/GaN HEMT device used for breakdown study. V_{GS} is varied from -3 V to 0 V while V_D is varied from 0 to 40 V.

in Fig.6.3 with kink seen at 3-5 V above the knee. A detailed study on the origin of kink on this sample explained using floating buffer is explained in chapter 4 of this thesis as wafer-A. Gate leakage of 10^{-4} A/mm has been observed on the devices used for this study. To characterize breakdown, a fixed predefined current is injected into the drain, the gate-source voltage is ramped down from a strong forward bias to below the threshold, and drain voltage (V_D), gate current (I_G) and source current (I_S) are monitored as shown in Fig.6.4. The technique traces the locus of drain voltage (V_{DS}, Drain gate voltage (V_{DG}), and I_G versus V_{GS} at fixed I_D on the output I-V characteristics. BDV is unambiguously defined as the maximum V_{DS} attained for an injected I_D of x A/mm, irrespective of V_{GS}. For all the measurements high resolution source measuring unit (HRSMU) and triax cables were used to insure precise measurements.

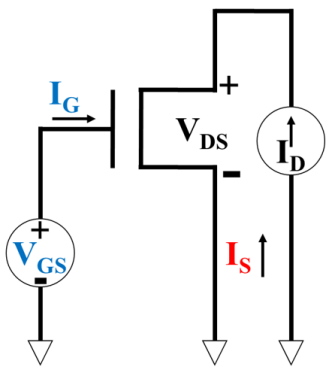

Figure 6.4: Shows schematic of drain injected breakdown technique. Constant current is injected using the drain while continuously source and gate current are monitored along with drain voltage.

Fig.6.5 shows the measured V_D for different I_D starting from 1nA and all the way up till

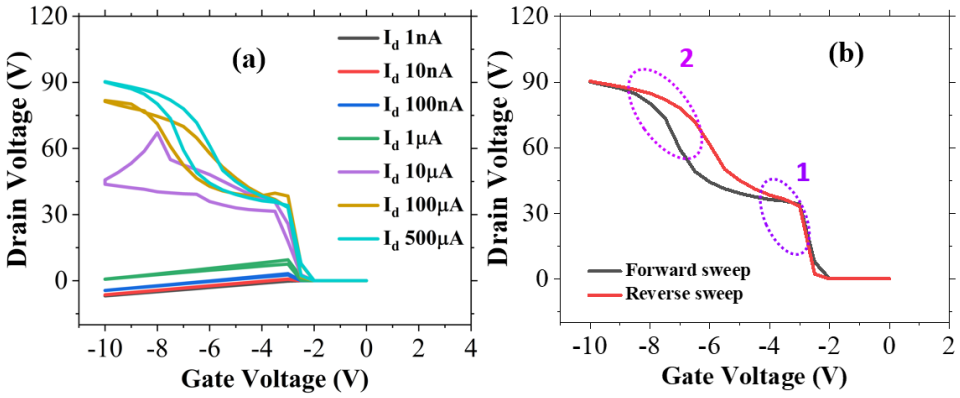

Figure 6.5: Shows (a): measured drain voltage for range of I_d bias changing from 1 nA up to 500 μA, (b) shows two step change observed during the high drain current injection labelled 1 and 2 for forward and reverse sweep for I_d 500 μA.

500μA. At 500μA as shown in Fig.6.5, with positive gate bias, the V_D remains very small and as the gate bias is varied further to negative bias from V_{GS}= 0, at V_{GS}= -3 V the channel gets pinched off resulting in an increase in measured drain voltage from near zero along with an increase in the magnitude of I_S and I_G. Further increase in negative gate bias shows increasing measured drain voltage going until BDV of 105 V at the end of the sweep at V_{GS}= -10 V. Two step change points change be seen (i) around V_{GS}= -3 V where V_{DS} shoots up till 35 V, the (ii) one is seen at V_{GS}= -8 V where V_{DS} goes past 85 V. The first step change is noticeable at lower I_D source currents as well however the second step change is absent till 1 μA I_D source and appears only after 10 μA I_D source. This behavior is consistent across all device on this wafer and other sister wafers as well. The reason to limit I_D to 500 μA is the burn out beyond, the V_{DS} under higher I_D tends to increase all the way up to 150 V leading to device burn out. For rest of the study I_D is limited up to 500 μA. A small hysteresis can also be observed the size of which remains consistent at higher I_D source. At lower I_D source value not much hysteresis has been observed.

Fig.6.6 shows the measured gate current during the V_{GS} sweep. Nothing significant can be seen apart from small increase in current beyond 1 μA I_D source. Fig.6.7 shows measured source current which is observed to be lower than gate current till I_D source of 10 μA. Expected pinch off in source current can also be observed till 10 μA drain current, at this point hysteresis can be observed along with two step change behaviour. Beyond this current bias (10 μA), the source current shoots up and exceeds gate current, any bias beyond this always shows higher source current compared to gate. Expected pinch off in source current can be observed till 1 μA drain current beyond which direct flow of current is observed even with higher pinched off gate bias. For all the bias conditions the observed source current remains higher than the measured gate current. These measurements are consistent and repeatable indicating that there is no physical

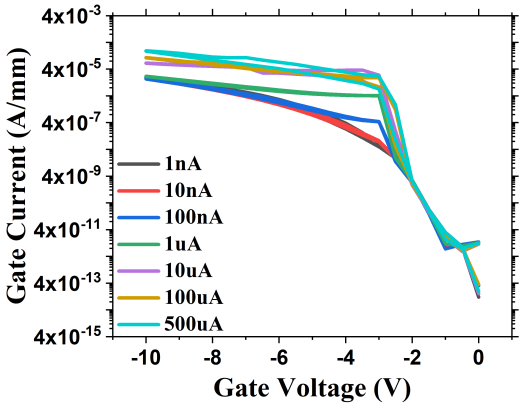

Figure 6.6: Shows measured gate current for range of I_d bias changing from 1 nA up to 500 μA.

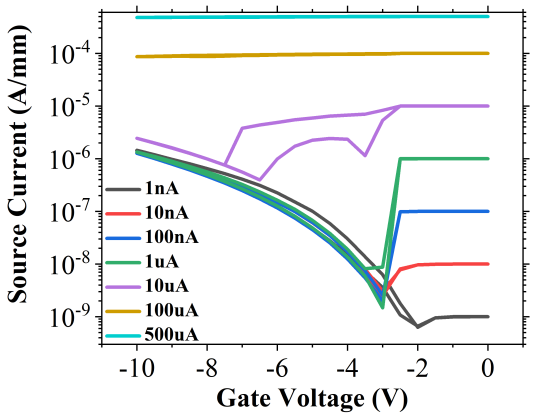

Figure 6.7: Shows measured source current for range of I_d bias changing from 1 nA up to 500 μA.

breakdown in the device. Interestingly both source and gate current show hysteresis with both showing two step change as shown in Fig.6.8. At I_D= 500 μA all the measured values, V_D, I_G and I_S shows two step process at same bias conditions as marked in the figure.

Based on different source and gate current during breakdown, normal leakage measurements has been performed on the exact devices. Same gate bias range has been used with V_{DS} fixed at 10 V as shown in Fig.6.9. No hysteresis in either of the measured current or nor any step change can be seen. The magnitude of all the currents are similar and no apparent change has been observed. Illumination techniques have successfully been used to identify and characterize trap levels by monitoring the recovery under light, whereas in this work illumination is used during the breakdown measurements to gain information about the processes involved. Light source for the experiments has been a Xe lamp with a wide spectrum of 250-1100 nm spectrally filtered by a prism monochromator controlled using lab view. The optical fiber connected to lamp has been fixed right on top of the device to ensure the distance remained fixed during all exposures. A range of photon energies varying from 2 eV to 4 eV has been performed with no difference on the

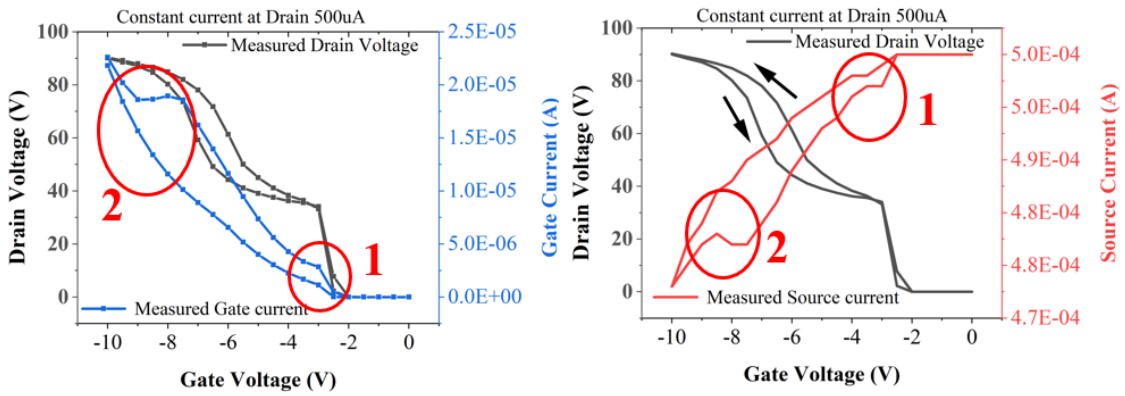

Figure 6.8: Shows measured source and gate current for range of I_D bias of 500 μA, a two step change process can be seen for both gate and source current at exact same position as for drain voltage.

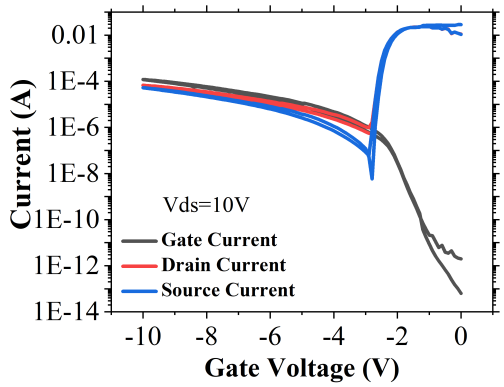

Figure 6.9: Shows gate leakage measurements on the same device with not much difference in the current for gate, source and drain during high off-state gate bias measured at drain bias= 10 V.

behaviour as compared to measurements under dark a shown in Fig.6.10.

To understand the BDV the Electroluminescence (EL) microscopy has been carried out with a 50x objective and Opticstar charge-coupled device (CCD) camera under bias conditions. EL measurement setup explained in chapter-3 has been used to capture spectra from both top and bottom side [113]. To enable back side spectroscopy wet chemical etch has been used to remove the backside metal coating under the device. The CCD camera used here records spectra integrated over several seconds hence all EL spectra are an average over a couple of repeated cycle of operations.

EL imaging: EL imaging has been performed under exact same electrical measurement conditions. Six (V_{GS}= -2 V, -4 V, -6 V, -7 V, -8 V and -10 V) different bias point aimed to capture both step change has been used. Fig.6.11 shows (a) the plot for EL intensity measured across the

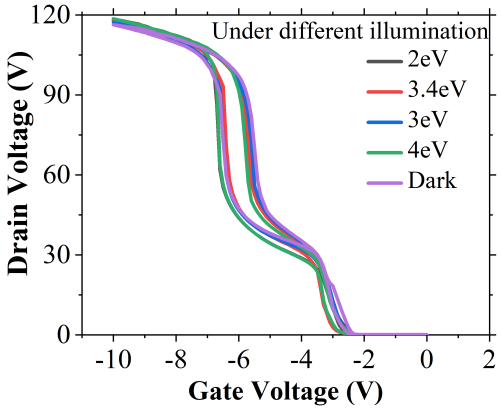

Figure 6.10: Shows effect of various illumination during breakdown study on the the device showing almost identical results.

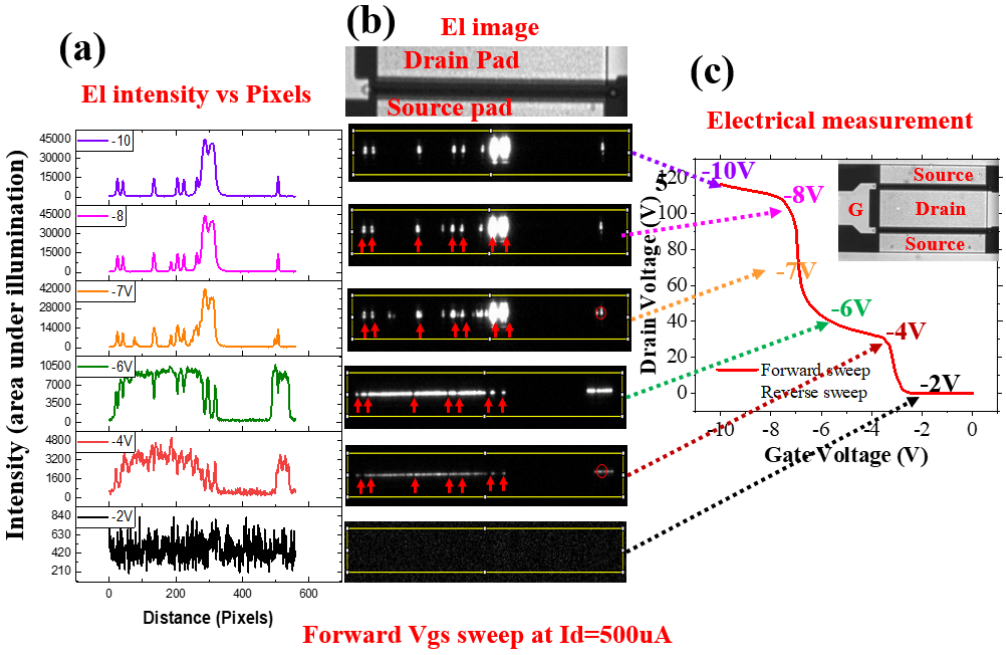

Figure 6.11: Shows EL intensity plot (a), EL image (b) under forward direction breakdown study, (c) measured from the back through the SiC. Uniform illumination at lower bias splitting into large bright spots can be seen in the EL image. The dark spots observed marked with red arrows at lower bias are the same exact spots where bright spots comes up.

width of the channel at the six different bias conditions, (b) shows the EL image captured under each bias conditions (c) V_{GS} sweep in forward direction with I_D fixed at 500 μA along with device image (inset). Based on the EL image (b) it can be seen uniform illumination across the width of the gate finger which starts appearing at the first step change around V_{GS}= -4 V. At second step change bias around -7 V high intensity EL spots can be observed which only gets brighter with

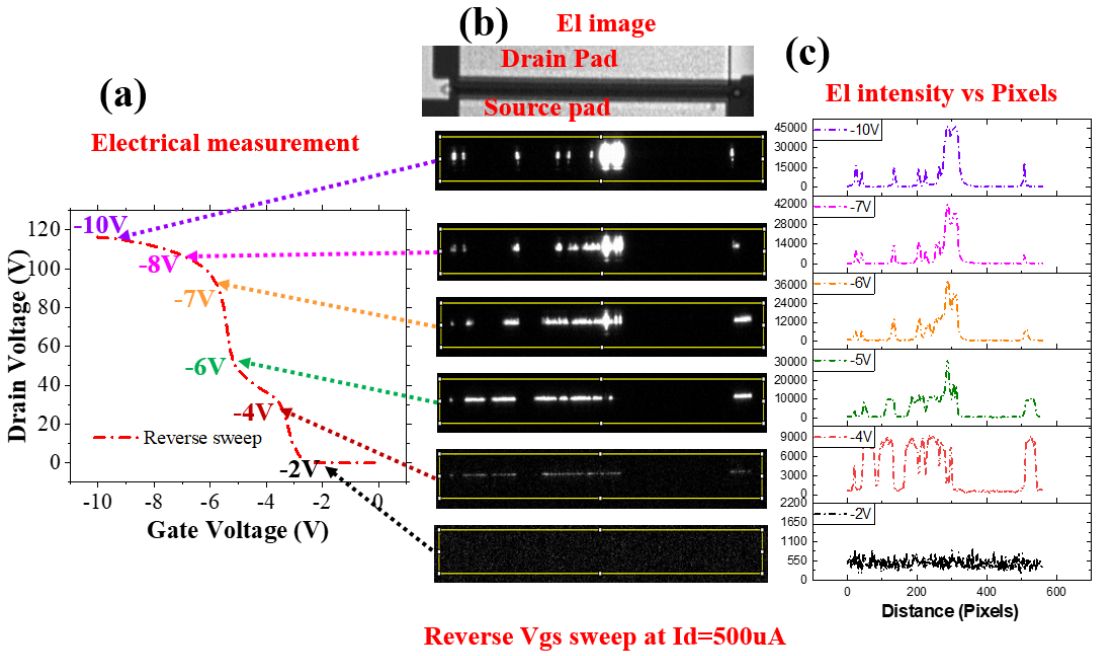

Figure 6.12: Shows EL intensity plot (a), EL image (b) under reverse direction breakdown study (c). Uniform illumination at lower bias splitting into large bright spots can be seen in the EL image. The dark spots observed at lower bias are the same exact spots where bright spots comes up.

further increase in bias. Intensity of these distributed bright spots are roughly four times the initial illumination as seen from the intensity vs pixel plot by comparing intensity observed at V_{GS}= -7 V with V_{GS}= -6 V or any lower Fig.6.11(a).

Another interesting finding observed on EL images Fig.6.11 (b) is the transition from dark to bright spots. At V_{GS}= -4 V and -6 V dark spots in the rather uniform line illumination can be seen (marked with arrow), there are the same spots which turn intense bright at V_{GS}= -7 V (marked with red arrows) while rest of the area brightness disappears. This change matches well with the step change observed in the measured drain voltage, drain current and the source currents. Very similar pattern has been observed on the return sweep as seen in Fig.6.12. These bright spots almost come together to form uniform illumination as the bias gets low. These measurements have been repeated on more than 5 set of devices and they appear very repeatable with almost identical intensity and same spot local position.

EL spectra: EL spectra has been recorded with a broad-spectrum fibre coupled to a compact spectrometer (Maya 2000-Ocean optics QEPro) sensitive in the range 200-1100 nm and measured across different bias points shown here in Fig.6.13. To have better access EL spectra measurements were performed from the back side of the device through the transparent GaN layer and SiC substrate, enabling access to the entire source-drain region including areas underneath the metal contacts. The electron temperatures at different gate biases are extracted by the

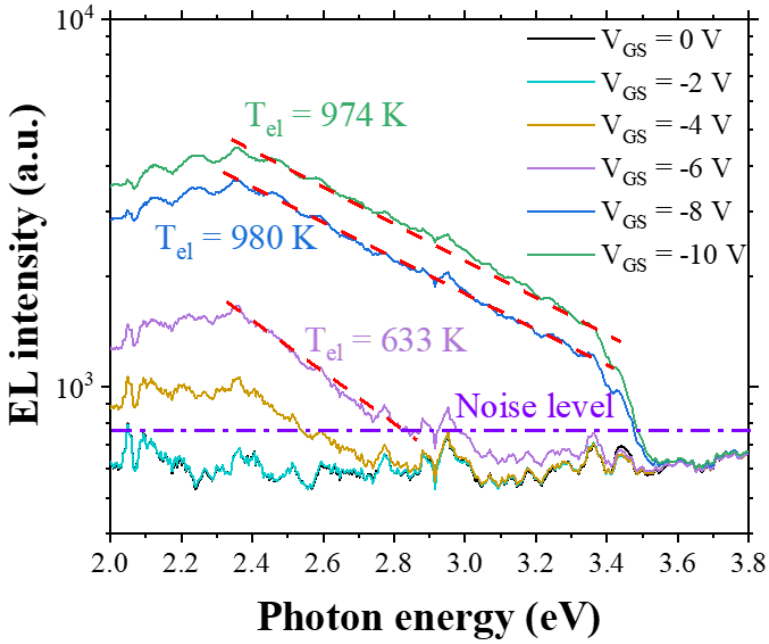

Figure 6.13: Shows the EL spectra measured across the backside of the device at different gate bias (with I_{DS}= 500 μA). The exponential fitting curves are used in the high photon energy part to extract the electron temperatures. The cutoff observed around 3.4 eV could be due to absorption in the SiC substrate.

exponential equation below:

$$I_{EL} \sim exp\left(-\frac{E_{photon}}{k_B T_{electron}}\right) \tag{6.1}$$

where I_{EL} is the EL intensity, E_{photon} is the measured photon energy, k_B is the Boltzmann constant and the $T_{electron}$ is the electron temperature. At a low gate bias (V_{GS} = 0, -2, -4 V), the measured EL intensity are close the noise level and it's not possible to calculate the electron temperature. At a high gate bias (V_{GS} = -6, -8, -10 V), there is a clear exponential behavior of EL intensity against the photon energy at the high energy part. A rapid increase of electron temperature can be found when V_{GS} varies from -6 V to -8 V where there is a dramatic drain bias increase in the same region shown in Fig.6.11(c), resulting in an increase of lateral electric field. However, the electron temperature gets saturated when V_{GS} varies from -8 V to -10 V, just corresponding the saturation plateau of V_{ds} where the lateral electric field does not change any more. No signal can be detected beyond the band gap energy of GaN 3.4 eV.

6.3 Discussion

In order to explore the breakdown mechanism in the carbon doped GaN-on-SiC HEMT, here we employ a device simulation. A generic structure is built and simulated by using Silvaco ATLAS.

This model is the same as the case 1 (wafer A) explained in chapter-4 Kink in floating buffer model [113], except in this case the additional impact ionization model has been implemented. The dependence of impact ionization coefficient on the electric field is calculated by the Chynoweth's equation:

$$\alpha = ae^{-\frac{b}{E}} \tag{6.2}$$

where α is the impact ionization coefficient, E is the electric field, a and b are constants. Here for the electrons, a has a value of 1.5 x 10^5 cm^{-1} and b has a value of 1.41 x 10^7 V cm^{-1} [178]. Same measurements conditions as observed in Fig.6.5 (b) has been simulated and shown

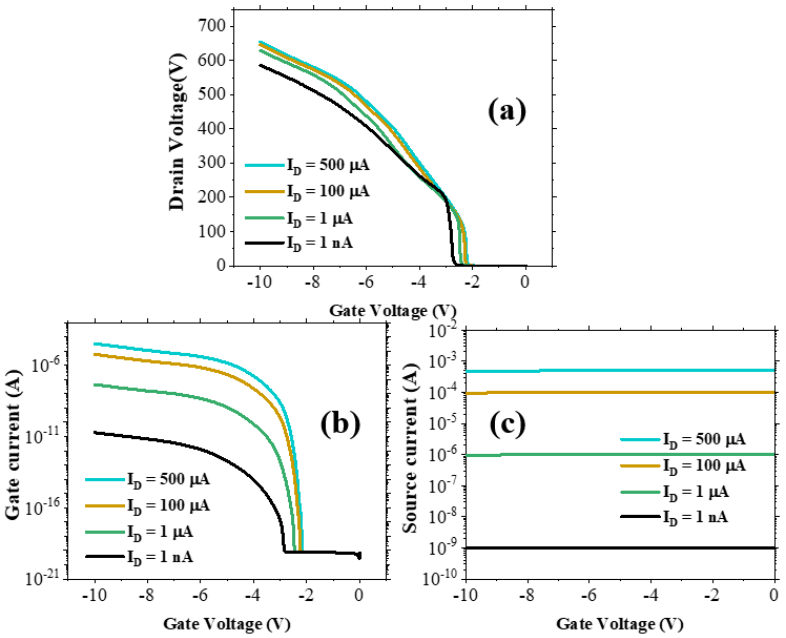

Figure 6.14: (a) Simulated drain voltage for a range of I_D bias; (b) simulated source current, (c) simulated gate currents. The behaviour looks very similar to experimental data however, the magnitude is much higher, also the measured source and gate currents are much higher than shown here.

in Fig.6.14. At a high current bias (I_D = 500 μA), the simulation can reproduce a similar trend with the measurement in terms of observed drain voltage Fig.6.14 (a), gate current Fig.6.14 (b) and source current Fig.6.14 (c). However, at a low current bias (I_D = 1nA), the simulation results although depicts exact similar behaviour the magnitude are far from the measurement. Currently as seen on the Fig.6.14 (b), gate current is much lower than the drain current at a low current bias (V_{GS} = -10 V) compared to observed experimentally. This can be possibly explained by a leakage path between source and gate, which is not involved in the simulation. The primary leakage path is drain induced punch through the gate leading to an electron current from the source to drain. The punch through occurs even if the impact ionization model is turned off in

the simulation which hints that the impact ionization is a secondary effect. This shows that EL observed here is due to Bremsstrahlung and not associated with impact ionization.

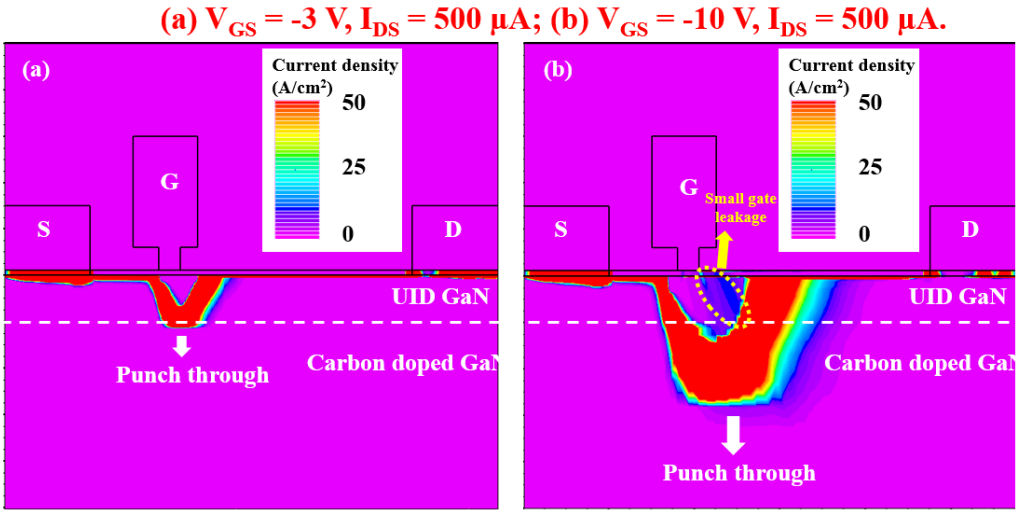

Figure 6.15: Shows the simulated current density distribution under 2 different conditions. (a) V_{GS} = -3 V, I_D = 500 μA and (b) V_{GS} = -10 V, I_D = 500 μA.

Further to understand impact of higher off state gate voltage at a high current bias (I_D = 500 μA), the current density distribution are plotted in Fig.6.15. When -2 V < V_{GS}< 0 V, a high density of free electrons in the 2DEG will contribute to the drain-to-source current. When -4 V < V_{GS} < -2 V, the device starts to be pinched-off, however a constant drain current will force a punch-through leakage path through the UID GaN layer as shown in Fig.6.15 (a). As the drain current bias continues to increase the gate voltage further up to -10 V, the depletion region under the gate gets deeper and the punch-through leakage path is pushed far away from the channel to the carbon-doped GaN layer shown in Fig.6.15 (b). Meanwhile, the drain voltage should be enough high to maintain this leakage path, consequently leading to a high electric field near the drain side of the gate edge. Thus, the impact ionization occurs at such a high reverse bias producing additional free carriers and forming a small gate leakage path.

Based of the simulations and the experimentally observed two setup change process the entire breakdown mechanism can be summed up into two process and summarized at these two conditions along the 2DEG:

Case 1: $I_S = I_G \gg I_D$. It suggests that there is another leakage path between the gate and the source (presently not replicated in simulation).

Case 2: $I_D = I_S \gg I_G$. It suggests that the punch through current dominates and it triggers the impact ionization near drain side of the gate edge.

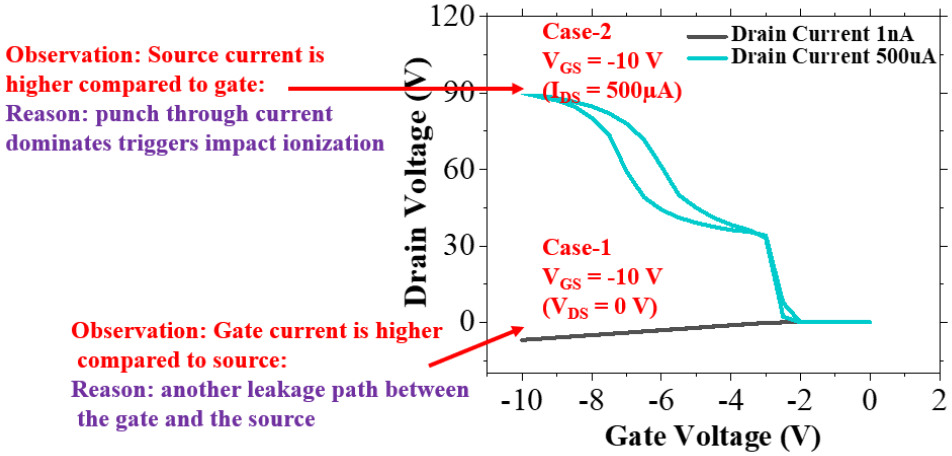

Figure 6.16: Shows breakdown measurements at two different drain current conditions and the the reason for both the process.

6.4 Conclusion

Breakdown (BD) study using drain current injection technique for GaN on silicon carbide substrate has been shown. Lower source current at 1 nA was observed with low drain injected current which surprisingly increased beyond gate at higher current injection. The two step process one initiated by leakage path between source and drain and other due to punch through current triggering impact ionization near drain side of the gate has been explained using simulation as shown in Fig.6.16. Electroluminescence has been performed to understand the localization of charge within the device indicates that the recombination of the electron-hole pair is the not the origin of the EL in this case since No signal can be detected beyond the band gap energy of GaN 3.4 eV. This study provide useful information about the quality of buffer and its usability for RF operations.

CHAPTER 7

LATERAL CHARGE TRANSPORT IN CARBON-DOPED BUFFERS FOR GAN-ON-SILICON POWER DEVICE

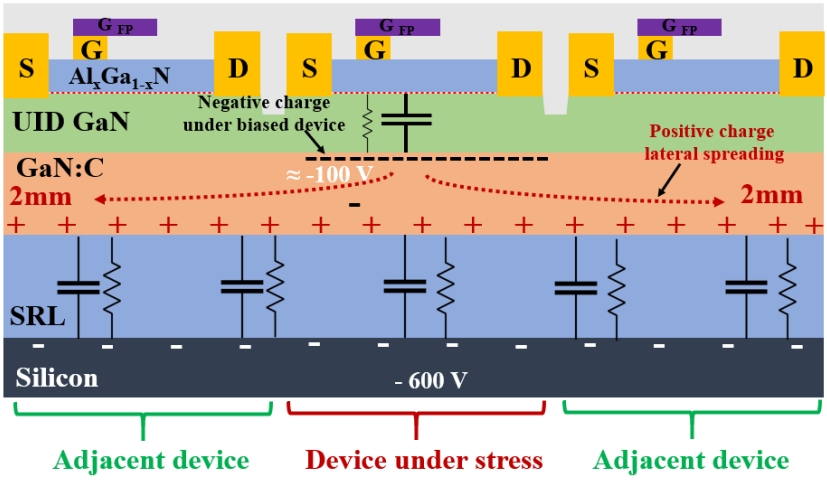

Figure 7.1: Schematic illustration of the lateral charge spreading under central device under stress and spreading put to the adjacent devices up to 2 mm far.

We demonstrate experimental evidence of lateral charge transport spreading up to 2 mm beyond the active area of a biased GaN-on-Silicon Power HEMT device and resulting in changes in R_{ON} in adjacent devices as shown in Fig. 7.1. Guarded surface leakage test structures have been used to show that the lateral leakage path lies within the bulk of the buffer and is not a surface effect. This behaviour is consistent with the accumulation of positive charge at the interface between the carbon doped GaN layer and the AlGaN strain relief layers. The time-dependent charge storage impacts unprobed device performance and can be a significant

concern for on-wafer reliability measurements, or more seriously, system integration where devices share the same epitaxy. Samples in this work have been fabricated at the University of Sheffield U.K. under the Power-GaN project funded by EPSRC. This chapter has significant content reproduced from my recently published work [179].

7.1 Introduction

GaN HEMTs are now being widely used for high power switching and high-frequency applications, and this has led to an increasing demand for a better understanding of their epitaxy. Due to intrinsic impurities and defects, GaN has an inherent n-type behaviour and hence deep levels have been added as a dopant to suppress leakage, improve short channel effects, and improve the breakdown voltage [180]. Along with its benefits, deep levels also bring problems such as charge trapping in the buffer which causes time-dependent issues like current collapse (CC) and dynamic R_{ON}. Time-dependent instability can come from surface or buffer related issues. Recent advancement in surface passivation techniques and good field plate design have enabled almost complete suppression of surface-related problems, however, buffer related effects are still a concern.

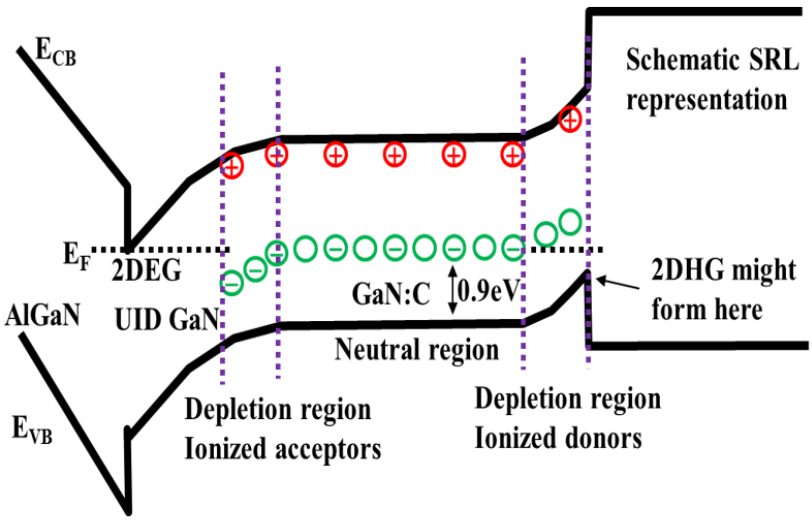

Figure 7.2: Band diagram showing compensating carbon acceptor and donor levels, resulting in negative and positively charged depletion regions at top and bottom of the GaN:C layer.

GaN-on-Si epitaxy normally uses a structure of an AlN nucleation layer, an AlGaN superlattice or step-graded AlGaN strain relief layer (SRL), a carbon doped GaN layer, an undoped GaN channel layer, topped by an AlGaN based barrier. Carbon with an acceptor level of 0.9 eV above the valence band is a widely used dopant to suppress leakage and enhance breakdown voltages [181],[182]. A key point is that the Fermi level is pinned in the lower half of the bandgap making

the buffer slightly p-type as shown in Fig. 7.2 and resulting in transport being via holes excited to the valence band or by trap-to-trap hopping [183],[67]. Transient effects are normally dominated by transport rather than trap capture/emission [183]. Polarization charge at the heterojunction interfaces will lead to the active 2-dimensional electron gas (2DEG) in the channel under the top AlGaN barrier, however of relevance to this paper, a 2-dimensional hole gas (2DHG) can also form at the top of the SRL as shown in Fig.7.1 [184][185]. Normally compensating donors associated with the carbon doping will act to suppress this parasitic 2DHG if the density is high enough [138]. However, when the 2DHG is not fully suppressed, lateral flow in the buffer has been observed extending up to 100 μm outside the active area of the device [186]. This lateral flow has resulted in a device area dependent sensitivity to substrate bias making it important to understand charge storage at interfaces and layers in the epitaxy in order to have reliable device operation [186] [187]. In this work, carbon doped GaN on silicon devices aimed for power applications have been evaluated, using stepped and ramped substrate bias. Substrate ramp measurements were found to be device active area dependent, suggesting that lateral charge spreading occurred beyond the physical active area of the device. Furthermore, a customized surface and buffer leakage test structure has been used to confirm the good surface quality and demonstrate that the leakage is related to the buffer conduction mechanism. Stepped substrate bias measurements show that this spreading mechanism extends up to 2 mm away from the device, impacting adjacent devices. Recovery trap time constants of up to 100 of seconds have been shown using dynamic on-resistance measurements. The lateral charge spreading beyond the active area with long recovery time constant can be a serious concern for wafer level reliability or for system integration when different devices share the same epitaxy.

7.2 Sample details and measurements

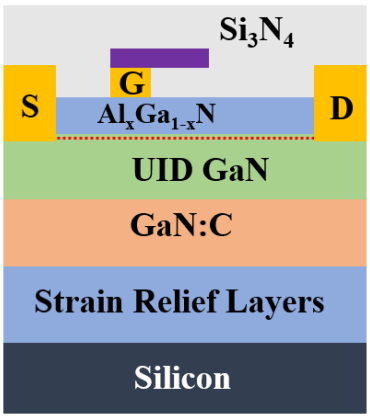

Figure 7.3: Schematic of Carbon doped epitaxy grown on silicon used for this study.

The samples studied here have been grown using MOCVD on a p-type silicon substrate,

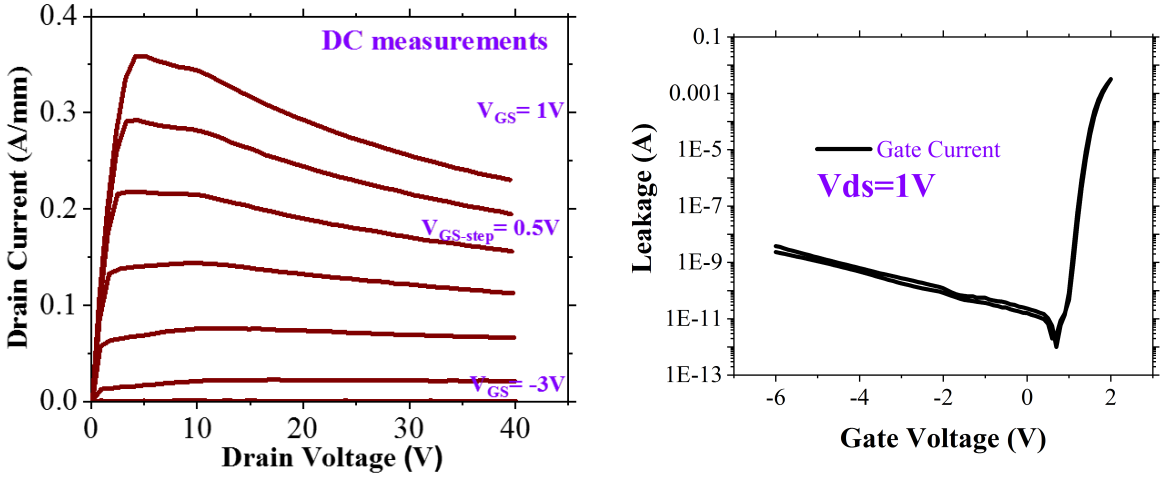

Figure 7.4: DC output characteristics of single finger device measured from V_{GS}= -3 V up to V_{GS}= 1 V with steps of 0.5 V, along with gate leakage measured at V_{DS}= 1 V.

using the conventional structure of an AlN nucleation layer, superlattice strain relief layers, carbon-doped GaN, unintentionally doped (UID) GaN channel and an AlGaN barrier. A schematic cross-section of the structure is shown in Fig. 7.3. The HEMT devices and test structures were fabricated using mesa isolation, Ti-Al-Ni-Au Ohmic contacts, Ni-Au Schottky gate and Si_3N_4 passivation. Measurements are performed on single finger (SF) transistors (W_G= 100 μm, L_G= 1.5 μm, L_{SG}= 2.5 μm and L_{GD}= 12 μm). The DC I-V output characteristics gave an ID_{max} of 400 mA/mm at V_{DS}= 10 V , with a threshold voltage of -2 V and an off-state leakage in the order of 10^{-9} A/mm as shown in Fig. 7.4.

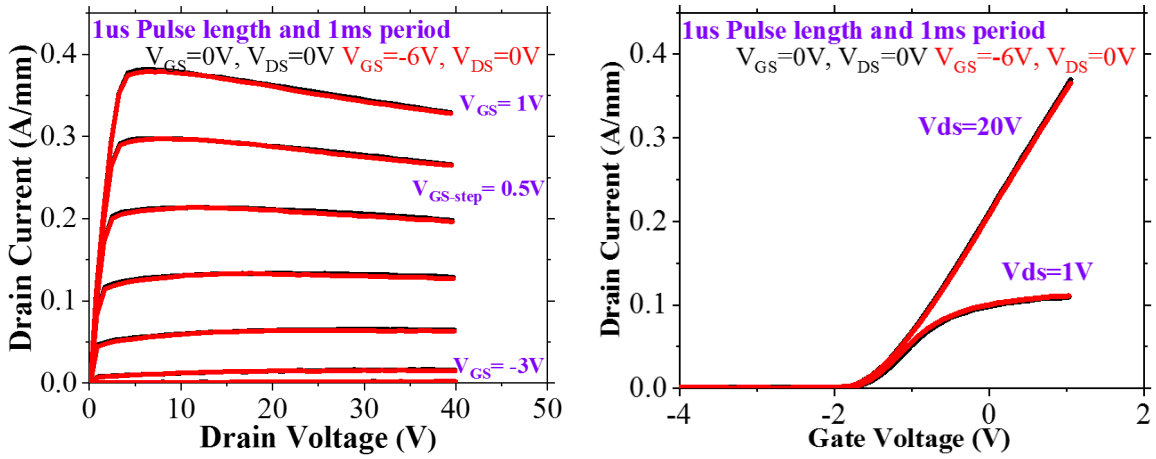

Figure 7.5: Pulse output and transfer characteristics of single finger device measured at steady state V_{GS}= 0 V and V_{DS}= 0 V is compared with gate stress V_{GS}= -6 V and V_{DS}= 0 V showing no knee walkout and any noticeable V_{th} shift.

The dynamic pulsed I-V output characteristics have been measured using Auriga pulse kit using 1 μs pulse length and 1ms pulse period. Steady-state pulse with V_{GS}= 0 V and V_{DS}= 0 V has been compared with gate stress V_{GS}= -6 V and V_{DS}= 0 V showing no knee walkout as seen in Fig. 7.5. This has been further verified using transfer characteristics measured at V_{DS}= 1 V and 20 V under exact same pulse conditions and no V_{th} shift has been observed.

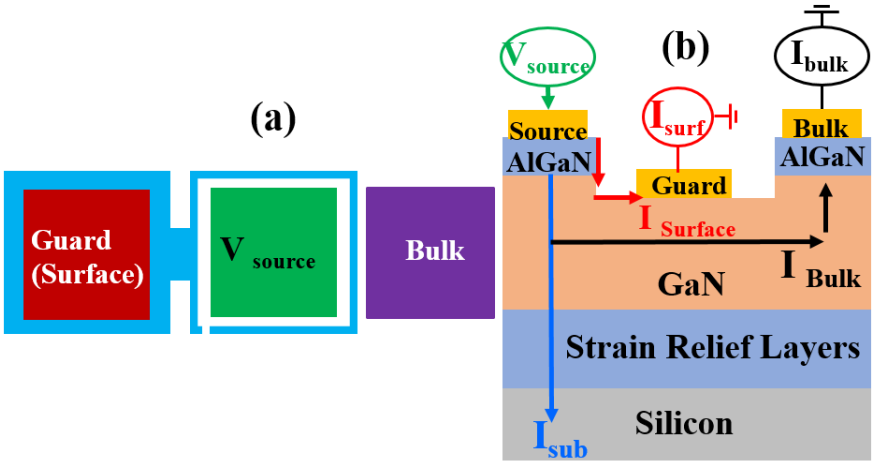

Figure 7.6: (a) Surface and buffer leakage test structure layout (b) schematic cross section under the test.

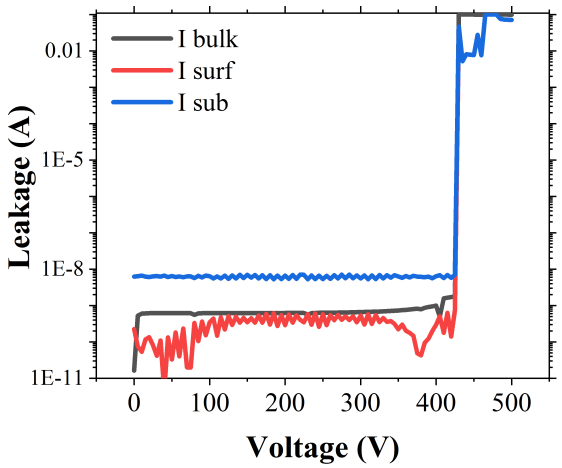

Figure 7.7: Surface and buffer leakage measurements after sweeping up to 500 V.

A customized test structure has been studied to separate the buffer and surface conduction mechanisms [188][189]. A top view and a schematic cross-section of the structure are shown in Fig. 7.6 (a). It consists of two ohmic pads on the top of the AlGaN layer (labeled as source and bulk contacts) separated by a mesa area. The third pad is connected to a guard ring around the

isolated source pad and sits directly on top of the etched GaN layer as shown Fig. 7.6(b). This pad is used to monitor any surface leakage path along the AlGaN/GaN surface as shown in the schematic. The bulk contact will measure any lateral leakage within the bulk of the epitaxy, and I_{sub} will measure the vertical leakage to the Si. The surface leakage is shown in Fig. 7.7 and it is in the order of 10^{-10} A being much lower than the lateral bulk leakage of about 1 nA when biasing the source pad up to 500 V ; note that this is a worst-case surface leakage current since the lateral field in the source/guard ring gap of up to 400 kV/cm is much higher than would be the case in the absence of a guard ring. It is quite clear that bulk lateral leakage exceeds surface leakage. The vertical substrate buffer leakage to the Si is an order of magnitude higher at 10^{-8}A.

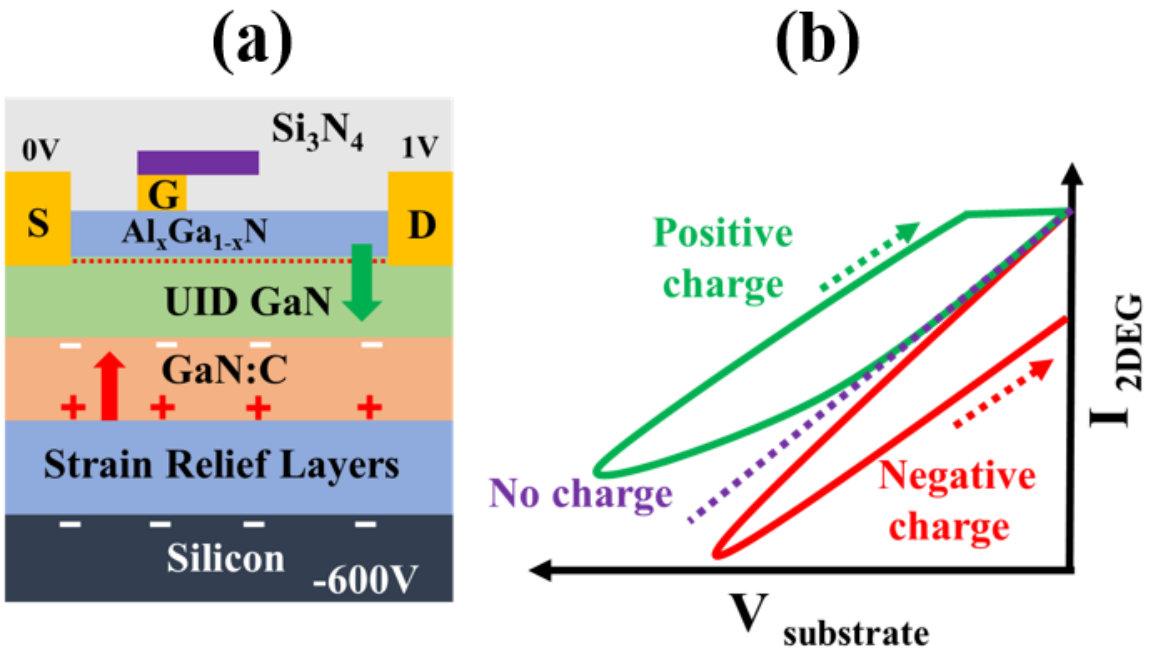

Figure 7.8: Back bias sweep schematic showing positive and negative charge storage upon deviation from stack capacitance and the effect on the structure.

To understand the long time-constant charge storage, substrate ramps have been used. The technique is now well established [187][190][191][192] and consists of using the silicon substrate as a back gate to control the channel conductivity. A small bias of 1 V is applied on the drain to monitor the channel conductivity while the substrate bias is ramped up to -600 V. The slow 1 V/s sweep rate has an effective time constant that is broadly similar to the charging/discharging time for C-doped GaN and gives a simple qualitative route to determining information about transport in the layers. Ideal stack capacitance is extracted based on physical thickness of layers which acts as basis for determining if there is any positive or negative charge storage. Any deviation from upwards from stack capacitance (no charge) is termed as positive charge while anything under is termed as negative charge as indicated in Fig. 7.8. Since the 2DEG channel remains on while the substrate is ramped, this technique is normally surface insensitive and gives information

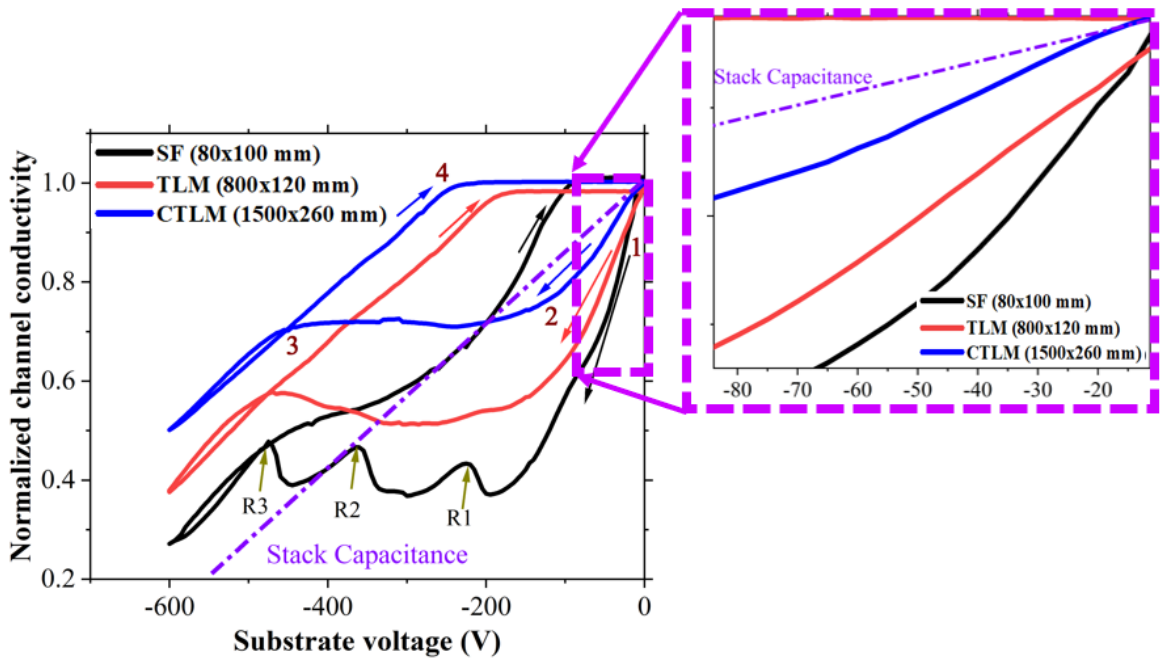

Figure 7.9: Normalized channel conductivity as a function of the substrate voltage of 3 structures with different active areas: single finger (SF of 80x100 μm), TLM (800x120 μm) and circular TLM (1500x260 μm). Sweep rate was 1 V/s. The dotted line represents the back-gate response for an ideal stack capacitance.

primarily about the buffer.

Bi-directional substrate ramp measurements were performed on 3 devices with 3 different active areas as shown in Fig. 7.9, along with the line corresponding to the buffer behaving as an ideal dielectric capacitor. The largest area device showed good behavior consistent with high-quality epitaxy [67]. However, a strong dependence on the area was observed with the magnitude of initial drop increasing with decreasing active area as illustrated in zoom out seen in Fig. 7.9. This could be explained by charge spreading laterally beyond the active area of the device as discussed later.

These indications of lateral charge flow beyond the device active area have been verified by performing a combination of on-resistance and step substrate bias stress of -600 V on a single finger device using a set of 8 independent adjacent devices. On-resistance of 8 single fingers (SF) transistors each with 100 μm width and 200 μm apart has been measured by repositioning the measurement probes. This was then followed by substrate bias of -600 V on the central device with a hold time of 1minute, immediately followed by a repeat of on-resistance measurements on the same set of 8 adjacent devices again by repositioning the probes. The sequence of the measurement is shown as shown in Fig. 7.10. The manual repositioning of the probes during the whole experiment took around 2 minutes. During the 1 minute voltage stress on the central device, all the adjacent devices were floating. The normalized on-resistance on all the devices

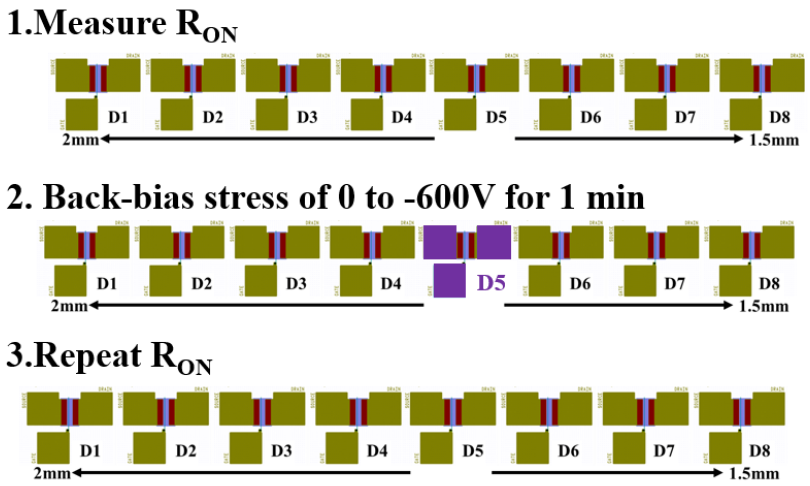

Figure 7.10: Measurement sequence for lateral charge spreading.

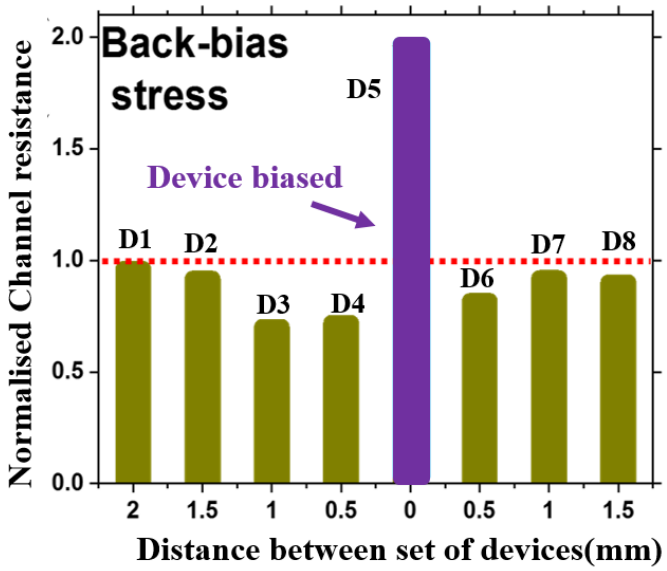

Figure 7.11: On-resistance of 8 single finger transistors each with 100 μm width was measured, followed by substrate bias stress on a central device (D5) stepping from 0 to -600 V and hold at -600 V for 1 minute. Immediately followed by the repeat of on- resistance on all 8 devices. Normalized channel resistance is plotted for all devices with stressed device D5 showing increase in resistance while a decrease in resistance for an adjacent device as far away as 2 mm.

before and after the stress is shown in Fig. 7.11. After stress, an increase in on-resistance was observed on the device under stress while the adjacent devices showed a decrease in resistance with devices up to 2 mm away showing an effect from the stress.

Dynamic R_{ON} measurements have also been used to evaluate the buffer by applying a worst-case off-state stress (V_{GS}= -6 V, V_{DS}= 100 V for 1000s) with the immediate change to

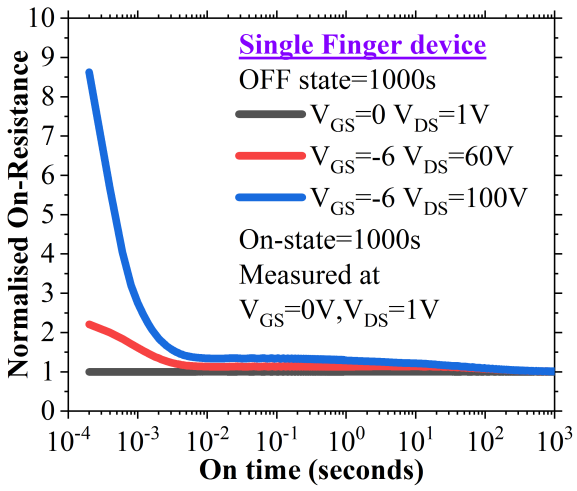

Figure 7.12: Normalized dynamic on-resistance following 1000s off-state stress for different stress values and recovery monitored at V_{GS}= 0 V and V_{DS}= 1 V for 1000 s.

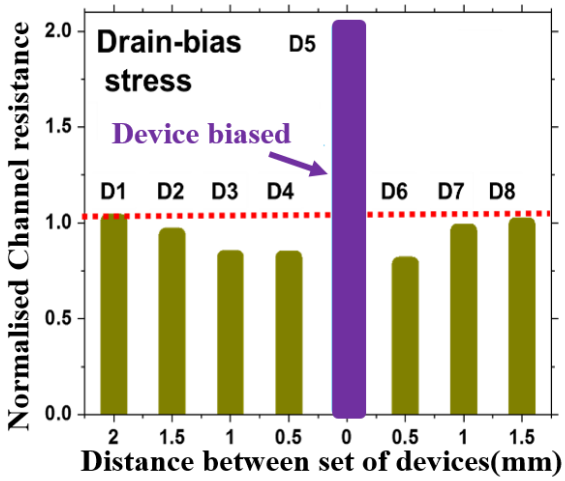

Figure 7.13: ON-resistance of 8 single finger transistors each with 100 μm width was measured, followed by drain bias stress on central device (D5) stepping from 0 to 100 V and hold at 100 V for 1minute, V_{GS} was kept at -6 V. Immediately followed by repeat of on-resistance on all 8 devices. Normalized channel resistance is plotted for all devices with stressed device D5 showing an increase in resistance while an decrease in resistance for adjacent devices as far away as 2 mm.

on-state (V_{GS}= 0 V and V_{DS}= 1 V) monitoring the recovery process for up to 1000 seconds giving information about the charge trapping and associated time constant. The impact of off-state drain stress shows negative charge storage in the device under stress as shown in Fig. 7.12, where it can be seen that there were two recovery time constants of <1 ms and ~50 s. To complement the substrate bias stress measurement of Fig. 7.11, we undertook similar measurements but applied a drain bias stress of V_{GS}= -6 V and V_{DS}= -100 V for 1min on the central device. The

normalized on-resistance on the set of 8 devices before and after the off-state drain bias stress is shown in Fig. 7.13 with the central device showing an increase and the adjacent devices showing a decrease in resistance. First the R_{ON} on all the devices were measured followed by drain stress on the device D5. This was followed immediately by R_{ON} measurements on D4, D3, D2, D1, D6, D7 and D8. The whole measurement process took few minutes to execute due to manual probing.

7.3 Result and Discussion

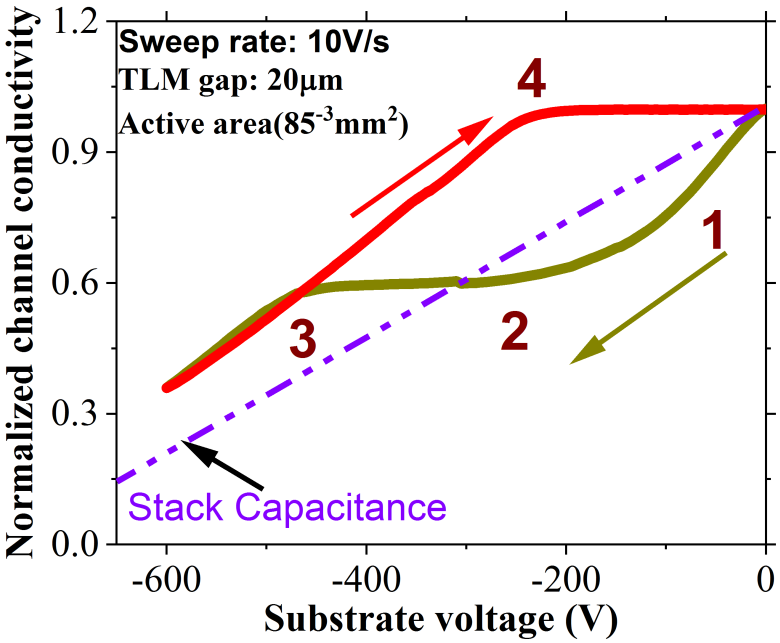

Figure 7.14: Shows the normalized channel conductivity of a large TLM structure as substrate bias is swept up to -600 V and back to 0 V with 10 V/sec sweep rate, the purple dotted line represents the stack capacitance.

Before considering the effect of the lateral conduction on adjacent devices, it is essential to note that based on the surface and the buffer leakage measurements obtained on the customized test structures in Fig. 7.7, the latreal leakage in these devices is mainly due to conduction through the buffer rather than on the surface. If we first consider the substrate ramp on the largest area device shown in Fig. 7.14 the device shows conventional behaviour that is quite typical of good quality epitaxy where there is vertical conduction in the epitaxy [67],[187]. This is because the linear device dimension of 1500x260 μm is comparable to the mm scale distance that we find charge flows laterally, so this device can be treated as showing 1D vertical conduction and lateral flow is relatively insignificant. The processes involved start with a vertical charge redistribution within the GaN:C layer which results in a dipole with a negative charge at the top of the GaN:C, and leading to a deviation below the capacitive line (region 1) in Fig. 7.14 with no leakage through

UID channel layer or the SRL and has been explained in Uren et.al [67]. With further increase in bias, the UID layer starts conducting by band-to-band transport generating a hole current, possibly involving a defect band in threading dislocations. This allows the formation of a positively charged layer at a blocking junction such as the GaN:C-SRL interface. This positive charge would be primarily the result of neutralization of ionized acceptors (region 2). At $VSub > |-450V|$, the SRL starts leaking and conducts electrons creating a resistive path through the structure while the holes remain stored giving positive charges (region 3). At the end of the return sweep, the 2DEG to GaN is forward biased, injecting electrons and neutralizing the positive charges (region 4). The buffer is neutral after removing the bias, showing no charge storage as evidenced by the absence of any change in drain current.

For the smaller devices, in Fig. 7.9, the magnitude of the initial drop in region 1 (VSub< |- 100 V|) during substrate ramp in Fig. 7.11 increases as the active device linear dimension decreases below the lateral distance that we observe for charge flow. This has previously been explained by hole charge flowing laterally within the buffer outside the active area defined in this case by the mesa [186],[187]. This lateral charge flow increases the effective area of the buffer layers of the device and hence their capacitance, changing the vertical potential distribution through the stack. This increases the electric field under the 2DEG and reduces the channel current especially for small area devices.

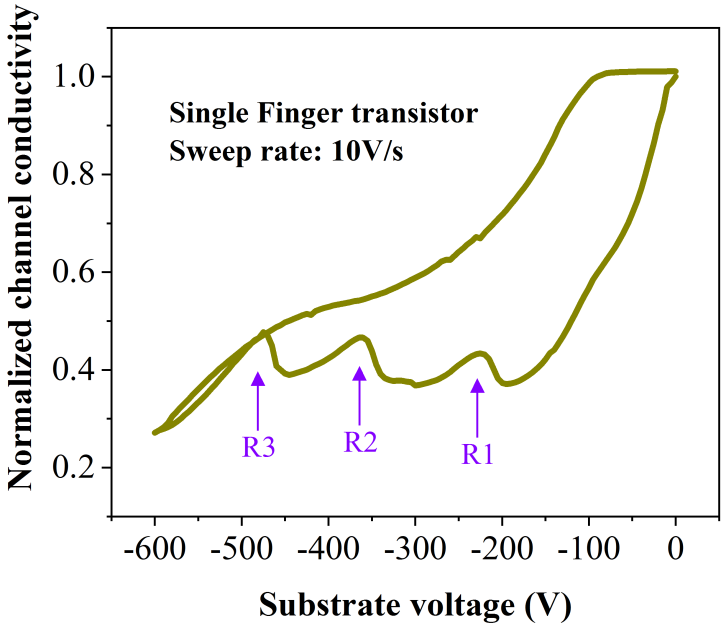

Figure 7.15: Normalized channel conductivity of a single finger transistor exhibiting ripples.

The unusual and interesting "ripples" seen in Fig. 7.15 (labeled as R1, R2 and R3) observed when ramping the substrates of single-finger transistors have been observed on all the devices

fabricated on this epitaxy and were reproduced in three separate device sets. They appear more prominently on small area devices and the voltage at which they appear is ramp rate dependent, making it possible that this is due to the sequential charging of layers in the super-lattice. Another possibility to explain this is the transport is controlled by a relaxation oscillation in the occupation of traps with charges stored locally until some critical density is reached at which it initiates a de-trapping phase. However, the presence of an oscillation suggests some gain within the de-trapping process, and its origin is still unknown.

For the largest devices, substrate ramps in Fig. 7.14 show evidence for the formation of negative and positive charges at the top and bottom of the carbon-doped GaN layer at substrate biases up to -600 V. Experimental evidence of these charges forming and spreading under stress beyond the active area can be clearly seen in the normalized channel resistance after step substrate bias up to -600 V on the central device as shown in Fig. 7.11. The resistance decreases around 25% on the adjacent unstressed devices while it shows the opposite behaviour on the stressed device. The mechanism for the device-to-device coupling can be assigned to a field induced dipole within the electrically isolated GaN:C layer as shown in Fig 7.16. The negative charge is attracted to the actively biased device, and the positive charges flow down to the blocking heterojunction and then laterally up to 2 mm in this case. The increase in resistance for the central device occurs because it has a small active area confining the negative charges under the central device. The decrease in R_{ON} on the adjacent devices is due to the spreading of the positive charges outside the active area of the stressed device during stress time. This lateral conduction may be associated with a pre-existing 2DHG at the heterojunction between the GaN:C layer and the SRL, but is more likely to be associated with bulk conduction in the GaN:C layer given the fact that the current only extends about a millimeter [138].

Under drain bias stress, the charge storage can be observed with a significant increase of up to 850% in on-resistance as shown in Fig. 7.12 which mostly recovers in 10ms, and this is assumed to be a surface virtual gate effect. The transients then show long recovery time constants lasting over 100 seconds, and this is the regime which is studied in the substrate bias induced bulk charging measurements in Fig. 7.9 and Fig. 7.11. Fig. 7.13 shows that similar slow bulk charging effects occur following normal transistor operation. An increase in the channel resistance on the central device and a decrease on all the adjacent devices is observed, which again can be explained by a dipole of positive and negative charged regions forming in the buffer during step stress. The increase in R_{ON} for the central device occurs by the formation of a negatively charged region in the gate-drain gap [67], with a leakage path between the drain and the GaN:C layer helping holes to flow laterally outside the active area, affecting the conduction of the adjacent devices. The voltage drop across the SRL results in a positive charge under the device and hence a decrease in R_{ON} for the adjacent devices.

This lateral charge spreading during on-wafer stress testing might have a significant impact during on-wafer reliability characterization due to cross-coupling between devices when they

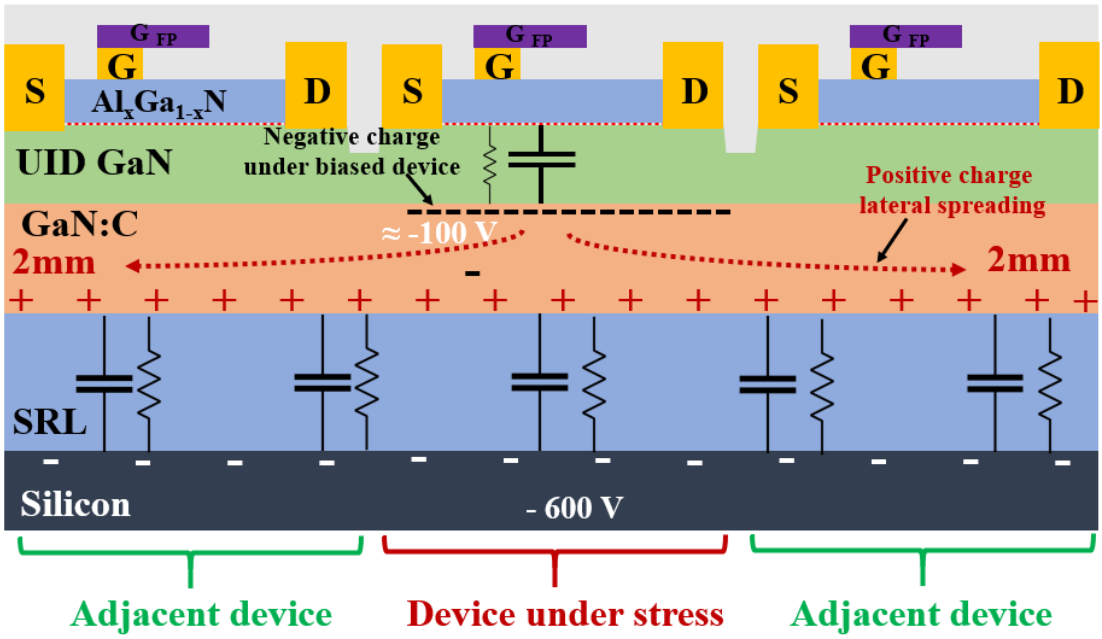

Figure 7.16: Schematic illustration of the lateral charge spreading showing the device under stress (central) and the adjacent devices.

share the same epitaxy. Substrate ramps and dynamic R_{ON} are routinely used methods for wafer level reliability assessment, and hence lateral charge spreading beyond the active area together with long time memory effects, could lead to erroneous results. Device coupling and time dependence further make the system integration harder with stress impacting adjacent devices.

7.4 Conclusion

Experimental evidence of lateral charge conduction in the buffer of GaN on silicon is shown. Lateral conduction in the carbon doped GaN layer has been proposed to be the mechanism for this device-to-device coupling. Substrate ramps have been used to evaluate the buffer showing positive and negative charge storage, and customized surface and buffer leakage test structures helped to separate the different leakages. The long trap time constants upon stress mean that prior test history can affect the performance of adjacent untested devices. This could have a significant effect for on-wafer reliability assessment, or for system integration where devices share the same epitaxy as would be required for integrated drivers and other applications.

CHAPTER 8

NEXT GENERATION GAN RF DEVICE: GAN-ON-DIAMOND

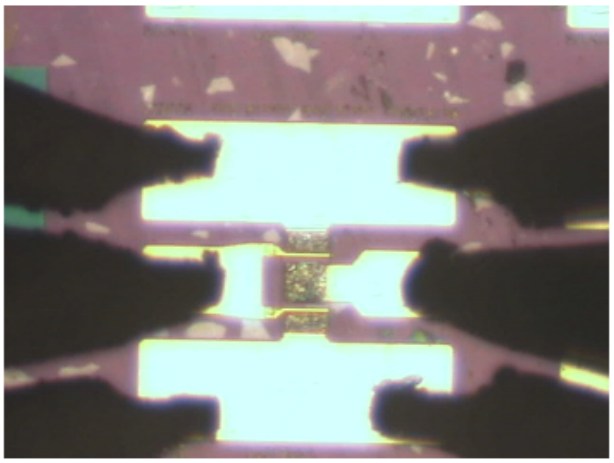

Figure 8.1: A GaN-on-diamond device probe using GSG probe is shown here.

This chapter explores GaN-on-diamond as alternative for future RF devices. So far we have shown the buffer being main issue due to defects and doping issues. This work evaluates impact of buffer thinning after the growth and deposition of diamond. In spite of thinning of buffer the electrical performance has remained intact while diamond has aided the thermal performance. Minimal trapping and excellent large signal RF performance at 1 GHz for ultra-thin GaN-on-diamond technology has been demonstrated. Maximum Power output of 23 dBm with gain of 18 dB and power added efficiency of 50.26% has been measured at 1 GHz in CW mode which improved marginally for pulse mode. Minimum CW-Pulsed RF dispersion observed can be explained by experimentally measured excellent thermal resistances of 9 ±1 K/(W/mm) using

Photoluminescence (PL). Fitting experimental data with finite element simulations gave effective thermal boundary resistance ($TBReff$) of 13 m^2K/GW which is crucial parameter in improving heat extraction from devices. These results demonstrate successful integration of ultra-thin GaN-on-diamond bringing diamond closer to the active region of the device making it thermally efficient without compromising electrical switching performance which is shown by minimal trapping. Obtained electrical and thermal results puts this work among the state-of-the-art RF devices. PL measurements has been performed by Callum Middleton and published in [193]. Sample (E-654) as shown in Fig.8.1 has been provided by Element 6 and has been processed at University of Sheffield. Mike Casbon from Cardiff university assisted during RF measurements at Cardiff university.

8.1 Introduction

High breakdown field and high saturation velocity together makes Gallium Nitride (GaN) perfect material for high RF power density devices and with added advantage of wide bandgap allows it to operate at higher temperatures [194]. Wu *et. al* demonstrated the first RF power device of 1.1 W/mm at 2 GHz with a power added efficiency of 18.6% since for an AlGaN/GaN HEMT in 1996 and since then there has been rapid progress thanks to advancement in epitaxy design and processing [195]. Recently Xing *et. al* demonstrated record high current gain cut off frequency (f_t) of 250 GHz with maximum drain current of 2.6 A/mm for GaN on silicon [196]. These excellent RF performances brings GaN to the forefront of next generation of devices however, self-heating effects has been one of the major limiting factors. Several techniques like flip chip bonding or use of good thermal conductivity substrate like silicon carbide has been used to tackle thermal challenges so far. Dumka *et. al* demonstrated GaN HEMTs on diamond, the highest known bulk thermal conductivity, as an alternative for better thermal management [197].They demonstrated over 7 W/mm output power density at 10 GHz along with the peak power added-efficiency of over 46% and power gain over 11 dB for 2 x 100 μm gate-width HEMTs at 40 V drain bias and since then several reports have been published utilizing GaN-on-diamond for RF devices.

A standard GaN epitaxy is grown mostly on foreign substrates which requires additional accommodation layer. These layers although aid in growth they also add extra thermal resistance which in turn makes the total effective thermal resistance of the entire stack much higher. Apart from thermal resistance, electrically they also are source of defects which can have severe trapping and reliability issues as shown in earlier chapters. Therefore aim of this study is to etch away all these strain relief and extra layer thus reducing not only the total effective thermal resistance but also getting rid of majority of defects and possible trap sites. Making GaN ultimately thin enough to allow diamond to sit closer to region of maximum heating as shown in Fig.8.2.

In this work demonstrate ultra-thin GaN (354 nm)-on-diamond which brings diamond closer

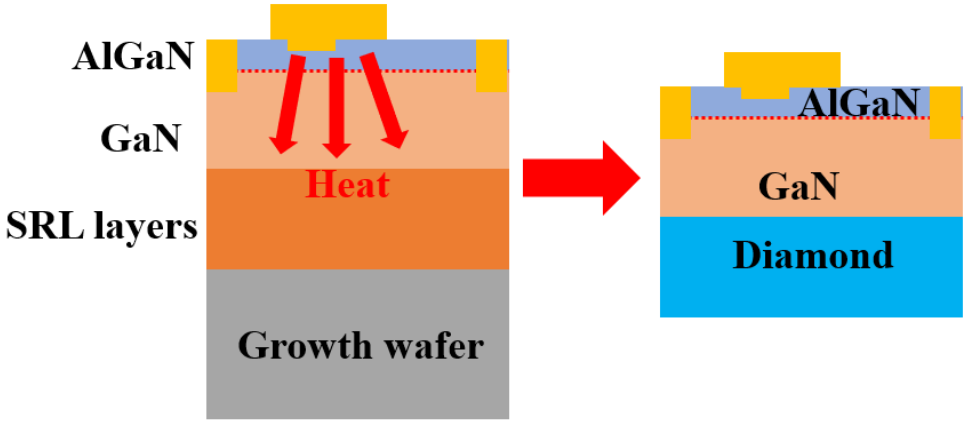

Figure 8.2: The figure here shows typical heat spreading in GaN RF device. In this work growth wafer and SRL is removed with further thinning down the GaN to deposit diamond and bringing it closer to heat zone.

to the active region of the device making it thermally efficient. In-spite of thinning down the GaN, the quality remains good which has been evaluated using gate and drain lag showing minimal trapping. Large signal RF measurements have been performed at 1 GHz showing excellent performance with minimum CW-Pulsed dispersion further validating good thermal management. Using Photoluminescence (PL) thermal resistance has been measured experimentally giving low value of 9 $\pm$1 K/(W/mm). This work demonstrates successful integration of ultra-thin GaN-on-diamond and exhibits performance which is in line with state-of-the-art devices.

8.2 Sample details and measurements

Standard GaN on Silicon epitaxy is used for this process. The first step involves etching the silicon and strain relief layer underneath GaN HEMT using a dry etch process as shown in Fig.8.3. The main objective of this study is to keep the GaN as thin as possible without any compromise to device performance. GaN layer thickness here is kept at 354 nm to keep the diamond closer to the active channel. The top of part of AlGaN-GaN HEMT has been kept untouched but all the nucleation and strain relief layer are removed. A 17 nm thick silicon nitride interface layer is grown on the remaining GaN which acts as a seed for diamond growth during the CVD process.

The first step in device processing is MESA etch using RIE to etch away 2DEG, followed by the ohmic contact process. Standard Ti/Al/Ni/Au ohmic metal stack followed by RTA has been used. Blanket PECVD silicon nitride passivation followed next. Pad opening for Gate metal followed by Ni/Au Schottky contact for gate metallisation as shown in Fig.8.4. Further details of growth and processing can be found in [198]. To enable pulse and RF measurements GSG probe-able devices have been fabricated. Devices with a gate width of 2x 50 μm, gate length of

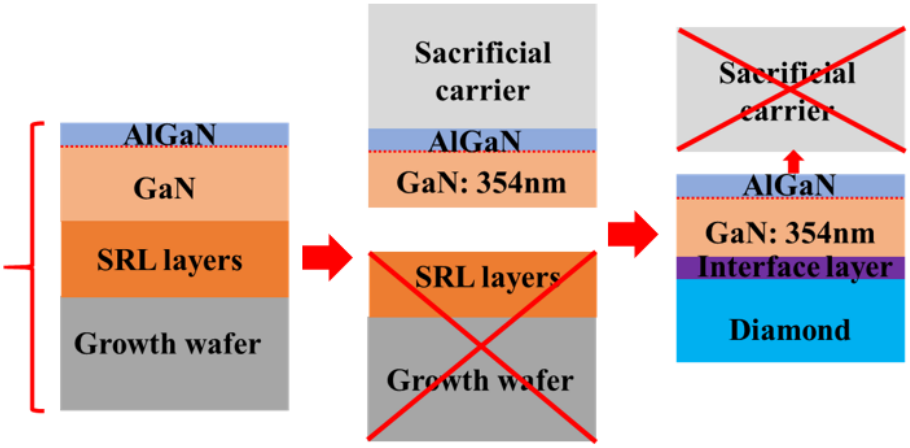

Figure 8.3: Shows the typical GaN on silicon stack followed by addition of carrier wafer and removal of substrate and SRL layer. The next shows removal of carrier wafer and growth of diamond using interlayer which in this case is $Si_3\ N_4$.

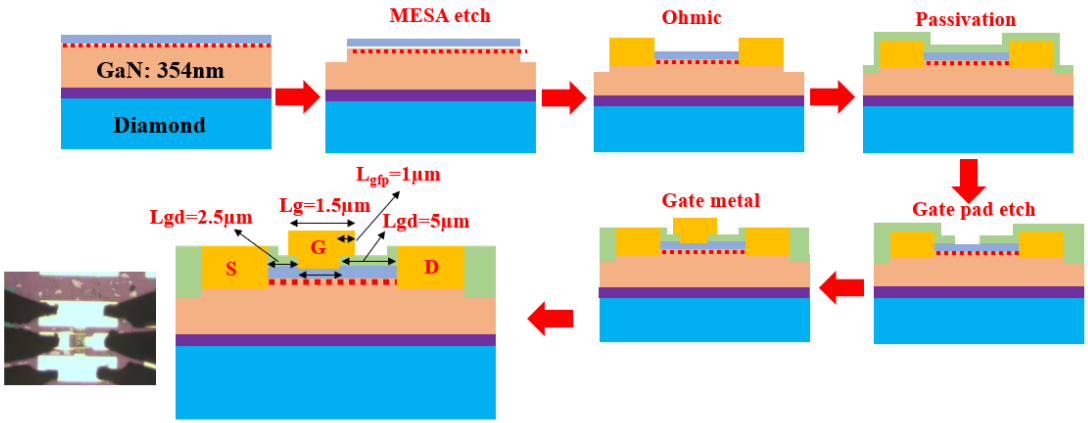

Figure 8.4: Shows fabrication process step starting from MESA etching to complete device. The device dimensions are also represented along with the device under test.

1.5 μm, source-gate separation of 2.5 μm, Gate-drain separation: 3, 5 and 7 μm with Gate-FP extension: 1 μm has been fabricated. In this study device with gate-drain of 7 μm has been used.

8.3 Result and Discussion

8.3.1 DC and Pulse measurements

DC output characteristics are shown in Fig. 8.5 with a maximum I_{DS} of 0.55 A/mm measured at V_{GS}= 1 V up to V_{DS}= 40 V. A threshold voltage (V_t) of -3.2 V and off-state leakage on the

order of 10^{-6} A/mm have been measured. Thermally induced current slump could be mitigated by using short pulse lengths. This has been evaluated using pulsed measurements with 200 ns pulse length and 1 ms period from a quiescent point of V_{GS} = 0 V and V_{DS} = 0 V, which corresponds to a stress-free steady state, show small improvement with I_{DS} increasing to 0.6 A/mm (as shown in Fig.8.5). The 5% reduction in maximum I_{DS} between DC and pulse indicates that the thermal droop associated with self-heating is small. The other possible reason for current slump either in the knee region or high field could be surface or buffer traps. Several reports in GaN HEMTs has shown severe current collapse and knee walkout due to trapping. These traps can be evaluated using varying gate and drain bias conditions. With any traps under the gate will create depletion region around leading to shift in threshold voltage (V_t).

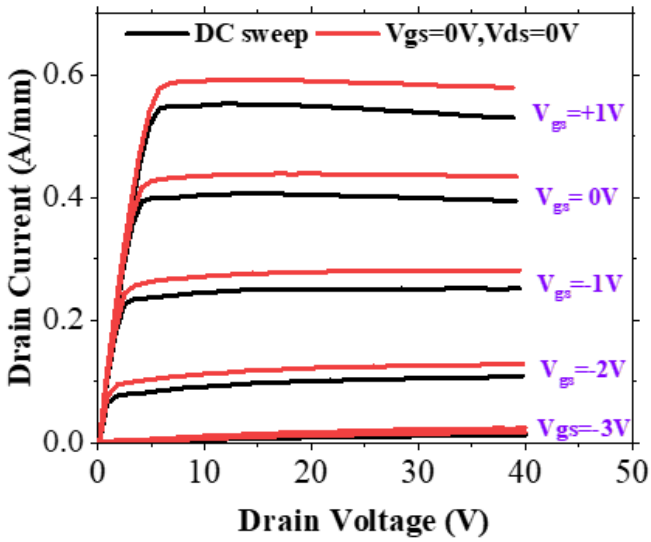

Figure 8.5: Shows DC output characteristics with V_{GS} varying from -3 V to +1 V overlaid with steady state pulse measurements done at V_{GS}= 0 V, V_{DS}= 0 V.

Similarly, any traps in between the gate-source or gate-drain region will impact the access resistance thus impacting the measured transconductance (g_m) of the device. Gate lag (V_{GS} = -6 V, V_{DS} = 0 V) stress using 200 ns pulse length and 1 ms period when compared with steady state pulse (V_{GS} = 0 V, V_{DS} = 0 V) shows negligible change in knee (as shown in Fig.8.6 (a)). This has been further confirmed by measuring transfer characteristics using same pulse conditions showing almost no shift in V_t (as shown in Fig.8.6(b)). Same pulse conditions drain lag stress measurements with (V_{GS} = -6 V, V_{DS} = 40 V) compared to steady state shows minimal trapping in access region with small change in transconductance which can also be seen in transfer characteristics as shown in Fig.8.7(a) and (b). Stable knee with no shift in V_t or changes in transconductance (g_m) demonstrates good quality of GaN buffer in device and suggest that no compromise has been made with thinning down the buffer in terms of electrical performance.

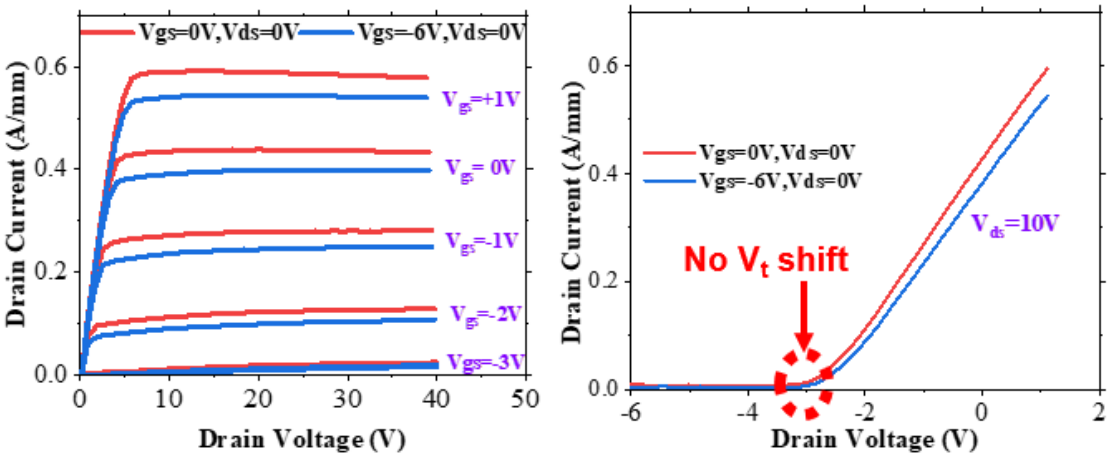

Figure 8.6: Shows gate lag pulse measurements done at V_{GS}= -6 V, V_{DS}= 0 V, both output and transfer characteristics (at V_{DS}= 10 V) are shown, almost no V_t shift can be seen.

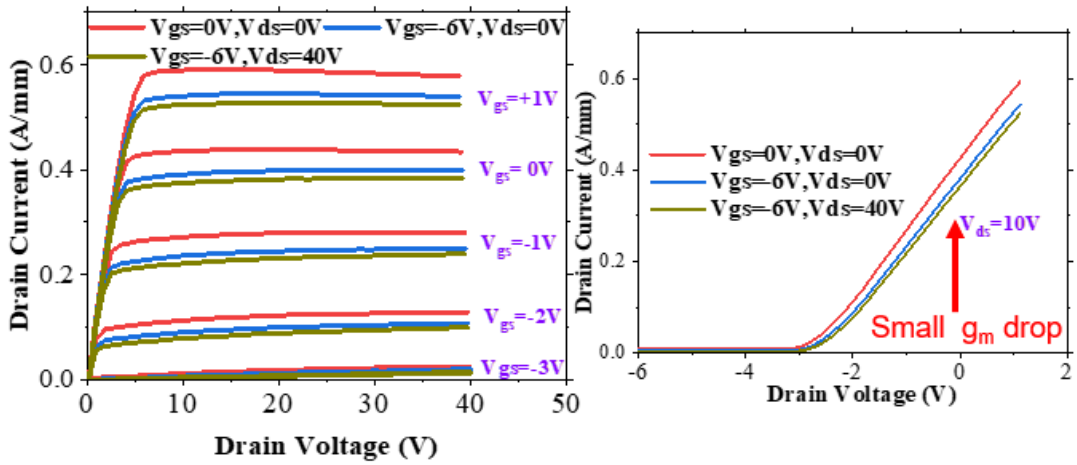

Figure 8.7: Shows drain lag pulse measurements done at V_{GS}= -6 V, V_{DS}= 40 V, both output and transfer characteristics (at V_{DS}= 10 V are shown, small g_m drop can be seen in transfer curve.

8.3.2 RF measurements

Large signal RF measurements have been performed using a VTD SWAP-X402 receiver and a high-speed FET switch which modulates the drain bias during DC while an external modulator with high-speed RF switches has been used to provide the RF pulse. This provides an ability to independently switch the RF and DC drain bias between CW and pulse without making any changes to the sampling regime [199].

Load pull measurements: RF knee walkout at 1 GHz has been measured in terms of RF fan diagrams. At this relatively low frequency (1 GHz) the effect of the output capacitance can

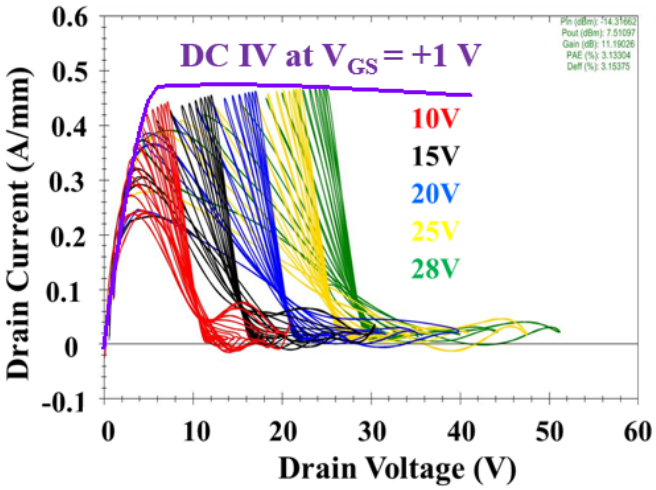

Figure 8.8: Shows RF fan diagrams measured at 1 GHz under different drain bais pints of 10 V, 15 V, 20 V, 25 V and 28 V. The DC IV measured at V_{GS} = 1 V is also overlaid.

be neglected. The fan diagrams display the same operating area for the device as pulsed IV at a given operating bias point and is measured by varying the RF load with the input power sufficient for saturated operation. This combination of RF load pull and IV waveform measurement allows the realisation of first pass design as devices can be tested under the exact conditions found in the PA operating mode. Operating bias is measured at drain bias voltage of 10 V, 15 V, 20 V, 25 V and 28 V. The DC IV sweep measured at V_{GS} = 1 V is overlaid to compare the dispersion. The load-lines show a quite modest knee walkout, even at 28 V drain bias and only limited knee walkout is observed indicating well controlled trapping even under RF operation as shown in Fig.8.8. Decent pinch off behaviour can also been seen at the tail end during high off state bias. Effect of steady knee under RF can also be seen with maximum output power increasing with drain bias, while the maximum efficiency is relatively constant as shown in Fig.8.9. It is also clear that the small device size is not ideal as the optimum high load value is taking the measurements into compression beyond 20 V drain bias.

CW and Pulsed RF: Large signal CW measured at 1 GHz exhibits a maximum power output of 23.40 dBm (2.18 W/mm) with a power added efficiency of 50% and a gain of 17.5 dB. To understand the thermal effect pulsed RF have been performed with 10 μs pulse length and 200 μs period. Under pulse RF these values marginally improved with maximum power output of 23.58 dBm with power added efficiency of 52.22% and gain of 17.55 dB which indicated good thermal behavior (as shown in Fig.8.10). The pulse length used during RF measured has been kept at 10 μs.

To give a practical assessment of the device performance the measurements has been preformed in class F of operation with a drain bias voltage of 28 V and I_d= 5 mA as shown in Fig.8.11. Good performance with output power of 2.69 W/mm with PAE of over 61.07%. The value for

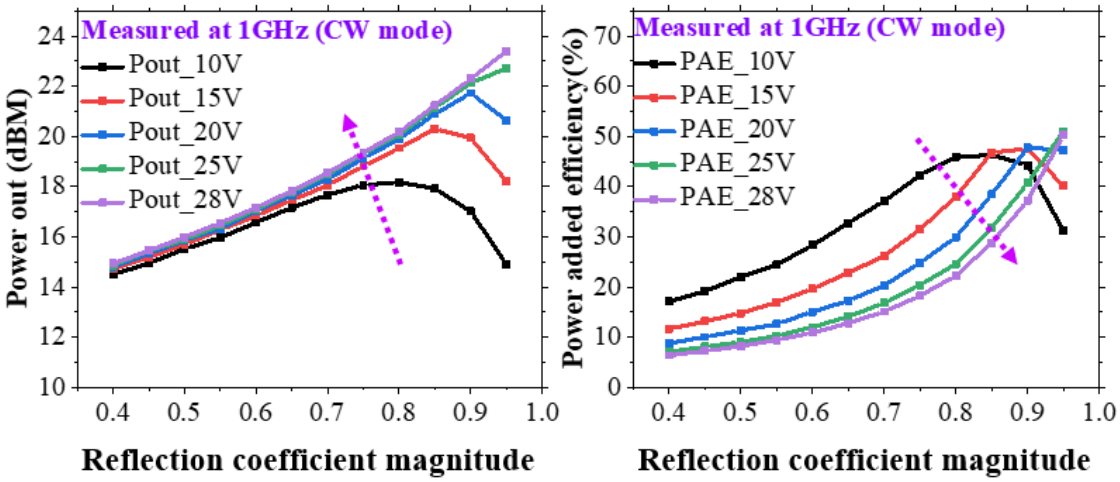

Figure 8.9: Shows variation of output power and PAE against load and drain bias voltage.

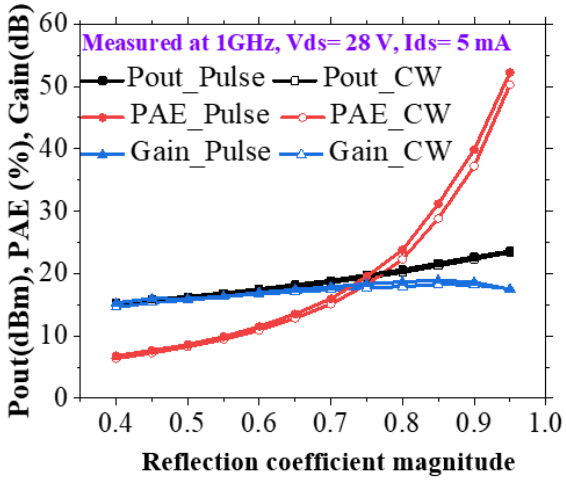

Figure 8.10: Shows variation of output power and PAE against real load at V_{DS}= 28 V and I_{DS}= 5 mA measured at 1 GHz.

pulsed RF under class F also remains similar with Pout of 2.72 W/mm and PAE of 61.07%. The gain during both the case remains at 21.16 dB.

Thermal study on this exact same device has been preformed by Callum et. al. using Photoluminescence (PL) to determine the GaN channel surface temperature [193]. A HeCd laser source (325 nm) with a laser spot size of less than 1μm size has been used. 2.61 ±0.03 K/(W/mm) temperature change in the device has been measured at distance 2μm from the gate edge with the nearest accessible area at the field plate edge as shown in Fig.8.12. Experimental data fitted to finite element simulations were performed showing thermal resistances of 9±1 K/(W/mm) comparable to reported 10±1 K/(W/mm) GaN-on-diamond values for much thicker GaN layers [200][201].

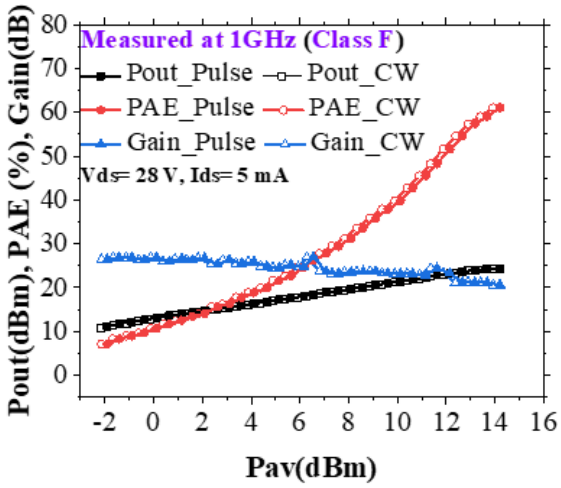

Figure 8.11: Shows variation of output power and PAE against available power at V_{DS}= 28 V and I_{DS}= 5 mA measured at 1 GHz for class F operation.

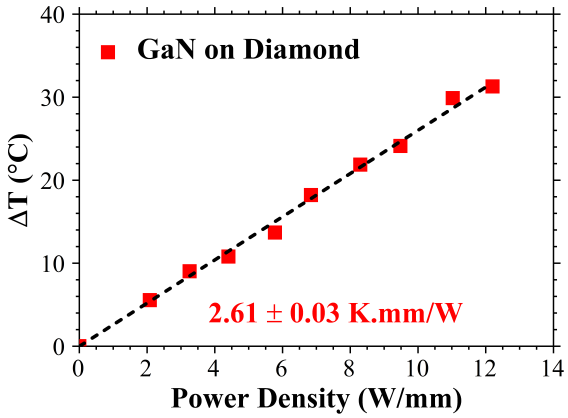

Figure 8.12: Shows temperatures measured 2 μm from the gate edge along with theoretical linear fits [193].

8.4 Conclusion

In summary, these results are encouraging and show evidence that successful integration of GaN-on-diamond is possible. Use of ultra-thin GaN allows the diamond to be closer to the active region of the device making it thermally efficient. The good electrical switching performance means the quality of GaN is not compromised as well. Excellent electrical and thermal performance puts this work among the state-of-the-art RF devices. This demonstration suggests that future GaN RF device might take this approach for better thermal and electrical performance.

CHAPTER 9

NEXT GENERATION RF DEVICE: GALLIUM OXIDE AN EMERGING NEW WIDE BANDGAP

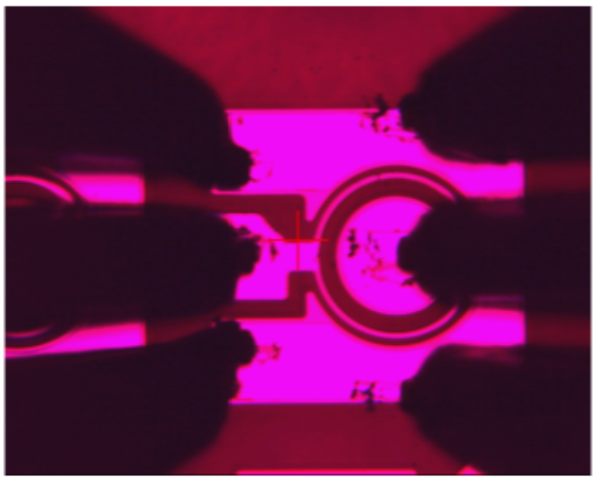

Figure 9.1: Shows microscope image of the device under test, GSG probes where used to make contact with devices to enable pulse measurements.

So far in thesis GaN and its issues have been discussed, while literature review β-Ga_2O_3 was presented for in chapter 2. This chapter explores this wide bandgap material which could be an alternative choice for future RF device. A β-Ga_2O_3 MOSFET under test is shown in Fig.9.1. In this chapter the thermal resistance is calculated based on a combination of electrical device performance and thermal simulations. Later β-Ga_2O_3 MOSFET detailed electrical study is presented showing good pulse performance with minimal trapping which makes these results encouraging given this is a relatively new technology with process and material

still evolving, however, the DC and RF performance has been found to be severely limited due to poor thermal conductivity. This chapter has significant content reproduced from my published work, with permission from IEEE [202]. Some additions have been made and all the figures have been reproduced with some reused after permission from IEEE.

9.1 Sample details and measurements

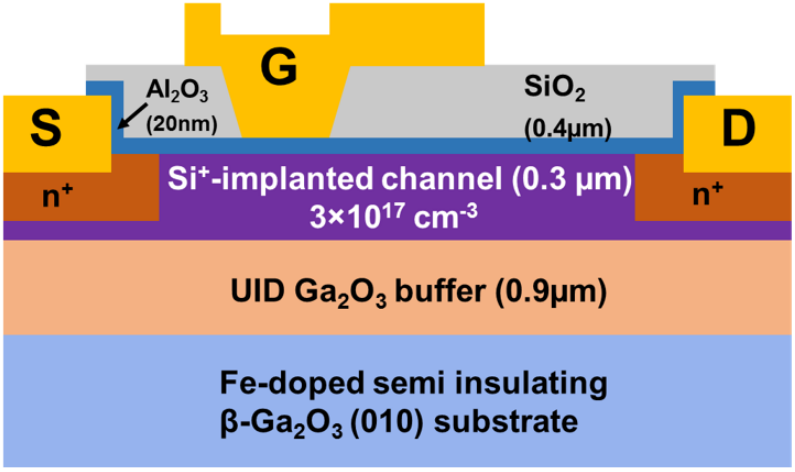

Figure 9.2: Schematic cross-section of the field-plated MOSFET used in this study is shown here.

Devices used in this study were grown on an Fe-doped semi-insulating β-Ga_2O_3 (010) substrate by ozone MBE with a 1.2 μm unintentionally-doped (UID) epilayer as the starting material [203],[204]. The MOSFET channel was defined by selective-area Si ion implants at multiple energies to form a 0.3-μm-deep box-like profile with a plateau concentration of 3x10^{17} cm^{-3}. Source and drain contacts were also doped by Si ion implantation (5x10^{19} cm^{-3}). Capless implant activation annealing was performed at 950° for 30 min in N_2 ambient. A metal stack of Ti (20 nm)/Au (230 nm), which was annealed at 470° for 1 min, was used as the ohmic electrode. A 20 nm Al_2O_3 gate dielectric was then deposited at 250° by plasma atomic layer deposition, on top of which a 0.4 μm SiO_2 dielectric was formed by chemical vapor deposition. CF4 RIE gate recess through the Si_{O2} was followed by depositions of Ti (3 nm)/Pt (12 nm)/Au (280 nm) for the gate electrode and Ti/Au for a gate-connected field plate. The device had a gate length of 2 μm, gate width of 500 μm, gate-source spacing of 5 μm, gate-drain spacing of 15 μm, and field plate length of 1 μm [205]. The cross-section of the device is shown in Fig.9.2.

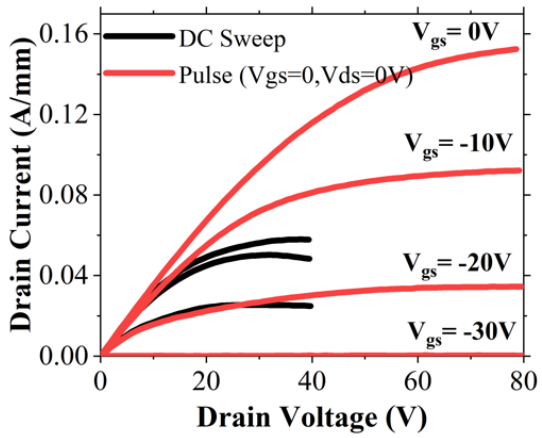

Figure 9.3: DC output characteristics with V_{GS} from -30 V to 0 V and V_{DS} up to 40 V, with droop observed due to self-heating at higher drain bias. Pulsed IV from a quiescent bias of V_{GS} = V_{DS} = 0 V up to V_{DS} = 80 V with 1 μs pulse length and 1 ms period is overlaid.

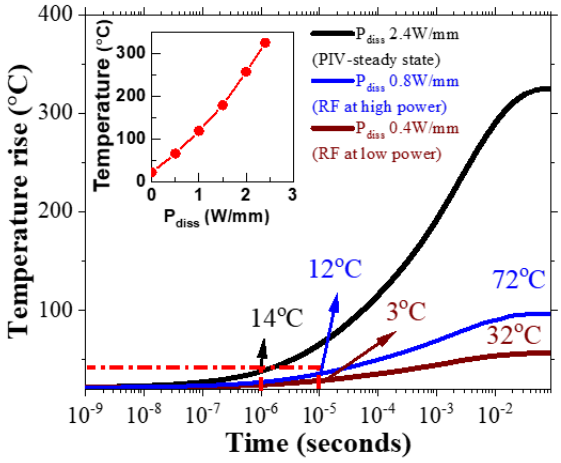

Figure 9.4: Single pulse thermal simulation showing the transient peak channel temperature at V_{DS} = 40 V and power dissipation of 2.4, 0.8 and 0.4 W/mm at 25°C ambient temperature. Durations of 1 μs and 10 μs that match the pulsed IV and pulsed RF measurement conditions, respectively, are highlighted. The simulated steady state peak channel temperature rise versus power dissipation is shown as an inset.

9.2 Result and Discussion

DC output characteristics are shown in Fig.9.3 with a maximum I_{DS} of 58 mA/mm, a threshold voltage (V_{TH}) of 28 V, and off-state leakage on the order of 10^{-9} A/mm. Pulsed measurements with 1 μs pulse length and 1 ms period from a quiescent point of V_{GS} = 0 V and V_{DS} = 0 V, which corresponds to a stress-free steady state, show excellent performance with the maximum I_{DS}

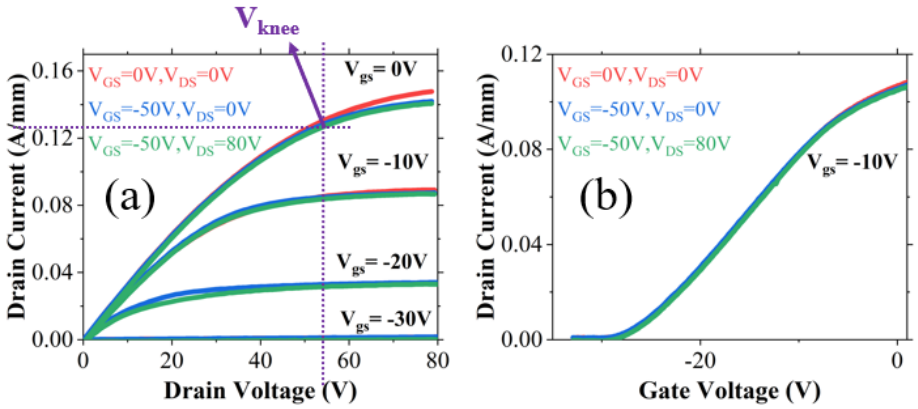

Figure 9.5: (a) Gate and drain lag measurements comparing different quiescent biases, with 1 μs pulse length and 1 ms pulse period: unstressed (red line) V_{GS} = 0 V, V_{DS} = 0 V; gate lag (blue line) V_{GS} = -50 V, V_{DS} = 0 V; and drain lag (green line) V_{GS} = -50 V, V_{DS} = 80 V. (b) Gate and drain lag measurements comparing different quiescent biases, showing almost no shift in threshold voltage and no drop in transconductance at V_{DS} = 40 V.

increasing to 150 mA/mm. Pulsed operation allowed DC measurements to be extended from V_{DS} = 40 V up to V_{DS} = 80 V without inducing thermal breakdown.

9.2.1 Pulse I-V measurements

To evaluate the reduction in channel temperature for pulsed versus steady state operation, the transient thermal response was simulated using a 3-D ANSYS finite element model, with dimensions matching the measured device and channel Joule heating distribution obtained from a drift-diffusion model simulated using Silvaco ATLAS [206]. In the thermal simulation anisotropic thermal conductivities of $23.4x(300/T)^{1.27}$ W/m.K and $13.7x(300/T)^{1.12}$ W/m.K in the out-of-plane [010] direction and in-plane [001] direction, respectively, were used [98]. Thermal conductivity values of 3 W/m.K, 1 W/m.K and 315 W/m.K were applied to the Al_2O_3 , SiO_2 and gold pad layers respectively; standard bulk specific heat capacity and density values were used for all materials. An isothermal boundary condition was applied to the back of the 600-μm-thick Ga_2O_3 substrate. Thermal simulation results shown in Fig.9.4 illustrate that the peak channel temperature is predicted to reach 39°C after a duration of 1 μs and then rise to 325°C after about 100 ms at a constant power dissipation (P_{diss}) of 2.4 W/mm, which corresponds to the DC condition of V_{DS} = 40 V and I_{DS} = 0.058 A/mm in Fig.9.3. For the pulsed IV measurement, the worst-case temperature rise at V_{DS} = 80 V and I_{DS} = 150 mA/mm was about 200°C. The self-heating induces the severe thermal droop observed in the DC IV curve of Fig.9.3.

Thermally induced current slump could therefore be mitigated by using short pulse lengths; however, traps in the devices could then potentially result in significant current collapse and

knee walkout due to surface or buffer traps, with well-known examples for GaN high electron mobility transistors [207][208][26]. The temporal charging of these traps will be a function of varying gate and drain potentials, with charge trapping under the gate leading to a threshold shift and trapping in the gate-source or gate-drain region a drop in transconductance. Using 1 μs pulse length and 1 ms period for gate lag (V_{GS} = -50 V, V_{DS} = 0 V) and drain lag (V_{GS} = -50 V, V_{DS} = 80 V) quiescent points, almost no drop in output conductance was observed, as illustrated in Fig.9.5(a). This has been further confirmed by using the same quiescent bias conditions and measuring transfer characteristics at V_{DS} = 40 V, under which the device showed almost no shift in V_{TH} and minimal drop in transconductance as shown in Fig.9.5(b). Hence there is no significant trapping in the gate dielectric or Ga_2O_3 bulk and only minimal surface trapping for these devices. Trapping is a major challenge in the device community and these results are encouraging given this is a relatively new technology with process and material still evolving.

9.2.2 RF measurements

Large signal CW and pulsed RF measurements have been performed based on the stable pulse performance. A large signal measurement system based on a VTD SWAP-X402 receiver has been used. A high-speed FET switch modulates the drain bias during DC while an external modulator with high-speed RF switches has been used to provide the RF pulse [209]. This provides an ability to independently switch the RF and DC drain bias between CW and pulse without making any changes to the sampling regime. At V_{DS} = 40 V and I_{DS} = 5mA (0.4 W/mm power dissipation) for 10 μs duration pulsed RF, a maximum Pout of 0.13 W/mm with a PAE of 12% and a drain efficiency up to 22.4% along with a maximum gain of 4.8 dB were obtained at 1 GHz as shown in Fig.9.6. By comparison, CW large signal performance dropped to a peak Pout of 0.11 W/mm with 19.5% drain efficiency and 9.1% PAE as is also shown in Fig.**??**. The difference in RF performance is due to self-heating: based on the thermal resistance extracted from simulation (Fig.9.4), the predicted temperature is 58°C during CW RF and 28°C for pulsed RF. The forward available power (Pav) rather than input power into the device (Pin) is plotted since the high reflection at the input in these long gate length devices makes Pin noisy and error prone. Rollover in the PAE and degradation in gain beyond an available power of 22 dBm were the reasons to limit the sweep at 22 dBm. These PAE and drain efficiency values exceed those reported by Green *et al.* for CW RF measurements at 800 MHz [206].

Measurements of CW and pulsed RF at higher operating power and elevated temperature have been performed to evaluate the performance degradation as is shown in Fig.9.7(a) and (b). Operating power of V_{DS} = 40 V and I_{DS} = 10mA (0.8 W/mm power dissipation) has been used to compare the performance degradation. In all cases CW operation showed a lower gain, PAE, drain efficiency and Pout than pulsed operation. Despite the fact that the load-pull was optimized for maximum power, meaning that the load is somewhat different in each case, there is a fairly consistent drop in performance with increasing channel temperature. Comparisons of CW and

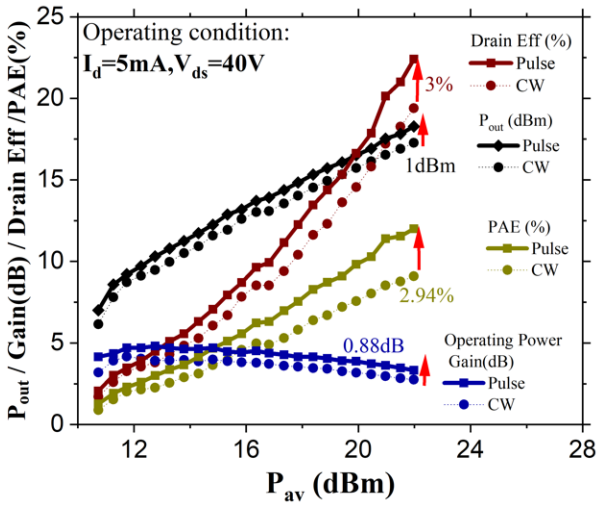

Figure 9.6: Pulsed and CW large signal measurements at 1 GHz with input available power sweep up to 22 dBm, measured at V_{DS} = 40 V with I_{DS} = 5mA.

pulsed measurements at V_{DS} = 40 V and 25°C but different bias currents (resulting in power dissipation increasing from 0.4 W/mm to 0.8 W/mm) showed that the difference in P_{out} increased from 1.01 to 1.89 dBm and the gain difference increased from 0.64 to 1.6 dB, but the change in PAE was similar at 2.92% and 3.62%. RF measurements performed at an elevated temperature of

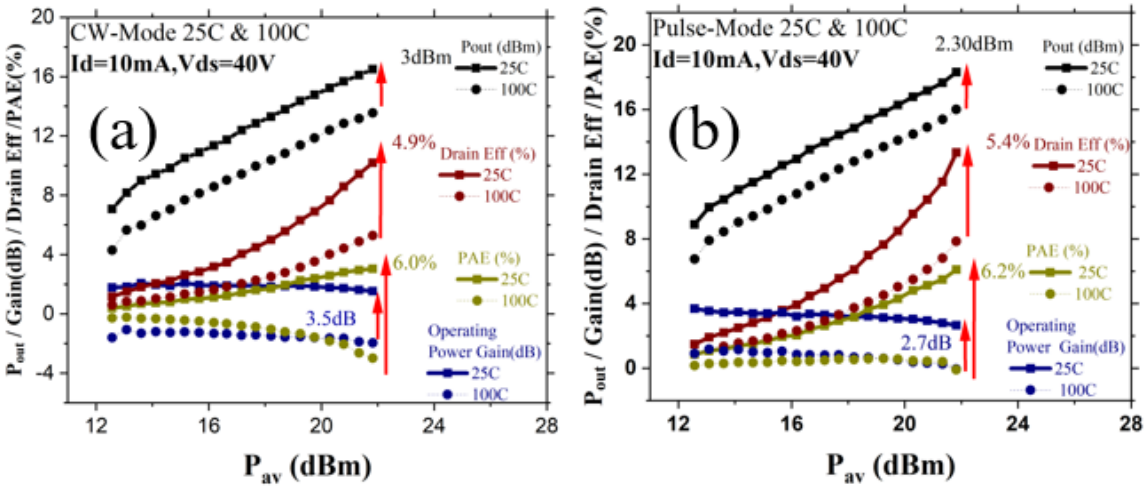

Figure 9.7: Comparison of CW (a) and pulse (b) large signal measurements performed at two different operating power levels of 0.4 W/mm and 0.8 W/mm at two different temperatures if 25°C and 100°C. Larger differences in performance between CW and pulsed modes can been seen with increasing operating power. Further degradation at elevated temperature can be observed as well.

100°C further degraded the performance for CW and pulsed modes with the device not showing any gain consistent with a thermal origin (Fig.9.7(a) and (b)).

These results demonstrate good quality epitaxy and surface treatment/passivation. We note that the RF performance is constrained by the long gate length, and that scaling will result in further improvements in Pout and gain. These results show a promising future for RF electronics based on Ga_2O_3 as well as the need for better heat dissipation during DC or CW operation.

9.3 Conclusion

β-Ga_2O_3 MOSFETs have been evaluated with pulsed IV and show minimal dispersion during gate and drain lag measurements. Pulsed large signal RF measurements show record PAE of 12% at 1 GHz for a 2 μm gate length and 22 μm source-drain spacing. These values can be further improved by scaling of the devices and improved heat management concepts.

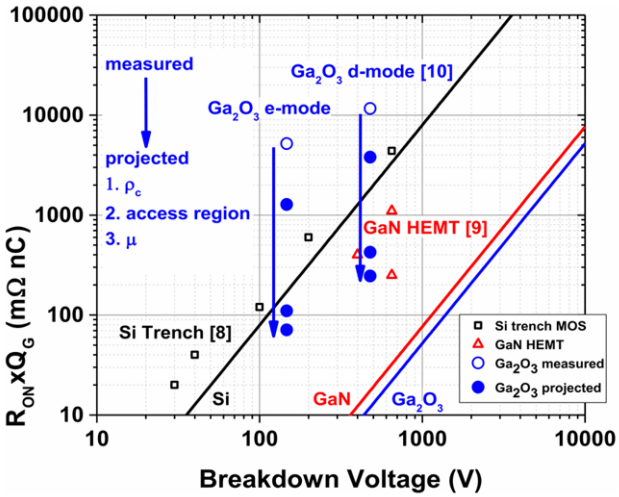

Figure 9.8: R_{ON}xQ_G as a function of VBK for state of the art GaN HEMTs, Si power trench- and Ga_2O_3 MOSFETS [209].

9.3.1 Future of Ga_2O_3 devices

Gregg Jessen *et. al* [209] predicts performance based on R_{ON}xQ_G limits projected as a function of V_{BK} and compared to state of the art realised Si trench power MOSFETs and GaN HEMTs as shown in Fig.9.8. Based on recent depletion-mode Ge-doped Ga_2O_3 MOSFET, along with enhancement-mode Si-doped Ga_2O_3 MOSFETs and improvement based on realised ohmic contacts with measured < 0.2 Ω.mm on samples with N_D > 1x10^{20} cm^{-3}, and access resistance scaling in the source and drift region it throws up much better devices compared to SiC or GaN. Further optimisation is expected due to very low R_{ON}. R_c values < 0.2 Ω-mm have been achieved

and modulation doping with R_{SH} ~300 Ω/sq has been demonstrated. $AlGaO/Ga_2O_3$ MODFETs should be able to take up the mobility higher and provide scaling advantages for lateral devices.

Scaling and synthesis of high quality Ga_2O_3 single crystals has been demonstrated. Two-inch Ga_2O_3 substrates are already commercially available, and larger diameters are being developed. The growth of Ga_2O_3 epitaxial films has been demonstrated by the established state-of-the-art semiconductor techniques such as molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD/MOVPE). Proof of concept prototypes of Ga_2O_3 transistors and Schottky diodes have been demonstrated. The origin of n-type conductivity remains controversial. Commonly, N-type in undoped Ga_2O_3 was attributed to oxygen vacancies; however, theoretic models disprove this assumption and link unintentional n-type to hydrogen or background impurities such as silicon. P-type remains at big at focus with no conclusive reports available and still an ongoing work. Significant progress has been made in the development of Ga_2O_3 transistors and diodes in the last few years, and the device characteristics demonstrated the great potential of Ga_2O_3 power devices for future high-power and high-voltage applications. Although Ga_2O_3 device technology development is happening at fast pace with some good quality device demonstrations, there still needs to be lot done to be able to take this technology to next level.

CHAPTER 10

CONCLUSIONS

This thesis primarily discusses different buffer related issues such as kink effect, source injected breakdown and lateral charge spreading in RF and power devices. Experiment and simulations together have been used to understand the mechanism causing these issues. The conclusions related to all these issues will be explained in this Chapter.

Kink effect, a hysteresis in drain current in the knee region of Fe doped GaN HEMTs on SiC for RF amplification has been observed with its magnitude having a direct dependence on drain bias, off state gate bias and sweep rate. The onset of kink appears at a voltage as little as 2 V above the knee, in an operating region where there is insufficient energy to form electron-hole pairs in GaN HEMT. As a result, the majority of previous explanations have been based on unusual deep level defect properties, in particular, strongly field dependent capture cross-sections. These defects are not compatible with Poole-Frenkel barrier lowering or conventional deep-levels, but all are based on highly unusual field dependent deep level traps for which there is no detailed model.

In this work, kink has been explained using a floating buffer model which arises due to the presence of background Carbon converting buffer into P-type creating a P-N junction between the buffer and the 2DEG. To observe kink and hysteresis, two effects must be present: the presence of a background substitutional Carbon impurity which makes the bulk of the GaN buffer P-type, and band-to-band trap-assisted-leakage of holes from the 2DEG into the buffer at moderate electric fields. Both these requirements are likely to be present in Fe doped GaN HEMT epitaxy explaining its relatively frequent observation. It has been shown that kink observed in Carbon-doped power devices arise essentially due to the same mechanism. The magnitude of the kink and its precise time dependence is strongly dependent on the Carbon concentration and its degree of self-compensation, the density of background donors, and the exact band-to-band leakage path,

helping to explain why even apparently identically grown epitaxy can result in different kink behaviour. Depending on the Carbon density, a kink can be either present or suppressed during the initial sweep providing an explanation for the reported difference in behavior which have been reported so far in the literature. Suppression of the kink effect would require a detailed control of native defects and unintentional dopants as well as parasitic leakage paths.

Effect of floating p-type buffer has been shown to result in transient behaviour which is dependent on the transport path to the trap state rather than just the trap properties themselves. Using drain current transient spectroscopy trap with ~0.9 eV has been shown with both "acceptors" and "donors" response. Simulation of these transients confirmed the presence of fictitious hole trap state which arises due to the necessity to take into account the full transport path to the traps and the existence of more than one active depletion region in the device. Depletion region located on drain side behaved like "electron" trap whereas those on the source side act like "hole" traps under bias. Response from these depletion regions has been verified by measuring a change in the drain (R_d) and source resistance (R_s). This change gives the positive and negative sign transients from the same trap, having the same activation energy but located in different parts of the device. Conventionally this would be interpreted as an "electron" and a "hole" trap having different capture cross-section. This calls into question some simplistic interpretations based on classical DLTS which assume the availability of a bath of majority carriers without considering the semi-insulating nature of the buffer. There is a considerable density of traps in GaN HEMTs almost all of which are neutral or inactive. Transport to and from those traps through the resulting semi-insulating buffer should be included in any complete analysis of the device reliability.

DC and Pulse I-V (P-I-V) characterization is an essential and quick method to measure and identify charge trapping in the device. Both these methods have been widely utilised and are often used to extract modified device models that aim to take into consideration the charge trapping effects when predicting the transistor's RF behaviour. These empirical and compact physical models use fitting functions for DC I-V and the fitting parameters of the trap controlling voltage for P-I-V at various quiescent biases and power dissipation. However, in this work, it has been shown that measured DC-I-V, and "knee-walkout" in P-I-V, does not necessarily provide a valid prediction of the "knee walkout" observed under RF excitation.

A case has been shown with a distinct difference in pulse and DC characterisation at various quiescent biases and pulse conditions. A conventional interpretation of this behaviour would suggest a dramatic difference in RF performance. However, large-signal RF measurements showed no significant difference in output power or efficiency. They showed 4 W/mm RF power at 1 GHz and 70% PAE. Two possible explanations for the observed difference has been suggested. First reason is the trapping time constant which can vary significantly than the duration typically used in P-I-V. This method typically uses a duration of not less than 200 ns which is sufficient to avoid any thermal effects, however, fast trapping on a timescale shorter than 200 ns can lead to

a strongly distorted P-I-V characteristic. This then becomes unrepresentative of the 1 GHz RF waveform which had a characteristic timescale much shorter than the trapping time resulting in different behaviour. This makes the trapping time constant vital parameter which needs to be accounted for in these compact physical models predicting expected RF behaviour from P-I-V. Wafers with different trapping time have been shown to match well with this prediction.

Second explanations have been the order of measurements performed under P-I-V and RF measurement cycle. P-I-V measurement follows a monotonic pattern exposing device under test first to low current high field and ending with high field low current regions. This allows the possibility of trapping which is often field dependant to occur resulting in distorted current in the next cycle unless it reaches minimum field required for de-trapping. RF measurement on another hand typically has sine wave on input having continuous up and down pattern which will cause a pattern on the output, which means every up sweep is preceded and followed by a down sweep. This would mean any trapping occurring at high drain bias will be de-trapped on the way back during the same run itself. It is this distinct order of measurement which can result in observed differences in the performances during P-I-V and RF. With measured example, it has been shown that although P-I-V measurements are a useful tool for identifying charge trapping, it can fall short in predicting the impact of traps under RF conditions. The great caution must be taken when utilizing Pulsed I-V measurements to extract the RF device model coefficients aimed at including trapping effects in GaN-based HFETs. Thus, appropriate large-signal RF-I-V waveform measurements are an essential additional requirement, if one is to develop robust nonlinear RF device models that include traps.

High power fast switching makes GaN HEMT vulnerable to breakdown (BD) which is defined as conditions at which a sudden increase in measured current/voltage is observed. In this work current controlled drain current injection technique has been used to evaluate the breakdown performance of Fe doped buffers used for RF amplification. The current controlled method gives the advantage of avoiding repetitive scanning and reduce burnout risk in unstable and fragile devices. In this method, source is kept grounded, and current is injected into the drain of the on-state device. The gate voltage is then ramped down to shut the device off leading to a rise in the drain-source voltage to a peak. This peak represents an unambiguous definition of three-terminal breakdown voltage (BDV). In this work two peaks, one at lower gate and other at higher gate voltage has been observed for a series of drain bias. Interestingly for all the cases, higher source current has been measured compared to gate current.

Using simulations and Electroluminescence measurements it has been shown that the breakdown is triggered by punch-through allowing the flow of current within the bulk of the GaN layer. Leakage path between source and gate dominates the process at lower injected currents. However, at higher injected current with an increase in drain voltages (and in pinch-off conditions), it's the punch-through which results in higher source currents primarily through the buffer. The dependence of impact ionization coefficient on the electric field has been used in

the simulations which hints that the impact ionization is a secondary effect and punch-through occurs even with impact ionization model being turned off. This complements the extracted electron temperature from EL spectra showing just the Bremsstrahlung effect.

Later in this work buffer for GaN-on-Silicon devices intended for power switching applications have been evaluated using stepped and ramped substrate bias. This epitaxy is vulnerable to lateral conduction at internal interfaces, for instance, a 2-dimensional hole gas (2DHG) can occur at the top of the strain relief layers (SRL) can be suppressed by a high density of compensating donors associated with Carbon doping. However, if not suppressed under high bias holes can extend far away from the device physical area. Substrate ramp measurements were used to investigate charge spreading, and it showed device active area dependence suggesting that lateral charge spreading occurred beyond the active physical area of the device. Furthermore, a customized surface and buffer leakage test structure confirmed the excellent surface quality and demonstrated that the leakage is related to the buffer conduction mechanism.

First-time experimental evidence of this lateral charge spreading has been shown using stepped substrate bias measurements. ON-resistance measurements pre and post substrate stress gave evidence that this spreading mechanism extends up to 2 mm away from the device, impacting adjacent devices. Recovery trap time constants of up to 100s of seconds have also been shown using dynamic on-resistance measurements.

The lateral charge spreading beyond the active area with long recovery time constant can be a serious concern resulting in cross-coupling between devices and buffer induced negative dynamic R_{ON} in adjacent devices. These observations provide useful information regarding the charge storage and lateral flow mechanisms within the epitaxy to be able to utilize them wisely for application such as integrated drivers which demand that active devices share the same die. Lateral charge flow beyond active area may also impact on-wafer reliability investigations since device probing can result in changes to unpowered adjacent devices during wafer level reliability measurements. The test methodologies such as substrate ramp which is common among techniques to evaluate buffer needs more attention given its impact on charge storage which can lead to measurement memory effects.

The last two Chapters show two new concepts for future RF devices. So far buffer has been major issue for GaN devices, the next Chapter introduces the idea of etching the standard GaN-on-Silicon epitaxy and thinning down the entire stack. A CVD diamond has then been deposited to making it thermally more stable. Thinning down the buffer results in getting rid of most of the defects and ensures that the diamond heat sink sits very close to the device heat zone. 354 nm thin GaN HEMT has been evaluated using the gate and drain lag measurements. Comparison between DC and steady state Pulse I-V showed 5% of the reduction in I_{DSmax} indicating that the thermal droop associated with self-heating is small. Further gate and drain lag measurements showed a minimal V_t shift and small transconductance drop which further make this device electrically better. Large signal CW measured at 1 GHz exhibit a maximum

power output of 23.4 dBm with a power added efficiency of 50% and a gain of 17.5 dB. These values marginally improved during Pulsed RF with a maximum power output of 23.6 dBm with power added efficiency of 52.2% and gain of 17.6 dB which indicates good thermal behaviour. Thermal performance has been further evaluated using photoluminescence (PL) to determine the GaN channel surface temperature using a HeCd laser source (325 nm) with a laser spot size of fewer than 1 μm. 2.61 $\pm$ 0.03 °C/(W/mm) temperature rise per unit power density has been measured at a distance 2 μm from the gate edge with the nearest accessible area at the field plate edge. As this corresponds to an average temperature of the measurement volume, finite element simulations were used to determining a thermal resistance at the peak temperature location of 9 $\pm$1 K/(W/mm). These results are encouraging and demonstrate that the successful integration of GaN-on-Diamond is possible without compromising electrical performance. Excellent electrical and thermal performance puts this work among the state-of-the-art RF devices and suggests that future GaN RF device might take this approach for better thermal and electrical performance.

The last Chapter introduces new material β-Ga_2O_3 for future RF devices. The wide bandgap of 4.9 eV and large electric breakdown strength of 8 MVcm^{-1} make β-Ga_2O_3 an attractive material for power devices. Johnson's Figure of Merit which evaluates materials suitability for high-frequency operation however also indicates that it may be useful for RF devices. A comprehensive review of material growth and device development has been presented along with a study on exploring its capabilities as an RF device. Further, a study on Fe-doped semi-insulating β-Ga_2O_3 [010] MOSFET has been evaluated using DC, Pulse I-V and large signal RF measurements at 1 GHz. DC output characteristics showed I_{DS} of 58 mA/mm with off-state leakage on the order of 10^{-9} A/mm. However, burnout at higher bias beyond V_{DS}= 60 V has been observed. Much improved I-V characteristics with minimal thermal droop has been observed for pulse measurements with 1 μs pulse length and 1ms pulse period, enabling higher bias operation to V_{DS}= 80 V, illustrating the large role self-heating plays in this materials system considering its low thermal conductivity of 23 W/m.K in the [010] direction at 300 K. Pulse gate and drain lag measurements were used as a tool to probe the surface/bulk states. Pulsed gate and drain stress measurements showed stable knee and no threshold voltage shift indicating no significant bulk trapping. A small knee walkout has only been observed for V_{DS} >40 V without any sizable V_t shift indicating minimal charge trapping. For CW mode of operation, a maximum P_{OUT} of 0.11 W/mm with 9.1% PAE and 19.5% drain efficiency has been observed while the observed maximum operating power gain of 3.08 dB has been measured, these efficiency values are well beyond what has been reported in the literature to date. The Pulsed RF large signal measurements (at 1 GHz, V_{DS}= 40V, I_{DS}= 5mA) further improved the maximum P_{OUT} to 0.13 W/mm, PAE went up to 12% and drained efficiency up to 22.4%. The difference between DC-Pulse and CW-Pulsed RF can be explained by the temperature rise in the devices. The thermal simulation shows channel temperature reaches 39°C after a duration of 1 μs and then rise to 325°C after about 100 ms which explains the difference between DC and static Pulse measurements. Mitigation of thermal

self-heating will be critical for the future success of these devices.

Based on the reported studies the future work would involve the inclusion of a built-in model for leakage in reverse biased GaN P-N junctions. This has recently been added as a feature in Silvaco Atlas. Currently, the simulations used in this study uses an approximation which with P++ shorting region located under the source and drain contacts, which provides a path for holes to flow into the semi-insulating buffer. Although there have been several reports that such leakage paths are often present under ohmic contacts using this simulation approach requires holes to flow from the p++ region at the drain to the gate region to impact the threshold voltage and thus results in unrealistically long time-constants at room temperature. This will be improved significantly by use of built-in a model which will be a more realistic approach of leakage path and its consequences on floating buffer under stress.

Another key advantage of including a built-in model for leakages will be a possible simulation of subthreshold leakages (off-state) and its associated breakdown in these buffers especially since they show significant charge storage. This hasn't been looked at under this study as the model was still not available.

DC and P-I-V can't be the basis for extraction of RF models are one of the key findings of this work. However, there has been only possible suggestions regarding this. Use of faster time scale in P-I-V to match the RF measurement time scale or *vice versa* would be a better comparison and will provide validity to the argument that trap time constant is the reason. A similar approach can be implemented in simulations where different switching modes can be exploited to represent P-I-V and RF measurement sequence to compare the impact of trapping. Based on these findings a compact model can then be built which could include the impact of trap time constant and measurement sequence allowing accurate predictability of RF parameters based on P-I-V measurements.

In terms of lateral charge spreading the limit of charge, spreading has been limited to 2 mm due to device mask set available under this study. This can be experimentally improved by better mask design and use of different etch depths to examine the limits of spread. Cross-coupling of the device can be a serious issue for reliability which makes essential to find the control mechanism to this spreading. This could be achieved by better doping schemes or by device design isolating different devices physically not just by 2DEG but deeper down at GaN-SRL interface.

The key observation in this work has been GaN buffer becoming p-type under the influence of Carbon doping based on simulation and experimental measurements. However, no direct measurements of these buffer have been done which confirms these predictions. Recently electric force microscopy has been used to investigate the contact potentials of Fe- and C-doped samples showing p-type nature of GaN:C. However, these measurements on the epitaxy used in this study would further validate the floating buffer model.

The new material β-Ga_2O_3 shows good surface and buffer properties; however, low thermal conductivity seems to be performance limiting factor. Possible thinning down the substrate and

deposition of diamond can be used as demonstrated on GaN-on-Diamond RF devices. The device used in this study has much larger gate lengths leading to higher gate capacitance limiting RF performance which could be improved significantly by gate scaling taking the RF performance much higher. Further improvements in device processing such as better ohmic and etching process can reduce the ON-resistance and leakages making them better devices.

APPENDIX A

APPENDIX A

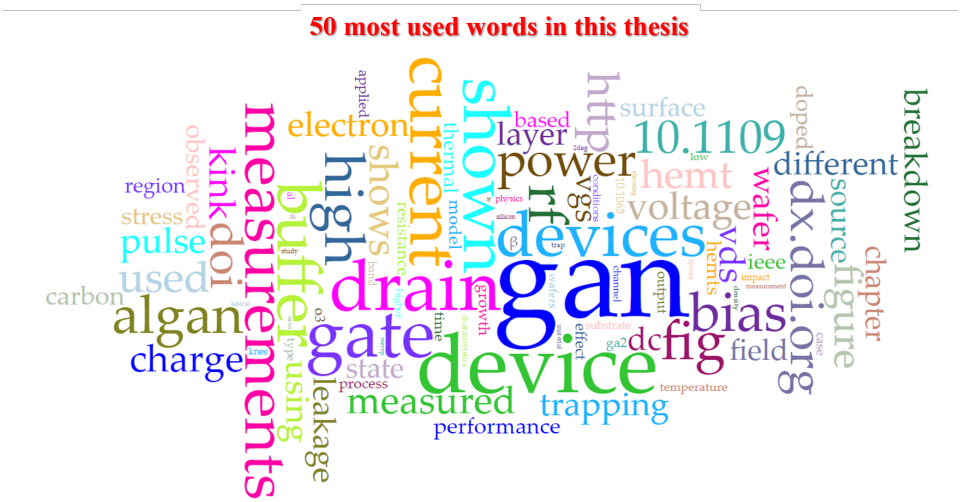

Figure A.1: For the joy of analytics it shows the 50 most used words in this thesis (generated using https://voyant-tools.org/).

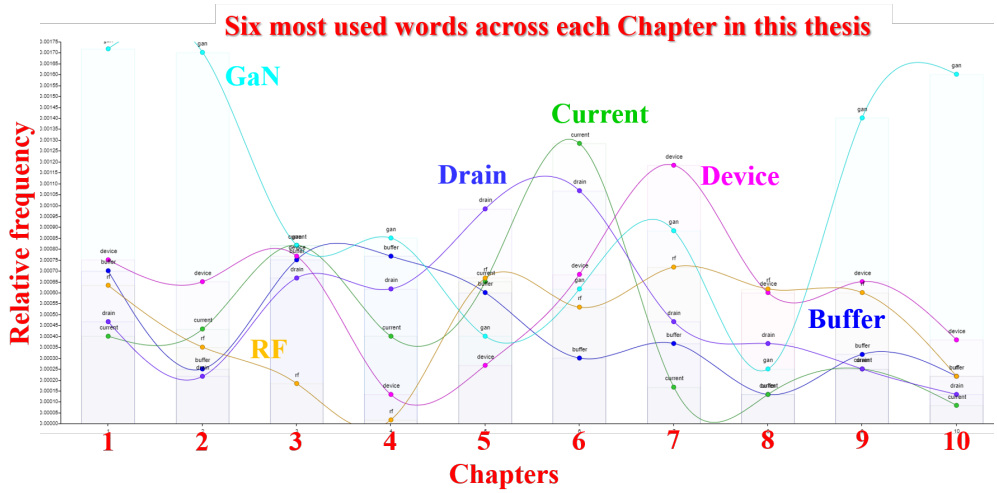

Figure A.2: shows he six most used words in this thesis across each Chapter (generated using https://voyant-tools.org/).

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