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The Characterisation of Gallium Nitride Devices for Power Electronic Applications

Leakage Mechanisms and Device Reliability

By

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Abstract

Highly efficient power conversion beyond the capabilities of silicon electronics is required to meet the growing global demand for power and to enable emerging technologies. The high breakdown field of wide bandgap semiconductors make these materials capable of meeting this demand in a power electronics revolution. Gallium nitride (GaN) is especially suited to this role due to its high electron mobility and its ability to form a high density 2D electron gas, resulting in enhanced efficiency. Compared to silicon, GaN systems can provide more efficient power conversion at higher voltages, all at a fraction of the system size.

Despite its promising material properties, a number of research topics remain before GaN technology can be fully exploited. In lateral devices, the substrate is usually grounded so increasing the vertical breakdown voltage of GaN-on-Si epitaxies is required to enable higher voltage devices while maintaining the low production cost associated with the use of silicon substrates. This has been approached from two directions in this thesis. Firstly from a material property perspective, by furthering the understanding of how carbon doping increases the resistivity of GaN. Through a combination of electrical measurements and device simulations, it is shown that carbon in GaN incorporates as donors as well as acceptors and that this self-compensation ratio of donors to acceptors is above 0.4. As the self-compensation ratio determines the material resistivity, it is an essential parameter in device design and future simulation works. Secondly, optimisation of epitaxial resistivity was approached at the device level. It is shown through electrical measurements that the resistivity of the epitaxy is reduced after processing Ti/Al based Ohmic contacts. These sub-contact leakage paths are further studied through a novel use of the quasi-static capacitance-voltage technique to reveal these paths extend up to 1.6 μm, all the way to the superlattice strain relief layers. The existence of these leakage paths is widely unknown and being aware of their impact is an important step forward for buffer design and accurate device simulation.

Vertical GaN-on-GaN devices are desired over lateral devices for their improved thermal performance, superior breakdown characteristics and reduced peak surface fields. The primary research efforts are focused on optimising vertical leakage and edge termination. The reverse leakage in vertical pn diodes is studied in the time domain and reveals the first evidence of impurity band conduction. The model required to explain the results also demonstrates the ability of charged point defects to control the conductivity of dislocations. This new understanding of the leakage dynamics could influence the way leakage is managed in future device designs. The reliability of these devices is also a topic of interest as qualification of this emerging vertical GaN technology is required before commercialisation. The mean time to failure of these vertical diodes was evaluated by adapting existing analysis techniques to facilitate the application of Weibull statistics to step stress measurements. These results represent the first lifetime estimations of this technology and this new technique will enable more rapid reliability testing of vertical GaN devices in the future.

Dedication and acknowledgements

My ability to produce this thesis was in no small part thanks to the support and knowledge of those around me. My thanks go to my supervisors; Martin Kuball and Mike Uren, for creating an excellent research group with members who are always available for fruitful discussion and guidance. Thanks to my collaborators at imec and Nagoya University for the samples they provided, without which none of this work would have been possible. Thanks also to the UK EPSRC for funding my research. And of course, a big thank you to everyone at the CDTR and everyone in the office for creating a great and enjoyable research environment - I will miss our weekly badminton games. Most of all thanks to Rosie, I would not have enjoyed this adventure half as much without your company.

AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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Chapter 1

Introduction

More than one tenth of the worlds electrical power is wasted in conversion losses between generation and consumption [1–3]. Through wide-spread adoption of high efficiency power converters, these losses can be halved [2], easing the demand for electrical power which is projected to increase by 12% in the US over the next 30 years [4]. The demand for highly efficient power converters is growing with applications in data centres, electric vehicles, wireless charging and LiDAR [5] as well as enabling new technologies where no other practical solutions exist. 30% of global greenhouse gas emissions comes from industrial power consumption [6] which has been reported to consume double the theoretical minimum power requirements, primarily due to energy inefficiency [7]. Therefore, highly efficient power electronics will impact positively on the global demand for power, global greenhouse gas emissions and can enable new technologies such as electric vehicles.

Applying mature and well proven silicon based technologies to this problem has resulted in diminishing returns of performance with system efficiencies ultimately limited by the material properties. The introduction of wide bandgap semiconductors can surmount these limits and facilitate ultra-high efficiencies and high power densities all delivered at a commercially viable price. Gallium nitride (GaN) power electronic devices are already being commercialised and beginning to compete with the $30B silicon power electronics market [5, 8]. As a wide bandgap semiconductor, GaN devices can operate at higher voltages, reducing the need for lossy step down and at higher temperatures, further reducing cooling requirements. The critical breakdown field of GaN is > 5 $\mathrm{MVcm^{-1}}$, more than ten times higher than Si, allowing device operation at higher voltages in smaller geometries [9]. In a high electron mobility transistor (HEMT) device architecture, GaN can deliver carrier mobilities of up to 2000 $\mathrm{cm^2V^{-1}s^{-1}}$ [10], reducing conduction losses and enabling up to a five times increase in the theoretical maximum switching speed.

Maximising the switching speed is desired since switching related losses depend on this duration when hard switching. An increase in the switching speed also allows the switching frequency to be proportionally increased without increasing switching losses, facilitating a reduction in the required size of passives [11, 12]. These smaller components, coupled with the high power density of GaN devices, gives rise to a >10 times reduction in the size of GaN based systems compared to silicon [13]. This gives GaN based power converters an advantage over Si and SiC in applications with weight and volume restrictions [14].

Taking the example of electric vehicles, efficiency and on-board power consumption are critical since batteries have a lower energy density than fuel tanks [15]. Currently silicon is still the primary material used in power conversion circuits but there is interest in the higher power conversion efficiency and reduced system size offered by new materials such as GaN [16]. In order to replace Si in electric vehicles, GaN power converters need to match or improve on the efficiency of existing technology. Current GaN based power converters are already able to compete with mature Si systems achieving efficiencies of up to 99% [17]. Additionally, GaN can operate at higher temperatures than Si which reduces the power requirements for cooling. The reduction in the volume of cooling systems coupled with the ability to use smaller passives enables GaN power converters to be smaller and lighter than Si equivalents. In all, GaN power converters have the potential to be lighter, more compact and more efficient, all of which increase the range of the vehicle while remaining competitive in total cost [18].

Power converters require high current transistors and diodes with current GaN technology targeting the application space of 600 V to 1200 V [16, 19]. The first GaN based HEMT was reported in 1993 by Khan et al. and was grown on a sapphire substrate [20]. However, the high defect density of the GaN and the poor thermal conductivity of sapphire made these devices unsuitable for power applications due to high leakage and difficulties in heat sinking. GaN-on-SiC fabrication in 1997 by Binari et al. solved these issues, taking advantage of the higher thermal conductivity of SiC and by including an AlN nucleation layer to reduce dislocation density [21]. This created devices suitable for high power operation but at great expense due to the cost of the SiC substrates, meaning this technology was not competitive to industry and was originally limited to defence based applications. It was not until 2001 with the development of GaN-on-Si technology that a suitable and affordable solution was found [22]. As a well-established material, silicon offers widely available infrastructure for growth on >150 mm wafers with a higher thermal conductivity than sapphire, and ten times cheaper than SiC. A challenge in growth on silicon is the large lattice mismatch and the differing coefficients of thermal expansion. This caused wafer cracking and introduced high densities of dislocations ($> 10^{10}$ cm^{-2}) which required the development of strain management techniques. By introducing compressive stress through AlN interlayers or AlN/GaN superlattice layers the cracking can be eliminated, although the epitaxies are still highly defective with typical dislocation densities in the order of 10^9 cm^{-2}. GaN HEMTs are normally-on since the 2DEG channel is only depleted with a negative bias on

the gate. However, there is a demand for normally-off devices as they offer fail-safe operation and more simplified gate driver circuitry [23]. Normally-off behaviour can be achieved in a cascode configuration with a low voltage Si MOSFET [24]. Additionally, true normally-off GaN HEMTs have been achieved by locally reducing the 2DEG density under the gate either by barrier recession, deposition of a p-type layer or Florine implantation [25–27]. GaN-on-Si wafers are sufficient for GaN HEMTs as the high dislocation densities do not affect the 2DEG. However, for vertical device geometries where vertical leakage is more critical the dislocation density is too high, although some pseudo-vertical devices have been demonstrated [28, 29]. Growth on native GaN substrates enabled by hydride vapour phase epitaxy (HVPE) or ammonothermal growth [30, 31] allows epitaxial growth with defect densities 10^4 times lower, facilitating production of the first vertical GaN-on-GaN pn diode in 2003 [32]. Unlike lateral devices, vertical devices can be scaled up to operate at higher electric fields without greatly increasing their area on the wafer [33]. Improvements in material quality and device design have increased the breakdown of vertical GaN pn diodes to 4 kV [34] but until recently the cost of the substrate has been prohibitive. The possibility of developing epitaxial lift-off techniques would allow the reuse of these expensive substrates, greatly reducing the production cost and enabling commercialisation.

After the 25 years of progress summarised above, GaN power devices are beginning to become commercially available with GaN based consumer products now available for purchase such as compact laptop chargers. However, some limitations are still to be overcome to harness the full potential promised by the material properties. The maximum forward bias surge current depends on the junction thermal capacity and the reliability of the device also depends on the junction temperature. These two factors are driving research into heat extraction from GaN devices since the thermal conductivity is lower than in silicon. GaN-on-GaN pn diodes offer high breakdown fields, low reverse leakage and have been reported to show avalanche capability. However, reverse bias leakage is still seen in these devices due to the presence of vertical dislocations. Reducing the reverse leakage would increase the operating efficiency, motivating work on further reduction of the dislocation density as well as study of the leakage mechanisms. Building a firmer understanding of the physics behind the leakage may present alternative methods of leakage suppression. This highlights the need for further study of bulk GaN devices which are already very low leakage and have the potential to approach the material limits of the reverse breakdown field.

In AlGaN/GaN-on-Si HEMTs, both the lateral and vertical leakage can be reduced by introducing carbon into the epitaxy below the channel [35]. The carbon can incorporate as an acceptor or a donor, making it an amphoteric dopant and various trap levels are possible. Overall, carbon has the effect of pinning the Fermi level in the mid gap, increasing the material resistivity. This method of leakage suppression works well and is commonly used despite an incomplete understanding of exactly how the carbon sets the resistivity. Since the carbon introduces acceptors and donors, these both influence the position of the Fermi level and the exact resistivity of carbon

doped GaN depends on this ratio of donors to acceptors, referred to as the self-compensation ratio. Direct measurements of the carbon self-compensation ratio are difficult as most methods for measuring dopant density are destructive and so only measure the total carbon density. Therefore, for a complete understanding of this widely used material, and for estimations of the resistivity of carbon doped GaN which are needed for simulation, an estimate of the carbon self-compensation ratio is required.

The vertical breakdown field also benefits from the carbon doping as it increases the resistivity of the epitaxy. Vertical breakdown is determined by the epitaxial resistivity and thickness which, when grown on silicon, is limited by strain management to ~ 7 μm [36, 37]. For operation of GaN-on-Si devices at higher voltages new strain management strategies need to be devised facilitating thicker epitaxial growth. Alternatively, the breakdown field of the epitaxy must be increased which is still much lower than the theoretical limits of GaN. For this latter reason, it is critical to study and optimise any aspects of the growth or processing which reduce the breakdown field of the epitaxy. For example, it has recently been shown that the passivation stoichiometry, deposited after growth, can influence the buffer resistivity [38, 39].

The typically stated requirements of a transistor specify a low specific on-resistance in the order of 1 mΩcm^2 with a dynamic on-resistance of less than 10% [40] i.e. the channel on-resistance never increases by more than 10%, regardless of any historical stress. Dynamic on-resistance or current collapse refers to the temporary increase in on-resistance of the channel after electrical stress in the off-state. In GaN HEMTs this occurs either via surface trapping causing a virtual gate or by bulk trapping acting as a back-gate. The use of source and gate field plates to redistribute the electric field and reduce the electric field peak at the drain side of the gate edge, as well as optimised surface passivation has allowed good management of surface related current collapse. In the bulk, trapping is mostly caused by deep levels related to the intentional carbon doping. Rapid de-trapping of these states and hence the suppression of current collapse requires leakage paths to facilitate the removal of the charge. It has been shown experimentally that low current collapse buffers can be achieved through a leaky GaN channel layer [41, 42] where leakage paths are either just under the contacts or distributed along the entire channel depending on the growth and processing. Thus in HEMTs an apparent trade-off is presented between current collapse and vertical leakage.

1.1 Thesis Structure

A selection of the challenges discussed above are addressed in this thesis. The following two chapters cover the required theoretical background and measurement techniques. In Chapter 4, two AlGaN/GaN samples, with and without carbon doping, are used to study the electrical effects of carbon in AlGaN. The empirically observed increase in resistivity is attributed to carbon being self-compensating. With the aid of device simulations, the carbon self-compensation ratio

in AlGaN, which was previously unknown, is estimated. Since this ratio alone sets the material resistivity, a reasonable estimate is required by researchers performing device simulations. Chapter 5 identifies and investigates a reduction in the epitaxial resistivity of an AlGaN/GaN HEMT epitaxy due to device processing. This is seen as an additional vertical leakage under Ti/Al based Ohmic contacts. Measurements of the leakage current on bespoke structures are used to identify the presence of these preferential leakage paths below the contacts. A novel analysis of quasi-static capacitance-voltage measurement data is used to identify the length of these leakage paths in the epitaxy and estimate their resistivity. This Ti/Al contact process is widely used and so the implications of this result extend to the majority of GaN devices. A full understanding of this behaviour is crucial for maximising the operating voltage of GaN-on-Si devices, which requires optimisation of the epitaxial breakdown field for successful high voltage device operation.

Continuing on to vertical devices, Chapter 6 investigates the reverse bias leakage mechanism in GaN-on-GaN pn diodes. Transient measurements of the reverse leakage and device capacitance reveal previously unseen features which are not possible to explain using existing models. A new model is constructed attributing the reverse leakage to conduction along impurity bands in the cores of the dislocations. In this model, the core conductivity is controlled by the charge states of surrounding point defect clusters. This work provides the first direct evidence for impurity band conduction along dislocations in bulk GaN. The reverse leakage in pn diodes is a critical parameter for the operating efficiency and this model provides new insight into the leakage mechanisms in GaN-on-GaN vertical devices. Another important factor for the commercialisation of this technology is the reliability. Chapter 7 evaluates the lifetimes of current vertical devices on bulk GaN. A step stress technique is used, which reduced the measurement time compared to conventional accelerated lifetime testing techniques. Analysis of these measurements is performed using methods not previously applied to GaN devices. The results provide the first lifetime estimations for vertical GaN-on-GaN pn diodes.

Chapter 2

Theoretical background

In order to understand the electrical characterisation in this thesis, some context is required. This chapter presents a summary of the material properties of GaN and compares it to other materials in the context of power electronics. An overview of GaN device architectures is presented as well as the material quality requirements and growth methods. This chapter also discusses some selected semiconductor physics which is relevant to later research chapters and introduces the challenges faced with device reliability.

2.1 Gallium Nitride

2.1.1 Crystal properties

Gallium nitride is a III-V compound semiconductor existing in two crystal structures; wurtzite and meta-stable zinc blend. For power devices, the more stable wurtzite crystal structure is used, shown in Figure 2.1. This is a hexagonal crystal system with inter-penetrating hexagonal close packed lattices of gallium and nitrogen. Wurtzite belongs to the symmetry group $P6_3mc$ meaning that the primitive cell has sixfold screw symmetry, mirror symmetry in the a plane and transflection symmetry in the c direction. Critically however, this crystal has no inversion symmetry in the c-plane. This means that reflecting the position of each atom about the centre of the primitive cell does not recover the original crystal. Coupled with the large difference in electro-negativity of the two constituent elements, this gives rise to an intrinsic internal electric field. This spontaneous polarisation is enhanced by a piezoelectric polarisation when the crystal is subject to tensile stress perpendicular to the c-plane.

The electronic properties of a crystal can be evaluated by consideration of the structure in reciprocal space. The primitive cell in reciprocal space is referred to as the Wigner-Seitz cell and

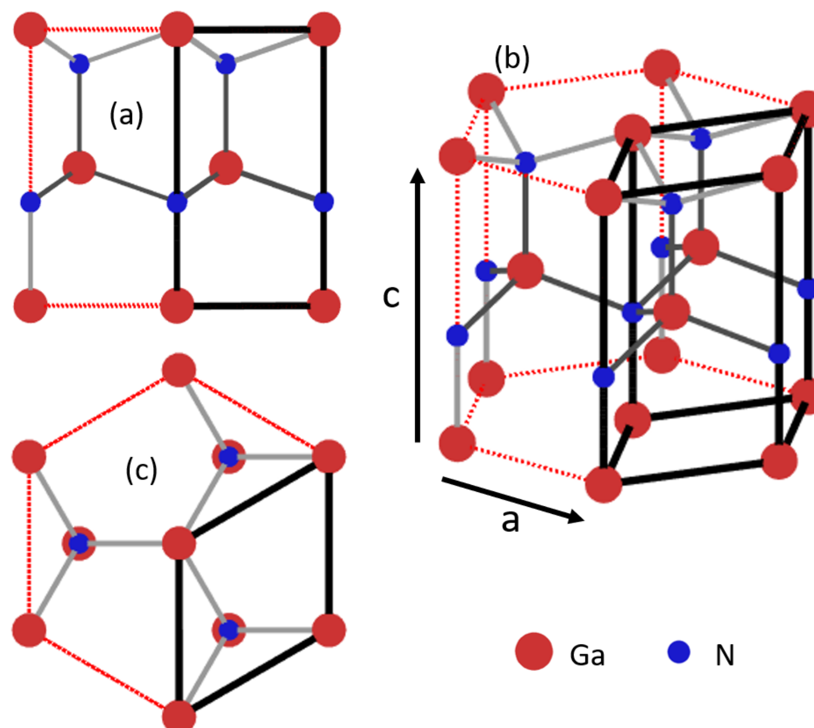

Figure 2.1: A hexagonal section of wurtzite GaN, viewed (a) along the a direction, (b) in isometric view and (c) along the c direction. The thick black lines outline the primitive cell while the solid grey lines represent bonds and the dashed lines highlight the hexagonal symmetry.

is constructed such that its basis vectors are orthogonal to the basis vectors of the primitive cell and the dot product of the two corresponding vectors is a multiple of 2π [43]. The centre of the reciprocal cell is referred to as the Γ point and represents zero momentum. The Γ point and the locations of other high symmetry points are labelled in Figure 2.2(a). Considering Bloch's theorem, electron plane waves with wave vector $\mathbf{k}$, must be periodic with the crystal lattice [44]. As such, the size of the Wigner-Seitz cell represents the longest possible wavelength an electron wave function can assume. The energy-momentum band structure can be constructed with this consideration of $\mathbf{k}$ space and the periodic crystal potential field $V(\mathbf{r})$ using the Schrödinger equation of the form

$$\left(\frac{-\hbar^2}{2m^*}\nabla^2 + V(\mathbf{r})\right)\Psi(\mathbf{r},\mathbf{k}) = E(\mathbf{k})\Psi(\mathbf{r},\mathbf{k}) \tag{2.1}$$

where m^* is the carrier effective mass, Ψ is the wave function and E is the carrier energy. By solving this equation for each momentum state, the electronic band structure can be constructed. The band structure of GaN is shown in Figure 2.2(b) between the high symmetry points.

Only the bands closest to the Fermi level, which are partially filled above 0 K, contribute to conduction. In GaN, conduction occurs at the Γ point where the bandgap is minimum. The carrier effective mass is inversely related to the curvature of the band which means that in GaN, electrons have a lower effective mass than holes. As the mobility is inversely proportional to the

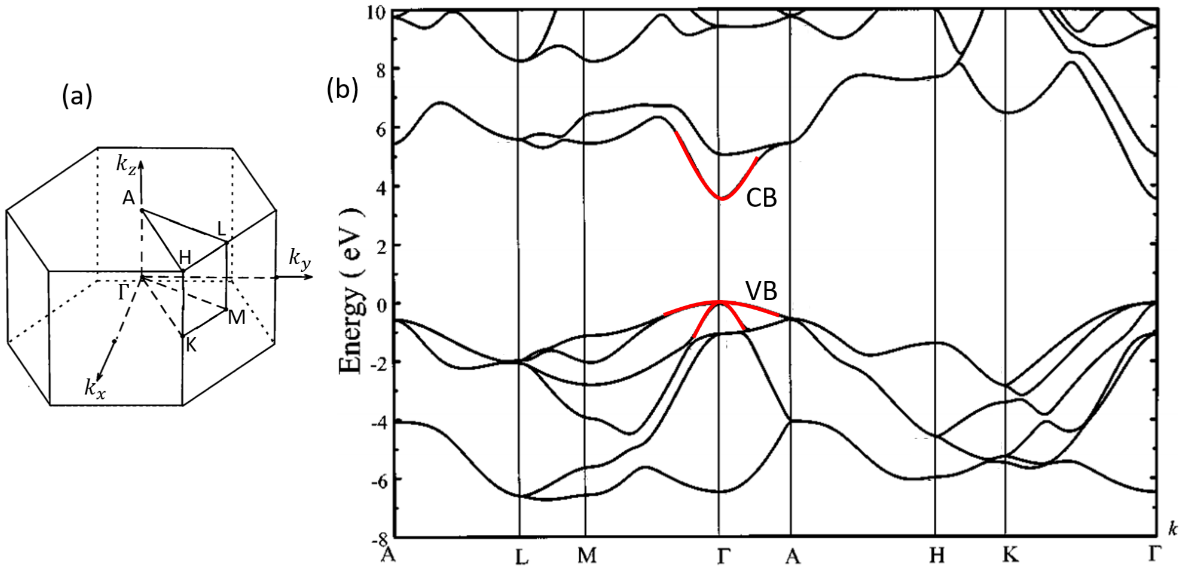

Figure 2.2: (a) The reciprocal cell with labelled high symmetry points. (b) The band structure of wurtzite GaN, adapted from [45]. Around the conduction band minimum (CB) and valence band maximum (VB) the bands are approximately parabolic with the light electron band and light and heavy hole bands.

effective mass, electrons have a higher mobility and as such, are used as the charge carrier in unipolar GaN devices. In addition, since the curvature of the conduction band differs between the Γ-M and Γ-A directions, the electron effective masses will be anisotropic. The electron effective masses parallel and perpendicular to the c axis are ${m^*}_e^{\parallel} = 0.2m_0$ and ${m^*}_e^{\perp} = 0.18m_0$ respectively where m_0 is the mass of a free electron [46].

The conduction band minimum and valence band maximum both coincide at the Γ point making wurtzite GaN a direct bandgap semiconductor. This means that zero momentum change is required for carriers transitioning across the bandgap. A direct bandgap can reduce the minority carrier lifetime by adding direct recombination to the list of available recombination mechanisms. The impact of this in the context of diodes is discussed in Section 2.4.2.1. A direct bandgap is a requirement for optoelectronic devices such as LEDs and solar cells since photons provide no momentum to the interaction. Indirect bandgap materials require the presence of phonons for optical interaction which greatly reduces the probability of these radiative transitions occurring. The direct bandgap of 3.4 eV makes GaN suitable for UV LEDs, which can be extended to blue LEDs when alloyed with indium. Moreover, the wide bandgap increases the energy required to create electron hole pairs and therefore increases the field required for impact ionisation and breakdown. Typically, the breakdown field scales with the bandgap to the power of 2.5 when the bandgap is direct [47]. This is the reason wide bandgap semiconductors are ideal for high power applications.

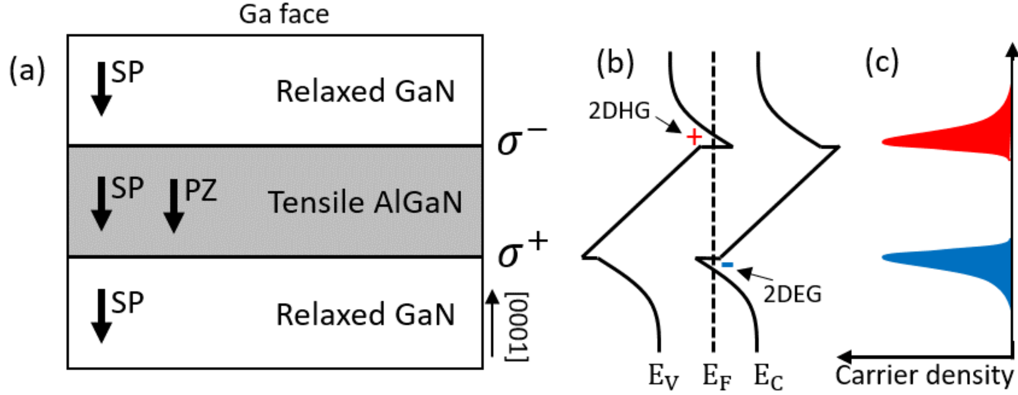

Figure 2.3: The spontaneous (SP) and piezoelectric (PZ) polarisation fields are shown in (a) on a purely instructive epitaxy with (b) the resulting band diagram and (c) the density of the carrier accumulation.

The band structure of wurtzite AlN contains many of the same features as GaN but with a much wider bandgap of 6.1 eV. The spontaneous polarisation of wurtzite AlN is higher than in GaN, with the polarisation field of AlGaN described by a non-linear interpolation [48]. Growing these materials epitaxially with abrupt changes in aluminium composition results in heterointerfaces at which there is a discontinuity in the polarisation field. In addition, the difference in lattice parameters between the two materials causes growth induced stress, adding a piezoelectric contribution to this discontinuity as shown in Figure 2.3(a). An interface charge, σ, is required to facilitate these internal field discontinuities and results in the accumulation of free carriers shown in Figures 2.3(b) and 2.3(c). Depending on the polarity of the interface charge, this results in the formation of a polarisation induced two dimensional electron gas (2DEG) or a two dimensional hole gas (2DHG). The density of the sheet charge is determined by the difference in the net polarisation fields, i.e. for material B on material A,

$$\sigma_{AB} = (P_A^{SP} + P_A^{PZ}) - (P_B^{SP} + P_B^{PZ}) \tag{2.2}$$

where P^{SP} and P^{PZ} are the spontaneous and piezoelectric polarisations respectively and have been determined empirically for the GaN-AlGaN-AlN material system as a function of the Al composition by Ambacher et al. [48]. These equations hold, providing there is no strain relaxation which typically will occur in layers $\gtrsim 20\ \mu$m thick [49]. To conserve net neutrality, the electrons which form the 2DEG must originate from elsewhere and leave behind a positively charged region of the crystal. In a HEMT, this source is commonly attributed to surface states on the AlGaN barrier and explains why a minimum barrier thickness is required for 2DEG formation [49]. As the barrier thickness is increased, the Fermi level at the surface is lowered by the polarisation field, shown in Figures 2.4(a) and 2.4(b). When the Fermi level drops below the highest surface state energy, that state can become unoccupied and the electrons in those states can migrate

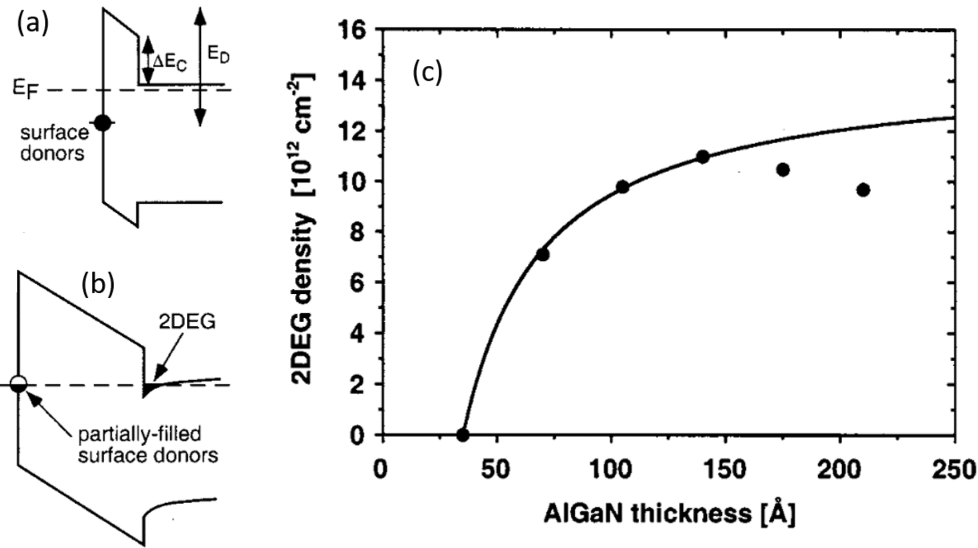

Figure 2.4: The source of electrons in the 2DEG, adapted from [49]. Band diagrams depicting the ionisation of surface donor states of depth E_D due to the polarisation field are shown in (a) and (b). The 2DEG density as a function of AlGaN barrier thickness is shown in (c). The deviation from the model above ~ 15 nm was attributed to strain relaxation.

to form the 2DEG. Therefore, the thicker the barrier, the more surface states will be emptied into the 2DEG. The experimentally measured 2DEG density as a function of AlGaN barrier thickness is shown as points in Figure 2.4(c) and fits well with this theory. This mechanism is completely analogous to the polar catastrophe in polar thin films [50]. From Figure 2.4(c) the minimum barrier thickness for 2DEG formation is seen to be around 3.5 nm with a $Al_{0.35}Ga_{0.65}N$ barrier. Increasing the polarisation field by increased Al content in the barrier, and thus reducing the minimum barrier thickness for 2DEG formation is not possible since the differing lattice constants result in cracking. However, thinner barriers can be achieved by the introduction of a 1 – 5 nm AlN layer between the channel and the barrier which boosts the polarisation field and comes with the added advantage of further increasing the 2DEG mobility by reducing alloy scattering at the interface [51]. The reduction of the 2DEG density with increasing barrier thicknesses above ~ 15 nm in Figure 2.4(c) was attributed to strain relaxation.

2.1.2 GaN for power applications

The primary materials used in the power semiconductor industry are compared in Table 2.1. The comparatively small bandgap of silicon makes it less naturally suited to high power electronics, however, because of its high maturity and low cost, a lot of work has gone into workarounds, pushing device performance to beyond their theoretical material limits. In contrast, the bandgaps of GaN, SiC and diamond are much larger, resulting in breakdown fields more than ten times larger than Si. This allows far simpler approaches in device design to achieve superior devices.

Table 2.1: Bulk intrinsic properties of semiconductors used in the power electronics industry [40, 55, 56].

	Bandgap (eV)	**Relative permittivity**	**Electron mobility** ($cm^2V^{-1}s^{-1}$)	**Breakdown field** (MV/cm)	**Baliga figure of merit (BFOM) normalised to Si**
Si	1.1	11.8	1450	0.3	1
4H-SiC	3.2	10	900	3	526
GaN	3.4	9.5	440	5	1131
C (diamond)	5.5	5.3	4500	10	51627
$\beta-\mathbf{Ga_2O_3}$	4.4-4.9	10-15	200-300	7-8	1485-4987

SiC has an advantage in heat extraction with its higher thermal conductivity but has a lower breakdown field. A good measure of the suitability of a material to power switching is the Baliga figure of merit (BFOM) [52]. This is defined as

$$\text{BFOM} = \epsilon\mu E_C^3 \tag{2.3}$$

where ϵ is the material permittivity, μ is the carrier mobility and E_C is the critical field. This analysis is also presented in Table 2.1 normalised to silicon. Here it is immediately obvious that on paper, diamond is the best material for high power devices. However, there is no known n-type dopant for diamond and even for unipolar devices, diamond is fundamentally unsuitable due to the 300 meV deep acceptor which has low activation and thus presents a high series resistance. The next highest figure of merit is beta phase Ga_2O_3 which is currently a material of high interest in the research community but is still in the very early phases of device development. Comparing GaN and SiC, the material based figure of merit of GaN is significantly better. This is reflected in the theoretical performance limits of GaN devices which should be able to block higher voltages while simultaneously providing lower on-resistances than the best SiC devices [53]. SiC has the advantage in heat extraction with a higher thermal conductivity and this is desired as junction temperature is linked to device lifetime. However, the property that sets GaN based devices apart from SiC equivalents is the polar crystal structure. With the polar structure of GaN comes the ability to use device architectures which exploit a 2DEG channel. This will be discussed in more detail in section 2.2.2 but among other things, this facilitates an increase in carrier mobility from the bulk value of 440 $cm^2V^{-1}s^{-1}$ (at 300 K with a donor density of ~ 10^{17} cm^{-3} [54]) to as high as 2000 $cm^2V^{-1}s^{-1}$ at room temperature [10].

2.2 Devices

2.2.1 Metal-semiconductor junctions

Metal-semiconductor junctions are required for device contacting and form with two distinct behaviours depending on the work function of the metal and the electron affinity of the semi-

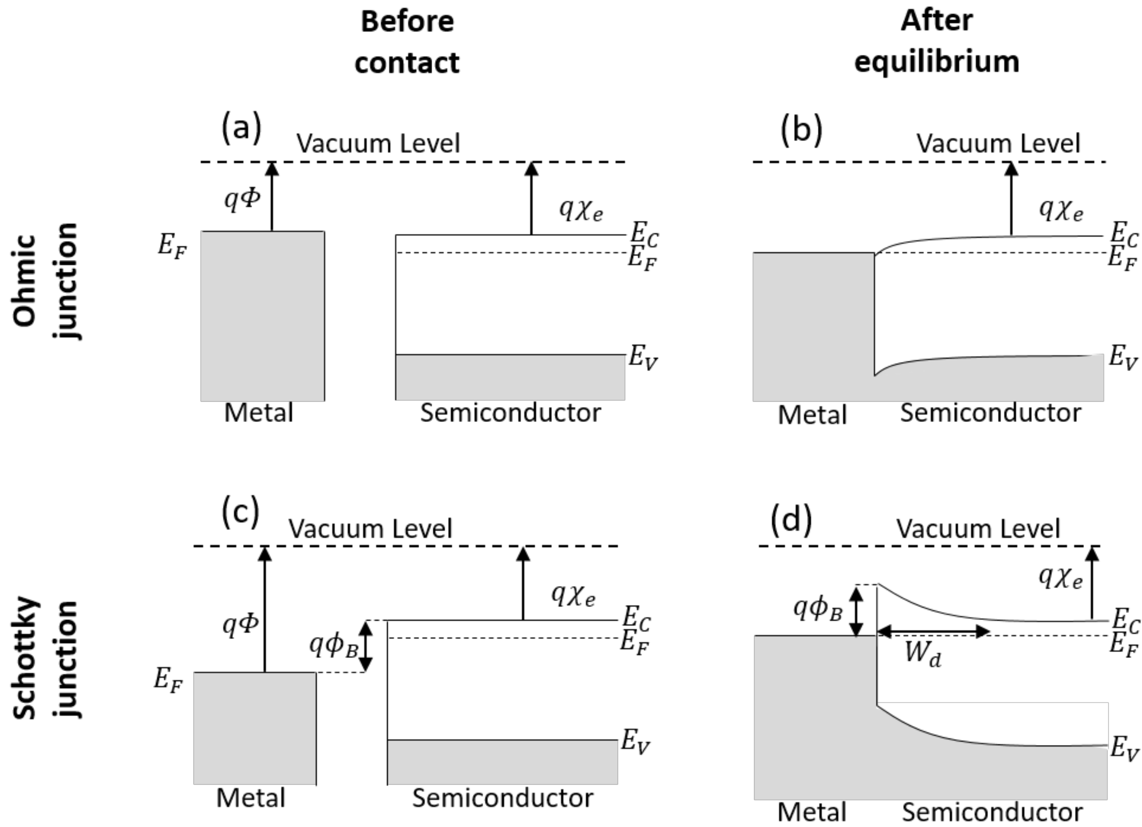

Figure 2.5: The band diagrams of metal-semiconductor junctions before contact and after equilibrium. (a) Before contact $\Phi < \chi_e$ resulting in the Ohmic contact in (b). (c) Before contact with $\Phi > \chi_e$ resulting in a barrier height of ϕ_B and (d) the resulting Schottky junction after contact with a depletion width of W_d.

conductor. The work function, Φ, and the electron affinity, χ_e, are defined as the energy to the vacuum level from the Fermi level and conduction band minimum respectively. If $\Phi \leqslant \chi_e$ as in Figure 2.5 (a), upon contact, electrons will move from the metal to the semiconductor increasing the chemical potential in the semiconductor and bending the bands down. This means after equilibrium, the band structure looks like Figure 2.5 (b) and there is no barrier to charge flow in either direction resulting in an Ohmic contact. The opposite case, in Figure 2.5 (c) where $\Phi > \chi_e$ introduces a barrier, ϕ_B, with a height of $\Phi - \chi_e$. On contact, electrons flow from the semiconductor to the metal, exposing a positive space-charge and forming the Schottky junction shown in Figure 2.5 (d).

The example band diagrams in Figure 2.5 feature an n-type material but the same can be applied to p-type semiconductors. In practice on GaN, Ohmic contacts are made on n-GaN with the metals titanium and aluminium. These metals are used together to permit diffusion of the contact metals into the GaN enabling the contact of 2DEGs. To make an Ohmic contact to a p-type

semiconductor, the work function must be high such that the metal Fermi level is in the vicinity of the valence band energy. Few metals have a sufficiently large work function to satisfy this requirement for GaN making Ohmic contacts to p-GaN challenging. Nickel is commonly used for this purpose, however, the contacts are not Ohmic but Schottky with a very small barrier. While the barrier height is set by the material, the depletion width, W_d is determined by the doping density as will be shown in section 2.4.4 (where the potential V_{bi} in equation 2.12 is equivalent to the barrier height ϕ_B). Therefore by heavily doping the p-GaN, the barrier width can be made very thin, reducing the impact of the barrier and rendering only weak Schottky behaviour. On the other hand, nickel on n-GaN presents a large barrier height and results in good rectifying behaviour.

It is not uncommon for multiple metals to be used in a stack. For example gold can be deposited on top of the metal-semiconductor junction to stop oxidisation of the contact metal in air. In HEMTs where the Ohmic contacts need to contact a 2DEG through a barrier, a common approach is to deposit layers of titanium, aluminium, nickel and then gold (Ti/Al/Ni/Au) [57]. During annealing the Ti/Al layers react and spike through the barrier into the 2DEG resulting in a low resistance electrical contact. The nickel acts as a cap and keeps the contact smooth with the inert gold ensuring the contact retains a conductive surface allowing the pad to be probed or wire bonded. This metal stack is not compatible with silicon foundries since in silicon devices gold is a rapidly diffusing contaminant. Acting as a deep recombination centre, gold destroys the minority carrier lifetime. Alternative gold free metal stacks providing similar contact resistances are Ta/Al/Ta [58] and Ti/Al/TiN [59].

2.2.2 Lateral device design

Because of the advantages presented by the 2DEG, early research was focused on developing lateral devices to exploit this. As such, lateral devices are the primary architecture entering the electronics industry today. The typical design of a lateral GaN power transistor is the HEMT, shown in Figure 2.6. The source and drain contacts make Ohmic contact to the 2DEG channel with a Schottky gate contact in between. The layers of the epitaxy will be discussed in detail in section 2.3.1.

A HEMT is a type of field effect transistor (FET) whereby the potential of the gate controls the size of the depletion region below it and the source-drain conductance is controlled by the gate potential in this way. Unlike conventional FETs, which create the depletion region by a pn junction, HEMTs employ a heterojunction for this job. This means that more specifically, HEMTs are a type of heterostructure FET (HFET) [43]. HFETs are desirable since the large barrier to the gate allows for low gate leakage and the confinement of the conductive channel gives rise to a high transconductance. However, most HFETs require doping in the channel layer to make it conductive and this presents a large number of impurity scattering sites. As a result the carrier mobility is low and the switching speeds are limited. To resolve this issue in gallium

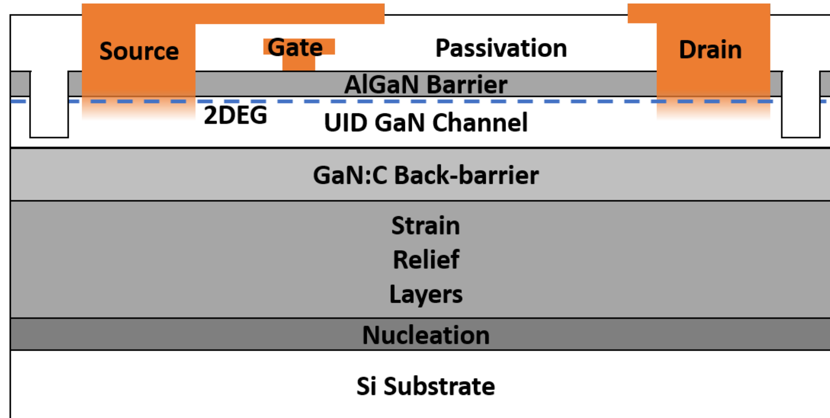

Figure 2.6: The layer structure and device topology of a typical power switching GaN-on-Si HEMT with mesa isolation. The 2DEG forms at the top of the unintentionally doped (UID) GaN channel, below the AlGaN barrier.

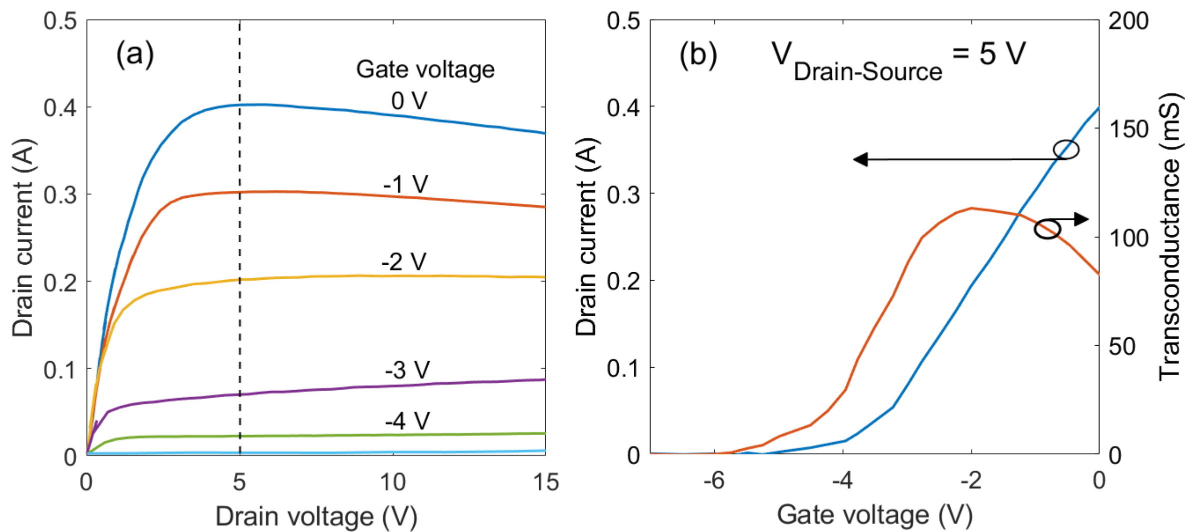

Figure 2.7: Typical DC (a) output and (b) transfer characteristics of a GaN HEMT. This data was replotted from [60] with permission. These recently published data are representative of the output and transfer characteristics currently achievable with GaN HEMTs.

arsenide devices, modulation doped FETs (MODFETs) were developed wherein a region below the heterointerface was doped to provide carriers in the channel with reduced impurity scattering. However, in GaN, this challenge is automatically resolved by not requiring dopants at all to form a conductive channel. Instead the polarisation induced 2DEG in GaN HEMTs provides all of the advantages of doped HFETs without the drawbacks of impurity scattering. Namely, these advantages are an increased transconductance, aided by the sheet charge being confined close to the gate metal, increased carrier mobility, and the carrier density in a 2DEG is typically in the order of 10^{13} cm^{-2} delivering the low specific on-resistance required for high power applications. The typical DC current-voltage characteristics of a GaN HEMT are shown in Figure 2.7 and demonstrate a transconductance of > 100 mS. The mobility of electrons in the 2DEG is far higher than in the bulk material which permits faster switching. This is desired as the switching speed dictates switching related loss and switching at a higher frequency reduces overall system size when considering passives. Taking the example of a capacitor smoothing the output ripple of a DC supply, at higher frequency a smaller capacitance can be used since $Z_C = 1/i\omega C$. For device fabrication on a wafer scale, each device is isolated by destroying the surrounding 2DEG. This is achieved either by etching away a trench around the device to create a mesa (shown in Figure 2.6) or by implanting the area around the device with ions such as nitrogen to locally destroy the crystalline properties of the material (and hence the 2DEG). These are referred to as mesa and implant isolation respectively.

In the majority of power switching applications, transistors will be accompanied by high power diodes such as in DC-DC converters. With the intention of developing GaN power ICs in the future, lateral diodes are also being developed on the same GaN-on-Si epitaxies [61–63]. Even now, early stage all GaN-on-Si ICs featuring HEMTs and lateral diodes have already been demonstrated [64, 65]. Lateral GaN-on-Si devices also allow for easy integration with Si MOSFETs, delivering versatile and compact circuits [66, 67]. These lateral diodes are mostly Schottky devices, modelled on the gate and drain of a HEMT. Thus these devices continue to harness the advantages of the 2DEG and have been developed with a range of field plate designs to increase the operating voltage [68, 69].

2.2.3 Vertical device design

In addition to lateral devices, vertical devices are also beginning to emerge. Despite the lack of 2DEG, the advantages of a vertical topology include increased breakdown voltage without increasing the device area, reduced peak surface fields and easier heat extraction [70]. In high power applications, pn diodes are desired over Schottky diodes as they are able to withstand higher voltages and have been reported to exhibit avalanche breakdown which is required for surge protection [71–73]. As well as pn diodes, a range of vertical device designs on bulk GaN are being investigated for a broad range of applications. For very high power devices, large areas are required for power dissipation and to drop the high potential in the off-state. A lateral geometry

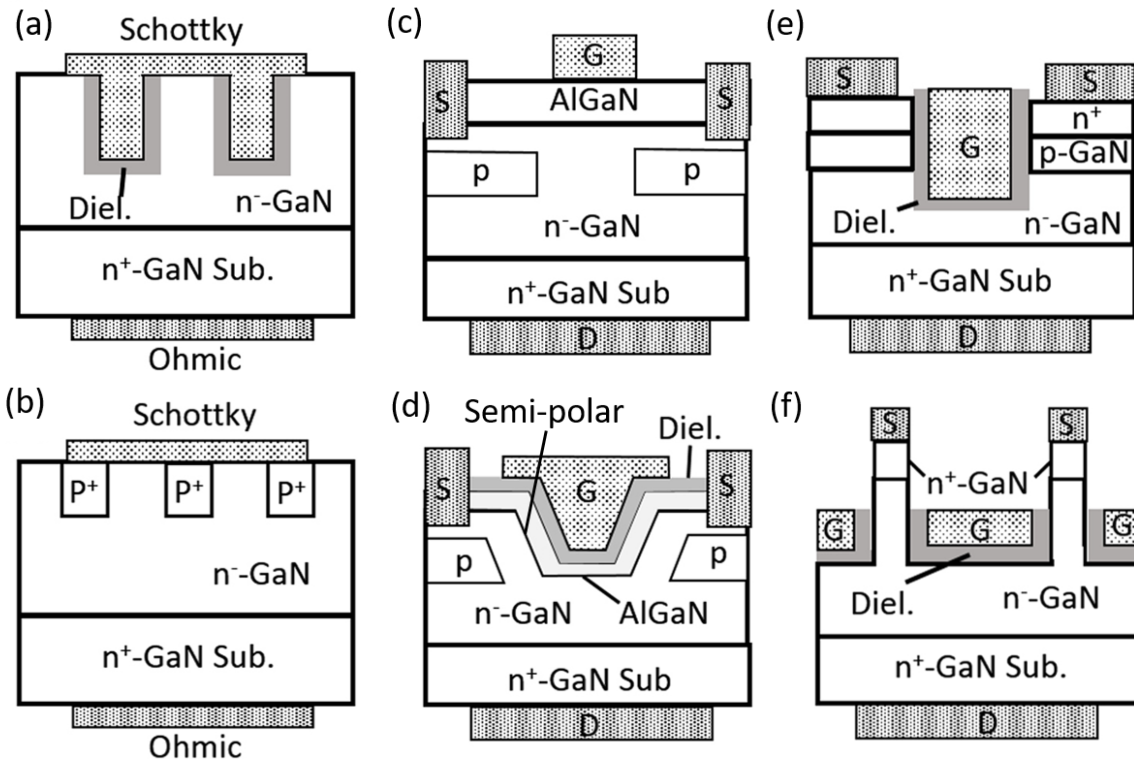

Figure 2.8: Vertical device designs of advanced Schottky barrier diodes, (a)-(b), current aperture vertical electron transistors, (c)-(d) and MOSFETs (e)-(f). Adapted from [19].

for this purpose is unfavourable since the cost of the device scales with the area of the wafer real estate. Therefore vertical devices surpass their lateral equivalents in chip size and ease of thermal management and present themselves as a more financially advantageous alternative. However, vertical architectures are much more sensitive to material quality [33]. As will be explained in section 2.3.2, these devices require low defect density material and this can be provided by growth on native substrates.

Schottky barrier diodes (SBDs) are capable of switching faster than pn diodes and so are more suited for high frequency applications. Schottky barrier diodes also have a lower turn-on voltage than pn diodes but are less suited for high power applications as the reverse leakage and breakdown characteristics are comparatively poor. Recently, trench schottky barrier diodes have been developed using a metal-insulator-semiconductor (MIS) [74] or pn junction [75] to increase the size of the depletion region in reverse bias. These devices are shown in Figures 2.8(a) and 2.8(b) respectively and enable the combination of the best properties of Schottky and pn diode characteristics. Namely, the high forward current and low turn-on voltage from the Schottky diode, with the high breakdown voltage and low reverse leakage of the pn diode. These structures enable low turn-on voltages for vertical GaN devices which can block high voltages.

In addition to diodes, vertical transistors are being developed. A key motivation for pushing the development of vertical transistors over lateral devices is the possibility of achieving far superior breakdown voltages. This is enabled by the bulk nature of the device and the resulting absence of surface breakdown. A common vertical transistor design on bulk GaN is the current aperture vertical electron transistor (CAVET) [76]. A p-type layer in the epitaxy impedes vertical conduction apart from through an aperture. Control of the 2DEG above this aperture controls the vertical conductivity of the device. This architecture, shown in Figure 2.8(c), maintains the electron mobility of a lateral 2DEG and so has comparable gate control to a HEMT but with the added advantage of no large surface fields around the gate, since the drain is on the substrate. Moreover, this design can be adapted to an enhancement mode device by growing the 2DEG-forming heterointerface on the semi-polar facet [77] as shown in Figure 2.8(d).

A different approach to vertical GaN transistors is to revert to the metal-oxide-semiconductor field effect transistor (MOSFET) topology, common in Si device design. A trench MOSFET is shown in Figure 2.8(e) which has fewer growth steps than a current aperture vertical electron transistor and defaults to enhancement mode behaviour [78]. The growth can be further simplified by moving to the fin MOSFET design in Figure 2.8(f). This architecture gives rise to enhancement mode operation without the need to grow any p-GaN [79]. Enhancement mode operation is desired in power switches because it acts as a safeguard should the gate control circuitry fail. However, the absence of a 2DEG in GaN MOSFETs means the carrier mobility is very low, typically around 150 $cm^2V^{-1}s^{-1}$ [79, 80].

2.3 Growth

2.3.1 Heteroepitaxial Growth

The growth of lateral GaN devices is typically done by metal-organic chemical vapour deposition (MOCVD) as this is a cost effective method for mass production and is faster than alternatives such as molecular beam epitaxy (MBE). The principle of metal-organic chemical vapour deposition is to combine two or more carrier gases over a high temperature substrate, typically 1000 °C, where they react, resulting in the epitaxial deposition of GaN. Carrier gases often used are tri-methyl-gallium ($Ga(CH_3)_3$), tri-methyl-aluminium ($Al(CH_3)_3$) and ammonia (NH_3). Due to the organic nature of the gases, carbon as well as other impurities are invariably incorporated into the GaN. The concentration of these impurities can be controlled by tuning the temperature and pressure of the reactor. In some cases carbon incorporation is desired in levels higher than provided by the carrier gases. In this case the additional carbon is supplied by the introduction of carbon tetrachloride (CCl_4) as an additional carrier gas. Nitrogen vacancies and low levels of other impurities such as oxygen make as-grown GaN n-type hence undoped GaN is often referred to as unintentionally doped (UID) GaN.

For lateral devices, silicon is the substrate material of choice as it is low cost and the epitaxy

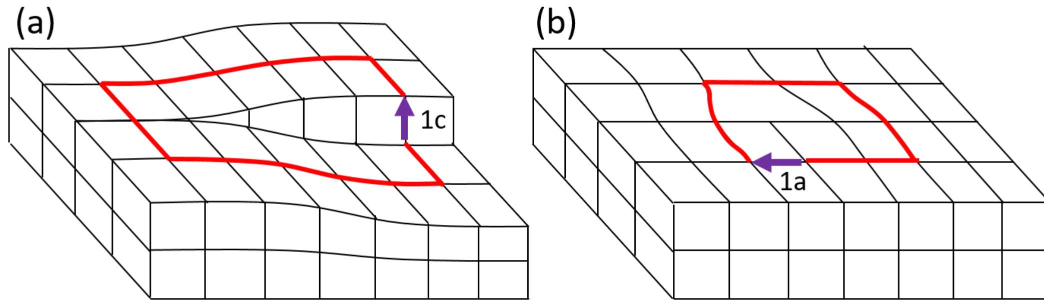

Figure 2.9: A depiction of (a) a screw and (b) an edge dislocation in a crystal lattice with Burgers vectors of 1c and 1a respectively. The arrow represents the Burgers vector and the extended defect propagates up from the lattices as shown.

can be grown in existing Si foundries. However, a lot of work has been done to devise transitional layers to make this growth possible due to the large lattice mismatch between Si and GaN as well as the differing coefficients of thermal expansion (CTE). A generic diagram of the required epitaxial layers for growth on Si is visible in Figure 2.6. When exposed to the tri-methyl-gallium used in the metal-organic chemical vapour deposition reactor, the Si is etched causing damage to large areas of the substrate. This effect is known as meltback etching and must be avoided for successful growth [81]. A thin AlN layer is deposited on the Si for this purpose and both protects the Si and provides a nucleation site for the growth. To manage the stress caused by the lattice mismatch, a number of AlN and AlGaN layers are incorporated to transition from the AlN nucleation layer to GaN. The exact design and composition of these layers, often referred to as transition layers or strain relief layers (SRL), are generally not disclosed by growers. However, they invariably consist of either a AlN/GaN or AlN/AlGaN superlattice, AlN interlayers or (step) graded AlGaN. To compensate for the differing coefficients of thermal expansion, the silicon wafer is intentionally warped to cause compressive stress during the growth of the III-N layers, which compensates for the tensile stress on cool down. These tricks to reduce the strain of the lattice mismatch and enable the growth of GaN-on-Si have their limitations. Currently, the maximum achievable thickness of the wide bandgap epitaxy is limited to $\sim 7\ \mu$m including the strain relief layers [36].

The strain relief layers also have the effect of reducing the dislocation density by approximately a factor of ten from 10^{10} to 10^{9} cm^{-2} [82]. This is due to the many junctions of differing strain each introducing a chance of causing dislocations to turn over by 90° where they may find another dislocation of the opposite Burgers vector and annihilate. The Burgers vector represents the magnitude and direction of a lattice distortion. For example, Figures 2.9(a) and 2.9(b) show a screw and an edge dislocation with Burgers vectors of 1c and 1a respectively. When tracing a circuit around the dislocation, following the lattice planes, the circuit does not return to its starting point by the displacement of the Burgers vector. Reduction of the dislocation density is important

since these extended defects give rise to leakage paths, explained in section 2.4.5. As leakage current flows along dislocations, these epitaxies with a high density of vertical dislocations are unsuitable for vertical devices. However, fortunately, there appears to be little impact on the lateral leakage and lateral mobility, likely because the high density of the 2DEG screens these scattering centres. As the operation of a lateral device never requires low resistance vertical conduction below the 2DEG, heavy doping of the buffer and strain relief layers with carbon can be used to reduce vertical leakage and increase the vertical breakdown voltage.

2.3.2 Homoepitaxial Growth

For vertical devices such as pn diodes, where reducing the vertical leakage is critical, the dislocation density is one of the most important epitaxial characteristics to consider. Homoepitaxial growth is desirable in this case since it introduces no additional strain or defects other than those already existing in the substrate. Bulk GaN substrates can be grown by hydride vapour phase epitaxy or by the ammonothermal method. The hydride vapour phase epitaxy process first reacts hydrogen chloride with gallium at high temperatures to produce gallium tri-chloride ($GaCl_3$). This is subsequently reacted with ammonia (NH_3) to produce GaN and is generally deposited on foreign seeds such as sapphire. The latter reaction takes place near equilibrium conditions with growth rates as high as 500 μm per hour [83]. In contrast, the ammonothermal method takes place in a high pressure autoclave. GaN solution is dissolved in ammonia and transported by convection to an area containing GaN seeds. The presence of the temperature gradient causes the solution to become supersaturated, forcing deposition onto the native seeds and prompting crystal growth [84]. This method has been able to produce 2" substrates of high structural quality but with a high point defect density and a growth rate of only a few μm per hour [85]. The ammonothermal method has also been used to grow seeds for faster hydride vapour phase epitaxy deposition resulting in a rapidly grown, low strain substrate. Bulk GaN substrates typically have dislocation densities in the order of 10^5 cm^{-2} but are currently much more expensive than Si substrates and only widely available in small, 2" wafers. However, advances in growing technology are rapidly driving down the cost and increasing the size of the available substrates.

2.4 Selected semiconductor physics

2.4.1 p- and n-type doping of GaN

GaN can be doped both n- and p-type by introducing impurities during the growth which incorporate substitutionally. For n-type doping during metal-organic chemical vapour deposition growth, silane gas (SiH_4) is introduced which causes the incorporation of silicon on the gallium site [54]. This is associated with a shallow donor level of 12-17 meV [54] creating conductive n-GaN. Conversely, p-GaN can be grown by introducing bis-cyclo-penta-dienyl-magnesium (Cp_2Mg) into the metal-organic chemical vapour deposition reactor which results in the incorporation

of magnesium on the gallium site [86] with an acceptor energy level of ~112 meV when in high densities [87]. This level is deep compared to the thermal energy at room temperature, therefore these acceptors are only partially ionised. In addition, as grown, the magnesium is generally incorporated in complexes with hydrogen which passivate the dopant, rendering it electrically inactive. The hydrogen can be removed by annealing in a hydrogen poor environment, reactivating the dopant [88, 89]. However, the deeper level means that very high donor densities are required for conductive p-GaN. Typically, densities as high as 10^{20} cm^{-3} are required as only 1-10 % are ionised at room temperature. Increasing the magnesium density beyond this value results in material degradation and a drop off in the hole density [87].

2.4.2 pn diodes

A pn diode is a junction between p- and n-type material and exhibits an asymmetric current-voltage characteristic, described by the Shockley equation as

$$I = I_0\left(\exp\left(\frac{qV}{nk_bT}\right) - 1\right) \tag{2.4}$$

where I_0 is the reverse saturation current, n is the ideality factor and k_b is the Boltzmann constant. When forward biased, carriers flow across the junction causing minority carriers to be injected on both sides. At low defect densities, the minority carrier lifetime is sufficiently long that the minority carriers travel all the way through the junction into the bulk quasi-neutral region where they recombine either by a band-to-band process or via defects. Conversely, in a junction with very high defect densities, the recombination of minority carriers can occur in the junction before the carrier has seen the full potential drop of the junction. At most, this halves the voltage drop seen by the carrier i.e. the voltage is divided by an ideality of two. More realistically, both of these two cases occur resulting in an ideality between one and two depending on the defect density at the junction. Study of the ideality over temperature is a good way to identify thermally activated defects in the junction and identify the activation energies. From the exponential term in the Shockley equation it looks like the forward current should be reduced at higher temperatures. Instead, the current increases and the turn on voltage shifts to lower voltages as the temperature is increased. This is because the reverse saturation current is also temperature dependant, with the form

$$I_0 = ep_{n0}\sqrt{\frac{D_p}{\tau_p}} + en_{p0}\sqrt{\frac{D_n}{\tau_n}} \tag{2.5}$$

where p_{n0} (n_{p0}) is the minority carrier density in the n (p) side of the junction, τ_p (τ_n) is the minority carrier lifetime for holes (electrons) and D_p (D_n) is the diffusion constant for holes (electrons). The diffusion constants are defined by the Einstein relation;

$$D_{e,h} = \frac{k_bT\mu_{e,h}}{e} \tag{2.6}$$

which linearly increases with temperature. The minority carrier density also increases with temperature but less strongly. Therefore, the reverse saturation current increases with temperature while the exponential term in the Shockley equation decreases with temperature. Overall, the temperature to the power of a half wins, resulting in an increase in forward and reverse current with temperature.

2.4.2.1 Minority carrier lifetime

The minority carrier lifetime is the mean time a minority carrier exists before recombination. This can occur via band-to-band recombination, via a defect state known as Shockley-Reed-Hall (SRH) recombination, or via Auger recombination. In Auger recombination the recombination energy is donated to a third carrier which typically de-excites non-radiatively. Shockley-Reed-Hall and Auger recombination generally deposit the additional energy as heat into the crystal (phonons), while band-to-band recombination emits the energy as photons. The effective minority carrier lifetime, τ_{eff}, is governed by the recombination option with the shortest time constant, described by the equation

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Band}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} \tag{2.7}$$

where τ_{Band}, τ_{SRH} and τ_{Auger} are the time constants for recombination via band-to-band, Shockley-Reed-Hall and Auger recombination respectively. As GaN is a direct bandgap semiconductor, band-to-band recombination does not require any momentum exchange and so can occur without requiring phonon interaction. This greatly increases the likelihood of band-to-band recombination compared to an indirect bandgap semiconductor and reduces the band-to-band recombination time constant accordingly. Shockley-Reed-Hall recombination via defect states intuitively depends on the defect density. The higher the material quality, the lower the recombination rate and the longer the time constant. Auger recombination is only significant at high current densities.

In metal-organic chemical vapour deposition grown GaN, the minority carrier diffusion length has been measured as 0.28 μm corresponding to a minority carrier lifetime of 6.5 ns [90]. In hydride vapour phase epitaxy grown GaN which has a much higher material quality, the minority carrier diffusion length has been measured as high as 2.5 μm corresponding to a minority carrier lifetime of 40 ns [91]. In order to achieve a diode ideality near 1, the minority carrier diffusion length must be greater than the depletion region size. In equilibrium, the typical depletion width of a GaN diode is around 0.5 μm and reduces in forward bias. This is less than or in the same order of magnitude as the diffusion lengths reported above meaning near ideal GaN diodes are achievable given a sufficiently high material quality, despite the direct bandgap nature of GaN.

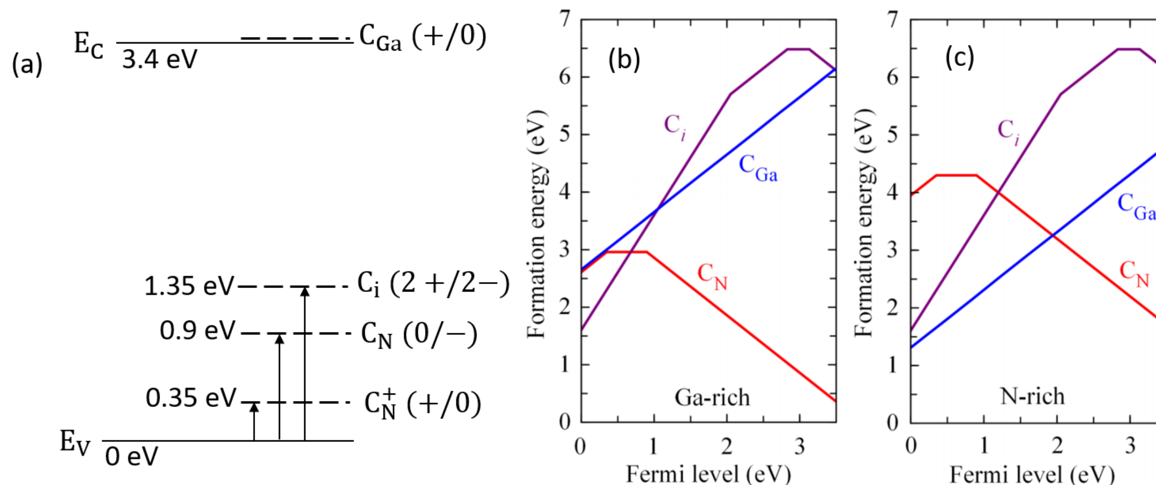

Figure 2.10: (a) The energy levels in GaN resulting from carbon incorporation with their charge states. Density functional theory simulations of the formation energies of these defects are reproduced from Lyons et al. [92]. These results are shown as a function of Fermi level in (b) Ga-rich and (c) N-rich growth conditions.

2.4.3 Carbon doping in GaN

In GaN-on-Si HEMTs for power switching applications, carbon is often intentionally incorporated in high densities in the buffer and strain relief layers to increase the material resistivity, suppressing buffer conduction and increasing the vertical breakdown voltage [93]. Carbon doped GaN (GaN:C) has been measured to have a resistivity in the order of 10^{13} Ωcm and its use in power devices is based on this empirical observation [35]. The exact mechanism that makes GaN:C highly resistive is only now becoming clear. Density functional theory (DFT) simulations by Lyons et al. [92] predict that carbon will incorporate in GaN primarily substitutionally with trap levels shown in Figure 2.10(a). This figure shows that carbon in GaN is amphoteric since depending on how it incorporates, it can act as a donor (+/0) or an acceptor (0/-). Substitutional carbon on the nitrogen site (C_N) forms a deep acceptor level at 0.9 eV above the valence band. It is predicted that this defect can undergo a lattice relaxation and become a donor-like complex by capturing a second hole. However the result is a very deep donor level 0.35 eV above the valence band and so is of little importance. Substitutional carbon on the gallium site (C_{Ga}) is predicted to incorporate as a shallow donor in or near the conduction band [92] while the lowest energy interstitial carbon configuration (C_i) forms a level of 1.35 eV above the valence band. These defect levels have also been observed spectroscopically [94–96]. The formation of these defects costs energy, so carbon will be incorporated in whichever configuration has the lowest formation energy. Therefore, the lower the formation energy the higher the relative abundance of a particular defect. Figures 2.10(b) and 2.10(c), show the simulated formation energies of each defect type in Ga-rich and N-rich growth conditions respectively. In these figures, the x-axis represents the

position of the Fermi level during growth. At a given Fermi level position the relative formation energies are a good indicator of the expected relative abundances of the defect states since a higher formation energy means a slower incorporation rate. The interstitial carbon defect only has the lowest formation energy when the Fermi level is very near the valence band in Ga-rich conditions. Most as-grown GaN is n-type because of unintentional dopants such as H and O and so interstitial carbon is unlikely to form in normal growth conditions. In both Ga-rich and N-rich conditions in n-type GaN, C_N is the most energetically favourable and so is predicted to be the most abundant. C_{Ga} is only the lowest energy in N-rich growth when the Fermi level is below the midgap and so in n-type GaN will not be the most abundant but can still be present in a lower density in addition to C_N.

The presence of both acceptors and donors in a semiconductor leads to a phenomenon called compensation. Compensation occurs when the electrons donated by a donor are accepted by an acceptor and no carriers are available for conduction despite the presence of dopants. The term self-compensation applies when both the donor and acceptor states are a result of the same amphoteric impurity. In this particular case, the donors and acceptors are the C_{Ga} and C_N defects respectively in Figure 2.10. Since the C_{Ga} level is very shallow, all these donors will be ionised at room temperature. In the absence of any other states, this would pull the Fermi level up to near the conduction band. However, with the presence of the C_N acceptor states at 0.9 eV, lifting the Fermi level towards 0.9 eV will begin to cause the ionisation of these acceptors which will push the Fermi level down again. From the discussion above there will always be more carbon acceptors than carbon donors but acceptors will only become ionised to match the charge of the ionised donor density. Therefore in equilibrium an equal number of donors and acceptors will be ionised and the Fermi level will be located in the vicinity of 0.9 eV. This pinning of the Fermi level in the midgap explains the experimental observations of increased resistivity in carbon doped GaN.

The high acceptor concentration pinning the Fermi level in the lower half of the bandgap makes GaN:C slightly p-type [41] and the hole concentration, p, can be calculated using standard equations for compensated semiconductors [97];

$$p = -\frac{N'_V + N_D}{2} + \frac{\sqrt{(N'_V + N_D)^2 + 4N'_V(N_A - N_D)}}{2} \tag{2.8}$$

Here, N_A and N_D are the acceptor and donor densities respectively and N'_V is the adjusted effective density of states in the valence band, since the acceptors are only partially ionised. This adjusted density of states is defined as

$$N'_V = \frac{N_V \exp(-E_A/k_b T)}{2} \tag{2.9}$$

where E_A is the difference in energy between the trap level and the valence band edge and N_V is the effective density of states, which laterally in GaN is $8.9 \times 10^{15} \times T^{3/2}\text{cm}^{-3}$. Since the carbon acceptor level is deep, N'_V is very small and is treated as $N'_V << N_A, N_D$. Under this

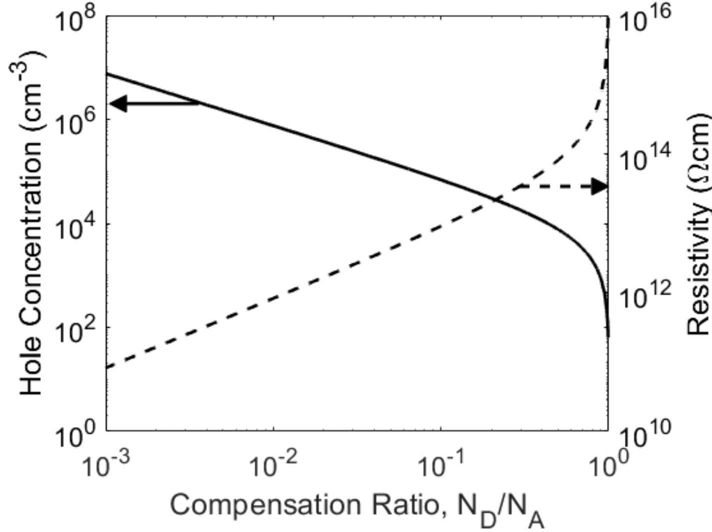

Figure 2.11: The hole concentration and resistivity of carbon doped GaN as a function of the compensation ratio, plotted from Equations 2.8, 2.10 and 2.11. This result is independent of the carbon density though a value of 10^{18} cm^{-3} was used in this plot at a temperature of 20 °C.

assumption, it has been shown that a Taylor expansion of this expression about $(N_A - N_D) = 0$ gives an excellent first order approximation of the hole concentration as [98]

$$p = N_V'(\frac{N_A}{N_D} - 1) + \mathcal{O}(N_V'^2) \tag{2.10}$$

Second order terms of this expression are negligible since N_V' is so small. Equations 2.8 and 2.10 are plotted, indistinguishably in Figure 2.11 along with the resulting resistivity, ρ, calculated by

$$\rho = (ep\mu_h)^{-1} \tag{2.11}$$

where μ_h is the hole mobility, assumed to be 10 cm^{2}V^{-1}s^{-1}.

Therefore, in a compensated material, Equation 2.10 demonstrates that the carrier concentration is determined by the ratio N_D/N_A alone, and not the net dopant density. This ratio is defined as the compensation ratio and through the carrier concentration, sets the material resistivity. In the special case of both the donor and acceptor being shallow with the total dopant density much higher than the intrinsic carrier density, and neglecting carrier freeze-out, equation 2.8 can be instead approximated as $p \simeq N_A - N_D$ [99], but this is not the case here. This understanding is relevant to Chapter 4 which explores the value of the carbon self-compensation ratio in AlGaN.

2.4.4 Capacitance in semiconductors

A depleted region in a semiconductor may exist at a junction as carriers are driven away by a built-in junction potential. If the edges of the depleted region are approximated to be abrupt, it can be treated as the dielectric of an ideal parallel plate capacitor. With this depletion approximation,

several properties of the materials and the junction can be extracted. From electrostatics, the depletion width, W_d, of a highly asymmetric pn junction or a Schottky junction can be expressed as

$$W_d = \sqrt{\frac{2\epsilon}{qN_D}(V_{bi} - V)} \tag{2.12}$$

where ϵ is the permittivity of GaN, N_D is the dopant density of the lower doped material, V_{bi} is the built-in junction potential and V is the applied bias. It is apparent from this equation that the depletion width expands with increasing applied reverse bias. As such, the capacitance is also a function of voltage, expressed as

$$C(V) = \frac{\epsilon A}{W_d(V)} \tag{2.13}$$

where A is the area of the junction. Therefore, measurements of the capacitance can be used to identify the depletion width as a function of voltage. The doping density, and built-in junction potential can also be extracted with this technique using the following analysis.

A small increase in the reverse bias, dV, causes a small volume of material at the depletion edge to become depleted, expanding the depletion volume. To do this, a number of carriers, carrying a total charge of dQ, must be swept out of the newly depleted region. By definition, the capacitance measures this change in charge with voltage since

$$C = \frac{dQ}{dV} \tag{2.14}$$

The charge that left the depletion region can be expressed as

$$dQ = qAN_D dW \tag{2.15}$$

Therefore, combining equations 2.14 and 2.15, the capacitance of the depletion region can be written as

$$C = qAN_D \frac{dW}{dV} \tag{2.16}$$

Differentiating equation 2.12 with respect to voltage and substituting into equation 2.16 removes the depletion width term and gives

$$C(V) = qAN_D \sqrt{\frac{\epsilon}{2qN_D(V_{bi} - V)}} \tag{2.17}$$

where the dependence of the capacitance on voltage as been made explicit. Re-arranging this result in terms of $1/C^2$ gives

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{qA^2 N_D \epsilon} \tag{2.18}$$

There are a few useful reasons to re-plot capacitance data as $1/C^2$ against voltage as in Figure 2.12. Firstly, using equation 2.18, the doping density can be derived from the gradient in Figure

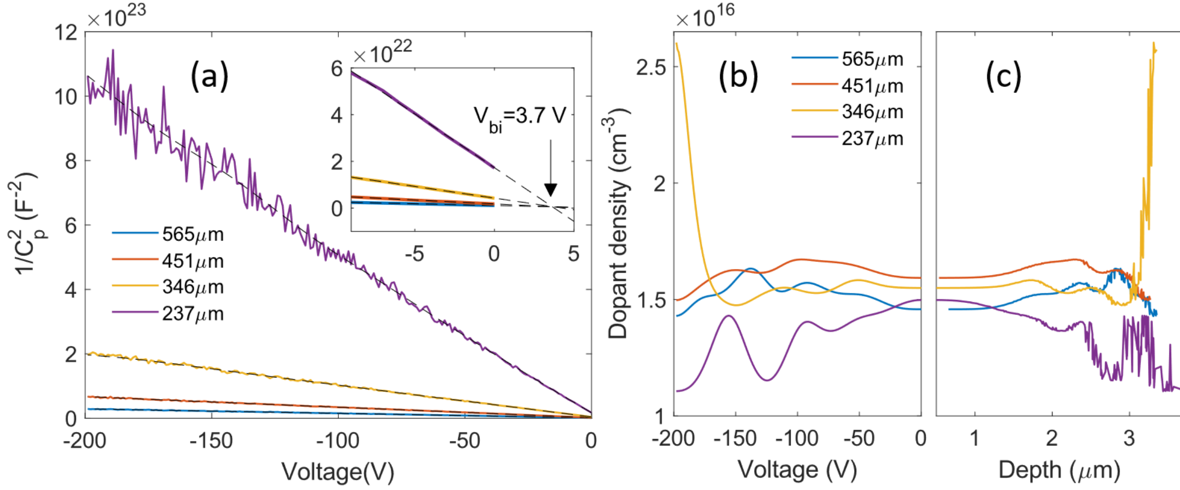

Figure 2.12: (a) Capacitance-voltage data of various diameter diodes plotted as $1/C^2$. Inset, the data near zero was extrapolated to find the built-in junction potential. The dopant density is shown as a function of (b) voltage and (c) depth using equation 2.13.

2.12(a) with some other constants. As a plot of equation 2.18 will be a straight line provided the doping is constant, it is easy to see changes in the doping with depth. Secondly, as the value of $1/C^2$ is only sensitive to the dopant density at the depletion edge, as this edge moves through the sample with increasing applied voltage, the dopant density through the full volume of the sample can be profiled as demonstrated in Figures 2.12(b) and 2.12(c). Finally, by linearly extrapolating the $1/C^2$ curve to $V = 0$, the built in junction potential can be determined (inset to Figure 2.12(a)).

2.4.5 Transport mechanisms

Beyond carrier promotion to the conduction or valence bands, there are other, non-Ohmic, means of transport by which leakage processes can occur. Direct tunnelling of carriers can occur through a barrier that is sufficiently thin, shown in Figure 2.13(a). The likelihood of this occurring decreases exponentially with barrier thickness so this is only possible over very short distances in the order of 1 nm. Tunnelling through thicker barriers is possible by (multi-step) trap assisted tunnelling (TAT) wherein the carrier tunnels a shorter distance to an unoccupied defect state within the barrier as one or more intermediate steps (Figure 2.13(b)). With the built-in electric fields of III-nitrides or with an applied bias, barriers can become triangular and this enables Fowler-Nordheim tunnelling; tunnelling to the conduction band of the barrier. This is shown in Figure 2.13(c) and provides a shorter tunnelling distance than the total barrier thickness. Another field enabled mechanism is Poole-Frenkel barrier lowering, shown in Figure 2.13(d). This is not directly a conduction mechanism but rather field assisted emission which can lead to current flow when repeated. The lowered barrier reduces the energy required for detrapping, reducing the effective depth of a trap.

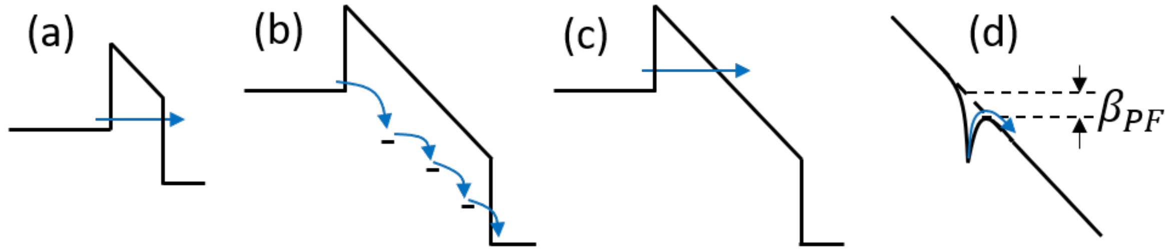

Figure 2.13: Transport mechanisms are presented through a barrier by (a) direct tunnelling, (b) trap-assisted-tunnelling, (c) Fowler-Nordheim tunnelling and (d) Poole-Frenkel barrier lowering where β_{PF} is the extent of the barrier lowering.

Table 2.2: The dependence of various conduction mechanisms on electric field (E) and temperature (T). This table was adapted from [103].

Mechanism	Expression	E-Field dependence
Poole Frenkel [100]	$I = I_0 \exp\left(\frac{\beta_{PF} E^{0.5}}{k_B T}\right)$	$\ln(I) \propto E^{0.5}$
Variable range hopping [101]	$I = I_0 \exp\left(\frac{CE}{2k_B T}\left(\frac{T_0}{T}\right)^{0.25}\right)$	$\ln(I) \propto E$
Surface leakage [102]	$I \propto \left(\frac{E}{\rho}\right)$	$I \propto E$

β_{PF} is the lowering of the barrier shown in Figure 2.13(d), C is a constant and T_0 is a characteristic temperature.

Similar to multi-step trap-assisted-tunnelling is the mechanism of variable range hopping (VRH) which equally involves carriers sequentially occupying multiple point defect states to cross a barrier. However, in the case of variable range hopping, each hop is thermally activated into states which are classically accessible and no tunnelling is required. Because of this, a variable range hopping current exhibits a temperature dependence while a trap-assisted-tunnelling current does not. Another leakage mechanism is hopping along surface states which exist from dangling bonds at the crystal surface. The dependence of this mechanism and those previously mentioned on electric field and temperature are shown in Table 2.2 with the exception of tunnelling mechanisms. Tunnelling currents are dependent on the barrier thickness and the density of states either side of the barrier and therefore are not dependent on temperature and have a more complicated dependence on voltage.

As stated in section 2.3.1, the presence of dislocations can give rise to leakage paths. It was originally thought that the very high dislocation densities in GaN would lead to rapid failure as the material degraded under stress due to the high number of leakage paths, as had been seen in II-VI semiconductors [104]. In this respect GaN is unusual and it appears that a large fraction of the dislocations are not electrically active. Recent work by Usami et al. identified the location of leakage paths in a structure using IR emission microscopy [105]. Cathodoluminescence (CL)

images of the same sample showed numerous dark spots signifying extended recombination centres. However, not all of the dark spots coincided with leakage points indicating the presence of non-leaky extended defects. Transmission electron microscope images of cross-sections taken through the leaky dislocations showed only pure screw dislocations with a Burgers vector of 1c [105]. Study of the current voltage characteristics of dislocation leakage and correlation with the dislocation density indicates that the mechanism for this transport is variable range hopping [106], along sites in the dislocation cores [107].

An additional method available for probing the conductivity of dislocations is conductive atomic force microscopy (CAFM). It has been observed that after surface etching, dislocations form pits with the pit size depending on the Burgers vector. Therefore the pit size and the conductivity can be correlated to the dislocation type. This was attempted by Cao et al. [108] however, analysis of conductive atomic force microscopy results requires great care; since the tip current depends on the contact area and force between the tip and the surface, scanning over a pit will always increase the leakage current when pushing forward up out of a pit. This issue of topology artefacts makes drawing conclusions from this technique challenging.

2.5 Reliability

Despite the promising material properties of GaN and the ability to fabricate lateral and vertical devices, there are still a number of reliability issues which need to be resolved. In lateral devices, although already in the early stages of commercialisation, HEMTs continue to suffer from issues related to the management of peak electric fields. While regarding the more early phase vertical devices, these challenges are related to optimising device designs but are equally related to electric field management, particularly at device edges. An ideal transistor presents an infinite resistance in the off-state and zero resistance in the on-state. In reality neither of these are ever true, but a constant, low on-state resistance is desired.

2.5.1 HEMT reliability

First discussing lateral GaN HEMTs, one reliability issue is current collapse. For a normally-on HEMT in the off-state, the gate is at a negative potential and the drain is at a large positive potential. The drain potential is dropped both laterally and vertically and results in high electric field regions. In these regions, 2DEG electrons can be accelerated to high energies and become trapped in acceptors in the GaN:C. This introduces a population of negatively charged trap states below the channel in the off state. When the device is turned on by setting the gate voltage to 0 V, the 2DEG channel does not fully recover because the negatively charged traps below it act as a back gate. Over time, these defect states thermally de-trap and the 2DEG density recovers to the initial density. This phenomenon is referred to as current collapse since the channel current is lower (has collapsed) after switching back to the on-state compared to the channel current

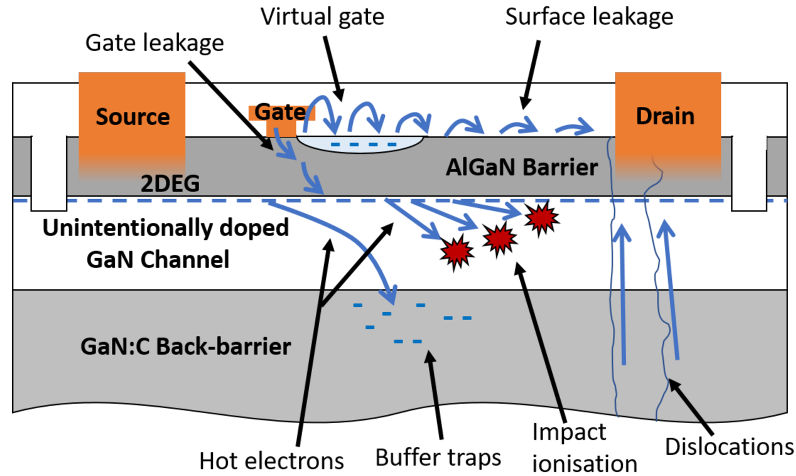

Figure 2.14: An illustration of the primary degradation mechanisms governing the reliability of AlGaN/GaN HEMTs as well as leakage and reversible charge storage phenomena.

before switching the device off. This phenomenon is equally described as dynamic on-resistance, referring to the higher than nominal channel resistance after switching to the on-state which gradually reduces to the nominal on-resistance. Both of these terms are used in equal measure but are both referring to the same physics. Dynamic on-resistance directly translates into power losses during switching since an increase in the on-resistance increases joule heating. However, the magnitude of the losses in a power converter will depend on the duty cycle of the switching. If the device is in the off-state most of the time, the buffer will not have time to de-trap and the channel resistance would be permanently higher, but if the device is mostly in the on-state, there will be little time for trapping and the on-resistance will remain low. A typical limit imposed on the dynamic on-resistance is a maximum increase in the on-resistance of 10% after switching on compared to the on-resistance before switching the device off.

The source of the increased on-resistance is the continued partial depletion of the 2DEG after the channel is turned on and is related to trapped charge on the surface and in the buffer. For both normally-on and normally-off devices in the off-state, the device experiences high electric fields between the gate and the drain. In the buffer this can mean the generation of hot electrons, which have been accelerated to have a kinetic energy far greater than the conduction band edge. These electrons can easily transit into the buffer where they are trapped in deep states with long time constants. On the surface, states associated with dangling bonds can allow surface hopping and the occupation of these states. If unaddressed, electrons can migrate onto the surface of the barrier from the gate, effectively increasing the gate length. This is referred to as a virtual gate [109]. After switching to the on-state, the electrons in the surface states remain, and continue to partially deplete the 2DEG. Likewise, the charged buffer traps act as a back-gate, partially depleting the 2DEG from the bottom. These charge storage phenomena are shown in Figure 2.14

as negative charge around the 2DEG.

Surface related current collapse can be resolved by the use of a passivation layer which reduces the density of surface states [38, 110, 111]. Additionally, surface migration can be further curbed by reducing the surface electric field at the gate edge. This can be done through the use of properly designed field plates [112–115]. Field plates are the extension of the contact metals laterally above the device. The T shaped gate and the source and drain field plates in Figure 2.6, reduce the peak electric field by causing the gate-drain voltage to be dropped at the edge of each field plate rather than all at the drain side of the gate edge [114–117]. The electric field is further reduced by increasing the gate-drain separation. For this reason, the gate is closer to the source to provide a larger distance over which the potential is dropped when the drain is biased. Field plates redistribute the electric field both on the surface and in the channel. In the semi-on state, the reduction of peak electric fields reduces impact ionisation, which can otherwise lead to degradation and accelerated device failure. Therefore this part of the device design also increases the lifetime of GaN based devices [118, 119].

The issue of buffer related current collapse has proved more difficult to address. Deep levels in the buffer layers are invariably present from unintentional dopants and even required to increase the resistivity of the buffer (see section 2.4.3). Therefore, rather than minimising the density of buffer traps, their impact can be managed by allowing them to discharge more quickly. This has been approached by reducing the resistivity of the top of the stack which has the effect of injecting positive charge from the surface and expediting the neutralisation of the buffer [42]. It has been shown that processes which result in positive buffer charge injection can successfully reduce buffer related current collapse in this way [120]. The on-resistance determines the conduction losses which along with switching losses make up the total power losses. Therefore, resolving current collapse is essential for realising low loss devices [40, 121].

The magnitude of the leakage currents in the off-state places another constraint on the device performance since any leakage current represents another loss mechanism and the possibility of device degradation [122]. Unlike in the on-state, the drain bias will be much higher than the source, gate and substrate and the resulting electric fields can give rise to high off-state leakage currents and hot electrons. Lateral gate-drain leakage on the surface can generally be suppressed by a good passivation layer and well designed field plates, just like the virtual gate [113]. Lateral source-drain leakage can also occur through the buffer, below the gate depletion region. This is referred to a punch through and is the reason for carbon doping the layer below the channel, rendering it highly resistive and minimising such lateral leakage [123, 124]. Finally, vertical drain-substrate leakage can also occur and effectively limits the maximum device operating voltage. This vertical leakage can be managed by increasing the total thickness of the epitaxy as well as increasing the resistivity of the buffer and strain relief layers by carbon doping. Therefore, as the solution for off-state leakage is to increase the density of trapping defects, there is an apparent trade off between buffer related current collapse and off-state leakage [125].

2.5.2 Vertical device reliability

As introduced in 2.2.3 the development of vertical GaN devices is an active research field with a wide variety of design concepts. Beyond material quality and cost which are continuously improving, the primary challenge faced by vertical GaN devices is the optimisation of electric field management at the device edges. Unlike in lateral devices, vertical transistors do not suffer from current collapse or virtual gate issues. As can be seen in Figures 2.8(c)-(f), with the drain on the substrate, the surface contacts consist of only the source and gate terminals yielding low surface fields and so completely resolving virtual gate and surface leakage issues. Furthermore, as buffer conduction is a requirement in the off-state, there is no intentional carbon doping and so no buffer related current collapse. However, for vertical transistors in the off-state and vertical diodes in reverse bias, high voltages are blocked across the device creating high vertical electric fields. In the bulk of the device, the breakdown field of high quality GaN can begin to approach the material limits. However, device failure is determined by the weakest point of the device which is the periphery. Here, the material may be defective due to implant isolation or surface states may be present from mesa etching. The solution to this issue is the implementation of an appropriate edge termination method.

2.5.2.1 Edge termination

In addition to extending the breakdown voltage, it has also been indicated that management of surface failure at the edge of vertical devices is the key to avalanche breakdown, a requirement for robust operation [19]. Edge termination is all about extending the distance over which the potential is dropped. In Si and SiC devices, a typical edge termination method is junction termination extension (JTE) [126, 127]. Junction termination extension involves the inclusion of a lower doped region around the surface of the structure which reduces the peak fields by increasing the width of the depletion region. A qualitative sketch of the electric field profile after junction termination extension is shown in Figure 2.15(b) compared to an unterminated structure in Figure 2.15(a). Junction termination extension can be taken even further with field rings which are annular ion implanted regions around the device of varying width and separation. Correctly implemented, these selectively doped rings distribute the electric field, dropping the potential over multiple junctions and thus reducing the peak electric field as shown in Figure 2.15(c). In some materials such as Si, where the diffusion rate is sufficiently high, the selectively implanted field rings can be annealed to drive-in and spatially redistribute the dopants. This results in the new dopant distribution shown in Figure 2.15(d) and the electric field is spread yet more evenly. These edge termination methods are a commonly implemented solution in more mature semiconductors such as Si and SiC and adaptation of these edge termination methods to GaN has been attempted with some success, both with termination extension [34, 128, 129] and field rings [130, 131]. However, these processes are more difficult in GaN due to material processing challenges related to the activation of selectively doped areas [132]. Due to the immaturity of

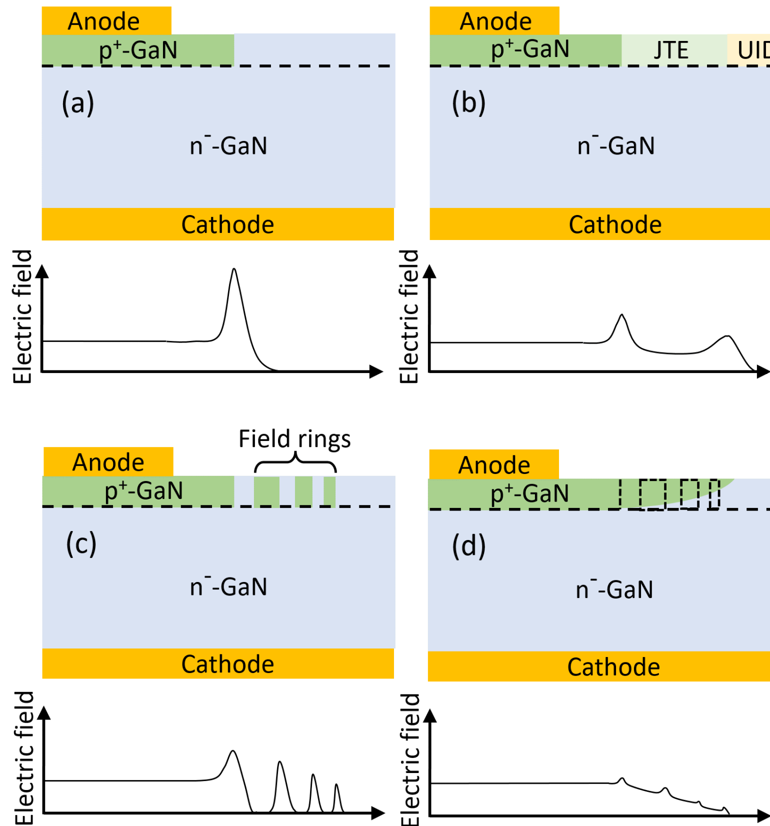

Figure 2.15: Vertical pn diodes with (a) no edge termination, (b) junction termination extension (JTE), and (c) field rings. Annealing of the field ring structure gives the dopant distribution shown in (d). A sketch of characteristic electric field profiles along the dashed lines are shown below each diagram. The peak electric field is much higher in the geometry with no edge termination.

selective area doping technologies in GaN, the resulting implanted material is highly defective and yields low quality devices [75]. As such, the development of edge termination technology has been identified as the target of future optimisation work [133].

An alternative and immediately achievable edge termination method in GaN devices is to bevel the structure. A properly designed bevelled edge on a planar pn junction can result in a reduction of the electric field on the surface. This increases the likelihood that breakdown will occur uniformly in the bulk and not unpredictably at the surface. A schematic example of how this can be done is shown in Figure 2.16. The surface field is reduced by redistributing the voltage drop to change the surface field profile [134]. This is only effective for small bevel angles after which the peak surface field rises above the peak internal field [135]. In this small angle range bulk breakdown is ensured, however at a fraction less than the ideal infinite planar junction, determined by the bevel angle. [136]. The effectiveness of the bevel in reducing the surface field compared to the bulk field is influenced by the doping levels. Calculations suggest that increasing

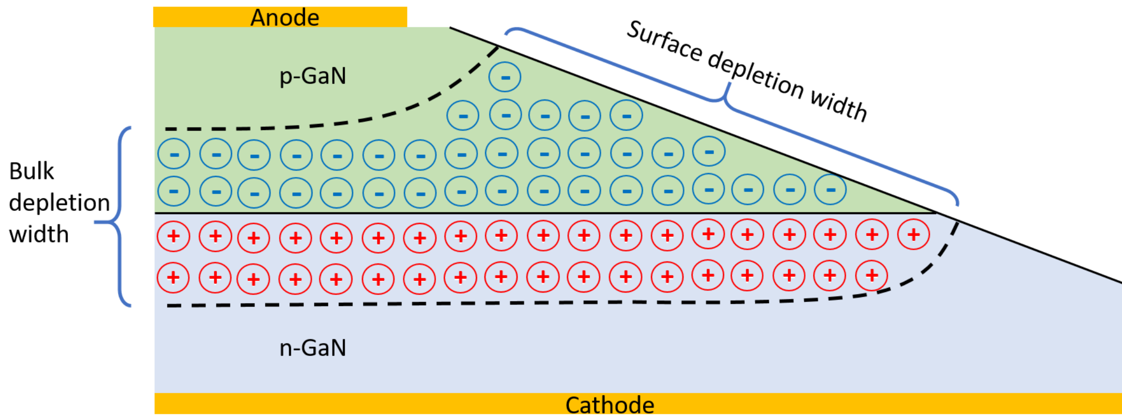

Figure 2.16: A schematic of the bevelled edge of a planar pn junction with equal doping densities. The dashed lines represent the depletion edge. In the depletion region, the space charge is shown and must be equal on each side of the junction. Where the pn junction reaches the surface, the lack of p-type material requires it to depleted further away from the junction to match the positive space charge in the n side. This results in an increased depletion width and a reduced surface electric field.

the background donor density in the n-type drift region would increase the bulk field, and the surface field would also increase but to a lesser extent [135]. This indicates that the bevel is more effective at higher doping densities since the surface field is a smaller fraction of the bulk field. The surface depletion width is extended since where the junction meets the surface, there is not sufficient p-type material to match the charge exposed in the n-type material, and so the depletion on the p-side must extend further up the bevel. This extension of the depletion width by depleting the material up to the surface is a similar principle to the reduced surface field (RESURF) effect which can increase the breakdown voltage in lateral GaN devices [137]. Management of the surface electric field is critical to reduce surface related reverse bias leakage. Surface states can give rise to a hopping current across the junction in this device geometry. As with surface issues on HEMTs, this can be addressed with a good passivation layer and by reducing the electric field, in this case by a bevelled edge termination. This principle of tapering edges to reduce peak fields has already been applied to vertical transistors [138]. As edge termination can extend the device operating voltage, it can be useful to study the effectiveness of different termination techniques using more simple structures such as pn diodes. As with test structures, studies of simple devices like pn diodes provide the foundations for more complicated structures such as the advanced schottky barrier diodes and vertical transistors of Figure 2.8.

Chapter 3

Characterisation techniques

To build up a physical understanding of device behaviour, various characterisation techniques have been employed in this thesis. This section begins by detailing the capabilities of the laboratory instrumentation and then goes on to detail the experimental methods and simulation processes applied in later chapters.

3.1 Measurement capabilities

3.1.1 Measurement environment

The devices throughout this work are unpackaged and measured on-wafer. This allows rapid feedback in device development as new samples can be measured and characterised without the need to spend time and money developing and optimising packaging. On-wafer measurements also allow finer control of the device conditions such as temperature and optical inspection of the device after breakdown is simple. However, on-wafer measurements require the use of a probe station and, in this case, extended cabling to source measurement units which cause the test circuit to have a high loop inductance. This limits the speed at which a device under test can be switched and the maximum switching speed of a device may be difficult to assess. Measurement of this device parameter is crucial for estimating switching losses. Quantitatively, the inductance of a typical power switching circuit is ~ 2 nH, whereas an estimate of the loop inductance of a probe station used in this work is around 100 times higher. In this thesis, all measurements were at sufficiently low frequencies that they were not affected by this limitation. Performing electrical measurements in the dark is important for unpackaged semiconducting devices since any light can affect the results, either by increasing the carrier density through photo-excitation or by introducing photo-currents. To avoid this problem, measurements were carried out in darkness

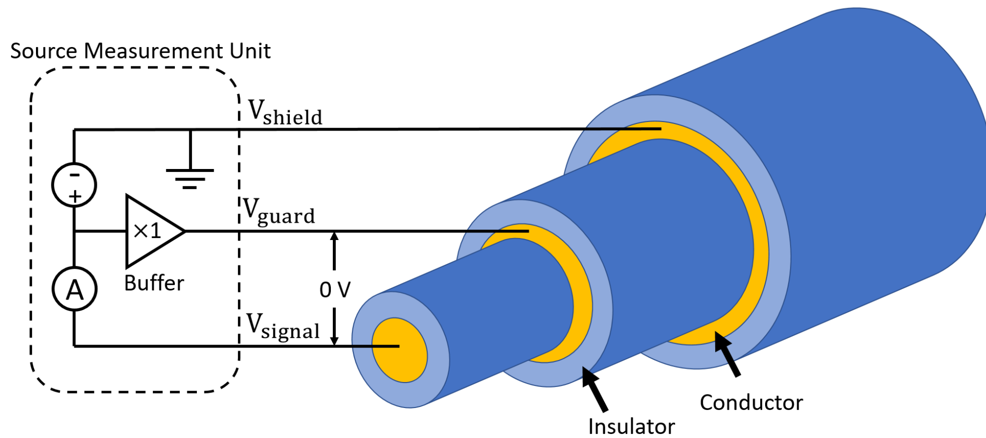

Figure 3.1: A cross-section of a triaxial cable with a diagram of the simplified biasing circuitry internal to the source measurement unit. Current measured by the source measurement unit cannot be attributed to leakage through the cable dielectric since the buffer input presents an ideally infinite impedance and there is no potential difference between the signal and guard.

inside a measurement enclosure. Since these enclosures are metallic they also act as a Faraday cage and help with the reduction of EM noise and interference.

3.1.2 Triaxial cabling

The grounded shield of co-axial cabling offers shielding of the core signal from electromagnetic interference. Coaxial cable is thus well suited for sensitive electrical measurements. However, at very low currents, leakage in the dielectric between the core and shield can become significant and mask the measurement signal. This can be addressed by the inclusion of an additional concentric sheath between the core and shield, referred to as the guard. As shown in Figure 3.1, the guard is biased through a current buffer to the same potential as the core and as such, there is no electric field across the dielectric surrounding the core. Thus, no leakage current due to the cable is present during low current measurements. Leakage from guard to shield remains present but this current is provided from the current buffer and so not included in the current measurement.

3.1.3 Probe stations

Measurements were performed on probe stations from Wentworth labs. These are composed of a top illumination microscope above a chuck for device positioning and probing and surrounded by space for magnetically attached micro-positioners. This is shown in Figure 3.2 inside the dark measurement enclosure. The probe stations and chucks are massive to reduce the amplitude of any vibrations. The positioners each have three degrees of translational freedom with a 3 μm

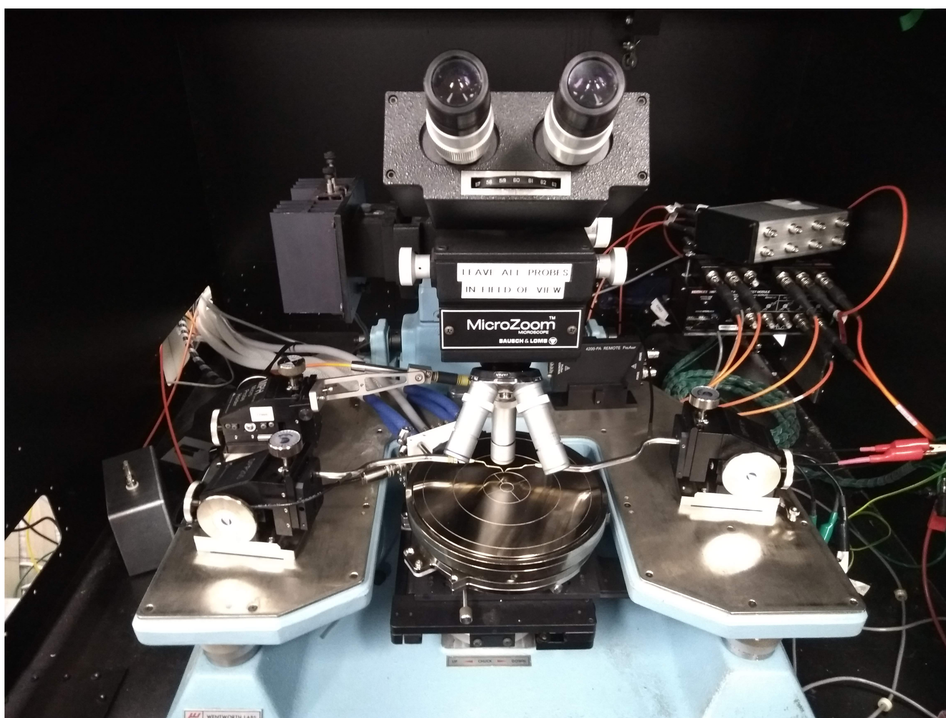

Figure 3.2: The probe station inside the measurement enclosure with a top illumination microscope, micro-positioners and a guarded chuck.

spacial precision and with a tungsten probe tip of nominally 5 μm diameter. As with triaxial cabling, the chuck is guarded; the top surface of the chuck sits on an insulator on top of another conductor, biased at the same potential through a current buffer. This way the chuck surface is guarded and ensures that current measured from the top conductor must be from the device under test since there are no other electric fields.

For measurements at elevated temperatures, the chuck contains resistive filaments which offer heating to a maximum temperature of around 300° C. In addition, the chuck can be actively cooled by pumping an ethylene-glycol based coolant through channels below the chuck. With both heating and cooling, the chuck temperature can quickly reach any set-point using a proportional-integral-derivative (PID) controller. The temperature of the chuck in Figure 3.2 is controlled by varying the heater power and coolant circulation via pulse width modulation (PWM). This is common for proportional-integral-derivative controlled heaters since it is cheap and easy to implement, however, pulse width modulation introduces unmanageable RF noise to low current measurements. Therefore, for measurements requiring very low noise ($<$ pA) at high temperatures an alternative method of regulating the current is required such as adjusting the magnitude of an applied DC voltage.

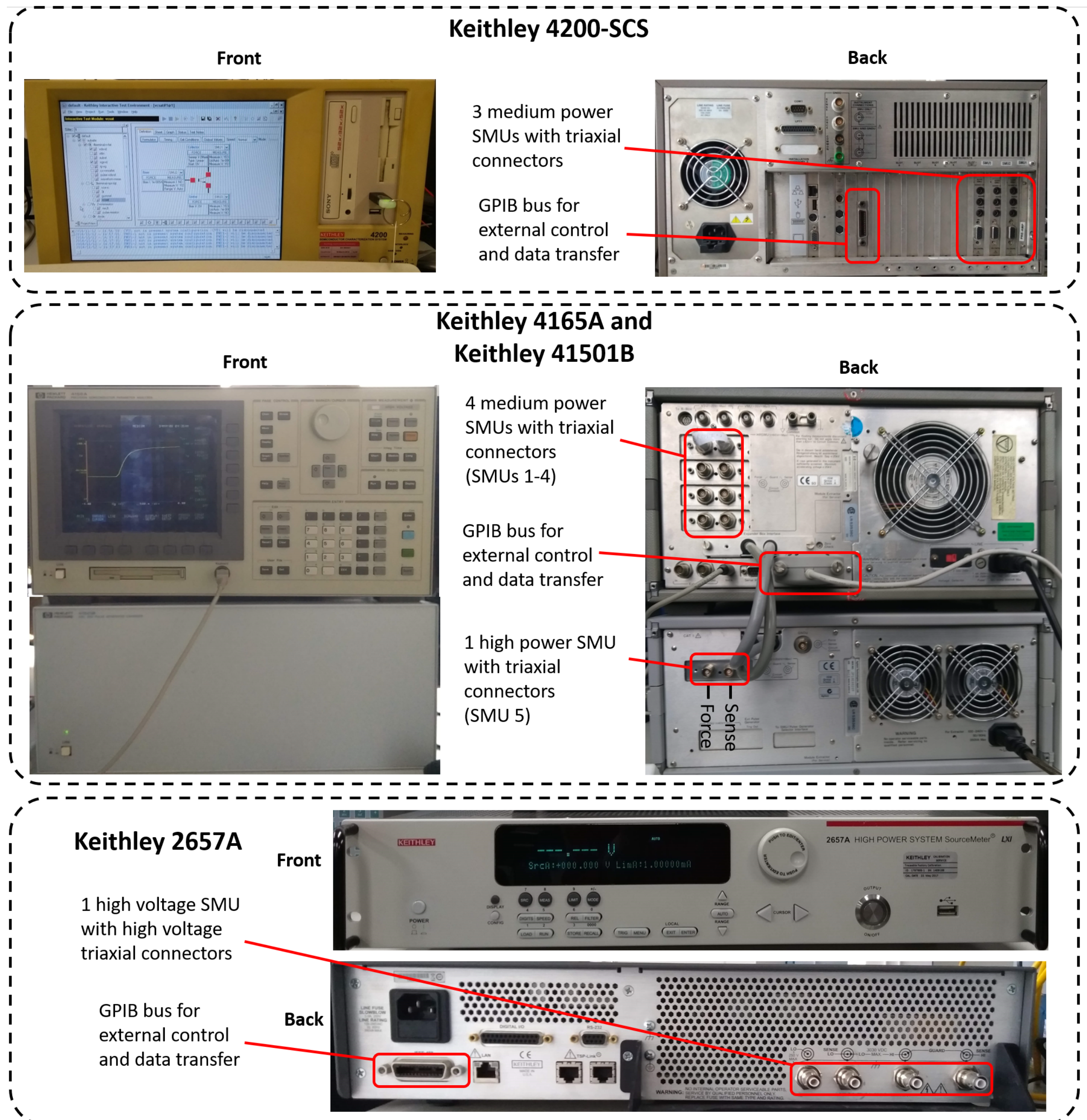

Figure 3.3: The semiconductor characterisation instrumentation available in the laboratory and their connectivity.

3.1.4 Laboratory Instrumentation

The laboratory is equipped with a number of source measurement units (SMUs) which are measurement instruments capable of sourcing either a current or voltage while simultaneously measuring the other. These units typically have two tri-axial connections for force and sense permitting kelvin configuration measurements. Each of the three systems have different capabilities as outlined below and shown in Figure 3.3.

Firstly, the Keithley 4200-SCS instrument has four medium resolution source measurement units with a current resolution down to 100 pA and a voltage range of ±200 V. In addition the system is equipped with a high voltage capacitance measurement unit (CMU) allowing CV measurement up to 200 V with the use of bias tees and in the frequency range of 10 kHz to 100 MHz. The system can also be configured with a low current pre-amplifier unit which improves the current resolution of one source measurement unit to 10 fA. The HP 4156A is composed of four high resolution source measurement units with a maximum current resolution of 1 fA and a voltage range of up to ±100 V. This is accompanied by the 41501B expander unit which adds an additional high power source measurement unit with a voltage range of up to ±200 V and current resolution of 1 nA. Lastly, the Keithley 2657A is a single high power source measurement unit sourcing up to ±3 kV at 1 mA or ±100 V at 100 mA with nA resolution. For safety, each system is equipped with an interlock connected to a micro-switch on the enclosure door. If the enclosure is opened while a source measurement unit is supplying a lethal voltage, the interlock is triggered and all voltage sources are set to zero volts. All of these instruments are equipped with a general purpose interface bus (GPIB) enabling external control for measurement automation and coordination making possible the simultaneous use of multiple systems for the same device measurement. The latter may be required in some measurement techniques, for example, when applying high voltages but measuring small currents as is the case in Chapter 7. The national instruments software, LabVIEW, was used for this purpose. New control programs were written by the author and existing programs were modified to perform the measurements in this thesis.

3.2 Electrical Characterisation Techniques

The primary measurement techniques applied in this thesis are outlined in this section.

3.2.1 Current-voltage

Measurement of current-voltage (I-V) characteristics is a simple but very effective characterisation tool. By rescaling the results with the dimensions of the device, the I-V can be expressed in terms of the current density versus electric field (J-E). The dependence of the current density on the electric field can be used to identify the transport mechanism based on known relations [139] such as those shown in Table 2.2. The dependence of the I-V on temperature can also be studied to determine if the transport process is thermally activated. This is performed by changing the

chuck temperature to set the temperature of the sample. Using the Arrhenius equation,

$$I = I_0 \exp\left(\frac{E_A}{k_b T}\right) \tag{3.1}$$

the current dependence on temperature can be used to extract an activation energy, E_A, often corresponding to the trap energy responsible for the leakage. Current-voltage sweeps form the basis of all electrical characterisation and as such, are used throughout this thesis.

3.2.2 Capacitance-voltage

One method to measure the capacitance of a sample is the capacitance-voltage (CV) technique. This entails applying a small amplitude AC signal across the sample which is modelled as a leaky capacitor. The current which flows through a leaky capacitor with parallel capacitance, C_p, and resistance, R_p is expressed as

$$I = \frac{V}{R_p} + iV\omega C_p \tag{3.2}$$

where ω is the angular frequency of the applied voltage and i is the imaginary unit due to the phase shift of 90°. The amplitude and phase of the measured current is fit to this model to extract the material parameters. Throughout this measurement a DC bias can be applied to the sample which is isolated from the small amplitude AC signal by a bias tee. This works well since the inductor in the DC branch of the bias tee presents no impedance to the DC voltage but presents a high impedance to the AC signal and the opposite is true for the capacitor in the AC branch. By varying the DC bias, the capacitance and depletion width can be identified as a function of voltage. As explained in section 2.4.4, this data also facilitates the extraction of the dopant density, profiled as a function of distance, and the built-in junction potential. It is necessary to perform a calibration of the system to correct for the capacitance and inductance of the system and setup. This is approached by assuming any parasitic capacitances are in parallel with the device under test and so simply add together. Parasitic inductances are treated as in series and measurements at multiple frequencies are used to distinguish these elements through their frequency dependence [140]. With the Keithley capacitance measurement unit used here, the calibration process is automated. With the device under test removed from the setup, the response of the system is measured and from this, a correction is applied to future measurements. This capacitance-voltage technique is primarily used in Chapter 6 to characterise the size of the depletion region of a pn diode and to profile the uniformity of the dopant density through the drift region.

3.2.3 Quasi-static capacitance-voltage

The Keithley capacitance measurement unit used for the capacitance-voltage technique described above is limited in frequency range to a minimum of 1 kHz [141]. In practice, measurements at frequencies below 10-100 kHz are obscured by noise and so it is not possible to use this

technique. However, measurement at low frequencies may be desired, for example, to measure slow dynamics such as RC networks with time constants much longer than the period of the small amplitude signal. In this case, a different approach can be taken in the form of the quasi-static capacitance-voltage (QSCV) technique. This entails applying a constant voltage ramp across the sample and measuring the resulting current. From the definition of a capacitor, $Q = CV$, the time derivative gives rise to a displacement current, I_{disp}, of

$$I_{\text{disp}} = C\frac{dV}{dt} + V\frac{dC}{dt} \tag{3.3}$$

Assuming a constant capacitance such that $dC/dt = 0$, the second term goes to zero and the displacement current is directly related to the capacitance. In reality, the measured current will be the sum of this displacement current and any leakage current. Conveniently, the displacement current is separable from the leakage current since it depends only on the ramp rate of the voltage and not the magnitude or polarity. That is, reversing the direction of the voltage ramp will change the sign of the displacement current but not the leakage current. Therefore, if the polarity of the voltage is kept the same (e.g. always above zero) and the ramp is performed in both directions, the displacement current can be identified from the difference between the two ramp directions.

Another possible addition to the measured current is the effect of trapping or charging. This may increase with voltage and may also partially change sign with ramp direction, and so may introduce some error in the separated displacement current. If present, this contribution adds to the separated displacement current and makes it appear to increase with voltage rather than depend only on the ramp rate. Therefore, this technique is not suited for capacitance measurements on samples which show a very large charge storage. Conveniently, this contribution is often small compared to the displacement current, especially at faster ramp rates.

It is important to ensure that the ramp is smooth and not stepped as would be provided by a source measurement unit. A stepped voltage ramp would result in displacement current spikes during the step followed by a decay during the current measurement. As the source measurement unit integrates the current for some time after the step, this would measure a lower current and underestimate the capacitance. On the other hand, a smooth ramp ensures the displacement current is constant and the full displacement current will be measured, regardless of integration time. This is assuming a constant capacitance which is a fair assumption over a small voltage change.

A smooth ramp was generated by an integrator circuit based on an op-amp with a capacitor in the feedback loop, shown in Figure 3.4. This causes the output voltage, V_{ramp}, to linearly increase at a rate set by the time constant of the RC network and the input voltage, V_{set}. The gain of an op-amp is determined by the ratio of the feedback impedance to the input impedance. Considering the definition of the impedance of a capacitor, $Z_C = 1/i\omega C$, the gain of this integrator circuit is

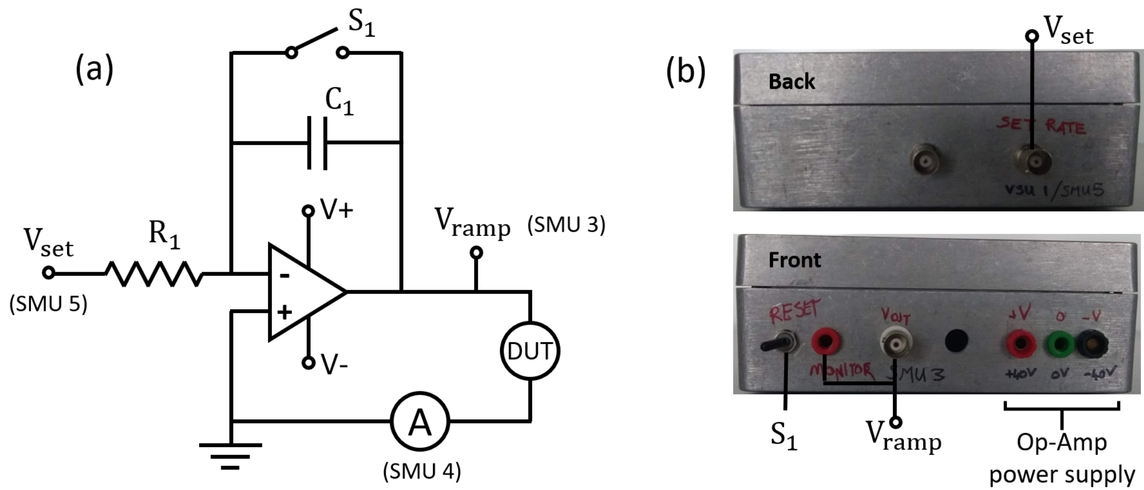

Figure 3.4: The integrator circuit used to generate the ramp is shown in (a) along with the labels of the source measurement units used for each task. Photographs of the ramp generator as shown in (b) with the terminals labelled.

given by

$$G = \frac{1}{i\omega C_1 R_1} \tag{3.4}$$

This equation describes the gain if V_{set} is an AC signal. If V_{set} is constant, the gain can be described (as derived here [142]) by the dimensionally equivalent form

$$G = \frac{t}{R_1 C_1} \tag{3.5}$$

which results in the output voltage, V_{ramp} increasing over time until the op-amp saturates at one of its voltage rails (40 V in this case). This circuit was used in conjunction with the Keithley 4156A and 41501B systems to set the ramp rate by applying a constant voltage to the V_{set} terminal using source measurement unit 5. Source measurement units 3 and 4 were then used to measure the voltage applied to and current flowing through the device under test. A switch was included in the circuit to discharge the capacitor, as required, before beginning a ramp. This technique is used in Chapter 5 to measure very low frequency capacitance.

3.2.4 Back-biasing

The back-biasing technique, also referred to as the substrate bias ramp or substrate bias technique is a method of identifying charge movement in the epitaxy below the 2DEG. A small potential difference is applied between two contacts in the same active area to monitor the conductivity of a 2DEG resistor. This is normally 0 V and 1 V as shown in Figure 3.5(a). The substrate is then used as a back gate and ramped to a negative bias to pinch off the 2DEG. This negative substrate bias results in vertical electric fields of the same polarity as in a HEMT with a positively biased drain

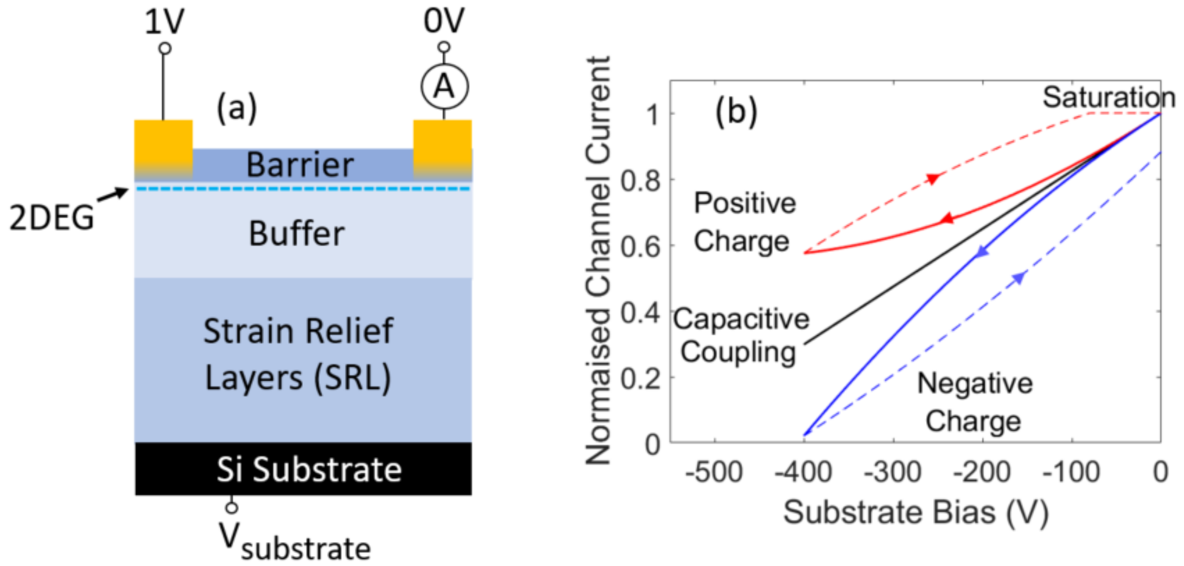

Figure 3.5: (a) A 2DEG resistor is used to sense the substrate bias. (b) An example of the measurement results that are possible from this technique. The measured channel current is normalised to the initial value, effectively normalising the conductivity to the 2DEG area between the contacts. Positive and negative charge refers to the injection of carriers into the buffer which may accumulate or become trapped.

and a grounded substrate. The rate of depletion of the 2DEG by this back gate can be analysed to identify charge movement and storage in the buffer. A useful advantage of this technique is that the 2DEG completely screens the surface from any strong electric fields. Therefore the measurement is sensitive only to charge in the buffer and surface effects can be ruled out. If the stack were an ideal dielectric, the epitaxy could be treated as the dielectric of an ideal capacitor with the 2DEG and substrate as the conductive plates. For an ideal capacitor, applying a bias to one plate would have the effect of inducing a charge of opposite polarity on the other plate of magnitude CV. It follows that applying a negative bias to the substrate would reduce the 2DEG density by CV per unit area. Therefore applying an increasingly negative bias at a constant rate would pinch off the 2DEG at a rate proportional to the stack capacitance per unit area. This is shown as the capacitive coupling line in Figure 3.5(b). Asserting an initial 2DEG density of n_0, the 2DEG density with an applied substrate bias, $n_{2\text{DEG}}$, would deplete as

$$n_{2\text{DEG}}(V) = n_0 - \frac{\epsilon|V|}{d} \tag{3.6}$$

where ϵ and d are the average permittivity and thickness respectively of the stack below the 2DEG.

When analysing measurement data, two deviations from this ideal behaviour are possible; the 2DEG depletes faster than ideal or slower as shown in Figure 3.5(b) . First discussing the 2DEG

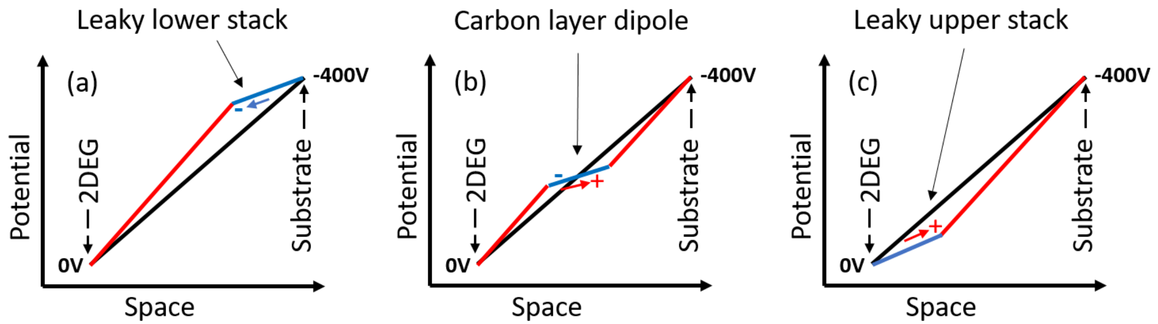

Figure 3.6: The inferred internal potential and charge movement through the epitaxy with a -400 V substrate bias (a) with the lower part of the stack leaking, (b) with a carbon doped region forming a dipole and (c) with the upper part of the stack leaking. The potential in red indicates an increase in the vertical electric field compared to an ideal dielectric.

depleting faster than the ideal case, this must be caused by excess negative charge near the 2DEG. There are two common ways this can occur depicted in Figures 3.6(a) and 3.6(b). Firstly, as the epitaxy begins to exhibit vertical leakage due to the high vertical field, if the lower part of the stack begins to leak first, this causes an injection of electrons from the substrate. Since the same potential must be dropped over the epitaxy it can be seen from Figure 3.6(a) that this must increase the potential in the top of the epitaxy compared to the ideal case. This increased negative potential causes a greater depletion of the 2DEG. An alternative way that excess negative charge can manifest below the 2DEG is the polarisation of carbon doped layers shown in Figure 3.6(b). Carbon is often present is layers below the channel and under a sufficiently high field, holes can be swept away from thermally ionised acceptors. These holes then accumulate or become trapped at a heterointerface lower in the epitaxy. This spatial separation of the positive free holes and negative ionised acceptors creates a dipole layer. The negative pole of this dipole will be closer to the 2DEG since the holes will be swept towards the negative substrate. Therefore the 2DEG will see a net negative charge and deplete more rapidly than in the absence of the dipole layer [120].

The other observable behaviour is the depletion of the 2DEG at a slower rate than expected from an ideal dielectric stack. This can only be attributed to excess positive charge below the 2DEG which acts to screen the 2DEG from the substrate bias. This can occur when, under the high vertical field, the top of the epitaxy begins to leak first. This is shown in Figure 3.6(c) and causes an injection of holes into the epitaxy, reducing the potential under the 2DEG.

When ramping back to 0 V, the stored charge continues to influence the 2DEG density. In the case of positive buffer charge, when the substrate bias is sufficiently small, stored positive charge can lower the barrier confining electrons to the 2DEG. This allows electrons to rapidly neutralise these positive charges and causes a saturation of the 2DEG density near or slightly above the initial unbiased density. Ultimately at the end of the measurement, the 2DEG density is unchanged or slightly higher than the initial density. This makes positive buffer charge

storage benign. In the opposite case, there is no equivalent mechanism to neutralise stored negative charge, meaning it is trapped with much longer time constants, causing the 2DEG density to remain partially depleted after the measurement. This lack of recovery is indicative that transistors on the same epitaxy will suffer from buffer related current collapse as the root cause is the same. Further detail on this analysis technique can be found in other material [42, 143, 144].

3.3 Test structures

Test structures are used to isolate specific device characteristics which cannot be measured on a complete device. For example, contact resistance and the sheet resistance of the 2DEG cannot be distinguished in a HEMT, since they are in series. Both of these quantities should be minimised to reduce conductive losses. These parameters can be quantified through the use of a transfer length measurement (TLM) structure shown in Figure 3.7. The transfer length measurement structure consists of a series of Ohmic contacts connected by a 2DEG, each increasingly further apart. By measuring the resistance between two contacts at various separations, the 2DEG sheet resistance and contact resistance can be distinguished. On a graph of resistance vs. length of 2DEG, the y-intercept is twice the contact resistance and the gradient is the 2DEG sheet resistivity. Extrapolating this line back to the negative x-axis gives two times the transfer length. During the measurement, current flows laterally in the 2DEG under the contact metals for a distance determined by the 2DEG sheet resistance and the contact resistance. This distance is called the transfer length, as it is the distance the current takes to transfer from semiconductor to metal, hence the name of the structures. Moving from the edge towards further under the contact, the current density and potential are reducing and the resulting potential distribution under the contact is described by the function [145]

$$V(x) = \frac{I\sqrt{R_s \rho_C}\cosh[(L-x)/\lambda]}{Z\sinh[L/\lambda]} \tag{3.7}$$

where R_s is the sheet resistance and ρ_C is the contact resistivity, L and Z are the length and width of the contact and λ is the transfer length.

Another useful test structure is the isolation structure. This consists of a single Ohmic contact, isolated by a mesa trench or implantation and can be used for characterising the vertical leakage though a stack and assessing the vertical breakdown. This is done by applying a bias to the Ohmic contact with the substrate at 0 V. Two such structures can also be used to evaluate the lateral leakage by measuring the current at a second isolation structure, biased at 0V like the substrate. It may not be obvious, however, if the lateral leakage is through the bulk or on the surface. A further test structure to make this distinction is the guard ring structure [146], shown in Figure 3.8. Here, a Schottky metal is deposited in a loop around the biased Ohmic contact and is also held at 0 V. All surface leakage will flow to the guard ring and be measured there.

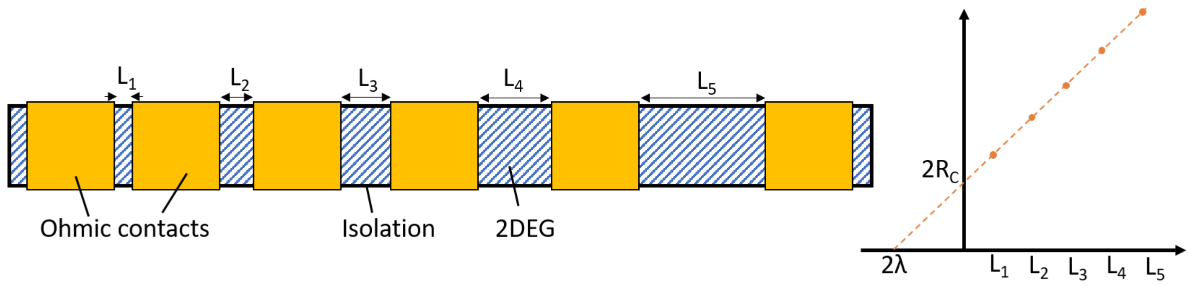

Figure 3.7: Top down view of a transfer length measurement structure. The structure consists of a series of Ohmic contacts with varying separation in the same active area. Outside of the mesa or implant isolation is more 2DEG but this is electrically isolated from the structure. Plotting the resistance of each gap vs. gap size allows determination of the contact resistance R_C, sheet resistivity and transfer length, λ.

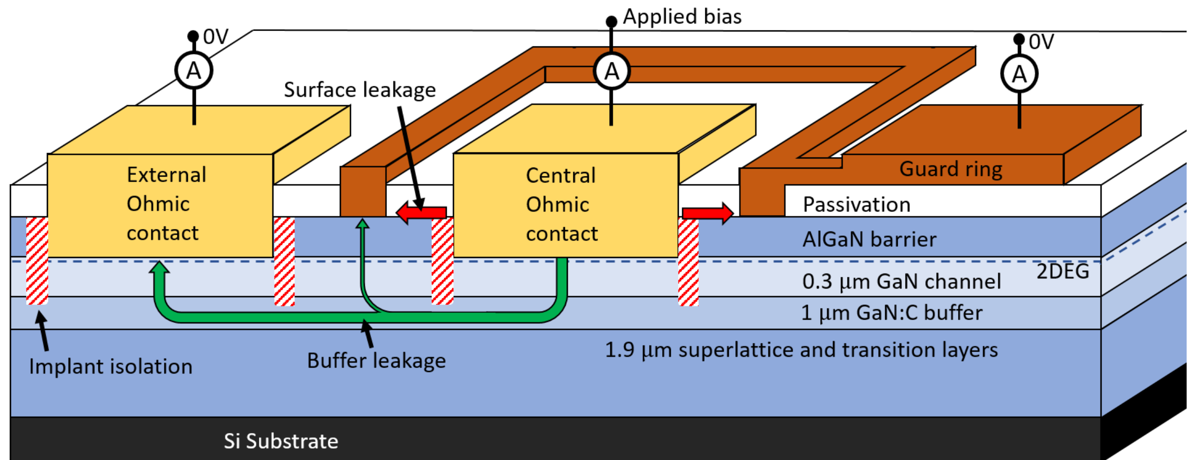

Figure 3.8: One half of a surface leakage structure. In the full structure, the Schottky guard ring completely surrounds the central Ohmic contact. The Ohmic contacts are surrounded by an implant isolation and the arrows indicate the flow of surface and buffer leakage currents.

Whereas the external Ohmic contact will measure only the current that has flowed through the buffer under the guard ring. A small fraction of the buffer current will flow to the guard ring but the Schottky junction limits this undesirable effect. This structure is used in Chapter 5 to study surface leakage and charging.

3.4 Materials analysis

3.4.1 Scanning transmission electron microscopy

Transmission electron microscopy permits the study of material structure and composition and allows the observation and characterisation of structure cross-sections. The principle uses a

focused electron beam which interacts with the sample as it is transmitted. The sample must be sufficiently thin for electron transmission and image clarity, therefore, in preparation, the sample must be thinned down to less than 100 nm. This can be achieved by focused ion beam (FIB), etching or mechanical polishing. As the electron beam passes through the thinned sample, some of the electrons are scattered by a large angle and are observable in the high angle annular dark field (HAADF), so named as scattering events to such a high angle have a low probability rendering the annulus dark. The larger the atomic weight, the more high angle scattering events occur, resulting in a brighter high angle annular dark field image. This is referred to as z-contrast since the image intensity is proportional to the proton number of the scattering centre. This technique can be adapted to scan over the surface of a sample (scanning transmission electron microscopy, STEM), and a profile of the atomic composition can be determined over an area. An image measured using this technique is used in Chapter 4 to determine the profile of the aluminium content in a nominally abrupt junction AlGaN/AlN/AlGaN heterostructure.

3.4.2 Secondary-ion mass spectroscopy

Secondary-ion mass spectroscopy (SIMS) is a destructive method of measuring the atomic composition of a sample. An ion beam is used to bombard the sample, causing the constituent atoms to be ejected as secondary ions. These secondary ions are then accelerated away from the sample surface and identified using typical mass spectrometry methods. Profiling of the composition as a function of depth is possible in this method since the ion beam ejects matter from deeper and deeper into the sample over time as it cuts through. The primary ion beam has a sputter rate of around 10 μm per hour giving depth profile resolutions of around 20 nm. The sensitivity of this technique varies depending on the element but is around 10^{15} cm^{-3} for the common dopants and impurities in GaN (C, Si, Mg, H, O). This method is applied in Chapter 4 for measuring the concentration of dopants in an AlGaN/GaN epitaxy.

3.5 Simulation

Correlation of experimental measurements with simulations enables the understanding of internal, unmeasurable or unintuitive processes. Electrical device simulations in this thesis have been carried out using ATLAS, a drift diffusion simulator produced by Silvaco. This framework is specifically designed for the electrical simulation of semiconducting devices.

A 2D device cross-section is simulated in which the carrier concentration, electric field, etc. are calculated based on circular boundary conditions in and out of the plane. The device cross-section is designed in a program called DevEdit which also handles the triangular meshing of the structure for the finite element calculations shown in Figure 3.9. A high density mesh is required in areas experiencing high electric fields or with sharp features such as heterointerfaces. If the mesh density is too low, it can lead to the simulation failing to converge and terminating without

output. If the simulation does converge, it is still possible that some device behaviour may be underestimated such as 2DEG density or peak electric fields. For example, in the mesh around the 2DEG, the vertical spacing of nodes should be approximately 1 nm since the 2DEG is only a few nanometers in thickness. The lateral spacing is less important provided there are no strong lateral electric fields. In general, a dense mesh is better but the higher the mesh density, the longer the simulation takes to run. DevEdit contains a library of standard material properties, thus in design, only the name of the desired material need be selected for the layer to be assigned an associated electron affinity, bandgap, mobility, etc. and these properties can be modified as required for specific device geometries. For example, in the channel region, the electron mobility must be increased from the bulk mobility to accurately simulate the 2DEG. The addition of dopants and trap levels can also be done at this stage as required. Traps are added by specifying the region, density and energy level as well as the capture cross section and degeneracy. The simulator is called by the program DeckBuild, in which the desired physical models are selected such as transport, scattering or generation/recombination statistics. The more models selected increases the computation time and not all models are always required. For example if currents are always low, the effect of joule heating need not be calculated. Polarisation charges at interfaces can be set here, either by instructing ATLAS to calculate them automatically or manually using the "interface charge" statement as demonstrated in Appendix C. Setting the polarisation charge in this way, using equations from the literature, ensures that strain/relaxation are accounted for. When simulating a HEMT epitaxy it is possible to set the charge of the simulated surface in order to tune the 2DEG density. This may be required for more accurate comparison of simulations with measured data and is also achieved using the "interface charge" statement.

It is also in Deckbuild that the details of the desired measurement are specified. In this input deck, the voltages of the contacts and ramp rates are set as well as the specification of the output parameters. The simulator is fundamentally based on solving the Poisson equation, carrier continuity and transport equations which together give the drift diffusion equations;

$$J_n = qn\mu_n E_n + qD_n \nabla n \tag{3.8}$$

$$J_p = qp\mu_p E_p + qD_p \nabla p \tag{3.9}$$

Here, J_n (J_p) is the electron (hole) current density, n (p) is the electron (hole) concentration, μ_n (μ_p) is the electron (hole) mobility, and D_n (D_p) is the diffusion coefficient for electrons (holes). E_n and E_p are the effective electric fields experienced by electrons and holes and may differ between the two carriers as they depend on the local gradients of the quasi-Fermi levels [147]. These equations along with any other models specified are solved at each node in the device mesh. The variation of an output parameter (e.g. electric field) along a 1D path through the device can be extracted by drawing a cut-line and the parameter along that path is plotted. This simulation tool is used in Chapter 4 to simulate buffer charge and substrate bias measurements.

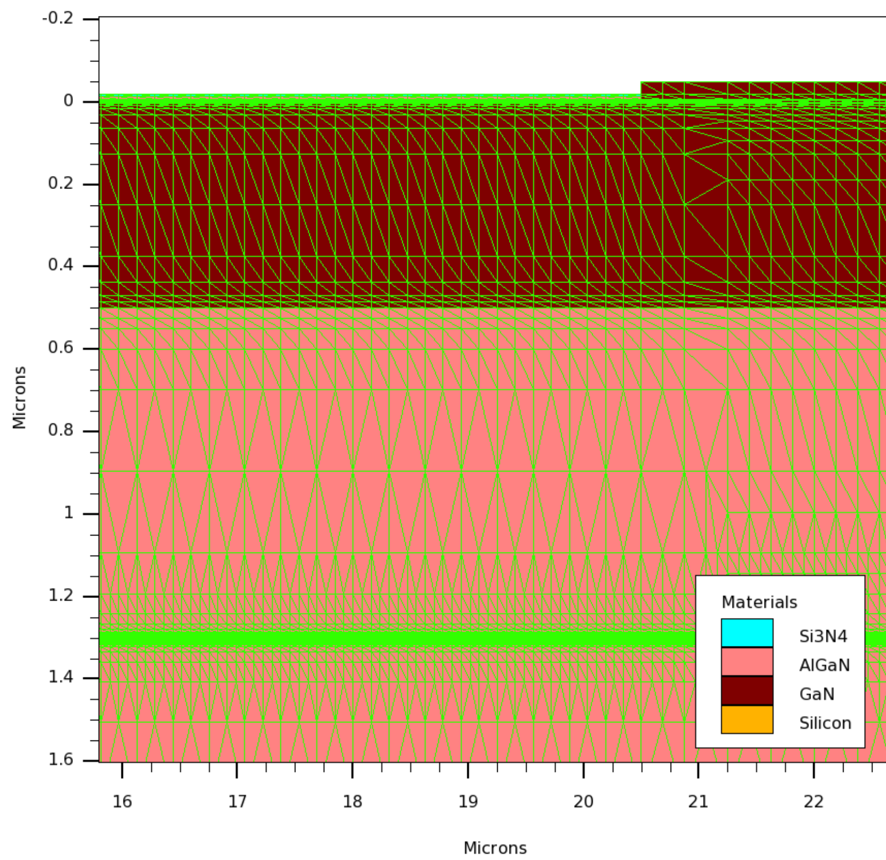

Figure 3.9: A section of a device simulation showcasing the finite element mesh where the equations are solved at each node. Note the high mesh density near the surface 2DEG and buried interlayer at 1.3 μm.

Chapter 4

The self-compensation ratio of carbon in AlGaN

As previously discussed, carbon is often incorporated into the buffer and strain relief layers of AlGaN/GaN HEMTs. This is to increase the buffer resistivity by the mechanism explained in section 2.4.3. The purpose is to increase the breakdown voltage and suppress buffer conduction [93, 148]. In turn, this facilitates higher voltage operation leading to more efficient switching. Equations 2.10 and 2.11 explicitly showed that the compensation ratio alone determines the free carrier density. Therefore, in the absence of parallel defect related conduction, the compensation ratio sets the resistivity and bulk leakage of carbon doped GaN. This chapter works towards determining this unknown ratio, of which a reasonable estimate is required for accurate device simulation.

The samples used in this study were grown by the Inter-University Micro-Electronics Centre (imec). Imec also performed the secondary-ion mass spectroscopy, scanning transmission electron microscopy and Hall measurements on these samples. The substrate bias ramps and lateral leakage measurements as a function of contact separation presented in section 4.3 have been published in IEEE Transactions on Electron Devices [149]. Significant content has been reproduced from this publication. The flow of the research in this chapter is presented in Figure 4.1.

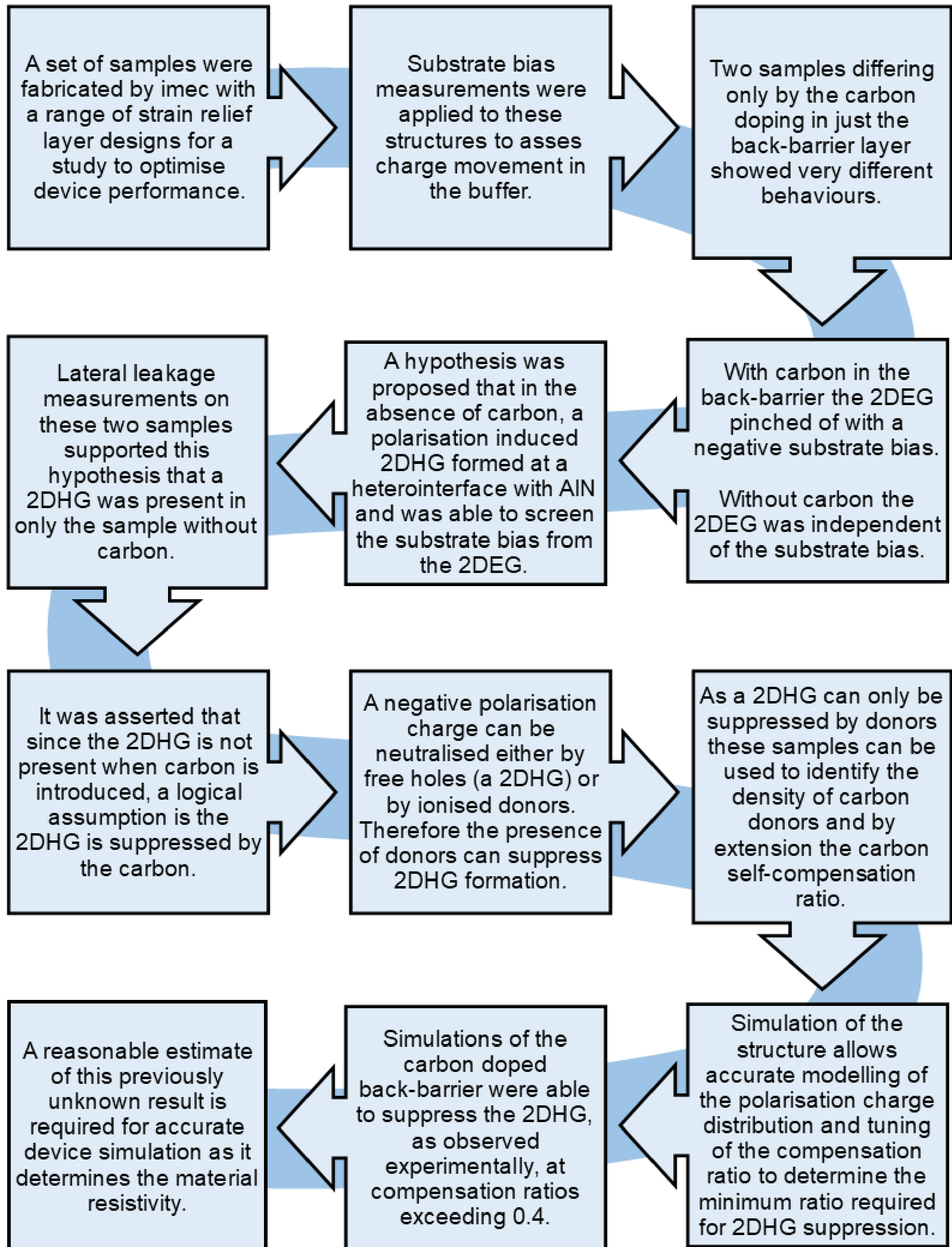

Figure 4.1: The flow of the research in this chapter.

4.1 Introduction

Despite the widespread use of carbon doped GaN, there is still some debate about the underlying physics of how it increases the material resistivity. Carbon can incorporate into GaN in multiple different ways; substitutionally on the nitrogen or gallium sites, interstitially, or in a variety of complexes with other point defects [92, 150, 151]. Early theoretical calculations struggled to identify the energy levels of these traps and predicted that carbon would exist primarily substitutionally on the nitrogen site (C_N) as an acceptor at $E_v + 0.3$ eV and on the gallium site (C_{Ga}) as a donor at $E_c - 0.2$ eV [152]. However, experimental attempts to observe these carbon levels through the use of various transient and optical spectroscopy techniques were unsuccessful. Instead, two different trap levels were experimentally correlated with carbon density; a deep acceptor around $E_v + 0.9$ eV and a shallow donor near the conduction band [94, 96, 153]. Today, after considerable debate, consensus has been reached on the depth of carbon levels in GaN. More recent theoretical work, improving on initial approximations [92], predicted that carbon on the nitrogen site is a deep acceptor with a level of $E_v + 0.9$ eV and carbon on the gallium site is a shallow donor in or near the conduction band. This acceptor level is much deeper than previous estimations and in agreement with the spectroscopic data. In addition, device simulations with this deeper C_N level agree well with experimental results [154].

There are no definitive results or methods for measuring the compensation ratio (N_D/N_A). The total carbon concentration can be profiled using secondary-ion mass spectroscopy, however, no information is gained with this technique about the compensation ratio. This is because the crystal structure is destroyed in the process and with it, the information about the site of origin of each atom. The resistivity of GaN:C inferred from electrical measurements of AlGaN/GaN HEMT epitaxies is in the order of 10^{13} Ωcm [42, 155]. This is in agreement with measurements of this property presented in Chapter 5. If all of the carbon were incorporated on the nitrogen site as deep acceptors the resistivity would be much lower - in the order of 10^6 Ωcm for a typical carbon density of 2×10^{18} cm^{-3} [42]. Therefore, donors must be present in high densities in order to compensate these acceptors and increase the resistivity to observed levels. From Figure 2.11, these indirect electrical measurements of resistivity indicate the compensation ratio must be between $0.1 - 0.6$. Dislocations through the GaN:C give rise to additional leakage, possibly via defect band conduction [156]. Therefore the ideal, bulk resistivity of GaN:C may be greater than what is measured. This means that the compensation ratio inferred from those measurements represents a lower limit. Regarding an upper limit, electrical measurements have directly observed Fermi level pinning near the carbon acceptor level demonstrating that C_N is dominant i.e. $N_D/N_A < 1$ [157]. This chapter presents electrical measurements and simulations which are able to refine this interval by identifying the donor charge required to neutralise known polarisation charges. Identifying a reasonable estimate of the compensation ratio improves understanding of the role of carbon in AlGaN which is pivotal in the management of buffer leakage and vertical breakdown.

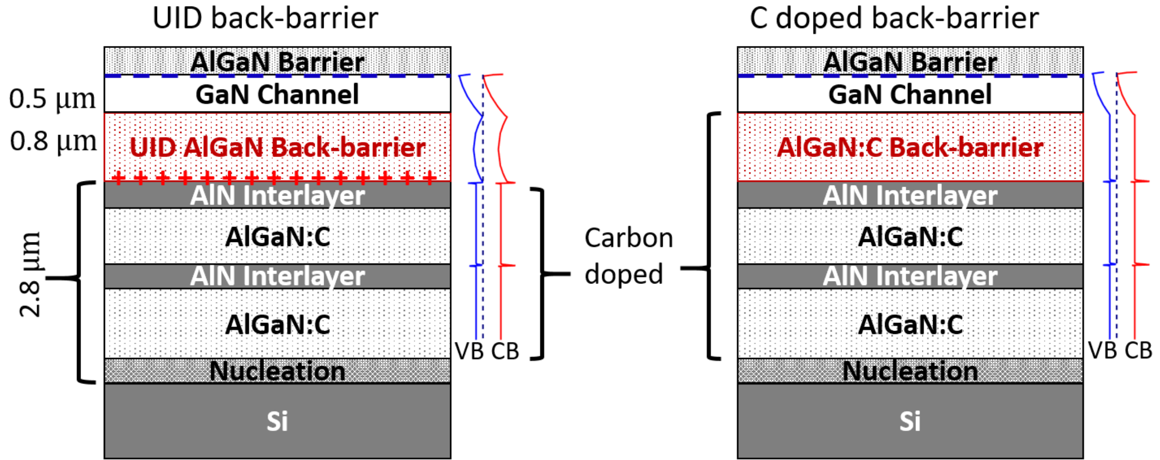

Figure 4.2: The samples used in this study differed only by the carbon doping level in the back-barrier; unintentional doping or 2×10^{19} cm^{-3}. In both samples a 2DEG formed in the unintentionally doped GaN channel below the AlGaN barrier, represented by the blue dashed line. In the sample with the unintentionally doped back-barrier the location of the 2DHG is shown above the top interlayer as a series of red crosses. A sketch of the band structure is presented to the right of both structures.

4.2 Experimental Details

4.2.1 Samples

The two samples in this study were grown by metal-organic chemical vapour deposition and are shown in Figure 4.2. The layer structures were typical of an AlGaN/GaN HEMT grown on silicon. The strain relief layers were implemented with 10 nm AlN interlayers in carbon doped $Al_{0.08}Ga_{0.92}N$, with a total thickness of 2.8 μm. These AlN interlayers were under tensile stress to introduce compressive stress into the buffer. This was followed by a 0.8 μm $Al_{0.08}Ga_{0.92}N$ back-barrier, a 0.5 μm unintentionally doped GaN channel and an AlGaN barrier to form a 2DEG. The two samples differed only by the doping level in the $Al_{0.08}Ga_{0.92}N$ back-barrier. The layer was either highly carbon doped with a concentration of 2×10^{19} cm^{-3}, as measured by secondary-ion mass spectroscopy, or unintentionally doped which is typically a level of $\sim 10^{16}$ cm^{-3} in metal-organic chemical vapour deposition GaN [158]. These samples will be referred to as the carbon doped and unintentionally doped samples respectively. Generally, back-barriers are made with GaN:C to provide a highly resistive layer and suppress buffer leakage below the channel, but trapping in the carbon related defects can lead to current collapse. AlGaN back-barriers were included in these epitaxies in an attempt to introduce a blocking hetero-interface and reduce trapping in the back-barrier [159]. This design is not commonly used however, presumably for reliability reasons pertaining to stress; the high electric fields in the top device layers and the inverse piezoelectric effect could cause delamination at heterointerfaces. Only Ohmic contacts

were processed on these samples which were made with an annealed Ti/Al/Ni/Au metal stack. Each cell of the mask-set contained transfer length measurement structures, isolation structures and a Hall bar structure. Isolation was implemented with a mesa trench with a depth of ~ 600 nm, ending in the back-barrier. The depth of this trench isolated the 2DEG but was not sufficiently deep to reach the back-barrier/AlN interlayer interface.

4.2.2 Measurement techniques

The samples were subjected to a substrate bias ramp as described in section 3.2.4. The channel conductivity was measured by applying 1 V across two contacts of a transfer length measurement structure with a Keithley 4200. The substrate bias was ramped at 5 Vs^{-1} in both directions, from 0 V down to -350 V and back to 0 V with a Keithley 2657A. Measurements above $|-350|$ V were not performed due to the high substrate current densities in the unintentionally doped sample.

Lateral leakage measurements were performed on the isolation structures which were 100 μm × 100 μm in area. This entailed applying a bias to one isolation structure which was ramped to -150 V. The current on a second isolation structure which was biased at 0 V was measured. This was done using the Keithley 4156A with a 41501B expander which also biased the substrate at 0 V during the measurement. No electric field between this second structure and the substrate ensured all current measured on the second structure must have flowed laterally. This measurement was performed with various separations between the isolation structures to identify the trend of the leakage current with separation. Additional lateral leakage measurements were performed with a constant separation between the two isolation structures but increasing the area of the structure at 0 V. Since all of the isolation structures were 100 μm × 100 μm the effective contact area was increased by probing multiple isolation structures and shorting them together as shown schematically in Figure 4.3. The additionally probed structures were further away from the biased structure leaving the separation and the surface electric field unchanged as the effective area was increased.

Finally, vertical leakage and charging properties were investigated in the low field range with up to 40 V over the epitaxy. This was a two terminal measurement applying a positive ramped bias to the substrate and measuring the current flowing through an Ohmic contact on the surface which was held at 0 V using a Keithley 4156A. In order to accurately measure any charging effects, a continuous ramp was required. If a stepped ramp was used, charging currents would decay during the current integration time. Therefore, a linear ramp generator was used to apply the substrate bias like that used for the quasi-static capacitance-voltage measurements described in section 3.2.3. The measurements were performed at various ramp rates between 0.1 and 1 Vs^{-1}.

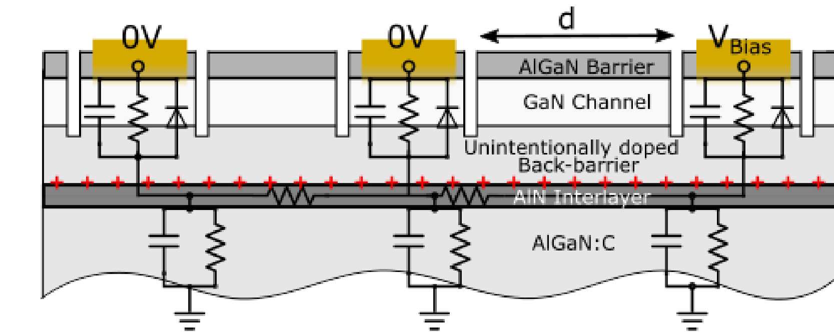

Figure 4.3: A schematic of three isolation structures demonstrating the way the effective area of the 0 V contact was increased. Overlaid is the equivalent circuit diagram of the structures. The diode-like behaviour over the channel layer is from to the band bending near the barrier which confines the electrons to the 2DEG.

4.3 Results

The substrate bias ramp measurement data are shown in Figure 4.4(a). The measurements were performed on a transfer length measurement structure with a channel length of 20 μm. These results are displayed with the capacitive coupling line which was calculated from the epitaxial thickness and mean permittivity as explained in section 3.2.4.The 2DEG density in the carbon doped sample showed an approximately linear dependence on substrate bias, similar to the ideal capacitive line. After the return sweep, the conductivity returned to slightly less than the initial value indicating an insignificant negative charge storage. This behaviour is consistent with other carbon doped epitaxies [42]. In stark contrast, the behaviour of the unintentionally doped sample was far from the ideal dielectric case. The 2DEG showed very little substrate bias dependence and on the return sweep appeared to saturate at the initial conductivity, as is typical for positive charge storage (see Section 3.2.4). This indicated there was no negative charge stored in the buffer after the measurement which is consistent with what has been observed in another study [160]. The substrate currents measured during the substrate bias ramp are shown in Figure 4.4(b). The vertical current is ~100 times higher in the unintentionally doped sample than in the carbon doped sample at −350 V. The substrate bias measurements were repeated on the sample with the carbon doped back-barrier with various transfer length measurement structure contact separations. The results, shown in Figure 4.5 present a variation in pinch-off behaviour with transfer length measurement structure gap. The smaller the transfer length measurement structure gap, the smaller the changes in channel conductivity, indicating a weaker dependence of the 2DEG density on the substrate bias.

The results of the lateral leakage measurements as a function of isolation structure separation are presented in Figure 4.6. The structures were between 3 μm and 18 μm apart. The lateral leakage current in the carbon doped sample decreased rapidly with increasing isolation structure separation. This structure separation, d, is shown in Figure 4.3 where the left most contact is

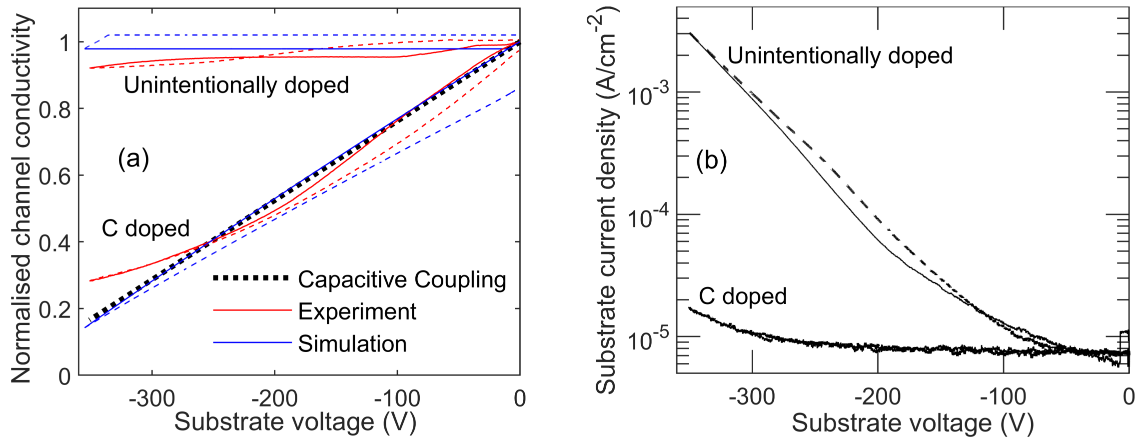

Figure 4.4: (a) The measured and simulated 2DEG conductivity during the substrate bias ramps on the unintentionally doped and C doped samples. The voltage was ramped at 5 Vs^{-1}. The solid line shows the sweep down to -350 V with the dash line the return to 0 V. The capacitive coupling line is the response of an ideal dielectric. (b) The substrate current density during the measurements. The unintentionally doped sample shows an ~ 100 times increase in vertical leakage at -350 V.

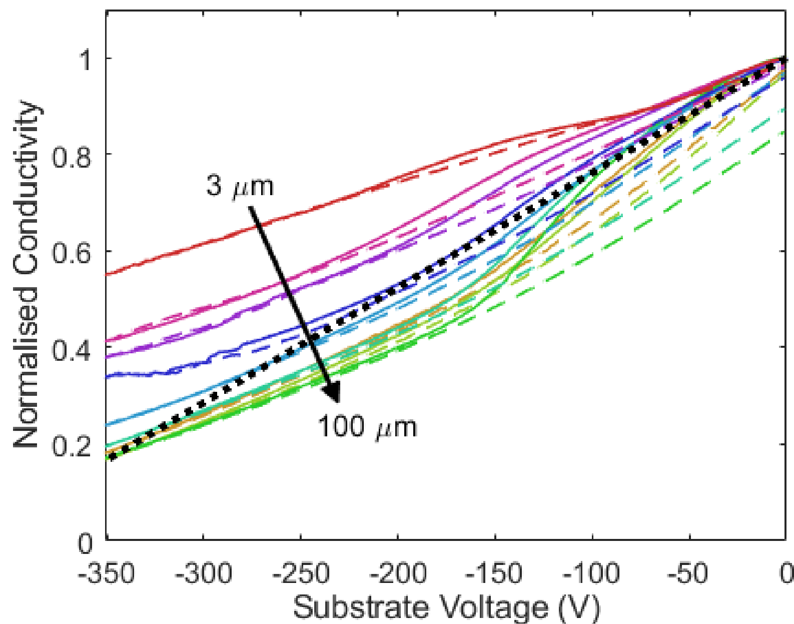

Figure 4.5: The normalised 2DEG conductivity during a substrate bias measurement for transfer length measurement structures of varying separation. The shorter the transfer length measurement structure gap, the slower the pinch off of the 2DEG. The dashed line represents the ideal capacitive line of the structure. The substrate bias was ramped at -5 Vs^{-1}.

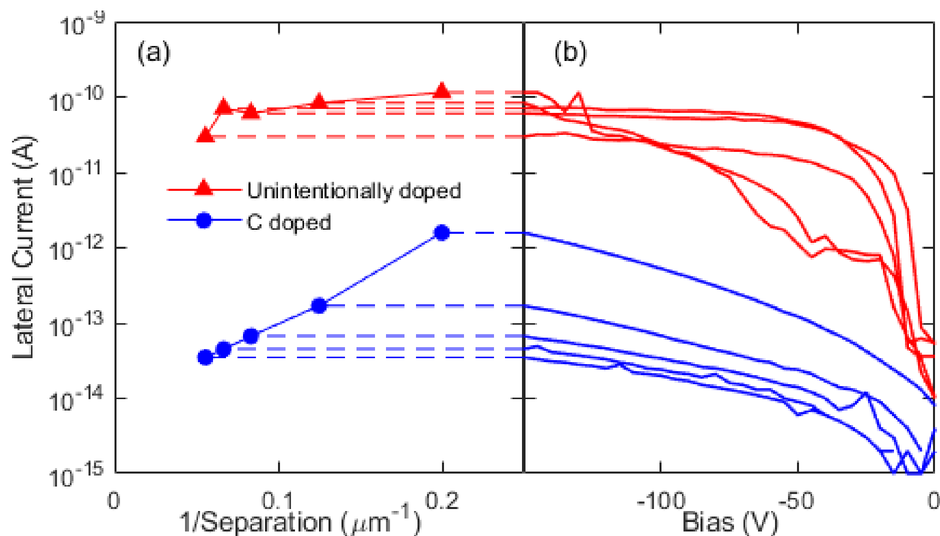

Figure 4.6: Lateral current between two isolation structures (a) as a function of inverse separation at 150 V and (b) as a function of voltage. (a) is plotted as inverse separation to show that on the C doped sample, the lateral current follows an exponential dependence on inverse separation whereas the lateral current on the unintentionally doped sample is $\gtrsim$ 100 times higher and only weakly dependent on separation.

not used in this particular measurement. The exponential reduction in current with inverse distance ($I \propto e^{C \times V/d} \propto e^{C \times E}$ where C is a constant) seen in Figure 4.6(a) is indicative of a leakage process which is exponentially dependent on the electric field such as variable range hopping [101]. Again, the unintentionally doped sample showed a different behaviour than the carbon doped sample with only a weak dependence on separation and a lateral current $\gtrsim$ 100 times higher. When increasing the metal-semiconductor area of the isolation structure biased at 0 V by probing multiple structures, additional probes were connected in parallel to the same source measurement unit. This increased wiring connected to the measurement system increased the noise floor into the pA level. This meant that the lateral leakage current level of the carbon doped sample in Figure 4.7 was below the noise floor. However, the lateral current in the unintentionally doped sample shows an approximately linear increase with increasing 0 V contact area.

The vertical leakage measurements on the sample with the carbon doped back-barrier showed no measurable leakage current up to 40 V. This is consistent with the vertical current during the substrate bias ramp in Figure 4.4(b) which was below the noise floor of 10 μAcm^{-2} until $|V_{\text{sub}}| >$ 250 V. However, the results of the measurement applied to the sample with the unintentionally doped back-barrier showed a surprising dependence on applied voltage and is shown in Figure 4.8. For ease of reference to these results, different stages in the current behaviour in this figure are numbered and referred to in the text. Initially, ①, the current increased with the voltage as expected from the substrate bias ramp. At ②, the voltage was constant for a few seconds as the system prepared to change the ramp direction. During this time when the voltage was

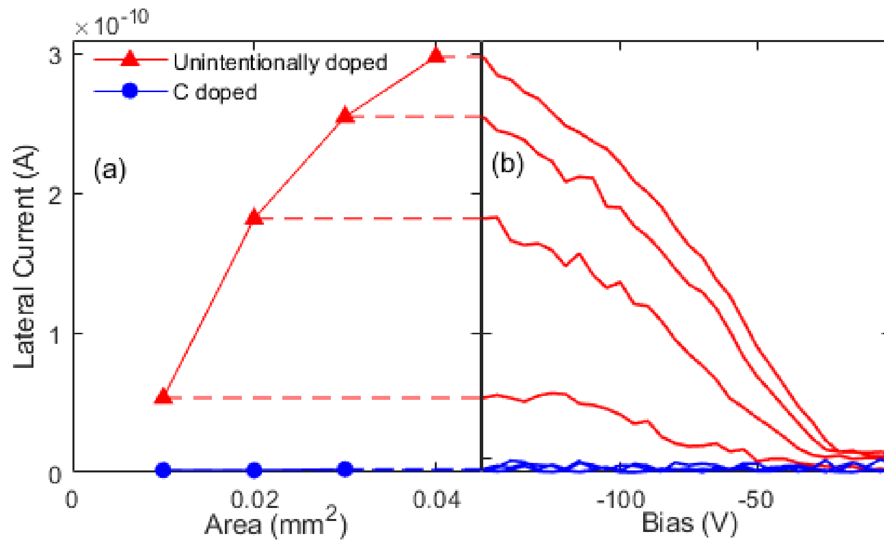

Figure 4.7: Lateral current between two isolation structures at a separation of 8 μm (a) as a function of contact area of the 0 V contact and (b) as a function of voltage. On the unintentionally doped sample, the lateral current shows a near linear dependence on area. The noise floor was in the order of pA as a result of adding additional probes to the system which was above the lateral leakage current level of the carbon doped sample.

fixed at 38 V, the vertical current increased. Then, as the voltage began to ramp down again, the current continued to increase, (3). At a point on the return ramp, (4), and at a time dependent on the ramp rate, the current turned over. Finally, (5), the current quickly reduced with a steep gradient. Increasing the ramp rate reduced the magnitude of the current and delayed the time in the return ramp that the current began to decrease. This result of increasing vertical current with decreasing field during the return ramp is obviously far from conventional field dependent leakage current behaviour.

4.4 Discussion

4.4.1 Substrate bias ramps

First discussing the substrate bias ramps in Figure 4.4, since this technique is sensitive to the electric field under the 2DEG, the weak dependence of the 2DEG conductivity on substrate bias seen in the unintentionally doped sample, means the field below the 2DEG is very low. Electrostatically, this screening of the substrate bias can only be caused by the accumulation of positive charge in the buffer. As the substrate bias increases, the positive charge must also increase to continue screening the 2DEG from the substrate bias as observed. On the return sweep, the 2DEG density saturated at a fixed level. This occurs since, as the bias is removed, the positive charge in the buffer is quickly neutralised as it lowers the barrier confining electrons to the 2DEG (the diode in the equivalent circuit diagram in Figure 4.3 is forward biased). This is in

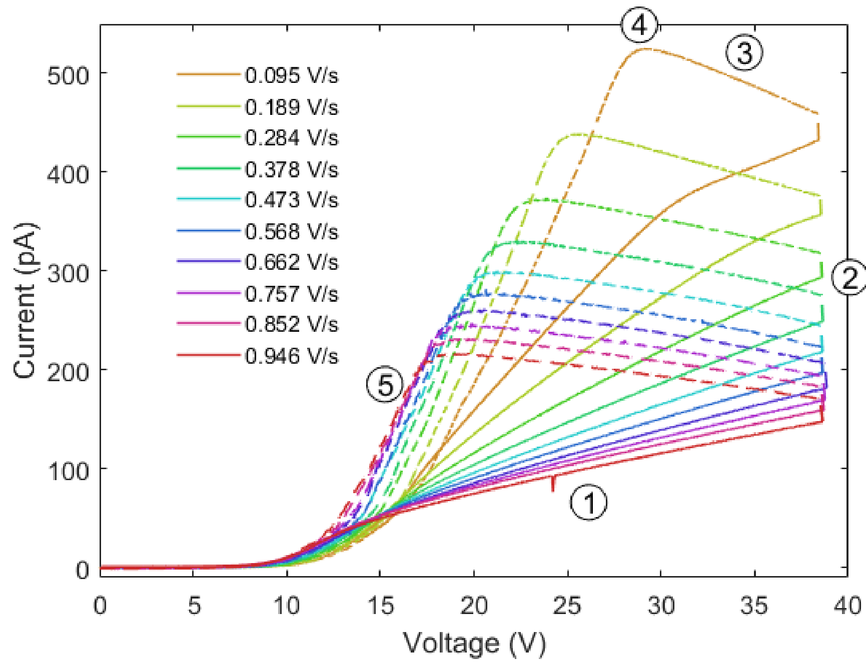

Figure 4.8: The vertical current measured during a linear ramp of the substrate potential at various ramp rates. An unusual hysteresis was observed in which the vertical current apparently continues to increase as the vertical field is reduced.

contrast to stored negative charge which has much longer time constants for neutralisation [120]. Since this behaviour is only observed in the unintentionally doped sample it is reasonable to infer that this behaviour is related in some way to the doping of the back-barrier. Therefore, two possible explanations are proposed; either a polarisation induced 2D hole gas (2DHG) is present at the unintentionally doped back-barrier/AlN interlayer interface [161–165], or, a population of donors is present in the unintentionally doped back-barrier with a sufficient density to screen the largest substrate bias [166].

Considering screening by ionised donors, the density required to be present can be calculated using Poisson's equation. Assuming that the donors are only present in the back-barrier and that they are uniformly distributed in the region, the charge distribution forms the top hat function as shown in Figure 4.9(a) with a height related to the charge density, ρ, from the ionised donors. Using Poisson's equation,

$$\nabla^2 \varphi = -\frac{\rho}{\epsilon} \tag{4.1}$$

the maximum potential which can be screened for a given back-barrier donor density can be calculated by double integration with respect to space. The form of the electric field and potential are shown in Figure 4.9(b) and 4.9(c) respectively. Screening was experimentally observed up to a substrate voltage of −600 V which from Figure 4.9 indicates a minimum donor density of 1.3×10^{17} cm^{-3}. Such a high density is unlikely in a good quality unintentionally doped layer

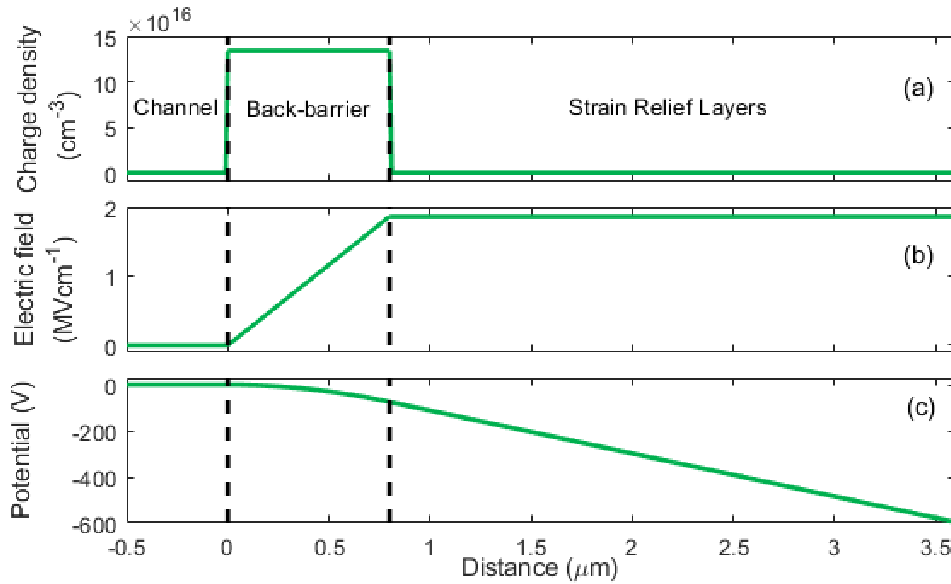

Figure 4.9: A calculation of the charge density required to screen a substrate bias of −600 V when distributed uniformly in the back-barrier. The charge density, (a), electric field, (b), and potential, (c), are each shown as a function of depth through the epitaxy.

as used here, therefore donors are unlikely to be the cause of the screening here. Instead, if the hetero-interface at the top of the interlayer is blocking, positive charge could accumulate there, either as free carriers or as ionised dopants. These two cases can be distinguished by considering the lateral resistivity as free carriers will provide a low resistance lateral conduction path.

During the substrate bias measurements, the substrate current in the unintentionally doped sample was observed to be 100 times higher than the carbon doped sample (Figure 4.4(b)). In the unintentionally doped sample, the thickness of the stack doped with carbon was reduced by a factor of ~0.7 compared to the carbon doped sample. Therefore, it may be logical to try to attribute this 100 times increase in leakage to the reduced thickness of highly resistive carbon doped GaN. However, even in the most extreme scenario of the entire 2DEG-substrate potential being dropped over only the carbon doped layers, a 0.7 times change in thickness would result in an increase in the electric field in the unintentionally doped sample by a factor of 1.4. Although the leakage current is likely to be exponentially dependent on the electric field, this is still a very small change in field compared to the measured 100 times difference in the vertical current. Therefore, this disparity cannot simply be attributed to the reduced thickness of highly resistive carbon doped layers. On the other hand, the presence of a 2DHG can account for this increased vertical leakage by considering that it spreads out over an area greater than the mesa area [167]. This results in a higher vertical leakage current since the same potential is dropped over additional parallel leakage paths because the active area is effectively increased.

4.4.2 Lateral leakage

The lateral leakage measurements further verify the presence of a 2DHG at the unintentionally doped back-barrier/AlN interlayer interface. With reference to the equivalent circuit diagram in Figure 4.3, the weak dependence on separation in the unintentionally doped sample in Figure 4.6 indicates the lateral resistivity is much lower than vertical resistivity. Assuming Ohmic transport through all the resistors, the current-distance gradient implies the total lateral resistivity is ~ 10 times lower than the vertical resistivity. In reality the vertical conductivity is far from Ohmic and so the lateral resistivity will be much less. This is consistent with the model of a low resistance 2DHG acting as a deep lateral conduction path below the mesa isolation trench. The lateral current increasing with the area of the unbiased contact in Figure 4.7 is particularly interesting. Proceeding with the assertion that the lateral resistance is small compared to the vertical resistance, the equivalent circuit diagram in Figure 4.3 reduces to two back-to-back leaky diodes. With -150 V on the biased isolation structure, the diode below that contact is forward biased resulting in a negatively biased 2DHG. The 2DHG will not be at a potential of -150 V since it will also be coupled to the 0 V substrate by some leakage process, but it will certainly be below 0 V over an extended area (since the 2DHG is not confined by the mesa isolation). The diodes below the isolation structures at 0 V will therefore be reverse biased and the current in Figure 4.7 represents the reverse bias leakage. It follows that any additional isolation structure biased at 0 V will experience the same bias conditions and so the measured leakage current scales linearly with the number of structures at 0 V. Therefore, the model to explain this data requires a p-type layer below the 2DEG, a blocking back-barrier and low resistance lateral conduction. The presence of a 2DHG satisfies these requirements and can explain the behaviour of the leakage current increasing with the total area of the isolation structures biased at 0 V.

As the density of the 2DHG must vary in order to change its potential, an obvious question is how far does this change in density extend and what limits it from extending over the entire sample? One model proposed by Chatterjee et al. [167] suggests the extension is limited by preferential leakage paths which pin the potential around them by sourcing electrons from the substrate. This is illustrated in Figure 4.10 as Model 1 with the vertical resistors in the strain relief layer representing dislocations. The preferential leakage paths are shown as orange resistors and the potential along the 2DHG is shown in orange. Since the potential at the dislocation is pinned and the potential in the active area is pinned, the 2DHG potential must drop linearly between these two potentials. In this model, the 2DHG extension area under a given isolated structure is fixed, based on the locations of these preferential leakage paths. An alternative model considers that the 2DHG is in AlGaN and so alloy scattering and dopants can give rise to a percolated potential. This would lower the hole mobility and increase the sheet resistance of the 2DHG so a lateral electric field and hole density gradient could be sustained. In this way, the 2DHG could be bound by many parallel vertical leakage paths with the magnitude of any lateral extension equivalent to a transfer length. This second model assumes the equivalent

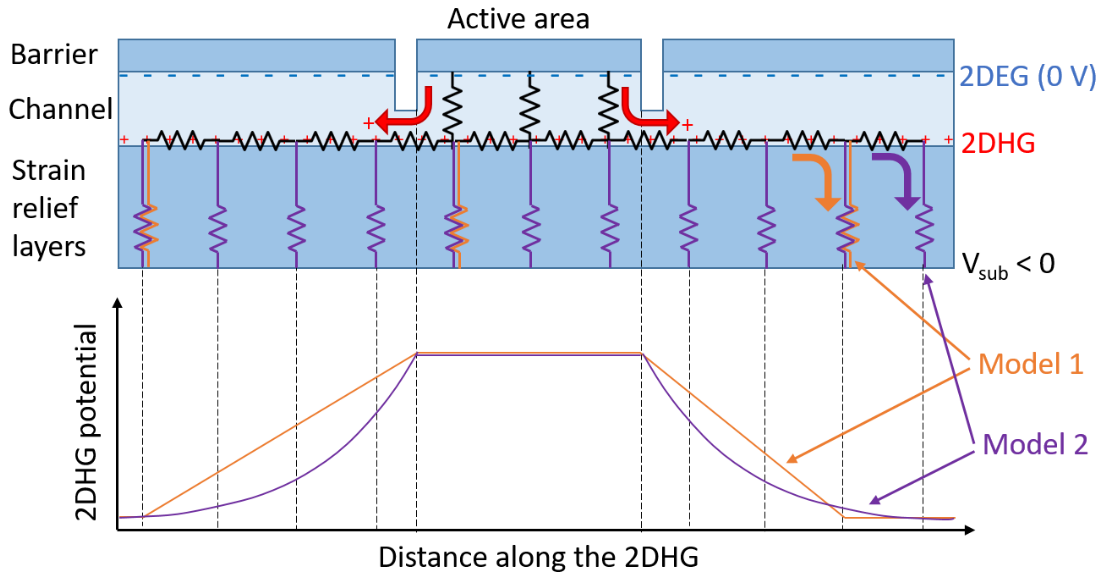

Figure 4.10: An epitaxy is presented with a 2DHG and a negative substrate bias. Overlaid is an equivalent circuit diagram where vertical resistors represent dislocations and the arrows represent hole flow. In the active area the 2DHG potential (and density) is increased relative to the rest of the wafer and the extension is limited by two possible models. In orange, the Chatterjee model whereby the potential is completely dropped at preferential leakage paths. In purple, the extension is limited by dropping the potential over many dislocations.

circuit diagram of the strain relief layer is instead composed of the many purple resistors in Figure 4.10. The resulting potential distribution, shown in purple, follows the same potential drop as in a 2DEG along the transfer length under a contact described in Section 3.3. Although here, the contact resistivity instead represents the dislocation resistivity and the transfer length is the extension outside of the mesa. Moving away from the isolated area, each time the hole gas encounters a dislocation, some of the potential is dropped until, eventually, the potential is the same as elsewhere in the wafer. The dislocations in this model would not need to be as leaky as those in the Chatterjee model since at the edge of the 2DHG, the potential is dropped over multiple dislocations rather than just one.

Electrical measurements of the 2DHG extension beyond the mesa area by Chatterjee et al. indicated an average extension length of 100 μm. Reinterpreting this as a 100 μm transfer length, λ, the sheet resistance of the hole gas can be estimated using the equivalent circuit diagram in Figure 4.11. It is assumed that the resistivity of the epitaxy below the 2DHG is $\rho_2 \sim 10^{13}$ Ωcm. To further simplify the model, it is assumed that the resistivity above the 2DHG, ρ_1, is much smaller such that it can be neglected. Under these assumptions, the sheet resistance, R_s, can be approximated as

$$R_s = \frac{\rho_2 L_2}{\lambda^2} \tag{4.2}$$

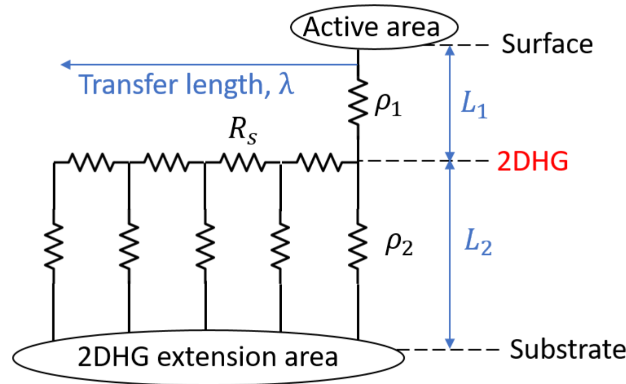

Figure 4.11: A circuit diagram to explain the transfer length interpretation of the 2DHG extension. The thickness and resistivity of the epitaxy above the 2DHG are represented by L_1 and ρ_1 respectively and likewise, L_2 and ρ_2 below the 2DHG. R_s is the sheet resistance.

where L_2 is the thickness of the strain relief layers in [167] (guessed as 2 μm). These model assumptions give rise to a sheet resistance in the order of 10^{13} $\Omega\square^{-1}$ which is exceptionally high for a free sheet charge and much higher than that interpreted from the lateral leakage in Figure 4.6. Further, assuming a sheet density of 10^{12} cm^{-2}, the apparent hole mobility from that sheet resistance is 10^{-6} cm^{2}V^{-1}s^{-1}, much lower than the bulk mobility of ~ 10 cm^{2}V^{-1}s^{-1} [168]. Discarding the assumption that ρ_1 is small, a numerical simulation of the equivalent circuit was performed. Here, it was instead assumed that $\rho_1 = \rho_2$ and the thicknesses L_1 and L_2 were guessed as 1.5 μm and 2 μm. No longer assuming a negligible series resistivity for ρ_1 reduced the required sheet resistance to 10^{12} $\Omega\square^{-1}$, though only by a factor of 10. The experimental data clearly shows a low resistance 2DHG, therefore based on these calculations it is clear that either the model or some other assumptions are incorrect. The most likely issue is in assuming that all the dislocations have the same resistivity and give rise to a 'bulk' resistivity of $\rho_2 \sim 10^{13}$ Ωcm. In reality, different dislocations with differing Burgers vectors (see Section 2.3.1) may vary in resistivity by orders of magnitude. This way the most leaky dislocations may limit the 2DHG after much smaller extensions. Unfortunately, it is not possible to test this as the density and conductance of such dislocations are not known.

4.4.3 Vertical leakage and charging

The measurements of the vertical current through the epitaxy with the unintentionally doped back-barrier, in Figure 4.8, showed some surprising results, most notably an apparent negative resistance when reducing the positive substrate voltage. This measurement was applying a positive substrate bias and hence the opposite polarity to the substrate bias ramps in Figure 4.4. The linear ramp used in these measurements would give rise to a displacement current based on the capacitance of the epitaxy. However, the displacement current expected from this structure

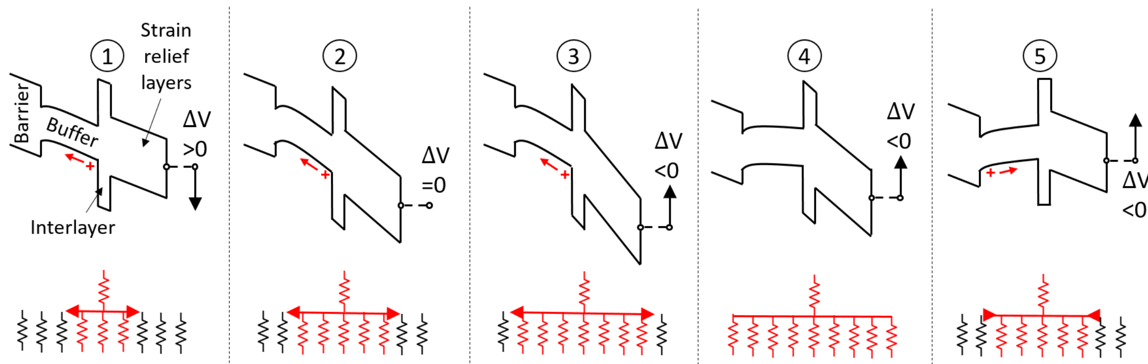

Figure 4.12: The vertical charging model is shown as a series of band and equivalent circuit diagrams. Holes flow from the 2DHG while its potential is less than zero, increasing the number of available vertical leakage paths. In the band diagrams, the arrow on the substrate indicated the direction of the substrate ramp. In the circuit diagrams the resistors in red indicate vertical leakage paths carrying current. The thick horizontal lines represent the region of the 2DHG at a reduced potential with the arrow heads indicating the direction of extension.

is a few pA, much smaller than the measured current. Since no leakage mechanism could give such a result, an alternative model has been constructed to explain this behaviour which again requires the presence of a 2DHG. Working around the current loop and with reference to the circled numbers in Figure 4.8, the model processes are described in each phase. For clarity, this description is also represented pictorially in Figure 4.12.

① As the substrate voltage increased, the vertical current increased. As the positive bias was applied to the substrate, the potential of the entire epitaxy became more positive as it was capacitively coupled between the substrate and the surface. A hole leakage current flowed from the interlayer 2DHG to the surface at 0 V. The potential of the 2DHG locally under the mesa was reduced compared to the rest of the 2DHG and this potential difference was dropped laterally along the 2DHG which is resistive. The resistivity of the strain relief layers below the 2DHG is constant and so the vertical current through this portion of the epitaxy is proportional to the area over which the potential is applied. As the substrate voltage was increased and the hole current continued, the area of the 2DHG at a reduced potential grew and so the vertical leakage through the epitaxy below the 2DHG increased with this area.

② The substrate voltage was constant but the vertical current continued to increase. The sustained vertical field meant the hole current continued and the area of the 2DHG at a lower potential outside the mesa area continued to expand. This caused the substrate leakage to continue to increase with the increasing size of the effective active area.

③ The substrate voltage began to ramp down but the vertical current continued to go up as if the epitaxy had a negative resistance. Reducing the substrate potential caused the 2DHG potential to capacitively reduce everywhere. However at this point, the 2DHG under the mesa

was still at a more positive potential than the surface so the leakage current between the two was reduced but continued. As such, the area of the 2DHG with a reduced density and at a reduced potential continued to expand. This expansion led to a continued increase in the current through the stack.

(4) During the return to 0 V, there was a turning point in the vertical current and it began to decrease. The substrate potential decreased to the point where the 2DHG potential was exactly 0 V and the hole current to the surface stopped as there was no longer any electric field through the top of the epitaxy. The 2DHG under the mesa stopped expanding and the current through the epitaxy stopped increasing.

(5) Finally, as the potential of the 2DHG continued to capacitively decrease, the 2DHG potential under the mesa became more negative than the surface and the leakage current restarted but in the opposite direction, with holes flowing from the surface to replenish the 2DHG density and keep its potential at 0 V. The area of the depleted 2DHG rapidly decreased in this phase causing a rapid decrease in the vertical leakage current.

The ramp rate dependence of the measurements can also be explained with this model. At the fastest ramp rate, the leakage in the top of the epitaxy occurred for less time so there was less time to change the 2DHG density. Therefore, the area of the reduced density 2DHG stayed small and the vertical leakage current stayed low. The time at which the turn over point, (4), occurred in the return ramp was also ramp rate dependent. If this measurement were performed so slowly that everything came into equilibrium, the high leakage between the surface and the 2DHG would keep the 2DHG at 0 V. Then on the return sweep, the 2DHG would instantly have a lower potential than the surface and the turn over would happen immediately. Conversely, considering an extremely fast measurement so that only a few holes flowed from the 2DHG to the surface during the positive substrate ramp. When ramping back down, the potential of the 2DHG would continue to be more positive than the surface right until the substrate was nearing 0 V and then the leakage current would reverse, and the few holes would return to the 2DHG. Therefore, the slower the ramp rate, the sooner the leakage current begins to decrease on the return ramp.

4.4.4 Sub-contact leakage

As established in section 4.4.1 the potential of the 2DHG must be able to change in order to screen the substrate bias in the substrate ramp measurement. This requires it to be in electrical contact with the Ohmic contacts. Electrical contact is also required to explain the lateral leakage and vertical charging measurements. Possible ways this can occur includes contact spiking, metal in-diffusion and the decoration of dislocations with the contact metals. Although it is not obvious which, if any of these, is the cause, the presence of these leakage paths is apparent from the substrate bias screening in the unintentionally doped sample. Since the only difference between the two samples is the doping in the back-barrier, the sub-contact leakage should be the same in both. Therefore, the sub-contact leakage can be further investigated by substrate ramp

measurements on the carbon doped sample, using transfer length measurement structures of varying channel length. These measurements are shown in Figure 4.5 on the sample with the carbon doped back-barrier. The 2DEG is depleted at a rate that depends on the distance between the contacts with the largest distance depleted fastest. This behaviour can only be explained by the field driven injection of positive charge into the buffer, just under the contacts. In this case with a carbon doped back-barrier, the positive charge is much less able to transport laterally as there is no 2DHG providing a low lateral resistance. Therefore, only the 2DEG near the contacts is affected. The size of the area around the contact that the holes extend into is determined by the time constant of the GaN:C ($\rho\epsilon \sim 10$ s) and the ramp rate of the measurement. As the contacts are moved closer together, a greater fraction of the total 2DEG is affected by the lower vertical field caused by the positive charge and so the rate of depletion is separation dependent. This phenomenon of increased vertical leakage under the Ohmic contacts will be investigated in depth in Chapter 5.

4.4.5 Self-compensation

By now there is a strong argument for the presence of a polarisation induced 2DHG in the unintentionally doped back-barrier. Equally compelling is the evidence that this 2DHG is not present when the back-barrier is carbon doped. Therefore it is a reasonable assertion that the presence of carbon is the cause of the 2DHG suppression. Only donors can suppress the 2DHG [169, 170] and this is explained considering the band diagram around the top interlayer as shown in Figure 4.13. The polarisation discontinuities at the top and bottom interfaces of the AlN interlayer result in the presence of interface charges; negative at the top interface and positive at the bottom. The negative interface charge at the top interface is neutralised either by free holes forming a 2DHG or by ionised donors. When the back-barrier is carbon doped, deep acceptor and shallow donor levels are present. At room temperature all of the shallow donors are ionised. Far from the interface, the net charge will be neutral despite the ionised donors, since an equal number of deep acceptors become ionised, pinning the Fermi level. However, in the depletion region above the interlayer, all of the deep acceptors will be neutral as the bands are pulled up by the interface charge. In this region the positive donor charge is revealed and if the donor density is sufficiently high, can completely neutralise the interface charge, suppressing any hole gas. The AlGaN layer below the interlayer is carbon doped in both samples. As the bands bend down at this interface, the ionisation of additional deep acceptors will neutralise any positive interface charge at the lower interface. As a result, no 2DEG will be present in either sample at the interlayers.

From this model of 2DHG suppression, it is required that donors are introduced by carbon doping, meaning that carbon is self-compensating. These measurements can be used with simulations to put limits on the minimum donor density (and therefore the minimum compensation

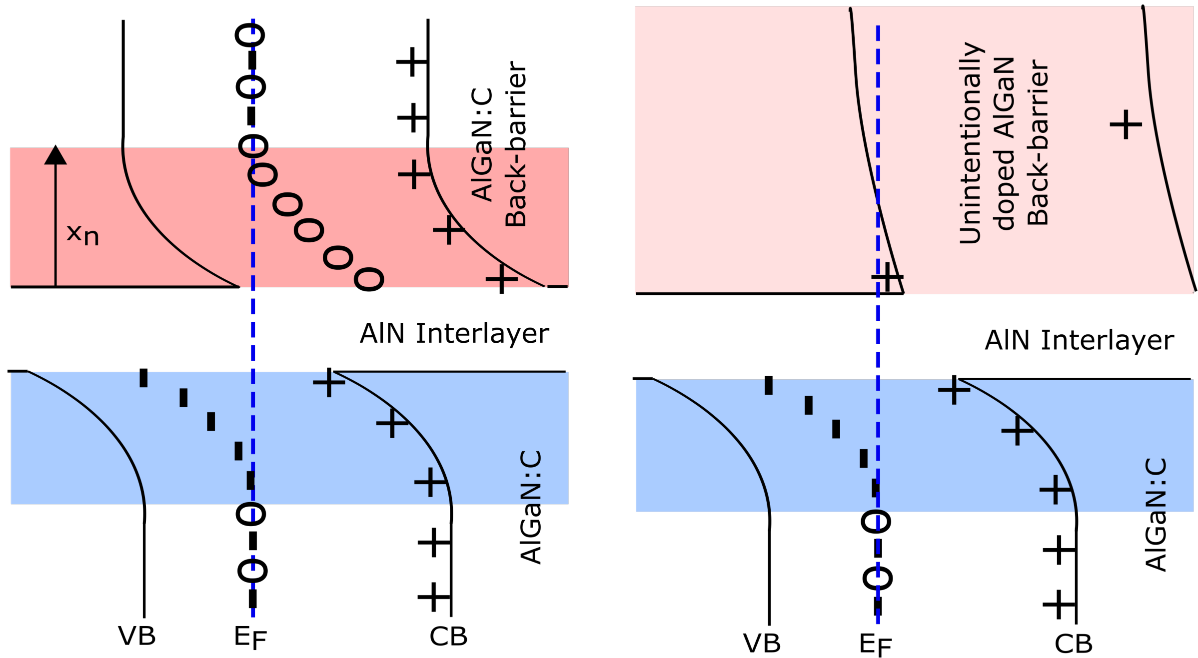

Figure 4.13: Diagram of the band structure around the AlN interlayer (a) with the carbon doped back-barrier and (b) with the unintentionally doped back-barrier. With carbon doping, the depletion region above the interlayer (in red and of width X_n) causes an ionised donor charge to be revealed which can neutralise the upper interface charge. Without carbon, the interface charge is not neutralised by donors and free holes can accumulate. In both cases, a net negative charge from additional ionised acceptors in the depletion region below the interlayer, neutralises the lower interface charges.

ratio) required to neutralise the polarisation charge. This is approached in the following section using technology computer aided design (TCAD) simulations. The purpose of these simulations is to quantify the carbon donor density required to reproduce the experimentally observed 2DHG suppression. The simulations will accurately model the magnitude and distribution of the polarisation charge around the interface and vary the carbon donor density (i.e. the self-compensation ratio). This will allow simulation of the 2DHG density and the minimum donor density required for 2DHG suppression can be identified. This result can then be converted into the lower bound of the carbon self-compensation ratio in these samples.

4.5 Simulations

Simulations of the epitaxy in Figure 4.2 are discussed both with and without carbon doping in the back-barrier. By varying the carbon self-compensation ratio it is possible to identify the minimum donor density required to suppress the formation of a 2DHG. The polarisation charges are calculated as a function of the aluminium composition following from the work of Ambacher et al. [48]. The exact composition profile was measured using a scanning transmission electron

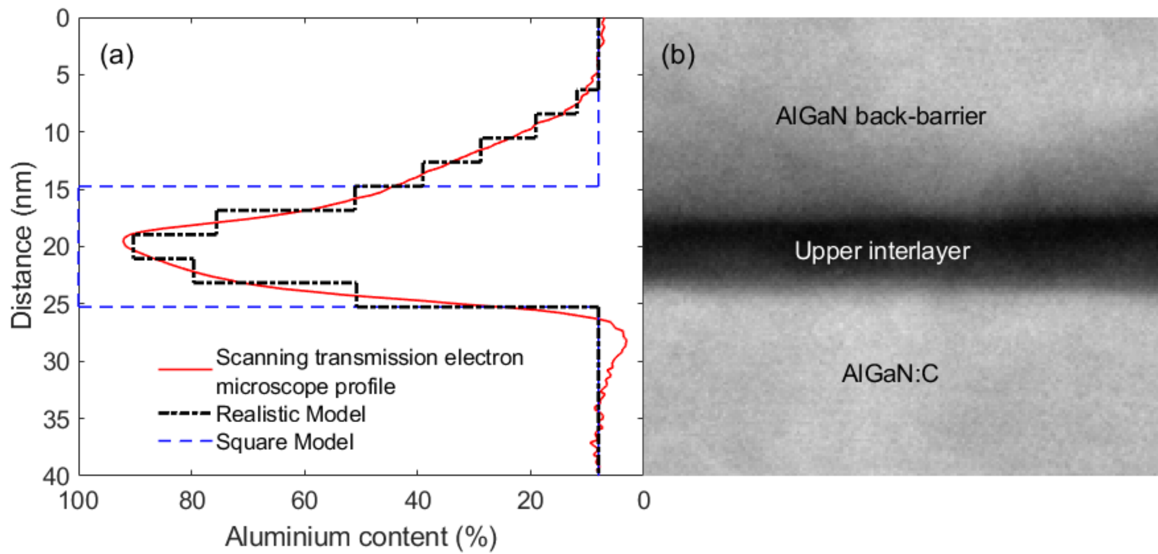

Figure 4.14: An scanning transmission electron microscopy z-contrast image of an AlN interlayer in AlGaN is shown in (b), acquired with a high-angle annular dark-field detector (courtesy of S. Stoffels, imec). The mean Al composition through the interlayer is shown in (a) along with the model used in the simulations. A square profile is also shown demonstrating the deviation from the ideal composition profile.

microscope image in the high angle annular dark field, shown in Figure 4.14(b). This technique, detailed in Section 3.4.1, looks at high angle scattering events of the electron beam. The heavier the atoms in the sample, the more high angle scattering occurs and the brighter the image. Therefore the Al composition was inferred by assuming the darkest point was AlN and the average grey far from the interlayer was $Al_{0.08}Ga_{0.92}N$. The image was averaged along the length of the interlayer to generate Figure 4.14(a). A model of the Al profile of the interlayer, used in the simulation, was approximated from the measured profile and is shown overlaid. This is compared to a square profile of an ideal 10 nm AlN interlayer in 8% AlGaN.

Since the structure was grown by metal-organic chemical vapour deposition, when rapidly changing Al composition, residual carrier gases in the reactor lead to a transition in Al content over a few nanometres of growth. As the junction is not abrupt, the polarisation charge is distributed over the transition. In calculating the polarisation charges it was assumed that the AlN layer was completely relaxed. This is a fair assumption since the nominal interlayer thickness was 10 nm which exceeds the critical thickness for relaxation of AlN on GaN [171]. However, if the interlayer were partially strained this would have introduced a piezoelectric polarisation to add to the spontaneous polarisation, resulting in an underestimate of the calculated interface charges.

The simulations were implemented using Silvaco's ATLAS drift diffusion simulator described in section 3.5. Donor and acceptor levels were included in the simulation to represent carbon

based on the energy levels determined by Lyons et al. [92] and discussed in section 2.4.3. To simulate a given self-compensation ratio, ξ, the total carbon density was divided into a donor density and an acceptor density by consideration of two constraints; the compensation ratio is defined as $\xi = N_D/N_A$, and the total carbon density must remain as $N_{\text{carbon}} = N_D + N_A$. Combining and rearranging these two constraints derives the formulae for the two trap densities as

$$N_A = \frac{N_{\text{carbon}}}{1+\xi} \tag{4.3}$$

$$N_D = \frac{\xi N_{\text{carbon}}}{1+\xi} \tag{4.4}$$

As required, the sum of these donor and acceptor densities recovers the total carbon density ($N_D + N_A = N_{\text{carbon}}$). The shallow donor level representing C_{Ga} was included at 0.02 eV below the conduction band of the $Al_{0.08}Ga_{0.92}N$ with a density of N_D. In addition, the deep acceptor representing C_N was included with a density of N_A and at a depth of 0.98 eV above the valence band. The depth of the donor in the simulation is not too important, so long as it is sufficiently shallow that it is thermally ionised at room temperature. The depth of the C_N deep acceptor level is 0.9 eV in GaN and 1.88 eV in AlN, the level used here of 0.98 eV in 8% AlGaN was determined through a linear interpolation between these levels. The total carbon density on both sites ($N_D + N_A$) was kept constant at the secondary-ion mass spectroscopy measured density of 2×10^{19} cm^{-3}. In addition to these trap levels in the carbon doped layers, unintentional donors were incorporated throughout the structure with a density of 10^{16} cm^{-3} at a level of 0.02 eV below the conduction band. The surface charge above the AlGaN barrier was set to 5×10^{12} cm^{-2} to bring the simulated 2DEG density in line with the Hall measured density of 5.9×10^{12} cm^{-2}. The simulated surface charge was lower than the simulated 2DEG density as some 2DEG electrons were provided by bulk donor states. To include the sub-contact leakage paths, described in section 4.4.4, some creative simulation was required. In a real device this leakage presumably occurs through a band-to-band trap-assisted-tunnelling process, however, this is currently beyond the capabilities of the simulator. Instead, small 15 nm p^{++} spike regions were added below the contacts which allowed a space charge limited hole current to flow locally in the unintentionally doped GaN when the structure was in reverse bias conditions. This was similar to the way preferential sub-contact leakage was implemented by Uren et al. [41]. Although there, the p-type spikes were much longer which would have contacted the 2DHG in these simulations. Generally in device simulations, only the top few layers of the epitaxy are simulated along with the processed device. This is done to reduce the simulation complexity and also because often the exact composition of the lower layers is not disclosed to protect intellectual property. The simulations performed here included the entire stack, including the deep buffer structure, which was absolutely necessary to understand the role played by the interlayers. The full simulation files required for this simulation of the structure with a carbon doped back-barrier are included in Appendix C.

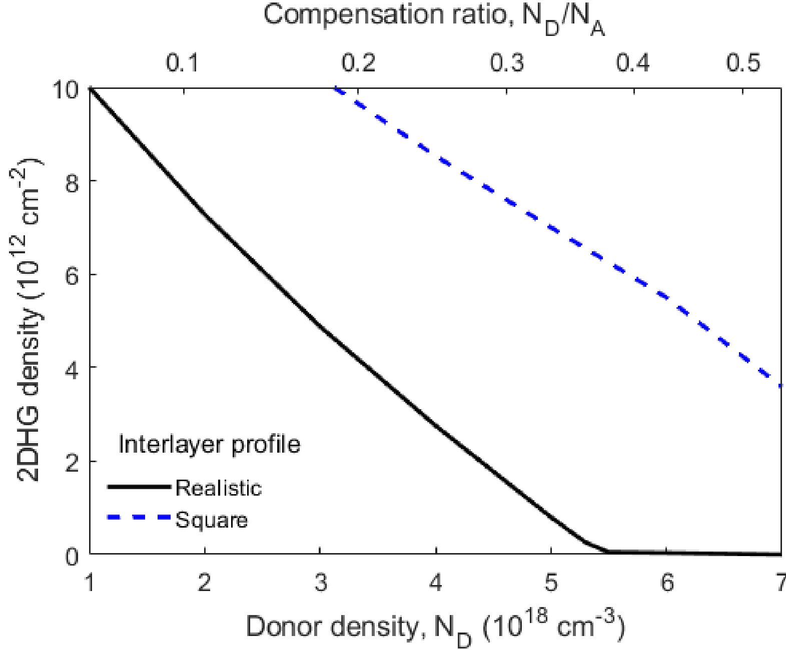

Figure 4.15: Simulated 2DHG density as a function of donor density (and compensation ratio) in the back-barrier. The simulations were repeated with realistic and square interlayer composition profiles. The 2DHG is completely suppressed at donor densities greater than 5.5×10^{18} cm^{-3} with a realistic profile corresponding to compensation ratios $\gtrsim 0.4$. Whereas with a square interlayer profile the 2DHG is not suppressed even at a donor density of 7×10^{18} cm^{-3}. This figure corrects that published in [149] where the tick mark positions on the compensation ratio axis were incorrectly linearly spaced between the extremal ratios.

4.5.1 Equilibrium conditions

For clarification, all of the parameters in this simulation have been set based on measured material properties, measured composition profiles and defect energy levels presented in the literature. The total number of carbon defects has been measured experimentally but the fraction that are donors and the fraction that are acceptors is varied in this set of simulations. Therefore, the only parameter which is varied in this set of simulations is the carbon self-compensation ratio. The minimum carbon self-compensation ratio required for 2DHG suppression was determined by running the carbon doped simulation with a range of carbon self-compensation ratios. In these simulations, no bias was applied and the density of any 2DHG formation at the back-barrier/AlN interlayer interface was monitored. The simulated 2DHG density as a function of self-compensation ratio is shown in Figure 4.15 where the 2DHG was completely suppressed at a donor density of 5.5×10^{18} cm^{-3} corresponding to a compensation ratio of ~ 0.4.

The simulated cross-section of the unintentionally doped back-barrier with this compensation ratio is shown in Figure 4.16(b) and displays hole concentration. Figures 4.16(a) and 4.16(c) show the band structure and net charge of the carbon levels respectively from a cut-line mid way

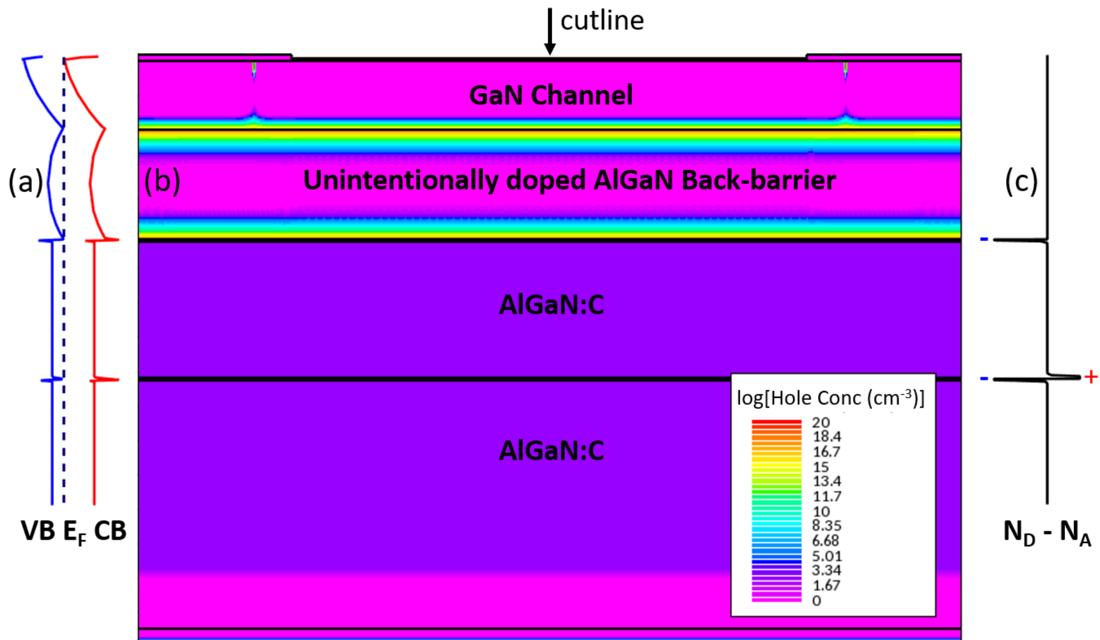

Figure 4.16: Simulation results of a transfer length measurement structure on the sample with the unintentionally doped back-barrier with all terminals at 0 V. A cross-section of the epitaxy showing hole concentration is presented in (b). The band structure from a cut line mid way between the contacts is shown in (a) and the net trap charge (ionised donors minus ionised acceptors) is shown in (c).

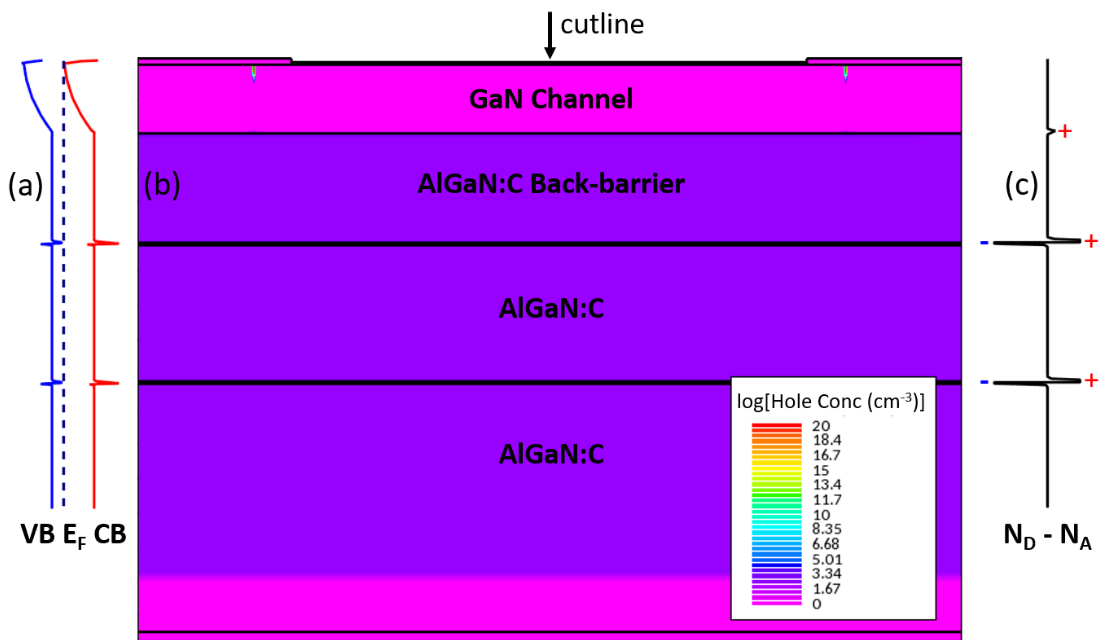

Figure 4.17: Simulation results of a transfer length measurement structure on the sample with a carbon doped back-barrier with all terminals at 0 V and $N_D/N_A = 0.4$. A cross-section of the epitaxy showing hole concentration is presented in (b). The band structure from a cut line mid way between the contacts is shown in (a) and the net trap charge (ionised donors minus ionised acceptors) is shown in (c).

between the contacts. At the upper and lower interfaces of the unintentionally doped back-barrier, holes accumulate with a density of 1.5×10^{12} and 8.6×10^{12} cm^{-2} respectively. The carbon doping results in a net negative trap charge below the interlayers as additional acceptors are ionised (as explained in section 4.4.5), which suppresses any 2DEG formation. The equivalent results for the simulation of the sample with a carbon doped back-barrier are shown in Figure 4.17 also with $N_D/N_A = 0.4$. In contrast to Figure 4.16(b), this simulation shows no accumulation of free holes in the back-barrier demonstrating a complete suppression of the 2DHG. Examination of Figure 4.17(c) presents the explanation; the interface charges are now neutralised by a net positive charge, revealed from the ionised carbon donors in a depletion region above the interlayer which was not present in Figure 4.16(c). The size of this depletion region was ~ 20 nm with $N_D/N_A = 0.4$ and increased up to ~ 35 nm with $N_D/N_A = 0.1$. The cause of this depletion region was outlined in section 4.4.5 and depicted in Figure 4.13. The indication is that the 2DHG can indeed be suppressed by carbon dopants but requires a compensation ratio of at least 0.4, in agreement with the previously estimated lower range of 0.1 − 0.6 [42]. Coupled with the previously discussed upper bound of 1 [157], the carbon self-compensation ratio in $Al_{0.08}Ga_{0.92}N$ must be $0.4 < N_D/N_A < 1$.

This set of simulations was repeated with the square interlayer profile rather than the realistic model. In that case, the 2DHG density was much higher and was not suppressed even at donor densities of 7×10^{18} cm^{-3}. This was because the polarisation charge was entirely located at the ideal heterointerface rather than being spread out over a few 10s of nm. The smearing of the interface charge from the gradient in Al composition means that it can be neutralised with a lower donor density since the depletion volume is larger. This demonstrates the necessity of modelling the aluminium composition profile realistically in simulations of the deep buffer.

The simulations require a donor density of at least 5.5×10^{18} cm^{-3} be present in the carbon doped back-barrier to suppress the 2DHG. In converting the donor density to a compensation ratio it was assumed that all of the donors were a result of carbon on the gallium site. In reality, to incorporate carbon during the growth, the growth temperature was reduced. This increases the generation rate of point defects such as nitrogen vacancies which also act as donors [172, 173]. This consideration implies the minimum bound of the self-compensation reported here is an overestimate. However, the density of additional point defects will be much lower than the required 5.5×10^{18} cm^{-3} donors and so the large majority must be related to C_{Ga}. Therefore, this will only introduce a small error in the lower bound of the compensation ratio.

4.5.2 Substrate bias ramp simulations

In order to verify these simulations were accurately representative of the samples, the simulated structures were subject to the same substrate bias ramps as in the experimental measurements. The simulation results are shown overlaid with the measurements in Figure 4.4(a). As in the experimental results, the 2DEG conductivity is independent of the substrate bias in the

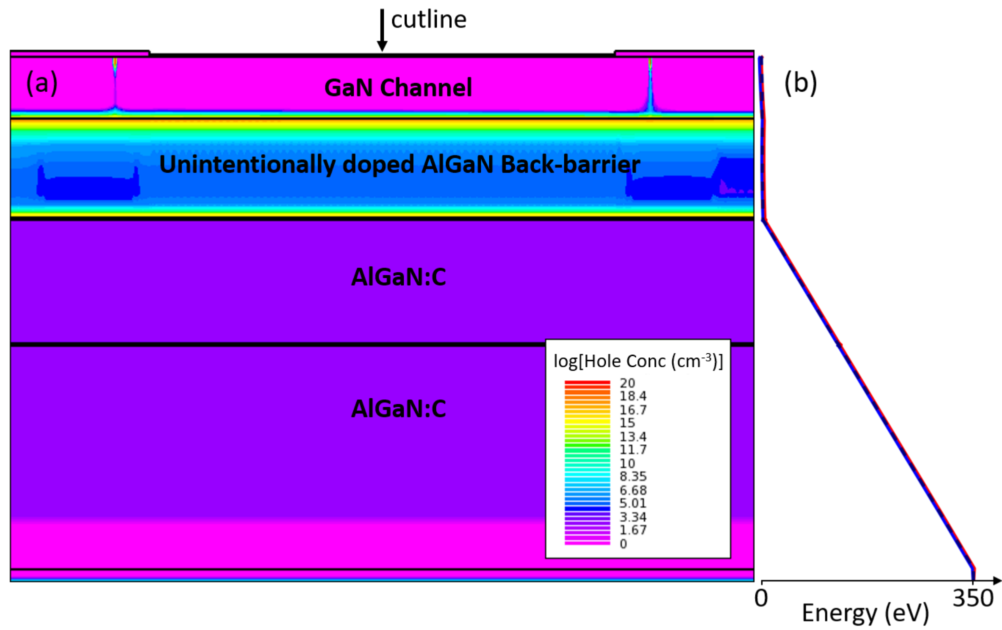

Figure 4.18: Simulated transfer length measurement structure with an unintentionally doped back-barrier and an applied −350 V substrate bias. A cross-section of the epitaxy showing hole concentration is presented in (a). The band structure from a cut line mid way between the contacts is shown in (b).

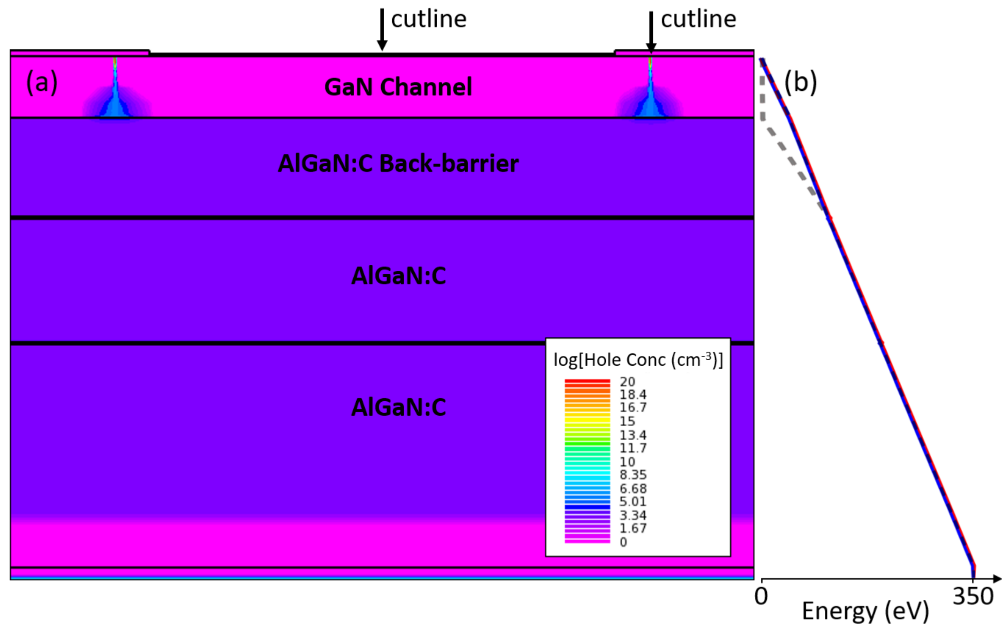

Figure 4.19: Simulated transfer length measurement structure with a carbon doped back-barrier (N_D/N_A = 0.4) and an applied −350 V substrate bias. A cross-section of the epitaxy showing hole concentration is presented in (a). The band structure from a cut line mid way between the contacts and directly through the contact spike is shown in (b), with a solid and dashed line respectively.

unintentionally doped sample and depletes linearly in the carbon doped sample. At applied substrate biases of $|V_{sub}| > 250$ V, the measured 2DEG conductivity on the carbon doped sample begins to deviate from the simulation. This is most likely related to the upper part of the stack starting to leak via a trap-assisted-tunnelling mechanism which is not included in the simulation. The simulated device cross-section with an unintentionally doped back-barrier is shown in Figure 4.18(a) with a substrate bias of −350 V. The corresponding band structure is shown in Figure 4.18(b) from a cut-line mid way between the contacts. From these results it is clear that the screening occurs from the top interlayer and all the field is dropped between this interlayer and the substrate. Holes are seen here flowing from the contact spike all the way to the interlayer where they are blocked and accumulate. The corresponding simulation result for the sample with the carbon doped back-barrier is shown in Figure 4.19. In this case, the vertical electric field is dropped linearly between the 2DEG and the substrate in areas not under a contact. Since the GaN channel layer is the same in both samples it is unsurprising that the holes are injected in the same way. However, with the carbon doped back-barrier, these injected holes pool under the contacts at the channel/back-barrier interface and form a locally reduced vertical electric field seen in the dashed grey line of Figure 4.19(b). The formation of these pools lower the electric field directly below the contact at the expense of increasing the vertical electric field in the back-barrier. This is an example of the Maxwell-Wagner effect which describes the accumulation of charge at discontinuities in material resistivity [174, 175]. This simulation result is consistent with the observed transfer length measurement structure gap dependence during the substrate bias ramps on the carbon doped sample and with the model discussed in section 4.4.4. These results are also relevant in Chapter 5 where the electric field below the contacts is discussed.

4.6 From AlGaN to GaN

This study has been concerning carbon doping in an $Al_{0.08}Ga_{0.92}N$ back-barrier. However, as discussed earlier, the back-barrier is more commonly GaN and so there will be interest in the transferability of these results to GaN. This is approached by examining the formation energies of C_N and C_{Ga} from the density functional theory simulations introduced in section 2.4.3. The root cause of the self-compensation is a result of the incorporation rates of the C_N and C_{Ga} configurations depending on the position of the Fermi level [92, 151]. If the Fermi level is high in the bandgap, the formation energy of C_N decreases, increasing the generation rate of acceptors and lowering the Fermi level. Equally, as the Fermi level becomes low, the formation energy of C_{Ga} becomes small giving rise to a large incorporation of donors, raising the Fermi level. In this way, an equilibrium Fermi level is found during growth which sets the self-compensation ratio. Therefore, based on this information it is likely that carbon will also be highly self-compensated in GaN, just as in AlGaN. There are other factors which influence the position of the Fermi level during growth such as the incorporation of hydrogen and these may explain why the

self-compensation ratio deviates from unity.

4.7 Conclusions

Substrate bias, lateral leakage and vertical charging measurements have been performed on two samples which differ only by the carbon concentration in the back-barrier. The differing behaviour of the samples was attributed to the formation of a polarisation induced 2DHG at the unintentionally doped back-barrier/AlN interlayer interface. The assertion was made that the presence of the carbon was the cause of the suppression of the 2DHG in the carbon doped sample. As only donors can neutralise the polarisation charge and suppress the 2DHG, this result allowed the determination of the minimum donor density introduced by the carbon. It was shown that the donor density required to suppress the 2DHG depended strongly on the composition profile through the interface. The same simulations with an ideal abrupt interface lead to unrealistic results, demonstrating the importance of accurately representing such features in these simulations. Additionally, leakage under the contacts was required in the simulations in order to match the experimental data. During the substrate bias ramps, these preferential leakage paths gave rise to substrate bias screening and transfer length measurement structure gap dependence in the unintentionally doped and carbon doped samples respectively. The simulated minimum donor density to suppress the polarisation induced 2DHG was found to be 5.5×10^{18} cm^{-3}. With the knowledge of the total carbon density from secondary-ion mass spectroscopy, the minimum carbon self-compensation ratio was shown to be 0.4 assuming an insignificant density of other point defect donors. The self-compensation ratio must also be less than unity since otherwise carbon doping would not increase the material resistivity. Therefore the carbon self-compensation ratio was determined to be $0.4 < N_D/N_A < 1$. The carbon self-compensation ratio is the key parameter for setting material resistivity and therefore strongly influences the vertical leakage and breakdown voltage. This value also defines the depletion behaviour under the gate in the off-state. Therefore, knowledge of this previously unknown value is fundamental for accurate device simulations.

Chapter 5

Vertical leakage and breakdown under Ti/Al contacts

The presence of preferential leakage paths under Ohmic contacts and the need to include them in simulations has already been observed in the previous chapter. This leakage reduces the resistivity and breakdown field of the GaN, thereby degrading the properties that make it desirable. This chapter uses a set of purpose designed structures to study and characterise the sub-contact leakage. Vertical leakage and quasi-static capacitance-voltage measurements were interpreted to identify the depth of the affected region under the contacts and place bounds on the resistivity of the leakage paths.

The work in this chapter was performed in collaboration with imec who grew the samples and processed the structures which were designed by Michael J. Uren. The structures were characterised here and a model was developed to explain the data. The results have been published in the IEEE journal Electron Device Letters [155]. Significant content has been reproduced from this publication. The flow of the research in this chapter is presented in Figure 5.1.

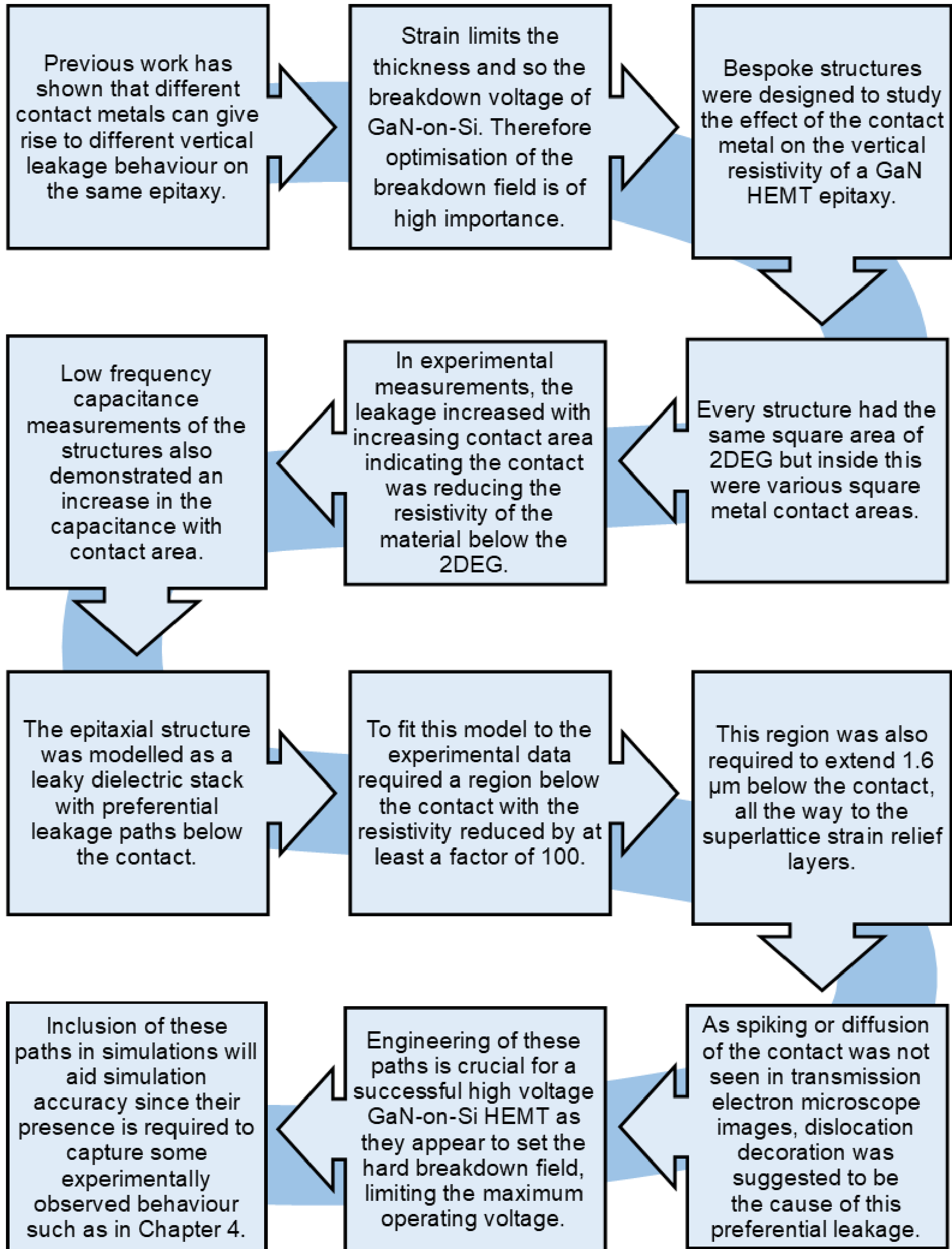

Figure 5.1: The flow of the research in this chapter.

5.1 Introduction

The high breakdown field associated with AlGaN/GaN HEMTs means they have the potential to make systems more efficient by operating at higher voltages. Growing the nitride layers on silicon, makes these devices more affordable and competitive since the substrates are cheap compared to SiC or bulk GaN and growth can take place in existing Si foundries. Coupled with the high electron mobility and high carrier density offered by the 2DEG, these devices are capable of sustaining high fields in the off-state and permitting high currents in the on-state.

However, point defects and other imperfections in the material quality introduce non-ideal behaviour such as current collapse and buffer leakage. As explained in section 2.5, current collapse, also referred to as dynamic on-resistance, is the phenomenon of a short term increase in the transistor on-state resistance after switching from the off-state to the on-state. It occurs when charge is trapped in the buffer (or the surface) during the high electric fields experienced in the off-state, which later act as a back-gate to the 2DEG. A reduced resistivity in the channel and buffer layers has been shown to allow this trapped charge to leak away on shorter time scales and thus has been linked to improved device performance. The presence of enhanced leakage paths in the sub-contact region has been observed to, at least partially, reduce current collapse in this way [41, 42]. As seen in the previous chapter and elsewhere [144], the inclusion of these leakage paths in simulations is required to match experimental data. Despite the importance of these sub-contact leakage paths, little is known about the extent to which they impact the vertical leakage or how far they extend. Prior speculative explanations have suggested the cause is contact spiking, metal in-diffusion into the GaN or the decoration of dislocations [41, 42] and all of these will increase the vertical leakage. Managing the off-state leakage and breakdown is critical for maximising the device operating voltage. Both of these can be achieved by minimising the peak electric fields. Lateral electric fields like those experienced in HEMTs in the off-state can be controlled by an optimised field plate design and a sufficiently large gate-drain access region. The challenge comes with management of the vertical electric fields. Historically, the solution to higher voltage operation has been to increase the thickness of the epitaxy. However, the maximum achievable thickness of AlGaN/GaN layers on Si is about 7 μm, after which the strain from the lattice mismatch causes cracking [36, 37]. An alternative solution is to optimise the breakdown field of the epitaxy in order to increase the hard breakdown voltage and this has been achieved with some success [176, 177]. Previously published work has shown that the vertical leakage through the epitaxy is influenced by the choice of contact metals [58]. In that work it was demonstrated that Ti/Al based contacts gave rise to an increase in the vertical leakage. However, contact metal stacks based on Ti/Al are desirable since they have been shown to offer low contact resistances and are compatible with fabrication in silicon foundries which cannot permit gold. This chapter studies the impact of Ti/Al/TiN contacts on the resistivity of an AlGaN/GaN HEMT epitaxy. Vertical breakdown and transient vertical leakage measurements have been applied to purpose designed vertical leakage structures to quantify the impact of

the contacts. Together with analysis of quasi-static CV data, the resistivity and depth of the preferential leakage paths have been evaluated. These results provide much needed information required for understanding the leakage dynamics through the epitaxy under the contacts, which is related to both buffer leakage and current collapse.

5.2 Experimental details

5.2.1 Epitaxy and structures

The structures in this work were fabricated on an AlGaN/GaN-on-Si epitaxy optimised for power HEMTs. The nitride layers detailed in Figure 5.2 were grown by metal-organic chemical vapour deposition on a silicon substrate which had a resistivity of > 1 Ωcm. AlN and AlGaN transition layers were grown on the silicon followed by an AlGaN/GaN superlattice for strain relief with a combined thickness of 1.9 μm. This was followed by a 1 μm carbon doped GaN buffer layer, a 0.3 μm unintentionally doped GaN channel and an AlGaN barrier to form a 2DEG. The epitaxy was passivated with Al_2O_3 and SiO_2 and the 2DEG sheet resistance was measured as 550 $\Omega\square^{-1}$. The Ohmic contacts were fabricated using the optimised process developed by Firrincieli et al. [59]. This entailed a full recess of the AlGaN barrier and the deposition of a Ti/Al/TiN metal stack. The Ti/Al thickness ratio was 0.05 and the contacts were annealed at 550°C which is lower than other equivalent processes. This resulted in fully Si CMOS compatible contacts with a low contact resistance of ~ 0.6 Ωmm. The unit Ωmm applies here since this contact resistance was measured using the lateral transfer length method described in Section 3.3. In a metal-2DEG junction the transfer length is much smaller than the length of the contact, so only the contact width affects the contact resistance. Taking a typical value for the transfer length as 1.6 μm, this result corresponds to a specific contact resistance of 0.01 mΩcm^2.

On this epitaxy a suite of vertical leakage structures were fabricated (shown in Figure 5.2) which were designed to study the impact of the contacts on the resistivity of the epitaxy. All structures had the same active area of 110 μm × 110 μm, isolated by a nitrogen implantation. The maximum energy of the nitrogen ions was 375 keV which equated to a maximum depth of ~ 550 nm. In the centre of each active area, a square hole was opened up in the passivation and the AlGaN barrier was recessed to make an Ohmic contact. The contact areas varied in size from 5 μm × 5 μm to 95 μm × 95 μm. On top of the Ohmic contacts a probing pad was deposited with an area of 100 μm × 100 μm which was the same for all structures. The design of the structures was motivated by the assertion that all structures with the same active area should show the same vertical current unless the presence of the contact affects the vertical leakage.

In addition to these structures, surface leakage structures were used which were capable of isolating and separating surface and buffer leakage [146]. This structure, those topology was introduced in section 3.3, centres on an isolated 100 μm × 100 μm Ohmic contact which is surrounded by a Schottky guard ring at a distance of 20 μm. Surface and buffer leakage with a

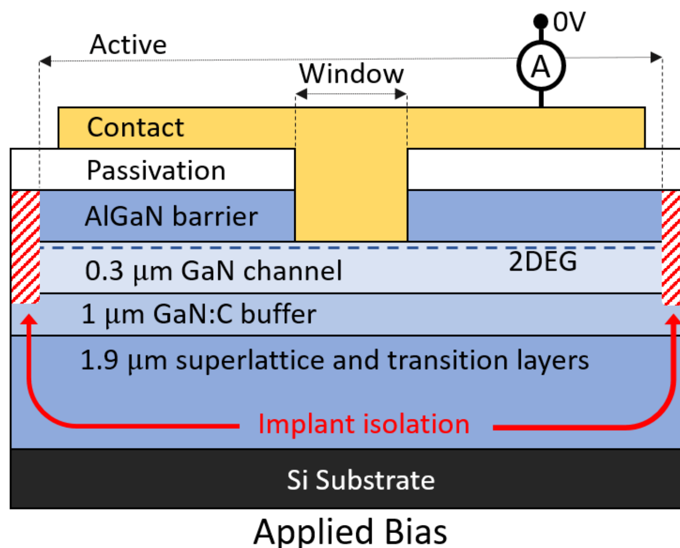

Figure 5.2: A cross-sectional diagram of a vertical leakage structure showing the layers of the epitaxy. The Ohmic contact area is defined by the window in the passivation but the active area is defined by the implant isolation.

lateral electric field were determined by applying a bias to the central Ohmic contact and 0 V on the guard ring and external Ohmic contact.

5.2.2 Characterisation

Vertical breakdown measurements of the epitaxy were performed using a simple 100 μm × 100 μm isolated Ohmic contact. This was compared to the same measurements on a vertical leakage structure with a contact area of 5 μm × 5 μm and an active area of 110 μm × 110 μm, as always. In all vertical measurements in this chapter, a negative bias was applied to the substrate such that the electric field in the epitaxy was of the same polarity as a biased HEMT with a positive drain with a grounded substrate. A Keithley 2657A was used to apply the substrate bias and the current was measured when applying 0 V to the surface with a Keithley 4200. The breakdown criterion was defined as a vertical current density of 10^3 Acm^{-2} (~ 100 mA).

In order to test for the presence of lateral conduction paths in the epitaxy, substrate bias ramps were performed as described in section 3.2.4. In the absence of lateral conduction paths, the magnitude of the substrate bias required to pinch off the 2DEG should be constant regardless of the active area. However, if such a lateral conduction path were present, it could extend laterally outside the isolation and effectively increase the active area. An example of this is a 2DHG which can extend up to 100 μm outside the active area [167]. A smaller isolated area would be more susceptible to this change in effective active area as it is a greater fractional change. Therefore, the pinch off voltages of smaller structures would differ more and more as the

isolated area became comparable to the extension area of lateral conduction paths.

The vertical leakage structures were measured by applying −200 V to the substrate using a Keithley 41501B and the current was measured from the surface contact at 0 V using a Keithley 4156A. The current was measured over 30 s and the current at the end of the transient was assumed to be only leakage current. The use of a transient measurement to determine the leakage current ensured the absence of any displacement or surface charging currents which may otherwise be present during a voltage ramp. Applying the voltage step at the start of the measurements causes a spike in displacement current which decays with a time constant determined by the resistivity and permittivity of the layers. The sampling time of 30 seconds was selected as it was sufficiently late that the decaying displacement current did not effect the measurement. This sampling time was equally sufficiently short that it was not sensitive to any change in the current over longer time scales as a result of, for example, (de)trapping of deep levels. An additional reason to use a transient measurement to assess the vertical leakage was the ability to account for surface charging. If surface charging were occurring, applying a ramped voltage would lead to the erroneous addition of a surface current. By using a transient, surface charging may only appear as a transient with a certain decay time constant which can be measured separately to assess its impact. This was done using the intentionally designed surface leakage structure shown in Figure 3.8. The structure was designed to measure the surface and buffer leakage components by biasing the central Ohmic contact as described previously. An additional, alternative application was to use the structure in the vertical leakage measurements. The central Ohmic and the guard ring were both held at 0 V with the substrate at -200 V. This guaranteed the current measured on the central Ohmic contact was only vertical current, since any lateral surface charging current would be supplied by the guard ring and not measured.

More than 35 of each of the vertical leakage structures were measured to ensure a sufficient distribution size. Following this, three vertical leakage structures of each geometry exhibiting mean vertical leakage behaviour were selected for quasi-static capacitance-voltage measurements. As described in section 3.2.3, a negative substrate bias was applied to the substrate using a linear ramp generator. The current was measured from the vertical leakage structures which were biased at 0 V using a 4156A. The bi-directional, continuous ramp was applied at a rate of -1 Vs^{-1} down to a voltage of −40 V.

5.3 Results

The vertical breakdown of the epitaxy, measured on isolated 100 μm × 100 μm Ohmic contacts is shown in Figure 5.3. A maximum breakdown voltage of 2.7 MVcm^{-1} was seen, demonstrating excellent breakdown performance. The same measurements were applied to vertical leakage structures with contact areas of 5 μm × 5 μm for comparison. The leakage current level and final breakdown field were both improved with the smaller contact, showing the same vertical

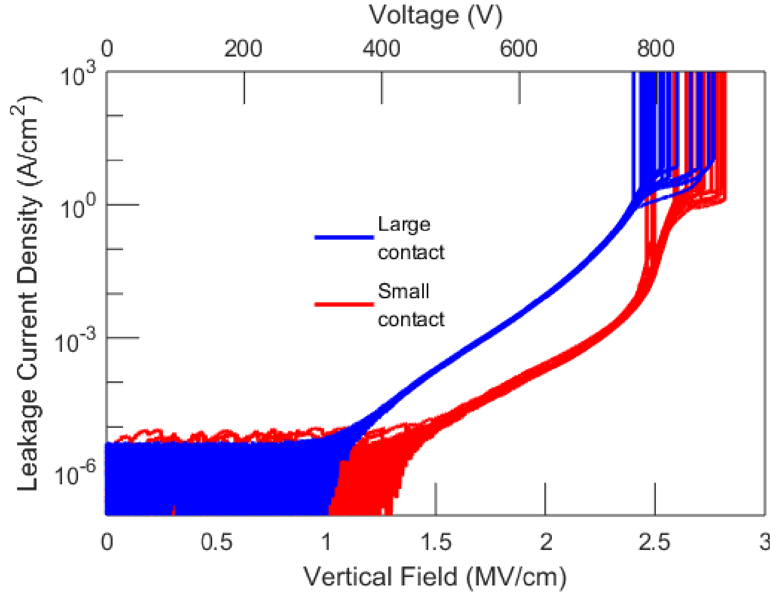

Figure 5.3: Vertical breakdown measurements on an isolated 100 μm × 100 μm contact (large contact) and a vertical leakage structure with a contact area of 5 μm × 5 μm (small contact). The measured current was normalised to the active area. The large contact structures showed an increased vertical leakage and on average, breakdown at an electric field 0.13 MVcm^{-1} lower.

leakage current at an electric field approximately 0.45 MVcm^{-1} higher. Meanwhile, the mean hard breakdown field increased by approximately 0.13 MVcm^{-1} with a smaller contact.

The results of the substrate bias ramp measurements on three different active areas are shown in Figure 5.4. The substrate bias was ramped down to −400 V and back at a ramp rate of −5 Vs^{-1}. Each of the curves were very similar and showed the same rate of pinch off, indicating no dependence on the size of the active area. On the downward ramp, the rate of depletion slowed between $70 < |V| < 180$ V followed by a return to a steeper gradient. On the return ramp, the 2DEG density returns to and saturates near the initial value by $|V| \sim 80$ V.

The surface leakage structure was first used by applying a bias to the central Ohmic and 0 V to the other contacts as shown in Figure 3.8. The lateral field between the central Ohmic and the guard ring was used to measure the surface resistivity. The guard ring current is shown in Figure 5.5(a). No buffer leakage was measurable above the noise floor on the external Ohmic contact. At 20°C the guard ring measured a surface current of 3.3 pA at the highest applied lateral field of 5 kVcm^{-1}. This corresponds to a 'sheet' resistance of $\sim 7 \times 10^{13}$ $\Omega\square^{-1}$. The current followed a power law relation with the electric field of $I \propto E^{1.32}$ and the current level increased with temperature like an activated process with an activation energy of $E_A = 0.7$ eV.

Secondly, the surface leakage structures were used to evaluate the effect of surface charging on the vertical leakage transient when −200 V was applied to the Si substrate. The central Ohmic and the guard were both set to 0 V ensuring only vertical current was measured by the Ohmic

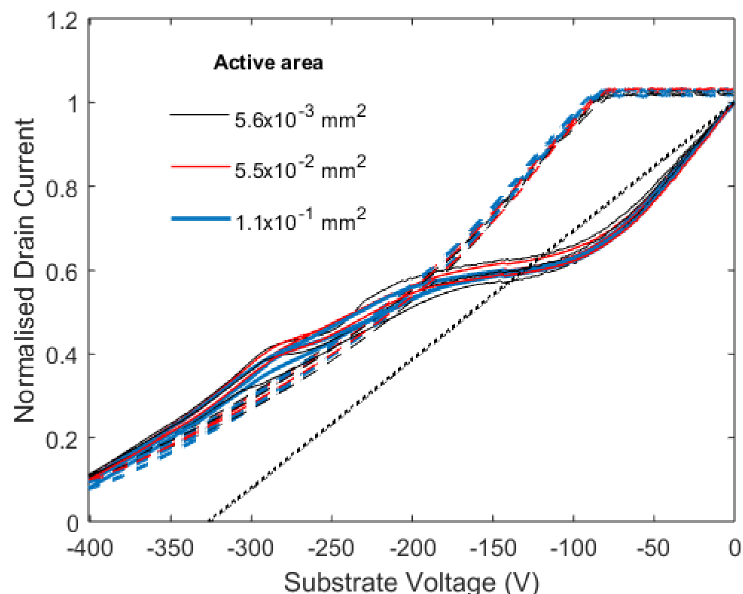

Figure 5.4: Substrate bias ramps on three different active areas showing pinch-off voltage independence from the active area. The substrate bias was ramped at $-5\ \mathrm{Vs}^{-1}$ with the solid and dash lines showing the ramp down and back respectively. The dotted line shows the capacitive coupling line that would be followed by an ideal dielectric. A reduced gradient was observed on the downward ramp in the substrate voltage range $70 < |V| < 180$ V.

inside the guard. The results are shown in Figure 5.5(b) and are compared with the transients of the vertical leakage structure with a similar contact area of 95 μm × 95 μm. At short time scales there are some subtle differences, but this does not affect the current level by 30 s.

The vertical leakage transients of the vertical leakage structure with the smallest geometry are shown in Figure 5.6(a). These transients have a decay time constant of $\tau =\sim 5$ s which is similar to that expected of carbon doped GaN, $\tau = \rho\epsilon =\sim 10$ s The gradient of the current at 30 s was small compared to the initial gradient indicating that processes with short time constants such as the displacement current spike had decayed. The current at 30s was used to make the histogram in Figure 5.6(b) which exhibits a Gaussian distribution. The same measurements and analysis were applied to all of the vertical leakage structure geometries and the parameters of the Gaussian fits are shown in Figure 5.7(a). Here it is apparent that the vertical current increases approximately linearly with contact area. From the y-intercept of the linear fit, the current density through the 110 μm × 110 μm active area in the absence of an Ohmic contact can be estimated as 120 pAmm^{-2}. Similarly, from the gradient of the fit, the additional current density due to the contacts is 325 pAmm^{-2}. This indicates that with 200 V across the epitaxy, the vertical leakage current under the contact metal is increased by a factor of ~ 3.5. The same data is shown on log-log axes in Figure 5.7(b). The approximately constant size of the bars indicate that the ratio of the standard deviation to the mean is approximately constant.

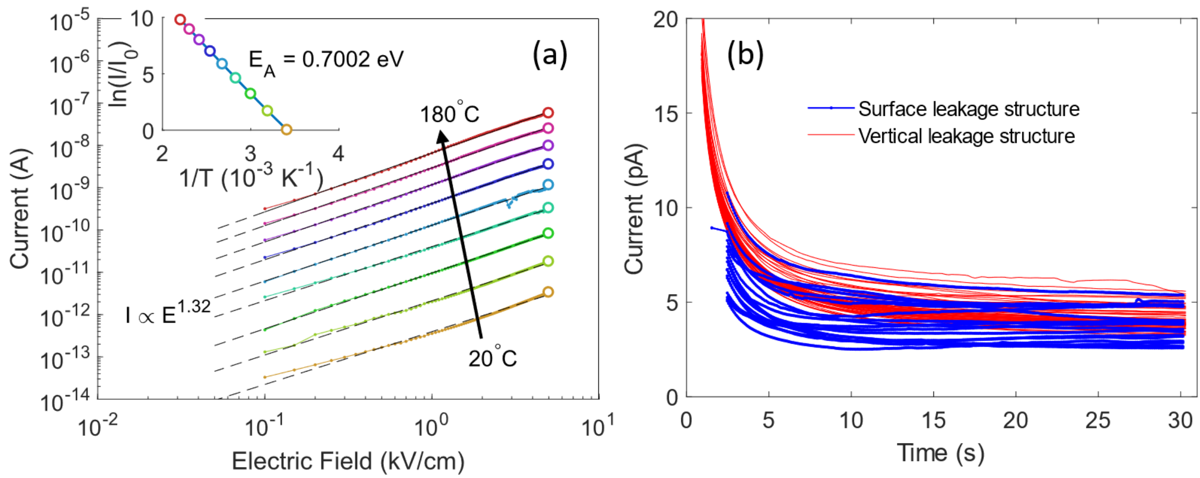

Figure 5.5: Results of measurements on the surface leakage structures when applying (a) a lateral field and (b) a vertical field. The guard ring current is shown in (a), indicating a lateral resistivity in the order of 10^{13} $\Omega\square^{-1}$ at 20°C. The current-field relation was a power law $I \propto E^{1.32}$ and the process is activated with an energy of 0.7 eV. The current on the central Ohmic contact, biased at 0 V, during vertical transient measurements is shown in (b) with a substrate bias of −200 V. Compared with the unguarded structure, these results show that charging of the surface only changes the first few seconds of the transient.

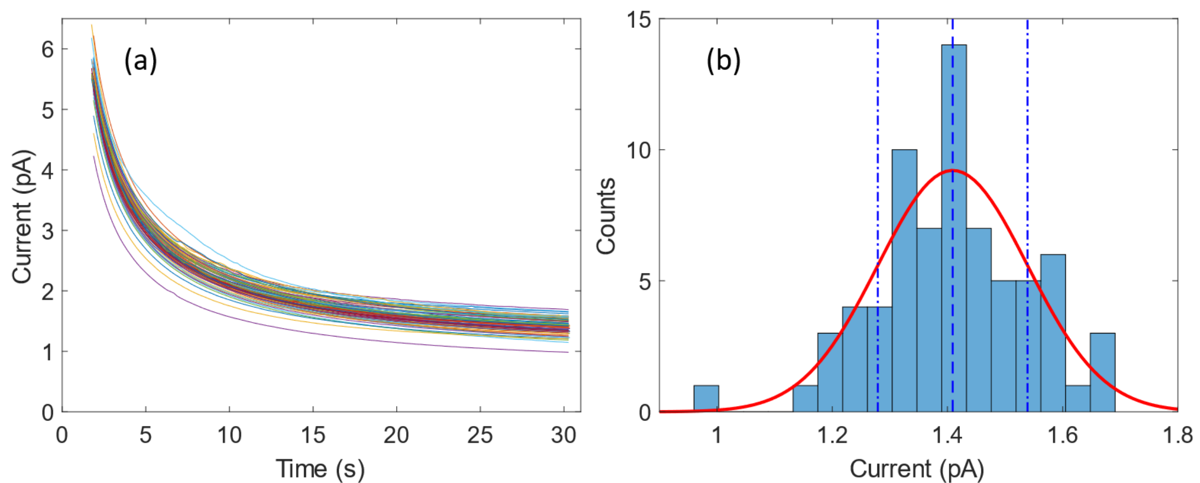

Figure 5.6: (a) The vertical transients measured on the vertical leakage structure with a contact area of 5 μm × 5 μm and a substrate bias of −200 V. The current at 30 s was binned to form the histogram in (b). The histogram was fitted with a Gaussian distribution to extract the mean and standard deviation of the distribution.

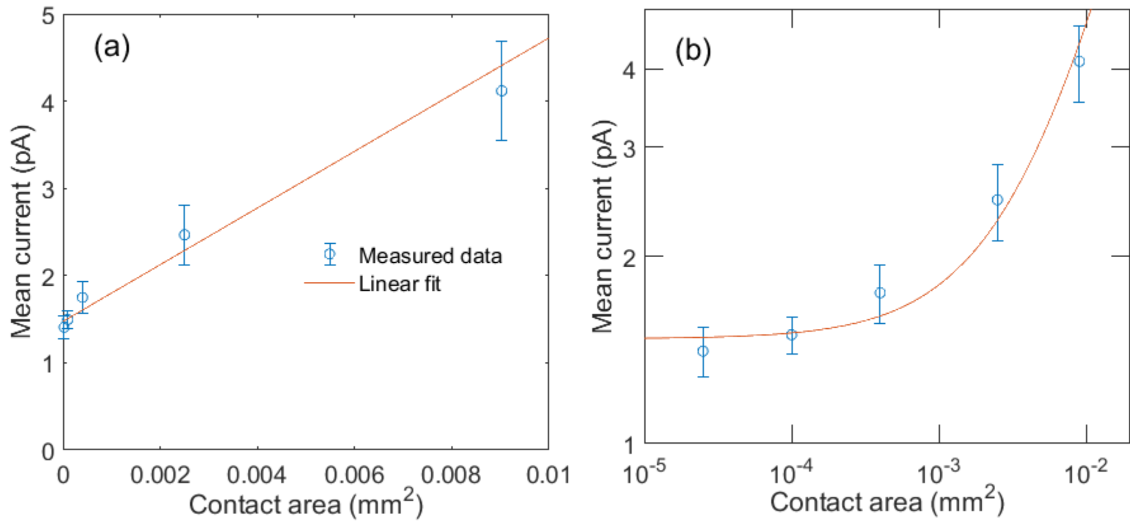

Figure 5.7: (a) The mean vertical leakage of the vertical leakage structures increases linearly with contact area. The bars show the standard deviation of the distributions. The same data is plotted in (b) on log-log axes where the similar sizes of the bars indicates the ratio of the standard deviation to the mean is approximately constant. The linear fit has a gradient of 325 pAmm^{-2} and a y-intercept of 1.47 pA.

The results of the quasi-static capacitance-voltage measurements on the vertical leakage structures with the smallest and largest contact areas are shown in Figure 5.8. The direct measurements are shown in Figure 5.8(a) followed by the decomposition of the bidirectional current-voltage curve into the displacement and leakage components in Figure 5.8(b). Finally, the displacement component of each measurement was used to infer the quasi-static capacitance of the structures in Figure 5.8(c). A parallel capacitance of 0.93 pF was subtracted from an open calibration. Like the vertical leakage, the capacitances of the structures increased approximately linearly with the area of the contact.

5.4 Discussion

All of the vertical leakage structures had the same active area of 110 μm × 110 μm, and regardless of the area of the contact, electrical contact was made to a 2DEG which had the same area. Therefore, with an ideal contact to the 2DEG, the vertical leakage between the 2DEG and the substrate would be the same for all structure geometries. However, as seen in Figure 5.7, increasing the area of the contact increases the vertical leakage current. This implies the presence of the contact introduces additional vertical leakage paths below the 2DEG. The increase in the vertical leakage current-voltage characteristics in Figure 5.3 with the larger contact indicates the leakage mechanisms are strongly influenced by the contacts. However, the small shift in the hard breakdown voltage indicates the final breakdown mechanisms remain similar.

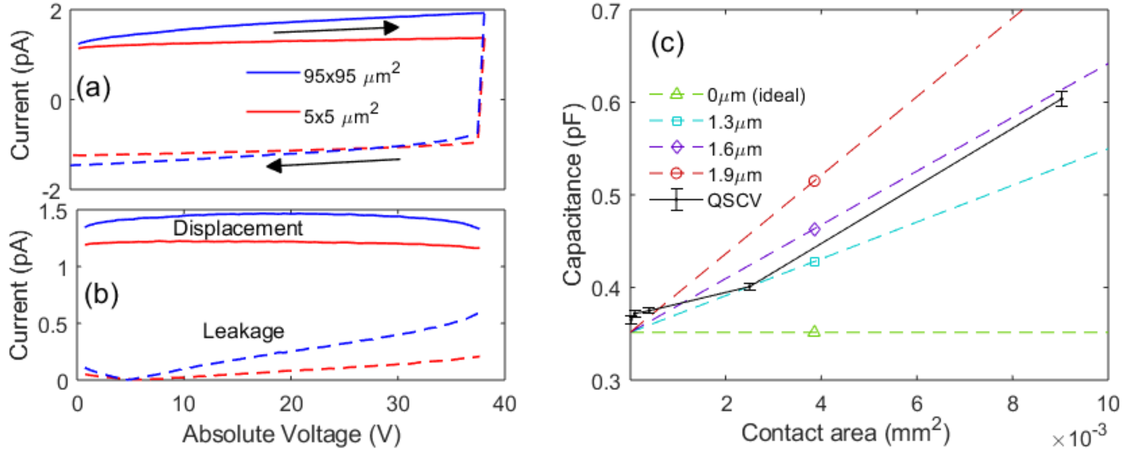

Figure 5.8: The quasi-static capacitance-voltage results of two vertical leakage structures. The measured current-voltage characteristics of the smallest and largest structures are shown in (a) which are then decomposed into the displacement and leakage components in (b) by identifying the fraction of the current which changes sign with the ramp rate. The displacement current is used with the ramp rate to identify the capacitance. The quasi-static capacitance of all the vertical leakage structures are shown in (c) and increases with contact area.

The substrate bias measurements showed no dependence on the active area indicating the absence of lateral conduction paths. This was expected since the buffer had been optimised to maximise breakdown voltage which would have been negatively impacted by the presence of lateral leakage paths. Therefore, the use of a 1D model in the analysis of the measurements on this epitaxy is justified. The deviation from the capacitive coupling line can be interpreted to infer the movement of charge in the epitaxy. One model to explain this data is that at $|V| \gtrsim 70$ V the top of the stack begins to leak, injecting positive charge into the buffer and reducing the vertical electric field near the 2DEG. This reduces its rate of depletion at the expense of increasing the electric field in the lower part of the epitaxy. Then at $|V| \gtrsim 180$ V, the entire epitaxy begins to leak and the 2DEG is resistively coupled to the substrate. On the return ramp, the 2DEG remains resistively and then capacitively coupled to the substrate until it recovers to its initial density. Then, the positive charge that was injected into the epitaxy lowers the barrier confining electrons to the 2DEG which rapidly neutralise it. This neutralisation of the positive charge as the substrate bias is removed causes the 2DEG density to saturate close to its initial value.

In Figure 5.5(a), a lateral field up to 5 kVcm^{-1} was applied between the central Ohmic and the guard ring of the surface leakage structure with the resulting surface current of 3.3 pA at 20°C. The current-field relationship of $I \propto E^{1.32}$ was similar to that expected for a surface leakage current which generally follows $I \propto E$. The leakage was also seen to be an activated process, consistent with surface hopping with an activation energy of $E_A = 0.7$ eV, likely related to the energy level of the surface states. Surface leakage on this process has been studied in detail by imec [178] and their results agree very well with those shown here. Specifically, the

near exponential increase in surface leakage with temperature. Apart from these data, all measurements were performed at room temperature and with much lower lateral electric fields, so surface leakage would have been at a minimum. In addition, there are two more considerations which support the argument that surface effects would not have affected the measurements. Firstly, during the quasi-static capacitance-voltage measurement, the magnitude of the applied substrate voltage was always less than 40 V, so although lateral fields on the surface were not well defined, those fields would be much lower than the 5 kVcm^{-1} experienced in the surface leakage structure. It is worth noting that there were no metal structures in the vicinity of the test structure, and all unbiased structures would be floating. Secondly, as shown in Figure 5.2, the size of the window in the passivation determines the contact area but the probing pad extends on top of the passivation to a 100 μm × 100 μm pad which is the same for all structures and acts as a field plate. Therefore, any residual surface charging would be the same for all structures and would appear as an offset in the displacement current. Equally, lateral leakage over the surface then down through the epitaxy would not affect the quasi-static capacitance-voltage measurements since the technique relies on the displacement component which is separable from the leakage current.

The vertical transients on the surface leakage structure in Figure 5.5(b) were able to isolate the component of the transient related to the surface. This was compared to the vertical leakage structure with the largest contact of 95 μm × 95 μm which had a similar contact area to the 100 μm × 100 μm of the central Ohmic in the surface leakage structure. When measuring the transient with the vertical leakage structure, the measured current would have contributions from both the vertical leakage and surface effects. Whereas with the surface leakage structure, the central Ohmic and the guard were at the same potential, therefore, no current would flow between them and the surface currents would flow from the guard. Consequently, the current measured from the central Ohmic must be only vertical current. This means that the difference between the transients of the two structures pertains to the surface leakage contribution. At early time scales of a few seconds, the transients differ, probably related to some surface charging. However, after 30 s the current was unchanged by the presence of the guard ring. Therefore, by using a transient technique to measure the vertical leakage, the effect of displacement and surface related currents have been removed.

5.4.1 Capacitance model

The quasi-static capacitance-voltage results indicated a linear relation between structure capacitance and contact area. An interpretation of this result is that the capacitance of the epitaxy directly under the contact is higher than the capacitance in the remaining, uncontacted active area. As the structure capacitance is the sum of these parallel capacitances, an increase in the area of the contact (and a decrease in the area of the uncontacted active area) would result in a net increase in the capacitance. An equivalent circuit diagram of this model is formalised in

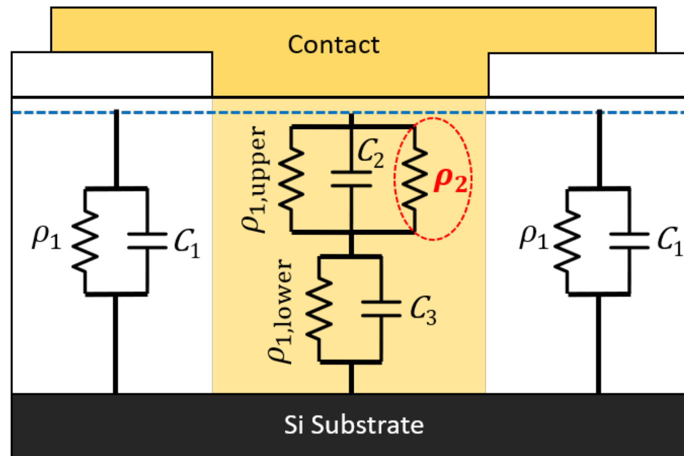

Figure 5.9: The equivalent circuit model constructed to explain the capacitance and vertical leakage dependence on contact area. The epitaxy is simplified into a leaky dielectric and an additional leakage path is included below the contact only, represented by ρ_2.

Figure 5.9. In the uncontacted active area, the epitaxy is simplified into a single leaky dielectric, represented by ρ_1 and C_1. Under the contact, the epitaxy is simplified into two layers; the top of the stack which is influenced by the contact and the lower part of the stack which has the same properties as in the uncontacted area. The resistivity of these two layers, $\rho_{1,\text{lower}}$ and $\rho_{1,\text{upper}}$ combine to have the same total resistivity as ρ_1 and likewise for the capacitances. The part of the model which introduces the dependence of the vertical leakage and capacitance on the contact area is the inclusion of an additional leakage path, represented by ρ_2. This resistor is in parallel with $\rho_{1,\text{upper}}$, reducing the resistivity of the upper part of the epitaxy compared to the uncontacted areas.

The effect of ρ_2 is to increase the leakage through the layer such that the leakage current is much greater than the displacement current of C_2. This means the layer no longer has a measurable capacitance and the capacitance of the epitaxy under the contact becomes C_3 rather than C_1. The capacitance per unit area of C_3 is higher than C_1 since this is a thinner portion of the epitaxy. An alternative way to interpret this is by looking at the potential drop between the two series resistors under the contact. The lower combined resistivity of $\rho_{1,\text{upper}}$ and ρ_2 compared to $\rho_{1,\text{lower}}$ means more of the potential is dropped over the lower layer. Therefore, under the contact a higher capacitance will be measured since the displacement current under the contact will now be $I_{\text{disp}} \sim C_3 \times \frac{dV}{dt}$. It follows that as the contact area is increased the capacitance of the entire structure increases.

Assuming that $\rho_2 << \rho_1$, the resistivity directly under the contact is approximately equal to ρ_2 and is also small compared to $\rho_{1,\text{lower}}$. Based on this, the exact change in the structure capacitance with contact area depends only on the depth to which the region of reduced resistivity extends below the contact. Accordingly, the only fitting parameter in this model is the depth that

ρ_2 extends down from the contact. The simulated response of the vertical leakage structures to the quasi-static capacitance-voltage measurements is shown in Figure 5.8(c) with different depths of ρ_2. The quasi-static capacitance-voltage measurements most closely follow the simulations with leakage paths extending 1.6 μm below the contact. This implies there is a region of reduced resistivity below the Ohmic contacts which extends all the way down into the top of the superlattice.

In Chapter 4, simulations of a similar epitaxy are shown in Figure 4.19. The contact metal stack of that sample was also Ti/Al based, though the process was different. In that process the AlGaN barrier was not recessed and the metal stack was Ti/Al/Ni/Au rather than the Ti/Al/TiN in this chapter. However, sub-contact leakage paths were included in that simulation and some qualitative comparisons can be made. A vertical cut-line of the potential directly under the contact spike is shown in Figure 4.19(b) as a dashed line. The effect of the contact spike with an applied vertical field was to inject carriers which reduced the effective resistivity of the GaN channel layer. In the channel layer, under the contact, there was no potential drop and this caused an increase in the electric field in the back-barrier. Since the vertical current depends on the electric field, this will cause an increase in the vertical leakage through the back-barrier under the contact. The subtle point here is that the depth of the region which is affected by the contact (and which is measured here) may be greater than the length of the sub-contact leakage path. This is since below the region of reduced resistivity, the electric field is higher, increasing field dependent leakage.

Regarding the physical cause of the additional leakage, transmission electron microscope images of other Ti/Al contacts have been compared. In-diffusion of the contact metals has been reported up to 30 nm down from the contacts [179, 180] and spiking has been seen as deep as 100 nm [181]. However, neither of these could explain a leakage path as deep as 1.6 μm. The scanning electron microscope (SEM) and transmission electron microscope images of the contacts here in this work are shown in Figure 5.10 and reveal a completely smooth metal-semiconductor interface, confirming the absence of spikes or in-diffusion on the scale of microns. One possibility which could give rise to such extended leakage paths without appearing in a transmission electron microscope image is the decoration of existing dislocations through the epitaxy. It is plausible that this could happen with the contact metals during annealing and such an affect has previously been observed with Ti/Al contacts [182].

In order to measure a higher displacement current under the contact, it must be true that the resistivity ρ_2, is sufficiently small that the vertical current is limited by the displacement current from C_3. Therefore, an upper bound for ρ_2 is the effective resistivity of the capacitor C_3 during the ramp. The effective resistivity of a capacitor during a voltage ramp can be derived as

$$\rho_C = \frac{V}{\epsilon}\left(\frac{dV}{dt}\right)^{-1} \tag{5.1}$$

by combining the definitions of a capacitor ($C = \epsilon A/d$), displacement current ($I = CdV/dt$) and

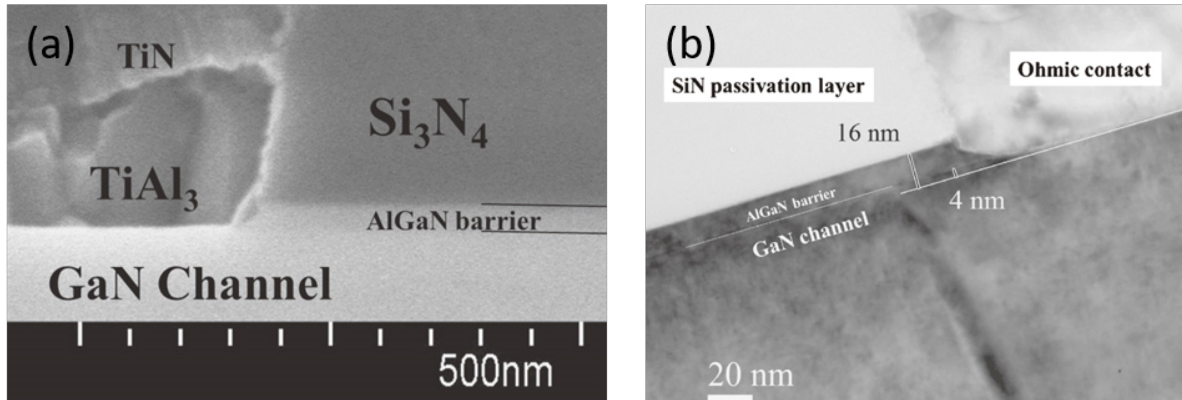

Figure 5.10: (a) Scanning electron microscope and (b) transmission electron microscope images of the Ti/Al/TiN contacts in this study [59]. The metal-semiconductor interface is flat and devoid of spiking. ©2014 The Japanese Journal of Applied Physics.

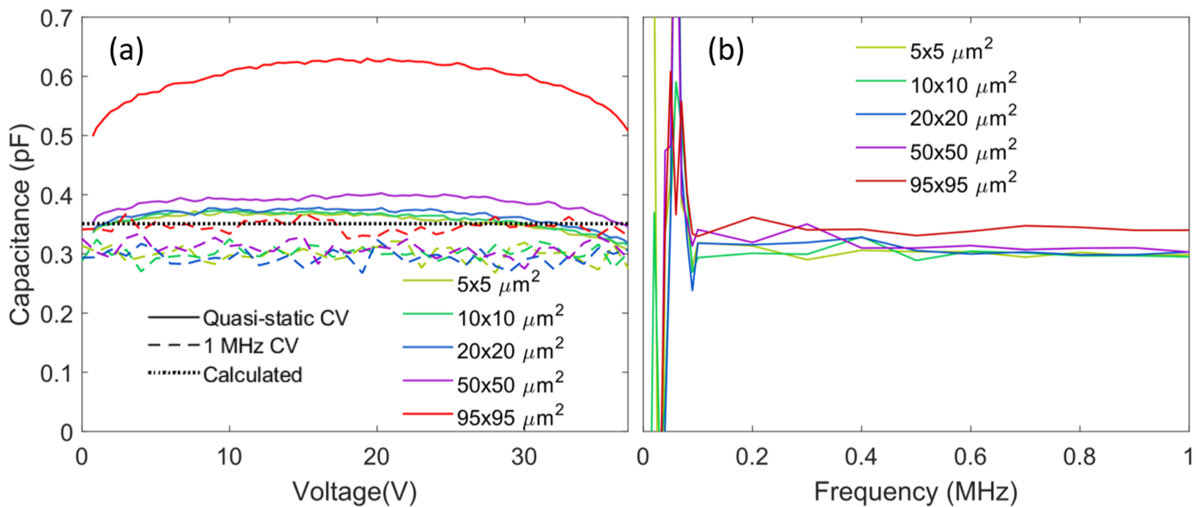

Figure 5.11: (a) The CV profiles of the vertical leakage structures with the indicated contact areas measured by quasi-static capacitance-voltage and conventional high frequency CV. The CV at 1 MHz is approximately constant for all structures and agrees fairly well with the calculated ideal capacitance. The capacitance as a function of measurement frequency in shown in (b). The capacitances of the structures do not disperse down to the lowest measurable frequency of 100 kHz.

resistivity ($\rho = RA/L$). This puts an upper bound on ρ_2 of $\sim 10^{11}$ Ωcm. The resistivity of the epitaxy in the absence of an Ohmic contact can be evaluated from the y-intercept in Figure 5.7(a). This intercept current with an active area of 110 μm × 110 μm and a total epitaxial thickness of 3.2 μm gives an average resistivity of 5×10^{13} Ωcm. This value is in good agreement with other estimations of the resistivity of carbon doped GaN [41, 183]. The implication is that the presence of the contact has reduced the resistivity of the GaN below it by at least a factor of 100.

In order to identify a lower bound for the resistivity of the sub-contact leakage paths, ρ_2,

conventional high frequency CV was used. The capacitance of the vertical leakage structures at 1MHz is shown in Figure 5.11(a) and compared to the quasi-static capacitance-voltage measurements. In contrast to the quasi-static results, all of the different structure geometries showed the same capacitance. This is expected since the leakage time constant ($\tau = RC = \rho_2\epsilon$) is much slower than the 1 MHz modulation used in this measurement. The capacitances of the structures were measured over a range of frequencies in Figure 5.11(b) in order to observe the capacitance dispersion at low frequencies, seen in the quasi-static measurements. The highest frequency at which dispersion is visible between the structures will indicate the time constant and hence resistivity of ρ_2. The lowest measurable frequency before the parasitic capacitances and inductances of the measurement system increased the noise floor was 100kHz. No dispersion was seen before this point which indicates at the very least that $\frac{1}{\rho_2\epsilon} < 100$ kHz resulting in the bounds $10^7 < \rho_2 < 10^{11}$ Ωcm. This is the main result of this chapter; the assertion that leakage paths extend below only the Ohmic contact for as far as 1.6 μm into the epitaxy, with resistivities potentially as low as 10 MΩcm. The presence of such leakage paths, though not previously studied to this extent, are evident in the transfer length measurement structure gap dependence in a number of other back-bias studies [144, 149, 184], showing that this issue is widespread. Reading from Figure 5.3, suppression of these leakage paths can reduce vertical leakage by two orders of magnitude and increase device breakdown voltage by 5%.

5.4.2 Vertical leakage simulations

The distributions of the vertical leakage currents in Figure 5.7(b) showed an approximately constant ratio of the standard deviation to the mean. At first sight, this is unexpected with the model set forward in the previous section. The model attributes the additional leakage to dislocations under the contact becoming more leaky. It follows, that increasing the contact area increases the number of affected dislocations and so the mean leakage current is proportional to the contact area. However, it may also be expected that the standard deviation is proportional to the square root of the contact area. After all, the larger the number of dislocations under the contact, the larger the variation that is possible. This would result in a scaling with contact area of $\frac{\sigma}{\mu} \propto \frac{1}{\sqrt{\text{contact area}}}$ but this is not what is seen.

In order to understand this discrepancy, the vertical leakage distributions were simulated using MATLAB based on two simple model assumptions; (1) the vertical leakage occurs only along dislocations (bulk leakage is ignored) and (2), under the contact, the dislocations are more leaky than in the uncontacted active area. The procedure of the simulations is shown in Figure 5.12. The vertical leakage structures were simulated in 2D, in plan view. Therefore, vertical dislocations appeared as points whose locations were determined using a random number generator. The simulation started by filling a 200 μm × 200 μm area with dislocations until the specified dislocation density was reached. An example of this 200 μm × 200 μm area is shown in Figure 5.12(a) with the square active and contact areas overlaid. Following this, for a given

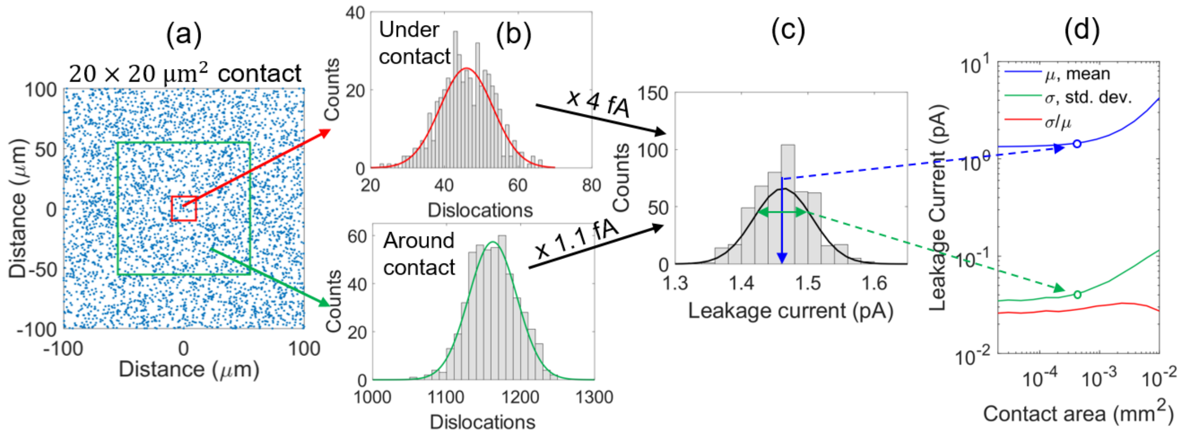

Figure 5.12: The procedure of the vertical leakage simulations is shown for a 20 μm × 20 μm contact. (a) A random spatial distribution of dislocations was generated with a random number generator and the number in the contact region and in the uncontacted active region were counted. (b) This was repeated 500 times to build up distributions for both regions. (c) The dislocations in each region were multiplied by a 'leakage per dislocation' to generate a leakage distribution for one structure (d) This was all repeated for a range of contact areas to simulate the scaling of the distribution parameters with contact area.

contact area, the number of dislocations under the contact and the number in the uncontacted active area around the contact were counted. This entire process was repeated 500 times to build up the distribution in Figure 5.12(b) of the number of dislocations in each of the areas for a given contact area.

To simulate the leakage distributions of the structure in Figure 5.12(c), the dislocations were multiplied by a value of the average 'leakage per dislocation' with 200 V across the epitaxy. The leakage current of the dislocations under the contact was increased by a factor which represented the preferential sub-contact leakage. All of the above was then repeated for a range of contact areas to build up the simulation of how the mean and standard deviation scaled with the area of the contact. The value of the 'leakage per dislocation' and the sub-contact factor were used as fitting parameters so that the simulated area dependence of the mean leakage agreed with the measurements.

The dislocation density of this GaN-on-Si sample was in the order of 10^9 cm^{-2}. It was initially assumed that 1% of these dislocations were electrically active, based on the observation that only dislocations with a Burgers vector of 1c are leaky [105]. The results of the simulation are shown in Figure 5.13(a) with a conductive dislocation density of 10^7 cm^{-2}. To fit the simulated mean leakage current to the measured data over the full range of contact areas, the current per dislocation was set to 1.1 fA and the factor of increased dislocation leakage under the contact was 3.6. This gave a 'leakage per dislocation' under the contact of 4 fA. This factor of 3.6 is in very good agreement with the measurement of this parameter (~ 3.5) extracted from Figure

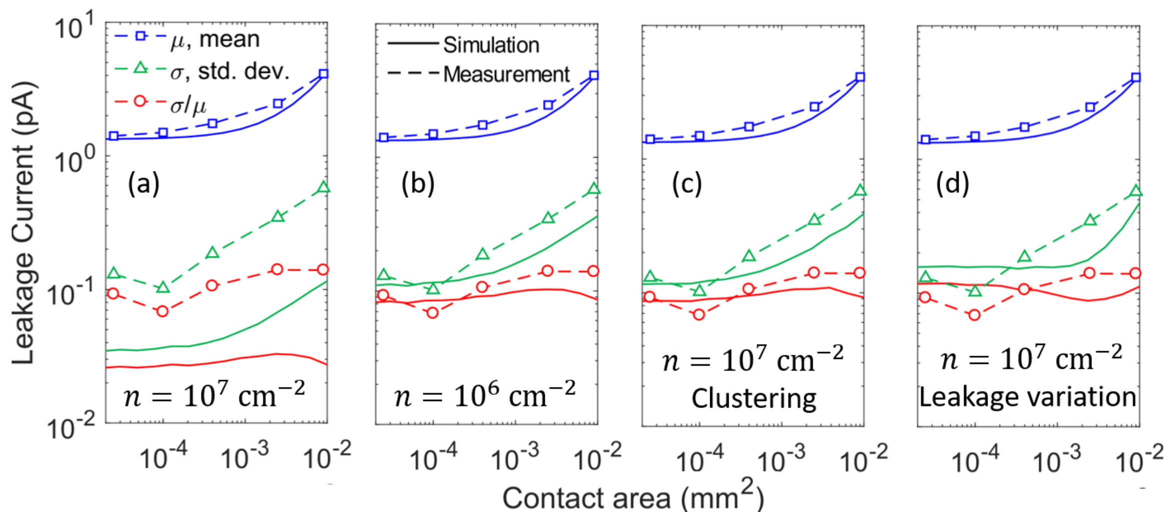

Figure 5.13: A comparison of four simulations with the measured distribution parameters. (a) With an electrically active dislocation density of 10^7 cm^{-2}, (b) a density of 10^6 cm^{-2}, (c) a density of 10^7 cm^{-2} with dislocation clustering, and (d) a density of 10^7 cm^{-2} with variation in the dislocation conductances.

5.7(a). To resolve potential confusion, this factor of 3.6 refers to the change in vertically averaged resistivity of the entire epitaxy under the contact. This differs from the estimated $10^2 - 10^6$ times reduction in resistivity estimated by the quasi-static capacitance-voltage measurements which was referring to just the material directly under the contact. This simulation shows all of the same trends as the measurements. Specifically, the ratio of the standard deviation to the mean is flat as seen in the experimental data. While this model may not be exactly what is going on, it demonstrates that these leakage distributions (and in particular the constant ratio of the standard deviation to the mean) can be explained using a simple model based on preferential leakage paths under the contact.

The magnitude of the standard deviation with contact area is predicted by the simulation to be much smaller. This suggests an additional source of random variation exists which is not being accounted for in the simulation. One way to increase the standard deviation in the simulation would be to lower the dislocation density by a factor of 10 and increase the dislocation leakage by the same factor to maintain the same mean current. This is shown in Figure 5.13(b) and is in better agreement with the measured data. However, this would correspond to only 0.1% of the dislocations being electrically active which is unrealistic. Recent studies of the relative densities of different dislocation types suggests the percentage of leaky dislocations is more like $1 - 10\%$ [105]. Alternatively, the source of variation could be from dislocation clustering. This was implemented in the simulation by introducing a clustering parameter, ξ. To generate a clustered dislocation distribution with average density, n, the first $n(1-\xi)$ dislocations were distributed randomly, as in the previous simulation. After this, the remaining $n\xi$ dislocation were allocated

sites within 1 μm of already existing dislocations. By this method, a clustering of $\xi = 0$ recovered the original unclustered simulation whilst $\xi = 1$ placed all dislocations in one cluster. The results of this simulation are shown in Figure 5.13(c) with $\xi = 0.91$ and gives an equally improved result with the dislocation density back at 10^7 cm^{-2}. It should be noted however, that the extent of the clustering required to give this result was unrealistically high; 91% of the dislocations are located near the site of the first 9% which were generated. Measurements of the spacial distribution of dislocations on GaN-on-Si wafers by cathodoluminescence [185] show a clustering of $\xi = 0.013$, much lower than that required here. The final investigated possible way to introduce additional variation was by adding random variations into the amount of current carried by each dislocation. The dislocation density was 10^7 cm^{-2} and the 'leakage per dislocation' was multiplied by a random number between 0.8 and 1.2. This range of variation was chosen as it best fitted the experimental data. The result shown in Figure 5.13(d) shows a very different shape to the previous simulations with the standard deviation only increasing sharply at high contact areas. The variation in leakage between different dislocations of ±20% may seem small. Considering that dislocation conductivity appears to depend strongly on the Burgers vectors [105], different dislocations could vary in leakage by orders of magnitude. However it is possible that the leakiest dislocation type will dominate the total current, and then it is the variation in leakage current of this dislocation type that defines the distribution which may only be small.

This idea that there may be orders of magnitude differences in leakage current between different types of active dislocations suggests an explanation for the simulation in Figure 5.13(b). The reduced dislocation density required to fit the measurements could be representative of 10% of the active dislocations being much leakier than the rest and defining the distribution shape. The 10^6 cm^{-2} density in this simulation would be referring to just these most leaky dislocations which would have an average spacing of approximately 10 μm.

To summarise these simulations, a simple 2D model is able to simulate the observed constant ratio of the standard deviation to the mean. The behaviour of $\frac{\sigma}{\mu} \propto \frac{1}{\sqrt{\text{contact area}}}$ can be forced in a non-physical simulation by setting the current carried by dislocations outside of the contact area to zero. Therefore, this constant ratio is a result of the interplay between the two distributions shown in Figure 5.12(b). The source of the underestimation of the distribution width in the first simulation in Figure 5.13(a) is still unknown. Possible sources relate to an overestimation of the electrically active dislocation density (or a fraction of the electrically active dislocations dominating the leakage), the clustering of dislocations, or a combination of both. Alternatively, it could be the case that this 2D model is oversimplified and a full 3D simulation is required, more like reality, in which the dislocation conductivity changes some way down under the contacts. However, adding a small random variation to the conductivities of the dislocations produced a result that did not agree well with the measurement data so this is less likely to be the source.

5.5 Conclusion

The effect that Ti/Al based Ohmic contacts have on the vertical leakage in AlGaN/GaN HEMT epitaxies has been studied. Vertical leakage structures were characterised to identify and quantify the additional vertical leakage as a result of the presence of the contact. Vertical current transients were measured on these structures and the magnitude of the leakage current was seen to increase linearly with the area of the contact. This is an important observation since it indicates that the presence of the contact reduces the resistivity of the epitaxy and hence, degrades the desirable properties of the GaN. Additionally, the vertical capacitance of these structures was measured both with conventional CV and by quasi-static CV. The quasi-static CV measurements revealed an increase in the structure capacitance, which was also linearly related to the contact area. These measurements supported the notion of a region below the contact with a reduced resistivity compared to the uncontacted epitaxy. The resistivity of this region was estimated to have reduced from 5×10^{13} Ωcm to between 10^{7} Ωcm and 10^{11} Ωcm. The quasi-static capacitance-voltage measurements also indicated that the preferential leakage paths extended $\sim 1.6\ \mu$m below the contact, all the way down into the superlattice. It was also observed that these leakage paths reduced the hard breakdown field. Therefore, optimising the Ohmic contacts is essential for maximising device operating voltages. These results indicate that the impact of the contacting process is not limited to the surface but may also play a role in managing current collapse and buffer leakage. The depth to which these paths extend is suggested here to be much greater than previously expected with previous estimations not exceeding 100 nm. It is worth noting that this was an unusually low temperature process and so a more typical 800°C process may have an even bigger effect. Inclusion of such paths in device simulations will enable improved simulation accuracy as they are a requirement for the recovery of observed behaviour.

CHAPTER 6

IMPURITY BAND CONDUCTION IN GAN-ON-GAN PN DIODES

The previous two chapters were discussing the development of HEMTs for high power applications. However, as explained in section 2.2.3, high power pn diodes with matched capabilities are required to compliment these HEMTs in many power switching circuit designs. The development of bulk GaN-on-GaN pn diodes for this purpose form the remainder of this thesis. In this chapter, the mechanism of reverse bias leakage is studied, resulting in a new model of leakage occurring through impurity band conduction in dislocation cores.

The devices in this section were grown by the Institute of Materials and Systems for Sustainability at Nagoya University. The author performed the measurements and developed the model to explain the data. The transient results and the model of impurity band conduction have been published in the AIP journal Applied Physics Letters [186]. Significant content has been reproduced from this publication. The flow of the research in this chapter is presented in Figure 6.1.

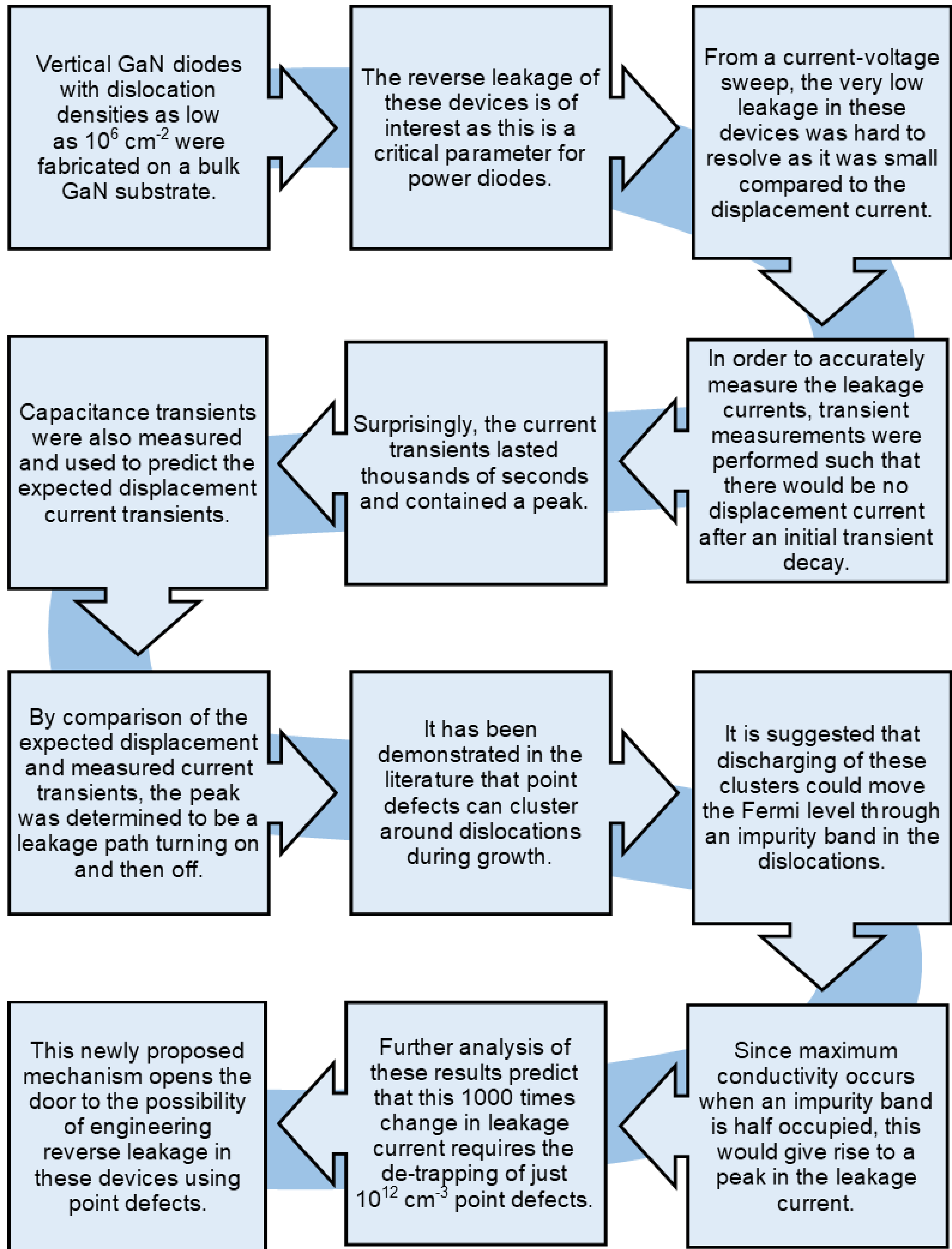

Figure 6.1: The flow of the research in this chapter.

6.1 Introduction

To meet the growing demand for efficient, high voltage and high power density switching systems, diodes with low on-resistance and simultaneous high breakdown voltage are required. GaN is an ideal material to meet this demand due to its high electron mobility and high breakdown field and outperforms its Si and SiC equivalents [53, 71, 72]. However, to scale up the breakdown voltage of lateral GaN-on-Si devices, the device area must be increased dramatically. This means a loss of yield which drives up the cost of production [33, 187]. Instead, vertical device geometries permit an increase in the breakdown voltage by increasing the epitaxial thickness rather than the area, and the device footprint can be even further reduced by contacting on the top and bottom of the wafer. In addition, as the forward biased current flows through the bulk material rather than a 2DEG, the device is heated over a larger volume resulting in lower peak temperatures [33]. Low cost vertical GaN-on-Si diodes have already been developed with some success but there are two main issues with this technology. Firstly, the devices exhibit reverse leakage currents much higher than would be possible with bulk GaN due to the high dislocation density [28, 139]. Moreover, the large lattice mismatch in these epitaxies limits the thickness of the drift region to 1.5 μm which severely limits the breakdown voltage [70]. The solution to both of these issues is homoepitaxial growth on bulk GaN substrates. Until recently, the development of GaN-on-GaN devices was limited by the availability of low cost bulk GaN substrates. However, high interest in this field has rapidly driven progress in the growth of affordable bulk GaN. Low dislocation density substrates are now readily available in 2" wafers [71] and even 4" and 6" wafers in small volumes [19], grown by hydride vapour phase epitaxy or ammonothermally as detailed in Section 2.3.2.

Dislocation density is a critical parameter in vertical GaN-on-GaN diodes as it puts a limit on the reverse leakage. Recent work has combined leakage measurements with electron microscopy techniques to identify the location of the vertical leakage. As described in section 2.4.5, analysis of the leaky dislocations indicated that pure screw dislocations with a Burgers vector of 1c are responsible for leakage in GaN-on-GaN pn diodes [105]. The dislocation density of free standing bulk GaN wafers is typically in the order of 10^6 cm^{-2}. This is much lower than GaN grown on foreign substrates such as GaN-on-Si where dislocation density is typically in the order of 10^9 cm^{-2}. This huge reduction in the dislocation density is the reason bulk GaN diodes can have much lower reverse leakage currents compared to GaN-on-Si devices [34, 139]. There has been extensive study of reverse leakage in Si doped GaN and many reports identifying the reverse current-voltage characteristics are consistent with variable range hopping [101, 106]. Since the leakage has already been correlated with the dislocation density, the logical conclusion is that the hopping current occurs along the length of the dislocation core [107, 108, 139].

In this chapter, the reverse bias leakage and capacitance are studied in the time domain. These transient measurements identify previously unreported leakage characteristics which are explained here by a model involving impurity band conduction. It is suggested that conduction

along the dislocation core is modulated by the charge state of surrounding point defect clusters. Although previously speculated [156, 157], this work represents the first direct observation of impurity band conduction along dislocations in GaN.

6.2 Device details

The vertical GaN-on-GaN pn diodes are shown in Figure 6.2(a) and were grown on an hydride vapour phase epitaxy bulk GaN substrate. The junction layers were grown by metal-organic chemical vapour deposition using Si as an n-type dopant and Mg as the p-type dopant. Starting with an n^+ interface layer on the substrate, an n^- drift layer of 5 μm was grown with a doping density of 3×10^{16} cm^{-3}. This was followed by p-GaN with a doping density of 4×10^{19} cm^{-3} for 0.5 μm. Finally, this was capped by a thin p^{++} layer of 8×10^{19} cm^{-3} as part of an optimised contacting recipe for Ohmic contacts to p-GaN.

As explained in section 2.5.2.1, the edge termination of the diode is critical as high surface fields can limit the reliability of the device and ultimately set the hard breakdown voltage. These devices were fabricated with a bevelled edge to reduce the surface electric field. The processing steps used to fabricate the bevelled edge are outlined in Figure 6.2(b). First a layer of photo-resist was deposited on the p-GaN. During exposure, the photomask was not in contact with the surface and instead, an intentional ~ 20 μm gap was present. This meant the exposure was not sharply defined causing the edge of the hardened photo-resist to be tapered. The result, after inductively coupled plasma etching, was a mesa structure with a slanted edge of 7-10°. The surface of the device was left unpassivated and Ohmic contacts were processed on the n- and p-GaN using Ti/Al and Ni/Au respectively. This optimised contact recipe was originally developed for LED fabrication and provided high quality Ohmic characteristics. Five circular device sizes were fabricated with diameters between 126 μm and 565 μm. The dislocation density of the substrate was stated by the manufacturer to be in the order of 10^6 cm^{-2}. This translates to an average distance between dislocations of 10 μm with around ~ 1000 dislocations in the largest device area of 0.25 mm^2, of which as little as a few percent may be electrically active [105].

6.3 Device Characteristics

6.3.1 Current-Voltage

To build up a picture of the device behaviour, an initial characterisation was performed. This began with the measurement of the reverse and forward current-voltage characteristics of which typical results are shown in Figure 6.3. The forward bias current-voltage characteristics in Figure 6.3(b) can be modelled by the Shockley equation (equation 2.4). The measurement was repeated over a range of temperatures with an obvious negative shift in the current-voltage characteristics with increasing temperature as expected from section 2.4.2. Assuming the exponential term in

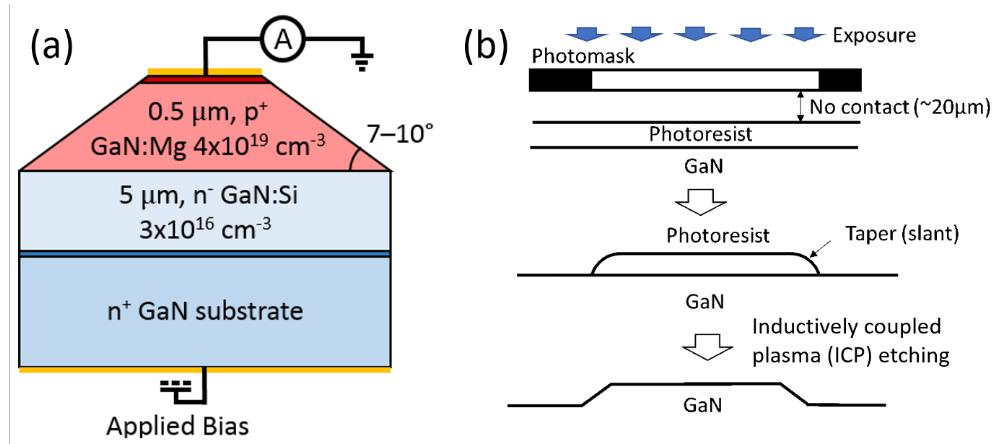

Figure 6.2: (a) A cross-section of the device layer structure. (b) The fabrication process to achieve a bevelled edge termination.

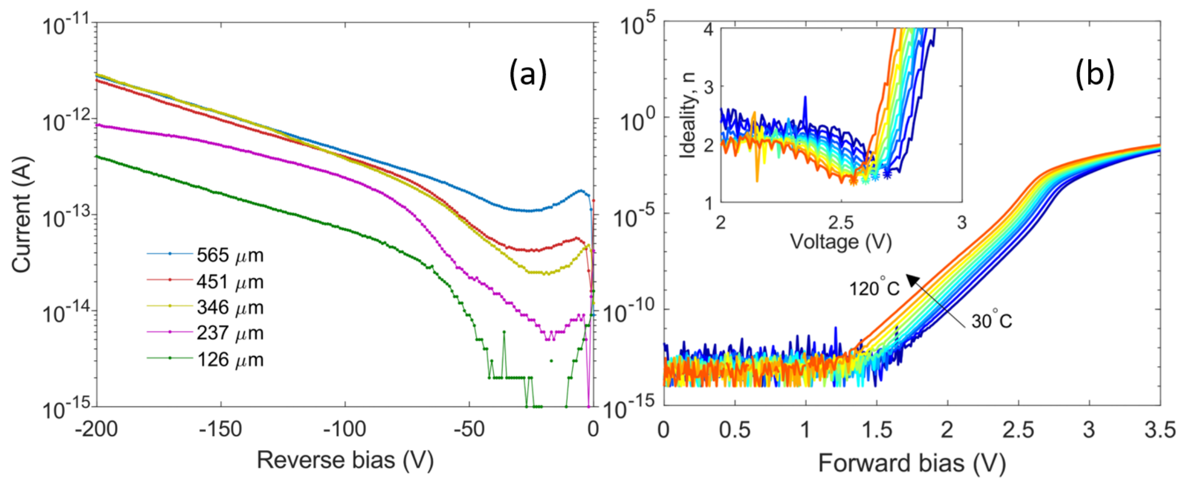

Figure 6.3: The reverse (a) and forward (b) current-voltage characteristics of the pn diodes. The reverse leakage ranged from 0.4 pA to 3pA at 200 V with an exponential dependence on voltage. The forward current-voltage characteristics of the largest diode are shown over a range of temperatures. The diode turns on at lower voltages as the temperature increases and has a peak ideality of 1.4 in forward bias (inset to (b)).

the Shockley equation is much greater than 1, equation 2.4 can be rearranged into the form

$$n \simeq \frac{q}{k_b T} \frac{V}{ln(I/I_0)} \tag{6.1}$$

This shows it is possible to determine the ideality from the gradient of the current-voltage characteristics on a log-linear plot. From this equation, the ideality is shown inset to Figure 6.3(b). The lowest ideality is approximately 1.4 before diverging as the series resistance becomes significant and limits the current. There is only a negligible change in the peak ideality with temperature, indicating the absence of thermally activated defects in the junction.

The reverse bias leakage current is shown for the five device sizes in Figure 6.3(a). The current-voltage characteristics were measured at a very slow ramp rate of 86 mVs^{-1} so that any displacement current was small and did not completely obscure the leakage current. The measured current appears to increase with size but not in any predictable way that obviously scales with area or periphery. The reverse currents at 200 V were ~ 0.4 pA and ~ 3 pA for the smallest and largest devices respectively. The approximately linear shape on this log-linear plot indicates an exponential dependence on electric field, characteristic of a hopping current (see Section 2.4.5).

6.3.2 Capacitance-Voltage

Capacitance voltage measurements were performed as described in section 3.2.2 to identify the behaviour of the depletion region with reverse bias. The results shown in Figure 6.4(a) are the only measurements from which all the analysis in this section is derived. When increasing the reverse bias from 0 V to 100 V, the capacitance of the largest device decreased from 30.9 pF to 7.8 pF. The size of the depletion width can be estimated using the depletion approximation and equation 2.13. The calculated depletion width of the four devices is shown in Figure 6.4(b). For the largest diode, the capacitances at 0 V and 100 V correspond to the depletion width increasing from 0.6 μm to 2.5 μm.

As explained in section 2.4.4, by re-plotting the data in Figure 6.4 as $1/C^2$, more information about the junction can be learned. This has been done in Figure 6.5(a). The overlaid dashed lines are the result of applying a moving average filter. This is a simple low pass filter to remove high frequency noise. The filter generates a smoothed curve one point at a time by evaluating the average value in a small window (5 points wide in this case) before moving the window by one point and generating the next point in the smoothed curve. Once the smoothed curve has been generated, this process can be repeated on the smoothed curve for further smoothing and was repeated 100 times here. Linear extrapolation of the curves to zero indicate a built-in junction potential of 3.7 V. The doping density can also be evaluated from this analysis. The derivative of equation 2.18 can be re-arranged into an expression for the doping density as

$$N_D = \frac{-2}{qA^2 \epsilon d(1/C^2)/dV} \tag{6.2}$$

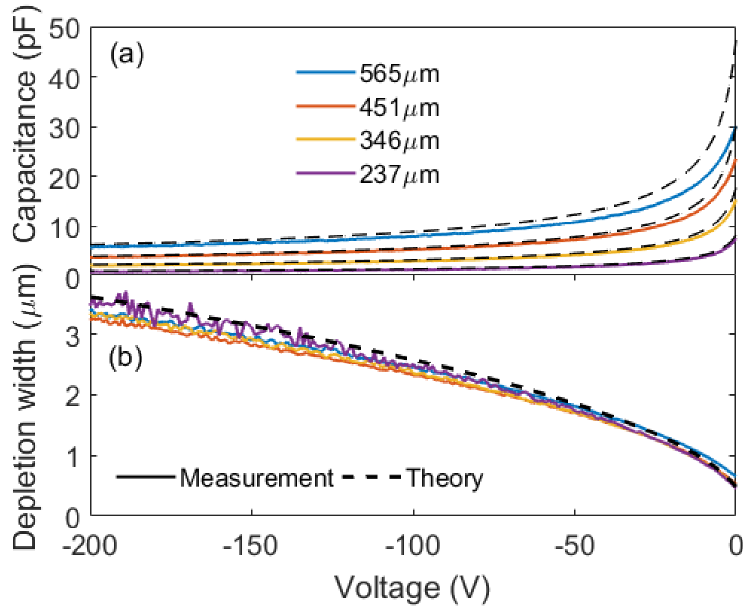

Figure 6.4: (a) Capacitance-voltage measurements on the four largest diodes with the diameters shown in the legend. The capacitance of the smallest diode was below the noise floor. (b) The calculated depletion width based on the measured capacitance, the diode area and the vertical permittivity of GaN which is 10.4 ϵ_0. The dashed lines are the theoretical predicted profiles of an ideal diode with the same properties.

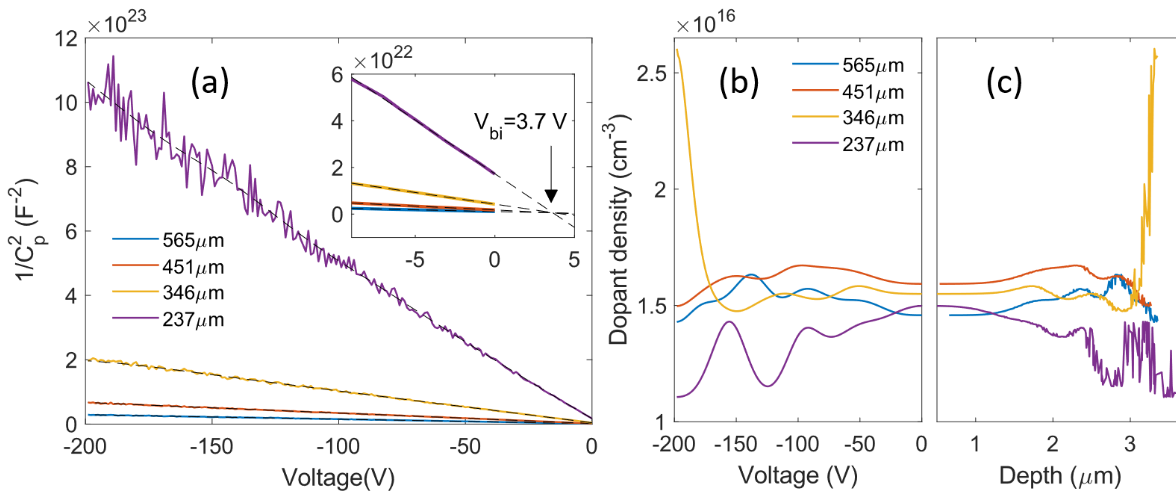

Figure 6.5: The data from Figure 6.4(a) is re-plotted in (a) as $1/C^2$. The data was smoothed with a moving average filter (dashed lines). Inset, the data near zero was extrapolated to find the built-in potential of the junction of 3.7 V. The dopant density was evaluated using equation 6.2 with the smoothed curves in (a). This is shown as a function of (b) voltage and (c) depth from the $W(V)$ curve in Figure 6.4(b).

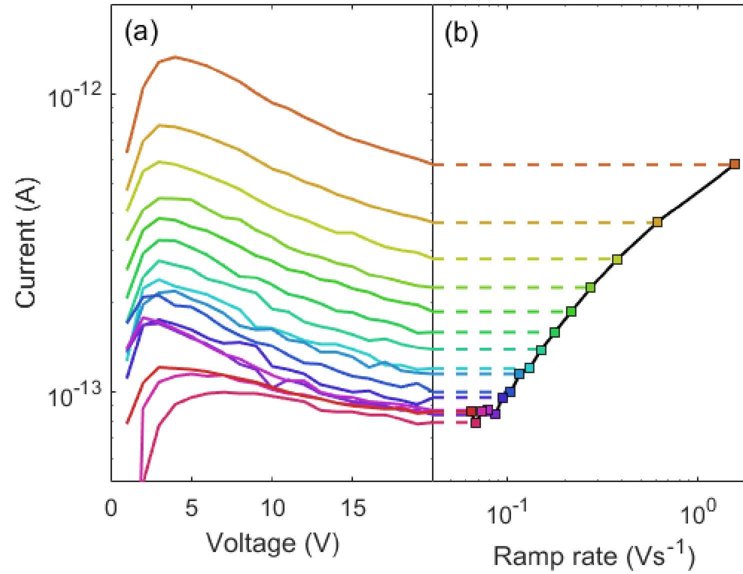

Figure 6.6: Reverse current-voltage measurements were repeated at various ramp rates on a 565 μm diameter device. The reverse current-voltage characteristics are shown in (a) and the current at 20 V reverse bias is shown as a function of ramp rate in (b).

A plot of this equation is shown in Figure 6.5(b). This value of the doping density is a local measurement at the edge of the depletion region which is why it may change with voltage as the depletion edge moves through the material. In conjunction with equation 2.13, the voltage can be expressed as the depth of the depletion edge. This allows the dopant density to be expressed as a function of depth into the n-GaN in Figure 6.5(c).

These measurements indicate an average doping density of about 1.8×10^{16} cm^{-3}. This is lower than the nominal density of 3×10^{16} cm^{-3}, however, these figures are fairly close considering the difficulty in controlling dopants at such low levels. Using the built-in junction potential and doping density it is possible to recreate the shape of the ideal diode CV profile from theory. This is shown overlaid to the measurement data in Figure 6.4 as dashed lines and models the data fairly well.

6.4 Transient behaviour

The current measured in the current-voltage curves was found to be strongly dependent on ramp rate, as shown in Figure 6.6. This was due to the fact that the reverse leakage current of the diodes was so low, that the displacement current was comparatively large and so made up a major contribution of the measurement at ramp rates above 0.1 Vs^{-1}. To identify the leakage current only, transient measurements were carried out such that after the displacement current spike (from the large dV/dt of applying the bias) had decayed, the current measured would be only

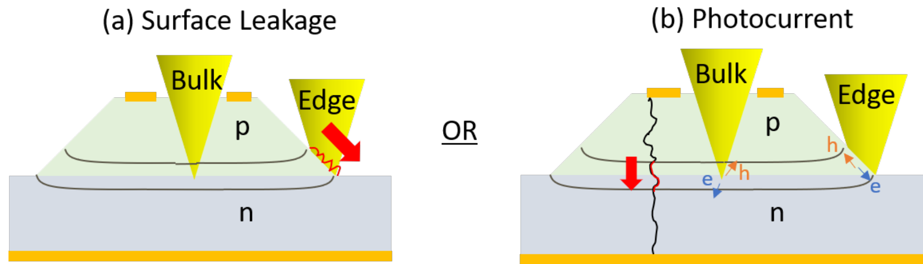

Figure 6.7: A schematic of where the devices are illuminated during the stress and the two possible outcomes of the measurement. (a) The transients are surface related: edge illumination causes an increased current or (b) the transients are not surface related and illumination of the bulk and the edge has the same effect.

the reverse leakage current at a fixed voltage. This is the same principle that was applied to the vertical leakage structures on the HEMT epitaxy in Chapter 5. These measurements yielded surprising transient results and are the subject of the remainder of this chapter.

6.4.1 Experimental details

Diodes with an area of 0.25 mm^2 were subjected to current and capacitance transient measurements. In both cases the devices were measured in a reverse bias stress for 1000 seconds then for another 1000 seconds with 0 V across the device. This was repeated sequentially with increasing reverse bias stress voltages between 20 V and 100 V. Immediate repeats of this measurement gave the same results showing that there were no long term effects such as charging or degradation. Following the current transient measurements, the same sequence of stress and recovery conditions were repeated to measure the capacitance transient behaviour. The current transients were measured with a Keithley 4156A and the capacitance transients with a Keithley 4200 with a high voltage capacitance measurement unit.

To investigate the possibility that any transient features were the result of surface effects, the transients during reverse bias stress were carried out under illumination with a broadband sub-bandgap light source. If a surface hopping current was present at the edge of the device, illumination of the surface would lower the barrier to hopping and increase the surface leakage. This was compared to a measurement where a part of the junction in the bulk was illuminated through a hole in the contact so that surface hopping could be distinguished from a photo-current. As shown in Figure 6.7(a), if a surface leakage were present, illumination on the surface would increase the current but there would be no change when illuminating the bulk. Conversely, in Figure 6.7(b), if illumination of the bulk and edge gave rise to the same increase in current this would indicate the photo-generation of carriers was causing a photo-current and that any leakage present was not due to the surface but a bulk process such as dislocation leakage.

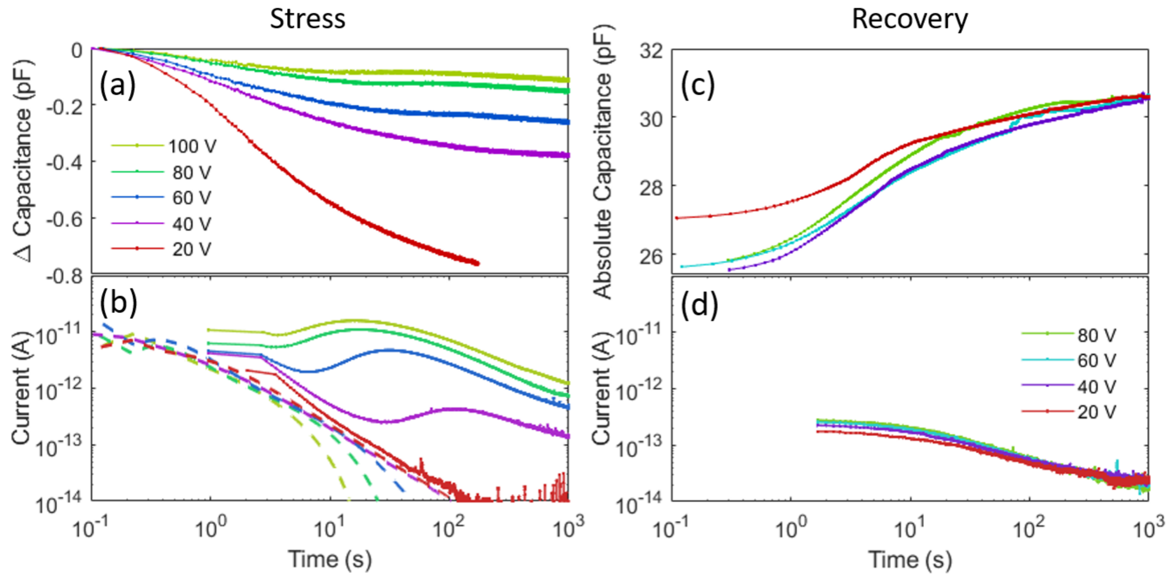

Figure 6.8: Transients of (a) capacitance and (b) current during reverse bias stress at the indicated bias. The current transients showed a peak which occurred earlier in time at higher stress voltages. The displacement current derived from the derivative of the capacitance transients in (a) are shown as dashed lines in (b) and agree fairly well with the measured currents early on and at low stress voltages. Capacitance and current transients are shown after the indicated stress in (c) and (d) respectively. All devices recovered to the same static capacitance of ~ 30.9 pF after 10^3 seconds. Evolution over a similar time scale was measured for the recovery current transients.

6.4.2 Results

The capacitance and current transients during stress and recovery are presented in Figure 6.8. The transients during stress in Figures 6.8(a) and 6.8(b) evolved over time scales of > 10^3 s with the current showing a peak, occurring at a time which was dependant on the magnitude of the stress voltage. This was accompanied by a subtle plateau in the capacitance transient occurring at about the same time. The results during the recovery phase of the measurement are shown in Figures 6.8(c) and 6.8(d). The capacitance transients show the devices recovering to the unbiased capacitance of ~ 30.9 pF over ~ 10^3 s and a current transient, despite no applied bias, on similar time scales. The sign of the recovery current was opposite to the current transient during the stress.

The prominence of the current peaks in the stress transient varied from device to device. The results shown here were the most distinct. The temperature dependence of the transients was investigated over a range of 30°C – 120°C, shown in Figure 6.9. Interestingly, there is no obvious dependence indicating this is not an activated process.

The results of the illumination measurements testing for surface leakage are shown in Figure 6.10. An increase in the transient current was observed when the device was illuminated both

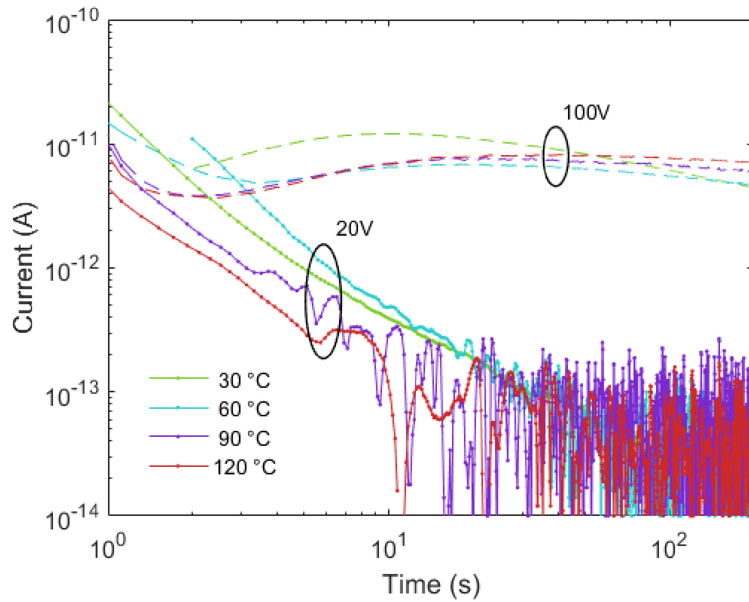

Figure 6.9: The transient during reverse bias stress at 20 V and 100 V at various temperatures. The time constants appear to be independent of temperature.

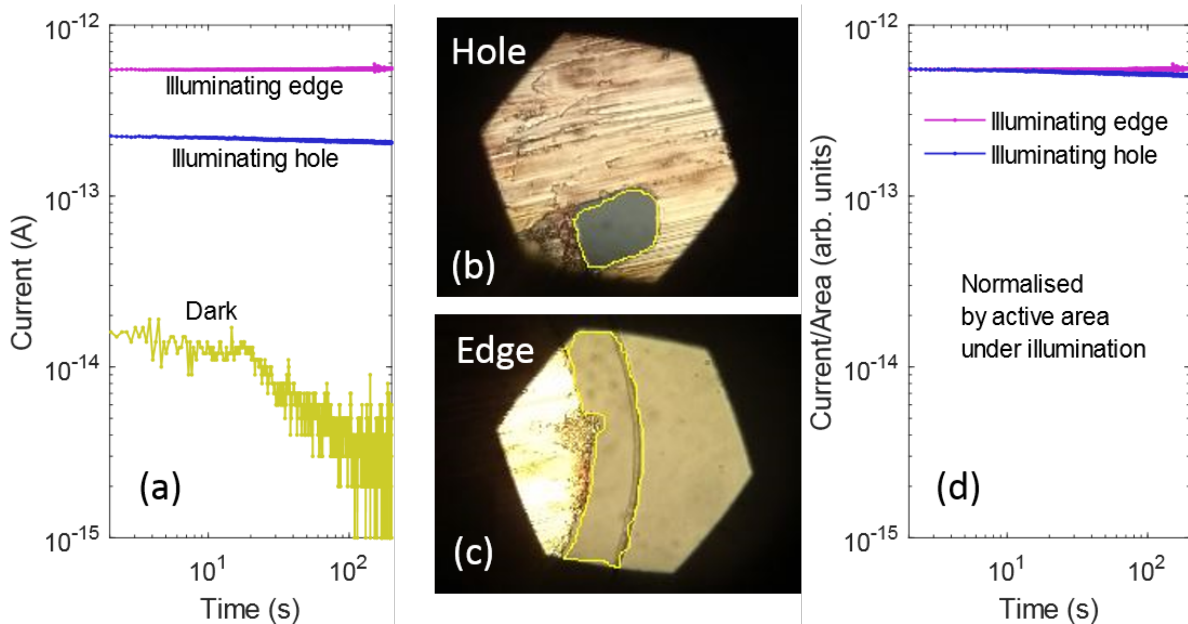

Figure 6.10: (a) Current transients at a reverse bias of 10 V in the dark and under illumination. The current levels were normalised in (d) by the illuminated active areas shown with a yellow border in (b) and (c). After normalisation, there was no difference in the illuminated transients.

through the hole and on the device edge compared to in the dark. The illuminated active areas are shown in Figures 6.10(b) and 6.10(c) circled in yellow and differ in size. When normalising the current transient levels by the area of the illuminated junction, these transients overlap and are very similar. This suggests that the increase in transient current seen when illuminating the junction is due to a photo-current as carriers are photo-excited in the illuminated depletion region. If the increased current were due to a surface leakage, illumination of the bulk junction through the hole in the contact should have had no effect on the magnitude of the current transient. Therefore, these results show no evidence to support the presence of a surface leakage current.

6.4.3 Impurity band conduction model

The peak in the current transients during stress is particularly intriguing since there is no existing model that can explain this behaviour. Transient peaks in reverse biased diodes have been reported before by Rosencher et al. [188]. However, that was in conjunction with a shrinking depletion region, causing the electric field to increased over time. Field assisted emission processes such as the Poole-Frenkel effect mean this causes an increase in the emission rate and the result is an increase in the transient current. When all of the traps have discharged, the transient drops and the overall shape is similar to that observed here. However, the capacitance transients in Figure 6.8(a) were decreasing over time meaning the depletion region was expanding and the electric field decreasing. Therefore, the model presented by Rosencher et al. cannot explain these measurements. Additionally, models involving multiple trap time constants cannot be used since this would cause a peak in the gradient of the transient but not a peak in the current. Surface leakage is not responsible after this was tested for and no evidence was found to suggest that the dark leakage was a surface phenomenon. Therefore, these results require a new model to account for this behaviour.

Capacitance transients are due to a changing depletion width which in turn are caused by a change in the trapped charge density. From the rate of change of the capacitance, the displacement current can be evaluated using $I_{disp} = V\frac{dC}{dt}$. This can be applied to the data in Figure 6.8(a) which is displayed as difference from the initial capacitance, because the subtraction of a constant does not affect the gradient. This is shown in Figure 6.8(b) as dashed lines and compared with the measured current transients. The measured current appears to follow the displacement current at short time scales, particularly visible in the 40 V and 20 V transients. However, starting at a time depending on the stress voltage, an additional current source is clearly visible above the displacement current which reaches a peak and then drops. If this charge flow were originating from the depletion region the capacitance would change and would be accounted for in the displacement current. Therefore the charge must be flowing all the way through the depletion region and must be a leakage current which turns on after a few seconds.

Considering the decreasing capacitance, it appears the depletion region is expanding. It is not possible to tell whether the expansion is occurring in the n or p side of the junction but in either

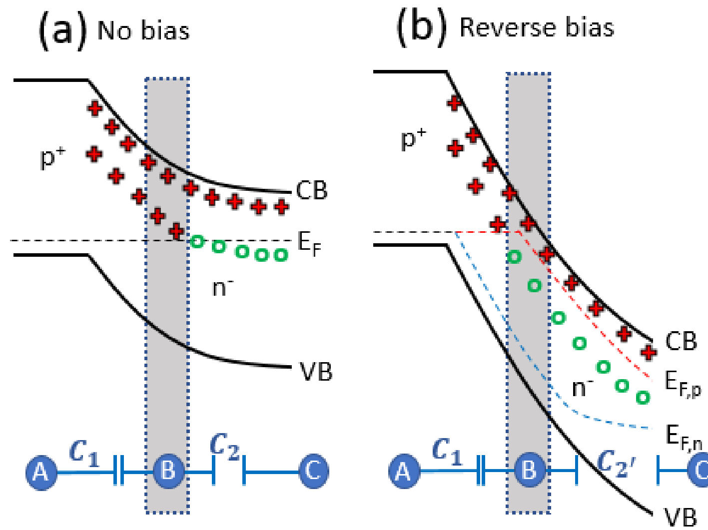

Figure 6.11: A sketch of the band structure of a pn diode (a) with no applied bias and (b) in reverse bias. The shallow Si donors are shown along with deep donors. In a region near the junction (shaded grey) some deep donors are neutralised in reverse bias. Below, the capacitances between the trapping region from the quasi-neutral regions are shown in blue.

case it means, under stress, the space-charge much be decreasing. This can occur in the n-GaN by a reduction of positive charge in the depletion region and in the p-GaN by a reduction of negative charge. Considering the n-GaN (and the equivalent is true for the p-GaN), a reduction of positive charge can occur with the neutralisation of donors or the ionisation of acceptors. During a reverse bias stress, there is limited opportunity for this to happen, however, one possibility is shown in Figure 6.11 where deep donors can be neutralised in reverse bias in a small region near the junction. A similar diagram can be constructed with a deep acceptor level to produce the same result of decreasing net charge in the n-GaN.

A model to explain the current transient peak was constructed based on two previously published observations; Firstly, dislocations in n-GaN are negatively charged by as much as 2.5 V [189–191] and in p-GaN are positively charged [189, 192]. This has been directly measured using electron holography and is potentially related to Ga vacancies in the dislocation core, however this remains a subject of debate. Based on this core charge, in the n-GaN, the band structure will be bent upwards around the dislocation and can be treated loosely as having a p-type dislocation core. The opposite is true for dislocations in p-GaN. Secondly, point defects have been observed to diffuse through GaN during growth, and cluster around dislocations [193]. Assuming the p-type dislocation core is in electrical contact with the p-GaN, when the junction is in reverse bias, the dislocation core will be in reverse bias with the surrounding n-GaN. The defect clusters around the dislocation will be in this depletion region and can change state, causing the displacement current.

As these clusters around the dislocation change their charge state, the conductivity of the core can be modulated by the field effect, much like gating a transistor channel. As the clusters change state, their charge will influence the Fermi level. Considering a leakage current along the dislocation core by variable range hopping [194, 195], the hopping probability depends on the density of states at the Fermi level [196, 197]. Therefore, movement of the Fermi level through an energy range with a higher density of states can increase the dislocation core conductivity. The peak conductivity is achieved when the Fermi level is in the middle of the impurity band and the density of states (DOS) is at a maximum [198].

Therefore it is suggested that the decreasing capacitance transients and the displacement current component of the current transients are a result of the discharging of deep defect states which are clustered around the dislocations. The observed peak in leakage current is attributed to a peak in conductivity along the dislocations as the Fermi level moves through an impurity band. It is assumed that the leakage current is limited by the conduction along the dislocations and that current flow between the dislocation core and the highly doped regions is lower resistance, possibly making a tunnel junction.

Figure 6.12 shows how defect clusters around dislocations can move the Fermi level in the dislocation core. In this example of deep donor states in n-GaN, the band diagram through the dislocation core is depicted from the dashed cut line in Figure 6.12(a). Figure 6.12(b) shows the equilibrium band structure where the shallow donors are not included for clarity. When stepped into reverse bias in Figure 6.12(c), the deep donor states in the shaded trapping region will neutralise, likely by tunnelling to the dislocation core. This is a temperature independent process and would explain why the transients are temperature independent. As the surrounding clusters discharge, they cause a displacement current and the depletion region must expand to maintain the same total charge. Additionally, the Fermi level in the core will drop which, assuming the presence of an impurity band, will temporarily increase the dislocation conductivity. The current transients resulting from this model are shown in Figure 6.13 and result in the same shape as the observed transients in Figure 6.8(b).

In line with this model, during recovery, the Fermi level would pass back through the impurity band as the clusters return to their original charge states. However, no peak was observed in the recovery transients in Figure 6.8(d). This is expected since despite a modulation of the dislocation conductivity, no field is applied across the diode and so no leakage current flows. Therefore, the measured current transients in recovery are proposed to be only displacement current. A comparison cannot be made between the measured recovery current transient and the expected displacement current like in Figure 6.8(b) because the potential distribution through the junction, needed for the calculation, is not known and cannot be measured.

One possible reason why these transient features have not been seen before could be due to the much higher dislocation densities in other devices. In these devices, the low dislocation density means there may be just a few dislocations per device, allowing the study of the transient

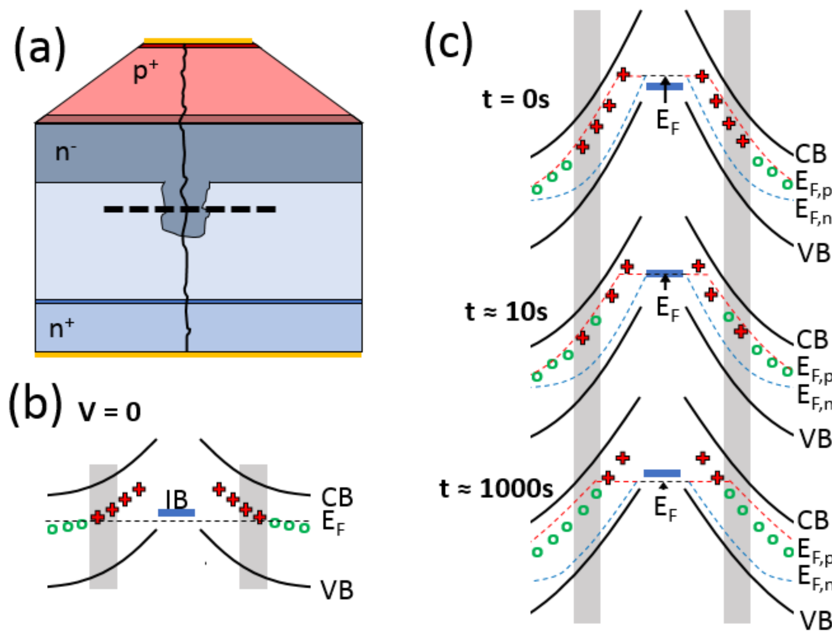

Figure 6.12: Band diagrams through a dislocation with the cut-line position indicated in (a) are shown at equilibrium (b) and in while evolving in reverse bias in (c). For clarity, the shallow donors are not shown. The proposed impurity band (IB) is represented by the blue shaded region.

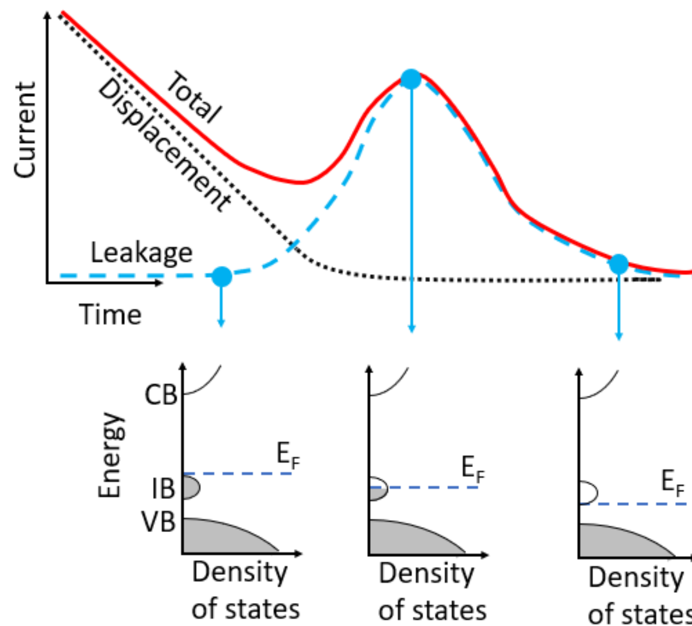

Figure 6.13: A sketch of a current transient decomposed into two components; displacement and leakage. Energy vs. density of states diagrams at progressively later times show how a monotonic movement of the Fermi level can give rise to a peak in the leakage current.

behaviour of just a few dislocations. The (dis)charging of the clusters by a tunnelling mechanism to the dislocation core means that the (dis)charging time constants will depend on the cluster-core separation. Random variation in this distance will introduce variation in the time at which the peak conductivity along the dislocation occurs. As the measured current is the sum of all of the dislocation currents, the greater the number of dislocation, the less defined the peak will be. Therefore, the same modulated impurity band conduction may occur in devices with higher dislocation densities, but the greater number of dislocations per device could mean the peak in the current is not visible.

6.4.4 Image Charges

As discussed earlier, the capacitance transients are caused by a change in the trapped charge density. During stress, the amount of charge moving out of the depletion region and causing the capacitance transient can be calculated by $Q = V \times \Delta C$. Curiously, the charge causing each of the transients in Figure 6.8(a) was approximately constant at $(3.8 \pm 0.4) \times 10^{10}$ cm^{-2}. The same analysis cannot be applied to the capacitance transients during recovery, since the voltage distribution in the junction is not known. However, the recovery charge can be determined from the current transient. Since the potential across the device is 0 V, there will be no leakage current and the current transient can be integrated to find the charge causing the transient. Once again, the charge in each transient was approximately constant. Although this time the charge was ~ 5 times larger at $(2.31 \pm 0.04) \times 10^{11}$ cm^{-2}.

In the model discussed in the previous section, clusters of point defects around the dislocation charge and discharge. The capacitance transients and recovery current transients are assumed to be a direct result of the (dis)charging of these clusters. Therefore, the amount of charge moving into the clusters during stress should be exactly equal to the amount of charge moving out during recovery - especially since repeat measurements yield the same result so there is no long term charging. This apparent disparity is resolved by the consideration of image charges.

Reconsidering Figure 6.11 as the pn junction between the dislocation core and the n-GaN, the depletion region around the dislocation expands when the device is in reverse bias. This has the effect of reducing the total capacitance of this depletion region. For a given cluster, the distance between the dislocation core and the cluster will be constant, with a constant capacitance C_1. However, as the junction is reverse biased, the distance between the cluster and the n depletion edge increases as the depletion region extends. This means the unbiased capacitance between the cluster and the depletion edge, C_2, decreases to C_2' in reverse bias as the depletion width is larger.

Continuing with the impurity band conduction model set out in section 6.4.3 the effect of this capacitance change is explained with reference to the locations designated by circled letters in Figure 6.11(b). When evolving towards equilibrium after stepping into reverse bias stress conditions, negative charge of magnitude Q moves from the dislocation core (A) to the trapping

region (B). To maintain net neutrality, an image charge flows around the external circuit from (C) to (A). It is the image charge flow around the external circuit that is measured and the magnitude of this charge, Q_{stress}, depends on the capacitances C_1 and C_2' as

$$Q_{\text{stress}} = \frac{QC_2'}{C_1 + C_2'} \tag{6.3}$$

When recovering from the stress the band structure looks more like Figure 6.11(a), with a small depletion region, and the same charge movement occurs in reverse; negative charge moves from the trapping region (B) to the dislocation core (A). However, this time the capacitances are different and the image charge that is measured flowing around the external circuit is

$$Q_{\text{recovery}} = \frac{QC_2}{C_1 + C_2} \tag{6.4}$$

These expressions show that a different charge flow around the external circuit can occur in the two stress conditions, despite the same charge, Q, moving the same distance in the device in both cases. The measured charge in the transients depends on the size of the depletion region. Therefore, a difference in the total charge in the transients between stress and recovery is expected. The factor of 5 difference measured here can be used along with a guess of the depletion region size to approximate Q (the real magnitude of cluster charging) and to find approximate values for the capacitances in Figure 6.11.

It has already been assumed in this model that the clusters are around the dislocations. This means that in reverse bias, C_1 remains high while C_2' becomes small. At a high reverse bias stress voltage $C_2' << C_1$ and Q_{stress} can be simplified to

$$Q_{\text{stress}} \simeq \frac{QC_2'}{C_1} \tag{6.5}$$

The image charge equations and the measured difference in transient charge are shown in Table 6.1 along with measurements of the static capacitance in reverse bias and unbiased. These five equations can be solved simultaneously to give an indication of the kinds of numbers which are associated with the unknowns. The solution to these equations is presented in the final column of Table 6.1. The high capacitance C_1 is indicative of the proximity of the trapping region to the dislocations. The magnitude of the charge density being trapped it also very reasonable since its magnitude is much lower than the density of impurities in the crystal. This result not only accounts for the large (apparently inconsistent) difference in measured charge during the stress and recovery transients but also demonstrates how a small change in charge density of just 10^{12} cm^{-2} is sufficient to modulate the bulk leakage by orders of magnitude.

6.5 Conclusion

GaN-on-GaN vertical pn diodes with very low reverse leakage currents have been studied. The low dislocation density allowed study of the transient behaviour of a few dislocations which showed a

Table 6.1: The image charge equations and measurement results are shown in the first two columns. These can be combined and solved simultaneously to produce the solution in the final column.

Image charges	**Measurements**	**Simultaneous solution**
$Q_{\text{stress}} \simeq \frac{QC_2'}{C_1}$	$Q_{\text{recovery}} = 5 * Q_{\text{stress}}$	$C_1 \sim 186$ pF
$Q_{\text{recovery}} = \frac{QC_2}{C_1+C_2}$	$\frac{1}{C_1} + \frac{1}{C_2'} = \frac{1}{6\text{ pF}}$	$C_2 \sim 37.2$ pF
	$\frac{1}{C_1} + \frac{1}{C_2} = \frac{1}{30.9\text{ pF}}$	$C_2' \sim 6.2$ pF
		$Q \sim 1.2 \times 10^{12}$ cm^{-2}

time dependent behaviour with previously unseen features. The model constructed to explain this data required the presence of an impurity band in the dislocations. If correct, this constitutes the first observation of impurity band conduction along dislocations in GaN. The model presents a mechanism whereby the Fermi level is driven through an impurity band in the dislocation core by the discharging of surrounding clusters which diffuse towards the dislocation during growth. The order of magnitude of the charge involved in the trapping/de-trapping processes was estimated by analysing the total charge in the transients and considering the method of images. These results and their analysis demonstrate the extent to which charged defects can affect dislocation leakage. The efficiency of power diodes is strongly dependent on the magnitude of the off-state leakage. Therefore, a full understanding of the off-state leakage mechanisms is critical for the development and optimisation of GaN-on-GaN vertical power diodes.

Chapter 7

The mean time to failure of GaN-on-GaN pn diodes

Unlike with Si based technologies, the reliability of GaN devices is still an area of active research and the factors which influence device lifetime are not completely understood. Specifically regarding vertical bulk GaN diodes, there have been no studies estimating the lifetime. This chapter applies a step stress measurement technique to the same bulk GaN pn diodes introduced in the previous chapter. An analysis method not previously applied in this field is used to extract the first estimations of the mean time to failure (MTTF) of this technology.

The devices were grown by the Institute of Materials and Systems for Sustainability at Nagoya University who also performed the electric field simulations. The measurements and the analysis were performed here. These results have been published in the Elsevier journal Microelectronics Reliability [199]. Significant content has been reproduced from this publication.

7.1 Introduction

As discussed in the previous chapter, vertical GaN-on-GaN pn diodes can outperform Si and SiC equivalents and operate at higher voltages with lower leakage currents than GaN-on-Si devices. An additional advantage of vertical devices is the ability to manage surface fields using edge termination techniques. In this way, peak electric fields can be moved into the bulk, away from the surface, and so the breakdown field of the device can begin to approach the bulk material limits [200].

Lateral GaN technology is maturing to the extent that devices are now being used in power switching systems. This level of maturity requires rigorous qualification to prove the devices are reliable and will not fail before a reasonable lifetime. Vertical GaN technology is not yet at

the maturity level of lateral GaN devices and so there are only a few in-depth reliability studies [201–204]. However as yet, there have been no estimations of the device lifetimes. In Si, failure by breakdown under high electric fields is attributed to the field induced generation of point defects. After the generation of a sufficient density of point defects, a percolation path can be formed which causes elevated leakage and ultimately, device failure. Lateral GaN HEMTs have been shown to follow similar failure distributions indicating that the failure of these devices can be described by the same model. This chapter aims to identify the failure mechanism for the vertical GaN-on-GaN pn diodes in Chapter 6 and to provide the first estimates of the mean time to failure of these vertical devices.

An accelerated lifetime test is applied using a step stress technique. This method was chosen over the more conventional time dependant dielectric breakdown (TDDB) technique as it ensures a bounded time to failure, reducing the total measurement time. The data are analysed using Weibull statistics which have been adapted to apply to step stress measurements. The results indicated that the mean time to failure depends only on the length of the device periphery, consistent with the formation of a surface percolation path. Through this analysis, a 126 μm diameter device is predicted to have a mean time to failure of 10 years under a constant reverse bias stress of 260 V.

7.2 Experimental details

The full growth and processing details of these devices were presented in section 6.2. One point to stress is that these devices are unpassivated. In this aspect, the fabrication will differ from commercial devices, when they are produced, as passivation increases the breakdown voltage. Three of the device sizes were selected for this study with diameters 126, 276 and 451 μm designated small, medium and large respectively. The devices were subject to a gradually increasing reverse stress which, starting from 0 V, was stepped up by 5 V every 60 s. As opposed to a time dependant dielectric breakdown measurement where the device is biased at a constant voltage until failure, this step stress technique is always increasing the reverse bias stress. This means that device failure will occur within a reasonable time window rather than in an unbounded time frame. Twelve of each device size were subjected to these measurements in order to generate three failure distributions. The criterion for failure was a reverse leakage current of 10 mA, corresponding to $6-80$ Acm^{-2}. The failure criterion was selected by experimentally measuring the typical leakage current before hard failure on a few devices as ~ 1 mA and increasing it by an order of magnitude. The bias was applied using a Keithley 2657A and the current was measured using a Keithley 4200 configured with a Keithley 4200-PA pre-amplifier.

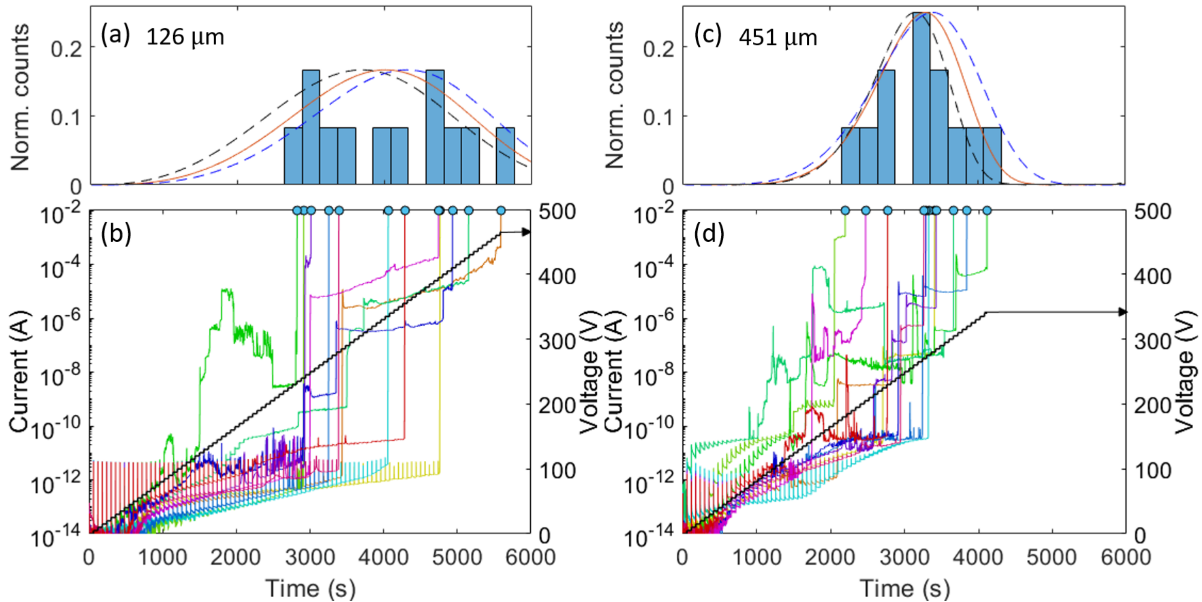

Figure 7.1: Step stress failure measurements on the small and large devices are shown in (b) and (d) respectively. The failure time is indicated with a circle when the current exceeded 10 mA. These failure times are binned in the histograms (a) and (c) with the Weibull step stress distribution fit and 95% confidence limits.

7.3 Results

The reverse leakage currents during the step stress measurements are shown in Figures 7.1(b) and 7.1(d) for the small and large devices respectively. The stress voltage over time is indicated on the right y-axis of these plots and the leakage current on the left y-axis. At low stress voltages, with the current below the pA level, current spikes at the edge of each voltage step are visible. While the leakage in this low current regime has been attributed to dislocation leakage [155], the spikes are caused by spikes in the displacement current ($C \cdot \frac{dV}{dt}$). As the current increases above this level, the leakage currents jump in steps both up and down before exceeding the failure criterion, at a time indicated by the circles. The small devices began to fail after ~ 2800 s at voltages greater than 230 V. This was later than the larger devices where failure began after ~ 2200 s corresponding to voltages greater than 185 V. The failure times of the small and large devices were binned in the histograms in Figures 7.1(a) and 7.1(c) respectively. The small devices demonstrated the ability to last the longest but also exhibited a broader distribution of failure times. Optical inspection of the devices after the measurement revealed a surface failure mechanism was responsible. Every device exhibited evidence of surface breakdown like that shown in Figure 7.2. In this optical image, dendritic structures are visible, extending from the bevelled junction towards the contact on the p-GaN.

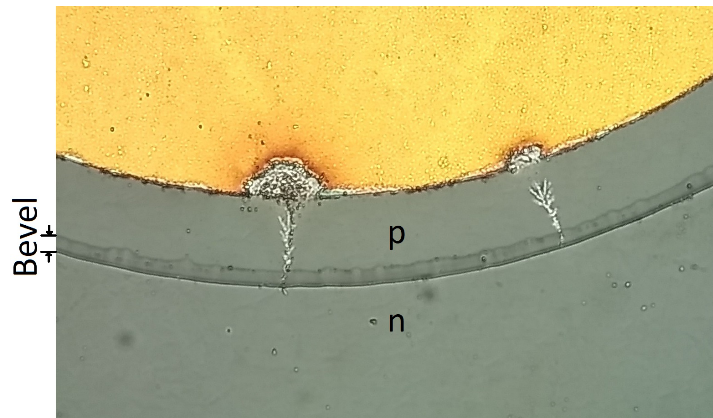

Figure 7.2: Photograph of the surface failure experienced by the devices. The dendritic structures originate from the pn junction on the bevel surface and extend towards the contact.

7.4 Analysis

The analysis of conventional time dependant dielectric breakdown measurements and estimations of device lifetimes are often achieved using Weibull statistics. In that analysis, the distribution of device failure times under constant voltage stress conditions can often be fit by the Weibull distribution of the form

$$F(t;V_i) = 1 - \exp\left\{ -\left(\frac{s}{s_0}\right)\left(t\left[\frac{V_i}{V_0}\right]^p\right)^\beta \right\} \tag{7.1}$$

where V_0, p and β are fitting parameters, V_i is the constant stress voltage and t is the time into the stress [205]. The factor s/s_0 is a scaling factor for the distribution which permits the comparison of distribution parameters between different device sizes [178]. The necessity of this distribution rescaling can be understood by considering that any device can be treated as many statistically independent units. A large device will be composed of more units and since failure of any one unit results in the failure of the entire device, larger devices will be more prone to failure. For devices with a failure mechanism related to the bulk material, the unit would be a unit of area. Therefore, the factor s/s_0 would be an area normalisation term (like in [178]). However, as seen in Figure 7.2, the failure of these devices occurs on the periphery and so the failure distributions here must be normalised by the length of the device periphery. In the following analysis, s represents the diameter of the device and s_0, the diameter of the large device.

Equation 7.1 is a cumulative distribution function (CDF) such that the value of $F(t;V_i)$ indicates the fraction of the population that will have already failed by time t during the constant voltage stress ,V_i. However, since the stress voltage was not constant during these step stress measurements, this conventional analysis cannot be directly applied. The adaptation of this Weibull analysis to step stress measurements was shown in the setting of cable dielectrics by Nelson in 1980 [205] and has not previously been applied to GaN devices. The basis of this analysis method is as follows; A suitable form for a step stress Weibull distribution can be

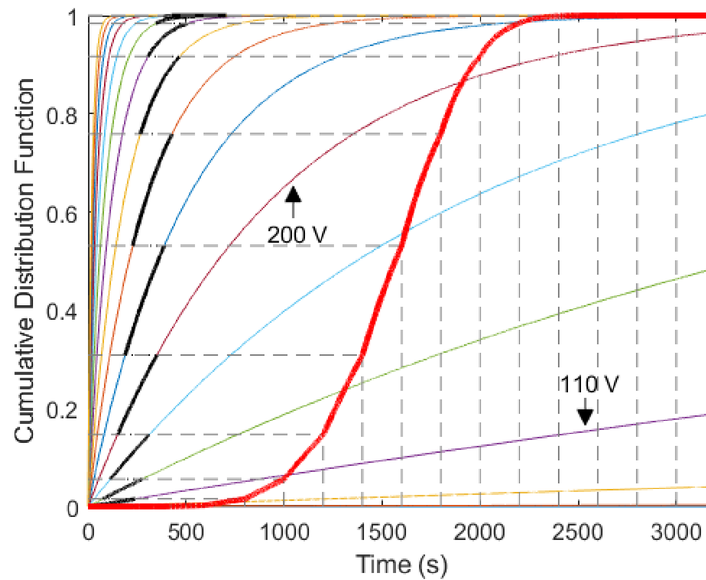

Figure 7.3: Construction of the step stress Weibull distribution with parameters $(V_0, p, \beta) = (1000, 4, 1)$ with a 30 V step every 200 s. The vertical dashed lines show the time of a step and the horizontal dashed lines show the fraction failed at that time. When the voltage steps, the step stress distribution (thick, red curve) is continued by moving laterally onto the next constant stress distribution at the same failure fraction.

constructed by using the constant stress Weibull distributions in equation 7.1 for every voltage step. This is shown instructively in Figure 7.3, for a given set of parameters (V_0, p, β). The step stress Weibull distribution is initially described by equation 7.1 where V_i now corresponds to the voltage of the ith step. Starting from $t = 0$, the step stress distribution follows the constant stress distribution of the first step voltage, $F(t; V_1)$. As the voltage steps up, the step stress distribution instead follows the constant stress distribution of the new voltage, $F(t; V_2)$. However, since the device has already experienced some cumulative stress from the previous step, the distribution is not started from $t = 0$. The value of F corresponds to the fraction failed and is a good measure of the total cumulative stress experienced by the device. Therefore, the step stress distribution is continued by moving along $F(t; V_2)$ starting from the same fraction failed that was reached by $F(t; V_1)$.

The step stress Weibull distribution can be calculated for any parameter set (V_0, p, β) in this way. In order to apply this fit to the measured failure distributions, the measurement results in Figure 7.1 were integrated into cumulative failure distributions, shown in Figure 7.4. The fitting was achieved using a least squares algorithm and the 95% confidence intervals were evaluated by varying one parameter at a time, after the fit. The result of the fitting to the small and large device distributions is shown in Figure 7.4 and fit parameters of all three distributions are shown in Table 7.1 with the 95% confidence limit in brackets. By differentiating the fits in Figure 7.4

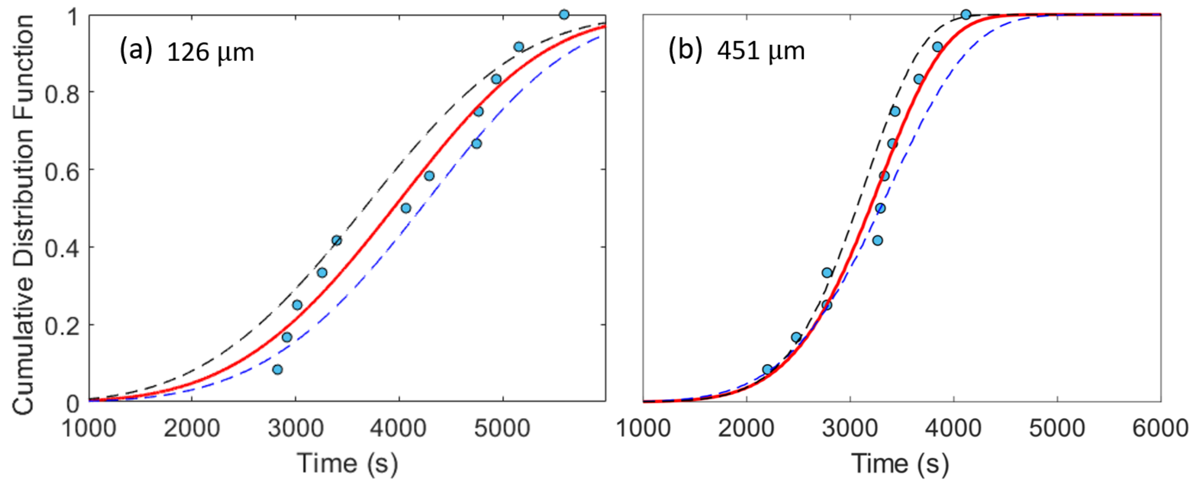

Figure 7.4: The failure time data in Figure 7.1 is integrated into cumulative failure distributions for (a) the small and (b) the large devices. These data are fit with the step stress Weibull distribution (solid line) and shown with the 95% confidence limits (dashed lines).

Table 7.1: Fit parameters of the three failure distributions with the inverse variance and the 95% confidence intervals. The average value of each parameter, weighted by the inverse variance, is included below. The values shown in this table are rounded but the exact values were used to calculate the mean.

Device size	**Fit parameters**								
	V_0			p			β		
	Value	1/Var	95%	Value	1/Var	95%	Value	1/Var	95%
Small	327	3.1e-2	13	20.9	0.29	4.1	0.176	1.5e4	0.018
Medium	312	5.5e-2	9.3	28.7	0.15	5.8	0.151	8.1e3	0.025
Large	324	9.0e-2	7.3	31.7	0.33	3.9	0.190	2.5e3	0.045
Weighted mean		320.5			26.98			0.1695	

it is possible to recover the probability distributions which are shown with the histograms in Figures 7.1(a) and 7.1(c). The probability distributions in these figures were multiplied by a factor to scale them up to the same peak amplitude as the histogram bars, allowing an easier comparison of the distribution shape.

7.5 Discussion

Analysing the V_0 parameter from each of the three parameter sets in Table 7.1, it is clear that the 95% confidence intervals all overlap. This indicates that these parameters are not statistically significantly different and the same is true for each of the β parameters. The three p parameters show more variation with a difference between the largest and the smallest value of $\Delta p = 10.8$. Here the 95% confidence intervals do not overlap but this does not guarantee that the differences

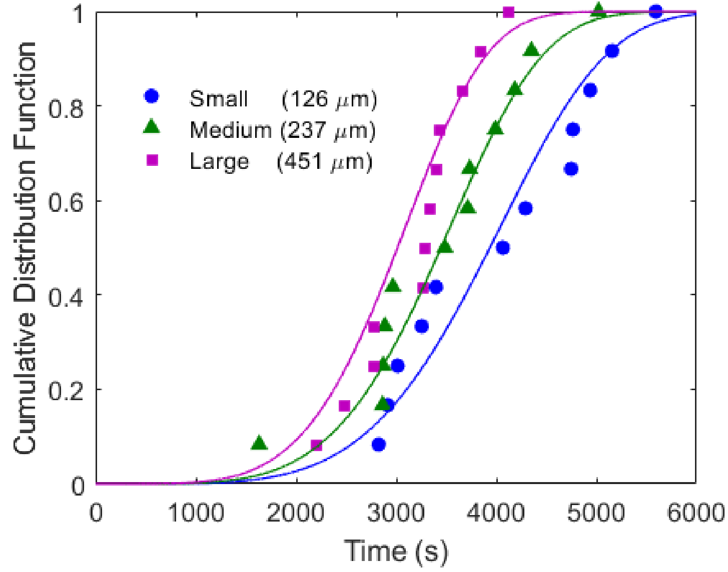

Figure 7.5: All three measured failure distributions are shown as symbols. Overlaid are the step stress Weibull distribution curves, each with the same average parameter set and differing only by the periphery scaling factor. The distribution curves represent the measurement data well, indicating that all of the device sizes can be described by the same parameters.

are statistically significant. As each fit is independent, the variance of Δp, σ^2, is the sum of the two p variances which is $\sigma^2 = 6.5$. The 95% confidence interval of the difference Δp is defined as $\Delta p \pm 1.96 \times \sigma^2$ or (-1.94, 23.54). The factor of 1.96 comes about as 95% of the area of a normal distribution is bound within 1.96 standard deviations of the mean. The inclusion of zero in the 95% confidence interval of Δp indicates that the difference between the two p parameters is not statistically significantly different from zero. Therefore all of the fit parameters, V_0, p and β do not differ significantly between the three distributions. As such, the measured distributions can all be suitably represented by the step stress Weibull distribution generated using the average parameter set. This average parameter set is shown at the bottom of Table 7.1 and was calculated using the inverse of the variance as a weighting such that the larger the uncertainty, the lower the weight. The three measured failure distributions are shown in Figure 7.5 and are plotted with the averaged step stress distributions. Each of the distribution curves in this plot differ only by the periphery scaling factor and show a good agreement with all of the data sets.

Equation 7.1 can be rearranged into the form

$$\ln[-\ln(1-F(t))] = \ln\left(\frac{s}{s_0}\right) + \beta \ln(t) + p^{\beta} \ln\left(\frac{V_i(t)}{V_0}\right) \tag{7.2}$$

where here, F is being expressed solely as a function of time, since the stress voltage $V_i(t)$ is a function of time which increases monotonically. From this equation, the data in Figure 7.5 can be replotted on ln[-ln(1-CDF)] vs. log(time) axes to recover a linear plot. This is shown in Figure

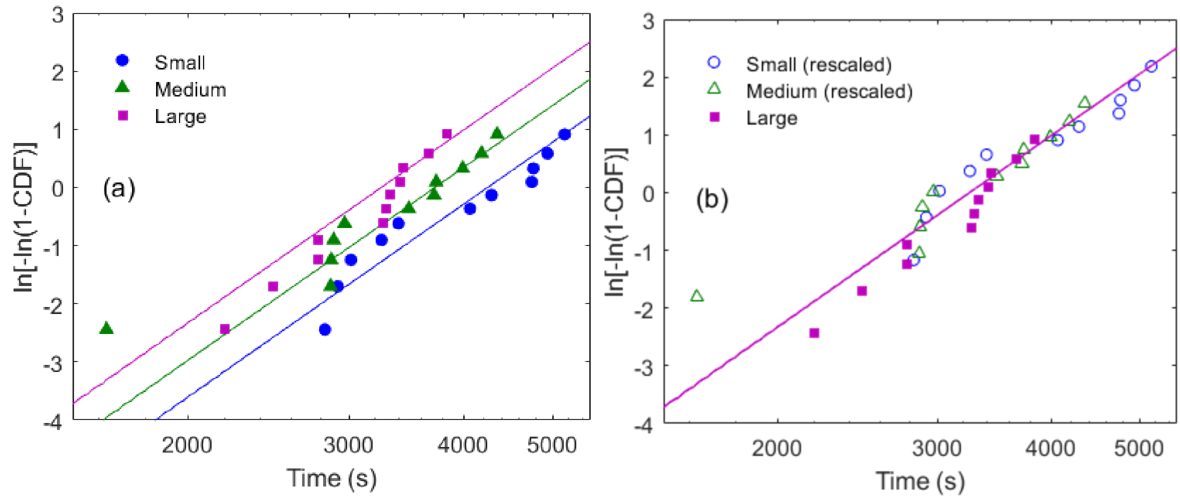

Figure 7.6: (a) The data in Figure 7.5 is replotted on ln[-ln(1-CDF)] vs. log(time) axes to force a linear fit. In (b), the failure distributions are shifted by the periphery scaling term and all align well.

7.6(a). In equation 7.2, the first term is the constant distribution rescaling, while the second and third terms are both linear in log(time). In this form it is possible to scale the measurement data by subtracting the scaling factor of $\ln(s/s_0)$, effectively shifting the data vertically along the y-axis. This has been done in Figure 7.6(b) where the rescaled measurement data all overlay to a good degree. The data and fit of the large devices are unchanged in this rescaled plot since their rescaling term is zero. This alignment of the distributions reinforces that this rescaling method is appropriate and the agreement between all of the rescaled data with the fit adds to the confidence in the average Weibull parameter set.

The mean time to failure during a constant reverse bias stress can be evaluated from the Weibull parameters using the function

$$\mathrm{MTTF}(V;s) = \left(\frac{V_0}{V}\right)^p \left(\frac{s_0}{s}\right)^{1/\beta} \Gamma\left(1+\frac{1}{\beta}\right) \tag{7.3}$$

where Γ is the gamma function, $\Gamma(z) = \int_0^\infty x^{z-1}e^{-x}dx$. Apart from the fit parameters, this function depends only on the stress voltage and the device size. As all of the devices can be well represented by the same parameter set, this indicates that the mean time to failure of these devices is determined only by the device geometry. The mean time to failure is shown as a function of stress voltage for the three device sizes in Figure 7.7(a). A mean time to failure of 10 years in constant operation places a maximum operating voltage of 260 V on the small devices, reducing to 196 V for the large devices. Using the more rigorous metric of 1% failure, enforcing the same 10 year lifetime, reduces the operating voltage of the small device to just 75 V. This enormous difference comes about from the large variability in failure times and the consequently small β parameter. The value of $\beta < 1$ seen here is indicative that the failure rate decreases over time. This means

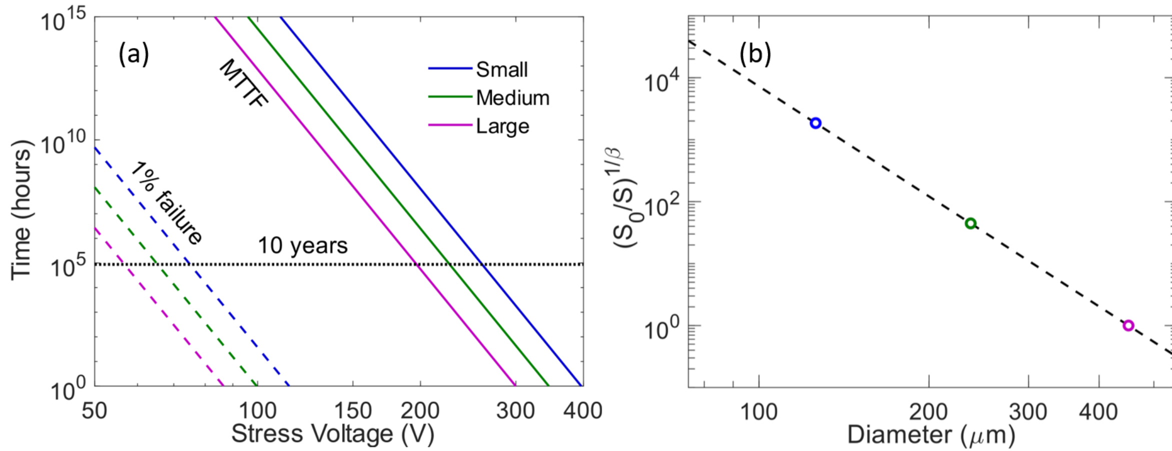

Figure 7.7: Lifetime estimations under constant stress using the average parameters set from the Weibull analysis. The mean time to failure and 1% failure times are shown in (a) indicating a mean time to failure of 10 years can be achieved on a small devices biased at 260 V. The periphery scaling factor is shown in (b) which emphasises the dependence of the mean time to failure on device size.

that the failure rate starts high and as a result, the Weibull failure distribution has a long tail at low voltages where a few percent are predicted to fail at short time scales. The dependence of the mean time to failure on device size is shown in Figure 7.7(b). This is the form of the periphery scaling factor in equation 7.3 and indicates that at any given voltage, the small device will have a mean time to failure 1000 times higher than the large device at the same voltage.

The fact that this failure data can be well represented by these statistics indicates that the failure follows the same distributions as Si and lateral GaN devices. By extension, the same failure model can be applied here in which a percolation path is constructed through the field induced generation of point defects. In order to investigate this further and establish why surface failure occurred rather than bulk failure, simulations of the devices were performed to extract the internal electric field distribution. The dopant densities used in the simulation were the nominal values of 4×10^{19} cm^{-3} and 3×10^{16} cm^{-3} in the p and n regions respectively as shown in Figure 6.2 and it was assumed that all the dopants were active. This may be an overestimation which would have the effect of increasing the field at the simulated junction but should not greatly affect the field distribution. The simulated reverse bias was increased until a peak electric field of 4 MVcm^{-1} was attained. Figure 7.8 shows the field distribution around this peak which occurred at a reverse bias of 230 V. Although the peak field is in the bulk, it is very close to the surface at the base of the bevel. Since the point defect generation rate depends on the strength of the electric field, the probability of forming a percolation path in this high field region is much higher and explains the observed surface failure [206]. This failure mechanism also completely explains the dependence of the lifetime on the length of the periphery. If point defects are created randomly, the probability of forming a percolation path (and device failure) increases with the length of the

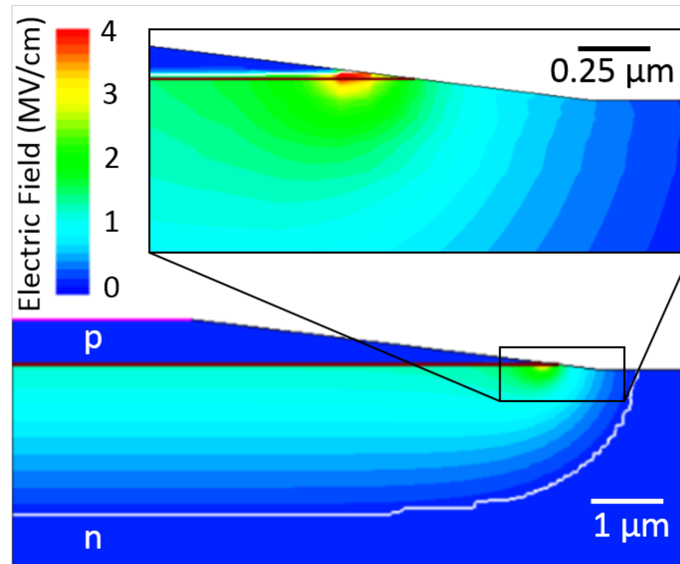

Figure 7.8: Simulations of the electric field in the device with a reverse bias of 230 V. The peak field of 4 $MVcm^{-1}$ occurs near the base of the bevel just away from the surface.

periphery where the field is high.

Of the small devices in Figure 7.1(b), two devices failed at voltages of 235 V and 465 V, with almost a factor a two difference between these extremal breakdown voltages. The surface breakdown mechanism depends strongly on the magnitude of the electric field which in turn depends strongly on the bevel topology (see section 2.5.2.1). To investigate the cause of such a large difference in failure conditions, the topology of these two extremal devices was investigated. Atomic force microscope height profiles are shown in Figure 7.9(a), very close to the location of the failures for each device. The angle of each point on the bevel to the horizontal is shown in Figure 7.9(b) and both of the devices show a peak angle of about $25-30°$. This differs wildly from the nominal $7-10°$ shown in Figure 6.2. The similarity of both of the device profiles indicates the factor of two difference in breakdown voltage may not have been caused by a difference in the electric field profile. One possible alternative cause of this difference in behaviour is a variation in surface conductivity. On these unpassivated devices, the surface is susceptible to reaction and exchange with the environment. Previous studies on GaN have shown that humidity can have a strong influence on the material properties [207]. Although the humidity in the laboratory was low and constantly regulated by air conditioning, the observed surface flashover could have be affected by variations in surface chemistry. This can be addressed in future studies by conducting the measurements with the devices submerged in a non-conductive fluid with a high breakdown field, for example, Flourinert™ which has a breakdown field 5 times higher than air [117, 208]. Eventually, commercial devices would be fabricated with a surface passivation layer which would increase the breakdown field of the device surface [209]. As the device failure is currently limited

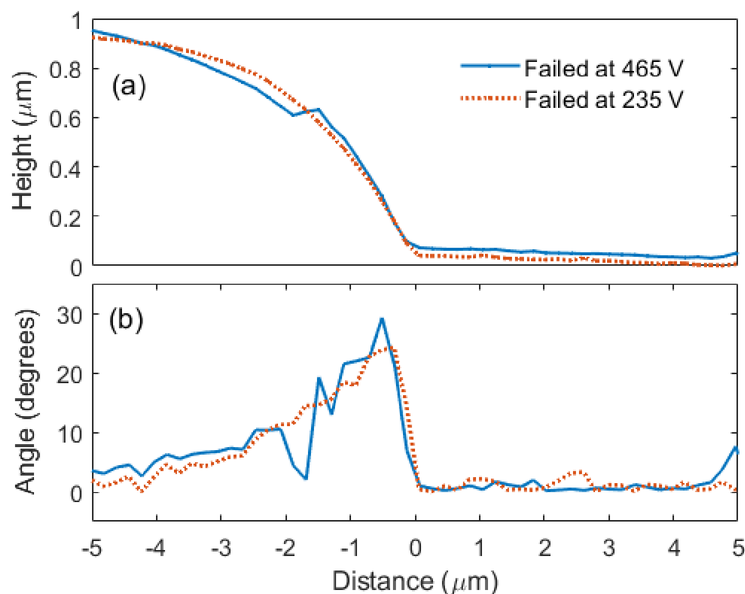

Figure 7.9: (a) Atomic force microscope height profiles, radially outwards, near the failure point of the first and last small devices to fail in Figure 7.1(b). The reverse bias at the time of failure is indicated. (b) The angle of the bevel to the horizontal is calculated from (a) and does not reveal any large differences between the two devices.

by surface failure, this would increase the device breakdown voltage and could possibly even shift the failure mechanism into the bulk material. As is, this surface failure indicates that the lifetime of these devices is currently limited by the device design or fabrication, and not by the material properties of the GaN. The noise measured in the leakage currents before failure resembled steps and is best seen in Figure 7.1(b). These apparently discrete current levels, which stepped both up and down with increasing time and voltage, are characteristic of telegraph noise [210, 211]. This is not uncommon in surface leakage currents which are sensitive to configuration changes at the surface such as those related to dangling bonds [212]. Therefore it is understood that the leakage current leading up to failure and the final breakdown mechanism are both surface related.

7.6 Conclusion

Step stress measurements have been applied to vertical GaN-on-GaN pn diodes in order to assess the reliability of the devices and identify a mean time to failure. An analysis technique not previously applied in this field was used to interpret the step stress data with Weibull statistics. The failure distributions of these vertical GaN devices were described well by a Weibull distribution, indicating the same failure model can be used with vertical GaN devices as it is for Si and lateral GaN devices. The failure mechanism was observed to be a surface related breakdown and consequently the failure rate was dependent on the length of the periphery. This indicated

that the lifetime of the devices was limited by the device design and not the material properties. This observation is important since it highlights the need to focus on design improvements over material quality issues. These results predict a mean time to failure of 10 years can be achieved with the small devices at an operating voltage of 260 V. However, a large variability was seen between devices leading to a very short 1% failure time. Benchmarking device performance is essential for commercialisation of these devices and this chapter outlines a new methodology to rapidly characterise the failure of future device generations.

Chapter 8

Conclusions

The availability of highly efficient, GaN based, power electronic systems can revolutionise the power electronics industry. GaN technology looks promising to address the increasing demand for light weight and high power density power conversion systems. One source of this demand is from the automotive industry as is evolves toward the development of hybrid and electric vehicles. The reduced size and weight of GaN systems compared to Si equivalents, as well as the increased possible power densities can enable these and other emerging technologies. Despite the very promising physical properties of GaN, a number of technical challenges must be resolved before this technology can become ubiquitous. In lateral AlGaN/GaN HEMTs, these issues include the management of current collapse for efficient switching at high frequency and the optimisation of vertical breakdown fields to enable high voltage operation. In vertical GaN diodes, which are at an earlier stage of maturity, these challenges centre around minimising vertical leakage and maximising breakdown voltage through material optimisation and device design.

The work in this thesis used electrical studies and device simulations to characterise GaN-on-Si and GaN-on-GaN devices in order to identify methods and strategies to optimise the device performance. One of the research aims in this thesis was the optimisation of the vertical breakdown and vertical leakage in GaN-on-Si HEMT epitaxies. Optimisation if these characteristics is essential as they place a limit on the maximum device operating voltage and by extension, the maximum operating efficiency. Two studies were performed with a view to furthering the understanding of factors which limit vertical leakage and breakdown.

Firstly, this work focused on the material properties of carbon doped AlGaN and the evaluation of the previously unknown carbon self-compensation ratio. This parameter sets the epitaxial resistivity and so strongly influences the vertical breakdown and leakage. This was performed through

the use of substrate bias and lateral leakage measurements. These techniques were applied to two nominally identical samples differing only by the carbon doping in the $Al_{0.08}Ga_{0.92}N$ back-barrier, above an AlN interlayer. The presence of a 2DHG was identified at the back-barrier/interlayer interface in the undoped sample but this hole gas was suppressed in the carbon doped sample. As only donors can suppress a 2DHG, this indicated that carbon must partially incorporate as donors as well as the more abundant acceptor trap. Through simulation of the device layers and interface charges, the minimum required donor density to neutralise the polarisation charge was determined. In conjunction with secondary-ion mass spectroscopy measurements of the total carbon density, this allowed the determination of the self-compensation ratio of carbon in $Al_{0.08}Ga_{0.92}N$ to be $0.4 < N_D/N_A < 1$. The upper constraint is unity since if the compensation ratio exceeded this value, carbon doped GaN would not be highly resistive. In carbon doped GaN and AlGaN, it is the compensation ratio which determines the material resistivity and therefore this parameter also impacts heavily on the vertical leakage and breakdown voltage. In addition, this ratio also determines the depletion behaviour under the gate in a HEMT in the off-state. Therefore, a good estimation of this previously unknown parameter is critical for accurate device simulation and device design. Already, the ratio presented here has been applied in multiple simulation works [213–215], highlighting the importance of this result to the GaN device community.

Continuing on the theme of vertical leakage and breakdown optimisation, the impact of device processing on the vertical resistivity of the wafer was investigated. It was identified that the presence of Ti/Al based contacts on the surface of an AlGaN/GaN HEMT epitaxy can have the effect of reducing the vertical breakdown voltage. This was found through measurements of vertical leakage and characterised by a novel application of the quasi-static capacitance-voltage technique. Bespoke structures were fabricated in order to study this effect, allowing the separation of vertical leakage in active areas with and without an Ohmic contact. Results indicated the region under the contact has a reduced resistivity and a higher capacitance. This is a significant result since the contact should have no effect on the properties of the bulk material below it. The capacitance data was used to infer that the resistivity of the effected region was reduced by at least a factor of 100 and extended $\sim 1.6\ \mu$m down from the surface. This extension accounted for half the thickness of the epitaxy and stopped at the top of the superlattice strain relief layers. Maximising the operating and breakdown voltage is essential for exploiting the full potential of GaN devices. Ti/Al based contacts such as these are standard for GaN-on-Si processes so identifying and understanding limitations such as these is a high priority. Through further study of this effect, it may be possible to reduce buffer leakage, increase breakdown voltage and even manage current collapse. The discovery of these preferential sub-contact leakage paths is a step forward in the understanding of these devices. The dissemination of this research will raise awareness of the existence of such features which are not widely considered. As these paths are required in some simulations to recover the measured device behaviour, the inclusion of these

paths in all future device simulations will enable improved simulation accuracy.

In many GaN power electronic circuit designs, high power diodes are required along with HEMTs. In order for these circuits to exploit the maximum efficiencies offered by GaN, these diodes must be capable of operating at the same high voltages as the HEMTs with matched, low off-state leakage. Vertical GaN diodes are most suited to this application over lateral devices since with thicker epitaxies they can operate at higher voltages, with improved thermal performance, and they have a low dislocation density leading to low reverse leakage. Targeting this application space, the reverse biased leakage of bulk GaN diodes was evaluated and characterised. In reverse bias, in the time domain, the devices exhibited previously unreported current and capacitance features which could not be explained by any existing models. The observed peak in leakage current after a few seconds of the stress was explained by a new model, attributing this behaviour to a peak in the conductivity of the dislocation cores. In this model, the cause of the change in conductivity was attributed to the Fermi level moving through a defect band, as surrounding defect clusters discharged. These data constitute the first direct evidence for impurity band conduction in dislocation cores which has only previously been speculated. Study of the image current identified that the three order of magnitude change in leakage current was caused by a discharging of only 10^{12} cm^{-2} carriers. This demonstrates the extent to which charged point defect clusters can affect dislocation leakage. The efficiency of power diodes hinges on the suppression of the off-state leakage thus a full understanding of these reverse leakage mechanisms is critical for the development of GaN-on-GaN vertical power diodes. The generation rate of point defects in GaN such as V_N and V_{Ga} depends on the growth temperature [172, 173, 216]. Therefore, based on this new model, it may be possible to reduce the conductivity of dislocations in GaN by tuning the growth conditions. This work has not only furthered the current understanding of leakage processes in bulk GaN, but has also supported the investigation of impurity band conduction and conduction/charging mechanisms in GaN:C [213].

Finally, the reliability of these vertical GaN diodes was evaluated and the first estimations of their lifetime were made. Establishing the reliability of these devices is essential before they can be commercially traded and no prior lifetime estimations exist on vertical GaN diodes. This work was achieved using a step stress measurement technique, where the reverse bias of the device was gradually stepped up until failure. In order to analyse this data, methods from the field of cable dielectrics were transferred to GaN for the first time and allowed the analysis of step stress data with Weibull statistics. The Weibull distribution accurately described the failures, indicating that vertical GaN devices can be modelled by the same failure models used with Si and lateral GaN devices. Namely, the field induced generation of point defects and the subsequent formation of a percolation path leading to failure. Using Weibull statistics, it was shown that the device failure rates depended only of the device geometry, specifically the length of the periphery. Optical inspection showed the failure occurred by surface breakdown, confirming that the failure rate should be depended on the length of the device periphery. The Weibull fit parameters were

used to estimate the mean time to failure. The smallest device was predicted to have a mean time to failure of 10 years when continuously stressed at a voltage of 260 V. These current results indicate these devices are limited by device design and further optimisation of the electric field around the device periphery is required, either by optimisation of the edge termination or the application of a passivation layer. These measurements provided a much needed evaluation of the current state of reliability of this technology and present a new methodology for future lifetime evaluations. This analysis will enable more rapid characterisation and reliability assessments of GaN devices in the future.

8.1 Future work

Electrical measurements comparing the charge storage and leakage behaviour of different strain relief layer designs has indicated superlattice strain relief layers give rise to superior performance[160]. Following on from that work, a new study modelling an optimised superlattice strain relief layers is set to begin between imec and the Centre for Device Thermography and Reliability (CDTR). The aim of this new project is to understand the physical processes which give rise to the improved behaviour in the superlattice strain relief layers when compared to the interlayer strain relief layers featured in Chapter 4. The simulation work in Chapter 4 identified that in the simulation of strain relief layers, it is imperative to construct the model with realistic composition profiles in order to recover realistic results. Initial simulations with ideal, abrupt interfaces yielded unrealistic, non-physical results, thus realistic profiles must be used in all future simulations of the strain relief layers and buffer structure of metal-organic chemical vapour deposition grown devices. Based on this assertion, this new study will rely heavily on scanning transmission electron microscopy cross-sections to ensure realistic composition profiles are implemented throughout the superlattice.

The results presented in Chapter 5 provide compelling evidence to support the presence of preferential leakage paths below the Ohmic contacts. However, further work could be done to verify the physical cause of this behaviour. It was suggested that the preferential leakage is caused by the contact metals decorating existing dislocations under the contact. Future studies could investigate this effect on structures processed with a different metal stack, i.e. Ta/Al/Ta, to identify whether the effect is Ti/Al specific. Alternatively, the same Ti/Al contact structures could be fabricated on low defect density material to verify if the dislocation density does indeed play a role. Additionally, to support the electrical measurements, a more direct measurement approach could also be taken. By mechanically polishing a sample, the dislocation decoration under the contact could be directly observed with kelvin probe mapping. Using this technique, it would even be possible to inspect the dislocation cross-section as a function of depth by polishing the sample at an angle. This could be used to directly measure the extension of the leakage paths.

Finally, the results in Chapter 6 were explained by a mechanism which modulates the conductivity of dislocations using the charge state of point defects. This opens an avenue for the exploration of the positive benefits of point defects and engineering of the point defect density to reduce the reverse leakage in GaN diodes. There have been results in the literature which demonstrate the ability to control the point defect density in metal-organic chemical vapour deposition by tuning of the growth parameters. Generally, the goal is to reduce the point defect density, however a new study could be devised in which the point defect density is intentionally varied with as many other parameters kept constant to assess the impact on the reverse leakage along dislocations. This study would be a method of testing this impurity band conduction model of leakage. With different defect densities, the distance the Fermi level moves during the transient would differ i.e. a low point defect density would result in the Fermi level only moving by a small amount. Depending on the width of the impurity band, the shape and magnitude of the transient would be expected to change with defect density. If successful, new growth regimes could be developed to create even lower leakage devices, possibly even approaching the limits of the ideal material despite a non-zero dislocation density.

RESEARCH OUTPUT

A.1 Publications

- **B. Rackauskas**, M. J. Uren, S. Stoffels, M. Zhao, S. Decoutere, and M. Kuball, "Determination of the Self-Compensation Ratio of Carbon in AlGaN for HEMTs", IEEE Trans. Electron Devices, vol. **65**, no. 5, pp. 1838–1842, May 2018, doi:10.1109/TED.2018.2813542.

- **B. Rackauskas**, S. Dalcanale, M. J. Uren, T. Kachi, and M. Kuball, "Leakage mechanisms in GaN-on-GaN vertical pn diodes", Appl. Phys. Lett., vol. **112**, no. 23, p. 233501, Jun. 2018, doi:10.1063/1.5033436.

- **B. Rackauskas**, M. J. Uren, S. Stoffels, M. Zhao, B. Bakeroot, S. Decoutere, and M. Kuball, "The impact of Ti/Al contacts on AlGaN/GaN HEMT vertical leakage and breakdown", IEEE Electron Device Lett., vol. **39**, no. 10, pp. 1580–1583, Oct. 2018, doi:10.1109/LED.2018.2866613.

- **B. Rackauskas**, M. J. Uren, T. Kachi, and M. Kuball, "Reliability and lifetime estimations of GaN-on-GaN vertical pn diodes", Microelec. Rel., vol. **95**, 48-51, Mar. 2019, doi:10.1016/j.microrel.2019.02.013.

A.2 Conference talks

- **B. Rackauskas**, M. J. Uren, S. Stoffels, M. Kuball, "Processes behind Suppressed Current Collapse Buffer Architectures", International Workshop on III-Nitrides 2016, Orlando, USA

- **B. Rackauskas**, M. J. Uren, S. Stoffels, M. Zhao, S. Decoutere, M. Kuball, "Self-compensation of Carbon in AlGaN", UK Nitrides Consortium Winter Meeting 2018, Manchester, UK

- **B. Rackauskas**, M. J. Uren, S. Stoffels, M. Zhao, S. Decoutere, M. Kuball, "Self-compensation of Carbon in AlGaN", International Symposium of Growth of III-Nitrides 2018, Warsaw, Poland
- **B. Rackauskas**, S. Dalcanale, M. J. Uren, T. Kachi, M. Kuball, "Impurity band conduction along dislocations in vertical GaN-on-GaN pn diodes", International Workshop on III-Nitrides 2018, Kanazawa, Japan (**talk given by M. Kuball**)

APPENDIX B

List of Abbreviations

2DEG 2-Dimensional Electron Gas

2DHG 2-Dimensional Hole Gas

AC Alternating Current

AFM Atomic Force Microscope

BFOM Baliga Figure Of Merit

CAFM Conductive Atomic Force Microscope

CAVET Current Aperture Vertical Electron Transistor

CDF Cumulative Distribution Function

CDTR Centre for Device Thermography and Reliability

CL Cathodo-Luminescence

CMOS Complementary Metal-Oxide-Semiconductor

CMU Capacitance Measurement Unit

CPU Central Processing Unit

CTE Coefficient of Thermal Expansion

CV Capacitance-Voltage

DC Direct Current

DOS Density Of States

DFT Density Functional Theory

FET Field Effect Transistor

FIB Focused Ion Beam

GPIB General Purpose Interface Bus

HAADF High Angle Annular Dark Field

HEMT High Electron Mobility Transistor

HFET Hetero-structure Field Effect Transistor

HV High Voltage

HVPE Hydride Vapour Phase Epitaxy

IB Impurity Band

imec Inter-university Micro-Electronics Centre

IP Intellectual Property

IV Current-Voltage

JTE Junction Termination Extension

LED Light Emitting Diode

LiDAR Light Detection And Ranging

MBE Molecular Beam Epitaxy

MOCVD Metal-Organic Chemical Vapour Deposition

MODFET MOdulation-Doped Field Effect Transistor

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor

MTTF Mean Time To Failure

PID Proportional Integral Derivative

PWM Pulse Width Modulation

QSCV Quasi-Static Capacitance-Voltage

RF Radio Frequency

SBD Schottky Barrier Diode

SEM Scanning Electron Microscopy

SIMS Secondary-Ion Mass Spectroscopy

SMU Source Measurement Unit

SRL Strain Relief Layers

STEM Scanning Transmission Electron Microscopy

TAT Trap Assisted Tunnelling

TCAD Technology Computer-Aided Design

TDDB Time Dependant Dielectric Breakdown

TEM Transmission Electron Microscopy

TLM Transfer Length Method

UID UnIntentionally Doped

UV Ultra Violet

VRH Variable Range Hopping

Appendix C

ATLAS simulation code

This appendix contains the code required to run the SILVACO ATLAS simulation presented in chapter 4 for the structure with a carbon doped back-barrier. For simulation of the unintentionally doped back-barrier structure, the carbon trap statements in the back-barrier can be commented out (lines starting with # are comments). This appendix comprises three files; the run file, the design file and the body file. The design file specifies the physical layout of the structure and defines the finite element mesh. This is created and edited in Devedit and compiled into a structure file (.str) before running the model. The body file calls the design structure file and specifies the material property definitions of each material layer (Al composition of AlGaN, trap density/levels, carrier mobilities etc.). The body file also defines which physical models to turn on and specifies the desired simulation outputs. Finally, the run file is the most high level file and is executed in Deckbuild to run the simulation. The run file calls the body file and defines the design of experiment e.g. which contacts are set to which voltage at which time. These three files described above are presented in the following sections.

C.1 Run File (U_runfile_5Vps_C_350V.in)

```
go atlas  simflags= "-V 5.20.2.R -P 4"
set fstub1="U"
set fstub2="15745_"
set fstub3="C_1.47e19_5.3e18_doped_ILs_v4"

set TL=293
source bodytext_U_C_v4.in


method newton autonr carriers=2 maxtraps=10 itlimit = 50
solve init
#regrid potential ratio=0.2 outf="new_grid.str" smooth=4


set time=0
solve vdrain=1
solve vsubstrate=0
save outf=$'fstub1'$'fstub2'$'fstub3'_Init_Vd=1_TL=$'TL'_rate=5.str master


log outf = $'fstub1'$'fstub2'$'fstub3'_IdVsub_Vd=1_TL=$'TL'_rate=5.log

# ramp up
solve vsubstrate=-115 ramptime=23 dt=1 tstop=23
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=-115f_Vd=1_TL=$'TL'_rate=5.str master

solve vsubstrate=-235 ramptime=24 dt=1 tstop=47
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=-235f_Vd=1_TL=$'TL'_rate=5.str master

solve vsubstrate=-355 ramptime=24 dt=1 tstop=71
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=-355f_Vd=1_TL=$'TL'_rate=5.str master
```

```
# ramp down

solve vsubstrate=-235 ramptime=24 dt=1 tstop=95
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=-235b_Vd=1_TL=$'TL'_rate=5.str master

solve vsubstrate=-115 ramptime=24 dt=1 tstop=119
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=-115b_Vd=1_TL=$'TL'_rate=5.str master

solve vsubstrate=0 ramptime=23 dt=1 tstop=142
save outf=$'fstub1'$'fstub2'$'fstub3'_Vsub=0b_Vd=1_TL=$'TL'_rate=5.str master


log off
```

C.2 Design File (U15745_4.de)

```
DevEdit version=2.8.21.R # file written Thu Jun 22 2017 11:37:32 GMT+1 (BST)

work.area x1=-5.5 y1=-0.5 x2=26.65 y2=5.22
# devedit 2.8.21.R (Fri Dec 19 15:47:22 PST 2014)
# libMeshBuild 1.24.19 (Tue Dec  9 04:44:54 PST 2014)
# libSSS 2.8.11 (Tue Dec  9 04:41:32 PST 2014)
# libSVC_Misc 1.28.12 (Fri Nov 14 19:53:38 PST 2014)
# libsflm 7.8.18 (Tue Dec  2 21:07:40 PST 2014)
# libSDB 1.12.31 (Wed Dec  3 01:58:14 PST 2014)
# libGeometry 1.30.13 (Fri Nov 14 19:52:25 PST 2014)
# libCardDeck 1.32.19 (Fri Nov 14 19:52:23 PST 2014)
# libDW_Set 1.28.12 (Fri Nov 14 19:53:36 PST 2014)
# libSvcFile 1.14.16 (Wed Dec  3 18:05:53 PST 2014)
# libsstl 1.10.8 (Fri Nov 14 19:52:31 PST 2014)
# libDW_Misc 1.40.16 (Tue Dec  2 09:09:46 PST 2014)
# libQSilCore 1.2.7 (Thu Nov 13 17:55:06 PST 2014)
# libDW_Version 3.8.0 (Fri Oct  3 16:08:41 PDT 2014)
region reg=1 name=Cap mat=Si3N4 color=0xffff pattern=0x3 \
polygon="20.5,-0.015 0.5,-0.015 0.5,-0.02 20.5,-0.02"
#
constr.mesh region=1 default

region reg=2 name=Barrier mat="UD4(Al0.25GaN)" color=0xcb00ff pattern=0x6 \
polygon="20.5,0 0.5,0 0.5,-0.015 20.5,-0.015"
#
constr.mesh region=2 default

region reg=3 name=UID mat=GaN color=0xcca3a3 pattern=0xd \
polygon="-5.5,0 0.5,0 20.5,0 26.5,0 26.5,0.5 -5.5,0.5"
#
constr.mesh region=3 default

region reg=4 name=Buffer mat="UD2(Al0.08GaN)" color=0x7a3d99 pattern=0x4 \
```

```
polygon="-5.5,1.292 -5.5,0.5 26.5,0.5 26.5,1.292"
#
constr.mesh region=4 default

region reg=5 name="Interlayer 1.0" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,1.308 26.5,1.308 26.5,1.31 -5.5,1.31"
#
constr.mesh region=5 default

region reg=6 name=Al0.08GaN:C mat="UD2(Al0.08GaN)" color=0x7a3d99 pattern=0x4 \
polygon="26.5,2.32 26.5,4.12 -5.5,4.12 -5.5,2.32" \
polygon="-5.5,2.302 -5.5,1.31 26.5,1.31 26.5,2.302"
#
constr.mesh region=6 default

region reg=7 name=substrate mat=Silicon elec.id=3 work.func=0 color=0xffcc00 pattern=0x4 \
polygon="26.5,4.22 -5.5,4.22 -5.5,4.12 26.5,4.12"
#
constr.mesh region=7 default

region reg=8 name=source mat=GaN elec.id=1 work.func=0 color=0xcca3a3 pattern=0xd \
polygon="-5.5,0 -5.5,-0.05 0.5,-0.05 0.5,-0.02 0.5,-0.015 0.5,0"
#
constr.mesh region=8 default

region reg=9 name=drain mat=GaN elec.id=2 work.func=0 color=0xcca3a3 pattern=0xd \
polygon="20.5,-0.05 26.5,-0.05 26.5,0 20.5,0 20.5,-0.015 20.5,-0.02"
#
constr.mesh region=9 default

region reg=10 name="Interlayer 2.0" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.318 26.5,2.318 26.5,2.32 -5.5,2.32"
#
constr.mesh region=10 default

region reg=11 name="Interlayer 1.1" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,1.306 26.5,1.306 26.5,1.308 -5.5,1.308"
#
```

```
constr.mesh region=11 default

region reg=12 name="Interlayer 1.2" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,1.306 -5.5,1.306 -5.5,1.304 26.5,1.304"
#
constr.mesh region=12 default

region reg=13 name="Interlayer 1.3" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,1.304 -5.5,1.304 -5.5,1.302 26.5,1.302"
#
constr.mesh region=13 default

region reg=14 name="Interlayer 1.4" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,1.302 -5.5,1.3 26.5,1.3 26.5,1.302"
#
constr.mesh region=14 default

region reg=15 name="Interlayer 1.5" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,1.3 -5.5,1.298 26.5,1.298 26.5,1.3"
#
constr.mesh region=15 default

region reg=16 name="Interlayer 1.6" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,1.298 -5.5,1.298 -5.5,1.296 26.5,1.296"
#
constr.mesh region=16 default

region reg=17 name="Interlayer 1.7" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,1.296 -5.5,1.296 -5.5,1.294 26.5,1.294"
#
constr.mesh region=17 default

region reg=18 name="Interlayer 1.8" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,1.294 -5.5,1.294 -5.5,1.292 26.5,1.292"
#
constr.mesh region=18 default

region reg=19 name="Interlayer 2.1" mat=AlGaN color=0xff8286 pattern=0x4 \
```

```
polygon="-5.5,2.316 26.5,2.316 26.5,2.318 -5.5,2.318"
#
constr.mesh region=19 default

region reg=20 name="Interlayer 2.2" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.314 26.5,2.314 26.5,2.316 -5.5,2.316"
#
constr.mesh region=20 default

region reg=21 name="Interlayer 2.3" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.312 26.5,2.312 26.5,2.314 -5.5,2.314"
#
constr.mesh region=21 default

region reg=22 name="Interlayer 2.4" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.31 26.5,2.31 26.5,2.312 -5.5,2.312"
#
constr.mesh region=22 default

region reg=23 name="Interlayer 2.5" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.308 26.5,2.308 26.5,2.31 -5.5,2.31"
#
constr.mesh region=23 default

region reg=24 name="Interlayer 2.6" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="-5.5,2.306 26.5,2.306 26.5,2.308 -5.5,2.308"
#
constr.mesh region=24 default

region reg=25 name="Interlayer 2.7" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,2.306 -5.5,2.306 -5.5,2.304 26.5,2.304"
#
constr.mesh region=25 default

region reg=26 name="Interlayer 2.8" mat=AlGaN color=0xff8286 pattern=0x4 \
polygon="26.5,2.304 -5.5,2.304 -5.5,2.302 26.5,2.302"
#
constr.mesh region=26 default
```

```
impurity id=1 imp=Donors color=0x8c5d00 \
peak.value=1e+20 ref.value=1000000000000 comb.func=Multiply \
y1=-0.4 y2=0 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.01 \
x1=-5.5 x2=0.5 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.01
impurity id=2 imp=Donors color=0x8c5d00 \
peak.value=1e+20 ref.value=1000000000000 comb.func=Multiply \
y1=-0.4 y2=0 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.01 \
x1=20.5 x2=26.5 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.01

# Set Meshing Parameters
#
base.mesh height=0.5 width=0.5
#
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 line.straightening=1 \
align.points when=automatic
#
imp.refine min.spacing=0.1
#
constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
max.width=10000 min.height=0.0001 min.width=0.0001
#
constr.mesh type=Semiconductor default
#
constr.mesh type=Insulator default
#
constr.mesh type=Metal default
#
constr.mesh type=Other default
#
constr.mesh region=1 default
#
constr.mesh region=2 default
#
constr.mesh region=3 default
#
constr.mesh region=4 default
#
```

```
constr.mesh region=5 default
#
constr.mesh region=6 default
#
constr.mesh region=7 default
#
constr.mesh region=8 default
#
constr.mesh region=9 default
#
constr.mesh region=10 default
#
constr.mesh region=11 default
#
constr.mesh region=12 default
#
constr.mesh region=13 default
#
constr.mesh region=14 default
#
constr.mesh region=15 default
#
constr.mesh region=16 default
#
constr.mesh region=17 default
#
constr.mesh region=18 default
#
constr.mesh region=19 default
#
constr.mesh region=20 default
#
constr.mesh region=21 default
#
constr.mesh region=22 default
#
constr.mesh region=23 default
#
```

```
constr.mesh region=24 default
#
constr.mesh region=25 default
#
constr.mesh region=26 default
Mesh Mode=MeshBuild
refine mode=y x1=-5.55 y1=0.009 x2=26.65 y2=0.02
refine mode=y x1=-5.5 y1=0.012 x2=27.31 y2=0.013
refine mode=y x1=-5.44 y1=0.01 x2=26.65 y2=0.017
refine mode=y x1=-5.61 y1=0.01 x2=26.77 y2=0.026
refine mode=y x1=-5.61 y1=0.013 x2=27.07 y2=0.017
refine mode=y x1=-5.61 y1=0.006 x2=26.71 y2=0.01
refine mode=y x1=-5.61 y1=-0.015 x2=25.04 y2=-0.011
refine mode=y x1=-5.55 y1=-0.003 x2=26.77 y2=0.002
refine mode=y x1=-5.61 y1=-0.003 x2=26.65 y2=0
refine mode=y x1=-0.26 y1=-0.0011 x2=21.37 y2=0.0004
refine mode=y x1=-5.67 y1=1.2325 x2=26.83 y2=1.2692
refine mode=y x1=-5.5 y1=1.3403 x2=27.13 y2=1.3741
refine mode=y x1=-5.55 y1=1.2052 x2=27.73 y2=1.2505
refine mode=y x1=-5.79 y1=1.3554 x2=27.19 y2=1.3713
refine mode=y x1=-5.85 y1=1.249 x2=26.83 y2=1.2656
refine mode=y x1=-5.61 y1=1.3511 x2=26.65 y2=1.3554
refine mode=y x1=-5.55 y1=1.2656 x2=26.71 y2=1.2742
refine mode=y x1=-5.91 y1=1.326 x2=27.19 y2=1.3353
refine mode=y x1=-6.03 y1=1.28 x2=26.83 y2=1.2828
refine mode=y x1=-5.79 y1=1.3202 x2=26.89 y2=1.3238
refine mode=y x1=-5.73 y1=1.2843 x2=27.25 y2=1.2871
refine mode=y x1=-5.85 y1=1.3137 x2=27.13 y2=1.3166
refine mode=y x1=-5.85 y1=1.2879 x2=26.89 y2=1.2886
refine mode=y x1=-5.91 y1=1.3123 x2=27.61 y2=1.313
refine mode=y x1=-6.03 y1=2.2727 x2=26.83 y2=2.2806
refine mode=y x1=-6.27 y1=2.3719 x2=26.12 y2=2.3762
refine mode=y x1=-6.57 y1=2.2447 x2=27.61 y2=2.2706
refine mode=y x1=-6.15 y1=2.3604 x2=25.04 y2=2.3604
refine mode=y x1=-6.09 y1=2.2749 x2=27.25 y2=2.2871
refine mode=y x1=-6.03 y1=2.3475 x2=27.31 y2=2.3733
refine mode=y x1=-6.15 y1=2.3417 x2=27.19 y2=2.3518
refine mode=y x1=26.06 y1=2.346 x2=26.6 y2=2.346
```

```
refine mode=y x1=-5.97 y1=2.2864 x2=27.31 y2=2.29
refine mode=y x1=-5.85 y1=2.3338 x2=26.89 y2=2.3352
refine mode=y x1=-5.85 y1=2.2928 x2=26.95 y2=2.2964
refine mode=y x1=-6.03 y1=2.3273 x2=27.07 y2=2.3281
refine mode=y x1=-6.09 y1=2.2979 x2=27.25 y2=2.2993
refine mode=y x1=-6.03 y1=2.3223 x2=27.01 y2=2.3252
refine mode=both x1=-3.76 y1=0.05 x2=-0.46 y2=1.12
refine mode=both x1=21.62 y1=0.05 x2=24.56 y2=1.14
refine mode=y x1=-5.5 y1=0.43 x2=26.77 y2=0.59
refine mode=y x1=0.08 y1=0.4 x2=21.02 y2=0.6
refine mode=y x1=-5.32 y1=0.38 x2=-4.24 y2=0.57
refine mode=y x1=25.04 y1=0.6 x2=26.36 y2=0.79
refine mode=y x1=-5.32 y1=0.42 x2=-14.01 y2=0.47
refine mode=y x1=-5.44 y1=0.45 x2=26.24 y2=0.53
refine mode=y x1=-5.38 y1=0.47 x2=26.6 y2=0.52
refine mode=y x1=-5.44 y1=1.2879 x2=27.07 y2=1.313
refine mode=y x1=-5.55 y1=2.2986 x2=26.71 y2=2.323
refine mode=y x1=-5.55 y1=1.2871 x2=26.95 y2=1.3073
refine mode=y x1=-5.5 y1=2.2964 x2=26.89 y2=2.3144


base.mesh height=0.5 width=0.5

bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 \
line.straightening=1 align.Points when=automatic
```

C.3 Body File (bodytext_U_C_v4.in)

```
# IMEC 15745 IL device (C doped deep buffer) TLM

#

#-----------------------------------------------------------------
# Layers
#---------------------------------------------------------------------------
# 1. SiN Cap
# 2. Al0.25GaN Barrier
# 3. UID GaN
# 4. Al0.08GaN Buffer
# 5. Interlayer 1.0
# 6. Al0.08GaN:C
# 7. Substrate
# 8. Source
# 9. Drain
# 10. Interlayer 2.0

# 11. Interlayer 1.1
# 12. Interlayer 1.2
# 13. Interlayer 1.3
# 14. Interlayer 1.4
# 15. Interlayer 1.5
# 16. Interlayer 1.6
# 17. Interlayer 1.7
# 18. Interlayer 1.8

# 19. Interlayer 2.1
# 20. Interlayer 2.2
# 21. Interlayer 2.3
# 22. Interlayer 2.4
# 23. Interlayer 2.5
# 24. Interlayer 2.6
```

```
# 25. Interlayer 2.7
# 26. Interlayer 2.8


set Lsd=20
set Lcontact=1
set t_barrier=0.015
set t_SiNcap=0.005
set RC=500

set Spike_depth = 0.05

set density_UID_donor = 1e16
set e_UID_donor = 0.02

# Polarisation charges (Ambacher 2002 - non-linear interpolations of material properties)

set Qp_GaN = 2.12e13
set Qp_Al0.08GaN = 2.44e13
set Qp_Al0.25GaN = 3.24e13
# relaxed ILs
set Qp_AlN = 5.625e13

set Qoffset=5.0e12

# Band Gaps  (from ATLAS)

set Eg_GaN = 3.42
set Eg_Al0.08GaN = 3.56
set Eg_Al0.13GaN = 3.64
set Eg_Al0.21GaN = 3.79
set Eg_Al0.25GaN = 3.87
set Eg_Al0.31GaN = 4.00
set Eg_Al0.41GaN = 4.23
set Eg_Al0.44GaN = 4.37
set Eg_Al0.54GaN = 4.55
set Eg_Al0.75GaN = 5.27
set Eg_Al0.78GaN = 5.32
```

```
set Eg_Al0.80GaN = 5.39
set Eg_Al0.90GaN = 5.75
set Eg_AlN = 6.13

# Trap properties
set e_level_deep_acceptor=0.98
set deep_acceptor_sign=1e-15
set deep_acceptor_sigp=1e-13

set density_deep_acceptor=1.47e19
#1e19
set density_compensating_donor=.53e19
#5e17

set e_compensating_donor=0.02
set ymin_C=0.5
set ymax_C=1.3

# Note that the location of the traps is set on the TRAP statement

#-----------------------------------------------------------------
# Get structure file from DevEdit
#-----------------------------------------------------------------

mesh inf=U15745_4.str  width=22


REGION MODIFY NUM=2 MATERIAL=AlGaN X.COMP=0.25
REGION MODIFY NUM=4 MATERIAL=AlGaN X.COMP=0.08

REGION MODIFY NUM=5 MATERIAL=AlGaN X.COMP=0.54
REGION MODIFY NUM=11 MATERIAL=AlGaN X.COMP=0.80
REGION MODIFY NUM=12 MATERIAL=AlGaN X.COMP=0.90
REGION MODIFY NUM=13 MATERIAL=AlGaN X.COMP=0.78
REGION MODIFY NUM=14 MATERIAL=AlGaN X.COMP=0.53
REGION MODIFY NUM=15 MATERIAL=AlGaN X.COMP=0.41
REGION MODIFY NUM=16 MATERIAL=AlGaN X.COMP=0.31
REGION MODIFY NUM=17 MATERIAL=AlGaN X.COMP=0.21
```

```
REGION MODIFY NUM=18 MATERIAL=AlGaN X.COMP=0.13

REGION MODIFY NUM=6 MATERIAL=AlGaN X.COMP=0.08

REGION MODIFY NUM=10 MATERIAL=AlGaN X.COMP=0.54
REGION MODIFY NUM=19 MATERIAL=AlGaN X.COMP=0.80
REGION MODIFY NUM=20 MATERIAL=AlGaN X.COMP=0.90
REGION MODIFY NUM=21 MATERIAL=AlGaN X.COMP=0.78
REGION MODIFY NUM=22 MATERIAL=AlGaN X.COMP=0.53
REGION MODIFY NUM=23 MATERIAL=AlGaN X.COMP=0.41
REGION MODIFY NUM=24 MATERIAL=AlGaN X.COMP=0.31
REGION MODIFY NUM=25 MATERIAL=AlGaN X.COMP=0.21
REGION MODIFY NUM=26 MATERIAL=AlGaN X.COMP=0.13

#------------------------------------------------------------------
# ... trap definitions
#------------------------------------------------------------------

### Spikes ###
doping acceptor conc=1.1e20 gaussian characteristic=0.005 \
x.min=-1 x.max=-1 y.min=0 y.max=$'Spike_depth'
doping acceptor conc=1.1e20 gaussian characteristic=0.005 \
x.min= 22  x.max= 22 y.min=0 y.max=$'Spike_depth'


### C doping ###
# below interlayer
trap acceptor e.level = $Eg_Al0.08GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=6
trap donor e.level = $Eg_Al0.08GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=6

### C above interlayer
trap acceptor e.level = $Eg_Al0.08GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=4
```

```
trap donor e.level = $Eg_Al0.08GaN-$'e_compensating_donor' \
 density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=4
#trap donor e.level = $Eg_Al0.08GaN-$e_UID_donor density = $'density_UID_donor' \
#   degen.fac=2 sign = 1e-13 sigp = 1e-15 region=4

## C doping in interlayer 1

trap acceptor e.level = $Eg_Al0.54GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=5
trap donor e.level = $Eg_Al0.54GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=5

trap acceptor e.level = $Eg_Al0.80GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=11
trap donor e.level = $Eg_Al0.80GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=11

trap acceptor e.level = $Eg_Al0.90GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=12
trap donor e.level = $Eg_Al0.90GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=12

trap acceptor e.level = $Eg_Al0.78GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=13
trap donor e.level = $Eg_Al0.78GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=13

trap acceptor e.level = $Eg_Al0.54GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
```

```
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=14
trap donor e.level = $Eg_Al0.54GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=14

## C doping in interlayer 1 tail

trap acceptor e.level = $Eg_Al0.41GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=15
trap donor e.level = $Eg_Al0.41GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=15

trap acceptor e.level = $Eg_Al0.31GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=16
trap donor e.level = $Eg_Al0.31GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=16

trap acceptor e.level = $Eg_Al0.21GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=17
trap donor e.level = $Eg_Al0.21GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=17

trap acceptor e.level = $Eg_Al0.13GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=18
trap donor e.level = $Eg_Al0.13GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=18


## C doping in interlayer 2
```

```
trap acceptor e.level = $Eg_Al0.54GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=10
trap donor e.level = $Eg_Al0.54GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=10

trap acceptor e.level = $Eg_Al0.80GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=19
trap donor e.level = $Eg_Al0.80GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=19

trap acceptor e.level = $Eg_Al0.90GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=20
trap donor e.level = $Eg_Al0.90GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=20

trap acceptor e.level = $Eg_Al0.78GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=21
trap donor e.level = $Eg_Al0.78GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=21

trap acceptor e.level = $Eg_Al0.54GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=22
trap donor e.level = $Eg_Al0.54GaN-$'e_compensating_donor' \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=22

## C doping in interlayer 2 tail

trap acceptor e.level = $Eg_Al0.41GaN - $'e_level_deep_acceptor' \
```

```
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=23
trap donor e.level = $Eg_Al0.41GaN-$'e_compensating_donor'  \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=23

trap acceptor e.level = $Eg_Al0.31GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=24
trap donor e.level = $Eg_Al0.31GaN-$'e_compensating_donor'  \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=24

trap acceptor e.level = $Eg_Al0.21GaN -$'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=25
trap donor e.level = $Eg_Al0.21GaN-$'e_compensating_donor'  \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=25

trap acceptor e.level = $Eg_Al0.13GaN - $'e_level_deep_acceptor' \
density = $'density_deep_acceptor' degen.fac=2 \
sign = $'deep_acceptor_sign' sigp = $'deep_acceptor_sigp' region=26
trap donor e.level = $Eg_Al0.13GaN-$'e_compensating_donor'  \
density = $'density_compensating_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=26

### Unintentional donors in all regions

trap donor e.level = $Eg_Al0.08GaN-$'e_UID_donor' density = $'density_UID_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=2
trap donor e.level = $Eg_GaN-$'e_UID_donor' density = $'density_UID_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=3

# UID doping in contacts not needed as already highly doped
trap donor e.level = $Eg_AlN-$'e_UID_donor' density = $'density_UID_donor' \
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=8
trap donor e.level = $Eg_Al0.08GaN-$'e_UID_donor' density = $'density_UID_donor' \
```

```
  degen.fac=2 sign = 1e-13 sigp = 1e-15 region=9




#-----------------------------------------------------------------
#...  Models statements
#-----------------------------------------------------------------

models name=Cap temp=$TL  \
srh ^auger \
fermidirac incomplete print \
fldmob
# \
# lat.temp joule.heat

models name=Buffer temp=$TL  \
srh ^auger \
fermidirac incomplete print \
fldmob
# fnholes fnord
# lat.temp joule.heat


models name=Barrier temp=$TL \
srh ^auger \
fermidirac incomplete print \
fldmob
# \
# lat.temp joule.heat

models MATERIAL=AlGaN FLDMOB FERMI SRH AUGER INCOMPLETE temp=$TL PRINT



models name=Al0.08GaN:C temp=$TL \
srh ^auger \
fermidirac incomplete print \
```

```
fldmob
# fnholes fnord

models name=drain temp=$TL print
# \
# lat.temp joule.heat

models name=source temp=$TL print
# \
# lat.temp joule.heat


#-----------------------------------------------------------------
#...Material Parameters
#-----------------------------------------------------------------
#...GaN
#-----------------------------------------------------------------

material material=GaN \
      edb=0.02 gcb=2 gvb=2 \
tcon.const tc.const=1.6 \
eg300=$Eg_GaN egalpha=0 egbeta=0 \
align = 0.385 \
PERMITTI = 10.4
# egalpha=7.7e-4 egbeta=600

#-----------------------------------------------------------------
#...Al(x)Ga(1-x)N
#-----------------------------------------------------------------

material material=AlGaN \
vsatn=1e7 vsatp=1e6 \
tcon.const tc.const=0.5 \
egalpha=0 egbeta=0  \
PERMITTI = 10.7

# egalpha=7.7e-4 egbeta=600
```

```
#-----------------------------------------------------------------
#...  Contacts statements
#-----------------------------------------------------------------

contact name=substrate resistance=$'RC'
contact name=source resistance=$'RC'
contact name=drain resistance=$'RC'

# enable the thermal contact to the substrate terminal and add a thermal conductivity

# thermcontact number=1 x.min=-$'Lcontact' x.max=$'Lsd'+$'Lcontact' \
y.min=1.4-0.01 y.max=1.4+0.01 temp=300 alpha=16000



#----------------------------------------------------------------
#...Mobility Values:
#----------------------------------------------------------------

mobility name=Cap \
mun=1500  \
betan=2.3 \
tmun=1.5 \
vsatn=1.91e7

mobility name=UID \
mun=1500  \
betan=2.3 \
tmun=1.5 \
vsatn=1.91e7 \
mup=8 \
tmup=1.5

mobility name=Buffer \
mun=400  \
betan=2.3 \
tmun=1.5 \
```

```
vsatn=1.91e7 \
mup=8 \
tmup=1.5

mobility name=Barrier \
mun=20 vsatn=1e7 \
mup=1 vsatp=1e7

# contact mobility
#mobility name=drain_contact \
# mun=$mu_contact mup=10

#mobility name=source_contact \
# mun=$mu_contact mup=10

#------------------------------------------------------------------
# define fixed polarization charge
#------------------------------------------------------------------

## AlGaN top surface charge
#interface charge=$Qoffset s.i. \
# y.min=-($t_barrier+$t_SiNcap+0.001) y.max=-($t_barrier+$t_SiNcap-0.001)

# Cap/Al0.25GaN interface
interface charge=-$Qoffset s.i. \
y.min=(-$t_barrier-0.001) y.max=(-$t_barrier+0.001)



# Barrier/UID GaN interface
interface charge =  ( $Qp_Al0.25GaN - $Qp_GaN )  s.s.\
      y.min=0 y.max=0

# GaN/Al0.08GaN interface
interface charge = ( $Qp_GaN - $Qp_Al0.08GaN )  s.s.\
      y.min=0.5 y.max=0.5

# ########## first interlayer
```

```
# Al0.08GaN/ interlayer 1.8
interface charge =  -1.2e12 s.s.\
     y.min=1.292 y.max=1.292

# interlayer 1.7/ interlayer 1.8
interface charge =  -2.1e12 s.s.\
     y.min=1.294 y.max=1.294

# interlayer 1.6/ interlayer 1.7
interface charge =  -2.9e12 s.s.\
     y.min=1.296 y.max=1.296

# interlayer 1.5/ interlayer 1.6
interface charge =  -3.1e12 s.s.\
     y.min=1.298 y.max=1.298

# interlayer 1.4/ interlayer 1.5
interface charge =  -4.2e12 s.s.\
     y.min=1.3 y.max=1.3

# interlayer 1.3/ interlayer 1.4
interface charge =  -9.5e12 s.s.\
     y.min=1.302 y.max=1.302

# interlayer 1.2/ interlayer 1.3
interface charge =  -5.7e12 s.s.\
     y.min=1.304 y.max=1.304

# interlayer 1.1/ interlayer 1.2
interface charge =  4.8e12 s.s.\
     y.min=1.306 y.max=1.306

# interlayer 1.0/ interlayer 1.1
interface charge =  1.0e13 s.s.\
     y.min=1.308 y.max=1.308

# interlayer 1.0/Al0.08GaN interface
```

```
interface charge =  1.4e13 s.s.\
     y.min=1.31 y.max=1.31

# ########## second interlayer

# Al0.08GaN/ interlayer 2.8
interface charge =  -1.2e12 s.s.\
     y.min=2.302 y.max=2.302

# interlayer 2.7/ interlayer 2.8
interface charge =  -2.1e12 s.s.\
     y.min=2.304 y.max=2.304

# interlayer 2.6/ interlayer 2.7
interface charge =  -2.9e12 s.s.\
     y.min=2.306 y.max=2.306

# interlayer 2.5/ interlayer 2.6
interface charge =  -3.1e12 s.s.\
     y.min=2.308 y.max=2.308

# interlayer 2.4/ interlayer 2.5
interface charge =  -4.2e12 s.s.\
     y.min=2.31 y.max=2.31

# interlayer 2.3/ interlayer 2.4
interface charge =  -9.5e12 s.s.\
     y.min=2.312 y.max=2.312

# interlayer 2.2/ interlayer 2.3
interface charge =  -5.7e12 s.s.\
     y.min=2.314 y.max=2.314

# interlayer 2.1/ interlayer 2.2
interface charge =  4.8e12 s.s.\
     y.min=2.316 y.max=2.316

# interlayer 2.0/ interlayer 2.1
```

```
interface charge =  1e13 s.s.\
     y.min=2.318 y.max=2.318

# interlayer 2.0/Al0.08GaN interface
interface charge =  1.4e13 s.s.\
     y.min=2.32 y.max=2.32

# AlN/Silicon interface
#interface charge = $Qp_AlN s.s.\
#      y.min=4.12 y.max=4.12



#------------------------------------------------------------------
#...Output options
#------------------------------------------------------------------
output  e.field j.electron j.conduc j.disp j.total ex.field \
        ey.field e.mobility  qss  charge val.band con.band \
        qfn qfp  band.param traps.ft traps devdeg l.temp noise.all
#------------------------------------------------------------------
```

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