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Design Trade-off Analysis and Optimisation of a High-density Active Shunt Regulator for Aircraft

by

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To my best friend & partner Junxi and my mother

Contents

Abstract

Moving towards More Electric Aircraft (MEA) demands for high efficiency and high power density power electronics. There are two important areas that are pushing the boundaries of future power converters: advanced converter topologies (e.g. three-level topology) and emerging power semiconductor devices (e.g. Wide Band Gap power devices). The benefits of these new technologies are still subject to quantified analysis from the system level point of view over a particular application.

The aim of this work is to investigate the design trade-offs and optimisation of a 27 kVA three-phase Active Shunt Regulator (ASR) system regarding three main design variables: topology, power device and switching frequency. The emerging technologies, the three-level T-type topology and Silicon Carbide (SiC) devices, are evaluated against the state-of-the-art commercial solution, i.e. Silicon IGBT and two-level topology. To realize a holistic view of the system, not only the active power devices, but also the passive components require designing and accurate modelling. Passive components considered in this work include the heatsinks, the filter inductors and the DC-link capacitors, which account for a substantial contribution to the power loss and volume/weight of the converter system. Power loss models, design procedures and volume/weight models are established for individual components of the ASR system. As the most challenging part, the core loss of inductors is thoroughly investigated and evaluated. Additionally, the neutral point voltage balancing issue in three-level converters is addressed in this work when the ASR system operates at a low power factor.

The developed mathematical optimisation tool shows a prediction on the achievable performance of the converter and the quantified design trade-offs. For example, increasing the switching frequency reduces the size of filter components while it requires larger heatsink for increased switching loss. Prototypes are built to validate the theoretical models and realize the optimal design identified.

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Finally, I want to thank my wife/partner/friend Junxi Yao for her company, love and understanding, in good times and bad times. And I couldn't thank my parents enough for everything. I wish they are proud of me.

Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

SIGNED: ..... DATE:.....

Memorandum

This PhD thesis with the title "Design Trade-off Analysis and Optimisation of a High-density Active Shunt Regulator for Aircraft" is based on the work carried out by the author as a member of the Electrical Energy Management Group (EEMG) in the Department of Electrical and Electronic Engineering of the University of Bristol. The main contributions claimed by the author are as follows:

I. Neutral Point balancing scheme for three-level three-phase converters

   a. Proposed an analytical model to analyse the device power losses impacted by Virtual Zero-level Modulation (VZM), which is a novel control scheme to balance the neutral point voltage.

   b. Experimentally implemented VZM in a test rig and evaluated the power losses.

   c. Proposed a hybrid NP balancing algorithm integrating VZM and conventional Zero-sequence Signal Injection to improve the efficiency performance.

II. Core loss modelling of filter inductors

   a. Proposed a test circuit with the ability to compensate asymmetric amplitude of square-wave inductor voltage caused by power device voltage drops.

   b. Proposed a discontinuous test procedure aiming at minimized testing process, the Triple Pulse Test, which reduces the requirement/stress of the hardware in the testing.

   c. The power loss of a customized high-power-density inductor based on Cobalt Iron alloys is experimentally characterized with the proposed approach.

   d. Proposed a user-friendly loss map for straightforward calculation of the inductor core loss.

   e. Proposed an analytical approach to estimate the inductor core loss for given PWM operation of the power converter. The analytical model is developed on both two-level and three-level converters.

III. System-level trade-off analysis and optimisation of a 27 kVA Active Shunt Regulator system

Publications

Journal Publications

1. **J. Wang**, K.J. Dagan, X. Yuan, W. Wang and P.H. Mellor, "A Practical Approach for Core Loss Estimation of a High-current Gapped Inductor in PWM Converters with a User-friendly Loss Map", *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5697–5710, Jun. 2019

Conference Publications

1. **J. Wang**, X. Yuan, Y. Zhang, K.J. Dagan, X. Liu, D. Drury, P.H. Mellor and A. Bloor, "Analytical Averaged Loss Model of Three-Phase T-type NPC STATCOM with Virtual Zero Voltage Level Synthesis Modulation," in *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017

2. **J. Wang**, X. Yuan, K.J. Dagan, P.H. Mellor, D. Drury and A. Bloor, "Universal Neutral Point Balancing Algorithm for Three-phase Three-level Converters with Hybrid of Zero-sequence Signal Injection and Virtual Zero-level Modulation" in *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE),* 2018

3. **J. Wang**, K.J. Dagan, X. Yuan, "An Efficient Analytical Inductor Core Loss Calculation Method for Two-level and Three-level PWM Converters based on a User-friendly Loss Map" in *Proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC),* 2019

List of Symbols

A	Area	m^2
A_c	Cross section area of the magnetic core	m^2
A_{cu}	Cross section area of copper conductor	m^2
A_p	Area product	m^2
B	Magnetic flux density	T
B_{DC}	DC component of magnetic flux density	T
B_m	Amplitude of the ac component of magnetic flux density	T
B_{pk}	Peak value of total magnetic flux density ($B_{pk} = B_{DC} + B_m$)	T
B_{sat}	Saturation flux density	T
C	Capacitance	F
D	Duty cycle (0~1)	
E_{sw}	Switching energy	J or mJ
f_0	Fundamental frequency	Hz
F_R	Winding resistance factor	
f_{sw}	Switching frequency (carrier frequency)	Hz
H	Magnetic Field Strength	A/m
I	Current	A
J	Current density	A/m^2
$J_n(x)$	Bessel function of order n and argument x	
k_{sw}	Switching loss factor	
L	Inductance	H
M	Modulation index	
MTL	Mean Turn Length of the inductor windings	m
$N1/N2$	Number of turns (primary winding/secondary winding)	
P	Power	W or kW
R_{on}	On-state resistance	Ω
R_{th}	Thermal resistance	K/W or °C/W
R_{wac}	Winding total equivalent resistance considering AC effects	Ω
R_{wdc}	Winding DC resistance	Ω
T_0	Period of a fundamental cycle	s
T_a	Ambient temperature	°C
T_j	Junction temperature	°C
T_{sw}	Switching period	s
U	Voltage	V

V	Volume	m^3 or ℓ
W	Weight	kg
γ	Specific power	kVA/kg
η	(relative) Efficiency	
μ_0	Permeability of free space	H/m
μ_r	Relative permeability	
ρ	Power density	kVA/ℓ
ρ_{cu}	Conductivity of copper	Ω·m
φ	Power factor angle	deg or rad

List of Abbreviations and Acronyms

2L	Two-level
3L	Three-level
3LT	Three-level T-type
AC	Alternating Current
APU	Auxiliary Power Unit
ASR	Active Shunt Regulator
CM	Common Mode
CoFe	Cobalt Iron
CSPI	Cooling System Performance Index
DC	Direct Current
DM	Differential Mode
DPT	Double Pulse Test
DSP	Digital Signal Processor
EMF	Electromotive force
EMI	Electromagnetic Interference
FACTS	Flexible AC Transmission System
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
IGSE	Improved Generalised Steinmetz Equation
MEA	More Electric Aircraft
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NP	Neutral Point
NPC	Neutral Point Clamped
PFC	Power Factor Correction
PM	Permanent Magnet
PMG	Permanent Magnet Generator
PWM	Pulse Width Modulation
RMS	Root Mean Square
SE	Steinmetz Equation
Si	Silicon
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
TPT	Triple Pulse Test

VS	Variable Speed
VSC	Voltage Source Converter
VSG	Variable Speed Generator
VZM	Virtual Zero-level Modulation
WBG	Wide Band Gap
WFG	Wound Field Generator
ZSI	Zero-sequence Signal Injection

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CHAPTER 1

Application Background and Research Aims

1.1 More Electric Aircraft (MEA) and electrical power generation in aircraft

More Electric Aircraft (MEA) is the current trend in modern aircrafts which aims to increase the use of electrical power systems that fully or partially replaces the conventional mechanical, hydraulic and pneumatic power systems [1]–[7]. MEA offers several attractive benefits, such as increased reliability, reduced complexity and lower installation and maintains cost [7], [8]. The electrification of aviation also leads to low-emission, low-energy-consumption and low-noise aircrafts that attract prioritized interests and resources from the governments and the industry [9], [10]. Moving towards MEA demands for increased on-board electric power generation. In current aircrafts, Variable Speed (VS) system is the preferred option for electrical power generation due to its simplicity, reliability and better flexibility [11]–[13]. For example, the latest Boeing 787 is equipped with four 250-kVA Variable Speed Generators (VSGs) as the main source of electric power generation [5], [11]. VS based aircraft electric systems show promising advances and implementations in the past decades [13], [14], in which the core components are the electric machines and power electronics [2], [6]. As the advances of aircrafts constantly call for the reduction of weight and volume, advanced technologies for the electric machines and power electronics are being actively explored to achieve better performance.

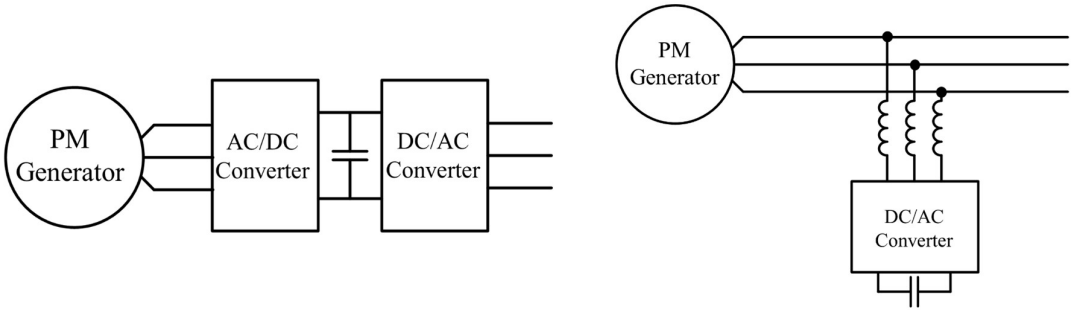
1.2 Permanent Magnet Generator (PMG) with an Active Shunt Regulator (ASR)

For future MEA, the power density of the electric machine is predicted to advance to 10 kVA/kg by 2025, and 20 kVA/kg by 2035 [11], [15]. As the VSG in the VS system, three-stage Wound Field Generators (WFG) are

the most commonly used option on commercial and military aircrafts [16]. However, WFGs are limited in power density because they cannot run at a very high speed due to the complex rotor windings. To achieve a higher power density, Permanent Magnet (PM) machines are considered a better option for future high-power generation systems on aircrafts. Permanent Magnet Generator (PMG) features many advantages compared to the WFG [7], [11], [17]:

- High power density (e.g. 3.3 – 16 kVA/kg)
- High efficiency throughout the frequency range (e.g. loss-less excitation, low rotor loss)
- Simple, robust construct and improved reliability

Due to the fixed excitation of a PM machine, the operation of a PM generator requires Pulse Width Modulation (PWM) power electronics converters to regulate the terminal voltage [16]–[18]. There are two options for the PM generator/converter configurations as shown in Figure 1-5.



(a) Back-to-back converter (b) Active Shunt Regulator

Figure 1-1. Candidate PM generator/power converter configurations

The back-to-back structure in Figure 1-5(a) can be considered as the state-of-the-art [11], [19], [20], in which the power converter is formed by a rectifier end and an inverter end with an internal DC-link. As the main advantage, this back-to-back converter can accommodate a wide speed range of the generator and has the ability to turn off the output voltage. The main disadvantage of the back-to-back configuration is the lower efficiency and lower power density as a result of the two-stage conversion.

In this work, the power generation system is considered in an Auxiliary Power Unit (APU) system with a shaft speed of 400±5 Hz. Because the shaft speed is relatively constant in this case, an Active Shunt Regulator (ASR) configuration shown in Figure 1-1(b) is considered. The ASR system has a simpler structure and potentially offers better efficiency and power density with less power electronics components required. The parallel power converter is a Voltage Source Converter (VSCs) that export capacitive/inductive reactive power to the coupled AC grid to regulate the generator output voltage. A circuit diagram of the target power generation system is shown in Figure 1-2.

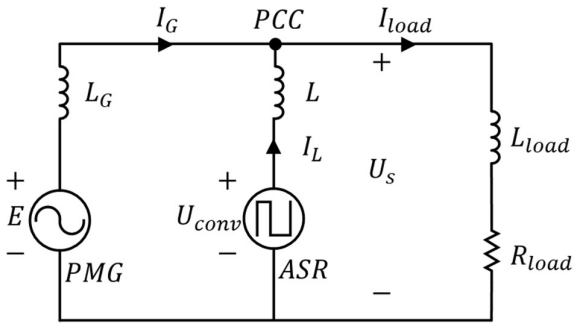
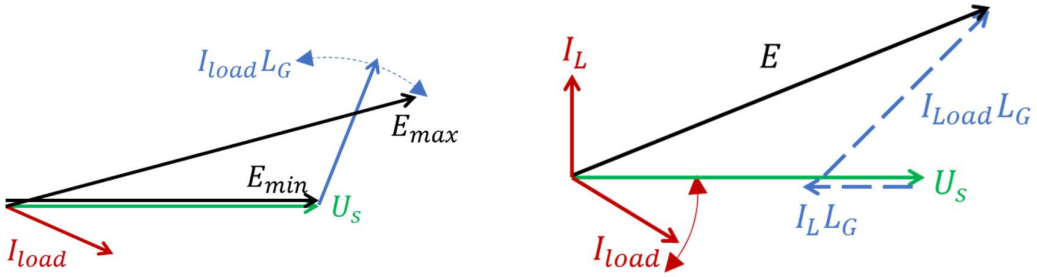


Figure 1-2. Circuit diagram of a power generation system with PMG, ASR and RL load

Where E is the induced EMF of the generator; I_L is the ASR output current; I_{load} is the load current; I_G is the generator output current; U_{conv} is ASR output voltage; U_s is the regulated generator terminal voltage. Figure 1-3 illustrates a comparison of the operation principle between WFG system and a PMG/ASR system. A WFG operates with the adjustable excitation to adapt to the load condition, while the PMG relies on the ASR to regulate the output voltage.



(a) (b)

Figure 1-3. Phasor diagram of a loaded (a) WFG (b)PMG

From the ASR point of view, the ideal power converter only inject/absorb reactive power to regulate the

generator terminal voltage, as shown in Figure 1-4.

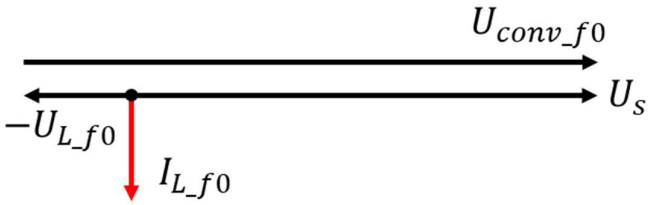


Figure 1-4. Phasor diagram of the loaded ASR system

Where U_{conv_f0} is the fundamental-frequency voltage generated by the ASR; I_L and U_L are the voltage and current on the line inductor. The operation principle of the ASR is similar to a Static Synchronous Compensator (STATCOM). STATCOMs are widely employed in AC power grid applications as reactive power compensators [21], which play an important role in Flexible AC Transmission System (FACTS) [22]. There are also examples applying STATCOMs to regulate the terminal voltage for self-excited induction generators [23] and PMGs for wind power generation [24]. Due to the distributed load on the aircraft, the Point of Common Coupling (PCC) for the shunt regulation is defined as the generator output terminal voltage. The regulated generator output terminal voltage must comply with the MIL-STD-704 standard [25]. Differently, the PCC in a typical STATCOM system is defined to be close to the load end. Because the PM + ASR configuration for aircrafts is relatively novel at the time of this work, there is only limited research can be found in the literatures while its performance is still under evaluation both in academia and industry.

The electrical systems on an aircraft have various specifications. As the widely adopted standard since 1950s, the 115/200 V AC system with a frequency of 400 Hz is commonly used for modern aircrafts such as Airbus A380-800 [11]. This work intends to develop PMG system to provide a like-to-like comparison with an existing 45 kVA, 115V WFG system that has been characterized. Therefore, a PMG/ASR system with 45 kVA continuous output and 115 Vrms regulated voltage has been designed in this project. Considering the predefined load condition in the target system, a 27-kVA rated ASR is designed as the subject of research in this work, as shown in Figure 1-5.

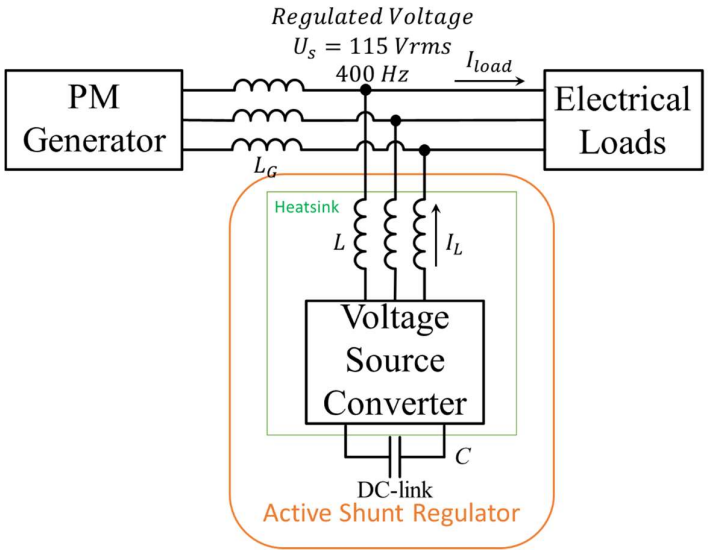


Figure 1-5. Active Shunt Regulator system for the PM generator based power generation system

The specifications of the PMG/ASR are summarized in Table 1-1.

TABLE 1-1. SPECIFICATIONS OF THE ASR SYSTEM

Regulated generator terminal voltage U_s	115 Vrms
Rated output of the generator	45 kVA
Lowest load power factor	0.75
Continuous rated current	130 Arms
Sustained overload current	200 Arms
Regulated voltage frequency f_0	400 Hz
Generator configuration	4 poles, 12000 rpm
Current rating I_n	78 Arms
DC-link voltage U_{DC}	350 V
ASR Capacity S	27 kVA

The following major components of the ASR system will be investigated in this work:

- Power device
- Line inductor
- DC-link capacitor
- Heatsink

1.3 Power Electronics in MEA

As one of the most important technologies for MEA [15], power electronics converters are also demanding advances in both efficiency and power density. For instance, a power density of 33 kW/ℓ and a efficiency of >

98% are targeted by 2025 for the automotive electric traction drive systems [26]. Previous research has been intensively conducted to identify the performance limitations and the future trends of the development of power converters [27]–[30].

For comparing and benchmarking the performance of power converters, several metrics are defined and widely used in the previous research and roadmaps [26]–[29]. For the ASR system, the performance metrics of interest are the overall converter efficiency η, power density ρ and specific power γ. The efficiency η is normally defined as follows ([27], [28]):

$$\eta = 1 - \frac{P_{loss}}{P_{out}} \tag{1-1}$$

Where P_{loss} is the power loss; P_{out} is the output power. However, in this study, the efficiency of the ASR system is not straightforward because it mainly generates reactive power rather than real power. Therefore, a Relative Efficiency of the converter system is defined in this study as

$$\eta = 1 - \frac{P_{loss}}{S_{out}} \tag{1-2}$$

Where S_{out} is the rated capacity of the converter, which is 27 kVA in the target system.

The power density of the converter is defined for per unit volume as

$$\rho = \frac{S_{rated}}{V_{total}} \left(\frac{kW}{dm^3}, \frac{kVA}{dm^3}\right) \tag{1-3}$$

For aircraft applications, the weight of components is equally important as the volume. For per unit weight, the specific power of the converter is defined as

$$\gamma = \frac{S_{rated}}{W_{total}} \left(\frac{kW}{kg}, \frac{kVA}{kg}\right) \tag{1-4}$$

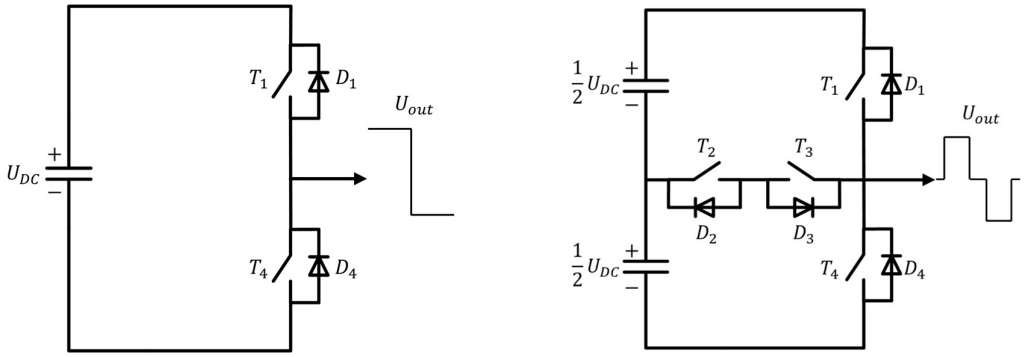
To achieve a high power density of the power electronics system in discussion, a key aspect is to effectively reduce the passive components, such as heatsinks and filter components, which account for a major portion of the volume, weight and cost [26]–[29], [31]. For example, the filter components occupy 40% of the total volume and

weight of the converter system in [32]. [33] reported that the passive components contribute over 80 % weight of a converter. As for the efficiency, moving from 96% to 99% efficiency would significantly reduce the heatsink size and would allow a transformative change from liquid cooling to air cooling. However, there are several conflicting design constraints which need to be considered together. For example, lower switching frequency may lead to improved efficiency, but it comes with the cost of larger filter components. Increasing the switching frequency results in the reduced size of the filters, but the associated additional switching losses will require bigger heatsink to extract the heat.

There are two important areas that drive further improvement of the power density of power converters: converter topologies and power semiconductor devices [30]. Naturally, an optimal solution may involve both the advanced converter topologies and emerging semiconductor devices, which are expected to lead to a significant reduction of the passive components.

1.3.1 Converter topologies

Two-level (*2L*) converter topology is the most widely used configuration for low-voltage industry applications, such as motor drives, due to its simple structure and maturity [34]. The basic concept of the two-level converter is illustrated in Figure 1-6. However, the two-level converters feature several disadvantages due to the switching over the full DC-link voltage, such as high switching losses and high output harmonics. The high switching losses prevent the two-level converters to operate at a higher switching frequency (e.g. 50 kHz instead of 10 kHz), because the switching losses and the associated thermal stress increases significantly at a higher switching frequency. The high output harmonics require large filter components to attenuate.



(a) two-level (b) three-level T-type

Figure 1-6. Converter topology concept

As the advanced technology, multilevel topologies have been intensively researched over the past decades [35], [36]. For low/medium-voltage applications, three-level (*3L*) converters show a range of attractive benefits, such as improved efficiency and low output voltage/current harmonics. These benefits are mainly a result of the commutation voltage at only half of the DC-link voltage, as shown in Figure 1-6(b).

Previous research [34], [37]–[39] have provided comparative studies to demonstrate the benefits of advanced three-level topologies over the conventional two-level topology. [34], [38], [40] demonstrated the benefits of reduced switching loss of the three-level topology. The reduced switching loss enables the converter to operate at a higher switching frequency or require a smaller heatsink. [34], [38], [39], [41] draws a conclusion that three-level inverters offer reduced voltage/current harmonics, which lead to smaller and lighter filter components. Other benefits of the *3L* topology such as reduced machine insulation stress and machine harmonic losses are also reported [34], [38]. Note both the two-level and three-level topologies introduced here are hard-switching topologies. Soft-switching topologies have been proposed to reduce the switching losses and achieve high switching frequency. However, it requires many auxiliary components with accurate parameters and greatly increases the circuit and control complexity [42], [43].

There are various options and derivations of the three-level topology [34], [35], such as Neutral Point Clamped (NPC) topology and three-level T-type (*3LT*) topology [44] (shown in Figure 1-6(b)). The NPC topology was firstly proposed in 1981 [45] and already has been widely used in medium-voltage applications [34]. But the

NPC topology suffers from unevenly distributed power loss between devices and increased conduction loss due to the current constantly flowing through series-connected devices [46]. As an alternative, the *3LT* topology is free from the two clamping diodes in the NPC and become a more attractive option for low-voltage applications nowadays. [34], [40] states that the *3LT* topology combines the positives of both *2L* and NPC topologies.

However, the three-level topology also poses several challenges and drawbacks at the same time. If a neutral point is not required, the three-level topology requires four times installed capacitance at the DC-link compared to the two-level topology [34], due to the series connection of the DC link. The conduction losses in a *3L* could increase due to the use of series-connected devices [34] compared to the *2L* topology. Originally, the series-connected devices in three-level topology was to overcome the limited voltage rating of the devices for medium-voltage applications. But for low-voltage applications in this case, reducing the required device voltage ratings is not necessary anymore, because the available power devices can sufficiently block the full DC-link voltage [34]. Additionally, the voltage balancing issue of a three-level topology must be solved, which poses a challenge for low-power-factor operations [47], [48].

Regarding the ASR system, the performance of the three-level topology is still subject to comprehensive evaluation considering both the efficiency and power density. In this work, the *3LT* topology is considered to compare against the traditional two-level topology.

1.3.2 Power devices

Silicon (Si) based Insulated Gate Bipolar Transistor (IGBT) is the most common option in industrial products for high power (1~100kW), low-voltage (≤ 600 V DC-link voltage) applications due to the maturity of this technology. However, Silicon IGBT/diode suffers from the tail current associated turn-off loss and the reverse-recovery loss in the diode [49], which limits the power density of the converters [50]. The typical switching

frequency of multi-kW power converters based on Si IGBT is only 10 kHz ~ 20 kHz. To rise the switching frequency of Si devices, large heatsinks are required to counter the high switching losses, which can degrade the power density of the converter substantially.

Nowadays, the Silicon based transistors are facing the challenge of emerging Wide Band Gap (WBG) devices such as Silicon Carbide (SiC) transistors and Gallium Nitride (GaN) transistors. These new-generation WBG power devices offer substantially lower power losses and faster switching speed [50]. 1200 V rated SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are commercially available by the time of this work targeting as the direct replacement of Si IGBT for low/medium voltage applications [51]. The main advantages of the SiC MOSFET over the Si IGBT are:

- Lower switching energies (e.g. 70% lower than Si devices [52])
- Higher thermal conductivity [27]
- Higher operating temperature

Apart from the SiC MOSFET, SiC diodes are also available, which features zero reverse-recovery loss compared to Si diodes [49]. There is an option of replacing only the Si diode with SiC diodes for the improved reverse-recovery loss and lower cost at the same time [49]. But it is still preferred to employ all-SiC (SiC MOSFET + SiC Schottky diode) solution for optimised converter performance, because a major portion of the switching losses are in the Si IGBTs as analysed in [34]. These merits of SiC MOSFET/diode open up the possibility of realizing power converters with substantially improved power efficiency and power density. The low switching loss of SiC devices enables the converter to operate at a higher switching frequency without considerable cooling efforts demanded. A higher switching frequency can lead to smaller filter components required target at attenuating the switching frequency harmonics, such as reduced line inductors and DC-link capacitors, which

allow the power converter to achieve a smaller volume and a lighter weight. However, high switching frequency at a certain degree can also degrade the system power density due to the enlarged heatsink, the increased EMI emissions and associated EMI filters [52].

Comparative evaluations are conducted in many publications to investigate the benefits of replacing Si devices with SiC devices in inverters/motor drives and DC/DC converters [49], [52]–[54]. These studies confirm the benefits of employing SiC devices regarding the power density and efficiency. For example, SiC devices can lead to a 159.4% increase of power density over Si devices as demonstrated in [52]. [55] shows a 70% reduction of switching loss by using SiC technology over Si devices. However, the precise improvement that the SiC devices can bring on the system still needs to be established on a particular application. Depending on the system specifications and constraints, the weighing of conflicting impact caused by increasing switching frequency, such as increased heatsink size against reduced filter size, still requires quantified analysis. Therefore, the design trade-offs considering Si IGBT/diode and SiC MOSFET/diode are subject to thorough investigation regarding the ASR application in discussion.

To investigate the power devices, this work is based on representative commercial products. To select an adequate product, the voltage ratings of power devices are normally over-rated as 1.5 to 2 times of the DC-link voltage [56], considering the overshoot voltage caused by the parasitic inductance. Considering the 350 V rated DC-link voltage in the ASR system and the commercially available options, 1200-V rated power devices are selected. Additionally, the commercially available Silicon Carbide (SiC) power devices are all rated at 1200 V or above. Next, considering the rated current at 78 Arms, it is preferred to select power modules over discrete devices. Off-the-shelf discrete SiC devices are rated at <100 A (e.g. C2M0025120D from © CREE). Considering the availability of commercial products, 300-A rated power modules are targeted for this application. To summarise, this work focuses on 1200-V, 300-A rated power modules and evaluate their performance in the target ASR system.

1.3.3 Device/topology combinations

As introduced, the topology and the power device are two fundamental directions to improve the power converter performance. For the given application, it is worth exploring whether the use of improved devices, more complex topologies or a combination of both results in the best overall solution.

Previous studies focusing on power devices are established on certain topologies. For example [54] demonstrated the benefits of SiC MOSFET in *3LT* inverters, which reports a 50% reduction of total power loss compared to a Si IGBT based configuration. [53] provides a benchmarking of SiC devices in single-phase T-type inverters regarding both the efficiency and power density. [52], [57] focuses on the optimisation of high power density 3-phase two-level converter with SiC device. [58], [59] evaluated commercially available two-level, 1200-V SiC MOSFET module and Si IGBT module. For the studies focusing on comparing topologies, mainly one type of power device is studied. For example, [38] compares two-level and three-level topologies based on only IGBT devices. [60] shows the design of a high power density converter for aircrafts considering two-level and three-level topologies based on Si devices. [34] considered the Si devices and SiC diode in two-level converters, but not considering the all-SiC options.

Therefore, there is still limited research providing a comparative study of the converter performance over various device-topology combinations within the same context. It is not clear how much a weighed improvement can be made through the advanced topology, the advanced power device or both, especially when multiple performance metrics are considered, i.e. the efficiency and power density. Therefore, this work intends to investigate, quantify and weigh the performance of several device-topology combinations. The considered devices are: 1. Si IGBT + Si diode; 2. SiC MOSFET + SiC Schottky diode. The considered topologies are: 1. Two-level 2. Three-level T-type. Two options of power devices and two topologies generate four combinations as shown in Figure 1-7.

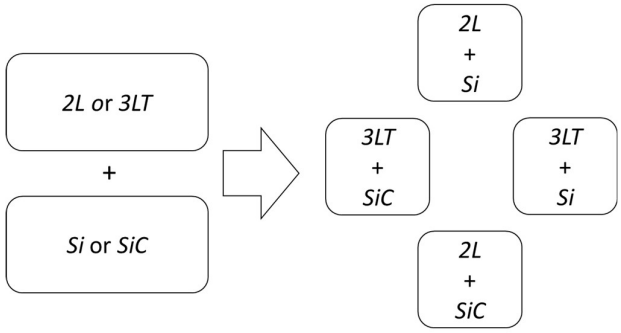
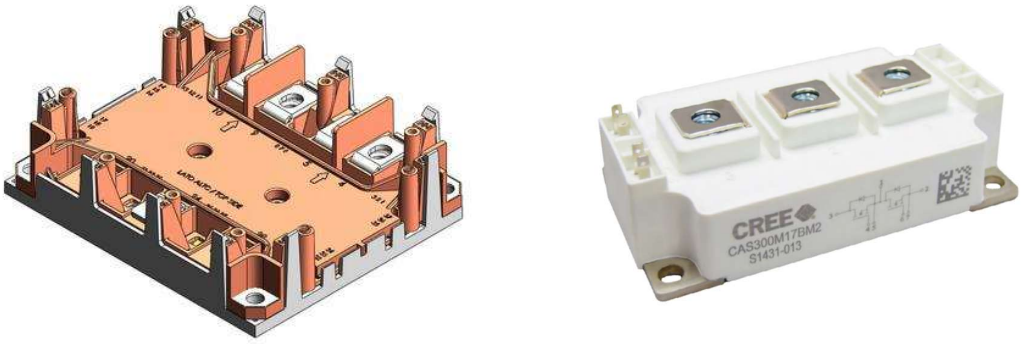


Figure 1-7. Four considered device-topology combinations

The four device-topology combinations are analysed in this study. The *2L*-Si option is considered the state-of-the-art industrial standard for benchmarking. Two representative commercial power modules are selected for the investigation:

(1) 1200-V, 300-A SKiM301TMLI12E4B power module from Semikron with Si IGBT + Si diode and three-level T-type topology. This power module can be treated as the reference of Si based solution for both two-level and three-level topology, with its footprint shown in Figure 1-8 (a).

(2) 1200-V, 300-A power module CAS300M12BM2 from CREE with SiC MOSFET + SiC Schottky diode and two-level topology. The footprint of this power module is shown in Figure 1-8 (b).



(a) SKiM301TMLI12E4B (b) CAS300M12BM2

Figure 1-8. Footprint of selected reference power modules

1.3.4 Passive components in the ASR

There are three main passive components in the target ASR system: (1) line inductor (2) DC-link capacitor (3) heatsink. The line inductors (also referred as the boost inductor) interface the power converter and the power

grid (generator output voltage), which provides the filtering of the switching-frequency current ripples. The line inductor L can contribute a significant portion of volume/weight among the passive components. For example, the line inductor can account for 32% of the converter volume enclosure [61], [62] and 59 ~78 % of the weight of the converter [52].

The DC-link of the ASR system is formed by capacitors as the energy buffer to stabilize the DC-link voltage. The DC-link capacitors also contributes to the converter volume/weight (e.g. 15% of the volume [63]). It should be noted that the DC-link voltage in the ASR system is floating. Referring to the phasor diagram Figure 1-4, the DC-link voltage needs to satisfy the following equation so that the converter can generate sufficient amplitude of AC voltage for the regulation considering the voltage drop on the line inductance.

$$\frac{U_{DC}}{2\sqrt{2}} \cdot M \geq U_s + \omega_0 L I_L \tag{1-5}$$

Where M is the modulation index of the converter, which varies between 0 ~ 1.15. Considering the rated current of the converter, the DC-link voltage is rated at 300 ~ 350 V. Therefore, the DC-link in this case cannot be connected to the existing 115 V AC/270 V DC systems in the aircrafts [4].

For the target power generation system, the standard of load current harmonics and Electromagnetic Interference (EMI) is defined by DO-160E for aerospace applications [64]. Apart from the line inductors, normally there are Differential Mode (DM) and Common Mode (CM) EMI filters installed within the power converter to satisfy the EMI standard [39], [52], which also contribute to the volume/weight of the converter system [30], [63], [65]. In the target system, the EMI filters can be placed inside the ASR converter, or at the generator output terminal (after the regulation point). Due to the scope of this thesis, EMI filters are not considered as part of the ASR system in the analysis.

Cooling system is another important component to dissipate the heat generated in the power converter.

Designed to cool the power converter, the heatsink size is directly relating to the converter power loss, of which the majority is the power device loss. Heatsinks also occupy significant portion of mass/weight of a power converter [27], [66] and therefore require careful design and analysis.

1.3.5 Optimisation of power converters

In industry, the typical process of developing a power converter is a repetitive process of prototyping, evaluation and improvement [67]. To achieve faster development and better performance, the use of Virtual Prototyping has been advocated [30], [68]–[70] in the industrial design procedure. Virtual Prototyping utilizes mathematical modelling and/or multi-physics software to aid and boost the design process of power converters towards optimized performance of the overall system. Previous studies have shown intensive efforts towards the optimisation of power converters, such as [30], [52], [63], [67], [71]–[75]. The optimisation of power electronics requires multi-domain and multi-objective considerations [30], [63]. A power electronics system does not only involve electrical design, but also involve the thermal stresses, electromagnetic issues and mechanical considerations. The efficiency, power density and specific power are all important metrics in modern power converters and are demanded as the objectives of the optimisation [28].

The multi-objective optimisation of power electronics consists of the following main sectors [30], [76]:

- Generation of design space (e.g. power device, topology and switching frequency)
- Definition of constraints (e.g. thermal limit and harmonics requirement)
- Performance functions (e.g. efficiency, volume and weight)
- Visualization and identification of design options and trade-offs for optimal searching

The Pareto Front analysis is commonly used to visualize and identify the performance trade-off limits in the optimisation of power converters [30], [77]. The most common Pareto Front analysis is the between the efficiency

and power density of power converters [63], [67], [72]. In recent studies, the cost is also considered as an important objective that requires Pareto Front optimisation [30].

In aerospace applications, the weight of systems is of great consideration as it impacts the fuel efficiency [5]. Therefore, the Pareto Front analysis in this work considers efficiency, power density and specific power as the three main optimisation objectives of the ASR system.

The multi-objective optimisation requires the utilization of software and programming, which provides efficient computation and handling of vast data and mathematical models [30]. In this work, the optimisation analysis is implemented in MATLAB based on analytical models of the system and individual components.

In the optimisation of a power converter, there are many coupling effects and considerations between individual components. In order to reduce the complexity of the optimisation algorithm, problem simplifications are necessary to break the whole system into individual sub-modules to be optimized [30]. In this work, simplifications to a certain extent will be introduced in the analysis of each individual components. Overall, the purpose of the optimisation analysis is to provide a top-level guidance of the design/selection of the key components of the system, such as topology, power device and switching frequency.

1.4 Research objectives

In this work, the enabling technologies, mainly SiC devices and three-level converter topology, are investigated aim at improving the system power density/specific weight by reducing the passive components. Design procedures and analytical models are developed for each individual component to serve the Virtual Prototyping purpose and predict the performance. A system-level optimisation tool is developed mathematically to explore the design trade-offs and performance limitations of the converter system. The ultimate objective is to identify the optimal design of the ASR system considering multiple conflicting performance objectives.

1.5 Structure of Thesis

CHAPTER 2 presents the models of the power losses of power devices. Quantified benchmarking is performed to compare the power loss performance of the considered device-topology combinations. Analytical formulas are established to estimate the device power loss over a range of operating points of the converter. Estimated device power loss enables the design/analysis of the heatsink.

CHAPTER 3 addresses the low-frequency Neutral Point voltage oscillation issue in three-level three-phase converters. A literature review is conducted to identify the existing Neutral Point voltage balancing schemes to counter this issue without adding additional DC-link capacitance. Limitations of the existing approaches/models are investigated. Improved voltage balancing scheme is explored and implemented.

CHAPTER 4 details the design process of the three main passive components: DC-link capacitor, line inductor and heatsinks. Literature reviews are conducted for the design/analysis of each individual component. The design concerns and the performance modelling of the passive components are explored.

CHAPTER 5 addresses the modelling of the inductor losses, especially the core loss. The literature review shows the challenges and state-of-the-art of modelling the inductor core loss in PWM converters. The testing approach and modelling method are investigated considering the inductor exposed in PWM excitation. Following empirical measurements, an analytical approach is presented to utilize the pre-measured loss map to estimate the inductor core loss for a given operating point of the two-level or three-level power converter.

CHAPTER 6 presents the system-level optimisation process. Based on the optimisation analysis, design trade-offs and performance limitations can be visualized in the form of Pareto Fronts. Prototypes are built to demonstrate the selected optimal of design.

CHAPTER 7 summarizes this work and presents an outlook of the future work.

CHAPTER 2

Modelling of Active Power Devices

Typically, power devices are the main source of power losses in a power converter. The modelling of the device power losses is important for the thermal considerations and the estimation of the converter efficiency. The device power loss reflects on the required heatsink performance, which is designed to extract the heat generated during the operation of power devices to prevent the devices exceeding a safe operating temperature. Previous studies have investigated the device power losses in PWM converters using analytical models [78]–[81]. Through analytical models, the averaged steady-state power loss of each power device can be estimated for a given operating point of the power converter.

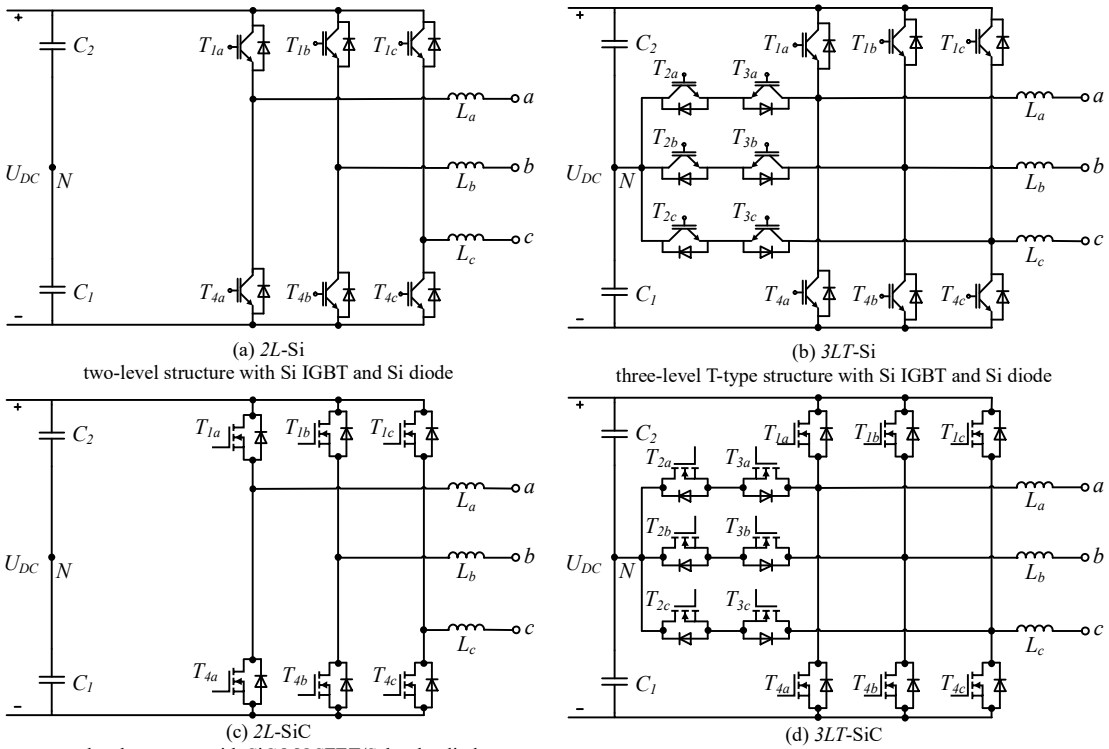
As discussed in the introduction, the benefits of the emerging SiC devices and three-level topology is subject to quantified evaluation on the target system. Therefore, this chapter intends to develop analytical models for the four hard-switched device-topology combinations in discussion to benchmark their power loss performance.

2.1 Topologies and power devices

As introduced in Section 1.3.3, this work intends to investigate four device-topology combinations:

- Two-level topology with Si IGBT/diode (*2L*-Si)
- Two-level topology with SiC MOSFET/Schottky diode (*2L*-SiC)
- Three-level T-type topology with Si IGBT/diode (*3LT*-Si)
- Three-level T-type topology with SiC MOSFET/Schottky diode (*3LT*-SiC)

The three-phase based configuration of these four device-topology combinations are shown in Figure 2-1.



(a) *2L*-Si
two-level structure with Si IGBT and Si diode

(b) *3LT*-Si
three-level T-type structure with Si IGBT and Si diode

(c) *2L*-SiC
two-level structure with SiC MOSFET/Schottky diode

(d) *3LT*-SiC
three-level T-type structure with SiC MOSFET/Schottky diode

Figure 2-1. Optional device-topology combinations in three-phase configuration

The *2L*-Si option is considered as the state-of-the-art industrial standard for benchmarking. Note the lower switch of the two-level phase leg is labeled as "T4" with reference to the T-type topology.

2.2 Operation of the ASR as a voltage source converter

In the target ASR system, the power converter is a three-phase, DC/AC, bidirectional VSC. Figure 2-2 shows a generic model of such a power converter.

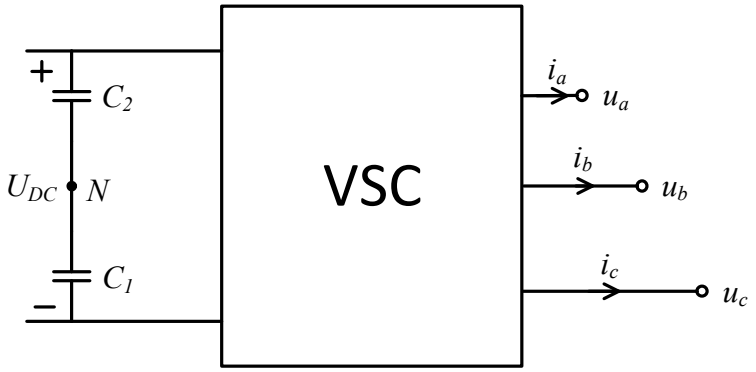


Figure 2-2. Generic model of a three-phase Voltage Source Converter

From the system point of view, the power converter is considered as a controllable voltage source generating

fundamental-frequency sinusoidal voltage superposed with high-frequency harmonics. The mathematical model of the power converter is expressed as (2-1) and (2-2) with regards to its output voltage and current at fundamental frequency.

$$\begin{cases} u_a = M \cdot \sin\theta \\ u_b = M \cdot \sin\left(\theta - \frac{2}{3}\pi\right) \\ u_c = M \cdot \sin\left(\theta + \frac{2}{3}\pi\right) \end{cases} \tag{2-1}$$

$$\begin{cases} i_a = I_m \sin(\theta - \varphi) \\ i_b = I_m \sin\left(\theta - \frac{2}{3}\pi - \varphi\right) \\ i_c = I_m \sin\left(\theta + \frac{2}{3}\pi - \varphi\right) \end{cases} \tag{2-2}$$

Where u_a, u_b, u_c are the fundamental-frequency phase reference voltages (in the range of −1 and +1); θ is the phase angle; M is the modulation index; $i_{a,b,c}$ are the three-phase load currents with the positive reference direction defined as flowing out from the power converter; φ is the power factor angle (lagging); I_m is the amplitude of the load currents. Note u_a, u_b, u_c are referenced to the DC-link neutral point N and they are also the reference voltages for the modulation. The phase output voltage (fundamental frequency) and load current of the converter are visualized in Figure 2-3. Note the power factor angle in the ASR system varies in the range of [−90°, +90°]. Considering the ideal operation of reactive power compensation shown in Figure 1-4, the ASR operates mostly at a zero power factor.

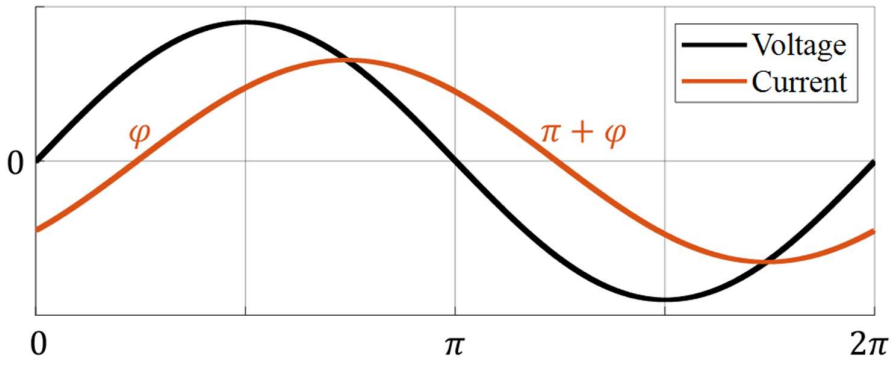


Figure 2-3. Phase reference voltage and load current of the power converter (fundamental frequency)

2.3 Analytical power loss modelling

In this section, a generic analytical power loss model is established based on the approach presented in [78]–[81]. The power losses of power devices consist of two mechanisms: conduction loss and switching loss. The following assumptions are made for simplicity in the analysis: 1. constant DC-link voltage 2. sinusoidal load current 3. the converter operates within the linear modulation region ($M \leq 1$). In the scope of this study, four types of power devices will be discussed: Silicon IGBT, Silicon Diode, SiC MOSFET and SiC Schottky Diode.

2.3.1 Conduction loss

The conduction loss is modelled by the *U-I* characteristic of a power device. For simplicity, the *U-I* characteristic of an IGBT/MOSFET/diode can be approximated by the form expressed in (2-3) in the conduction region.

$$u_{FW}(t) = U_{FW0} + R_{on} \cdot i(t) \tag{2-3}$$

Where u_{FW} is the instantaneous device forward voltage drop; U_{FW0} is the initial device forward voltage drop; R_{on} is the device on-state resistance; $i(t)$ is the instantaneous device current. Next, the instantaneous conduction loss of the power device P_{cond} is obtained as (2-4).

$$P_{cond}(t) = u_{FW}(t) \cdot |i(t)| \tag{2-4}$$

Over one fundamental cycle, one power device does not constantly conduct the current. The conduction loss of a power device can be expressed and averaged as (2-5).

$$P_{cond} = \frac{1}{2\pi} \cdot \int_0^{2\pi} g_{cond}(\omega t) \cdot u_{FW}(\omega t) \cdot |i(\omega t)| d\omega t \tag{2-5}$$

Where $g_{cond}(\omega t)$ is the conduction function, which is a piecewise function indicating the conduction intervals of a power device in one fundamental cycle. The conduction intervals for each single device will be analysed in the Section 2.4 and 2.5 for the four device-topology combinations.

2.3.2 Switching loss

The switching loss includes turn-on loss of the IGBT/MOSFET, the turn-off loss of the IGBT/MOSFET and the reverse-recovery loss of diodes. There are the following factors that affect the switching loss of a power device: (a) Switching voltage U_{sw} (b) Switching current I_{sw} (c) Temperature (d) Setup (DC-link parasitic inductance and gate driving circuit).

Considering the temperature and the setup kept constant, the switching loss is a function of switching voltage U_{sw} and switching current I_{sw}. The switching energies (in *mJ*) with reference to various switching current I_{sw} can be found from the manufacturer datasheet. The data showing E_{sw} vs. I_{sw} can be curve-fitted with a cubic function as in (2-6) with coefficients A, B and C. The effect of U_{sw} is considered linear regarding the base voltage U_{base} [79], which is the testing voltage of the switching energy.

$$E_{sw} = \frac{U_{sw}}{U_{base}}(A + B \cdot I_{sw} + C \cdot I_{sw}^2) \tag{2-6}$$

The switching loss (in power) over one fundamental cycle is calculated by adding up the switching energies of all n switching actions and averaging them over the fundamental period as

$$P_{sw} = \frac{1}{2\pi}\sum_{i=1}^{n} E_{sw,i}(i(\omega t)) \tag{2-7}$$

From the fundamental cycle point of view, the switching energy of each switching transition can be expressed as (2-8). Considering one power device does not constantly switch in each switching window, a piecewise function $g_{sw}(\omega t)$ is introduced to indicate the switch intervals of a power device over a fundamental cycle.

$$E_{sw\_avg} = \frac{1}{2\pi} \cdot \int_0^{2\pi} g_{sw}(\omega t) \cdot E_{sw}\big(i(\omega t)\big) d\omega t \tag{2-8}$$

The total averaged switching loss in power is obtained by multiplying the switching frequency f_{sw} and averaged switching energy for each transition.

$$P_{sw} = f_{sw} \cdot E_{sw\_avg} \tag{2-9}$$

Combining (2-6)-(2-9), an generic expression for the averaged switching loss is derived as

$$P_{sw} = f_{sw} \cdot \frac{1}{2\pi} \cdot \frac{U_{sw}}{U_{base}} \int_0^{2\pi} g_{sw}(\omega t) \cdot (A + B \cdot I_m \sin(\omega t - \varphi) + C \cdot I_m^2 \sin^2(\omega t - \varphi)) d\omega t \qquad (2\text{-}10)$$

2.3.3 Total converter loss

The total converter loss equals the sum of conduction losses and switching losses on all power devices.

$$P_{loss\_tot} = \sum (P_{cond} + P_{sw}) = \sum P_{cond} + \sum (P_{sw\_on} + P_{sw\_off} + P_{sw\_rr}) \qquad (2\text{-}11)$$

Where P_{sw_on}/P_{sw_off} are the switch-on/off power loss of IGBTs/MOSFETs; P_{rr} is the reverse recovery loss of the anti-parallel diodes.

For each power device, its conduction/switching intervals over one fundamental cycle are required for the formulas (2-5) and (2-10). The conduction/switching intervals of power devices depend on the following factors:

- Converter operating point: modulation index M and output power factor φ in (2-1) and (2-2)
- Topology: *2L* or *3LT*
- Modulation scheme: standard SPWM or non-standard modulation scheme
- Power devices: “Si IGBT + Si diode” or “SiC MOSFET + SiC Schottky diode”

The following sections derives the power loss model for various topology-device combinations based on standard Sinusoidal Pulse Width Modulation (SPWM).

2.4 Two-level converter with SPWM

A two-level converter outputs two voltage states: “+1” (positive DC rail, $+U_{DC}/2$) and “−1” (negative DC rail, $-U_{DC}/2$), as illustrated in Figure 2-4. In each switching window, the desired fundamental-frequency voltage is synthesised by the two available voltage levels.

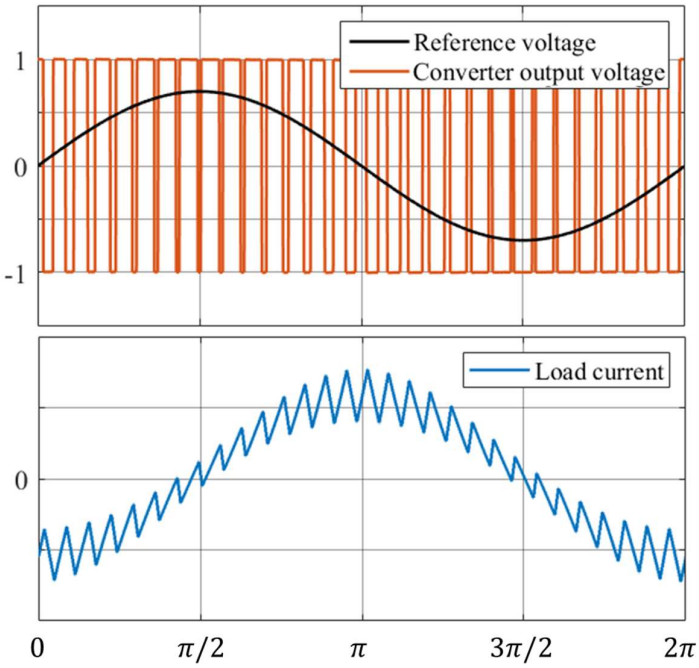


Figure 2-4. Voltage/current waveforms of a two-level phase leg with SPWM ($\varphi = \pi/2$)

The reference voltage, which is the fundamental-frequency sinusoidal voltage that the VSC generates, is normalized with reference to half the DC-link voltage as

$$u_{ref} = u_a \div \frac{U_{DC}}{2} \tag{2-12}$$

In angular domain, the instantaneous reference voltage of phase *a* can be expressed as

$$u_{ref} = Msin(\omega t) \tag{2-13}$$

The switching states of the two-level converter are achieved as shown in Table 2-1.

TABLE 2-1. SWITCHING STATES IN A TWO-LEVEL CONVERTER

State	U_{out}	T1	T4
"+1"	$+U_{DC}/2$	*ON*	*OFF*
"−1"	$-U_{DC}/2$	*OFF*	*ON*

From the power device point of view, the instantaneous output voltage (+1 or −1) determines whether the T1/D1 pair operates or the T4/D4 pair operates. The load current direction determines whether it flows through T1/D4 or D1/T4. An example of the conduction and commutation states of the *3LT* topology is illustrated in Figure 2-7. If the instantaneous load current $I > 0$, it either flows through T1 or D4. For example, T_1 conducts the load current when the load current is positive and output voltage is $+U_{DC}/2$.

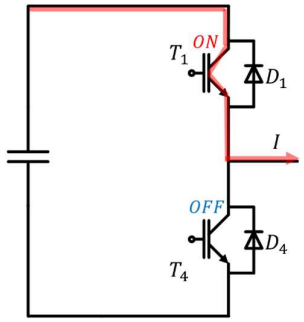
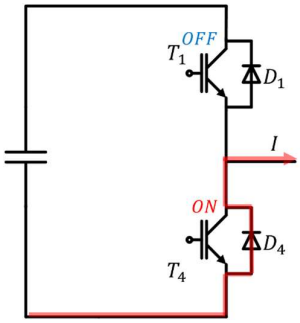
	"+1"	"−1"
I > 0		

Figure 2-5. Example of conduction and commutation states of the two-level topology (IGBT based)

In one switching window, the ON duty cycle of T_1/D_1 is calculated from the reference voltage in per unit.

$$D_{T1/D1} = (u_{ref} + 1)/2 = (Msin(\omega t) + 1)/2 \tag{2-14}$$

The ON duty cycle of T_4/D_4 is complementary to $D_{T1/D1}$ and hence derived as in (2-15).

$$D_{T4/D4} = 1 - D_{T1/D1} = (1 - Msin(\omega t))/2 \tag{2-15}$$

Based on these fundamental formulas and concepts, the analytical power loss model can be established for the *2L* topology with Si and SiC devices.

2.4.1 Two-level structure with Si IGBT and Si diode (*2L*-Si)

In a two-level converter with Si IGBT and Si diode, the conduction intervals of each power device can be obtained as follows. Taking T1 as an example, T1 conducts when the converter outputs state "+1" and the load current $I > 0$ at the same time. As illustrated in Figure 2-3, the load current is positive in the interval $[\varphi, \pi+\varphi]$. Within this range, the duty cycle of output state "+1" and subsequently the duty cycle of T1 in each switching window is calculated through (2-14). Thus, the conduction function of T1 is as (2-16).

$$g_{cond}(\theta) = \begin{cases} \big(1 + Msin(\omega t)\big)/2\,, & \theta \in [\varphi, \pi + \varphi] \\ 0\,, & \theta \notin [\varphi, \pi + \varphi] \end{cases} \tag{2-16}$$

Combining (2-5) and (2-16), the averaged conduction loss of T1 now can be derived as (2-17). It shows that the conduction loss of T1 depends on the converter operating point described by modulation index *M*, power factor *cos(φ)* and load current amplitude I_M.

$$P_{con,T1} = \frac{1}{2\pi} \cdot \int_{\varphi}^{\pi+\varphi} \left[\frac{1 + Msin(\omega t)}{2}\right] \cdot [U_{FW0} + R_{on} \cdot I_M \sin(\omega t - \varphi)] \cdot I_M \sin(\omega t - \varphi)\ dt \tag{2-17}$$

$$= \left(\frac{1}{8} + \frac{M\cos(\varphi)}{3\pi}\right) I_M^2 R_{on} + \left(\frac{1}{2\pi} + \frac{M\cos(\varphi)}{8}\right) I_M U_{FW0}$$

The conduction intervals of each power devices are found from the conduction states shown in Figure 2-5 and summarized in Table 2-2.

TABLE 2-2. DEVICE CONDUCTION FUNCTIONS (*2L*-SI)

	T1	D1	T4	D4
Conduction Condition	$U = +1$ $I > 0$	$U = +1$ $I < 0$	$U = -1$ $I > 0$	$U = -1$ $I < 0$
Conduction Interval	$\varphi \sim \pi + \varphi$	$0 \sim \varphi$ $\pi + \varphi \sim 2\pi$	$0 \sim \varphi$ $\pi + \varphi \sim 2\pi$	$\varphi \sim \pi + \varphi$
$g_{cond}(\theta)$	$\frac{1}{2}(1 + Msin(\omega t))$	$\frac{1}{2}(1 + Msin(\omega t))$	$\frac{1}{2}(1 - Msin(\omega t))$	$\frac{1}{2}(1 - Msin(\omega t))$

Next, the switching intervals are developed as follows with T1 and D4 as an example. In the interval [φ, $\pi+\varphi$], the load current is positive as illustrated in Figure 2-3. As shown in shown in Figure 2-5, T1 and D4 alternates to conduct this positive load current. When the commutation is from D4 to T1, a turn-on switching transition occur in T1 and a reverse-recovery transition occur in D4. When the commutation is from T1 to D4, a turn-off switching transition occurs in T1. The commutation associated switching loss energies are summarized in Table 2-3.

TABLE 2-3. SWITCHING LOSS ENERGIES (*2L*-SI)

Switching transition	Switching energies			
	$I \geq 0$		$I < 0$	
"+1"→ "−1"	$E_{on,\ D4}$	$E_{off,\ T1}$	$E_{on,\ T4}$	$E_{off,\ D1}$
"−1"→ "+1"	$E_{on,\ T1}$	$E_{off,\ D4}$	$E_{on,\ D1}$	$E_{off,\ T4}$

Hence, the switching interval function for T1 is found as (2-18).

$$g_{sw}(\theta) = \begin{cases} 1, & \theta \in [\varphi, \pi + \varphi] \\ 0, & \theta \notin [\varphi, \pi + \varphi] \end{cases} \tag{2-18}$$

Combining (2-10) and (2-18), the averaged switching loss of T1 now can be derived as (2-19).

$$\begin{aligned} P_{sw} &= f_{sw} \cdot \frac{1}{2\pi} \cdot \frac{U_{sw}}{U_{base}} \int_{\varphi}^{\pi+\varphi} \left(A + B \cdot I_m \sin(\omega t - \varphi) + C \cdot I_m^2 \sin^2(\omega t - \varphi)\right) d\omega t \\ &= \left(\frac{f_{sw}}{2\pi} \frac{U_{sw}}{U_{base}}\right) \times \left(A \cdot \pi + 2 \cdot B \cdot I_M + \frac{\pi C}{2} \cdot I_M^2\right) \end{aligned} \tag{2-19}$$

The switching intervals of all power devices in *2L*-Si case are identified and summarized in Table 2-4.

TABLE 2-4. DEVICE SWITCHING INTERVALS (*2L*-SI)

Devices	T1	D1	T4	D4
Switching Interval	$\varphi \sim \pi + \varphi$	$0 \sim \varphi$ $\varphi + \pi \sim 2\pi$	$0 \sim \varphi$ $\varphi + \pi \sim 2\pi$	$\varphi \sim \pi + \varphi$

Note the turn-on loss and the turn-off loss in an IGBT always occur in a pair in one switching window. Therefore, the turn-on loss E_{on} and turn-off loss E_{off} can be added up to E_{tot} to extract the coefficients A, B and C in (2-6) for an IGBT. The full expressions of the device power losses are given in Appendix A.1.1.

2.4.2 Two-level topology with SiC MOSFET + SiC Shottky Diode (*2L*-SiC)

In the case of all-SiC power devices, the power loss model must be altered. MOSFETs is able to conduct the load current in both positive and negative direction when the gate signal is ON. This feature can be utilised to reduce the conduction loss since the conduction characteristic of the MOSFET channel is superior than its body diode. The body diode suffers from both high conduction voltage drop and high reverse-recovery loss. The operation utilizing the MOSFET channel to conduct both positive/negative current is referred as "synchronous conduction" [52], [82]. For commercial SiC power modules, SiC Schottky diodes are installed to replace the body diodes as the anti-parallel diode to improve the performance [83]. The previous study has shown that the Schottky diode can share the load current with the MOSFET channel in the synchronous conduction [82] under high current conditions. For simplicity, with synchronous conduction implemented, it is assumed that all the conduction losses take place in the MOSFET channels as in [52], which neglects the deadtime conduction and current sharing effect.

The conduction loss model is adapted by modifying the conduction intervals of power devices as shown in Table 2-5. For example, in the *2L*-Si case, diode D1 conducts the current in the interval $[0, \varphi]$ and $[\pi+\varphi, 2\pi]$ when the converter outputs state "+1". Now in the *2L*-SiC case, the SiC MOSFET channel conducts both the positive and negative current, and therefore the conduction interval for T1 becomes $[0, 2\pi]$. The conduction intervals and modulation functions are listed in Table 2-5.

TABLE 2-5. DEVICE CONDUCTION INTERVALS (*2L*-SIC)

Devices	T1	T4
Conduction interval	$[0, 2\pi]$	$[0, 2\pi]$
$f(\omega t)$	$\frac{1}{2}(1 + Msin(\omega t))$	$\frac{1}{2}(1 - Msin(\omega t))$

Additionally, the initial voltage drop U_{FW0} of MOSFETs is zero. In this case, the expression of the conduction loss of switch T1 can be derived as

$$P_{con,T1} = \frac{1}{2\pi} \cdot \int_0^{2\pi} \left[\frac{1 + Msin(\omega t)}{2}\right] \cdot [R_{on} \cdot I_M \sin(\omega t - \varphi)] \cdot I_M \sin(\omega t - \varphi)\ dt = \frac{I_M^2 R_{on.T1/T4}}{4} \tag{2-20}$$

It can be noticed that (2-20) is not correlated to the power factor anymore comparing to the IGBT case (2-17) , which is confirmed in [52], due to the operation of synchronous conduction. The switching intervals in this case do not require changes since the commutation transitions stay the same due to the existence of the dead time. The full expressions of the device power losses are given in Appendix A.1.2.

2.5 Three-level converter with SPWM

A three-level converter structure outputs three voltage levels as illustrated in Figure 2-6: "+1" (positive DC rail, $+U_{DC}/2$); "−1" (negative DC rail, $-U_{DC}/2$); "0" (neutral point voltage). In each switching window, the desired fundamental-frequency voltage is synthesised by the two or three available voltage levels.

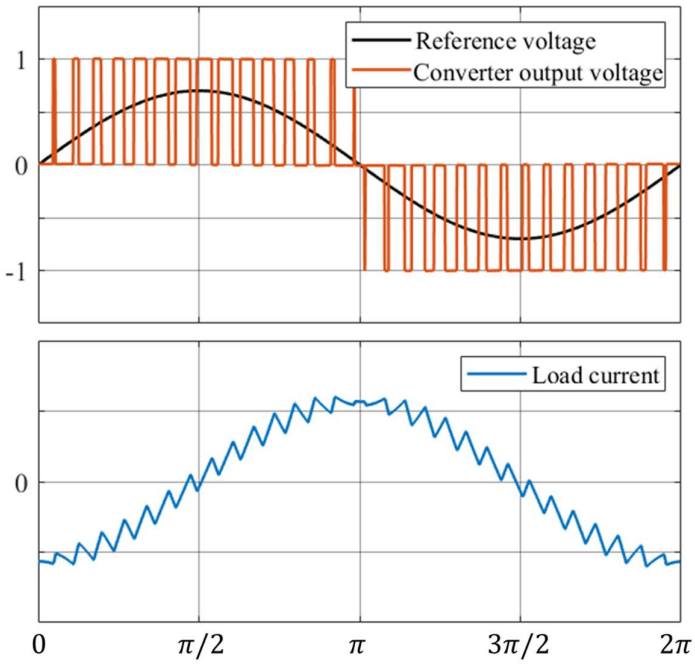


Figure 2-6. Voltage/current waveforms of a three-level phase leg with SPWM ($\varphi = \pi/2$)

In the three-level T-type converter, the switching states are shown in Table 2-6.

TABLE 2-6. SWITCHING STATES IN A THREE-LEVEL T-TYPE CONVERTER

State	U_{out}	T1	T2	T3	T4
"+1"	$+U_{DC}/2$	*ON*	*ON*	*OFF*	*OFF*
"0"	0 (U_{NP})	*OFF*	*ON*	*ON*	*OFF*
"−1"	$-U_{DC}/2$	*OFF*	*OFF*	*ON*	*ON*

When the *3LT* converter outputs "+1" or "−1", only one device conducts the load current, e.g. T1 or D1 or T4 or D4. When the *3LT* converter outputs "0", the load current is conducted by two power devices, e.g. T2 + D3 or T3 + D2. An example of the conduction and commutation states of the *3LT* topology is shown in Figure 2-7.

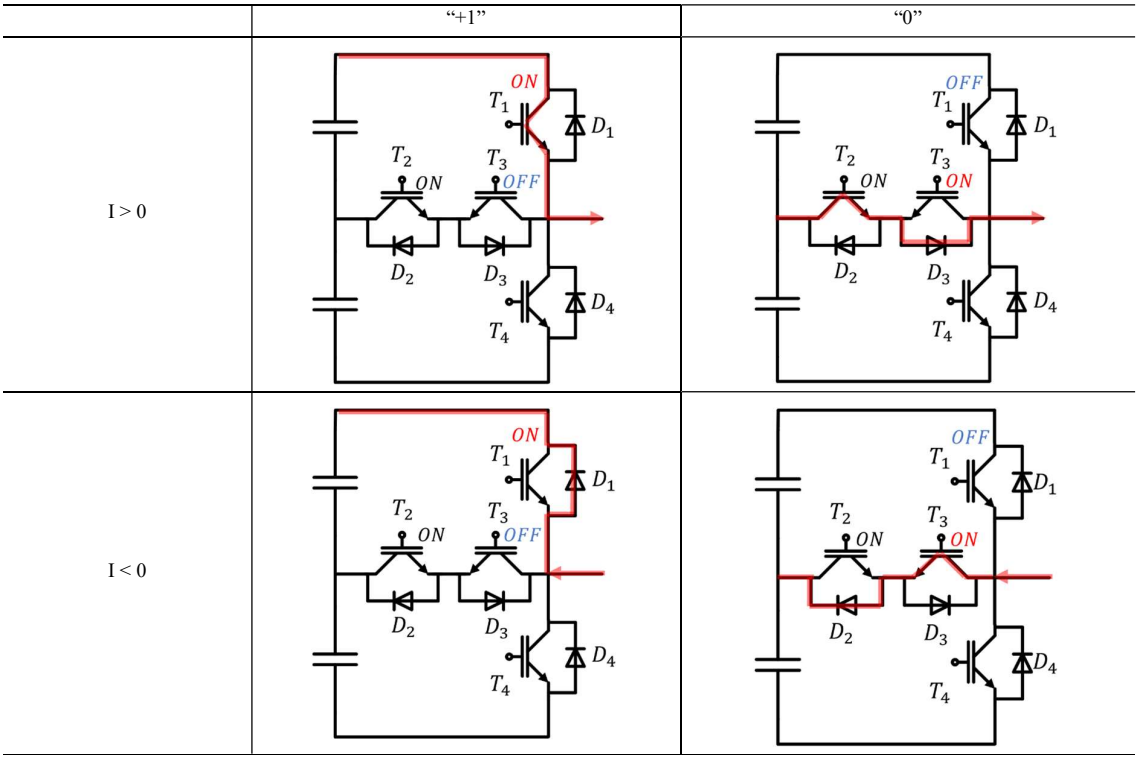


Figure 2-7. Example of conduction and commutation states of the three-level T-type topology ($U_{ref} > 0$, IGBT based)

In conventional SPWM, only two voltage levels are utilized in one switching window. When $U_{ref} > 0$, the converter output voltage jumps between "+1" and "0". When $U_{ref} < 0$, the converter output voltage jumps between "0" and "−1". With SPWM applied, the duty cycles of the output voltage levels are calculated through Table 2-7.

TABLE 2-7. OUTPUT VOLTAGE LEVELS IN 3L TOPOLOGY AND DUTY CYCLES WITH SPWM

	D_{+1}	D_{NP}	D_{-1}
$U_{ref} \geq 0$	$Msin(\omega t)$	$1 - Msin(\omega t)$	0
$U_{ref} \leq 0$	0	$1+ Msin(\omega t)$	$-Msin(\omega t)$

In this section, the analytical power loss model is established for the *3LT* topology. Due to the symmetry of the topology, only T1/D1 and T2/D2 need to be analysed.

2.5.1 Three-level T-type structure with Si IGBT and Si diode (*3LT*-Si)

In the *3LT*-Si, the conduction loss model is established as follows. Taking T1 as an example, T1 conducts when the converter outputs state "+1" and the load current $I > 0$ at the same time. Only in the interval $[\varphi, \pi]$, the load current is positive, and the converter reference voltage is positive (converter output voltage jumps between "+1" and "0"). Within this range, the duty cycle of T1 in one switching window is found from Table 2-7. Therefore, the conduction function of T1 is expressed as

$$g_{cond}(\theta) = \begin{cases} Msin(\omega t), & \theta \in [\varphi, \pi] \\ 0\,, & \theta \notin [\varphi, \pi] \end{cases} \tag{2-21}$$

Combining (2-5) and (2-21), the averaged conduction loss of T1 now can be derived as (2-22).

$$\begin{aligned} P_{con,T1} &= \frac{1}{2\pi} \cdot \int_{\varphi}^{\pi} Msin(\omega t) \cdot [U_{FW0} + R_{on} \cdot I_M \sin(\omega t - \varphi)] \cdot I_M \sin(\omega t - \varphi)\ dt \\ &= M\left(\frac{1}{6\pi} + \frac{\cos(\varphi)}{3\pi} + \frac{\cos(\varphi)^2}{6\pi}\right) I_M^2 R_{on} + M\left(\frac{\cos(\varphi)}{4} + \frac{\sin(\varphi)}{4\pi} - \frac{\varphi \sin(\varphi)}{4\pi}\right) I_M U_{FW0} \end{aligned} \tag{2-22}$$

Table 2-8 listed the conduction functions of the power devices in the *3LT*-Si configuration.

TABLE 2-8. DEVICES CONDUCTION FUNCTIONS (*3LT*-SI)

	T1	D1	T2		D2	
Conduction Condition	$I \geq 0$	$I < 0$	$I \geq 0$		$I < 0$	
	$U_{ref} \geq 0$ $U = +1$	$U_{ref} \geq 0$ $U = +1$	$U_{ref} \geq 0$ $U = 0$	$U_{ref} < 0$ $U = 0$	$U_{ref} \geq 0$ $U = 0$	$U_{ref} < 0$ $U = 0$
Conduction Interval	$\varphi \sim \pi$	$0 \sim \varphi$	$\varphi \sim \pi$	$\pi \sim \pi + \varphi$	$0 \sim \varphi$	$\pi + \varphi \sim 2\pi$
$g_{cond}(\theta)$	$Msin(\omega t)$	$Msin(\omega t)$	$1 - Msin(\omega t)$	$1 + Msin(\omega t)$	$1 - Msin(\omega t)$	$1 + Msin(\omega t)$

The switching functions for the *3LT*-Si configuration are developed as follows. An example is considered in the phase angle range $[\varphi, \pi]$ where the U_{ref} is positive and the load current is positive. In this case, two conduction path, T1 and T2+D3, alternate to conduct the load current as shown in Figure 2-7. When the commutation is from T1 to T2+D3 ("+1" to "0"), a turn-off loss occurs in T1 and a turn-on loss occurs in D3. Note there is no turn-on loss in T2 in this commutation, since T2 was previously ON due to the modulation states shown in Table 2-6. When the commutation is from T2+D3 to T1 ("0" to "+1"), a turn-on loss occurs in T1 and a turn-off loss occurs

in D3. The commutation associated switching loss energies are summarized in Table 2-9.

TABLE 2-9. SWITCHING LOSS ENERGIES (*3LT*-SI)

Switching transition			Switching energies			
			$I \geq 0$		$I < 0$	
"+1"	→	"0"	$E_{\text{on, D3}}$	$E_{\text{off, T1}}$	$E_{\text{on, T3}}$	$E_{\text{off, D1}}$
"0"	→	"+1"	$E_{\text{on, T1}}$	$E_{\text{off, D3}}$	$E_{\text{on, D1}}$	$E_{\text{off, T3}}$
"−1"	→	"0"	$E_{\text{on, T2}}$	$E_{\text{off, D4}}$	$E_{\text{on, D2}}$	$E_{\text{off, T4}}$
"0"	→	"−1"	$E_{\text{on, D4}}$	$E_{\text{off, T2}}$	$E_{\text{on, T4}}$	$E_{\text{off, D2}}$

Subsequently, the switching intervals for all power devices can be found summarized in Table 2-10.

TABLE 2-10. DEVICE SWITCHING INTERVALS (*3LT*-SI)

Devices	T1	D1	T2	D2
Switching Interval	$\varphi \sim \pi$	$0 \sim \varphi$	$\pi \sim \varphi + \pi$	$\pi + \varphi \sim 2\pi$

Hence, the switching interval function for T1 is found as (2-18).

$$g_{sw}(\theta) = \begin{cases} 1, & \theta \in [\varphi, \pi] \\ 0, & \theta \notin [\varphi, \pi] \end{cases} \tag{2-23}$$

Combining (2-10) and (2-23), the averaged switching loss of T1 in *3LT*-Si now can be derived as

$$\begin{aligned} P_{sw} &= f_{sw} \cdot \frac{1}{2\pi} \cdot \frac{U_{sw}}{U_{base}} \int_{\varphi}^{\pi} \left(A + B \cdot I_m \sin(\omega t - \varphi) + C \cdot I_m^2 \sin^2(\omega t - \varphi)\right) d\omega t \\ &= \left(\frac{f_{sw}}{2\pi} \frac{U_{sw}}{U_{base}}\right) \times \left[\left(\frac{\pi}{2} - \frac{\varphi}{2} + \frac{\cos(\varphi)\sin(\varphi)}{2}\right) C \cdot I_M^2 + (1 + \cos(\varphi)) B \cdot I_M + (\pi - \varphi) A \right] \end{aligned} \tag{2-24}$$

The full expressions of the device power losses are given in Appendix A.2.1.

2.5.2 Three-level T-type structure with SiC MOSFET + SiC Shottky Diode (*3LT*-SiC)

Applying the principles elaborated in Section 2.4.2, the loss model in the *3LT*-SiC case is altered based on the IGBT-based case derived in Section 2.5.1. The same assumption is made that all the conduction losses take place in the MOSFET channels as a result of the synchronous conduction operation. The altered conduction model of *3LT*-SiC case is shown in Table 2-11.

TABLE 2-11. DEVICES CONDUCTION FUNCTIONS (*3LT*-SIC)

	T1	T2	
Conduction Conditions	$U_{\text{ref}} \geq 0$ $U = +1$	$U_{\text{ref}} \geq 0$ $U = 0$	$U_{\text{ref}} < 0$ $U = 0$
Conduction Interval	$0 \sim \pi$	$0 \sim \pi$	$\pi \sim 2\pi$
$g_{cond}(\theta)$	$Msin(\omega t)$	$1 - Msin(\omega t)$	$1 + Msin(\omega t)$

The full expressions of the device power losses in *3LT-SiC* configuration are given in Appendix A.2.2.

2.6 Case study

Following the presented power loss model, the power losses of the converter can be calculated mathematically with the parameters of the power devices extracted from the datasheet (see Table 2-12). The switching energies can also be experimentally characterized over a local setup through Double Pulse Test (DPT) for better accuracy [52], [84].

TABLE 2-12. DEVICE CHARACTERISTICS EXTRACTED FROM DATASHEET (T_J = 150 °C)

		U_{FW0}	R_{on}	U_{FW} @78 A	E_{tot} [J] vs. I [A] $E_{tot} = E_{on} + E_{off}$ for IGBT/MOSFET, $E_{tot} = E_{rr}$ for diode				E_{tot} U_{DC} = 350V I = 78A
		V	mΩ	V	A	B	C	U_{base} [V]	mJ
CAS300M12BM2 U_{GS} = -5/+20 V $R_{Gon} = R_{Goff}$ = 2.5Ω	T1/T4	0	7.5	0.585	1.535e-3	2.106e-5	4.431e-8	600	2.01
	D1/D4	0.72	4.9	1.10	0	0	0	600	0
SKiM301TMLI12E4B U_{GE} = -15/+15 V $R_{Gon} = R_{Goff}$ = 2.7Ω	T1/T4	0.78	4.6	1.13	6.267e-3	5.914e-5	2.126e-8	300	6.42
	D1/D4	0.86	5.8	1.31	2.209e-3	-1.716e-6	-2.988e-10	300	1.2
	T2/T3	0.75	3.7	1.03	8.463e-3	2.043e-5	6.123e-8	300	6.08
	D2/D3	0.7	3.4	0.96	2.267e-3	-2.140e-6	2.704e-10	300	1.226

Based on the two selected power modules, there are following assumptions made for the loss calculation:

1. For *2L*-Si case, it is assumed that the devices T1/T4/D1/D4 have the same characteristics as the main arm switches T1/T4/D1/D4 in the selected T-type IGBT module SKiM301TMLI12E4B.
2. For *3LT*-SiC case, all the devices are assumed to be identical as T1/D1 in the selected two-level, all-SiC power module CAS300M12BM2.

The power losses among all power devices are firstly estimated for the two-level based options with the results plotted in Figure 2-8.

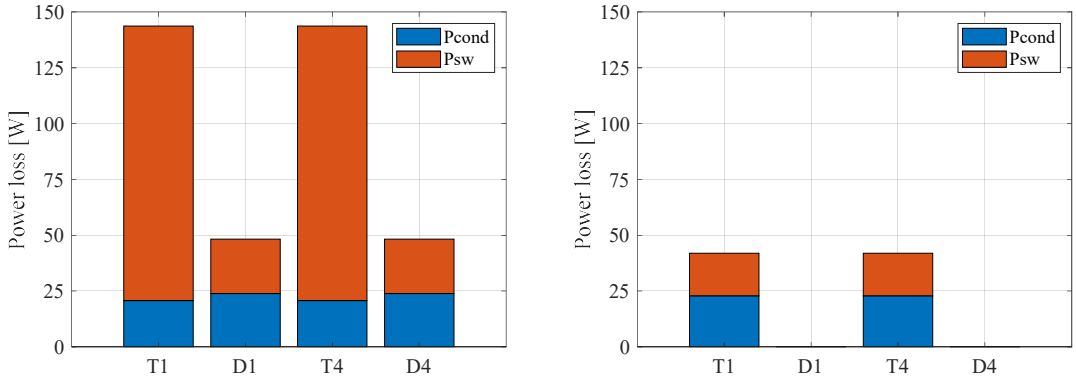


Figure 2-8. U_{DC} = 350 V, I_n = 78A, fsw = 20 kHz (a) *2L*-Si (b) *2L*-SiC

The following findings can be observed in Figure 2-8:

- In the Si case, the switching losses are substantial at *fsw* = 20 kHz. The majority power losses occur in the IGBTs (T1/T4).
- In the SiC case, the total power loss, the switching loss in particular, is much lower. Note due to the synchronous conduction and zero reverse-recovery loss in the SiC Schottky diode, there is little power losses occurring in the diodes (except for the conduction loss in deadtime)

In the case of *3LT* topology, the power losses over devices are shown in Figure 2-9. It can be seen that the peak power loss on a single power device in *3L-Si* is reduced compared to *2L-Si* (47 W instead of 143 W). Furthermore, under this operating point, the power losses in the middle arm switches T2/T3 are larger than the main arm switches (T1/T4).

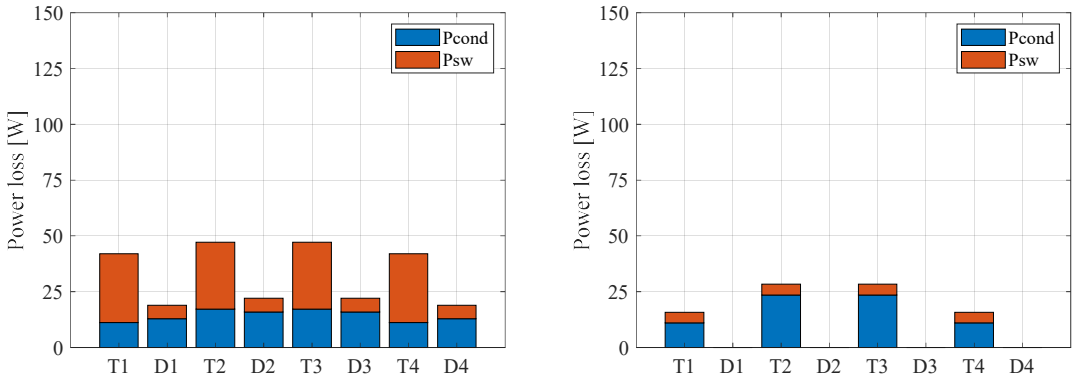


Figure 2-9. U_{DC} = 350 V, I_n = 78A, *fsw* = 20 kHz (a) *3LT*-Si (b) *3LT*-SiC

To compare the differences of the two topologies in discussion, the converter power loss of two investigated cases, *2L*-SiC and *3LT*-SiC, are plotted against the switching frequency as shown in Figure 2-10.

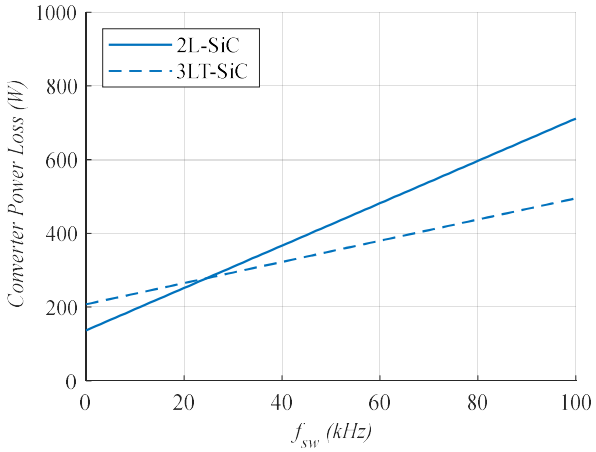


Figure 2-10. Converter power loss (*2L*-SiC and *3LT*-SiC) against *fsw*

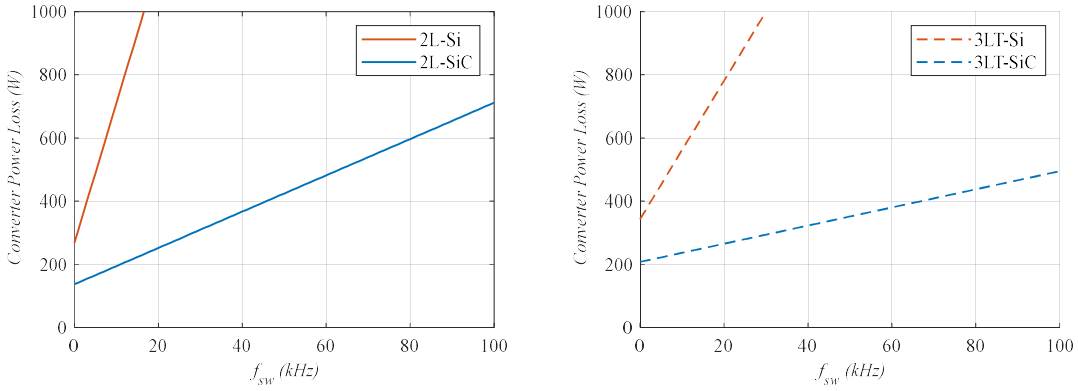
This graph is refered as the "power loss curve" of the converter. The power loss curve is in the form as

$$P_{loss} = P_{cond} + P_{sw}(f_{sw}) = P_{cond} + k_{sw} \cdot f_{sw} \tag{2-25}$$

Where P_{cond} is the conduction loss; k_{sw} is the switching loss factor, which is the gradient of the power loss curve. As can be seen from Figure 2-10, the conduction loss in the two-level converter is less than the three-level T-type converter. This is mainly due to the middle arm of the *3LT* converter formed by two power devices in series. When the load current is conducted by the middle arm (i.e. when the converter outputs voltage "0"), the conduction loss is the sum of two power devices, e.g. T2+D3 or D2+T3, which lead to a larger conduction loss.

It can also be seen that k_{sw} is smaller in the *3LT* case. This is the result of the halved switching voltage of the devices in the three-level topology compared to the two-level topology. This feature makes the three-level topology favourable when the design aim is to rise the switching frequency.

The intersection point in Figure 2-10 shows the switching frequency (around 27 kHz) where the total losses of two topologies are equal. For switching frequencies less than 27 kHz, the two-level topology has less total power loss due to smaller conduction loss. For higher switching frequencies, the three-level T-type topology offers less total power loss as a result of smaller switching loss factor k_{sw}. Figure 2-11 plots the power loss curve of four device-topology combinations focusing on the impact of power devices, Si versus SiC.



(a) *2L*-Si and *2L*-SiC (b) *3LT*-Si and *3LT*-SiC

Figure 2-11. Converter power loss against *fsw*

As Figure 2-11 shows, by replacing Si IGBT/Si Diode with all-SiC devices, the switching loss can be

substantially reduced due to the superior switching loss characteristics of the SiC devices. As Table 2-12 shows, the switching loss in SiC MOSFETs is substantially less than what in Si IGBTs. Additionally, SiC Schottkey diodes have zero reverse-recovery loss.

It can also be seen that the conduction loss is also reduced in the all-SiC case. For the rated current 78 Arms, the investigated SiC devices (T1 and D1) offers smaller forward voltage drop than the Silicon devices (T1 and D1) as shown in Table 2-12. Additionally, the use of "synchronous conduction" in the SiC cases further reduce the conduction loss. As shown in Table 2-12, the SiC MOSFET provides smaller forward conduction voltage drop than the SiC Schottky Diode.

The converter relative efficiencies for four investigated device-toplology combinations are plotted against the switching frequency as shown in Figure 2-12.

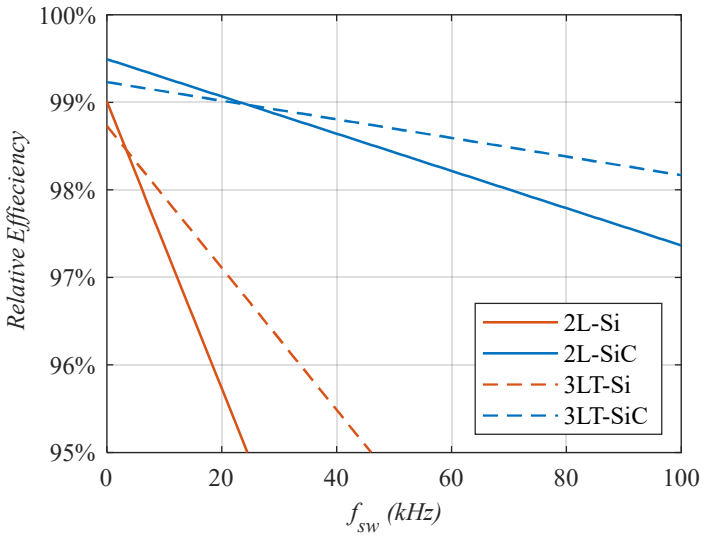


Figure 2-12 Converter relative efficiency against *fsw* considering power devices

As can be seen from Figure 2-12, for f_{sw} greater than 30 kHz, the *3LT*-SiC configuration offers the highest efficiency among all options. Up to 100 kHz, the two SiC based options can still maintain efficiencies of >97%. The efficiencies of the two Si based options drop steeply below 97% at 16 kHz for *2L-Si* and 20 kHz for *3LT-Si* respectively.

2.7 Summary

This chapter has evaluated the device power losses through analytical models for the four device-topology combinations. The analytical formulas are developed based on the operation principle of the converter topology. The analytical models provide quantified estimation of both the switching loss and conduction loss of each power device.

From the power device point of view, by replacing Si devices (IGBTs + diodes) with the emerging SiC devices (MOSFETs + diodes), the power losses of the converter can be substantially reduced due to the superior switching characteristics of SiC devices. Meanwhile, changing from a *2L* topology to *3LT* topology also reduce the ramp of switching loss against the increases of switching frequency, although *3LT* leads to slightly higher conduction loss due to the middle arm with two devices in series. The combination of SiC devices and *3LT* topology shows the best efficiency performance when the switching frequency is greater than 30 kHz.

From another angle, the use of SiC devices and *3LT* topology leads to less penalty in the efficiency and potential heatsink size when the converter operates at a high switching frequency (e.g. > 50 kHz). Operating at a high switching frequency will lead to the reduction of the filter components, which will be investigated in CHAPTER 4.

CHAPTER 3

Neutral Point Voltage Balancing in Three-level Converters

For three-phase, three-level converters, low-frequency Neutral Point (NP) voltage oscillation is an inherent problem of the topology [85]–[87]. The unbalanced NP voltage leads to low-frequency harmonics in the output voltage/currents and higher voltages for the DC-link capacitors and power devices to withstand [85]–[87]. Uncontrolled NP voltage may also cause instability of the converter control system [86]. Therefore, to utilize the three-level T-type topology in the target ASR system, the NP voltage oscillation issue must be addressed.

To suppress this NP voltage oscillation, one solution is to install larger DC-link capacitances [88]. However, increased DC-link capacitances lead to larger volume of the capacitors, especially in the case of film capacitors [89]. Larger DC-link capacitors are against the aim of optimizing the size of passive components in this work. This work intends to achieve a design with low DC-link capacitance, which mainly considers the high frequency voltage ripples. Therefore, if the low-frequency NP voltage oscillation needs to be suppressed by DC-link capacitors, the required capacitance can be substantially enlarged.

The alternative solution is to apply special modulation schemes to slightly change the operation of the power converter at high-frequency domain without compromising the basic functionality of it, i.e. outputting a desired fundamental-frequency voltage. This approach does not directly require additional hardware, which reduces the need of larger capacitors as a drawback in three-level converters to specifically counter the NP voltage oscillation. However, these special modulation schemes may result in impact of power losses of the power devices.

There are mainly two known modulation-based approaches to suppress the NP voltage oscillation. The conventional approach is Zero-sequence Signal Injection (ZSI) [47], [90], [91]. However, according to [47], [90],

[91], this approach is unable to effectively control the NP oscillation when the converter is operating at high modulation index and low power factor [85], [88]. This limitation becomes problematic for certain applications where the power converter operates over a wide range of power factor, e.g. [-90°, +90°], which is exactly the case for the target ASR system.

The alternative approach is a novel modulation strategy, Virtual Zero-level Modulation (VZM), which can eliminate the low frequency NP voltage oscillations over full power factor and modulation index range. The mechanism of VZM is fully utilizing the three available voltage levels in each switching window to gain extra controllability of the NP voltage. In principle, VZM is equivalent to Nearest-Three Virtual Space Vector (NTV^2) modulation [92], [93], "Disassembly of Zero Level" [94] and modulation strategy presented in [95], because they all utilize the three voltage levels on switching window basis to achieve the balancing.

This chapter investigates the NP voltage oscillation issue and elaborates the two available modulation solutions to address this problem.

The main content of this chapter has been presented by the author in the following publications:

- **J. Wang**, X. Yuan, Y. Zhang, K.J. Dagan, X. Liu, D. Drury, P.H. Mellor and A. Bloor, "Analytical Averaged Loss Model of Three-Phase T-type NPC STATCOM with Virtual Zero Voltage Level Synthesis Modulation," in *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.
- **J. Wang**, X. Yuan, K.J. Dagan, P.H. Mellor, D. Drury and A. Bloor, "Universal Neutral Point Balancing Algorithm for Three-phase Three-level Converters with Hybrid of Zero-sequence Signal Injection and Virtual Zero-level Modulation" in *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE),* 2018

3.1 Neutral point voltage oscillation in three-phase, three-level converters

The NP voltage oscillation can be considered as the result of a current i_{NP} drawn from the NP, as shown in Figure 3-1. This current is contributed by three phase legs in a three-phase system. The positive reference direction of i_{NP} is defined as flowing out from the neutral point. Whenever the output of a phase leg is clamped to the NP, the

load current is drawn from the NP.

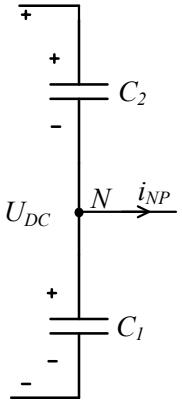


Figure 3-1. Illustration of the neutral point current i_{NP}

The NP voltage oscillation is defined as with reference to two DC-link capacitor voltages.

$$U_{NP} = U_{C1} - \frac{U_{C1} + U_{C2}}{2} \tag{3-1}$$

From the NP current point of view, two capacitors are treated virtually in parallel [87]. The deviation of u_{NP} over a period of time T is determined by i_{NP} and the DC-link capacitances as expressed in (3-2), assuming two capacitors are identical ($C = C1 = C2$).

$$\Delta u_{NP} = \frac{i_{NP} \cdot T}{2C} \tag{3-2}$$

The operation principles of a three-level, three-phase converter have been elaborated in Section 2.5. Following Table 2-7, the duty cycles of phase x ($x = a,b,c$) can be re-written in (3-3)-(3-5) calculated from the reference voltage of phase x U_x that is defined in (2-1).

$$D_{+1x} = \begin{cases} U_x, if\ U_x > 0 \\ 0, if\ U_x \leq 0 \end{cases} \tag{3-3}$$

$$D_{-1x} = \begin{cases} -U_x, if\ U_x < 0 \\ 0, if\ U_x \geq 0 \end{cases} \tag{3-4}$$

$$D_{NPx} = 1 - D_{+1x} - D_{-1x} \tag{3-5}$$

Next, the average NP current over one switching period can be found from (3-6) contributed by three phases, where $i_{a,b,c}$ are the load currents.

$$i_{NP} = i_a D_{NPa} + i_b D_{NPb} + i_c D_{NPc} \tag{3-6}$$

Substituting (2-1), (2-2) and (3-3)-(3-5) into (3-6), the expression of average i_{NP} in the case of SPWM can be derived as (3-7) as a function of phase angle θ.

$$i_{NP}(\theta) = I_m \begin{bmatrix} \sin(\varphi-\theta)\left(\left|M\sin(\theta)\right|-1\right) \\ +\sin\left(\varphi-\theta+\frac{2}{3}\pi\right)\left(\left|M\sin\left(\theta-\frac{2}{3}\pi\right)\right|-1\right) \\ -\sin\left(\theta-\varphi+\frac{2}{3}\pi\right)\left(\left|M\sin\left(\theta+\frac{2}{3}\pi\right)\right|-1\right) \end{bmatrix} \tag{3-7}$$

With SPWM applied in a three-phase system, the current flowing out from the neutral point i_{NP} is in the shape of Figure 3-2 shows from the fundamental-frequency point of view.

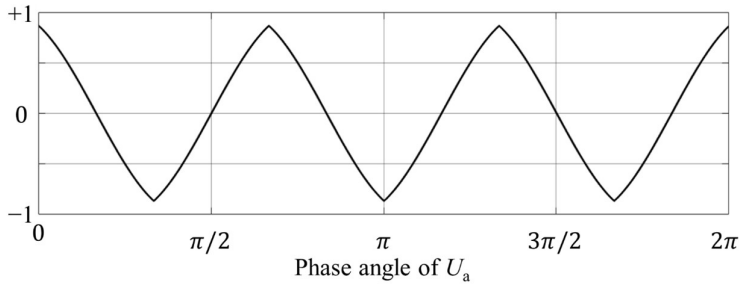


Figure 3-2. Example of uncontrolled, filtered neutral point current normalized to peak load current (M = 1, φ = 90°)

It can be seen that the frequency of the periodical NP current is three times the fundamental frequency. This NP current causes the $3f_0$ voltage oscillation at the DC-link neutral point. If the fundamental frequency is 400 Hz, the NP current frequency and associated NP voltage oscillation is at 1200 Hz.

Following [87], a normalized amplitude of the NP voltage oscillation is defined as (3-8) to quantify the issue across various systems against a base value that is associated with the fundamental-frequency f_0, the load current I_{rms} and the capacitance C.

$$\Delta U_{NP\_norm} = \frac{\Delta U_{NP}}{\Delta U_{NP\_base}} = \Delta U_{NP} \div \frac{I_{rms}}{f_0 \cdot C} \tag{3-8}$$

Where ΔU_{NP} is the peak-to-peak value of NP voltage deviation. According to previous research [47], the ΔU_{NP_norm} can reach 0.08 at the worst-case operation of the power converter, which is at the full modulation index and zero power factor. If the capacitors need to suppress the low-frequency ($3f_0$) neutral point oscillation to 1% of the DC-link voltage, the required capacitance C is 445.7 µF, which leads to 891.4 µF installed capacitance at the DC-link.

As a comparison, the DC-link capacitance sized in Section 4.1 to attenuate the switching-frequency voltage ripple at 1% U_{DC} is only 40 μF when the converter operates at 40 kHz. This comparison means the DC-link capacitance needs to be enlarged by a factor of 11 in this case due to the low-frequency oscillation. Additionally, the DC-link capacitance targeting high-frequency ripples can be even further reduced by operating the converter at a higher f_{sw} (see equation (4-5)), while the fundamental frequency is fixed at 400 Hz for the target system.

Alternatively, modulation schemes can be applied to balance the NP voltage. As the control subject, the desired NP current i^*_{NP} in each switching cycle is expressed in (3-9), which is rearranged from (3-2). This reference NP current i^*_{NP} can drag the NP voltage deviation ΔU_{NP} back to zero within one switching window.

$$i^*_{NP} = \Delta U_{NP} \cdot f_{sw} \cdot 2C \tag{3-9}$$

Thus, the NP voltage can be balanced by forcing the NP current to track the desired value on switching window basis through the modulation schemes. As introduced, there are mainly two degrees of freedom in the modulation to achieve this goal, which are Zero-sequence Signal Injection (ZSI) and Virtual Zero-level Modulation (VZM).

3.2 Zero-sequence Signal Injection (ZSI)

The injection of zero-sequence signal is the conventional approach to suppress the NP voltage oscillation. The principle of ZSI is to inject a zero-sequence signal into the reference voltages of all three phases at the same time, as expressed in (3-10). The injected zero-sequence signal will be cancelled out and not show in the output line-to-line voltages.

$$\begin{cases} U_{a\_ZSI} = U_a + U_{ZSI} \\ U_{b\_ZSI} = U_b + U_{ZSI} \\ U_{c\_ZSI} = U_c + U_{ZSI} \end{cases} \tag{3-10}$$

The allowable range of U_{VZI} is constrained by keeping the modified reference voltages, U_{abc_ZSI} within the linear modulation range ($|U| \leq 1$). Therefore, the upper and lower boundaries of U_{VZI} (U_{ZSI_low} and U_{ZSI_up}) are defined by (3-11).

$$U_{ZSI\_up} = 1 - \max(U_a, U_b, U_c)$$
$$U_{ZSI\_low} = -1 - \min(U_a, U_b, U_c) \tag{3-11}$$

The effect of injected zero-sequence signal U_{ZSI} regarding the neutral point voltage/current is not straightforward [96], as it changes D_{NP_a}, D_{NP_b} and D_{NP_c} in (3-6) all together at the same time. Therefore, an optimal searching based approach is illustrated in Figure 3-3 to utilize ZSI to balance the NP voltage, which is developed based on the approach presented in [96]. This simplified approach searches the optimal U_{VZI} by trials (iterations) within the allowable range (3-11) in each switching window. Each attempt yields a theoretical NP current after control $I_{np\_trial\_nth}$. The optimal U_{ZSI} is the one leads to the closest value $I_{np\_trial\_nth}$ with respect to the desired NP current. In this way, the selected U_{VZI} will force the converter to track the desired NP current i^*_{NP} as close as possible on switching window basis. When the trial step is sufficiently small, the selected U_{VZI} can be considered the optimal towards the control objective – balancing the NP voltage.

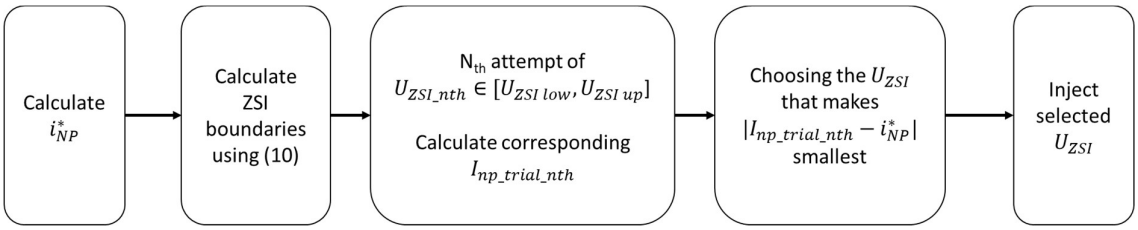


Figure 3-3. Process of ZSI to balance the neutral point voltage

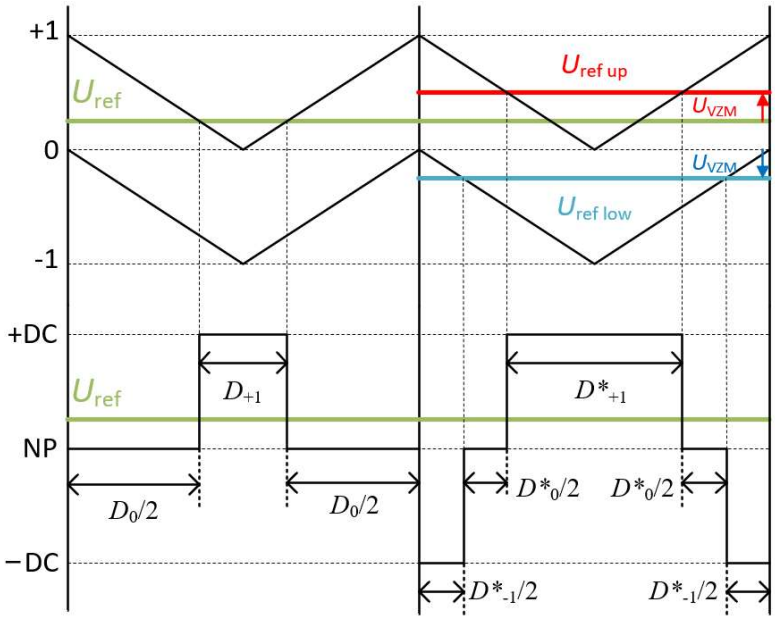
However, as the limitation of this approach, even when the optimal U_{VZI} is selected, ZSI still loses the controllability over the NP voltage at a high modulation index and a lower power factor [42].

3.3 Virtual Zero-level Modulation (VZM)

3.3.1 Principles of NP voltage balancing based on VZM

As another degree of freedom, the controllability of NP current can be gained with VZM by controlling one individual D_{NP_x} in (3-6), instead of all three of them at the same time. In principle, VZM is realized by replacing part of the output zero-level with "virtual" zero-level synthesized by "+1" and "−1", as shown in Figure 3-4, which maintains the same output volt-time area of this switching window. This operation doubles the switching

transitions in one switching window, i.e. four instead of two.



(a) (b)

Figure 3-4. Multilevel-carrier-based modulation ($U_{ref} > 0$) (a) SPWM (b) VZM

A strategy using VZM to balance the NP voltage is shown in Figure 3-5. The balancing strategy was originally proposed in [95]. This work further refines and simplifies this strategy to achieve more straightforward understanding and easier implementation in practical.

As proven in [95], only one phase leg needs to switch between three voltage levels in each switching window to eliminate the low-frequency NP oscillation. This phase is referred as the dominant phase y which can be manipulated most effectively for the voltage balancing purpose. Phase y is selected by the logic shown in Figure 3-5, which is a simplified logic based on [95].

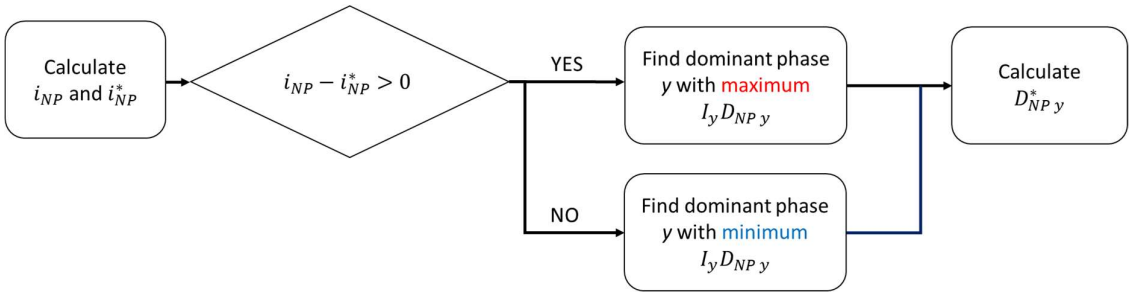


Figure 3-5. Strategy of using VZM to balance the neutral point voltage

The NP duty cycle of this phase D_{NP_y} will be manipulated following (3-12) to force the NP current to track the desired value i^*_{NP}.

$$D^*_{NP\_y} = \frac{\left[i^*_{NP} - \left(i_{NP} - i_y D_{NP\_y}\right)\right]}{i_y} \tag{3-12}$$

The boundaries of D_{NP_y} are given in (3-13), which ensures the volt-time area in each switching window unaffected and the modified reference voltage to remain within the linear modulation range. Firstly, the direct control objects are the duty cycles, which need to be equal to/greater than zero and be smaller than one. Secondly, as noticeable from Figure 3-4, the NP duty cycle can only be reduced by VZM, which means the modified D'_{NP_y} must be smaller than the unmodified D_{NP_y}.

$$0 \le D'_{NP_y} < D_{NP_y} \tag{3-13}$$

Therefore, the ideally reference $D^*_{NP\_y}$ are trimmed by these constraints to obtain an achievable D'_{NP_y} prior to the following algorithm to avoid unreasonable commands. $D^*_{NP\_y}$ can be unreasonable when the NP voltage deviation is too large, e.g. in the start-up stage of the converter, because in principle it attempts to pull back the deviation in only one switching window. Once an achievable D'_{NP_y} is found, the modified duty cycles of state "+1" and state "-1" can be calculated by

$$\begin{aligned} D'_{-1\_y} &= \frac{1}{2}\left(1 - D'_{NP\_y} - U_{ref}\right) \\ D'_{+1\_y} &= 1 - D'_{NP\_y} - D'_{-1\_y} \end{aligned} \tag{3-14}$$

For level-shifted carrier-based modulation, VZM is realized by three stages:

(I) Split the original reference modulating waves U_{ref} to two parts using (3-15);

$$U_{up} = \begin{cases} U_{ref},\ if\ U_{ref} > 0 \\ 0,\ if\ U_{ref} \le 0 \end{cases} \text{ and } U_{low} = \begin{cases} 0,\ if\ U_{ref} > 0 \\ U,\ if\ U_{ref} \le 0 \end{cases} \tag{3-15}$$

(II) Calculate a compensation signal $U_{VZM} > 0$ with (3-16) based on desired D'_{NP_y};

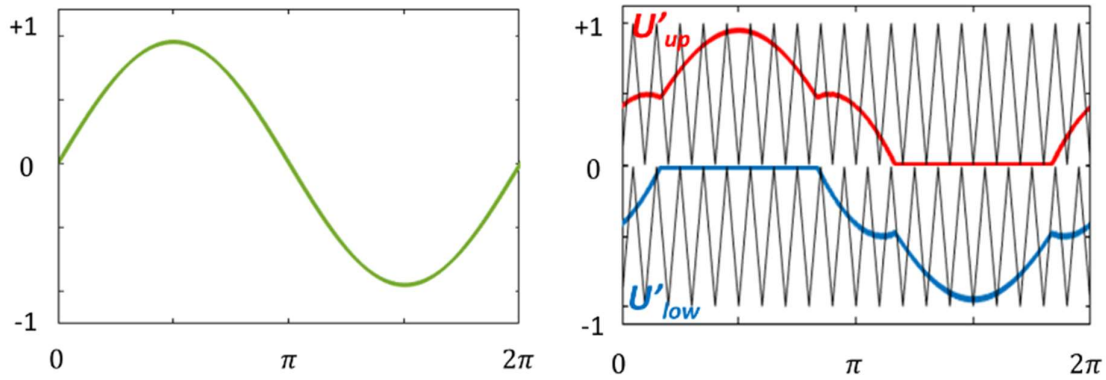
$$U_{VZM} = (D_{NP\_y} - D'_{NP\_y})/2 \tag{3-16}$$

(III) Inject the calculated to $U_{VZM} > 0$ both modulating waves of the dominant phase y following (3-17);

$$\begin{cases} U'_{up\_y} = U_{up\_y} + U_{VZM} \\ U'_{low\_y} = U_{low\_y} - U_{VZM} \end{cases} \tag{3-17}$$

(IV) Feed the modified modulating waves into multilevel carriers to generate the PWM gate signals.

Figure 3-6 shows the reference voltage signal before and after the alteration by VZM strategy. Note if $U_{VZM} = 0$, the split of modulating signals does not make any difference compared to the original modulating wave. It should be noted that the sum of U'_{up} and U'_{low} equals to original U, which means this VZM injection does not alter the output volt-time area defined by the original reference voltage.



(a) (b)

Figure 3-6. Modulating waves (a) original SPWM (b) Split modulating waves with U_{VZM} injected

3.3.2 Case study

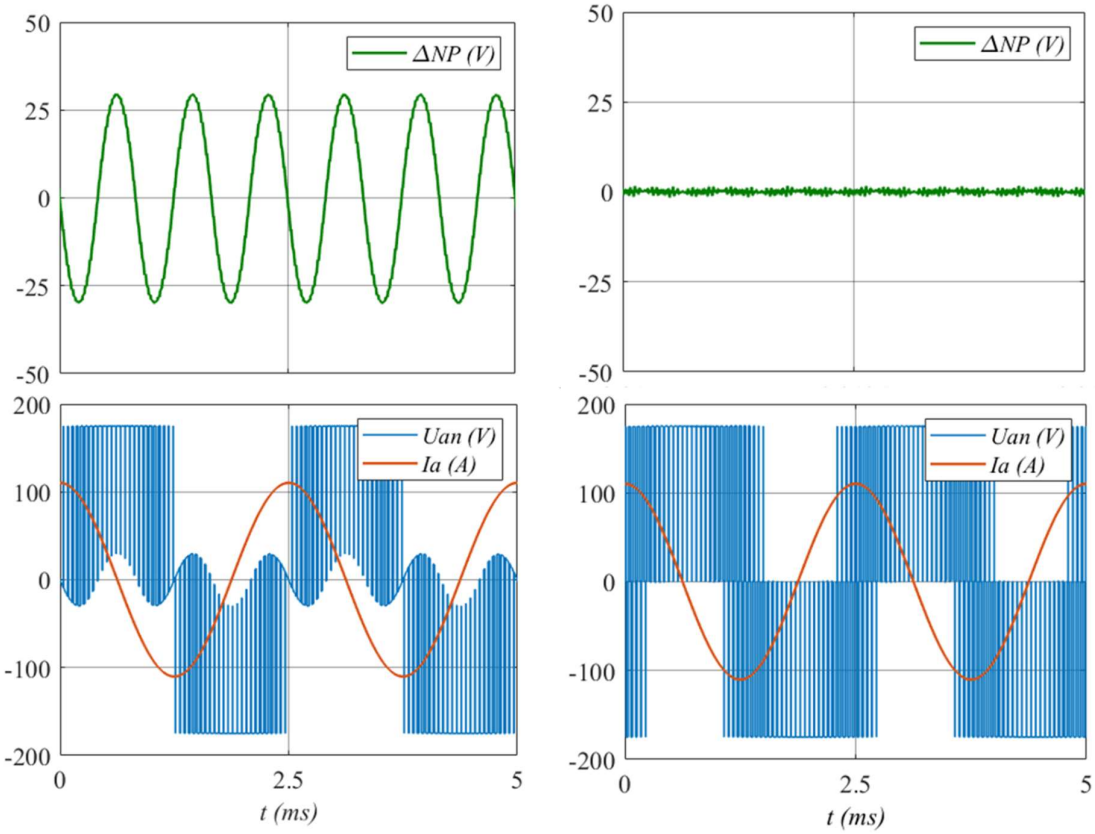
A case study is conducted on the ASR system to validate the performance of VZM in a simulation model built in Matlab/Simulink. The specifications of this system are presented in Table 3-1.

TABLE 3-1. SPECIFICATIONS OF A STATCOM SYSTEM

Power Rating	27 kVA	Converter Output	78 Arms
DC-link Voltage	350 V	Power factor *cos(φ)*	0 (lagging)
Switching frequency	20 kHz	Grid frequency	400 Hz
Modulation Index	0.97	DC-link Capacitance	C1 = C2 = 180 μF

The waveforms of the studied converter system in the simulation are plotted in Figure 3-7. It is visible that VZM is able to effectively suppress the NP voltage oscillation when the system operates at a high modulation

index and low power factor.



(a) SPWM (b) VZM

Figure 3-7. Simulation waveform of the three-phase three-level system

3.4 Analytical loss model with VZM

As introduced, VZM results in doubling the switching transitions and alteration of the output voltage levels on switching window basis. Therefore, it is motivated to investigate the quantified impact on power losses brought by this novel control scheme based on the power loss model introduced in CHAPTER 2.

Plotted from simulation, Figure 3-8 shows the the simulated reference voltage, load current, NP current (low-frequency) and VZM activation region over a fundamental cycle, when $\varphi = \pi/2$ (lagging).

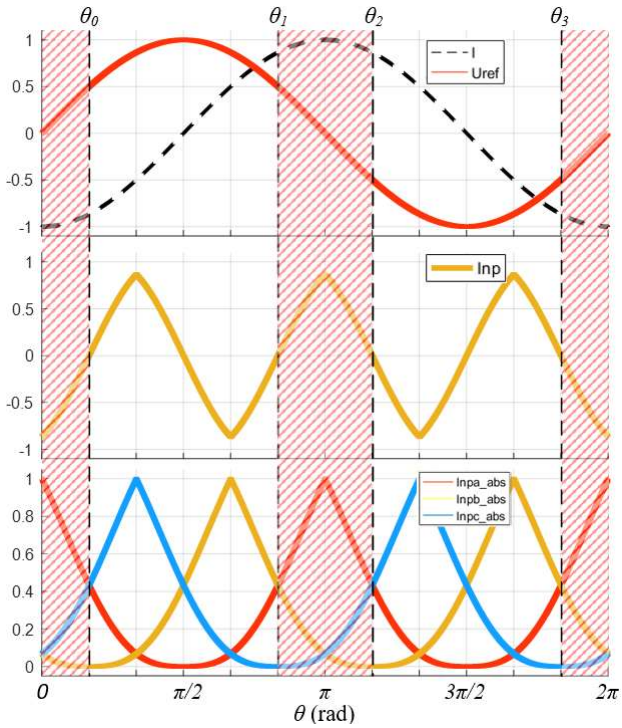


Figure 3-8. VZM activated intervals when $\varphi = \pi/2$

As can be observed, the NP current and VZM activated region shows a periodical pattern (shadowed area in Figure 3-8). For each phase leg, the VZM activated regions only account for 1/3 of the fundamental period and are formed by two 60° intervals with a 120° break in between. Taking *Phase A* as an instance, when $\varphi = \pi/2$ lagging, the VZM activated regions are [0, π/6], [5π/6, 7π/6] and [11π/6, 2π], where *Phase A* is detected as the dominant phase for the NP balancing scheme in Figure 3-5. Define θ_0 as the NP current phase angle. By numerical approximation, θ_0 is found from (3-7) for various power factor angles and visualized in Figure 3-9.

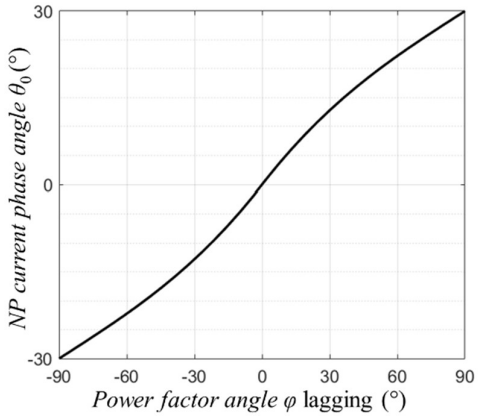


Figure 3-9. NP current angle θ_0 as a function of power factor angle φ (lagging)

Next, θ_1, θ_2 and θ_3 can be found by (3-18) to fully constrain the VZM activation region.

$$\theta_1 = \theta_0 + \frac{2}{3}\pi;\ \theta_2 = \theta_0 + \pi;\ \theta_3 = \theta_0 + \frac{5}{3}\pi; \tag{3-18}$$

Following the approach presented in Section 2.5, the conduction intervals and switching transitions are re-analysed when VZM is applied as follows.

3.4.1 *3LT*-Si configuration

The analysis firstly starts with the *3LT*-Si case. Taking shadowed interval [5π/6, 7π/6] in Figure 3-8 as an example, where the VZM is activated for phase *A*, the converter's output voltage jumps between +1/0/−1. When the load current is positive, the conduction loss is in T1 when outputting +1, T2+D3 when outputting 0 and D4 when outputting −1. The switching loss occurring in this interval is the switch-on and switch-off loss of T1+T2 and reverse recovery loss of D3+D4. This means T1 would have extra conduction interval and switching interval between [π, 7π/6] compared to the SPWM case.

The device conduction intervals, corresponding duty cycles and switching intervals are summarised in Table 3-2 and Table 3-3. The duty cycles in SPWM regions, $g_{cond\_SPWM}(\theta)$, are the same as Table 2-7. The duty cycles in VZM regions, $g_{cond\_VZM}(\theta)$, are calculated by (3-14) with the assumption that $i^*_{NP} = 0$ for VZM activated operation. Note the assumption $i^*_{NP} = 0$ stands for ideal steady-state operation that the initial NP voltage deviation is zero.

TABLE 3-2. DEVICE CONDUCTION INTERVALS APPLYING VZM (*3LT*-SI)

	T1	D1	T2	D2	
SPWM Conduction Interval	$[\varphi, \theta_1]$	$[\theta_0, \varphi]$	$[\varphi, \theta_1]$ $[\theta_2, \pi+\varphi]$	$[\theta_0, \varphi]$	$[\pi+\varphi, \theta_3]$
$g_{cond\_SPWM}(\theta)$	D_{+1}	D_{+1}	D_{NP}	D_{NP}	
VZM Conduction Interval	$[\theta_1, \theta_2]$	$[0, \theta_0]$ $[\theta_3, 2\pi]$	$[\theta_1, \theta_2]$	$[0, \theta_0]$ $[\theta_3, 2\pi]$	
$g_{cond\_VZM}(\theta)$	D'_{+1_y}	D'_{+1_y}	D'_{NP_y}	D'_{NP_y}	

TABLE 3-3. DEVICE SWITCHING INTERVALS APPLYING VZM (*3LT*-SI)

	T1	D1	T2	D2
Switching interval *SPWM*	$[\varphi, \pi]$	$[0, \varphi]$	$[\pi, \pi+\varphi]$	$[\pi+\varphi, 2\pi]$
Switching interval *VZM*	$[\pi, \theta_2]$	$[\theta_3, 2\pi]$	$[\theta_1, \pi]$	$[0, \theta_0]$

3.4.2 *3LT*-SiC configuration

In the case of all-SiC power devices, the conduction intervals of the devices need to be altered as explained in Section 2.4.2. Due to the use of "synchronous conduction", SiC MOSFET channel conducts the load current in both positive and negative direction. Therefore, all the conduction losses take place in the MOSFET channels, with the deadtime neglected for simplicity. In this case, the model needs to be adapted accordingly by moving the conduction intervals of D1/D2 onto T1/T2, while the switching intervals stay the same. The altered conduction intervals and duty cycles for *3LT*-SiC case is summarized in Table 3-4.

TABLE 3-4. DEVICE CONDUCTION INTERVALS APPLYING VZM (*3LT*-SIC)

	T1	T2	
SPWM Conduction Interval	$[\theta_0, \theta_1]$	$[\theta_0, \theta_1]$	$[\theta_2, \theta_3]$
$g_{cond\_SPWM}(\theta)$	D_{+1}	D_{NP}	
VZM Conduction Interval	$[0, \theta_0]$ $[\theta_1, \theta_2]$ $[\theta_3, 2\pi]$	$[0, \theta_0]$ $[\theta_1, \theta_2]$ $[\theta_3, 2\pi]$	
$g_{cond\_VZM}(\theta)$	D'_{+1_y}	D'_{NP_y}	

3.4.3 Case study

A case study is conducted the ASR system to evaluate the impact on device power losses due to VZM. Taking the *3LT-SiC* configuration at f_{sw} = 10 kHz as an example, a comparison of power loss between SPWM and VZM is calculated through the proposed model and presented in Table 3-5.

TABLE 3-5. COMPARISON OF TOTAL CONVERTER POWER LOSS (T-TYPE, SIC, 10 KHZ)

	SPWM	VZM	Difference (VZM/ SPWM)
Conduction	217 W	176 W	−18.9%
Switching	28 W	41 W	+ 46.4%
Total	246 W	217 W	− 11.8%

As expected, the switching loss increases by 46.4 % when VZM is applied due to extra switching transitions. However, the conduction loss with VZM shows a reduction of 18.9%. This is because VZM reduces the use of the NP voltage level as explained in Section 3.3, which leads to the re-routing of the current from the middle arm (T2/D2/T3/D3) to the main arm (T1/D1/T4/D4) for an overall longer period in each fundamental cycle. When the output is clamped to NP voltage, the current flows through two devices (T2+D3 or T3+D2). When the output is +1 or −1, the current flows through only one device instead (T1/D1/T4/D4), which leads to lower conduction loss.

Overall, the total power loss applying VZM shows a reduction in this studied case. This is due to the relatively low switching frequency and high load current in this case, which makes the conduction loss dominant among the total power loss.

Figure 3-10 plots the variation of total converter power loss versus switching frequency. In the *3LT*-Si case, it can be found that, when the switching frequency is below approximately 5 kHz, VZM reduces the total power loss compared to SWPM due to the reduced conduction loss; from 5 kHz onwards, the switching loss starts to become the major part and the total power loss applying VZM will exceed SPWM. The point of intersection at 5 kHz is where two modulation schemes give equal total power loss. When the devices are replaced with all-SiC devices, the trend is similar and the intersection moves to around 33 kHz due to the smaller switching losses.

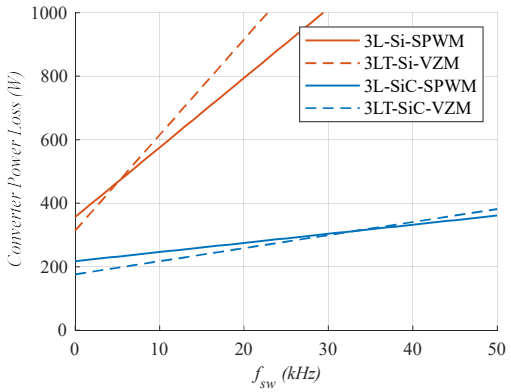


Figure 3-10. Converter power loss vs. switching frequency

3.4.4 Exprimental verification

An experimental setup is built to verify the proposed power loss model and a picture of it is shown in Figure 3-11. It is formed by DC-link stage, converter stage and load stage. To replicate the low power factor operation, a three-phase inductor with star-connection is connected as the load. In this configuration, the power converter operates at a low power factor at nearly 90 degrees lagging. Three load currents and two DC-link capacitor voltages are sensed and fed to the Digital Signal Processor (DSP) board for the NP balancing algorithm. A power analyzer is used to measure the output real power of the power converter P_{AC}. A DC power supply EA-PS 8500-

30 is connected to the DC-link to provide a stable DC-link voltage with an output power of P_{DC}.

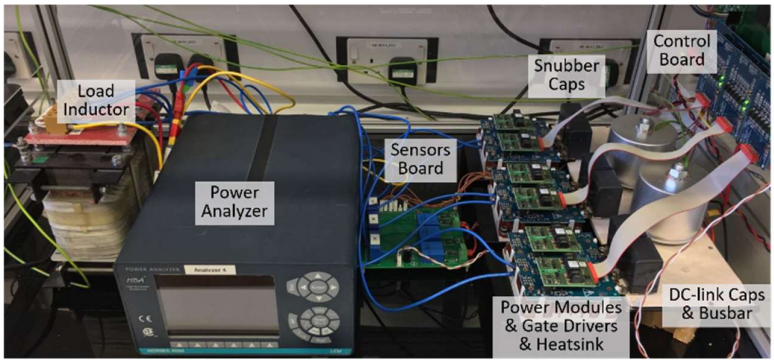


Figure 3-11. Test Rig 1

In this configuration, the power loss occurs in the power conversion stage can be obtained as in (3-19).

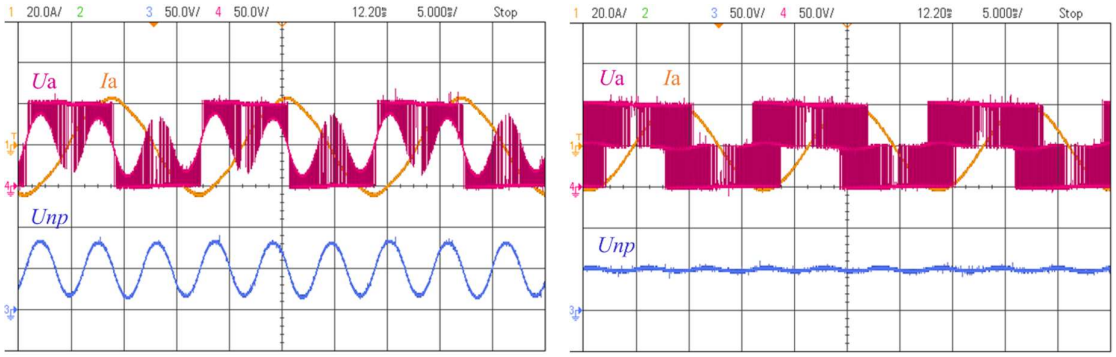
$$P_{loss} = P_{DC} - P_{AC} \tag{3-19}$$

The specifications of the downscaled test rig are presented in Table 3-6. A deadtime of 2 μs is implemented between T1 and T4 to avoid the shoot-through.

TABLE 3-6. SPECIFICATIONS OF DOWNSCALED TEST RIG

DC-link Voltage	100 V	Modulation Index	0.9
Load Current	13.1 Arms	Power device	SKiM301TMLI12E4B from Semikron
Power angle φ	86.5° (lagging)	DC-link Capacitance	$C_1 = C_2 = 220$ μF
Fundamental frequency	60 Hz	Load inductance	6.23 mH per phase

The output waveforms of the test rig are captured and presented in Figure 3-12. As can be seen, VZM effectively suppresses the amplitude of NP voltage oscillation from 70 volts to 6 volts (peak-to-peak). Due to the existence of the deadtime and the delay in the control circuit, the low-frequency NP voltage oscillation is not completely removed in this case. But this can be improved by optimizing the control circuit and the algorithm.



(a) SPWM (b) VZM

Figure 3-12. Experimental waveforms
*U*a as the phase output voltage; *I*a as the phase current and U_{NP} as the neutral point voltage $M = 1$, $\varphi = \pi/2$, $f_{sw} = 10$ kHz

The power loss measurements of the converter are plotted in Figure 3-13, with a comparison with the

estimation. As the graph shows, the experimental results (circles and solid lines) show good consistency with the estimated curves (dashed lines) within the uncertainty of measurement. In higher frequency region, the measured power loss is slightly greater than the estimated value. The possible causes of the discrepancy are:

- Deviated VZM activated region due to the delay of control
- Inaccuracy in the testing of switching energies
- Power losses in the DC-link busbars and DC-link capacitors.

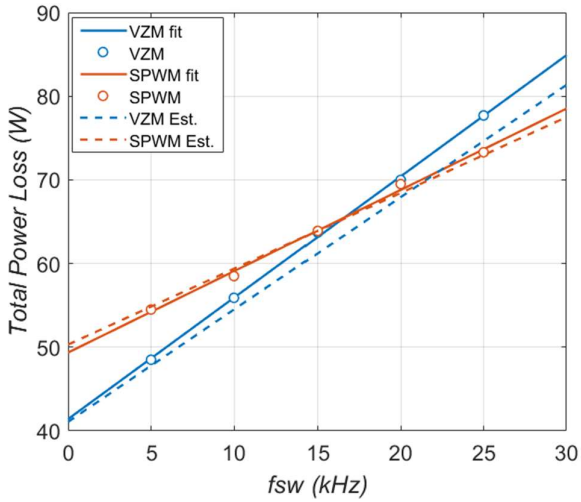


Figure 3-13. Experimental converter power loss vs. theoretical estimation (T = 25°C)

3.5 Hybrid Voltage Balancing Scheme

As analysed in Section 3.4, VZM increases the switching loss significantly due to the extra switching transitions, although it reduces the conduction loss at the same time due to the reduced use of the middle arm formed by two power devices. In the case of high-voltage, low-current, high-switching-frequency power electronics systems, the switching loss is the main contributor of converter power loss, where the drawback of VZM becomes significant. Additionally, VZM also increases the high-frequency harmonics [95]. Therefore, it is undesirable to activate VZM constantly, especially when ZSI is capable already to suppress the NP oscillation.

Following this motivation, a novel carrier-based voltage balancing scheme is proposed in this section, which

is a hybrid of ZSI and VZM. To utilize these two degrees of freedom, a logic coordinating the use of VZM and ZSI is developed and implemented. To minimize the main drawback of VZM, i.e. the increased switching loss, VZM is only activated when necessary. This whole algorithm aims at providing a simple and universal carrier-based solution for the NP balancing issue that can easily be implemented in digital controllers.

3.5.1 Principles of novel NP voltage balancing scheme

A top-level process of proposed scheme is shown in Figure 3-14.

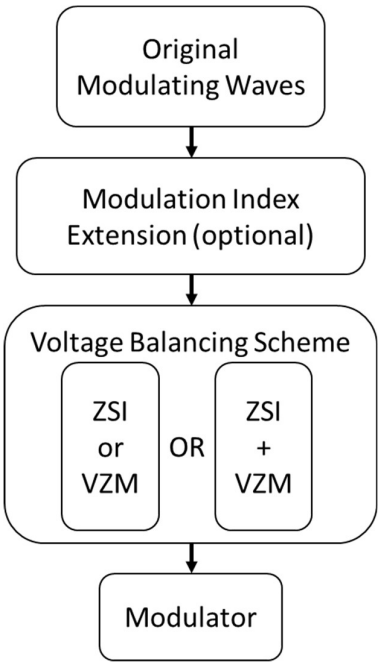


Figure 3-14. Top-level control scheme

The original sinusoidal modulating waves firstly go through an optional step for the extension of modulation index (from maximum 1 to 1.15) by injecting a zero-sequence third-order harmonic. An option of this zero-sequence signal is (3-20) as used in [95].

$$U_{off} = -\frac{[\max(U_a, U_b, U_c) + \min(U_a, U_b, U_c)]}{2} \tag{3-20}$$

Next, the modulating waves go through the voltage balancing block and finally are fed into the modulator to generate gate signals. The detailed process of NP balancing block is presented in Figure 3-15.

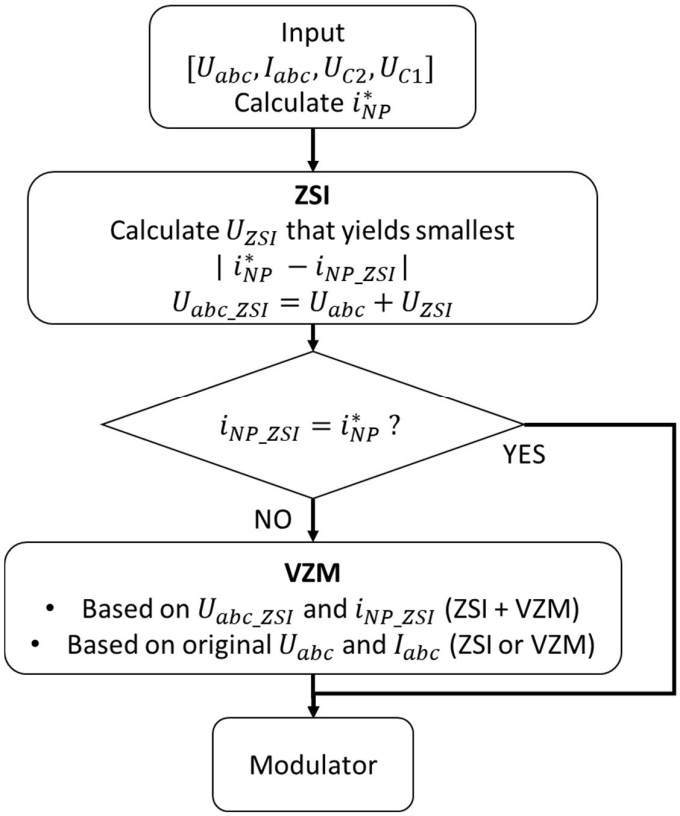


Figure 3-15. Proposed hybrid voltage balancing scheme

In this scheme, the ZSI block and the VZM block are placed in series. The ZSI block acts as the first-stage compensation and yields the altered reference voltages U_{abc_ZSI} and the compensated i_{NP_ZSI} by calculation. Then these variables are fed into the VZM block for a second-stage compensation and yields the final altered reference voltages for the generation of gate signals.

Between the first stage and second stage, a judgement step is placed comparing the ZSI compensated i_{NP_ZSI} and desired i^*_{NP}. If i_{NP_ZSI} equals to i^*_{NP}, it means the control objective is already satisfied by ZSI, and VZM at the second stage will be bypassed. This step ensures that the activation of VZM is reduced and only activated when needed. In practice, due to limited decimal precision and number of iterations, it is more feasible to set a threshold value (e.g. $| i_{NP\_ZSI} - i^*_{NP}| < 0.01$ p.u.) as the criteria, rather than strictly requiring $i_{NP\_ZSI} - i^*_{NP} = 0$. From another angle, this threshold value can be treated as sacrificing controllability in exchange for less power loss. The larger the threshold value is, the less VZM will be used, resulting in less power loss and higher NP voltage oscillation.

When the judgement step indicates that ZSI cannot satisfy the control objective, there are two options for the following action as shown in Figure 3-6: (1) Discard the calculated U_{ZSI} and activate VZM based on original U_{abc}, for which the balancing scheme is referred as "ZSI or VZM"; (2) Keep the alterations made by ZSI stage and activate VZM on top of modified modulating waves U_{abc_ZSI}, which is referred as "ZSI + VZM". The differences of these two options will be evaluated through simulation regarding the dynamic performance in the next section.

3.5.2 Performance evaluation by simulation

The proposed voltage balancing scheme is implemented in Matlab/Simulink on the ASR system with the parameters listed in Table 3-7.

TABLE 3-7 SIMULATION PARAMETERS OF THE ASR SYSTEM

Power Rating	27 kVA	Current	78 Arms
DC-link Voltage	350 V	DC-link Capacitance	C1 = C2 = 180 μF
Switching frequency	20 kHz	Fundamental frequency	400 Hz
Modulation Index	0 ~ 1.15	Power Factor φ	**[-90°, +90°]**

Firstly, the steady-state voltage balancing performance of the proposed scheme is evaluated over various power factor and modulation index. The results are shown in Figure 3-16 and Figure 3-17.

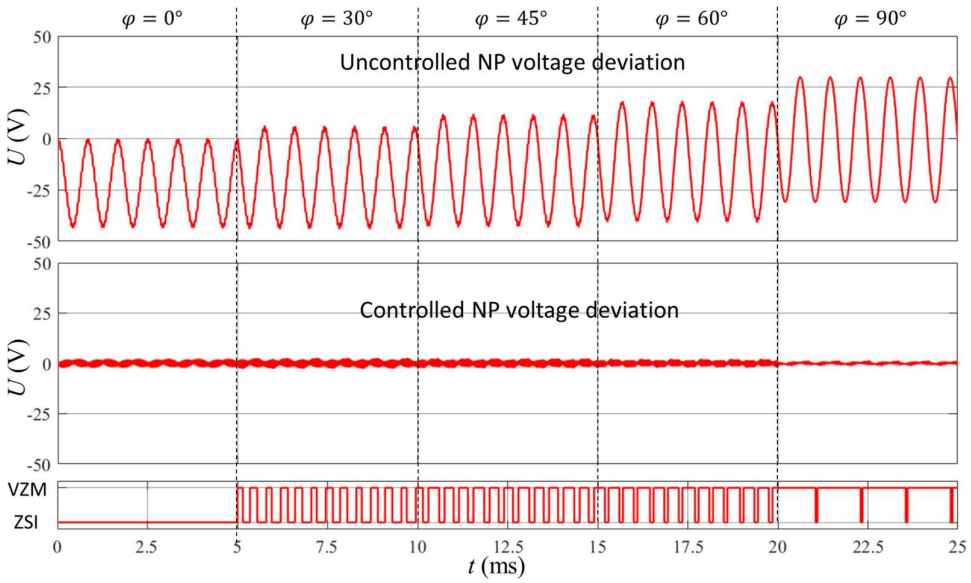


Figure 3-16. Uncontrolled NP voltage; controlled NP voltage; switching between ZSI and VZM, M = 1 with sinusoidal modulating waves

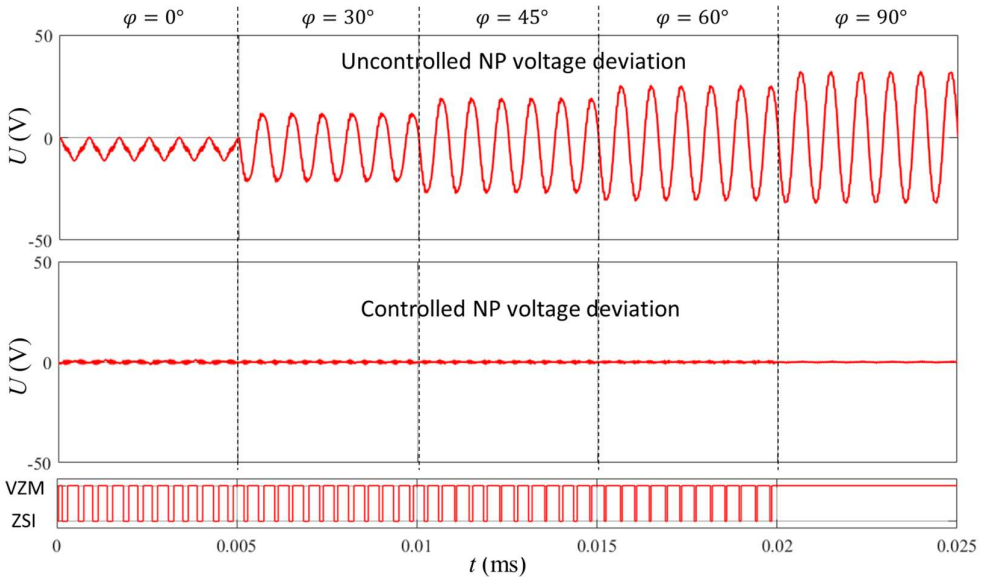


Figure 3-17. Uncontrolled NP voltage; controlled NP voltage; switching between ZSI and VZM, M = 1.15 with modulation index extension (3-20)

As the simulation results show, the proposed algorithm is effective in eliminating the low-frequency NP oscillation over full power factor range, without undermining the achievable modulation index (M = 1 for SPWM and M = 1.15 for extended modulation index). Note when the power factor equals 90°, the VZM mode will be always activated as shown in Figure 3-16 and Figure 3-17. This confirms the conclusion from previous studies that ZSI loses the NP controllability at low power factor.

The performances of "ZSI or VZM" or "ZSI + VZM" are also compared in simulation. Given an initial unbalance of voltages, the balancing performance of the two options are evaluated and presented in Figure 3-18.

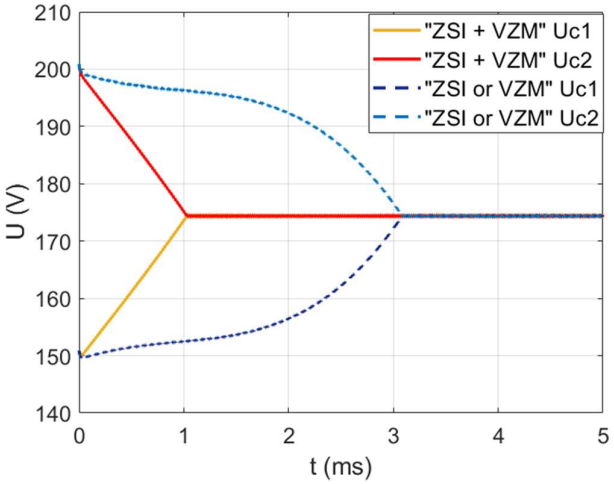


Figure 3-18. Dynamic balancing performace, "ZSI + VZM" vs. "ZSI or VZM" M = 0.9, φ = 30°, with modulation index extension (3-20)

As shown in the figure, the unbalance of capacitor voltages can be successfully compensated by both options. It is visible that "ZSI + VZM" offers quicker dynamic performance compared to "ZSI or VZM". This can be explained by their achievable controllability region regarding NP current.

The controllability regions of NP current by applying ZSI, VZM and proposed hybrid scheme (ZSI+VZM) can be analysed as follows:

- For ZSI, the achievable NP current is obtained by recording all trial NP current in Figure 3-3.
- For VZM, it can be assumed that there is no dead time, which means D^*_{NP} in (3-12) of one phase can be completely reduced to zero. Therefore, the max/min achievable NP current is obtained by removing the min/max phase term from (3-6).
- For proposed hybrid scheme "ZSI + VZM", in each trial incident of ZSI control, it is followed by removing one of the phase terms to find the final achievable NP current of this trial.

The controllability region of three schemes are analysed and plotted in Figure 3-19, with the controlled NP current normalized to peak load current. The larger colored area indicates the better controllability and quicker dynamic performance regarding NP current. For example, when $U_{C2} < U_{C1}$, a positive NP current is desirable to drag down the NP voltage. In this case, a larger NP current will be able to achieve the control objective in a shorter period.

As Figure 3-19 shows, by applying the proposed hybrid scheme ("ZSI + VZM"), the controllability region (red area) is expanded compared to either ZSI or VZM. This explains the faster dynamic performance gained by this hybrid balancing scheme which utilizes the two degrees of freedom at the same time. In Figure 3-19, it is also noticeable that ZSI scheme loses bidirectional controllability when φ equals 90°. This analysis confirms again that the ZSI cannot suppress the NP oscillation in the case of a lower power factor and a high modulation index.

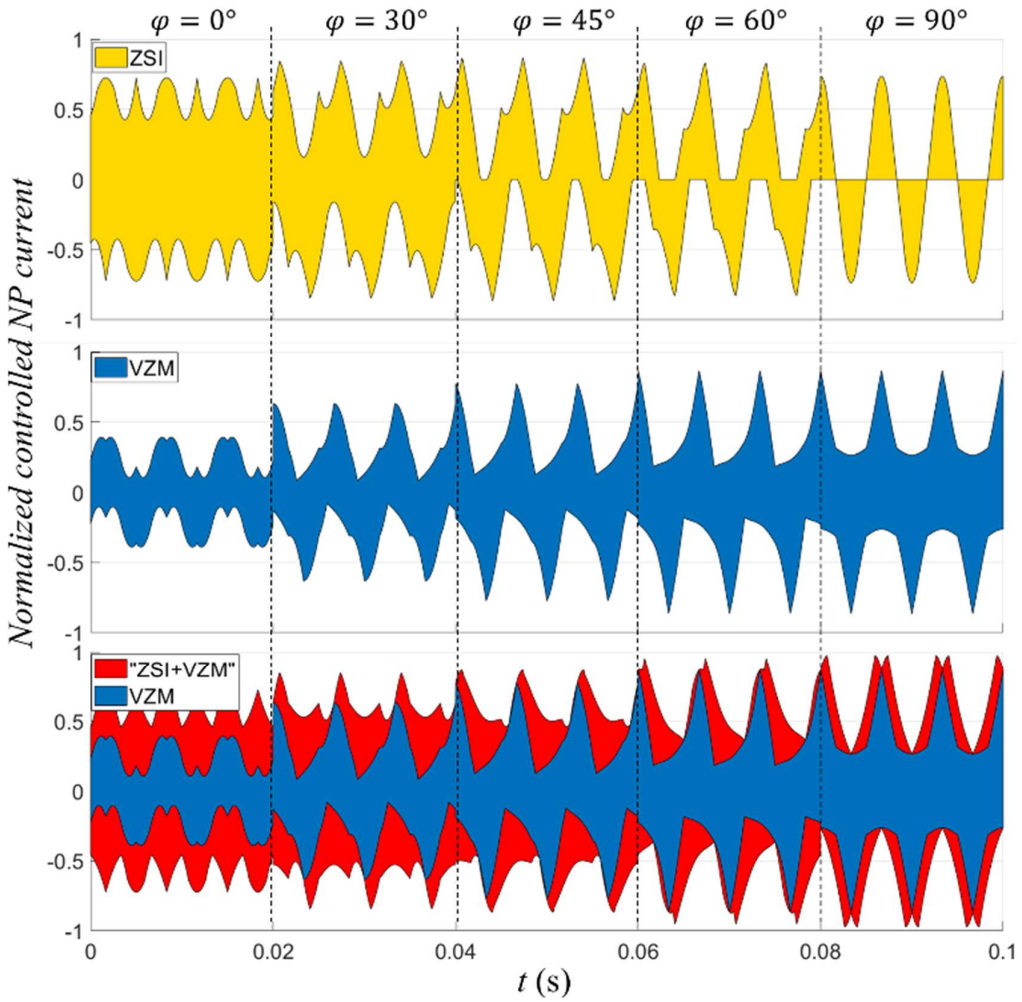


Figure 3-19. Achievable NP current under various control schemes, M = 0.85
with modulation index extension (3-20)

Note there is no PI/PID controller required in this hybrid control scheme. Hence it can be easily implemented in digital controller with reduced tuning process of parameters.

3.5.3 Experimental verification

To verify and evaluate the proposed control scheme, a downscaled test rig is built with the components listed in Table 3-8. The control scheme is programmed in a DSP, TMS320F28335.

TABLE 3-8. COMPONENTS IN THE DOWNSCALED TEST RIG 2

DC-link voltage supply	Elektro-Automatik TS 8000 T	Power Analyzer	Norma 4000
Power device	SKiM301TMLI12E4B from Semikron	Load inductance	6.23 mH per phase
DC-link Capacitance	$C_1 = C_2 = 220$ µF	Load resistance	2.2 Ω per phase

A picture of the test rig is shown in Figure 3-20.

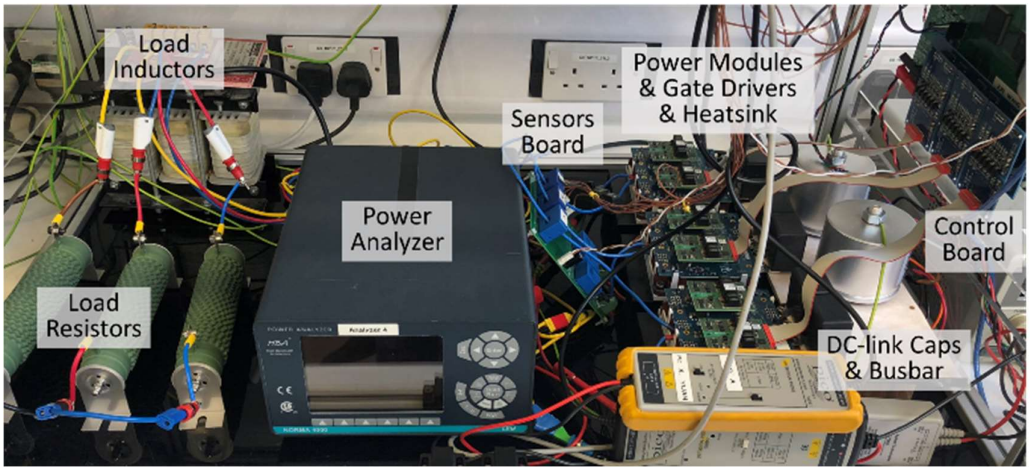


Figure 3-20. Test rig 2

Firstly, the voltage balancing performance of the control schemes are assessed. As shown in Figure 3-21, without the voltage balancing control, the NP voltage oscillation reaches ± 20 V in this test rig with a frequency of $3{\cdot}f_0$, and the output current is clearly distorted. In Figure 3-22 and Figure 3-23, it is clear that both VZM and proposed hybrid scheme can successfully suppress the low frequency NP voltage oscillation. The NP oscillation is suppressed to switching-frequency ripples with an amplitude less than ± 1V. The operating point shown in the figures is at full modulation index (M = 1.15), which shows that the balancing schemes do not undermine the output capacity of the power converter.

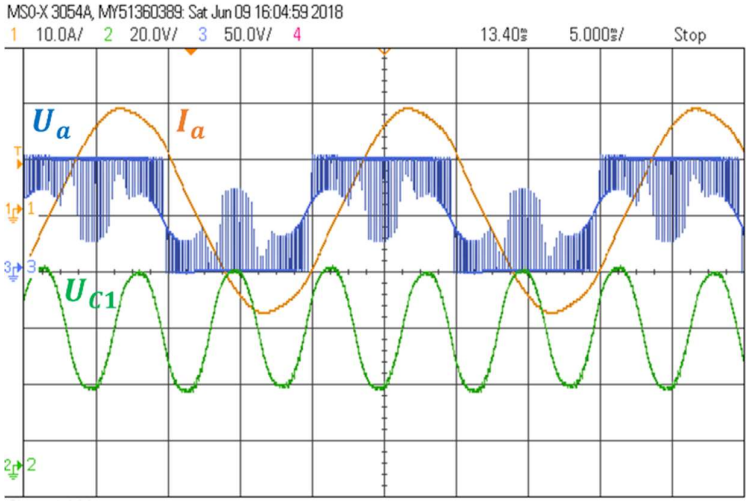


Figure 3-21. Experimental waveforms with SPWM
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

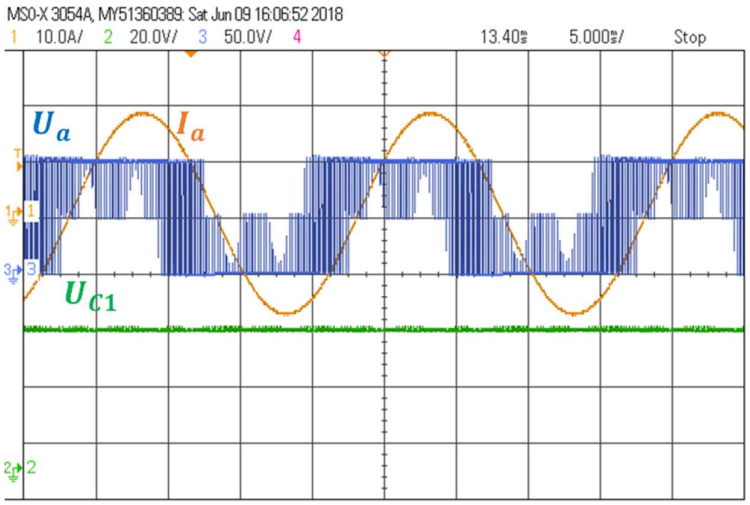


Figure 3-22. Experimental waveforms with VZM
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

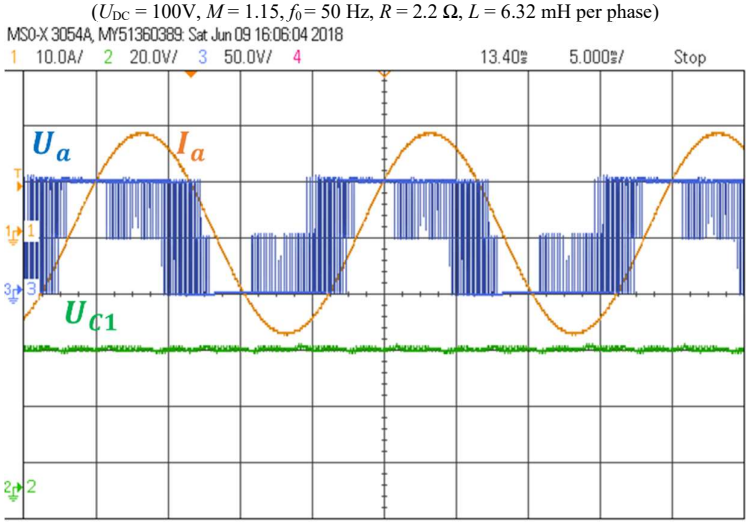


Figure 3-23. Experimental waveforms with proposed hybrid scheme
(U_{DC} = 100 V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

In practice, the delays in the close-loop NP control, e.g. sampling delays, can result in nonideal suppression of NP oscillation. In the presented test rig, the delays are minimized by (1) trading off the noise filtering for less delays in the sampling loop (2) optimizing the algorithm to ensure the computation time of the whole scheme shorter than one switching period.

The power loss of power conversion stage is measured as (3-19) by instruments listed in Table 3-8 with the converter operating at various switching frequencies. The results and fitted curves are plotted in Figure 3-24. It is visible that the proposed hybrid NP balancing scheme (red) has reduced switching loss compared to VZM (blue), as the gradient of its power loss curve, k_{sw}, is clearly smaller. This effect of proposed hybrid balancing scheme is

expected as it reduces the usage of VZM, which increases the switching transitions once activated.

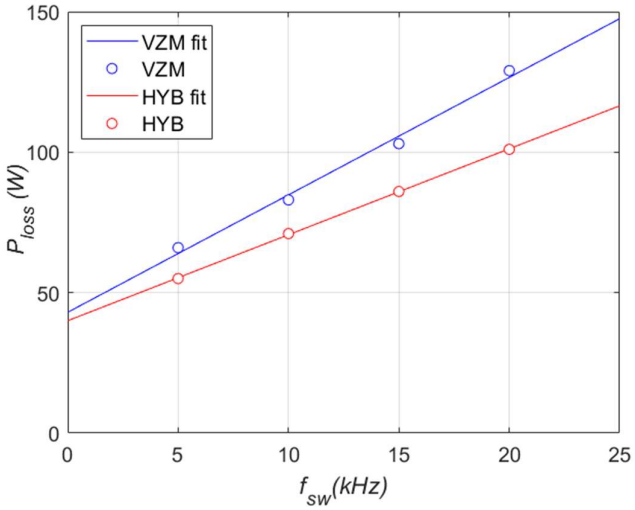


Figure 3-24. Comparison of power loss measured experimentally
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

3.6 Summary

This chapter investigated the neutral point voltage oscillation issue in three-phase, three-level converters. To address this issue, modulation-based solutions, i.e. voltage balancing schemes, are reviewed and investigated in this chapter. The aim is to achieve voltage balancing on switching window basis over the full operation range of modulation index and power factor.

The conventional approach is Zero-sequence Signal Injection, which is effective at unity power factor and low modulation index. However, it loses controllability of the NP voltage when the power factor is low and modulation index is high according to previous research. The reason behind this limitation is further investigated in this work through a controllability region analysis, which draws the same conclusion.

A relatively novel approach, Virtual Zero-level Modulation, is reviewed, implemented and evaluated in this chapter. VZM is able to successfully eliminate the low-frequency NP voltage oscillation over the full power factor and modulation index range. The controllability of VZM over the NP voltage is verified both in simulation and

experimental test rig.

The main disadvantage of VZM is the increased number of switching transitions, which leads to undesirably increase of device switching losses. To thoroughly investigate and quantify this disadvantage of VZM, an analytical power loss model is developed to analyse the impact brought by VZM on the device losses. The analytical model enables the derivation of the steady-state averaged conduction/switching loss of each power devices when VZM is applied. Experimental evaluation is conducted on a down-scaled test rig and it verifies the developed power loss model. As indicated by the model, VZM rises the total switching loss dramatically, but reduces the total conduction loss at the same time.

With the intention of minimizing the extra switching loss brought by VZM, a hybrid voltage balancing scheme is proposed in this study to achieve the voltage balancing, which combines ZSI and VZM. The novel hybrid modulation scheme coordinates the use of the two mechanisms and preferentially apply ZSI to minimize the use of VZM. The controllability performance of the proposed hybrid scheme is evaluated through simulation models, and the optimal internal logic "ZSI+VZM" is identified. Experimental verifications are conducted through a down-scaled test rig, and it shows the effectiveness of the hybrid scheme with respect to both the voltage balancing and reduced switching loss compared to pure VZM.

CHAPTER 4

Modelling of Passive Components

In the target ASR system, there are mainly three passive components that account for substantial contribution to the volume/weight of the power converter, which are (a) DC-link capacitors (b) line inductors (c) heatsinks. In order to achieve a more compact design of the converter, it is important to understand the design procedure of each individual passive component. The optimisation of the converter system requires conducting dedicated design for each individual case in the pre-defined design space introduced in Section 1.3.4.

In this chapter, the design procedure for the passive components will be presented. Following the design procedure, the models estimating the volume/weight of the components will be introduced in order to predict the performance of each design.

4.1 DC-link capacitors

DC-link capacitors are used to stabilize the DC-link voltage for the power converter. Because the ASR system is designed to operate on an aircraft, the stability and endurance of the power components are of great concern. Generally, film capacitor is the preferred option for aircraft applications due to its superior reliability, long life cycle, self-healing ability and low failure rate. Also, they have relatively low ESR (Equivalent Series Resistance) and low self-inductance (ESL) compared to electrolytic capacitors.

Film capacitors are normally bulkier than electrolytic capacitors with the equivalent capacitance. In other words, the size of film capacitor is very sensitive to its capacitance. Given the key of this work is to achieve smaller size of passive components, it is desired to have small DC-link capacitors [39], [61], [97]–[99], which is

particularly important when film capacitors are used. The main constraint of film DC-link capacitors is the allowable high-frequency DC-link voltage ripple [52].

4.1.1 Sizing of DC-link capacitance and DC-link voltage ripple modelling

In the VSC system, there are high-frequency ripples over the DC-link voltage U_{DC}, which is caused by the PWM operation of the converter. Modelling of the ripple components ΔU_{DC} determines the design of the DC-link capacitors. As the foundation of this topic, [100], [101] presents an analytical model to predict the amplitude of ΔU_{DC} in a three-phase VSC over various operating points. To quantify the high frequency voltage ripple, the peak-to-peak amplitude of ΔU_{DC} is normalized over a base value as

$$\Delta U_{DCN} = \frac{I_{rms}}{C_{DC} f_{sw}} \tag{4-1}$$

Where C_{DC} is the total DC-link capacitance; I_{rms} is the load RMS phase current (e.g. $I_M/\sqrt{2}$ in (2-2)). A normalized high-frequency voltage ripple k_{DC_norm} is defined with respect to the ΔU_{DC} and ΔU_{DCN} as

$$\frac{\Delta U_{DC}}{\Delta U_{DCN}} = k_{DC\_norm} \tag{4-2}$$

According to [100], ΔU_{DC} is a function of modulation index M and power factor $cos\ \varphi$. The mathematical expressions of k_{DC_norm} is as (4-3) for a converter modulated by SPWM.

$$k_{DC_{norm}} = \frac{M}{16}\left[\left(6 - \frac{96\sqrt{3}}{5\pi}M + \frac{9}{2}M^2\right)cos^2\varphi + \frac{8\sqrt{3}}{5\pi}M\right]^{0.5} \tag{4-3}$$

Note it is demonstrated in [100] that at zero load power factor, ΔU_{DC} is the same regardless of the modulation scheme. Expression (4-3) is visualized in Figure 4-1. It can be seen that the amplitude of ripple component reaches the worst-case when $M = 1.15$ and $cos\ \varphi = 0$, where $k_{DC\_norm\_max} \approx 0.0724$.

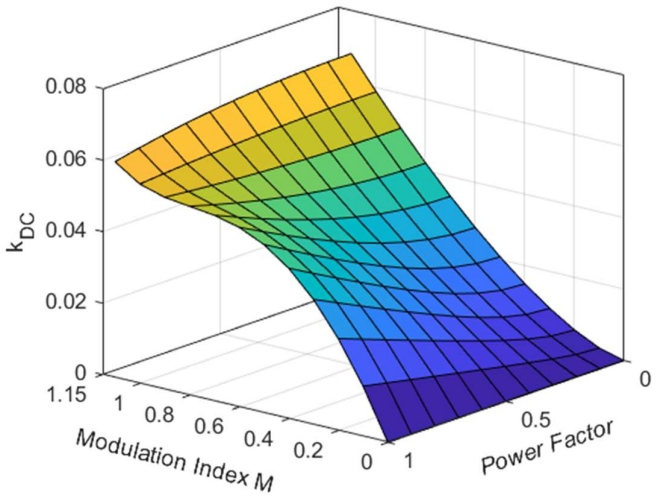


Figure 4-1. High-frequency ripple voltage factor in VSC with SPWM

The DC-link capacitance is designed against the allowable maximum amplitude of high frequency voltage ripple as (4-4), in which k_{vr} is the DC-link voltage ripple tolerance factor.

$$\Delta U_{DC} \leq k_{vr} \cdot U_{DC} \tag{4-4}$$

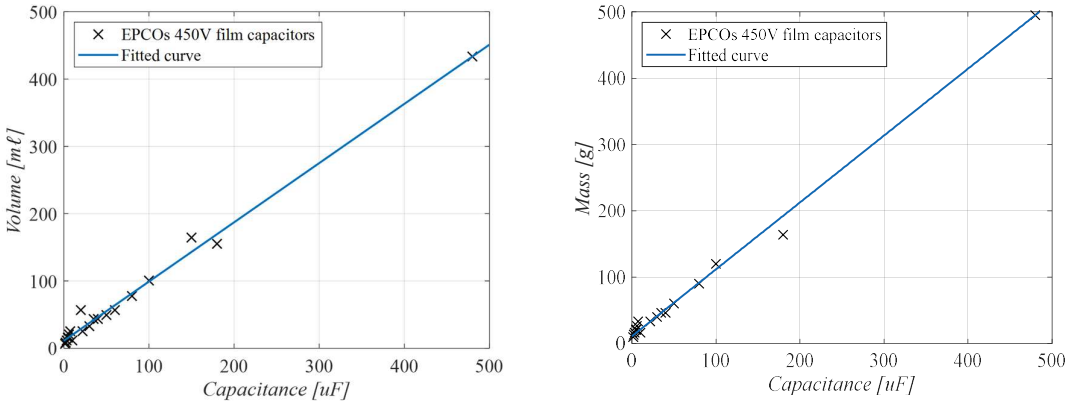
Therefore, the required DC-link capacitance considering the worst case is found by

$$k_{DC\_norm\_max} \cdot \frac{I_{rms}}{C_{DC} f_{sw}} = k_{vr} \cdot U_{DC} \rightarrow C_{DC} = k_{DC\_norm\_max} \cdot \frac{I_{rms}}{k_{vr} \cdot U_{DC} \cdot f_{sw}} \tag{4-5}$$

4.1.2 Volume/weight modelling of DC-link film capacitors

The DC-link voltage of the system is rated at 300 ~ 350 V. Considering a safety margin, the DC-link capacitor should be rated at >450 V. If the DC-link is formed by two capacitors in series, C_1 and C_2, as shown in Figure 2-1, theoretically, each capacitor only needs to be rated at half the DC-link voltage due to series connection. But, in case of extremely unbalanced voltage between the capacitors, e.g. whole DC-link voltage applied on one capacitor due to control system's malfunction, each capacitor should be rated greater than the DC-link voltage (e.g. >450V).

The volume of DC-link capacitors is modelled based on commercial metallized polypropylene capacitors from *EPCOS*, the *B3267X and B3277X series* with 450 V rated voltage. Curve fitting is performed on the volume of capacitors against their capacitance, as shown in Figure 4-2.



(a) Volume (b) Mass

Figure 4-2. Volume/mass of capacitor with respect to capacitance
(EPCOs 450V rated film capacitors, series *B3267X* and *B3277X*)

The approximated volume/mass model extracted from these off-the-shelf capacitors is expressed as

$$V_{cap}\ (m\ell) = 8.054 + 0.8864 \cdot C(\mu F) \tag{4-6}$$

$$V_{cap}\ (g) = 10.78 + 1.009 \cdot C(\mu F) \tag{4-7}$$

If two identical capacitors are placed in series to form the DC-link capacitance, as shown in Figure 2-2, the capacitance of each capacitor needs to be doubled to achieve the same DC-link capacitance as

$$C_1 = C_2 = 2C_{DC} \tag{4-8}$$

Hence, in this configuration, the total volume of DC-link capacitors is the sum of two capacitors, each with a capacitance of $2C_{\mathrm{DC}}$.

4.1.3 Case study

By inputting the specifications of the ASR system listed in Table 1-1, the required DC-link capacitance and the volume of the capacitors can be estimated through the model elaborated in the previous sections. For simplified theoretical analysis, it is assumed that the capacitors can be scaled over capacitance continuously by the fitted curve shown in Figure 4-2, regardless of the availability of actual off-the-shelf capacitors. The DC-link capacitance is designed against the allowable worst-case voltage ripple. The required DC-link capacitance over the switching frequency is plotted in Figure 4-3.

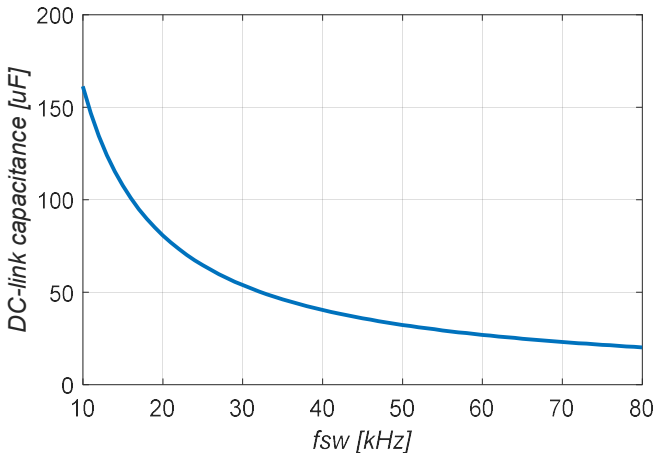


Figure 4-3. DC-link capacitance vs. switching frequency (k_{vr}= 1%)

It is visible that the required DC-link capacitance drops reverse-proportionally along the increase of switching frequency. If the switching frequency moves from 10 kHz to 70 kHz, the DC-link capacitance will reduce from 161 µF to 23 µF. Subsequently, the total volume occupied by the physical capacitors can be found from model (4-10). Two configurations for the DC-link are considered depending on the application:

1) Single-capacitor: optional for the two-level converter structure with no neutral point

2) Two-series-capacitor: existence of a DC-link neutral point; optional for two-level topology; mandatory for three-level topology.

The total capacitor volume against various switching frequencies is plotted in Figure 4-4.

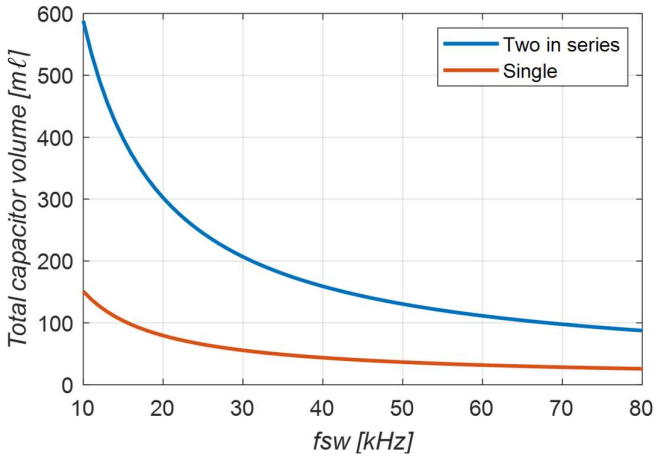


Figure 4-4. Total volume of DC-link capacitors vs. switching frequency (k_{vr} = 1%)

It can be seen that the two-series-capacitors configuration yields approximately four times volume compared to the single-capacitor configuration. As an example, when switching frequency is at 40 kHz, the DC-link capacitance is required at 40 μF. For the single-capacitor configuration, only one 40μF capacitor is needed to satisfy the DC-link ripple requirement, which occupies a volume of 43.8 mℓ. For the two-series-capacitor configuration, two pieces of 80μF rated capacitors are required, which is in total 160μF of installed capacitance and 159.1 mℓ of volume. Therefore, for the sake of increasing power density, the single-capacitor configuration is preferred in the two-level based configurations.

It can also be noticed that, when the switching frequency moves from 10 kHz to 70 kHz, the volume of capacitors in the two-series-capacitor case will decrease from 588 mℓ to 98 mℓ, which is an 83% reduction.

4.2 Line inductors

The sizing of the line inductance is constrained by the requirement of the allowable current ripple. The output current ripple of the power converter leads to additional noise and power loss in both the converter and the load [102]. Furthermore, the power quality and harmonic content must satisfy the requirement defined in RTCA DO-160E [64]. Hence, the sizing of line inductance is determined by the modelling of output current harmonics.

4.2.1 Sizing of line inductance and modelling of output current ripple

The requirement of current ripple is defined as the maximum amplitude of the peak-to-peak current $\Delta I_{\text{pp-max}}$ in one switching cycle. The constraint regarding $\Delta I_{\text{pp-max}}$ is specified by a percentage k_{cr} of peak load current I_{m} as

$$\Delta I_{pp-max} = k_{cr} \cdot I_m \tag{4-9}$$

Previous study [103], [104] presents a comprehensive investigation of the peak-to-peak current ripple in both two-level and three-level converters. As the conclusion, the worst-case amplitude of the current ripple in a three-phase voltage source converter can be approximated by the following formulas for two-level [105], [106] and

three-level converters [103].

$$\Delta I_{pp-\max-2level} \approx \frac{U_{DC} T_{sw}}{6L} \ (2-level\ converter) \tag{4-10}$$

$$\Delta I_{pp-\max-3level} \approx \frac{U_{DC} T_{sw}}{12L} \ (3-level\ converter) \tag{4-11}$$

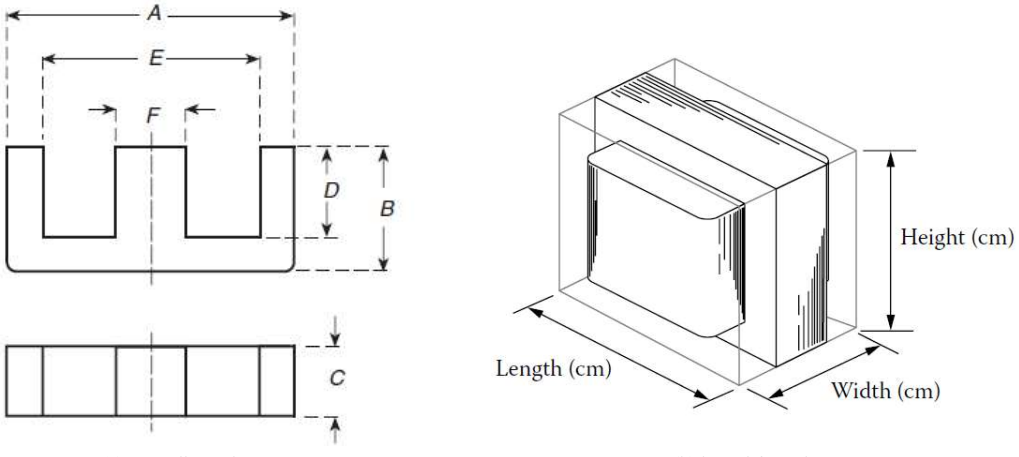
It can be seen that the maximum current ripple in a three-level converter is approximately half of the value in a two-level converter. By rearranging the equation, the required inductance can be derived as

$$L_{2level} = \frac{U_{DC} T_{sw}}{6 \cdot \Delta I_{pp-\max}} \ (2-level\ converter) \tag{4-12}$$

$$L_{3level} = \frac{U_{DC} T_{sw}}{12 \cdot \Delta I_{pp-\max}} \ (3-level\ converter) \tag{4-13}$$

4.2.2 Design and modelling of line inductors

There are a wide range of materials and shapes of magnetic cores to choose for the design of inductors. Ferrite cores are the mostly common used core material in high-frequency power electronics [107]. However, a low saturation flux density (B_{sat} < 0.5T) of ferrite cores becomes the limitation of the power density of ferrite-based inductors. As an alternative material, Cobalt Iron (CoFe) Alloys offers a very high saturation flux density (B_{sat} < 2.35 T), which have been used in aviation industry for high-power-density generator and motors [108], [109]. Therefore, this work adopts CoFe alloy for the line inductors aiming at achieving a high power density.



(a) Core dimensions (b) boxed footprint

Figure 4-5. Illustration of EE core
Reprinted from [110]

For the shape of cores, double E (EE) core, as shown in Figure 4-5, is one of the most commonly used inductor core shape for high power inductor designs [107]. This work bases on EE cores with an air gap in the central leg to avoid core saturation. The design of the line inductors is based on Area Product Method [107], [110], [111]. The Area Product A_p of an inductor core is defined as

$$A_p = W_a A_c = \frac{L I_{max} I_{rms}}{K_u J_m B_{pk}} \tag{4-14}$$

Where A_c is the cross-sectional area of the core; W_a is the core window area; K_u is the window utilization factor (copper filling factor); J_{max} is the maximum current density; B_{max} is the maximum flux density. The design/selection of the magnetic cores must satisfy the required A_p. The windings are selected based on allowable current density $J_{\max}$.

Once the core dimensions are determined the number of turns of the windings N can be found from (4-15).

$$N \geq L \frac{I_{max}}{A_c B_{max}} \tag{4-15}$$

Next, the air gap length l_g is derived as

$$l_g = \frac{\mu_0 \cdot N^2 \cdot A_c}{L} - \frac{l_m}{\mu_r} \tag{4-16}$$

Where μ_0 is the vacuum permeability; μ_r is the relative permeability of the core material; l_m is the mean magnetic path length.

In this work, the EE cores are fully customized based on the relative geometry dimensions scaled by parameter a as shown in Table 3-8. Given one set of required electrical parameters (L, I_{max} and I_{rms}), an customized inductor core can be designed by solving the dimensional parameter a through (4-14) and Table 3-8. Once the main dimensions of the core are determined, the derivative parameters can be retrieved accordingly, such as the volume of the core, magnetic path length and the boxed volume of the inductor, as listed in Table 4-1.

TABLE 4-1. RELATIVE DIMENSIONS OF ONE DESIGN OF EE CORES

	Symbol	Relative dimensions	
Main Dimensions			
Core length	*A*	5.7	*a*
Core width	*B*	0.7	*a*
Core depth	*C*	4.25	*a*
Window height	*2D*	0.4	*a*
Window width	*(E-F)/2*	1.85	*a*
Central leg width	*F*	1	*a*
Derivative parameters			
Mean Turn Length	*MTL*	18	*a*
Mean Magnetic Path Length	l_m	5.7	*a*
Area product	A_p	2.537	a^4
Core volume	V_{core}	27.7	a^3
Total boxed volume of inductor	V_L	68	a^3

To model the volume of inductors the previous studies [27], [107] consider the volume of a inductor to be a function of its stored energy

$$V_L = K_{L-energy} \cdot L \cdot I_{rms}^2 \tag{4-17}$$

Where the coefficient of $K_{\text{L\_energy}}$ can be extracted empirically from existing inductor designs. Alternatively, the inductor volume can be modelled as a function of the Area Product as (4-18) [27], [31], [112], [113].

$$V_L = K_{L-AP} \cdot A_p^{0.75} \tag{4-18}$$

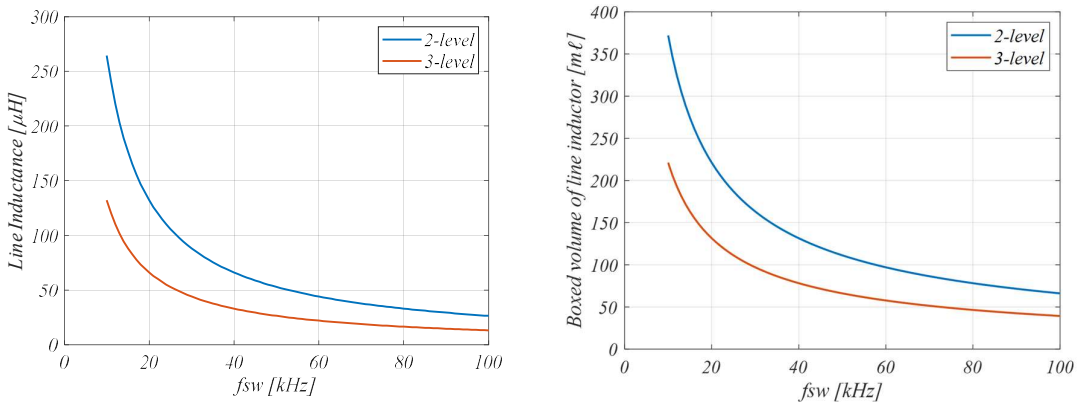
Where the coefficient of $K_{\text{L\_AP}}$ can be extracted empirically from existing inductor designs. These two models provide a simplified prediction of the inductor size based on the system specifications.

However, the above two models both requires abundant databases of existing inductor designs, which is not available for *CoFe* based inductors because they are heavily customized depending on the application. In addition, apart from modelling the size of the inductor, this work also intends to model the inductor power losses, which will be elaborated in CHAPTER 5. To model the inductor losses, detailed geometry information is necessary, such as the cross-section area and magnetic length of the core. Therefore, this work requires conducting the whole design process of individual inductors for each individual design of the converter in the design space.

4.2.3 Case study

Following expressions (4-12) and (4-13), the line inductance for both two-level and three-level configurations are designed over the switching frequency range (10 kHz – 100 kHz) for the target ASR system.

The maximum allowable current ripple percentage k_{cr} is set at 20%. For simplicity, it is assumed that three separate inductors are designed for each phase instead of one three-phase inductor. The results are shown in Figure 4-6.



(a) inductance (one phase) (b) boxed inductor volume (one phase)

Figure 4-6. Line inductance and inductor volumes against switching frequency
(k_{cr} = 20%; K_u = 0.7; J_{max} = 15×10^6 A/m^2; B_{max} = 1.65 T)

As can be seen, the required line inductance drops in an inverse proportional manner along the frequency axis. For the two-level topology case, when the switching frequency rises from 20 kHz to 70 kHz, the inductance changes from 132.2 μH to 37.8μH, which leads to a 61% reduction of the inductor boxed volume (221 mℓ to 86 mℓ). Furthermore, as indicated by expressions (4-12) and (4-13), the three-level configuration only requires half the inductance compared to the two-level case. Therefore, increasing the switching frequency and replacing two-level topology with three-level topology can both effectively reduce the line inductance, and subsequently the physical size of the line inductors.

As a reference design, a customized inductor is fabricated based on double EE cores and *CoFe* laminations. This reference inductor is co-designed and built with Dr. Kfir Pzenica. The winding bobbin is excluded from the design to achieve a more compact structure and better thermal conductivity. The dimensions of the core are derived following Table 3-8 with an target switching frequency at 73 kHz for a two-level converter. This reference design will be characterized regarding its power losses in CHAPTER 5.

Figure 4-7. Customized inductor with EE cores made from CoFe alloys

4.3 Heatsinks

Heatsinks are important in power converters to ensure the components, mainly power devices, to operate at a safe level of temperature. The magnitude of device power losses directly impacts on the design of heatsinks. The main design constraint of heatsinks is mainly determined by maintaining the junction temperature of each power device below the upper limit.

4.3.1 Heatsink sizing for power devices

To choose the size of heatsink, a common approach in based on steady-state thermal resistance network of the device-heatsink system. The thermal resistance R_{th} is defined as

$$R_{th} = \frac{\Delta T}{P} \left[\frac{^{\circ}\text{C}}{W}\right] \tag{4-19}$$

Where ΔT is the temperature rise; P is the power loss.

The thermal resistance of a piece of material is rated through

$$R_{th} = \frac{d}{\lambda \cdot \text{A}} \left[\frac{^{\circ}\text{C}}{W}\right] \tag{4-20}$$

Where d is the material thickness; λ is the heat conductivity of the material; A is the heat flow area.

For power modules with a base plate, the main heat conduction path from device junction to ambient has a

multi-layer structure [114]. This heat path is modelled as the sum of three thermal resistances:

- R_{th_jc}: junction-to-case thermal resistance (per device), determined by the design and manufacture of the power module internally.
- R_{th_cs}: case-to-heatsink thermal resistance (per module), determined by the thermal interface material applied and the size and quality of the contact areas between the module package and the heatsink, where "case" refers to the base plate of the power module.
- R_{th_sa}: heatsink-to-ambient thermal resistance (per heatsink), determined by the heatsink.

A thermal network diagram for a heatsink mounted with a power module is shown in Figure 4-8.

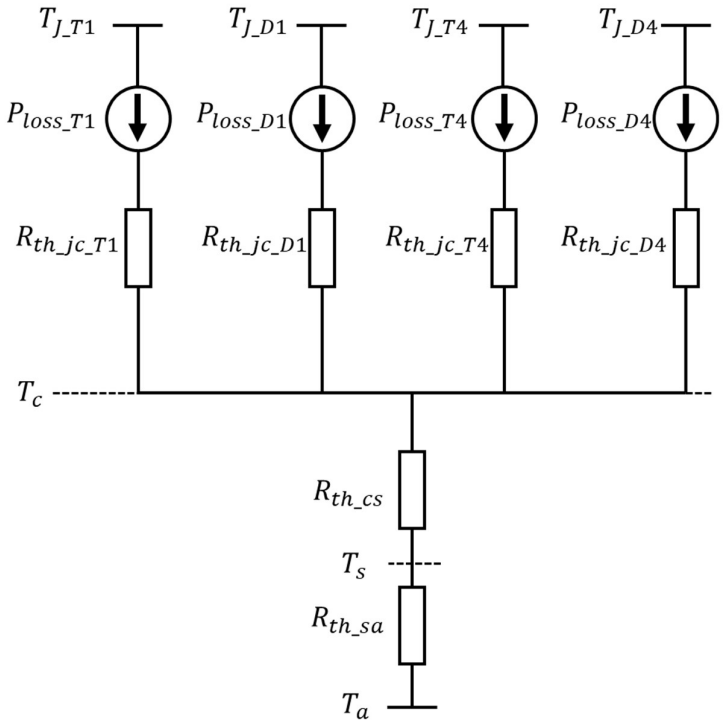


Figure 4-8. Thermal network of a heatsink mounted with one half-bridge power module with base plate

The analytical method of estimating the device power losses is presented in CHAPTER 2. Following the calculated power loss, the temperatures shown in Figure 4-8 during steady state operation can be calculated as follows:

a) To calculate heatsink temperature T_s, considering all the sources of power loss on a heatsink (e.g. three power modules), the individual loss of all n_1 components mounted on the heatsink are added up, e.g. 6 IGBTs and 6 diodes in total for three half-bridge modules. The expression of T_s is as (4-21), where T_a is the ambient temperature; $P_{tot(T)}$ is the total loss of a semiconductor switch (IGBT or MOSFET); $P_{tot(D)}$ is the total loss of a diode.

$$T_s = n_1 \times \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th\_sa} + T_a \tag{4-21}$$

b) To calculate case temperature T_c considering R_{th_cs} is specified for a module, all sources of power loss n_2 in a single module are added up, e.g. 2 IGBTs and 2 diodes in a half-bridge module.

$$T_c = n_2 \times \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th\_cs} + T_s \tag{4-22}$$

c) The junction temperature T_j of a particular device can be calculated from the case temperature and the power loss of the device, as R_{th_jc} is specified for a single device.

$$T_{j\_T} = P_{tot(T)} \cdot R_{th\_jc} + T_c \tag{4-23}$$

The required R_{th_sa} is determined by satisfying the junction temperature constraint for each power device. In other words, the power device estimated with largest temperature rise would determine the required performance of the heatsink. Once the required R_{th_sa} is known, a heatsink can be designed/selected. For off-the-shelf products, the R_{th_sa} value can be found from the manufacturer datasheet of heatsinks (e.g. [52], [115]).

For this study, the thermal parameters of the power modules are found from the datasheet as shown in Table 4-2. The R_{th_cs} is reported at 0.025 ~ 0.055 *°C/W* depending on the thermal interface material [51], [116], which are theoretically evaluated through equation (4-20). The maximum junction temperature T_{j_max} is set at 125 *°C* as a common constraint [111], which is mainly limited by the packaging of the selected power modules in this study. It can be seen from Table 4-2, the SiC devices offers superior thermal performance inside the power module comparing to the Si power module, e.g. R_{th_jc} at 0.075 *°C/W* for SiC module compared to 0.19 *°C/W* for Si module. This superiority of SiC devices is due to a higher thermal conductivity and small layer thicknesses [27].

TABLE 4-2. THERMAL PARAMETERS OF POWER MODULES

	CAS300M12BM2	SKiM301TMLI12E4B
R_{th_jc} [°C/W] (IGBT/MOSFET)	0.075	0.19 (T1/T4) 0.3 (T2/T3)
R_{th_jc} [°C/W] (Diode)	0.076	0.29 (D1/D4) 0.35 (D2/D3)
R_{th_cs} [°C/W]	0.025	0.025
$T_{j\ max}$ [°C]	125	125

4.3.2 Volume/weight modelling of heatsinks

Once the required thermal resistance of a heatsink is determined, the size of air-cooled heatsinks can be theoretically estimated through the achievable Cooling System Performance Index (CSPI). CSPI was proposed in [116]–[119] and defined as

$$CSPI\left[\frac{W}{K\cdot\ell}\right]=\frac{1}{R_{th_{sa}}\left[\frac{K}{W}\right]\cdot V_{heatsink}[\ell]} \tag{4-24}$$

[116]–[119] provide a comprehensive investigation of the performance of highly optimized air-cooled heatsinks over various materials. To reduce the complexity of this study, the material of the heatsink is limited to aluminum, with reference to the common commercial extrusion heatsinks from ©Aavid [52], [115]. According to [116], the CSPI of air-cooled aluminum heatsinks with fans can reach 17.7 W/K·litre. This value will be assumed achievable for the investigation of this study. The weight of the heatsink is estimated assuming the half of the heatsink volume is occupied by air referring to the demonstrated design in [119].

Following the assumption, the volume of the heatsink in the optimisation algorithm is scaled through CSPI with respect to the required thermal resistance of the heatsink. Additionally, [116]–[119] also shows the achievable minimum thermal resistance of forced-air-cooled heatsinks at 0.1 ~ 0.25 °C/W and natural-cooled heatsinks at > 0.5 °C/W. Based on this limitation, it is considered in the analysis that an air-cooled heatsink can only achieve a thermal resistance of < 0.1 °C/W through an infinite volume of the heatsink.

When a forced air-cooled heatsink cannot satisfy the requirement of thermal resistance, a liquid cooling system can be applied to cool the power devices（[120], [121]). [122] reports the thermal resistance of a highly

optimized cold plate that reaches a minimum value at around 0.85 °C/W per cm^2, which is equivalent to 0.013 °C/W for a base plate size as CAS300M12BM2. Commercial products and previous studies [123], [124] reported a cold plate with three power modules mounted reaching a thermal resistance at 0.013 ~ 0.03 °C/W. The volume of liquid-cooling systems is relatively independent to the required thermal resistance. As [122] demonstrates, the primary constraint of the cold plate size is the base plate area of the power module in order to accommodate the power module. In this work, only the size of the cold plate is considered regardless of the auxiliary systems (e.g. pumps, pipes, heat exchanger and valves).

4.3.3 Case study

Following the power loss modelling established in CHAPTER 2 and CHAPTER 3, the required thermal resistances of heatsinks are evaluated over the target switching frequencies, with the results shown in

Figure 4-9. To simplify the considerations, it is assumed that three separate heatsinks are designed for each power module. This analysis assumes the ambient temperature as $T_a = 40$ °C, i.e. 85 °C temperature rise is allowed from the power module base plate to the junctions of power devices.

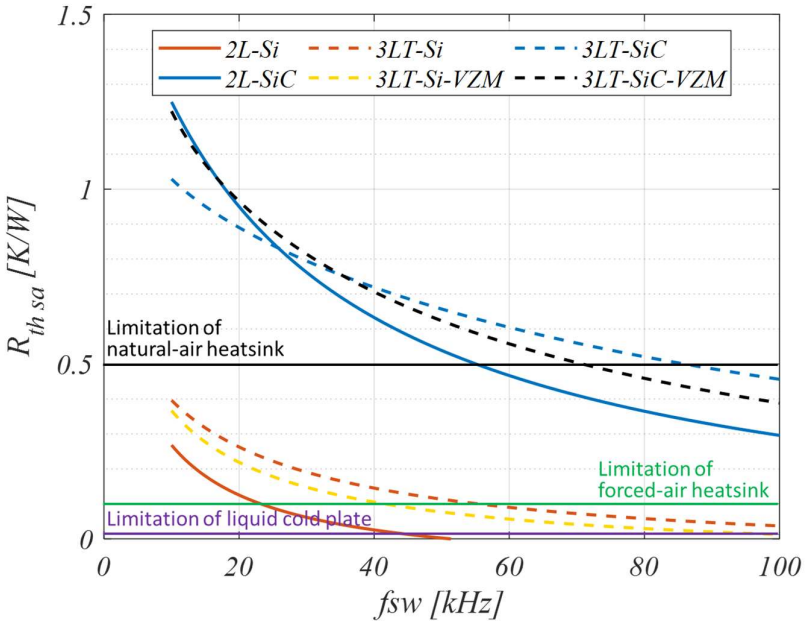


Figure 4-9. Required thermal resistance with T_a = 40 °C

As shown in

Figure 4-9, with the rising of f_{sw}, the minimal R_{th_sa} drops accordingly in all cases, which means more cooling efforts are required to counter the increased switching loss. A lower R_{th_sa} leads to a larger heatsink volume for air-cooled solutions as indicated by CSPI. When the R_{th_sa} reaches the limitation, the cooling method must be changed to satisfy the demand of more cooling capability. For example, when required R_{th_sa} drops below 0.5 °C/W, the cooling method must be changed from natural-air-cooling to forced-air cooling, which introduces the fans and auxiliary power supplies. When R_{th_sa} drops below 0.1 °C/W, the heatsink must be replaced by a cold plate cooled by liquid coolant, which brings in auxiliary systems such as pumps and heat exchangers.

Due to the extra-low switching losses of SiC devices, the SiC based configurations require much less cooling efforts compared to the Si based options. Up to 100 kHz, all SiC based options only need air-cooled heatsinks. Additionally, the *2L*-SiC option only requires natural-air-cooling heatsinks when the f_{sw} is less than 55 kHz.

In the options based on Si devices, the required R_{th_sa} drops dramatically. The *2L*-Si case shows that from 22 kHz onwards, forced-air-cooled heatsinks cannot accommodate the increased switching losses, for which cold

plates must be adopted instead. From 50 kHz onwards, no matter what cooling efforts is made on the *2L*-Si based converter, the internal temperature rise within the power module will exceed the allowable range. From the topology point of view, three-level T-type topology shows improvement of switching loss and subsequently requires less cooling efforts, as shown in

Figure 4-9. But, if the voltage balancing scheme VZM is considered, the improvement of switching loss brought by the three-level topology will be degraded. A forced-air-cooling heatsink allows the *3LT*-Si option to operate up to approximately 50 kHz.

Next, if force-air-cooling heatsinks are applied, the heatsink volumes can be estimated by scaling through the CSPI. The results are illustrated in Figure 4-10.

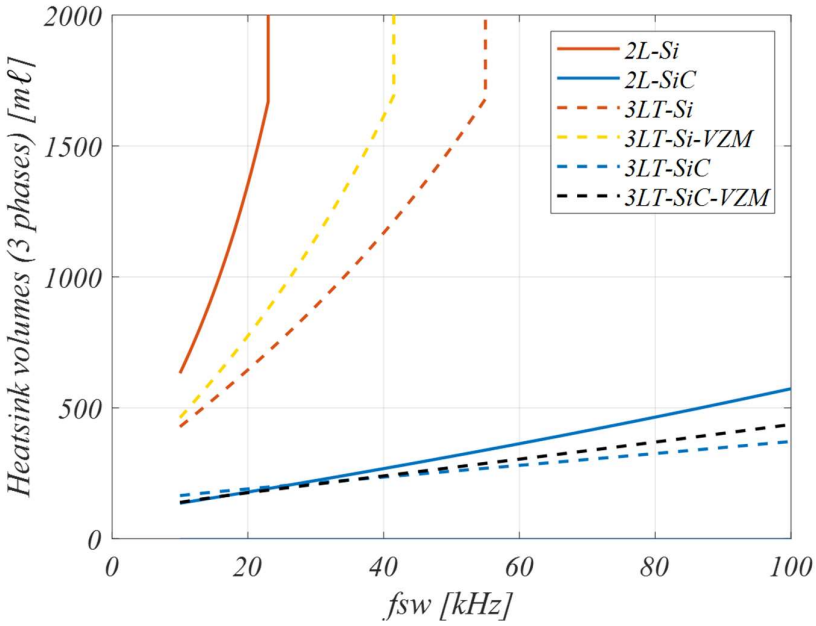


Figure 4-10. Air-cooled heatsink volumes (CSPI = 17.7 W/K·litre)

As can be observed in Figure 4-10, at 10 kHz switching frequency, the SiC based options feature substantial reductions of the volume of heatsinks, which are only 68 % compared to the *3LT*-Si case and 78% compared to the *2L*-Si case. Furthermore, the SiC devices enables the converter to operate at higher switching frequencies without overheating internally. A three-phase *2L*-SiC converter operating at at f_{sw} = 70 kHz only requires forced-

air-cooled heatsinks with a total volume of 413 mℓ.

In aerospace applications, liquid cooling solutions are preferred in the cases where the harsh environment must be considered. For this type of application, power converter system can share the existing coolant circulation system on an aircraft (e.g. liquid jacket cooling system for starter/generators). The inlet coolant temperature of the existing system is assumed to be 80 °C. In this case, the allowable temperature rise from the power module base plate to device junctions becomes 45 °C. The required performance of heatsink is evaluated in this case and plotted in Figure 4-11.

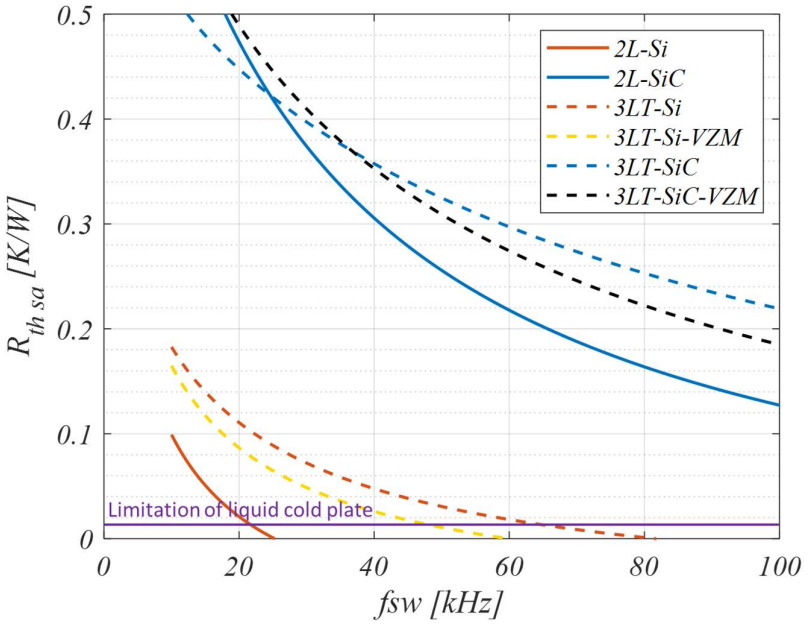


Figure 4-11. Required thermal resistance with T_a = 80 °C

As shown in Figure 4-11, applying a cold plate with a thermal resistance at around 0.01 ~ 0.05 °C/W provides ample cooling for SiC based options with up to 100 kHz switching frequency. For Si-based options, the cold plate allows the *3LT*-Si option to operate up to around 50 kHz and the *2L*-Si option to run up to approximately 20 kHz. From another angle, given that the design and cooling capability of a cold plate is relatively fixed, applying the cold plate leads to a lower operating temperature of the SiC based options. For example, if the cold plate offers a R_{th_sa} of 0.015 °C/W, the MOSFETs in the *2L*-SiC case with a switching frequency of 70 kHz would only operate

at 104 °C in steady state, while the upper limit is 125 °C.

As a reference design, an aluminum cold plate is designed by Dr. Kfir Pzenica with a volume of 0.1474 litre and a weight of 356 g for this project. The size of the cold plate is designed to accommodate the power module CAS300M12BM2. A picture of the cold plate is shown in Figure 4-12.

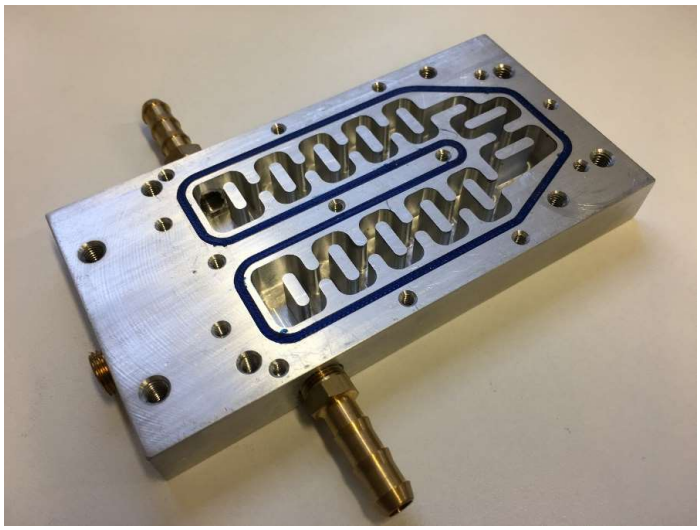


Figure 4-12. Customized aluminum cold plate

4.4 Summary

This chapter has elaborated the design and modelling of three main passive components in the target ASR system: DC-link capacitor, line inductor and heatsink.

For aerospace applications, film capacitors are selected as the DC-link capacitors due to their long life cycle, self-healing ability, low failure rate and low ESL/ESR compared to electrolytic capacitors. As the drawback, film capacitors feature low capacitance over per unit volume. Hence, a low DC-link capacitance design is desired for achieving a high power density of a converter. The DC-link capacitors are sized against the switching-frequency voltage requirement following the established model of DC-link voltage ripple from the literature. For the target system, increasing the switching frequency exhibit effective reduction in the size of DC-link capacitors. The

volume/weight model of capacitors is extracted from available 450V rated commercial products.

Line inductor is the other important filter component for the functionality of the target ASR system. The dimensioning of line inductance is based on the output current ripple requirement. The modelling of current ripples are well established in the literature, both for two-level and three-level converters. The line inductors can be designed with selected magnetic core shapes and materials. This work utilized gapped EE core and CoFe material to realize the line inductors aiming at high power density. The design approach is based on Area Product method assuming fully customized dimensions. The case study shows that increasing the switching frequency is very effective in shrinking the inductor size. In addition, the three-level topology only requires half the inductance compared to the two-level converter topology.

Heatsinks are designed to cool the power devices. The required performance of the heatsink is found from the thermal resistance model of the power module-heatsink system and the averaged device power losses derived in CHAPTER 2. The performance limitation of the heatsinks are identified from the literatures. Both the air-cooled and liquid-cooled heatsinks are considered for the target application. The volume/weight of air-cooled heatsinks are scaled over the Cooling System Performance Index (CSPI). The liquid-cooled cold plates provide ample cooling for the power devices. The geometry of the cold plate is mainly sized to mount the power module. A reference design of the cold plate is presented.

CHAPTER 5

Power Loss Modelling of Inductors

In power converters, filter inductors are used to attenuate current ripple and contributes substantially to the total converter volume, weight and power losses. Particularly, filter inductors can contribute to 30~50% of the weight or volume of a typical power converter [33]. The power loss characterization of inductors has been a hot research topic. Accurate estimation of inductor loss is beneficial for the thermal design and optimisation of power converters [27], [71], [72] in early design stage. It is especially important when considers the high-frequency operation and associated high-frequency core loss and copper loss with the use of wide-bandgap switching devices [30]. In the scope of this work, the switching frequency of power devices targets at over 50 kHz.

The power losses in an inductor are categorized to two parts: the copper loss and the core loss. Generally, the the copper loss can be modelled relatively accurate through analytical approaches (e.g. [107]), while the modelling of the core loss remains challenging in PWM power converters. This chapter investigates the methods of modelling both the copper loss and core loss in order to estimate the inductor loss in the target ASR system.

The main content of this chapter has been presented by the author in the following publications:

- **J. Wang**, K.J. Dagan, X. Yuan, W. Wang and P.H. Mellor, "A Practical Approach for Core Loss Estimation of High-current Gapped Inductors in PWM Converters with User-friendly Loss Map" *in IEEE Transactions on Power Electronics*, 2018
- **J. Wang**, K.J. Dagan, X. Yuan, "An Efficient Analytical Inductor Core Loss Calculation Method for Two-level and Three-level PWM Converters based on a User-friendly Loss Map" in *Proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC),* 2019

5.1 Background on inductor core loss modelling

Within the context of PWM power converters, there are several challenges in estimating the core loss of filter

inductors. Challenge A: In a PWM converter, the inductor is exposed to rectangular voltage and triangular current, rather than sinusoidal excitation. However, normally only a limited loss profile generated from sinusoidal excitation can be found in manufacturer's datasheet for one type of core material. Furthermore, Fourier Transformation cannot be applied to analyse the core loss [125]. Challenge B: The high frequency triangular current waveform contains a varying, low-frequency DC component. This DC bias factor is also referred as pre-magnetisation, indicating the position of the B-H loop relative to the origin where $H_0 = 0$. Pre-magnetisation is reported to have significant impact on the core loss [126]–[129] for particular materials such as Soft Ferrites.

A widely accepted empirical core loss model is the Steinmetz Equation (SE) (5-1), which indicates the core loss is a function of frequency f and flux density swing ΔB.

$$P = k f^{\alpha} \Delta B^{\beta} \tag{5-1}$$

However, SE is limited in accuracy as the coefficients are only accurate within a certain range of frequency [130], [131]. Moreover, SE is only valid for sinusoidal excitation, which means SE is not directly applicable for the filter inductors driven by PWM converters.

To overcome Challenge A, Improved Generalised Steinmetz Equation (IGSE) (5-2) was introduced to calculate the loss of any arbitrary flux waveform [132]–[134].

$$Q = \int_0^T k_i \left(\frac{dB}{dt}\right)^{\alpha} (\Delta B)^{\beta-\alpha}\, dt \tag{5-2}$$

IGSE enables the conversion of SE parameters from sinusoidal excitation to rectangular. The concept of IGSE also includes decomposing a complex waveform into individual B-H loops. It is widely accepted and proven to be accurate. However, as the main drawback, IGSE does not consider the effect of pre-magnetisation [129].

To take the pre-magnetisation effect into account, Challenge B, "loss map" approach was proposed in publications [126]–[128]. This approach relies on experimental B-H loop measurement to construct a core loss profile covering various inductor operating points described by H_0, ΔB and f. The measurement configuration of

these studies is based on a buck (chopper) converter with rectangular output voltage. The method of utilising the pre-measured loss map to calculate the inductor core loss for PWM inverters is also proposed in [126]–[128], based on decomposing the B-H trajectory into calculable quasi-closed loops. In [135], [136], the loss map calculation method is revised to a half-loop based approach. An approximation method is also proposed for 3-phase PWM converters where there are consecutive segments with varying dB/dt and the sign not reversed. In [135], [137], based on dynamic B-H loop measurement, Iron Loss Analyser (ILA) is introduced as a system accurately measuring instantaneous core loss (at switching cycles level) and verifies the accuracy of revised loss map. Although, this concept is for real-time experimental evaluation on an operating PWM converter, instead of the estimation of core loss from pre-measured data. As an alternative of loss map, [129] investigated the impact of pre-magnetisation on the SE parameters and presented it in Steinmetz Pre-magnetisation Graphs, with measurements based on a H-bridge converter. However, the accuracy of this approach is limited by the accuracy of original SE parameters. To summarize, establishing a loss map is still the most practical approach to achieve accurate estimation of the core loss.

When it comes to customised inductors (e.g. the gapped EE core inductor presented in Section 4.2), the outcomes of the above research are hardly transferable. Most of the previous studies are based on performing B-H loop measurements on toroidal cores, characterising the property of one type of core material with a relatively low excitation current (e.g. <10 A). However, inductors with gapped cores are widely used for relatively high-current applications (e.g. >100 A) to avoid core saturation. Even if the core loss profile of a magnetic material is given, it still cannot be applied on gapped cores directly. For example, the H axis of the loss map for a gapped core must be rescaled, since the operational range of H is extended. Additionally, a gapped core potentially comes with excessive gap loss as reported in [138], which is essentially eddy current losses concentrated around the airgap. This is not predictable from the loss data measured from toroidal core and directly associated with the

physical shape of the core, especially the airgap length. But these effects can still be evaluated as B-H loop measurement covers all the core loss components including hysteresis loss and eddy current loss [139], [140]. Furthermore, core loss is very sensitive to the actual physical property of individual inductor cores. For laminated cores, the thickness and alignments of the laminations could drift from the designed form unpredictably from batch to batch. It is also pointed out in [141] that "Characterizing a specific core or a specific wound component is better (more accurate, easier to use) than characterizing a material". Additionally, the effect of pre-magnetisation is normally not assessed by the supplier of the core material. To count in this effect for better accuracy, additional experimental evaluation is required. Therefore, evaluation of a specific inductor on the user's side is necessary to achieve better accuracy.

To evaluate a specific, customised inductor, new challenges arise. Consider a specific high-current gapped inductor is given with the structure unalterable (e.g. potted/housed). To meet the designed operating point of H, it is not feasible to reduce the amplitude of excitation current by increasing the number of turns as the windings are fixed. In this case, the inductor loss mapping process requires high excitation current. This high current can result in unwanted temperature rise, a large DC current-time product for current probes and asymmetric excitation voltage due to significant voltage drop on power devices.

In addition, the loss map approach developed in previous studies is not straightforward for practical purposes. Firstly, it is normally employed in the form of a three-dimensional look-up table [135], [142] that is difficult to be presented or utilised. Secondly, the variables in loss map is normally in magnetic form while it is more common to use electrical and time-domain variables in the context of power electronics. The translation between these variables complicates the loss mapping process and core loss calculations. Additionally, the translation involves the effective dimensions of the core. In some cases this information is not available (e.g. not provided for housed inductor), or not accurate, which could affect the accuracy of the core loss calculation [140].

Therefore, this study intends to present a whole process of characterizing and estimating the core loss of a customised, high-current, gapped inductor for PWM operations. It covers from experimentally establishing a loss map to utilizing the loss map to estimate the inductor's core loss in PWM converters. The main contributions of this work are given as follows. To excite the inductor-under-test, a new test circuit is proposed, which is based on a half-bridge structure and enables the compensation of the asymmetric rectangular voltage caused by the device voltage drops. To overcome the other challenges raised by high excitation current (e.g. 100 A), a refined discontinuous testing procedure, Triple Pulse Test (TPT), is proposed in this study. The idea of Triple Pulse Test is to run necessary cycles only and avoid unnecessary operations. Similar ideas were discussed in previous studies, such as in [143] and [144]. This study further reveals the significant benefits of TPT in the context of testing the core loss with high excitation current. TPT does not require the full continuous operation capability of the converter and inductor. It reduces the requirements of the test setup (such as thermal stress, current-time stress for current probes, current capacity of DC sources) and enables a fast evaluation. Additionally, Triple Pulse Test is analogous to the Double Pulse Test (DPT) in characterising switching loss of power devices. As such, it can be easily understood and adopted by a power electronics engineer who is familiar with DPT. Furthermore, a loss map calculation approach is presented to utilise the pre-built loss profile to calculate/estimate the core loss of the tested inductor when operating in a PWM converter. A user-friendly loss map and core loss calculation method involving only time-domain and electrical variables, which replaces the conventional magnetic variables, has been proposed to enable straightforward loss mapping process and simplified core loss estimation. Analytical models are proposed to utilize the established loss map to estimate the core loss in a two-level and three-level converter for a given operating point. An experimental evaluation of the proposed approach is conducted on a real PWM converter.

5.2 Empirical core loss characterization

5.2.1 Core loss Measurement

B-H loop measurements have been widely used for the evaluation of core loss [128], [129], [142]. This approach measures the core loss of an inductor with the copper loss excluded. To perform B-H loop measurement, the inductor is equipped with two windings: a primary winding for excitation current and a secondary winding to sense core flux. Figure 5-1 shows a basic schematic of a B-H loop measurement test rig, formed by a DC power supply, a power converter, the inductor-under-test, voltage and current probes and a digital oscilloscope.

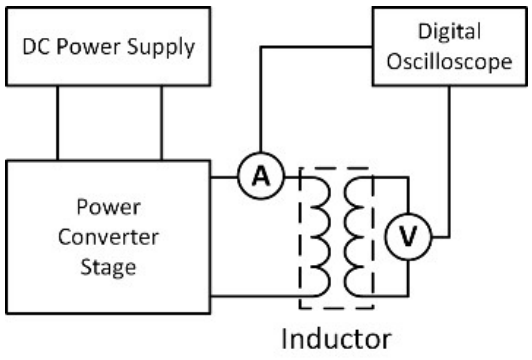


Figure 5-1. Overview of the B-H loop test system

By measuring the excitation current I on the primary side and the open-circuit voltage U_{Lsec} on the secondary side, the magnetic field H and flux density B can be found by the relationships expressed by (5-3) and (5-4)

$$B(t) = \frac{1}{N_2 A_e} \int_0^T U_{Lsec}(t)\, dt \tag{5-3}$$

$$H(t) = \frac{N_1 \cdot I(t)}{l_e} \tag{5-4}$$

Where N_1 and N_2 are the numbers of turns of the primary winding and secondary wingding, respectively; A_e is the effective cross-section area of the core; l_e is the effective length of magnetic path.

Then the core loss is obtained from (5-5) by integrating the product of the secondary voltage and primary current, with the turns ratio accounted. Note that in (5-5), the geometry parameters of the core A_e and l_e are irrelevant regarding the measured total core loss in the form of energy.

$$Q = A_e l_e \int H \, dB = \frac{N_1}{N_2} \int_0^T I(t) \cdot U_{Lsec}(t) \, dt \tag{5-5}$$

A typical voltage-current waveform for B-H loop test is shown in Figure 5-2, with square-wave excitation voltage. The curvy shape of the current, instead of a triangular shape, is caused by the magnetisation process [128]. In practice, the accuracy of B-H loop measurement is sensitive to the phase discrepancy between the measured voltage and current [128], [140], [145]. Therefore, the phase differences of the probes must be carefully calibrated.

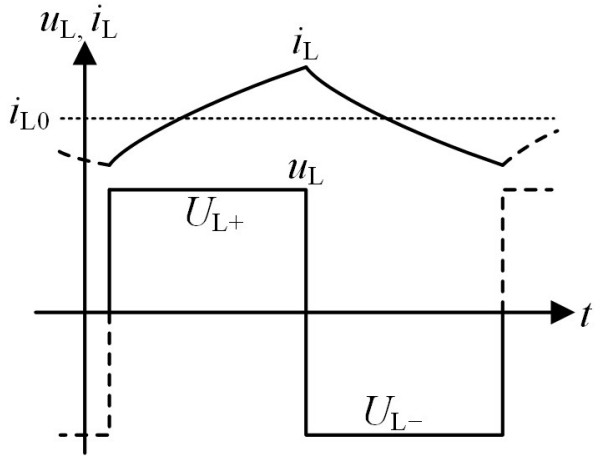


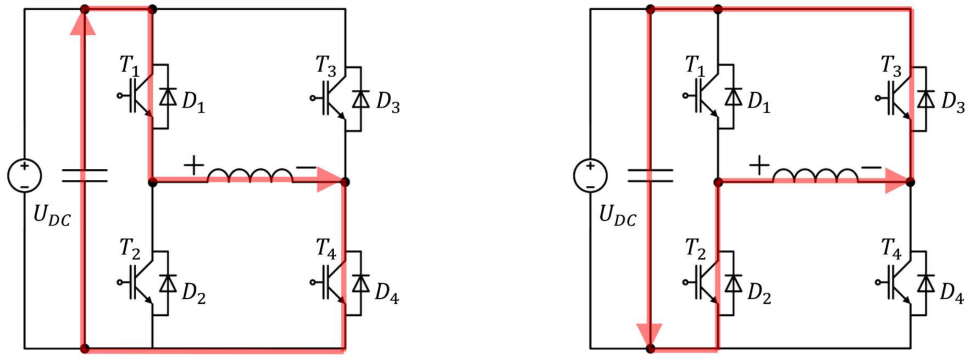
Figure 5-2. Typical inductor voltage/current waveforms for B-H loop measurement with DC-biased current

5.2.2 Power Converter Configuration

For the power converter stage, a common configuration is a buck converter [128], [129]. However, a buck converter can only evaluate the operating points with the current flowing in one direction. In PWM converters, there are operating points of the inductor with the current crossing both directions within one switching cycle. Therefore, this topology is not ideal for the evaluation of the whole operating region of the inductor in a PWM converter.

As an option with bidirectional conduction capability, a test circuit formed by a H-bridge structure is shown in Figure 5-3, which is also a common configuration in studies such as [146], [147]. However, for the scope of this study, H-bridge configuration features a significant drawback. For a pre-built high-power gapped inductor, a high excitation current must be driven into the inductor, especially for the operating points with high H_0. When a

high current is fed into the inductor, the voltage drops across the power devices at the power converter stage becomes significant. When a DC-biased current as shown in Figure 5-2 is driven into the inductor, an asymmetric square-wave voltage will cross the inductor, with unequal amplitudes U_{L+} and $|U_{L-}|$. In the positive cycle shown in Figure 5-3(a), the inductor current is drawn from the DC-link and flows through T1, the inductor and T4.



(a) positive cycle with DC-biased current (charging inductor) (b) negative cycle with DC-biased current (discharging inductor)

Figure 5-3. H-bridge test circuit

The inductor voltage U_{L+} can be expressed by (5-6). In the negative cycle shown in Figure 5-3(b), the inductor current flows through diodes D2, D3 and charges the DC-link capacitor. The inductor voltage U_{L-} in this case can be expressed by (5-7).

$$U_{L+} = U_{DC} - 2U_{IGBT} \tag{5-6}$$

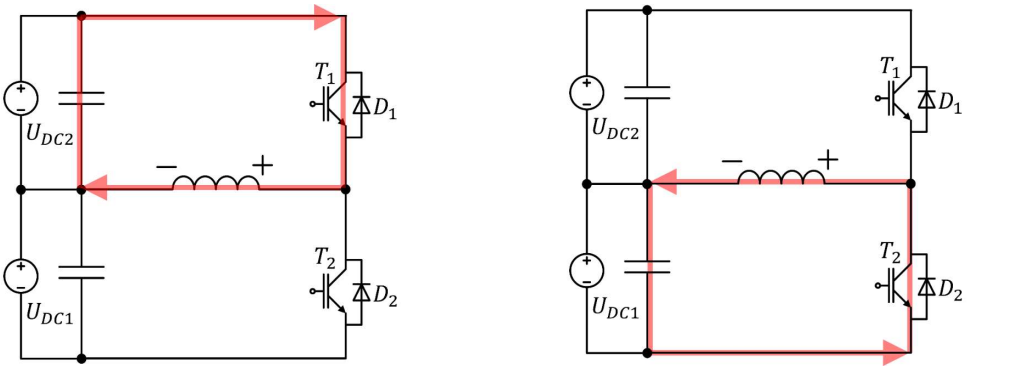
$$U_{L-} = -(U_{DC} + 2U_{Diode}) \tag{5-7}$$

Where, U_{DC} is the converter DC-link voltage, U_{IGBT} is the IGBT forward voltage drop, U_{Diode} is the diode forward voltage drop.

Taking the selected IGBT power module SKiM301TMLI12E4B as an example, given a current of 100 A, U_{IGBT} is around 1.5 volts and U_{Diode} is around 1.8 volts according to the datasheet. Assuming U_{DC} = 50 V, theoretically the voltage drops would lead to U_{L+} = 47 V and U_{L-} = −53.6 V following (5-6) and (5-7), which is a 6.6 V bias in total. This asymmetry will prevent the measured B-H trajectory from forming a closed loop and have unneglectable impact on the measured core loss. Unclosed B-H loop will compromise an important assumption to be elaborated in the next section, where it assumes the positive half cycle and the negative half cycle of a B-H

loop each consumes equal energies.

To achieve more reliable and accurate measurements, this asymmetry caused by device voltage drops must be mitigated. Therefore, an alternative test circuit for the power stage is proposed in this work as shown in Figure 5-4. This test circuit comprises a half bridge structure with two adjustable DC power sources (U_{DC1} and U_{DC2}) and two capacitors in series to form the DC-link. The inductor is placed between the output port of the half bridge and the neutral point of the DC-link.



(a) positive cycle with DC-biased current (charging inductor) (b) negative cycle with DC-biased current (discharging inductor)

Figure 5-4. Half bridge test circuit

This configuration brings extra degree of freedom: the two DC-link voltage supplies can be adjusted to compensate the asymmetric voltage drops. In the positive cycle, the current is drawn from the pre-charged capacitor with voltage U_{DC2}, flows through *T1* and charges the inductor, as shown in Figure 5-4(a). In this case the inductor voltage U_{L+} is expressed by (5-8). Figure 5-4(b) shows the current in the negative cycle, where the inductor voltage U_{L-} is expressed by (5-9).

$$U_{L+} = U_{DC2} - U_{IGBT} \tag{5-8}$$

$$U_{L-} = -(U_{DC1} + U_{Diode}) \tag{5-9}$$

By tuning the output voltages of the two DC power supplies, U_{DC2} and U_{DC1}, the inductor voltages U_{L+} and $|U_{L-}|$ can be compensated to equal. For example, if U_{IGBT} = 1.5 V and U_{Diode} = 1.8 V, U_{DC2} and U_{DC1} can be set as 51.5 V and 48.2 V respectively to achieve $U_{L+} = |U_{L-}|$ = 50V. In practice, the voltage drops on the power devices (U_{IGBT} and U_{Diode}) may deviate from what has been given the datasheet. The parasitic resistance of the test circuit

also contributes to the voltage drops. In this case, the values of supply voltages U_{DC2}/U_{DC1} are empirically determined by adjusting U_{DC2}/U_{DC1} and measuring U_{L+}/U_{L-} until the inductor voltage reaches target symmetric rectangular for each operating point.

5.2.3 Test Procedure – Triple Pulse Test

The goal of the B-H loop measurement is to measure the area of a closed B-H loop given the operating point described by H_0, ΔB and dB/dt. To overcome the challenges introduced by high excitation current, a refined discontinuous measurement procedure is proposed in this study. The idea of this approach is to apply limited pulses (e.g. three pulses) to reach the desired B-H loop and avoid further unnecessary operation, which leads to a test waveform that is similar to the saturation property test in [144]. For the scope of this study, where a large peak current is required (e.g. 100 A), this Triple Pulse Test (TPT) holds the following merits:

A. Does not require a DC power supply with the capacity of supplying a large continuous current. As this is a relatively fast and short transition (e.g. < 200 μs), the current required in this process is mainly drawn from the DC-link capacitors.

B. Significant temperature rise is avoided due to little heat generated from this process.

C. In the case where the current is measured by current probes, the DC current-time product $I \cdot t$ (in $A \cdot \mu s$) in the process must not exceed the allowable range, so that they would not saturate (reach non-linear operation region). Taking current probe N2781B as an example, the maximum allowable non-continuous current-time product is stated at 15000 $A \cdot \mu s$. This means that if the DC biased current is 100 A, the time duration of the whole testing process is limited to < 150 μs. A large DC current-time product is avoided in the proposed process as limited pulse cycles are supplied.

The process of the TPT approach is illustrated in Figure 5-5: Stage I, an initial pulse is supplied to build up

the desired pre-magnetisation H_0; Stage II, several cycles with desired flux density swing are supplied to force the B-H trajectory into target steady state; Stage III, the B-H trajectory stabilises and forms the desired B-H loop; Stage IV, the power devices are all turned-off, and the energy stored in the inductor releases through the free-wheeling diodes, which leads to the current dropping back to zero at the end of this process. The B-H loop of interest is obtained in Stage III. The turn-on and turn-off delay of the power devices is compensated in the generation of gate signals to ensure the ON duration $T2+$ equals to the OFF duration $T2-$.

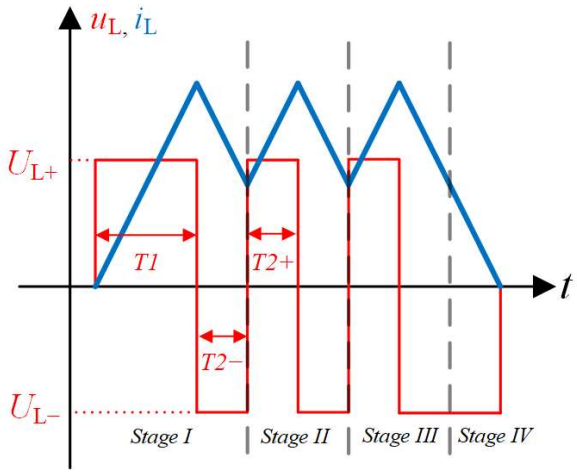


Figure 5-5. Inductor current/voltage waveform of Triple Pulse Test

By experimental observations on the tested inductor, the B-H trajectory stabilises at the target B-H loop in the third pulse cycle for most of the operating points. An example of the B-H trajectory measured from one discontinuous measurement is shown in Figure 5-6, where the blue loop is the second pulse cycle and the red loop is the third pulse cycle. The dashed line shows the pre-magnetisation process and the de-magnetisation process. It is visible that the blue and red loops are self-closed and similar in shape and area. Consecutive pulses would only repeat the trajectory of the third loop and result in the same close-loop area. Therefore, in the following study, the third B-H loop cycle is captured for core loss calculation and the proposed test approach is therefore called TPT. Note TPT procedure should not make any differences compared to the B-H loop measurement used in other studies, since it only intends to measure the first steady-state B-H loop and avoid further unnecessary operations. The number of required cycles may vary depending on the inductor-under-test.

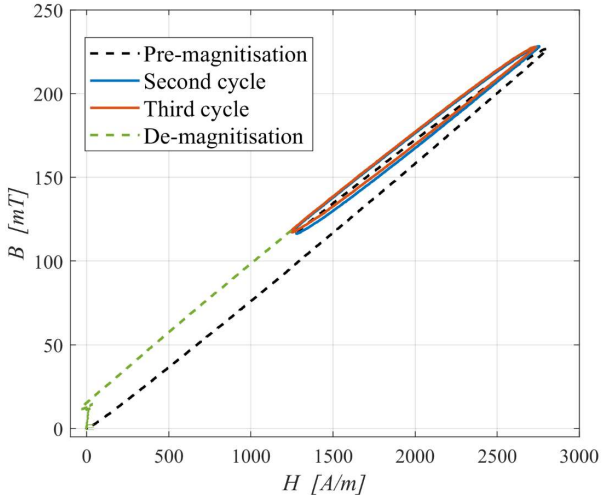


Figure 5-6. Example of measured B-H trajectory from Triple Pulse Test (H0 ≈ 2000 A/m, ΔB ≈ 130 mT)

The concept of this proposed TPT is analogous to the Double Pulse Test (DPT) [52], which is widely used for evaluating the switching loss of a semiconductor device (e.g. IGBT or MOSFET). Therefore, it is relatively easy for engineers who are familiar with DPT to adopt the TPT approach for inductor core loss characterisation. A comparison between these two test procedures is presented in Table 5-1.

TABLE 5-1. COMPARISON BETWEEN DPT AND TPT

	DPT for power devices	TPT for inductors
Initialization pulse(s)	To build up the switching current I_0	To build up pre-magnetisation H_0
Pulse of interest	Rising edge for turn-on loss Falling edge for turn-off loss	A closed B-H loop with H_0 and ΔB
Voltage U	Switching voltage U_{sw}	Flux density change rate dB/dt
$T1$	Determined by U_{sw}, I_0	Determined by dB/dt, H_0
$T2-$/ $T2+$	Not relevant	Determined by dB/dt and ΔB

5.2.4 Test setup

The customised inductor-under-test is shown in Figure 5-7, with the parameters listed in Table 5-2. It is formed by EE cores (double E-core) made from Cobalt Iron (CoFe) laminations. The rated current of the inductor is 78 Arms. This inductor is designed as the output current ripple filter of the ASR system as introduced in Section 4.2.3.

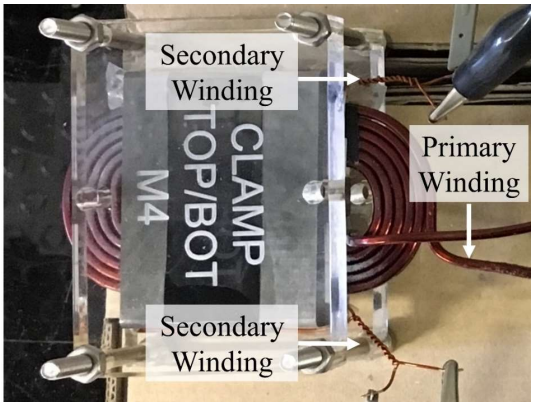


Figure 5-7. The tested inductor with added secondary windings for TPT

The airgap is at the central leg of the EE core with a length l_g of 0.52 mm. The copper windings are spaced away from the central leg for larger than four times l_g to avoid the fringing flux effect.

TABLE 5-2. SPECIFICATIONS OF THE INDUCTOR UNDER TEST

Core Material	VACOFLUX48 0.1mm Cobalt Iron laminations	Winding	1.9 * 2.8 mm rectangular copper
Air gap length l_g	0.52mm	Rated current	80 Arms
Shape	EE cores	Rated Inductance	36 µH
N1	6 turns	N2	3 turns

As illustrated in Figure 5-7 and in Table II, the primary winding (main inductor winding) has 6 turns. Two secondary windings, with three turns for each, are fitted for TPT at two side legs of the inductor to capture the flux on both sides in case of asymmetric flux distribution. In this case, the relationship between the two measured secondary voltages and the total flux density change is shown in equation (5-10)

$$U_{Lsec1} + U_{Lsec2} = N_2 \frac{d\Phi_1}{dt} + N_2 \frac{d\Phi_2}{dt} = N_2 \frac{d\Phi}{dt} = N_2 A_e \frac{dB}{dt} = U_{Lsec} \tag{5-10}$$

A test rig is built and shown in Figure 5-8, formed by DC-link, power converter and measurement probes.

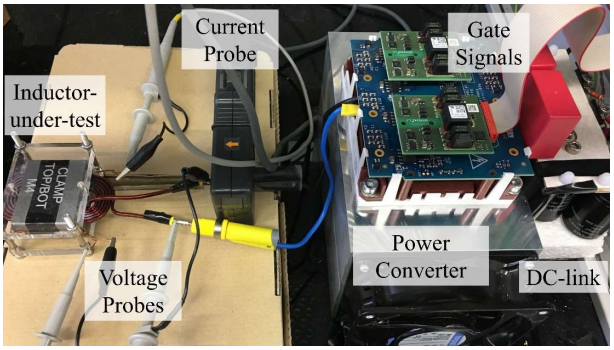


Figure 5-8. Test rig no. 3: B-H loop measurement

The signals are measured by high-bandwidth voltage and current probes shown in Table 5-3 and fed to a

digital oscilloscope. The phase discrepancy between the voltage and current probes is aligned by offline de-skew through a de-skew tool Keysight U1880A.

TABLE 5-3. INSTRUMENTS AND COMPONENTS IN THE TEST RIG

Power supply	Elektro-Automatik TS 8000 T	Power module	Semikron SKiM301TMLI12E4B
Voltage probe	Keysight N2862B (150 MHz)	Current probe	Keysight N2781B (10MHz)
Digital Oscilloscope	MSO-X 3054A (500 MHz, 4 GSa/s)		

5.3 Loss Map Approach

The above presented test rig and procedure enables the core loss measurement of the inductor. The following section elaborates how to establish a loss map based on finite measurements in order to estimate the core loss for PWM operations. As mentioned in the introduction, a loss map needs to be built up experimentally for a given inductor, which is a database of core loss that covers all possible operating points. For this purpose, the variables describing one operating point must be identified first. There are three known variables describing a closed B-H loop excited by symmetric square-wave excitation (regardless of the operating temperature):

A. Flux density change rate $|dB/dt|$. This variable is convertible to frequency f for repetitive symmetric excitation as appeared in a number of papers [142]. However, for an instantaneous point on the B-H trajectory, it is more suitable to refer this variable as $|dB/dt|$ rather than frequency. In the context of power electronics, $|dB/dt|$ is proportional to the amplitude of the applied square-wave voltage on the inductor. This is also pointed out in [146] and indicated in Improved Generalised Steinmetz Equation (5-9).

B. Flux density swing ΔB.

C. Pre-magnetisation/DC-bias of the magnetic field H_0.

Therefore, a loss map, a database of core loss, is a function of the above three variables, as expressed in

(5-11).

$$Q = f\left(\left|\frac{dB}{dt}\right|, \Delta B, H_0\right) \tag{5-11}$$

A loss map produced from finite discrete measurements can be utilized as a three-dimensional lookup table with interpolations or fitted curves/surfaces with mathematical expressions. For the first variable, it is reported that the effect of $|dB/dt|$ regarding core loss is independent from the other two variables ([129], [146], [148]). The correlation between the core loss and dB/dt is in the form of (5-12) as indicated in IGSE. Therefore, factor dB/dt can be assessed independently by only one set of data (i.e. fixed ΔB and H_0) to determine the coefficient α. This simplifies the loss mapping process by one dimension.

$$Q \propto \left(\left|\frac{dB}{dt}\right|\right)^{\alpha} \tag{5-12}$$

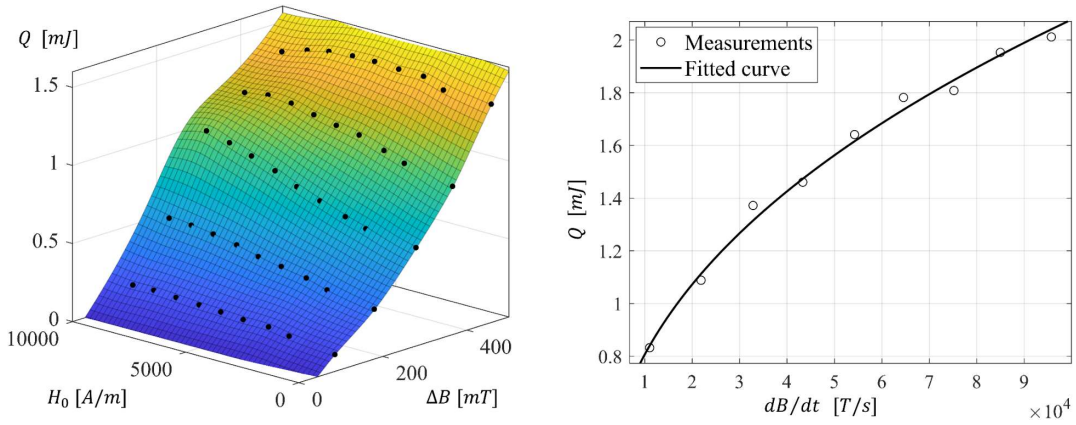
According to previous studies, the other two variables, ΔB and H_0, are coupled factors with respect to the core loss. Therefore, given a fixed dB/dt, data sets covering the possible operating region of interest formed by various ΔB and H_0 need be evaluated as shown in (13).

$$Q = \left(\left|\frac{dB}{dt}\right|\right)^{\alpha} \cdot f'(\Delta B, H_0) \tag{5-13}$$

To establish the loss map, the inductor-under-test is characterized experimentally using the test rig shown in Figure 5-8. The core loss measurement is conducted with the presented TPT procedure. The measured data of secondary voltage and primary current is then processed in Matlab following expressions (5-3)-(5-5).

The loss mapping process is conducted in two steps. Firstly, keeping $|dB/dt|$ (U_{L+} and U_{L-}) fixed, operating points with various ΔB and H_0 are tested. The results are shown in in Figure 5-9(a) in the form of a surface with thin spine interpolation. It shows that the relationship between H_0, ΔB and core loss Q is complex and difficult to be fitted with a generalised expression. This finding is similar to the previous studies [129]. Secondly, to determine the dependency of $|dB/dt|$, a set of points with constant ΔB and H_0 is realized by varying $|dB/dt|$. The results are

shown in Figure 5-9 (b). Curve fitting is performed on this set of data to determine the parameter α in (5-13). As can be seen from Figure 5-9 (b), the measured data is well fitted with a power equation as in (5-12).



(a) Q vs. ΔB, H0 (dB/dt = 21840 T/s) (b) Q vs. dB/dt (ΔB = 365 mT and H0 = 4000 A/m)

Figure 5-9. Loss map of tested inductor

5.3.1 Core Loss Calculation for PWM operations

The loss map developed above is based on closed B-H loops excited by symmetric square wave (duty cycle equals 50%, $U_{L+} = |U_{L-}|$) as shown in Figure 5-2. However, for filter inductors in PWM converters, it is more common to witness an asymmetric quasi-square-wave excitation $U_L(t)$ in each switching window as shown in Figure 5-10, where $U_{ab} \neq |U_{bc}|$ and $T_{ab} \neq T_{bc}$. The non-50-to-50 duty cycle is due to the Pulse Width Modulation. The unequal $|U_{ab}|$ and $|U_{bc}|$ are caused by the fundamental-frequency sinusoidal DC-bias.

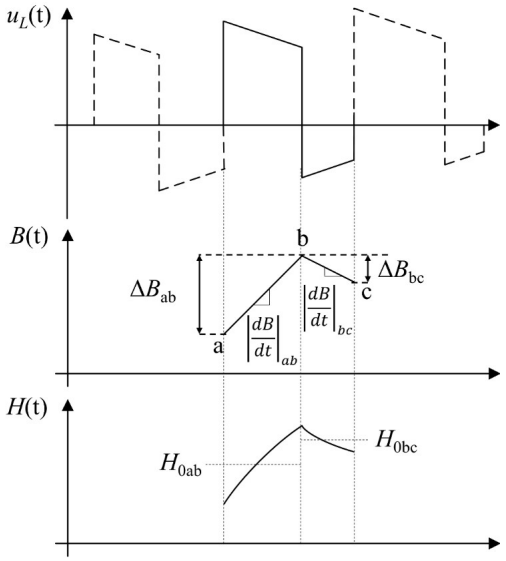


Figure 5-10. Typical waveforms of the filter inductor with a single-phase two-level PWM converter

To calculate the core loss for this type of waveform utilizing the loss map produced, an approach combining the piecewise concept of IGSE [125], [131], [133], [134] and revised loss map calculation [135], [136], [142] is adopted in this study. The idea of this approach is decomposing a given PWM waveform into calculable half-loop segments. One half-loop segment is either the positive half with dB/dt >0 (red part in Figure 5-11) or the negative half with dB/dt <0 (blue part in Figure 5-11) of a B-H loop.

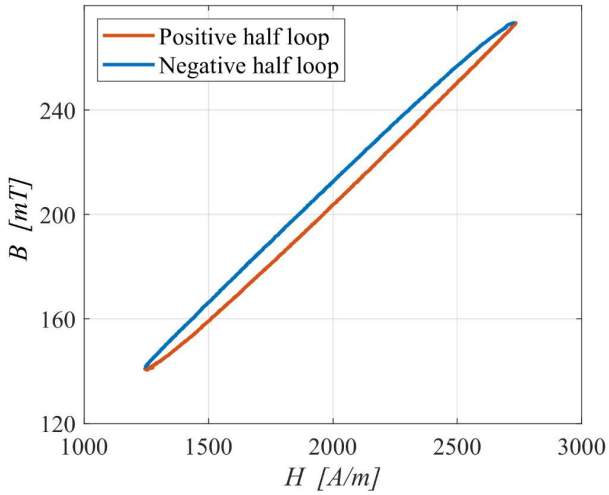


Figure 5-11. Example of a measured B-H loop excited by symmetric square wave with DC-bias ($H_0 \approx 2000$ A/m, $\Delta B \approx 130$ mT)

Three important assumptions are made in this approach:

1) The start/end points of one half-loop segment are considered at the moments where the polarity of dB/dt reverses, e.g. point a and point b shown in Figure 5-10. In the case of varying $|dB/dt|$ within one segment, the average value (e.g. $\Delta B_{ab}/T_{ab}$) is treated as the equivalent $|dB/dt|$. This is similar to the linear approximation (revised loss map approach) in [135], [142], [149], which has been proven to be accurate.

2) Considering the core loss is instantaneous, it is assumed that the positive half ($dB/dt > 0$) and the negative half ($dB/dt < 0$) each consumes 50% of the total energy loss of the closed B-H loop with symmetric excitation [135], [140], [149]. For example, the core loss of segment ab is obtained by

equation (5-14) from the loss map described by (5-11).

$$Q_{ab} = \frac{1}{2} \cdot f\left(\left|\frac{dB}{dt}\right|_{ab}, \Delta B_{ab}, H_{0_{ab}}\right) \tag{5-14}$$

3) The "relaxation effect" [131], [141], [147], [150], [151] is not considered, because the typical voltage applied on the filter inductors of PWM converters does not experience any periods with constant flux density ($U_L = 0$) due to the varying fundamental-frequency DC-bias.

Based on the above assumptions, a given quasi-square-wave excitation can be decomposed into *n* pieces of half-loop segments. Then the energy loss for each segment can be found individually through the loss map. The total power loss of a given waveform can be calculated by adding up the power losses of all half-loop segments that forms this waveform as expressed in (5-15).

$$Q_{total} = \sum_{n=1}^{n} Q_{(n)} \tag{5-15}$$

In this way, a switching window with non-50-to-50 duty cycle is decomposed into two half-loop segments, which are corresponding to a wider pulse and a narrower pulse. For instance, given the waveform *a* to *c* in Figure 5-10, the waveform is decomposed into wider segment *ab* and narrower segment *bc*. For segment *ab*, three descriptive variables of it, ΔB_{ab}, H_{0ab} and $|dB/dt|_{ab}$, are fed into the loss map to obtain the core loss Q_{ab} by (5-14). The narrower segment *bc* is equivalent to half a symmetric full cycle with higher frequency $1/2T_{bc}$ (i.e. higher *dB/dt*) in the loss map. The total core loss from point *a* to *c* equals to the sum of Q_{ab} and Q_{bc}. For more complex waveforms, such as PWM waveforms, they only need to be decomposed into finite piecewise half-loop segments following this approach. Note in Figure 5-9(b), the top right tested point reaches 365 mT with a speed of 9.6e4 T/s, which is equivalent to a 130 kHz symmetric positive-negative cycle. Therefore, the testing in this work equivalently covered a wide range of frequency. Theoretically, the presented approach can be extended to any frequency if the hardware allows.

5.3.2 User-Friendly Loss Map and Core Loss Calculation

As mentioned previously, this study aims at utilizing a pre-measured loss map, such as Figure 5-9, to estimate the core loss in a PWM converter, which is, specifically, to calculate the inductor core loss over a fundamental cycle of a PWM waveform. In this case, the steady-state PWM waveforms on the inductor must be provided and processed to be fed into the loss map, and the steady-state PWM waveforms are normally generated by simulations [152]. These waveforms are generated in the form of the inductor current I and voltage U_L. However the conventional loss map used in previous studies (e.g. [128], [143]) requires H/B waveforms in time-domain [152]. Referring to equations (5-3) and (5-4), to translate the voltage/current waveforms into H/B waveforms, it involves the geometry parameters of the inductor core, which introduces additional complexity and uncertainty. It has been pointed out in [140] that the inaccuracy of the effective dimensions of the core may lead to substantial errors in loss calculation, if the loss map is supplied in the form of loss density (e.g. J/m^3). In some cases, the accurate geometry information is not available, e.g. housed inductors. Therefore, it is motivated to convert the whole process into electrical and time-domain variables rather than H/B based, which is more user-friendly in practice.

Figure 5-12 shows one sample segment in time-domain. Two consecutive zero-crossings of the inductor primary voltage U_{Lpri} are detected as the start/end point of one half-loop segment.

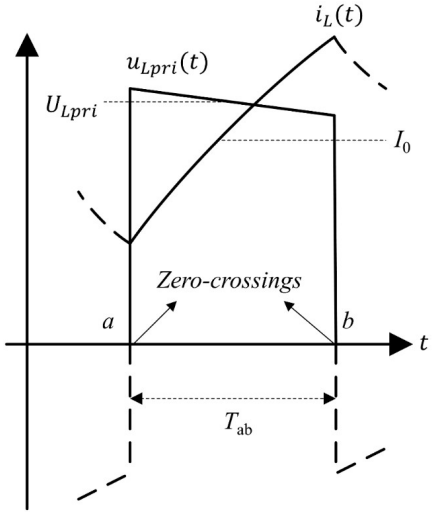


Figure 5-12. Example of half-loop segment ab with only electrical and time-domain measurements

For an individual inductor, the loss map in magnetic/time domain can be converted into electrical/time domain following equations (5-16)-(5-18), assuming $U_{L1}/U_{L2} = N1/N2$. The average current I_0 of this segment corresponds to H_0, as in (5-16). The time duration T_{ab} and average primary inductor voltage U_{Lpri} correspond to ΔB and dB/dt respectively as shown in (5-17) and (5-18).

$$H_0 = \frac{1}{T_{ab}} \cdot \frac{N_1}{l_e} \int_a^b i(t)dt = I_0 \cdot \frac{N_1}{l_e} \tag{5-16}$$

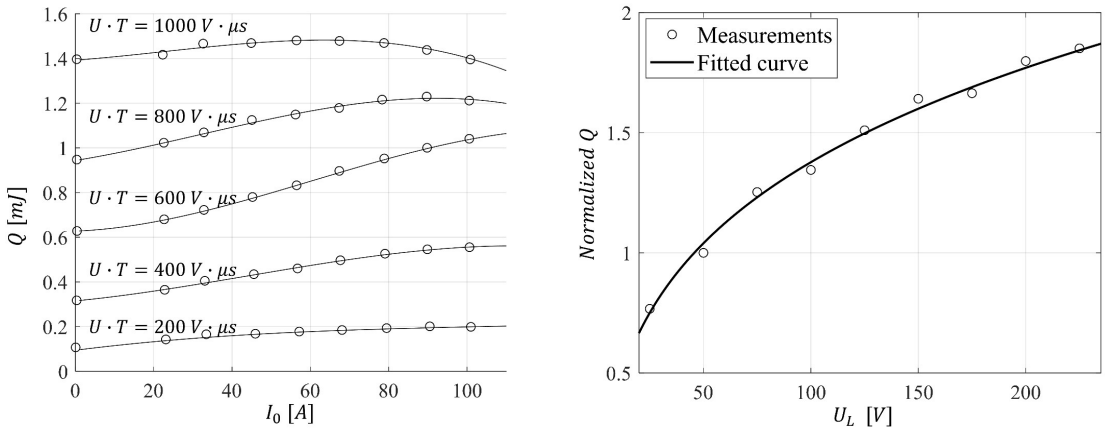
$$\frac{dB}{dt} = \frac{1}{T_{ab}} \frac{1}{N_2 A_e} \int_a^b U_{Lsec}(t)\, dt = U_{Lpri} \cdot \frac{1}{N_1 A_e} \tag{5-17}$$

$$\Delta B = \frac{1}{N_2 A_e} \int_a^b U_{Lsec}(t)\, dt = U_{Lpri} \cdot T_{ab} \cdot \frac{1}{N_1 A_e} \tag{5-18}$$

In this way, the loss map generated can be converted to the form expressed as (5-19) with electrical and time-domain variables for one particular tested inductor. It becomes a look-up table with three inputs: average inductor voltage U_{Lpri}, volt-time product $U_{Lpri}T$ and DC-biased current I_0. The output Q is the energy loss of a half-loop segment in *mJ*.

$$Q = g\left(U_{Lpri}, U_{Lpri}T_{ab}, I_0\right) \tag{5-19}$$

This form of loss map will not only enable more straightforward core loss calculation, but also simplify the loss mapping process, compared to magnetic-domain loss map. The electrical and time-domain parameters (pulse width and height) required in the Triple Pulse Test can be obtained directly give an target operating point on the user-friendly loss map, without translating from magnetic domain. Furthermore, it is also difficult to illustrate the conventional three-dimensional loss map in surfaces for practical purposes, e.g. to present in a datasheet. Therefore, a core loss profile presented in curves is proposed in this work as follows. Figure 5-13(a) shows the energy loss in *mJ* versus the biased current I_0, with various sets of volt-time product in $V{\cdot}\mu s$ (corresponding to ΔB).



(a) Q vs. U_L·T and I0 (UL = 50 V) (b) Q vs. U_L normalized to 50 V

Figure 5-13. User-friendly loss map of tested inductor

It is noticeable that the effect of I_0 is not identical for each set of data with the same volt-time product. But for each individual set, it can be well fitted with a cubic function. Operating points in between the curves can be obtained by interpolation. Converted from Figure 5-9(b), Figure 5-13(b) illustrates the core loss normalized to 50 V with respect to the inductor voltage U_L, as the testing voltage for Figure 5-13(a) is ±50 V. These curves shown Figure 5-13 can be printed on datasheets by the manufacturers of inductors.

To summarize, the energy of a half-loop segment can be found from a user-friendly loss map by two steps: (A) Input $U_L \cdot T$ and I_0 to Figure 5-13(a) to find the energy in mJ. (B) Input U_L to Figure 5-13(b) to scale the energy with respect to the testing voltage ±50 V. The core loss calculation flow following the above description is shown in Figure 5-14. In the case of a PWM waveform, it is decomposed into half-loop segments ($n = 2 \cdot f_{sw} / f_0$) for each fundamental cycle, and the energy loss of each single segment is calculated and summed up. As an example, consider a single-phase two-level converter is outputting a PWM waveform with 50 Hz fundamental frequency and 20 kHz switching frequency with a modulation index less than 1. In this case, 400 positive and 400 negative half-loop segments can be extracted from one fundamental cycle. This calculation flow can be easily implemented as an automated block either in simulation models or experimental evaluation, once the loss map of a specific inductor is pre-built with the boundaries covering possible operating plane.

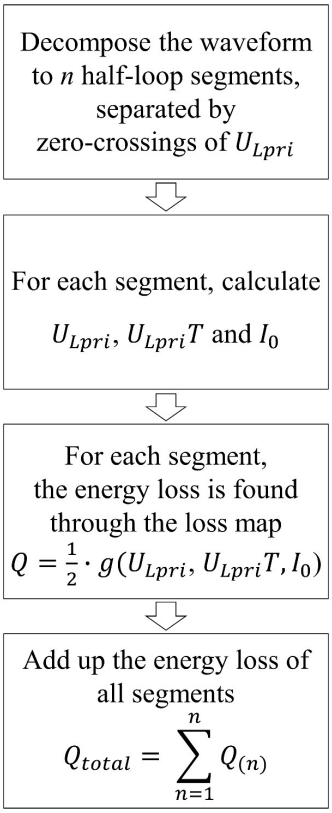


Figure 5-14. Core loss calculation flow for a given voltage/current waveform

5.4 Analytical loss map inputs for two-level and three-level PWM converters

For core loss estimation purpose, apart from a loss map, the inputs of the loss map, i.e. the steady-state PWM waveforms, need to be retrieved. One approach is to draw the waveforms from a simulation model [152]. But time-domain simulations are time-consuming and difficult to be integrated into mathematical models and iterative optimisation tools.

Hence, it is motivated to generate the inputs analytically for core loss estimation. There are previous studies that presented analytical approaches of estimating the core loss, such as [153]–[156]. However, [153], [156] are based on Steinmetz Equation (SE) and Improved Generalized Steinmetz Equation (IGSE), which have not considered the effect of pre-magnetisation. In addition, these studies mainly focused on the line inductors in two-level Power Factor Correction (PFC) converters.

This section establishes the analytical loss map inputs for both the two-level and three-level converters.

5.4.1 Analytical core loss model in a two-level converter

To start with, a single-phase, two-level, grid-connected STATCOM system is considered as an example as shown in Figure 5-15, which is in principle the same as the ASR system under investigation.

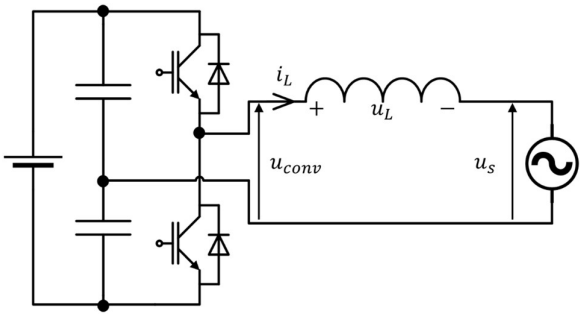


Figure 5-15. Grid-tied single-phase two-level converter

From the grid-frequency point of view, the phase/amplitude relationships of the currents/voltages in this system can be found from the phasor diagram in Figure 1-4. From the inductor point of view, the operation of the system can then be represented by Figure 5-16 [157]. The converter on one side is generating varying-duty-cycle square waves on switching window basis. On the other side, the grid is a stable source of sinusoidal voltage u_s with a frequency of f_0.

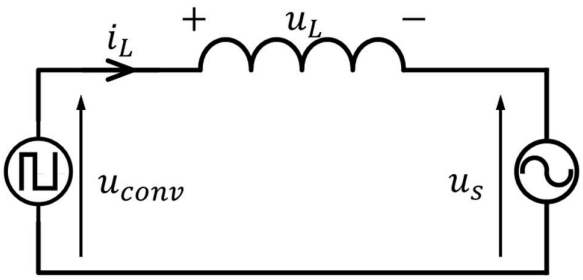


Figure 5-16. Equivalent circuit for core loss calculation

In this equivalent circuit, the inductor voltage u_L is found from the converter output voltage u_{conv} and the grid voltage u_s as

$$u_L(t) = u_{conv}(t) - u_s(t) \tag{5-20}$$

Another example is a converter-fed passive load with a LC low-pass filter as shown in Figure 5-17.

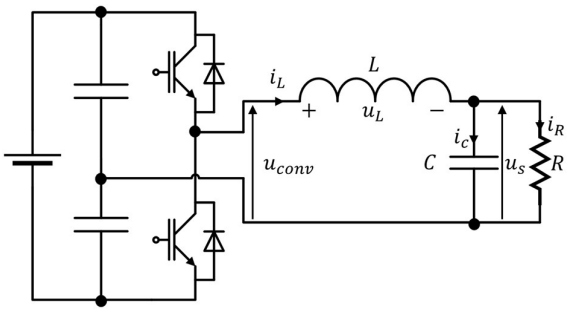


Figure 5-17. Two-level inverter with a passive load and low-pass LC filter

The phasor diagram of this configuration can be derived as in Figure 5-18.

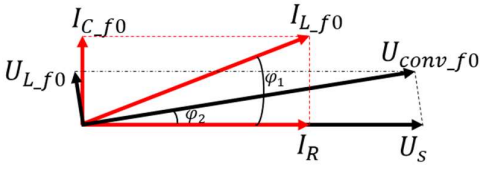
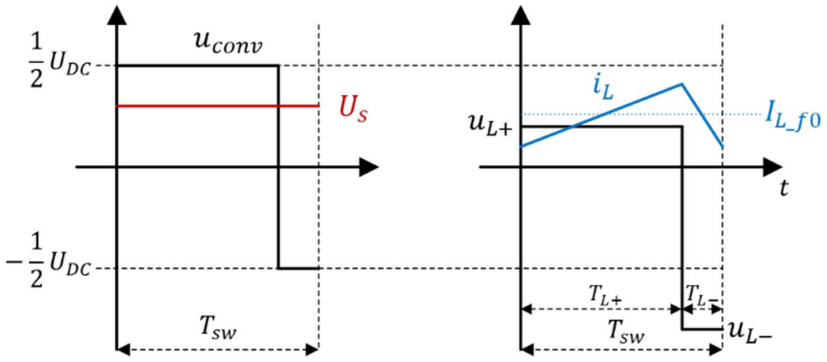


Figure 5-18. Phasor diagram of converter with RLC load at fundamental frequency

For simplification, it can also be assumed that the filtered load voltage U_R is sinusoidal. In this case, the operation of the inductor can also be represented by the equivalent circuit shown in Figure 5-16.

Assuming the converter switching frequency $f_{SW} >> f_0$, the grid/load voltage u_s can be treated as constant in each switching window. Subsequently, the converter voltage and grid voltage in one switching window is considered as illustrated in Figure 5-19 (a).



(a) (b)

Figure 5-19. Example of a two-level converter in one switching window ($U_{ref}>0$)
(a) converter output voltage, grid/load voltage (b) inductor voltage/current

In the +DC cycle, the converter outputs $+U_{DC}/2$. In the −DC cycle, the converter outputs $-U_{DC}/2$. Following (5-20), the inductor voltage u_{L+}/u_{L-} in each switching window can be found by (5-21) and (5-22) for +DC/−DC cycles respectively, as illustrated in Figure 5-19(b).

$$U_{L+} = \frac{U_{DC}}{2} - U_s \tag{5-21}$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \tag{5-22}$$

In order to utilize the user-friendly loss map (5-19), the three inputs must be found for each segment, which are $U_L T$, U_L and I_0. As mentioned, the segments are separated by the zero crossings of the inductor voltage u_L. As shown in Figure 5-19(b), the instants zero-crossings of u_L can be treated the same as the converter voltage. Therefore, in one switching window, the +DC cycle corresponds to the positive segment; the −DC cycle corresponds to the negative segment.

The time duration and duty cycles of u_{conv} can be found from the reference voltage of the converter, which is U_{conv_f0}. Assuming conventional SPWM is applied, the duty cycles of the +DC/−DC cycles in one switching window can be calculated by (5-23), (5-24), which are explained in Section 2.4. And the time durations are found from the duty cycles by (5-25).

$$D_{L+} = \left[\frac{U_{conv\_f0}}{(U_{DC}/2)} + 1\right]/2 \tag{5-23}$$

$$D_{L-} = 1 - D_{L+} \tag{5-24}$$

$$T_{L+/L-} = D_{L+/L-} \cdot \frac{1}{f_{sw}} \tag{5-25}$$

The DC-bias current I_0 for the segments can also be found from the fundamental component of the inductor current I_{L_f0} as shown in Figure 5-19(b). The I_{L_f0} can be derived from the phasor diagrams such as Figure 5-18.

Following the above process, the three inputs of segments for the user-friendly loss map can be generated on switching window basis. In order to find the averaged core loss, the above process needs to be repeated for each switching window over one fundamental cycle. This process can be achieved by performing iterations in MATLAB. The whole process is visualized in Figure 5-20.

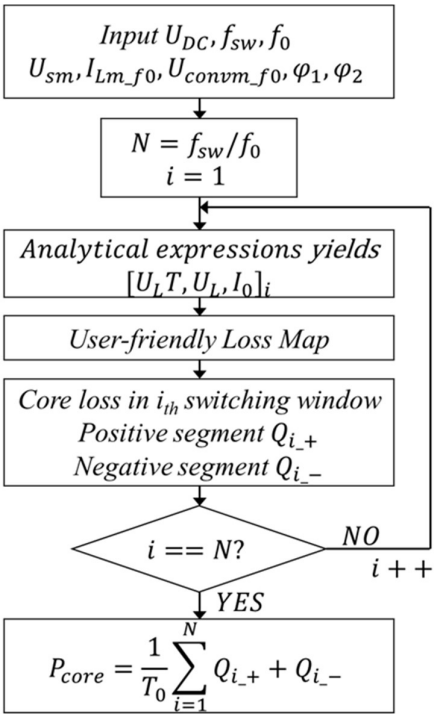


Figure 5-20 Analytical core loss computation process

As an example, assuming f_0 = 100 Hz and f_{sw} = 20 kHz, one fundamental cycle can be sliced up to N = 200 switching windows. Each switching window contains one positive segment and one negative segment (unless T_{+DC} or T_{-DC} equals to zero when the peak reference voltage reaches the modulation boundaries). For the i_{th} (i = *1…N*) switching window, three fundamental-frequency components are expressed by (5-26)-(5-28), with the phase angle referenced to the load/grid voltage.

$$U_s = U_{sm} \cdot \sin\left(\frac{i}{N} \cdot 2\pi\right) \tag{5-26}$$

$$I_{L\_f0} = I_{Lm\_f0} \cdot \sin\left(\frac{i}{N} \cdot 2\pi + \varphi_1\right) \tag{5-27}$$

$$U_{conv\_f0} = U_{convm\_f0} \cdot \sin\left(\frac{i}{N} \cdot 2\pi + \varphi_2\right) \tag{5-28}$$

Where U_{sm}, I_{Lm_f0}, U_{convm_f0} are the amplitudes of the fundamental-frequency load/grid voltage, inductor current and converter output voltage; φ_1 and φ_2 are the phase angles. All these constants can be found from the operating model of the converter and the load, i.e. the phasor diagrams. By inputting (5-21)-(5-28) into the loss map, the core loss of the i_{th} switching window can be calculated, which contains the core loss for the positive

segment Q_{i_+} and the negative segment Q_{i_-} in the form of energy.

Finally, the core losses of all switching windows are summed up to yield the total core loss of one fundamental cycle. Subsequently, the averaged core loss in power P_L can be obtained.

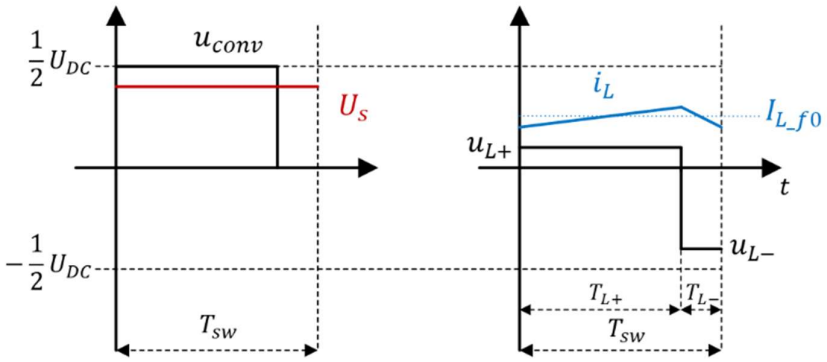
To summarize, for the analytical core loss estimation, the operation of the inductor is found by the equivalent circuit shown in Figure 5-16 at switching window level. To extract the inputs for the calculation, the amplitudes and phase relationships of the fundamental-frequency component of U_{conv_f0}, I_{L_f0} and U_s are found from the operating model of the converter and the load. These inputs associated with the converter/load operation are similar to the required parameters in the analytical model presented in CHAPTER 2. This feature enables the proposed core loss estimation to be directly integrated into the analytical system-level modelling of the power converter in this work.

Note the proposed approach only relies on the prediction of the converter output voltage rather than the instantaneous current ripple prediction at switching period level. Current ripple prediction (e.g. [103], [157]) assumes that the inductance L is constant for simplification. The presented approach will bypass the uncertainty of instantaneous inductance L at high frequencies. Additionally, the converter output voltage is easier to model in the discussed Voltage Source Converters (VSCs).

5.4.2 Analytical core loss model in a three-level converter

The above proposed analytical approach can be extended to a three-level converter. As elaborated in Section 2.5, a three-level converter outputs three voltage levels: positive DC rail voltage U_{+DC}, neutral point voltage U_{NP} and negative DC rail voltage U_{-DC}. With SPWM applied, in each switching window the ideal converter output voltage is formed by U_{+DC}/U_{NP} when $U_{ref} > 0$, or U_{-DC}/U_{NP} when $U_{ref} < 0$. Therefore, the inductor voltage is still a two-level square-wave within each switching window as shown in Figure 5-21, shifted up/down due to the

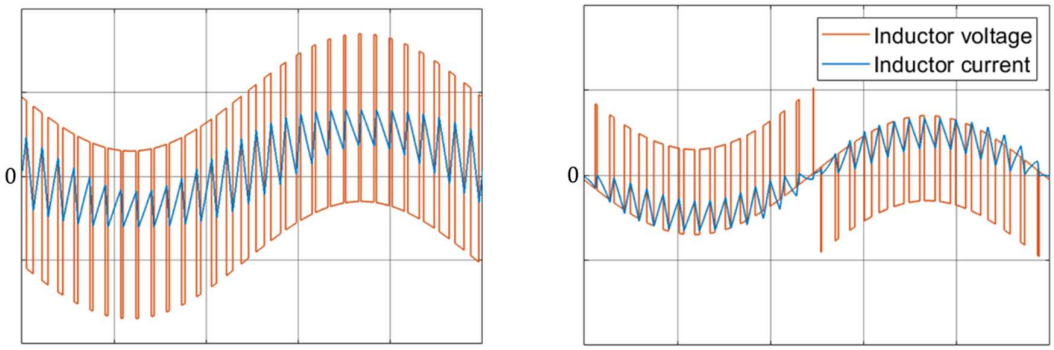
grid/load side voltage.



(a) (b)

Figure 5-21. Example of a three-level converter in one switching window (U_{ref}>0)
(a) converter output voltage, grid/load voltage (b) inductor voltage/current

Figure 5-22 shows a comparison of the inductor voltage/current waveforms in a two-level and a three-level converter with the same switching frequency f_{sw}.



(a) two-level converter (b) three-level converter

Figure 5-22. Example of inductor voltage/current waveforms over a fundamental cycle

The operation principle of a three-level converter is elaborated in Section 2.5. The duty cycles in a three-level converter can be derived from the reference voltage as following. When $U_{conv\_f0} \geq 0$, the duty cycles and inductor voltages are calculated from the expressions below

$$D_{+DC} = U_{conv_{f0}}/(U_{DC}/2) \tag{5-29}$$

$$D_{NP} = 1 - D_{+DC} \tag{5-30}$$

$$U_{L+} = \frac{U_{DC}}{2} - U_s \tag{5-31}$$

$$U_{L-} = 0 - U_s \tag{5-32}$$

When $U_{conv\_f0} \leq 0$, the duty cycles and inductor voltages are calculated from the expressions below

$$D_{-DC} = -U_{conv_{f0}}/(U_{DC}/2) \tag{5-33}$$

$$D_{NP} = 1 - D_{-DC} \tag{5-34}$$

$$U_{L+} = 0 - U_s \tag{5-35}$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \tag{5-36}$$

Hence, by replacing equations (5-21)-(5-25) with (5-29)-(5-36) in the calculation flow in Figure 5-20, the core loss of the inductor in a three-level converter can also be calculated.

In summary, the Sections 5.1-5.4 have elaborated the empirical characterization method and the loss map calculation approach of core loss. This whole process enables the analytical estimation of core loss in a PWM converter for a given operating point.

5.5 Analytical copper loss modelling

5.5.1 AC resistance of windings

The analytical model for copper loss estimation is presented as follows. Firstly, the DC resistance of the winding can be found as

$$R_{DC} = \frac{\rho_{cu} l_w}{A_{cu}} \tag{5-37}$$

Due to the exposure in high-frequency PWM excitation, both the skin effect and proximity effect [107] must be considered in the modelling of the copper loss. Considering both effects, the AC-to-DC resistance ratio F_R of the winding selected at a particular frequency can be calculated analytically. For example, the F_R of rectangular windings can be expressed as (5-38) ([107], [158]):

$$F_R = \frac{R_{AC}}{R_{DC}} = \frac{h}{\delta}\eta\left[\frac{\sinh\left(2\frac{h}{\delta}\right) + \sin\left(2\frac{h}{\delta}\right)}{\cosh\left(2\frac{h}{\delta}\right) - \cos\left(2\frac{h}{\delta}\right)} + \frac{2}{3}(N_l^2 - 1)\cdot\frac{\sinh\left(\frac{h}{\delta}\right) - \sin\left(\frac{h}{\delta}\right)}{\cosh\left(\frac{h}{\delta}\right) + \cos\left(\frac{h}{\delta}\right)}\right] \tag{5-38}$$

Where h is the thickness of the conductor; δ is the skin depth; η is the porosity factor; N_l is the layer numbers. The skin depth δ at a given frequency f is calculated as

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f}} \tag{5-39}$$

Where ρ is the resistivity of the conductor (1.724×10^{-8} Ω·m for copper at T = 20 ºC), μ_0 is the vacuum permeability ($4\pi \cdot 10^{-7}$ H/m).

The output current of the PWM converter contains a fundament sinusoidal component at f_0 and high frequency harmonics. The current can be decomposed to amplitude-frequency spectrum through Fourier Transform. For each frequency components, the AC resistance needs to be calculated individually. The total copper loss is obtained by adding up the copper losses for all the frequency components [107] as (5-40).

$$P_w = R_{wdc} I_0^2 + R_{wdc} \sum_{n=1}^{\infty} F_{Rn} I_n^2 \tag{5-40}$$

5.5.2 Analytical prediction of voltage/current harmonics

In order to calculate the copper loss through (5-40), the current harmonic contents need to be analytically predicted. In Voltage Source Converters, the current harmonic content can be predicted from the converter output voltage harmonics [155], [157], [159]–[162]. The output voltage harmonics in PWM converters are well analysed analytically in [159] based on Bessel Functions [163]. For a two-level converter with naturally sampled PWM, the time-varying phase leg output voltage can be expressed as follows [159]:

$$\begin{aligned} u_{an}(t) = & \frac{U_{DC}}{2} M cos(\omega_0 t + \theta_0) \\ & + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2U_{DC}}{m\pi} J_n\left(m\frac{\pi}{2}M\right) \sin\left((m+n)\frac{\pi}{2}\right) \cdot cos(m[\omega_{sw} t + \theta_{sw}] + n[\omega_0 t + \theta_0]) \end{aligned} \tag{5-41}$$

Where U_{DC} is the total DC-link voltage as defined in Figure 2-1; n is the multiplication index of fundamental frequency f_0; m is the multiplication index of the switching frequency f_{sw}; $J_n(x)$ is the Bessel function of order n and argument x. The combination of m and n represents the high-frequency harmonics content at multiples of the switching frequency and the side bands.

The amplitude of the voltage harmonic at a frequency $f_h = m \cdot f_{sw} + n \cdot f_{sw}$ is

$$\widehat{U}_{an(f_h)} = \frac{2U_{DC}}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin\left((m+n)\frac{\pi}{2}\right) \tag{5-42}$$

Next, the amplitude of the current harmonic content at frequency f can be expressed as (see [157])

$$\hat{I}_{a(f_h)} = \frac{\widehat{U}_{an(f)}}{L_a \cdot 2\pi f} \tag{5-43}$$

For three-level converters, the amplitude of the voltage harmonic at frequency f can be expressed as (5-44), when Phase Opposition Disposition (POD) modulation is applied.

$$\widehat{U}_{an(f_h)} = \frac{U_{DC}}{m\pi} J_{2n+1}(m\pi M)\cos(n\pi) \tag{5-44}$$

The above expressions enable the analytical calculation of copper loss for both the two-level and three-level converters given an operating point of the converter and the inductor design.

5.6 Experimental verification

5.6.1 Loss map approach and core loss calculation

To evaluate the proposed inductor loss model presented, an experiment was designed and conducted. A test rig was designed to feed the inductor-under-test with PWM excitation. As shown in Figure 5-23, the circuit is formed by a two-level converter with RLC load. The output of the power converter is filtered by the LC filter and applies on the load resistor.

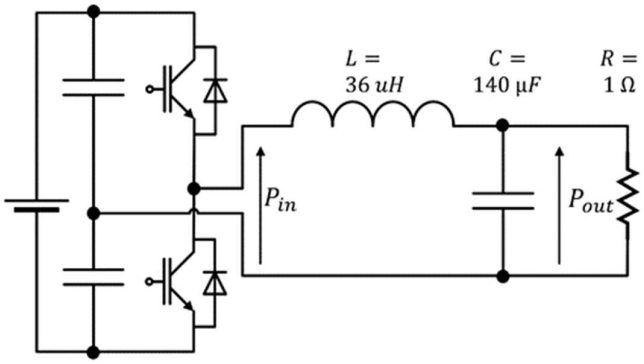
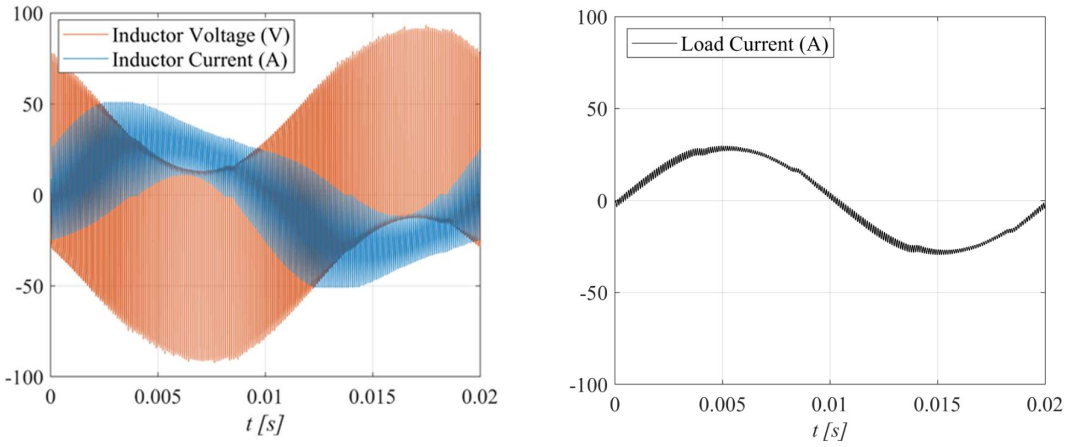


Figure 5-23. Single -phase two-level inverter

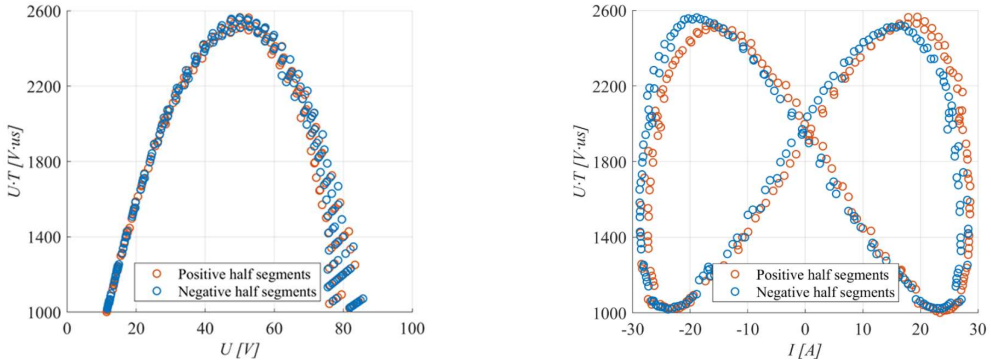
The inductor voltage/current waveforms are captured and fed into the loss map to calculate the core loss. The resulting measured waveforms of the inductor voltage and current, and the load current are shown in for one PWM operating point.



(a) inductor voltage and current (b) filtered load current

Figure 5-24. Experimental waveforms over one fundamental cycle
(U_{DC} = 100 V, M = 0.7 , f_{sw} = 10 kHz, f_0 = 50 Hz)

The voltage/current information measured was fed through the calculation flow shown in Figure 5-14 and the core loss for each segment is generated. The operating plane of the inductor described by the three variables is plotted in Figure 5-25 over a fundamental cycle. In this case, the inductor voltage varies between 10 ~ 90 Volts; The volt-time product varies between 1000 to 2500 Volts-microseconds. The biased current is between -30 ~ +30 A, equals to the filtered fundamental-frequency load current. The core loss of each segments is calculable as the pre-built loss map covers the whole operating plane.

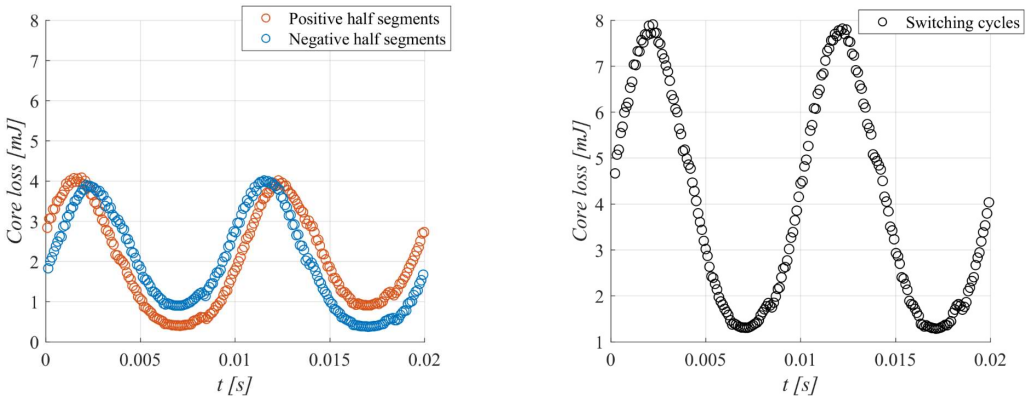


(a) U·T and U (b) U·T and I

Figure 5-25. Operating plane of the core over one fundamental cycle (U_{DC} = 100 V, M = 0.7 , f_{sw} = 10 kHz)

Calculated from the loss map approach, the instantaneous core loss is shown in Figure 5-26 over a

fundamental cycle. As f_{sw} = 10 kHz and f_0 = 50 Hz, the instantaneous core loss of 200 positive half segments and 200 negative half segments are found and plotted in Figure 5-26(a). Within each switching cycle, the core loss of the positive half and negative half are added up to obtain the instantaneous core loss of each switching window, which is plotted in Figure 5-26(b). It can be seen that, for one fundamental sinusoidal cycle, there are two peaks of the core loss occurring at maximum inductor current ripple.



(a) Plotted by half-loop segments (b) Plotted by switching cycles

Figure 5-26. Estimated core loss over one fundamental cycle (U_{DC} = 100 V, M = 0.7, f_{sw} = 10 kHz)

In addition to the core loss, the copper loss of the inductor can be estimated relatively accurately by the analytical models presented in Section 5.5. The DC resistance of the windings is measured at 3.59 mΩ by a DC Milliohm Meter. The measured inductor current is processed by Fast Fourier Transformation (FFT) in Matlab to extract the amplitude-frequency spectrum. The copper loss is then calculated through analytical models presented through (5-38)-(5-40) by inputting the amplitude-frequency spectrum of the measured inductor current.

The total power loss of the inductor is experimentally measured according to (5-45) by measuring the input (P_{in}) and output power (P_{out}) of the inductor (shown in (5-45)) with the power loss on the capacitor neglected.

$$P_L = P_{in} - P_{out} \tag{5-45}$$

The powers are obtained by mathematically integrating the instantaneous voltage-current product and averaging it over fundamental cycles, as in (5-46). The voltage and current signals are measured with the high-bandwidth voltage and current probes shown in Table 5-3 as in the TPT.

$$P = \frac{1}{2\pi}\int_0^{2\pi} U \cdot I \, d\theta \tag{5-46}$$

Rather than directly integrating the inductor voltage and current, the real power loss of the inductor is measured by P_{in}–P_{out} to reduce the error caused by the phase discrepancy of the probes. As demonstrated in [145], the greater power factor of a voltage-current pair has, the less error in the measured real power loss would be caused by the phase discrepancy.

The estimated inductor core loss using the approach proposed in this work and the calculated copper loss according to (5-40) are added up and compared with the experimentally measured total loss of the inductor. The results are shown in Figure 5-27, with several combinations of DC-link voltage and switching frequency.

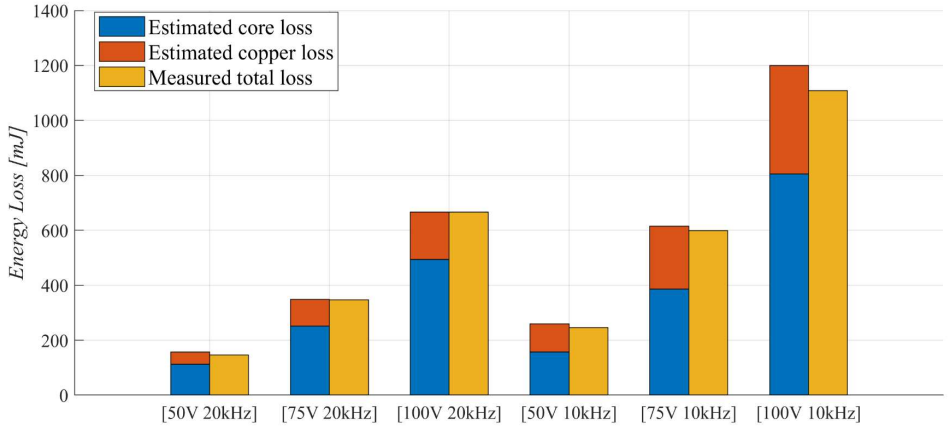


Figure 5-27. Experimental results of inductor losses over one fundamental cycle (0.02 s) with various combinations of U_{DC} and f_{sw}

It can be seen that the measured total power loss agrees very well with the sum of the estimated core loss and copper loss, with an average error of less than 5%. The results indicate that the inductor loss modelling approach proposed in this work is valid and accurate.

Note at the lower switching frequency, i.e. 10kHz, the core loss is higher due to larger swings of flux density ΔB of half-loop segments, which is proportional to volt-time product $U_L \cdot T$. Although the number of segments is doubled at 20 kHz, the larger ΔB ($U_L \cdot T$) of the segments in the 10 kHz case resulted in overall higher core loss.

5.6.2 Analytical loss map inputs for core loss estimation

Another experiment is designed and conducted to investigate whether the operating space and core loss of the inductor can be correctly predicted by the presented analytical model. A single-phase test rig with RLC load (Figure 5-16) is built with the specifications listed in Table 5-4.

TABLE 5-4. SPECIFICATIONS OF TEST RIG 4

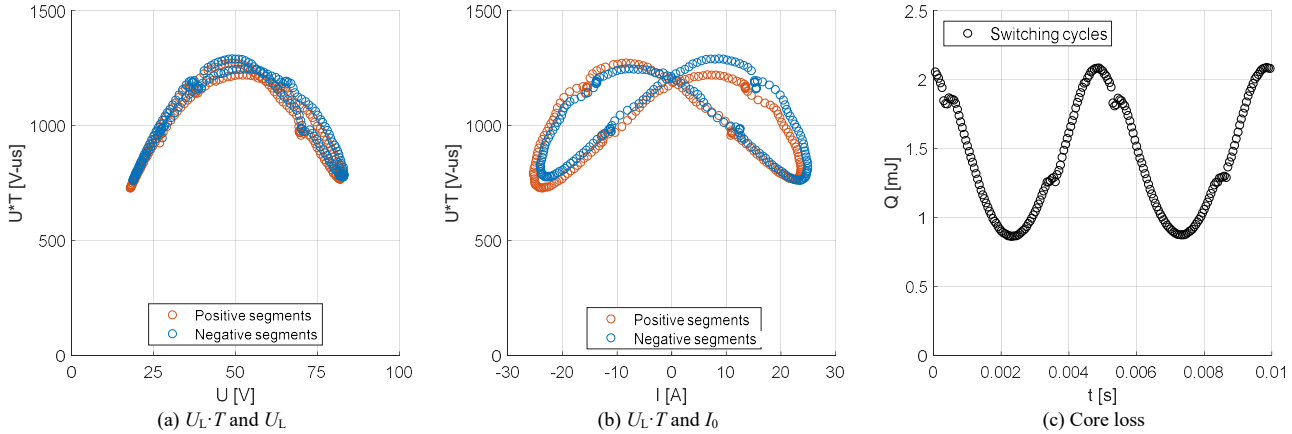
Fundamental frequency f_0	100 Hz	R	1.1 Ω
Switching frequency f_{sw}	10 kHz/20 kHz	L	36 µH
Dead time	2 µs	C	135 µF

Because the selected power module SKiM301TMLI12E4B is based on a *3LT* topology, it allows the operation either as a two-level converter or a three-level converter. This enables a straightforward comparison between these two converter topologies regarding the inductor core loss.

The power converter is programmed to operate as two setups: (A) a two-level converter with f_{sw} = 20 kHz; (B) a three-level converter with f_{sw} = 10 kHz. As discussed in Section 4.2, the inductance of the filter inductor in the discussed configuration is designed based on the maximum peak-to-peak current ripple $\Delta I_{MAXpk\text{-}pk}$ [52]. According to [103], a three-level converter offers approximately half the $\Delta I_{MAXpk\text{-}pk}$ compared to a two-level converter when the other parameters are the same. Therefore, if the same inductor is used, a three-level converter with $0.5f_{sw}$ can be considered equivalent to a two-level converter with f_{sw} from the $\Delta I_{MAXpk\text{-}pk}$ point of view. Hence, setup (A) and (B) provides a comparison between these two topologies on the same inductor with the $\Delta I_{MAXpk\text{-}pk}$ of both setups maintained equal. The experimental waveforms are measured and analysed through the loss map calculation process.

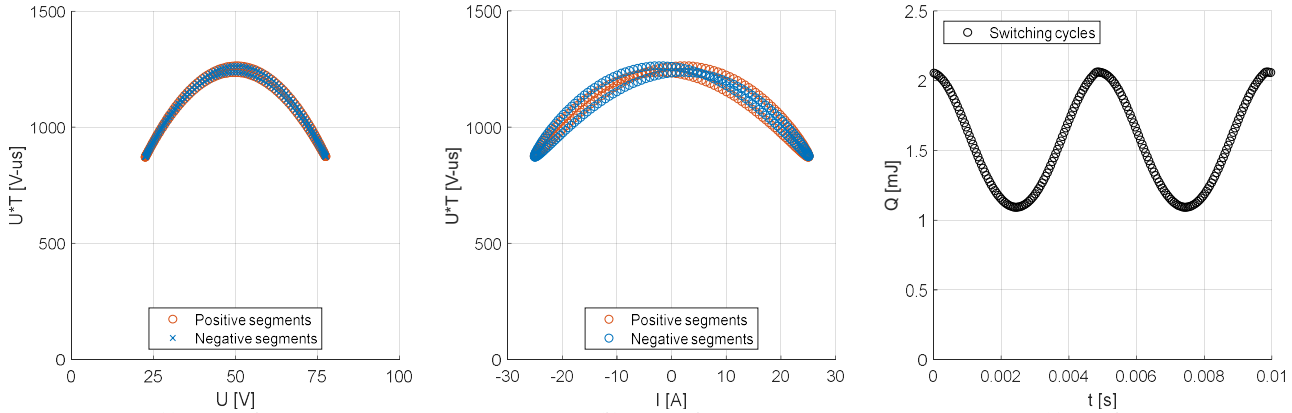
The results based on experimental measurements are visualized in Figure 5-28 and Figure 5-30 for the two-level and three-level setups respectively. Figure 5-28(a)(b) shows the operating space of the inductor core with respect to the three inputs of the loss map. Figure 5-28(c) shows the core loss calculated from the experimental waveform through the loss map approach.

In order to verify the proposed model, the parameters of the test rig are fed into the calculation flow presented in Figure 5-20 to analytically estimate the operating space and loss of the core. The analytically calculated results are plotted in Figure 5-29 and Figure 5-31 for the two-level and three-level setups respectively.



(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

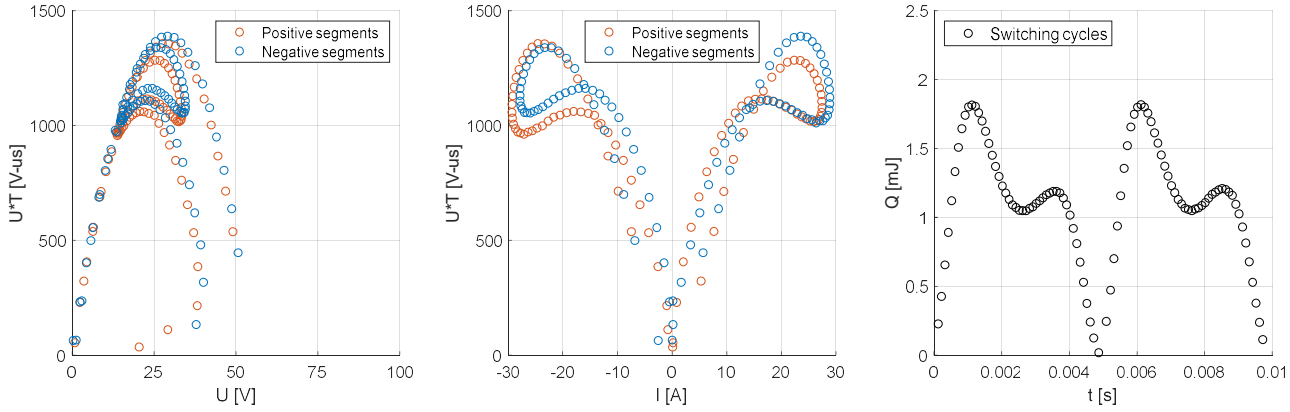
Figure 5-28. Operating space and core loss extracted from measurements in a two-level converter
U_{DC} = 100 V, $f$sw = 20 kHz, M = 0.7



(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

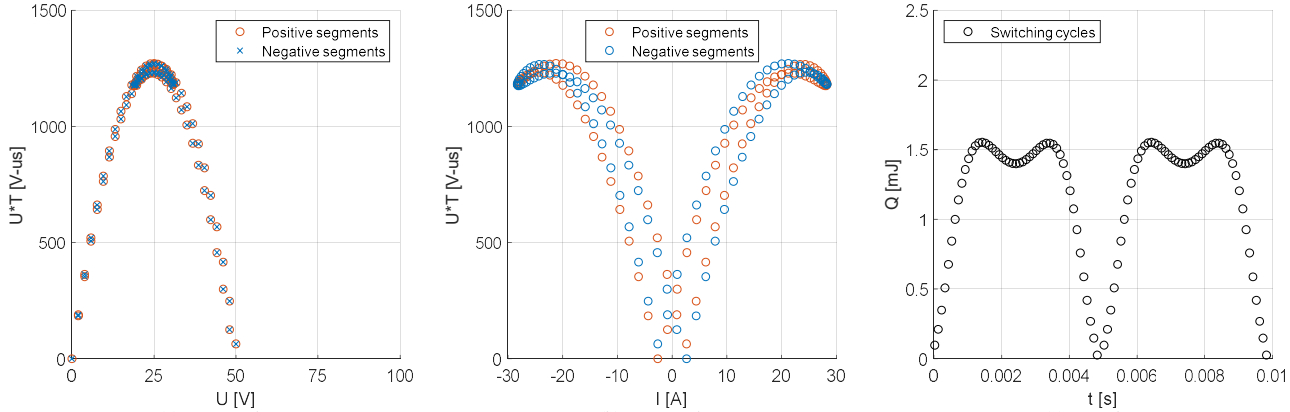
Figure 5-29. Operating space and core loss extracted from analytical model in a two-level converter
U_{DC} = 100 V, $f$sw = 20 kHz, M = 0.7

Comparing Figure 5-28 and Figure 5-29, it can be seen that both the operating space and the instantaneous core loss are well predicted by the analytical model in the two-level setup. The result shows that the core loss has two peaks over one fundamental cycle. Figure 5-30 and Figure 5-31 indicate that the theoretical estimation also agrees with the experimental results in the three-level setup, although there are visible discrepancies. These discrepancies are mainly caused by the non-ideal operation of the power converter and the load.



(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

Figure 5-30. Operating space and core loss extracted from measurements in a three-level converter
U_{DC} = 100 V, $f$sw = 10 kHz, M = 0.7



(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

Figure 5-31. Operating space and core loss extracted from analytical model in a three-level converter
U_{DC} = 100 V, $f$sw = 10 kHz, M = 0.7

A comparison of the averaged core loss in two setups is shown in Table 5-5.

TABLE 5-5. COMPARISON OF AVERAGED CORE LOSS

	Experimental	Analytical
Setup (A) two-level, f_{SW} = 20 kHz	28.5 W	31.0 W
Setup (B) three-level, f_{SW} =10 kHz	10.6 W	11.4 W

Table 5-5 indicate that the core loss derived experimentally agrees well with the theoretical results. The analytical model yields slightly higher core loss than the experimental results. It is also clear that the core loss in the three-level case is only approximately one third of the number in the two-level case.

Comparing the operating space in the two-level and three-level cases, the following findings can be observed. Given the same inductor, the halved switching frequency in the three-level setup leads to a similar peak $U_L T$ product as the two-level setup, which is around 1250 V-μs. This means the maximum current ripple $\Delta I_{MAXpk\text{-}pk}$ are

kept the same in the two cases as expected. From the amplitude of U_L point of view, it is clear that in the three-level converter the U_L of segments concentrated at around 25 V and reaches maximum at only 50 V. In the two-level case, U_L spreads between 25 V to 80 V. Additionally, in the three-level setup, there are a number of switching cycles where the inductor operates with low $U_L T$ product, e.g. < 500 V-μs. In the meantime, the $U_L T$ product in the two-level setup are all above 750 V-μs. Furthermore, the number of switching cycles is twice in the two-level converter to achieve the same peak current ripple. All these factors lead to the much smaller inductor core loss in the three-level converter as indicated in Table 5-5.

The discrepancy between the theoretical model and the experimental results are mainly caused by the following non-ideal factors of the setup:

- Dead-time effect.
- Trapezoidal converter output voltage instead of ideal square wave.
- Additional resistances in the converter-load loop, which is neglected in the presented model for simplicity.
- Fluctuation of the DC-link voltage and neutral point voltage. The DC-link voltages are assumed constant in the theoretical model while they fluctuate in the test rig.

5.7 Summary

This chapter investigates the modelling of the inductor loss. The inductor loss consists of the copper loss and the core loss. The copper loss can be relatively accurately estimated through analytical models that have been well established in the literatures.

The core loss is relatively challenging to model, especially in the case of PWM converters. The conventional

approach is through Steinmetz Equation and manufacturers' datasheets of inductor cores/materials, which are not sufficient for accurate modelling of core loss in PWM converters. The available datasheets are mainly based on sinusoidal excitation with the pre-magnetisation effect and the gap loss neglected.

To accurately characterize the core loss, an empirical test approach – B-H loop measurement is widely used in literatures. This work proposes a half-bridge based configuration as the power converter stage for the B-H loop measurement. The proposed configuration enables the compensation of asymmetric rectangular inductor voltage caused by the device voltage drops when the testing current is high (e.g. >100A). A test approach, Triple Pulse Test, is introduced to capture the core loss at a certain operating point. TPT procedure eases the requirement of the setup hardware due to short testing time window.

With the help of B-H loop measurement, a loss map can be established for the purpose of estimating the core loss in a PWM converter. This work proposes a user-friendly loss map for individual inductors which simplifies the calculation of core loss. The proposed user-friendly loss map only involves electrical parameters.

Given the pre-measured loss map, the current/voltage waveforms are still needed to calculate the averaged core loss, which were retrieved by simulations in previous studies. To provide a fast estimation, an analytical approach is proposed to generate the inputs for the loss map given an operating point of the PWM converter. The analytical model is developed for both two-level and three-level converters. Experiments are conducted to validate the proposed test approach and modelling. The results show consistency between the estimated core loss and the measurements, which confirms the accuracy of the inductor loss model.

CHAPTER 6

System-level Trade-off Analysis and Optimisation

In this chapter, the models of individual components are combined to form a quantified system-level view of the target ASR system. The aim is to build a mathematical tool which conduct designs and analysis linking the converter performance metrics with the primary design variable of the power converter, topology, power device and switching frequency f_{sw}. Figure 6-1 illustrates an overview of the components to be considered in this work.

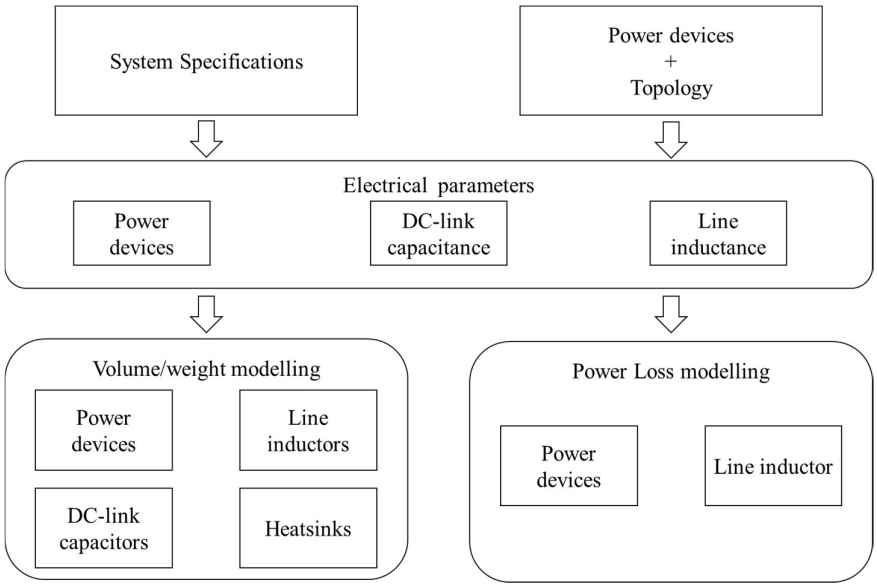


Figure 6-1. Overview of system-level trade-off analysis

The total power loss of the converter P_{loss_tot} is considered the sum of the power device losses P_{pd} and line inductor losses P_L

$$P_{loss\_tot} = P_{pd} + P_L \tag{6-1}$$

The total effective volume V_{total} in this study includes the power modules, heatsink, inductors and DC-link capacitors, which can be expressed as

$$V_{total} = V_{pm} + V_L + V_{cap} + V_{hs} \tag{6-2}$$

The design inputs, which are the specifications and constraints of the system, are listed in Table 6-1.

TABLE 6-1. DESIGN INPUTS

	Value
Phase current I_n	78 A
DC-link voltage U_{DC}	350 V
Fundamental frequency f_0	400 Hz
DC-link voltage ripple requirement	1%
Current Ripple requirement	20 %
Switching frequency f_{sw}	10 kHz ~ 100 kHz
Modulation Index M	dynamic
Ambient Air temperature	40 °C
Liquid coolant inlet temperature	80 °C

The detailed process of the optimisation algorithm is illustrated in Figure 6-2. A design space is firstly generated from combinations of considered topologies, power devices and a range of switching frequency. For each set of design from the design space, the passive components are tailored following to the design inputs. The performances of each components are estimated and recorded, which include power loss, volume and weight. Finally, all the designs and associated performance metrics are collected and visualized.

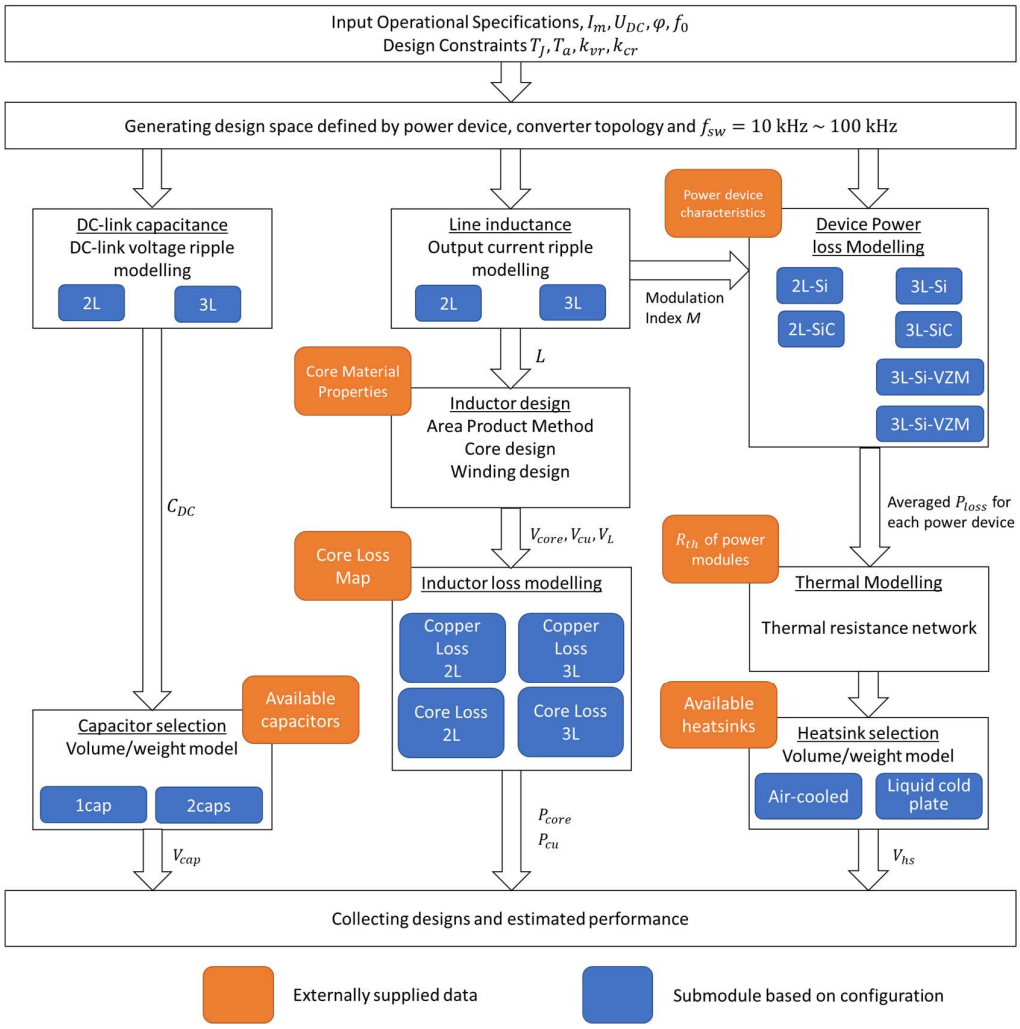


Figure 6-2. Process of analytical design optimisation

6.1 Efficiency analysis

As one of the main performance metrics of the converter system, power efficiency can be estimated through the models established in previous chapters. In the efficiency domain, the power devices and the inductor are both the major contributors of power loss. The device power losses over the discussed device-topologies combinations have been analysed in CHAPTER 2 through analytical models. Following designs of inductors conducted for each switching frequency following Section 4.2, the power loss of the line inductors can also be predicted through the models established in CHAPTER 5. Considering both elements, the converter relative efficiency is evaluated as a function of the switching frequency f_{sw} over various design options. The results are shown in Figure 6-3.

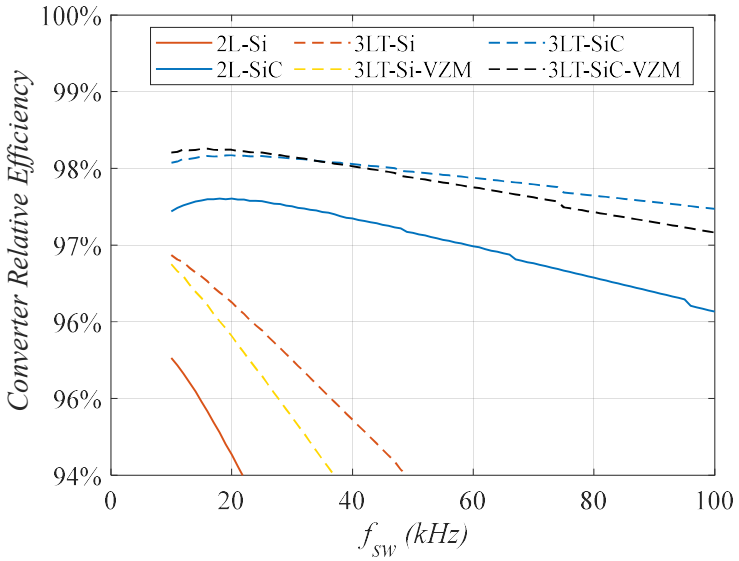


Figure 6-3. Converter overall relative efficiency considering power device losses and line inductor losses

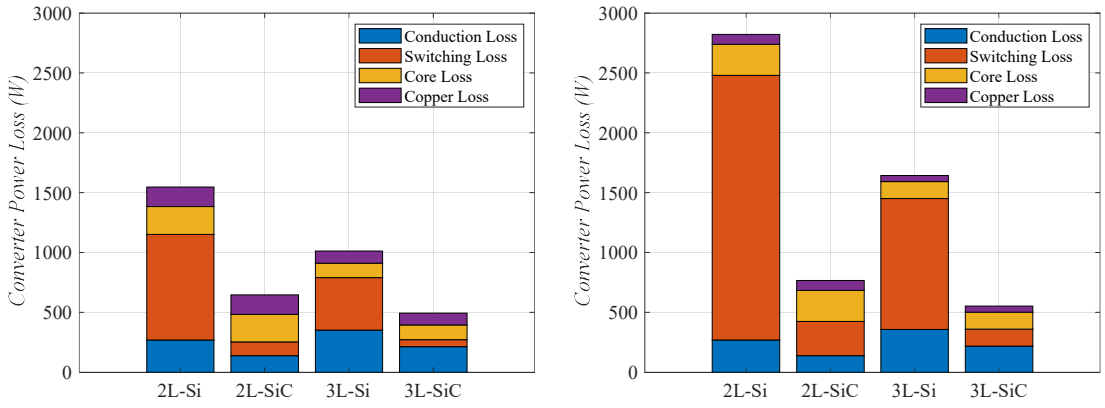
Compared to Figure 2-12, the estimated overall converter efficiency becomes nonlinear against the f_{sw}. The nonlinearity is a result of the nonlinear design of the inductor and associated inductor losses. Note the proximity effect of the copper loss is not considered in this analytical evaluation due to its complex dependency regarding physical winding placements.

For Si IGBT based options, the efficiencies drop dramatically along the f_{sw} axis, as a result of relatively high switching losses. The efficiency of the *3LT*-Si case drops less steep compared to the *2L*-Si case due to the benefits

of the three-level topology, but it still drops to less than 96% when the f_{sw} reaches 25 kHz. Therefore, Si IGBT based converters generally do not operate at over 25 kHz from the converter efficiency point of view.

The all-SiC based options offer better performance mainly due to reduced switching loss. Overall, the *3LT*-SiC case features the best efficiency performance, which maintains over 97.8% even when the f_{sw} is increased to 70 kHz. When the effect of VZM is considered to balance the DC-link capacitor voltages, the efficiency of *3LT*-SiC case drops slightly due to additional switching transitions, which is 0.2% difference at f_{sw} = 70 kHz.

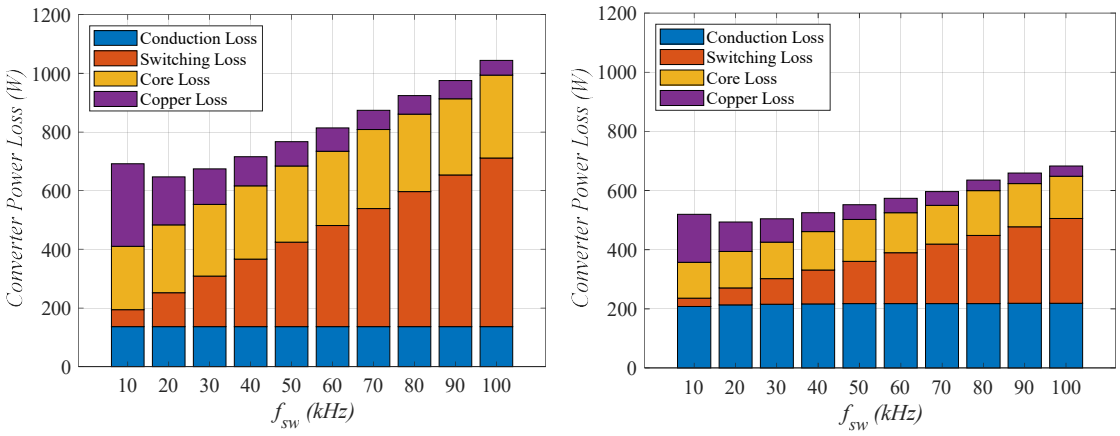
Slightly different to the conclusions in Section 2.6, the overall efficiency of the *2L*-SiC option is constantly smaller than the *3LT*-SiC case with the line inductor losses considered. But it can still maintain over 97% when the f_{sw} is increased to 60 kHz. As two examples, the composition of power losses at f_{sw} = 20 kHz and f_{sw} = 50 kHz are plotted in Figure 6-4 for four device-topology combinations.



(a) f_{sw} = 20 kHz (b) f_{sw} = 50 kHz

Figure 6-4. Power loss composition of four power device-topology combinations

It can be seen that, for Si IGBT based options, device losses are the main contributor (>70 %) to the total loss. For all-SiC options at f_{sw} = 50 kHz, the device loss and inductor loss nearly each contribute half to the total power loss. Figure 6-5 shows the changing trend of power loss composition over f_{sw} for SiC based options.



(a) *2L*-SiC (b) *3LT*-SiC

Figure 6-5. Power loss composition vs. f_{sw}

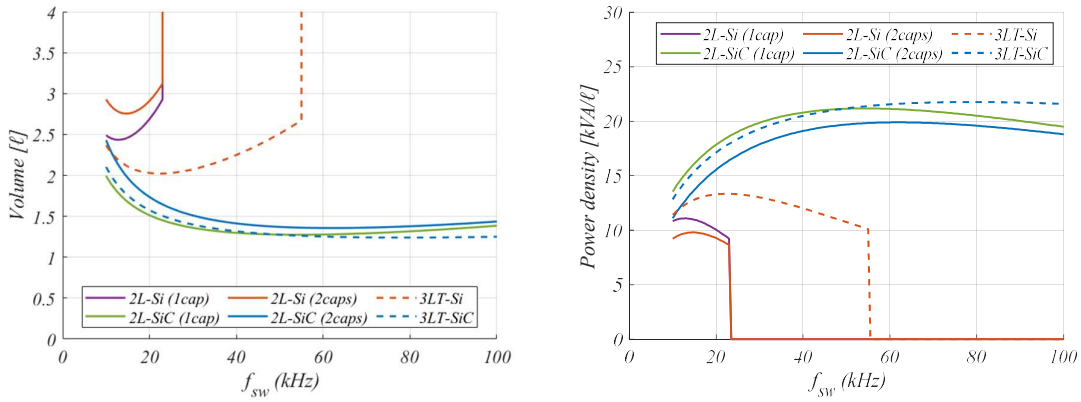
As shown in Figure 6-5, the lowest total power loss of both cases is achieved at around f_{sw} = 20 kHz. With the increasing of f_{sw}, the core loss rises while the copper loss drops in both cases. The decreasing of copper loss is mainly due to the reduced number of turns and subsequently the reduced DC resistance of the windings. Another finding is that the inductor loss can contribute substantially to the system power loss. For instance, at a switching frequency of <50 kHz in the *2L-SiC* case, the proportion of inductor loss even outweighs the power devices loss.

6.2 Power density/specific power analysis

As the other concerned performance metric of the power converter, the volume/weight and power density/specific power can be estimated through the established models.

6.2.1 Power density with forced-air cooling

By performing the process illustrated in Figure 6-2, the volumes and power densities across various converter configurations are evaluated as a function of the switching frequency f_{sw}. The results are shown in Figure 6-6.

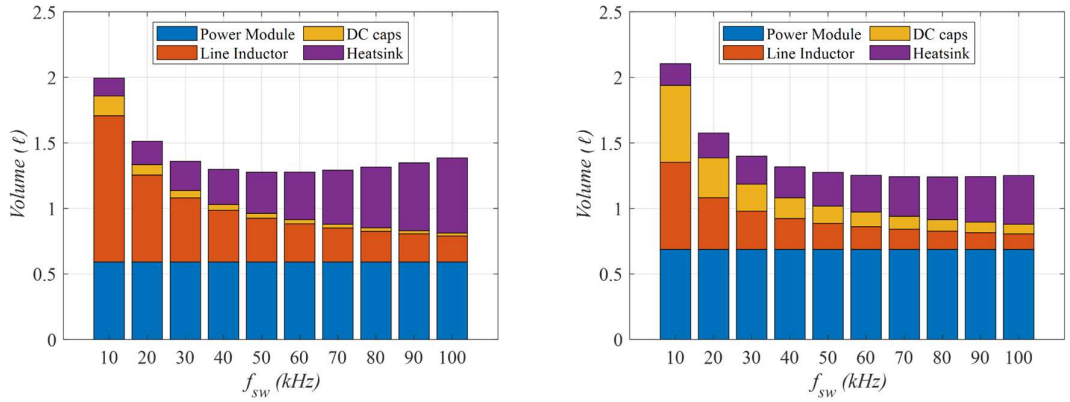


(a) Volume (b) Power density

Figure 6-6. Volumetric power density of target power converter with forced-air cooling

The Si IGBT based configurations show a steep drop of power density after 20 kHz due to substantial heatsink size as a result of high switching losses. From around 50 kHz onwards, due to the substantial power loss generated on the internal thermal resistances, there is no heatsink that can satisfy the pre-defined temperature rise. In this case, the size of the heatsink is considered infinite, and the power density drops to nearly zero as shown in Figure 6-6(b). As the last-generation commercial option, the maximum achievable power density of *2L-Si* is at 15 kHz at around 10 kVA/ℓ for the target application. By replacing the topology with the *3LT* topology, the Si based solution can endure slightly higher switching frequency, up to 55 kHz, and achieves a power density of 13 kVA/ℓ at around 23 kHz, as a result of reduced switching loss.

From the power density point of view, the top two competitive configurations are: (a) *2L*-SiC with single capacitor (b) *3LT*-SiC, which can both reach around 21 kVA/ℓ. The detailed composition of component volumes of these two configurations are plotted in Figure 6-7.



(a) *2L*-SiC with single capacitor (b) *3LT*-SiC

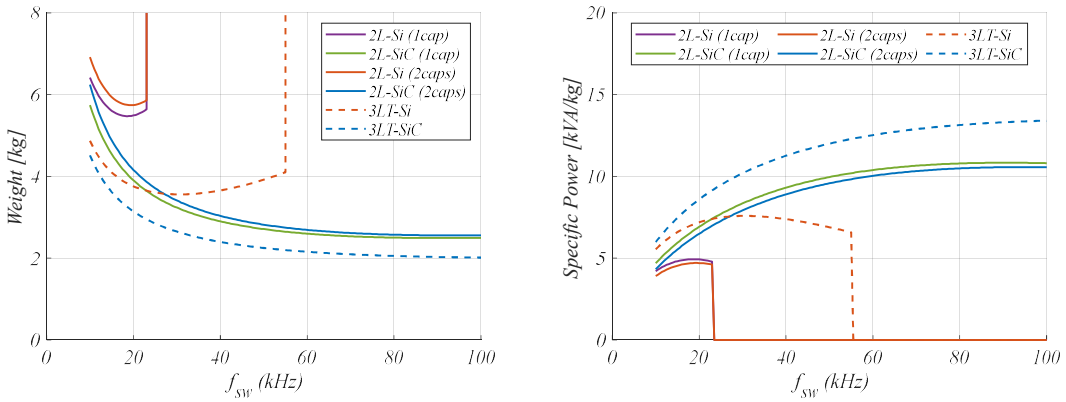
Figure 6-7. Component volume breakdown with forced air cooling vs. f_{sw}

One of the advantages of the *3LT* configuration is the reduced switching loss, especially at higher frequencies. This advantage leads to less cooling efforts required and hence smaller heatsink size. Another advantage is that *3LT* configuration only requires half of line inductance compared to the two-level option. However, as the main drawback, the *3LT* configuration requires nearly four times installed capacitor size compared to the single-capacitor two-level configuration. Additionally, the size of *3LT* power module is slightly bigger.

The main advantage of the *2L* configuration is that only one DC-link capacitor is needed, which leads to an approximately 75% reduction in capacitor size compared to the *3LT* configuration. Additionally, the *2L* power module size is slightly smaller in the studied commercial products. As the disadvantage, the *2L* topology results in larger inductors to satisfy the current ripple requirement and dramatic rise of switching loss with the increase of switching frequency.

6.2.2 Specific power with fored-air-cooling

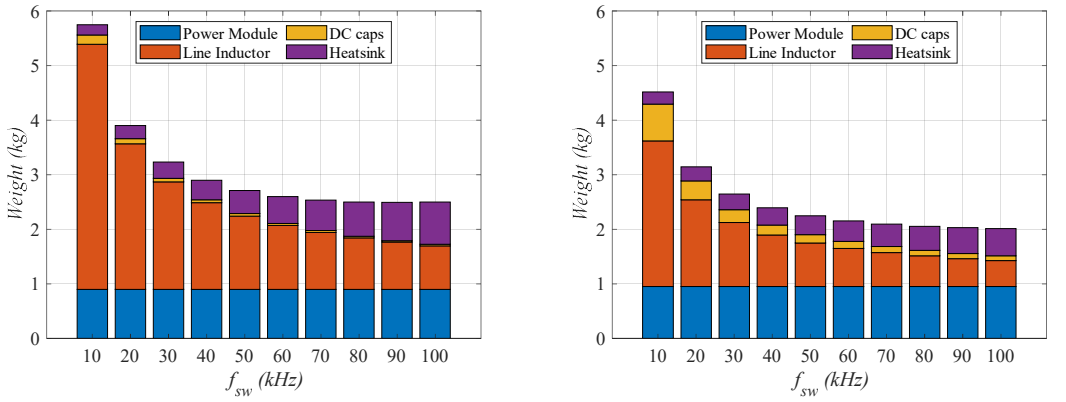
From the weight point of view, the performance of the power converter is evaluated as a function of f_{sw} with the results illustrated in Figure 6-8.



(a) Weight (b) Specific power

Figure 6-8. Weight/specific power of power converter with forced air cooling

As noticeable, the results indicate slightly different findings compared to the previous section. The *3LT*-SiC shows the most superior specific power, which reaches 13 kVA/kg at f_{sw} > 75 kHz. The *2L*-SiC configuration shows an achievable specific power at approximately 10 kVA/kg at f_{sw} > 60 kHz. The composition of the weight by components as shown in Figure 6-9.



(a) *2L*-SiC with single capacitor (b) *3LT*-SiC

Figure 6-9. Component weight breakdown with forced air cooling vs. f_{sw}

As the graph indicates, the line inductor contributes substantially to the weight, especially at the lower switching frequencies. For example, at 20 kHz, the line inductor accounts for 68% weight of the power converter.

From the density point of view, the average density of the capacitors is approximately 1.16 g/mℓ derived from the selected commercial products. The average density of the aluminum heatsink is 1.35 g/mℓ assuming half the heatsink is occupied by air. The inductor is mainly formed by the CoFe alloy and copper, with the densities of 8.12 g/mℓ and 8.96 g/mℓ respectively. This difference explains why the line inductor contributes to the weight

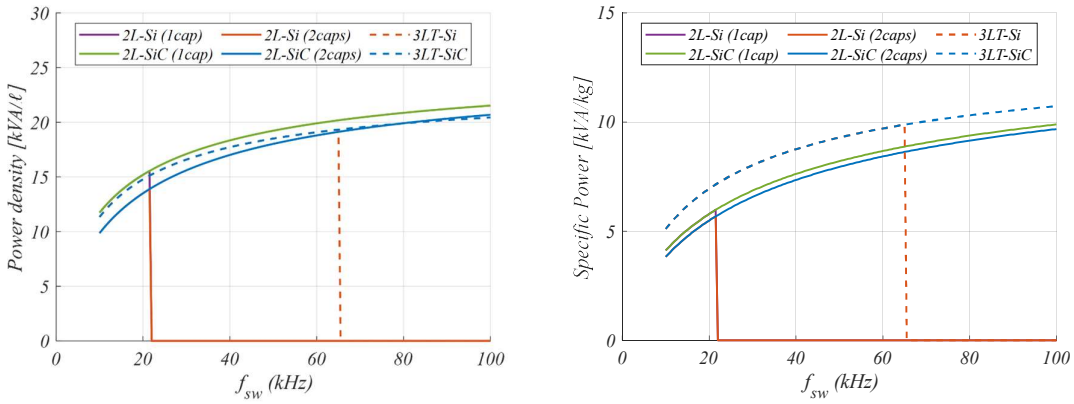
more substantially compared to volume. Therefore, reducing the size of the line inductors presents priority in the weight optimisation of the converter.

According to the model presented in 4.2.1, rising the operating switching frequency f_{sw} is the most effective mean to shrink the inductor size from the design point of view. From this angle, implementing SiC devices enables the converter to operate at higher switching frequency without breaking the thermal limit. Meanwhile, deploying the three-level topology leads to nearly half of the required inductor size compared to the two-level topology.

6.2.3 Power density/specific power with liquid cold plate

To adapt to the harsh environment on an aircraft, e.g. low air pressure, it is preferred in practical to use liquid cooling over air cooling in certain applications. Apart from considering the harsh environment, sharing the existing liquid cooling system with the electric machine can yield better power density of the whole integrated generator/converter system. As discussed in Section 4.3, the size of liquid-cooled cold plate is relatively insensitive to the required thermal resistance. Referring to Figure 4-11, a cold plate provides ample cooling for the power modules in the studied case, of which the size is mainly constrained by the bottom surface area of the power module and internal configuration of the liquid flow path (e.g. tubes or mini-channels).

Considering the volume/weight of the cold plate to be constant, the remaining variables contributing to the converter volume/weight are only the line inductors and DC-link capacitors. The cost of rising the f_{sw} – the increased switching loss is no longer reflected on the size of the heatsink, as the cold plate is fixed. In this case, the power density/specific power of the converter is assessed and plotted in Figure 6-10.



(a) Power density (b) Specific power

Figure 6-10. Power density/specific power of power converter with cold plate

As the f_{sw} rises, the power density/specific power curves show a constant rising trend reflecting the reduction of filter components size. From the volume point of view, the *2L-SiC(1cap)* case shows the highest achievable power density, which benefits from the single DC-link capacitor configuration compared to the three-level option. From the weight point of view, *3L-SiC* shows the best performance due to the benefit in the reduction of the line inductor.

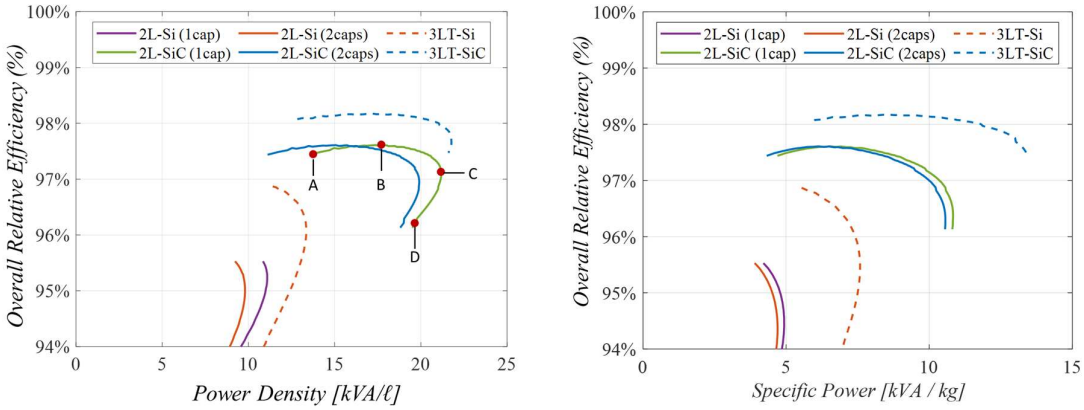
For the Si based options, the cold plate allows them to operate at a higher switching frequency without paying the penalty on the heatsink size. Therefore, the Si based options can achieve a better power density compared with the air-cooled case by rising the switching frequency. For example, the cold plate enables the *3LT*-Si configuration to run at a higher switching frequency, 64 kHz instead of 55 kHz. This enables the *3LT* -Si configuration to achieve 9.8 kVA/kg and 19.33 kVA/ℓ at 65 kHz, with an efficiency of 92.7%.

6.3 Multi-objective optimisation

As discussed in Section 1.4, a multi-objective optimisation is target in this work, which shows the design trade-offs between the metrics of interest, i.e. efficiency, power density and specific power. This optimisation is intended to provide a guidance for the initial design of the power converter.

The Pareto Front analysis has been proposed and conducted in [77] to identify the performance limit

considering both the efficiency and power density of the converter. The efficiency-power density and efficiency-specific power Pareto Front of the system with air-cooled heatsinks are shown in Figure 6-11.



(a) Power density (b) Specific power

Figure 6-11. Pareto Front analysis with forced air cooling

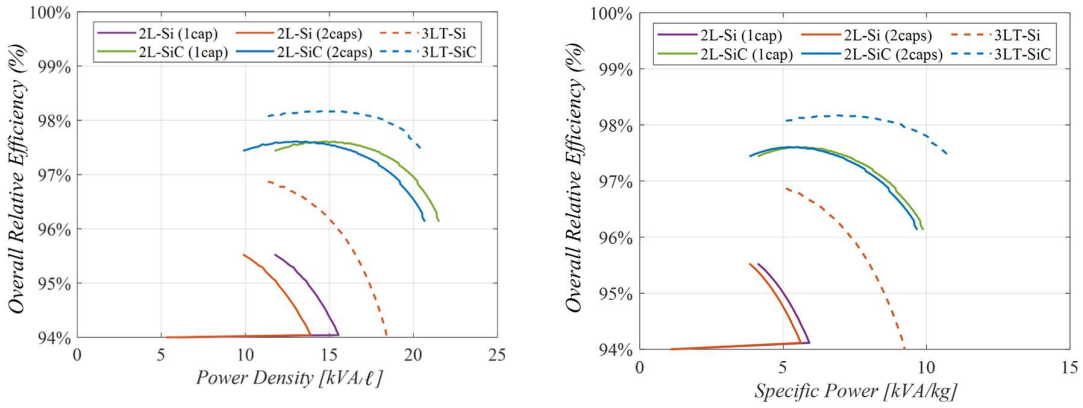
In Figure 6-11(a), the *2L*-SiC (1cap) configuration is set as an example. From point A to C, the power density increases as the switching frequency rises. This is because the volumes of the filter components are the major contributors in this region and the higher switching frequency leads to smaller line inductors and DC-link capacitors. It is noticeable that from point A to B, both the power density and the efficiency are improving. In this part, there are two counter effects regarding the efficiency: the switching loss rises while inductor loss drops. The reduction of inductor loss outweighs the increase of device switching loss in this region, which is mainly a result of the reduced number of turns and associated reduction in copper loss. From point B, the increase in switching loss becomes dominant, and subsequently the efficiency shows a constant downward trend thereafter.

The point C is where the theoretical maximum power density can be achieved. From point C to D, the power density starts to descend, because the heatsink volume starts to be the major contributor. As introduced, the heatsink size increases as a result of the increase of switching loss. In this region, the efficiency and the power density both degenerate as the switching frequency rises. Therefore, an optimal design should be selected between point A to C, which benefits both in the efficiency and the power density.

As can be seen from Figure 6-11(a) regarding the power density, *2L*-SiC (1cap) and *3LT*-SiC both can reach around 21 kVA/ℓ, while the *3LT*-SiC option offers better efficiency. The maximum theoretical power density of the *3LT-SiC* configuration is 21.77 kVA/ℓ at 77 kHz with a relative efficiency of 97.67% (97.47% with VZM balancing scheme).

From the weight point of view, Figure 6-11(b) shows the superior performance of the *3LT*-SiC solution both in weight and efficiency. As the benefit of reduced inductor size, the *3LT*-SiC solution shows a maximum theoretical specific power of 13 kVA/kg.

When the customized cold plate (shown in Figure 4-12) is applied, the Pareto Front is re-assessed with the results shown in Figure 6-12.



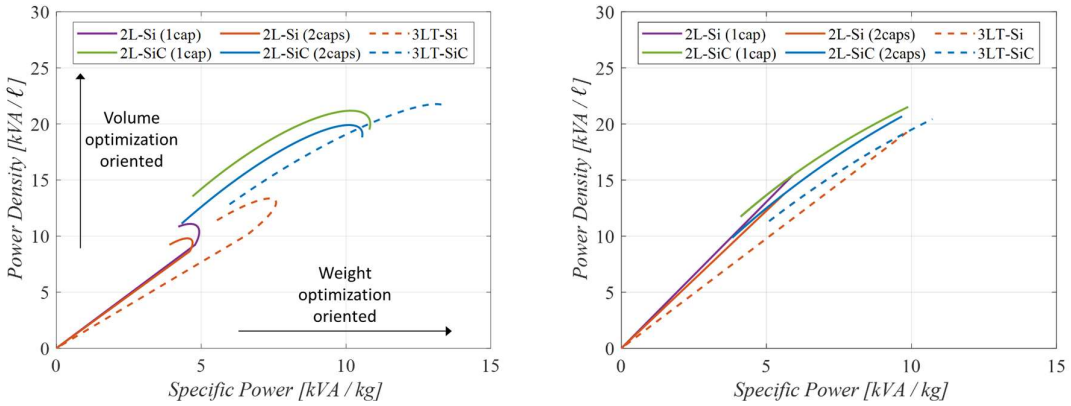
(a) Power density (b) Specific power

Figure 6-12 Pareto Front analysis with a cold plate

For the *3LT*-SiC option, the benefits of reduced loss and smaller heatsink at higher frequencies are no longer effective given the fixed cold plate. From the power density point of view, the *2L*-SiC option shows the best power density achievable of 21 kVA/ℓ. From the specific point of view, the *3LT*-SiC option is still the most attractive option due to the less requirement of the major weight contributor – line inductors.

For aerospace applications, both the volume and the weight require consideration. The trade-offs between the power density and the specific weight can also be visualized by the Pareto Front analysis, as shown in Figure

6-13



(a) Air-cooled heatsink (b) Liquid-cooled heatsink

Figure 6-13. Trade-offs between power density and specific power

As Figure 6-13 shows, the *2L* converter overall shows a better performance towards the smaller volume; the *3LT* options features a better performance towards the lighter weight. The SiC devices offers a significant improvement pushing the boundaries both in the aspects of power density and specific power. It is worth noticing that, if the efficiency is not concerned, the *3LT*-Si options with a cold plate shows very competitive volume/weight performance of 19 kVA/ℓ and 9 kVA/kg.

6.4 Prototyping

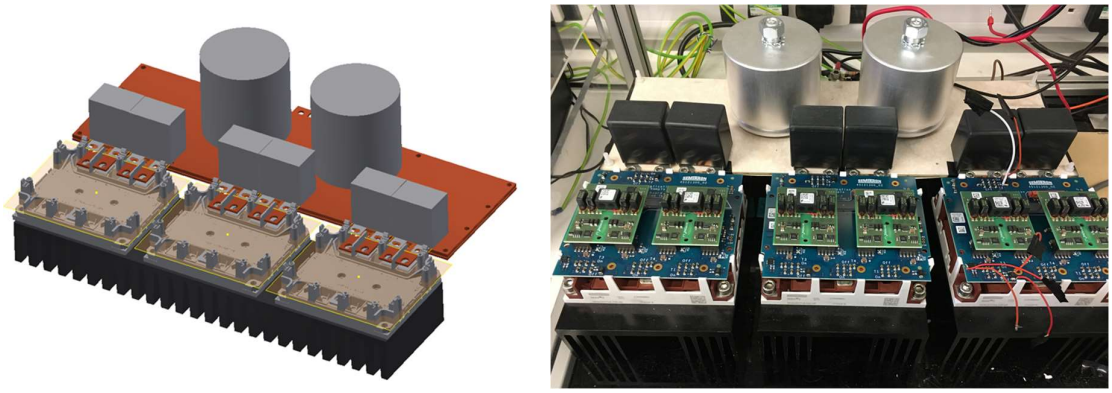
Two prototypes are designed and built for this project:

- Prototype I: *3LT*-Si based converter with power module SKiM301TMLI12E4B and natural-air-cooled heatsinks
- Prototype II: *2L*-SiC based converter with power module CAS300M12BM2 and liquid cold plates

The *3LT*-Si converter is built mainly to validate the models and control strategies for three-level converters. Note this *3LT*-Si converter is not optimized for power density.

The mechanical structure of the power converter is designed through a Computer Aided Design (CAD)

software, ©Autodesk Inventor. Based on the 3D models of individual components, the prototype is virtually structured and assembled, with an illustration shown in Figure 6-14 (a). The realized hardware of this prototype is shown in Figure 6-14 (b). The DC-link of this prototype is formed by DC-link capacitors, snubber capacitors and busbars to exhibit low parasitic inductance.



(a) 3D CAD (b) built hardware

Figure 6-14. Prototype I: *3LT*-Si prototype with power module SKiM301TMLI12E4B and natural-air-cooled heatsink

A single-phase version is designed for conducting the Triple Pulse Test for the core loss evaluation and the Double Pulse Test for the switching energy evaluation.

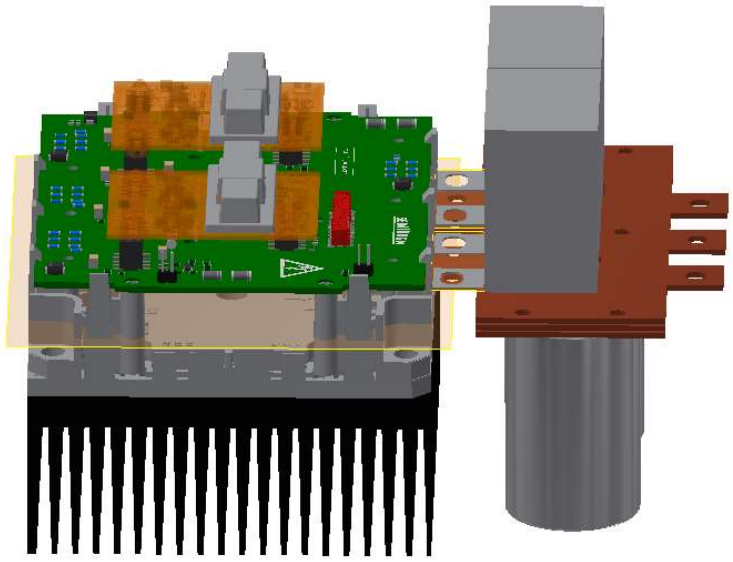
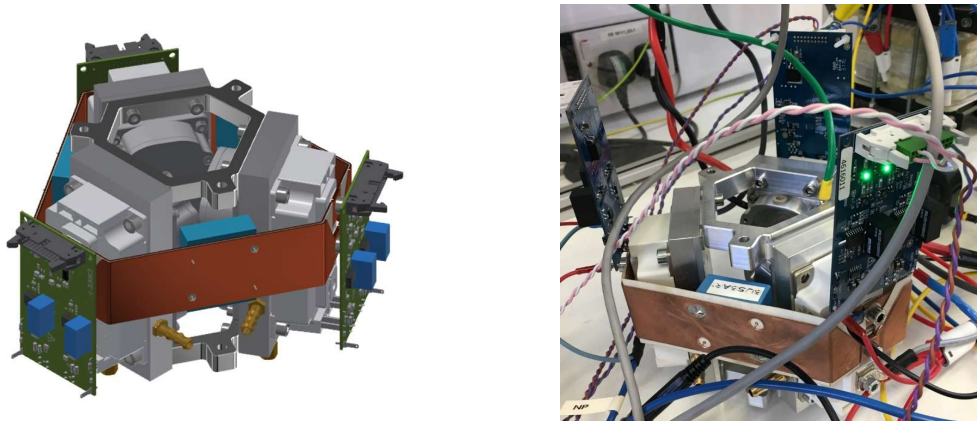


Figure 6-15. Virtual view of designed single-phase three-level converter

The second prototype is based on the *2L*-SiC configuration with liquid cold plates. This prototype is co-designed and developed with Dr. Kfir Pzenica. Figure 6-16 shows the design and built hardware of the prototype,

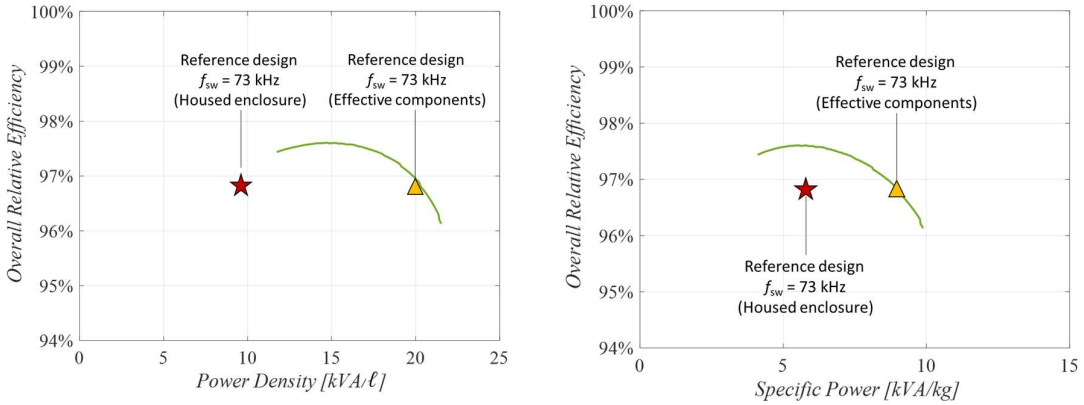
which is based on a hexagonal shape.



(a) 3D CAD (b) built hardware

Figure 6-16. Prototype II:*2L*-SiC prototype with power module CAS300M12BM2 and liquid cold plates

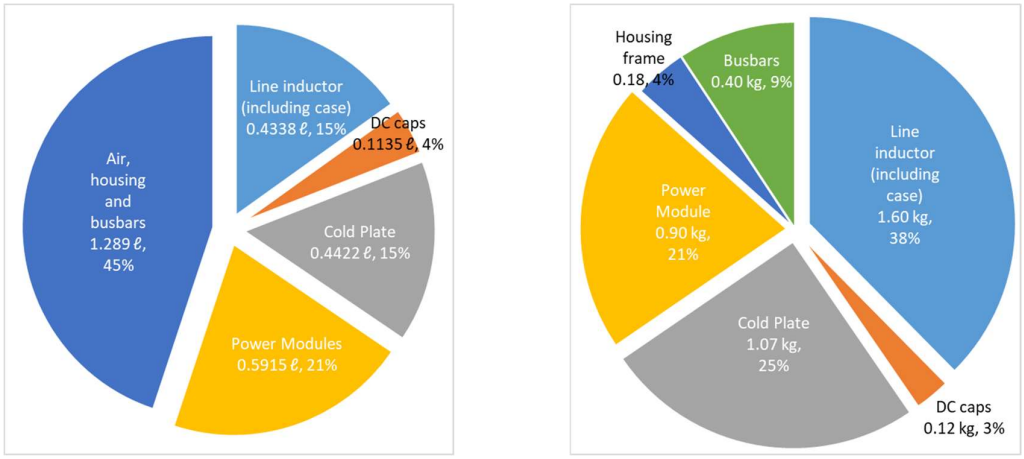
The Prototype II is optimized towards high power density. The switching frequency is selected at f_{sw} = 73 kHz to push the power density for higher following Figure 6-10, while a f_{sw} below 75 kHz avoids the converter output current harmonics at around $2f_{sw}$ to fall in the EMI requirement defined from 150 kHz by DO-160 [64]. The power density of the prototype is expected to reach 20 kVA/ℓ and 9 kVA/kg considering only the effective components. However, the housing and placement of the components must be considered in the realized hardware. The actual prototype considering the housed enclosure can only achieve the target power density by approximately 50 %, as indicated in Figure 6-12. The realized specific power is 6.33 kVA/kg which is 70% of the target value.



(a) Power density (b) Specific power

Figure 6-17. Power density/specific weight performance of Prototype II (estimated efficiency)

The breakdown of volume/weight by components are illustrated in Figure 6-18.



(a) Volume (b) Weight

Figure 6-18. Volume/weight contribution of each component in Prototype II

From the volume point of view, nearly 45% of the prototype is occupied by air, interconnections and the housing frame. The volume of the line inductors is also nearly doubled with the additional case.

In terms of the weight, the line inductors are the major contributor, which includes the aluminum case and epoxy potting material. Apart from the effective components, the busbars and the housing frame only account for 13 % of the weight as addition.

The volume-weight performance is visualized in Figure 6-19, which shows that the Prototype II accomplished the weight goal better than the volume goal.

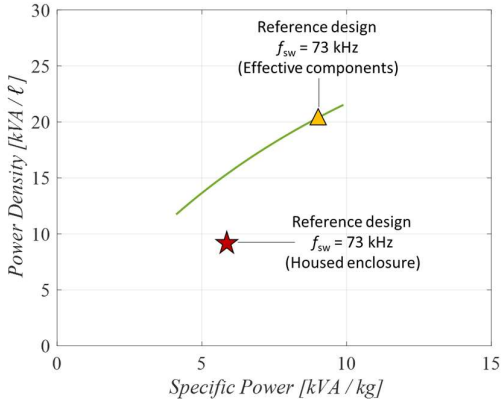


Figure 6-19. Volume/weight performance of Prototype II

Further experimental commissioning of the Prototype II together with the PM generator is to be conducted to evaluate the converter performance at a full scale.

6.5 Summary

The system-level optimisation of the ASR is presented in this chapter with the aid of the mathematical models established in previous chapters. The design space is generated considering three main design variables: topology, power device and switching frequency. Dedicated design procedure and performance prediction are conducted individually for each design out from the design space. The design trade-offs between the contradictory objectives are analysed and visualized in the form of Pareto Fronts. The detailed contributions of individual components towards the power loss and volume/weight are investigated to gain the understanding of the quantified benefits/drawbacks of choosing a set of design variables.

Overall, the optimisation model shows that rising the switching frequency to an extent, e.g. from 10 kHz to 70 kHz, can effectively increase the power density/specific power of the converter by shrinking the filter components. From this perspective, the SiC technology is the main propeller of improving the power density/specific power, because its low switching losses allow the converter to operate at a higher switching frequency without a substantial sacrifice of the efficiency and cooling requirement. As a benchmarking, by replacing Si devices with SiC devices in the *2L* converter, the switching frequency can be pushed from 20 kHz to over 100 kHz, with the maximum power density improved from 10 kVA/ℓ to 21 kVA/ℓ.

The advanced *3LT* topology is the secondary enabling technology for the improving the performance. The main benefits of the *3LT* is the reduced switching loss and less output harmonics. As a benchmarking, by changing from *2L-Si* to *3LT-Si*, the switching frequency can rise from 20 kHz to 50 ~ 60 kHz from the thermal point of view. With the same switching frequency, the power density/specific power can be improved by the *3LT* topology as a result of less filtering required at the AC output end. However, the *3LT* topology introduces four times installed DC-link capacitance and additional complexity of control compared to the *2L* option.

The combination of these two aspects, i.e. the *3LT-SiC*, results in the most promising performance with both improved efficiency and volume/weight as indicated by the optimisation model. Meanwhile, only the upgrade of power devices from *Si* to *SiC* can still lead to competitive improvement of performance. A 20 kVA/ℓ power density and a 10 kVA/kg specific power are expected to be achieved by the *2L-SiC* configuration.

Two prototypes are built to validate the models and to realize the optimal design. If only the effective components are considered, the power density/specific power of the Prototype II aligns well with the theoretical prediction. However, when the housings and interconnections are included, the power density and specific power of the whole prototype can only achieve 50% and 70% of the theoretical values, respectively. Further experimental commissioning of the ASR+PM generator system is required to evaluate the converter performance at a full scale.

CHAPTER 7

Conclusion & Future work

7.1 Summary

The aim of this research is to analyse the system-level design trade-offs and perform optimisation of the ASR system towards high efficiency and high power density/specific power. The passive components and the active power devices are analytically modelled in the built optimisation tool.

CHAPTER 2 establishes the analytical models of the device power losses across various device-topology combinations. Analytical formulas are developed to calculate the conduction losses and switching losses as a function of the operational parameters of the converter, i.e. modulation index, switching frequency and power factor. A case study is conducted to evaluate the power losses among devices for the ASR system over a arrange of switching frequency. With reference to the *2L-Si* option, both the SiC devices and *3LT* topology can effectively reduce the switching loss and allow the converter to operate at a high switching frequency.

CHAPTER 3 addresses the low-frequency Neutral Point voltage oscillation issue in three-level three-phase converters. Neutral Point voltage balancing schemes are introduced to solve this issue without adding additional DC-link capacitance. Special attentions are paid on this issue when the converter operates at low power factor. Two existing voltage balancing schemes are introduced and discussed, the conventional Zero-sequence Signal Injection (ZSI) and the Virtual Zero-level Modulation (VZM). When VZM is applied, the analytical device power loss model is established. The model shows the VZM leads to substantial increase of the switching losses due to the use of additional switching transitions. A novel voltage balancing scheme is proposed to improve the additional switching loss caused by VZM. The proposed scheme is a hybrid of ZSI and VZM. Downscaled experiments are

conducted to verify the effectiveness of the control schemes and the analytical power loss model.

CHAPTER 4 elaborates the design procedures and considerations of the three main passive components: (1) DC-link capacitor (2) line inductor (3) heatsink. For (1), film capacitor is selected as the DC-link capacitor due to the reliability consideration, of which the size is very sensitive to the capacitance. Subsequently, the design of DC-link capacitors aims at a low DC-link capacitance, which is mainly constrained by the high-frequency voltage ripples. Based on the modelling of voltage ripples, the volume/weight of the required DC-link capacitors are analysed based on commercial products. For (2), the line inductance is determined against the allowable amplitude of high-frequency current ripples, which can be modelled analytically. To design the inductor, gapped EE core and *CoFe* alloys are selected aiming at high power density. The case studies show that increasing the switching frequency can effectively reduce the size/weight of both the DC-link capacitors and line inductors. For (3), the required performance of heatsink is obtained through the device power loss modelling and the thermal resistance model. Both air-cooled and liquid-cooled heatsinks are considered in this work. A higher device power loss leads to a larger air-cooled heatsink while the size of the liquid cold plate is relatively fixed.

CHAPTER 5 investigates the modelling of the filter inductor loss, which is especially important for high-frequency operation of the converter. The inductor loss consists of the core loss and the copper loss. While the copper loss can be accurately predicted by analytical models, the core loss estimation is challenging in the case of PWM converters. This work employs empirical B-H loop measurement to characterize the core loss of inductors. A half-bridge based testing is proposed to address the asymmetric testing voltage caused by device voltage drops at a high testing current. A Triple Pulse Test procedure is proposed to capture the steady state B-H loops with simplified requirement of the test setup. By performing the empirical test, a loss map can be established for the purpose of estimating the core loss for PWM operation, which can be considered as the datasheet of the core. A user-friendly loss map is proposed for individual inductors to enable more straightforward calculation process.

Aiming at the modelling of the core loss for a given operating point, an analytical approach is proposed to calculate the core loss in two-level and three-level converters with the aid of the pre-measured loss map. Experimental results show consistency between the proposed model and the measurements.

CHAPTER 6 presents the system-level optimisation of the ASR system and explores the design trade-offs exhibited regarding the performance indices. The optimisation process considers the topology, the power device and the switching frequency as the main design variables. Based on the design space generated from the combinations of these three variables, the possible designs are evaluated to identify the limitations of the performances and trade-offs. The results show that the increase of the switching frequency to an extent, e.g. from 10 kHz to 70 kHz, can effectively increase the power density/specific power of the converter by reducing the required filter components. Both the SiC devices and the *3LT* topology enable the converter operate at a higher switching frequency without sacrificing substantial efficiency and enlarging the heatsink size significantly. Two prototypes are built to validate the models and demonstrate the system performance. The design with *2L-SiC* configuration at f_{sw} = 73 kHz is selected and realized as the Prototype II, which achieves the expected power density of 20 kVA/ℓ and 9 kVA/kg with only the effective components counted.

In summary, this work indicates that both the emerging SiC devices and the advanced three-level T-type topology can fundamentally improve the performance of the power converter. By operating at a higher switching frequency, the filter components can be cut down substantially. The thermal consideration is the main constraint of the use of higher switching frequency, which requires additional cooling measures to counter the high-frequency switching loss and magnetic component loss. The overall optimal design can be selected with the guidance of the optimisation tool considering multiple performance objective. The built prototype demonstrates that the theoretical optimisation and Virtual Prototyping can lead to a practical realization with the performance well predicted.

7.2 Main contributions

The main contributions to the knowledge of this work can be summarized as follows:

- Neutral Point Balancing scheme for three-level three-phase converter
    - Identified and improved a novel modulation scheme, Virtual Zero-level Modulation (VZM), to balance the DC-link capacitor voltages on switching-window basis over the full operation range of modulation index/power factor
    - Proposed an analytical model to analyse the device power losses impacted by Virtual Zero-level Modulation, which is verified by experiments.
    - Proposed a hybrid NP balancing algorithm integrating VZM and conventional ZSI to improve the efficiency performance. The effectiveness of the proposed hybrid balancing scheme is confirmed by experiments.
- Inductor core loss modelling
    - Proposed a test circuit with the ability to compensate asymmetric amplitude of square-wave inductor voltage caused by power device voltage drops. The voltage drops are particularly significant when the excitation current is high (e.g. >100 A).
    - Proposed a discontinuous test procedure aiming at minimized testing process, the Triple Pulse Test. This procedure avoids unnecessary operation and reduces the requirement/stress of the hardware in the testing, e.g. capacity of the DC power supply, current-time ($I \cdot t$ in $A \cdot \mu s$) stress on current probes and thermal stress on the inductor and power converter.
    - Characterized the power loss of an *CoFe* alloy based inductor that is customized targeting high

power density

- Proposed a user-friendly loss map for straightforward calculation of the inductor core loss.
- Proposed an analytical approach to estimate the inductor core loss for given PWM operation of the power converter. The analytical model is developed on both two-level and three-level converters.

- System-level optimisation and trade-off analysis of a 27 kVA Active Shunt Regulator system
  - A mathematical optimisation tool is built to show the design trade-offs and identify the optimal design considering three main design variables: topology, power device and switching frequency
  - A Si IGBT based prototype is designed and built to perform experimental tests and validate the power loss models and voltage balancing schemes
  - A SiC MOSFET based prototype is co-designed and tested with Dr. Kfir Pzenica to realize the identified high-power-density design

7.3 Future work

This work focuses on the system-level modelling and optimisation of the target power electronics system. The results show that the increase of switching frequency constantly reduces the size of the filter components in theory up to 100 kHz. However, for even higher switching frequency, there are other issues must be considered, such as the increased high-frequency loss of inductors and associated thermal considerations and EMI emissions/filters.

7.3.1 Thermal constraint of inductors

It has been reported that the thermal constraint must be taken into considerations of the design of inductors. The inductor cannot be shrunk unlimitedly by increasing the switching frequency, because the inductor high-frequency loss rises while the heat dissipation ability drops as the inductor becomes smaller [71], [110]. Previous studies mainly considers the inductors' heat dissipation through passive radiation and convection, for which the surface area of the inductor is constrained by the thermal requirement [27], [110]. However, as this work shows, the power loss of the inductor can be more substantial, which requires active cooling efforts (e.g. a heatsink) to dissipate the heat generated in the inductor. With the heatsink considered, the conduction thermal model varies significantly between different inductor designs due to various winding placement, potting material, housing and heatsink arrangements. As an example, [164] presents the thermal performance analysis of a compact planar inductor through lumped-circuit thermal model considering a cold plate. If a considerable number of inductor designs need to be considered, such as this work, accurate thermal models must be built individually for each design, which requires intensive efforts of analysis and experimental evaluation. Furthermore, if the dimensions of the inductor cores are considered completely customizable, considerable optimisation efforts can be conducted to find the best physical shape/assembly of an inductor, e.g. enlarging the bottom surface area for better conducted heat dissipation through a cold plate.

7.3.2 Power loss profiles of inductors

For accurate core loss estimation, intensive efforts have been made in this work to test the core loss and establish the loss map of one particular inductor that has been physically built. For the optimisation analysis, the inductors in this work are individually designed for each combination of topology and switching frequency. However, for more accurate modelling, it is desired to test each design of inductor individually. For example, the gap loss reported in [138] strongly depends on the air gap length and the geometry of the core, which can only be

assessed empirically on a built inductor.

Therefore, further work can be conducted through experimental tests of a range of inductors that are built for various topology-switching frequency. Considering both thermal performance and power loss, ideally, a datasheet should be established for each design of inductor with a core loss map and thermal parameters presented, which is similar to the datasheet of commercial power modules. Furthermore, if a rich database of inductors can be built considering various core materials, windings and geometries, finding an optimal inductor for a certain application can be achieved by conducting a mathematical optimisation process.

7.3.3 EMI filter modelling

As discussed in Section 1.2, the EMI issues in the PM generator/ASR system is not addressed in this work. As possible options, the EMI filters can be placed inside the ASR converter, or at the generator output terminal (after the regulation point). The existing literatures mainly focuses on the EMI filter design of inverter systems [52] or grid-rectifier systems [65]. For this purpose, comprehensive EMI models must be established for the shunt-regulated power generation system to design and model the EMI filters. Theoretically, the EMI filter is another factor that limits the ceiling of increasing the switching frequency. Trade-offs between the size of EMI filters and switching frequency are to be established in the ASR system.

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Appendix A

Analytical averaged loss model expressions

A.1 Two-level converter

A.1.1 *2L*-Si

Conduction loss with Si IGBT + Si Diode

T1/T4
$$P_{cond.T1/T4} = \left(\frac{1}{8} + \frac{M\cos(\varphi)}{3\pi}\right) I_M^2 R_{on.T1/T4} + \left(\frac{1}{2\pi} + \frac{M\cos(\varphi)}{8}\right) I_M U_{FW0.T1/T4} \quad \text{(A-1)}$$

D1/D4
$$P_{cond.D1/D4} = \left(\frac{1}{8} - \frac{M\cos(\varphi)}{3\pi}\right) I_M^2 R_{on.D1/D4} + \left(\frac{1}{2\pi} - \frac{M\cos(\varphi)}{8}\right) I_M U_{FW0.D1/D4} \quad \text{(A-2)}$$

Switching loss with Si IGBT + Si Diode

T1/T4
$$P_{sw.T1/T4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right) \times \left(\frac{\pi C_{T1/T4}}{2} I_M^2 + 2B_{T1/T4} I_M \cdot + \pi A_{T1/T4}\right) \quad \text{(A-3)}$$

D1/D4
$$P_{sw.D1/D4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right) \times \left(\frac{\pi C_{T1/T4}}{2} I_M^2 + 2B_{D1/D4} I_M \cdot + \pi A_{D1/D4}\right) \quad \text{(A-4)}$$

A.1.2 *2L*-SiC

Conduction loss with SiC IGBT + SiC Schottky Diode

T1/T4
$$P_{cond.T1/T4} = \frac{I_M^2 R_{on.T1/T4}}{4} \quad \text{(A-5)}$$

D1/D4
$$P_{cond.D1/D4} = 0 \quad \text{(A-6)}$$

Switching loss with SiC MOSFET + SiC Schottky Diode

T1/T4
$$P_{sw.T1/T4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right) \times \left(\frac{\pi C_{T1/T4}}{2} I_M^2 + 2B_{T1/T4} I_M \cdot + \pi A_{T1/T4}\right) \quad \text{(A-7)}$$

D1/D4
$$P_{sw.D1/D4} = 0 \quad \text{(A-8)}$$

A.2 Three-level T-type converter

A.2.1 *3LT*-Si

Conduction loss with Si IGBT + Si Diode

T1/T4

$$P_{cond.T1/T4} = M\left(\frac{1}{6\pi}+\frac{\cos(\varphi)}{3\pi}+\frac{\cos(\varphi)^2}{6\pi}\right)I_M^2 R_{on.T1/T4} + M\left(\frac{\cos(\varphi)}{4}+\frac{\sin(\varphi)}{4\pi}-\frac{\varphi\sin(\varphi)}{4\pi}\right)I_M U_{FW0.T1/T4} \quad \text{(A-9)}$$

D1/D4

$$P_{cond.D1/D4} = M\left(\frac{1}{6\pi}-\frac{\cos(\varphi)}{3\pi}+\frac{\cos(\varphi)^2}{6\pi}\right)I_M^2 R_{on.D1/D4} + M\left(\frac{\sin(\varphi)}{4\pi}-\frac{\varphi\sin(\varphi)}{4\pi}\right)I_M U_{FW0.D1/D4} \quad \text{(A-10)}$$

T2/T3

$$P_{cond.T2/T3} = \left(\frac{1}{4}-M\frac{1}{3\pi}-M\frac{\cos(\varphi)^2}{3\pi}\right)I_M^2 R_{on.T2/T3} + \left(\frac{1}{\pi}-M\frac{\cos(\varphi)}{4}-M\frac{\sin(\varphi)}{2\pi}+M\frac{\varphi\sin(\varphi)}{2\pi}\right)I_M U_{FW0.T2/T3} \quad \text{(A-11)}$$

D2/D3

$$P_{cond.D2/D3} = \left(\frac{1}{4}-M\frac{1}{3\pi}-M\frac{\cos(\varphi)^2}{3\pi}\right)I_M^2 R_{on.D2/D3} + \left(\frac{1}{\pi}-M\frac{\cos(\varphi)}{4}-M\frac{\sin(\varphi)}{2\pi}+M\frac{\varphi\sin(\varphi)}{2\pi}\right)I_M U_{FW0.D2/D3} \quad \text{(A-12)}$$

Switching loss with Si IGBT + Si Diode

T1/T4

$$P_{sw.T1/T4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right)\times \left[\left(\frac{\pi}{2}-\frac{\varphi}{2}+\frac{\cos(\varphi)\sin(\varphi)}{2}\right)C_{T1/T4}\cdot I_M^2+(1+\cos(\varphi))B_{T1/T4}\cdot I_M+(\pi-\varphi)A_{T1/T4}\right] \quad \text{(A-13)}$$

D1/D4

$$P_{sw.D1/D4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right)\times \left[\left(\frac{\varphi}{2}-\frac{\cos(\varphi)\sin(\varphi)}{2}\right)C_{D1/D4}\cdot I_M^2+(1-\cos(\varphi))B_{D1/D4}\cdot I_M\pm\varphi A_{D1/D4}\right] \quad \text{(A-14)}$$

T2/T3

$$P_{sw.T2/T3} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right)\times \left[\frac{\varphi}{2}-\frac{\cos(\varphi)\sin(\varphi)}{2}\right)C_{T2/T3}\cdot I_M^2+(1-\cos(\varphi))B_{T2/T3}\cdot I_M\pm\varphi A_{T2/T3}\Big] \quad \text{(A-15)}$$

D2/D3

$$P_{sw.D2/D3} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right)\times \left[\left(\frac{\pi}{2}-\frac{\varphi}{2}+\frac{\cos(\varphi)\sin(\varphi)}{2}\right)C_{D2/D3}\cdot I_M^2+(1+\cos(\varphi))B_{D2/D3}\cdot I_M+(\pi-\varphi)A_{D2/D3}\right] \quad \text{(A-16)}$$

A.2.2 *3LT*-SiC

Conduction loss with SiC MOSFET + SiC Diode

T1/T4
$$P_{cond.T1/T4} = M \cdot \frac{\cos(\varphi)^2 + 1}{3\pi} I_M^2 R_{on.T1/T4} \tag{A-17}$$

D1/D4
$$P_{cond.D1/D4} = 0 \tag{A-18}$$

T2/T3
$$P_{cond.T2/T3} = \left(\frac{1}{2} - M \cdot \frac{2(\cos(\varphi)^2 + 1)}{3\pi}\right) I_M^2 R_{on.T2/T3} \tag{A-19}$$

D2/D3
$$P_{cond.D2/D3} = 0 \tag{A-20}$$

Switching loss with SiC MOSFET + SiC Diode

T1/T4
$$P_{sw.T1/T4} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right) \times \left[\left(\frac{\pi}{2} - \frac{\varphi}{2} + \frac{\cos(\varphi)\sin(\varphi)}{2}\right) C_{T1/T4} \cdot I_M^2 + (1 + \cos(\varphi)) B_{T1/T4} \cdot I_M + (\pi - \varphi) A_{T1/T4}\right] \tag{A-21}$$

D1/D4
$$P_{sw.D1/D4} = 0 \tag{A-22}$$

T2/T3
$$P_{sw.T2/T3} = \left(\frac{f_{sw}}{2\pi}\frac{U_{sw}}{U_{base}}\right) \times \left[\left(\frac{\varphi}{2} - \frac{\cos(\varphi)\sin(\varphi)}{2}\right) C_{T2/T3} \cdot I_M^2 + (1 - \cos(\varphi)) B_{T2/T3} \cdot I_M \pm \varphi A_{T2/T3}\right] \tag{A-23}$$

D2/D3
$$P_{sw.D2/D3} = 0 \tag{A-24}$$