Performance of Wide-Bandgap Gallium Nitride vs Silicon Carbide Cascode Transistors

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***Abstract*—Wide-bandgap (WBG) cascodes combine the advantages of gate drivability and reliability of silicon MOSFETs with the conversion efficiency of WBG devices. In cascodes, a low voltage silicon MOSFET drives a vertical SiC JFET or a lateral GaN HEMT. This paper will present the first systematic comparison of the WBG cascodes considering static & dynamic performance, 3rd quadrant operation and avalanche ruggedness, as well as the temperature sensitivities. The results show that the GaN cascode outperforms the SiC cascode in switching performance, however, demonstrates is more temperature sensitive at on-state. A model is developed to predict the dI_{DS}/dt and its derivative against R_G. Whilst turn-ON dI_{DS}/dt and dV_{DS}/dt have positive temperature coefficients in the SiC cascode and negative coefficients in the GaN cascode, the SiC cascode is more avalanche rugged, whereas the GaN cascode is incapable of unclamped inductive switching.**

***Index Terms*—Silicon Carbide, Gallium Nitride, Power Semiconductor Devices, Cascode**

I. Introduction

Gallium Nitride (GaN) semiconductor devices have emerged in power conversion systems, for example, for application in electric vehicle charging systems, inverters for solar plants and point of load converters. The key type of the GaN power devices for high voltage (>600V) is the high electron mobility transistors (HEMTs). Due to fact that these devices posses high saturation electron velocity and a high breakdown field in the heterojunction between AlGaN and GaN layer that is provided by the two-dimensional electron gas layer (2DEG) [1], these devices have low on-state resistance. The electrons are generated by the spontaneous polarization occurred at the interface of the heterojunction. The GaN layer has lower level of conduction band than fermi level at heterojunction which provides the electrons that complete the band-discontinuity confined within the quantum wells. These devices are more efficient compared to silicon based power MOSFETs in terms of the on-state resistance and the reverse recovery charge [2]. On the other hand, the blocking voltage rating, the current handling capability and its thermal impedance are limited due to the lateral architecture of GaN HEMTs. The vertical device structure is not available due to the absence of the bulk GaN substrate, thus, the lateral structures are grown on the silicon substrates with a few strain-relaxed buffer layers. These layers relieve the stress of the crystal mismatch between GaN layer and Si substrate. SiC MOSFETs have also improved significantly considering the switching rates and the on-state resistance, although it has a critical reliability issue due to the charge trapping between the SiO_2 gate oxide layers and SiC layer [3]. This is because of the presence of the carbon atom which cause the increase of the trap density during the oxidation process. Additionally, the critical electric field in the gate oxide of the SiC MOSFETs is considerably higher compared to silicon MOS-gated devices [4].

The simple cross-section view of a vertical SiC JFET and a lateral GaN HEMT are demonstrated in Fig. 1. Due to the high mobility, doping and drift velocity of electrons, the depletion mode devices are created as N channel devices. As for the SiC JFET structure, N drift region is used for

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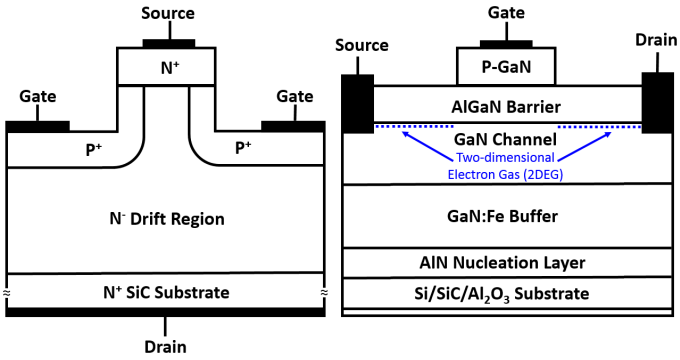

Fig. 1. Cross-section of SiC JFET & GaN e-HEMT with partial 2DEG.

voltage blocking. When the negative voltage is applied to the gates, the depletion region is created in the junction between N drift region and P body region. After sufficient voltage is applied, the depletion areas are merged on both sides of the channel under source terminal which cuts off the conduction between source and drain. With respect to a lateral structure of GaN HEMT, these devices include heterojunction between two different materials which have various bandgaps, such as GaN and AlGaN layers. The electrons from GaN side move to heterojunction and the 2DEG layer is formed. This layer provides highly efficient conduction between source and drain. These devices are generally fabricated on the silicon or SiC substrates. To relieve the mismatch between GaN and substrate, AlN or GaN:Fe layers are used which are essential at higher temperatures due to the critical differences in the coefficient of thermal expansion between the substrate and GaN layer.

A low voltage Si MOSFET is used as a driving MOSFET in cascode structure for the normally-on SiC JFET and GaN HEMT. This allows using the devices as normally-off devices even when they provide low on-state resistance and high switching speed, and include small parasitic components.

In this paper, the static, dynamic and avalanche performances of the GaN and SiC cascode devices are analyzed. These analysis provide inclusive measurement results to allow clear understanding of the cascode devices. The SiC cascode is UnitedSiC's UJ3C065080K3S device with ratings of 650 V & 23 A at 100°C while the GaN cascode is Transphorm's TP65H050WS with similar ratings of 650 V & 25 A at 100°C.

II. STATIC PERFORMANCE

The forward conduction and the reverse conduction measurements provide testing of the state-on resistance ($R_{DS\text{-}ON}$) which creates the static on-state conduction losses. These losses are essential parameters to analyse two cascode configurations. The circuit diagram is shown in Fig. 2.

A. Forward Conduction

A current pulse passes through the device with rated gate voltage and the ON-state voltage is measured across the device which provides ON-state performance of the device. The resistive heating of the device due to the current pulse causes

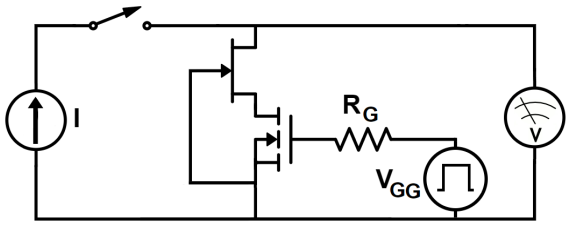

Fig. 2. Static tests circuit.

an increase in junction temperature based on the junction to case thermal impedance. Unless it is negative, the ON-state voltage increases with the duration of the pulse. Due to the similarity of the high temperature current ratings for SiC and GaN, according to chip areas of the devices, the specific ON-state resistance can be calculated. The device were measured as 5mm^2 and 7mm^2 for SiC JFET and GaN HEMT, respectively, by the de-capsulation of the chips. The measurement results for the SiC and GaN devices are clearly shown in Fig. 3 with 5 A and 10 A current pulse for 5 seconds. The specific ON-state resistance is one order of magnitude higher for GaN cascode than the SiC cascode device, while the temperature coefficient is four orders of magnitude higher for the GaN than the SiC cascode device.

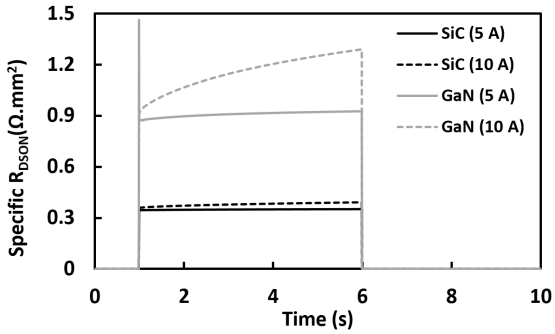

Fig. 3. Self-heating in specific ON-state resistance of SiC & GaN cascodes with 5 A and 10 A.

The lower thermal conductivity, the lateral structure of the device with low voltage Si-MOSFET and the package for GaN device all have an impact on the higher temperature coefficient. While the magnitude of the current pulse is increased to 15 A as illustrated in Fig. 4, the influence of the higher thermal impedance is obvious. The current source is forced to saturate by the dissipated power of the GaN device.

B. Reverse Conduction

The reverse conduction has been investigated by a current pulse similar to the forward conduction, whereas the direction of the current is changed and it passes through the body diode of the device. The results of the experimental measurements with 5 A and 10 A for 5 seconds are demonstrated in Fig. 5. It is clearly seen that the body diode forward voltage is higher for GaN cascode device than the SiC cascode device. Due to the material characteristics of the compounds, a variety of

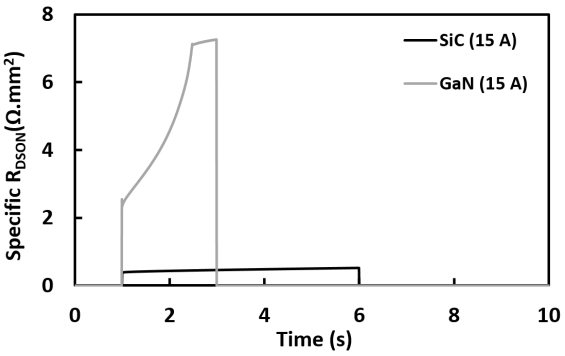

Fig. 4. Specific ON-state resistance of the SiC and GaN cascode devices conducting 15 A.

the voltage rises for the body diode forward voltages with temperature can be seen.

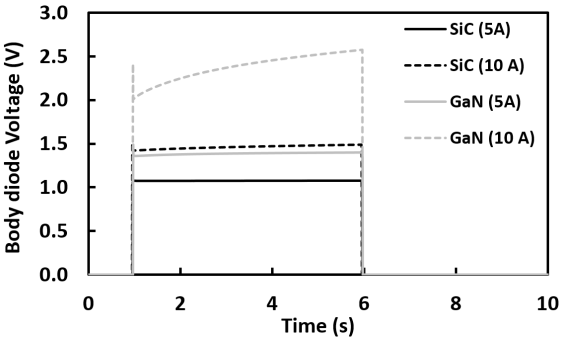

Fig. 5. Self-heating in body diode forward voltages of SiC & GaN cascodes with 5 A and 10 A.

III. Dynamic Performance

The dynamic transient's performance has been investigated by the double pulse tester (DPT) with its circuit diagram shown in Fig. 6. The test rig used in the experimental measurement to evaluate the transients of the devices is also shown in Fig. 7. As it seen in Fig. 6, a SiC Schottky barrier diode is used as a free-wheeling diode at the high side, while the device under test is placed at the low-side. On the test rig, due to the upper limit of the standalone GaN HEMTs, the gate voltage is adjusted to 15 V to drive the cascode device effectively. The drain voltage is fixed at 650 V to avoid failure that can be caused by overshoots up to 900 V, whereas the load current is fixed at 5 A through the pulse length of the gate driver. The devices at low side are heated and the temperature is increased by steps of 25°C from 25°C to 175°C.

A. Transient's Modelling

The evaluation of the performance for cascode devices can be investigated by the practical models that depend on the internal circuit's operation. A simple accurate model is generated to assume the differences in switching performance compared to the experimental measurements for cascode devices. A low voltage power MOSFET is used as a driver transistor

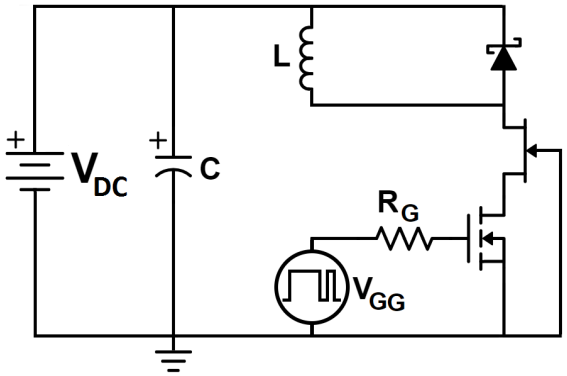

Fig. 6. Dynamic tests circuit.

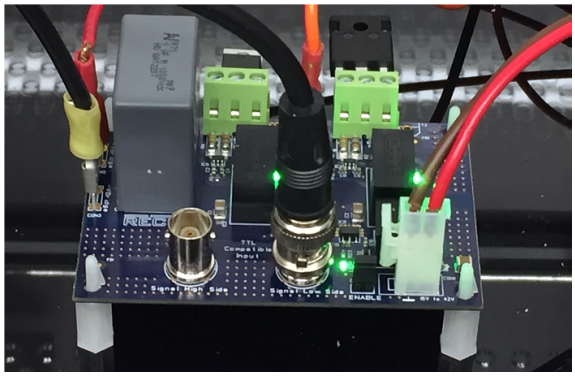

Fig. 7. Test board PCB.

in cascode structure. Its drain-source current in the channel region is defined in equation 1 when pinch-off happens [5].

$$I_{DS} = \frac{W\mu C_{OX}}{2L}\left(V_{GS} - V_{TH}\right)^2 \tag{1}$$

in which W is the channel's width, L is the channel's length, μ is the majority carriers' mobility and C_{OX} is the gate oxide layer's capacitance density. V_{GS} is the only time-dependent parameter in the equation 1. As a result, the equation 2(a) and (b) can be obtained by derivative of equation 1 against time.

$$\left.\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right|_{ON} = \frac{W\mu C_{OX}}{L}\left(V_{GS} - V_{TH}\right)\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{ON} \tag{2a}$$

$$\left.\frac{\mathrm{d}I_{DS}}{\mathrm{d}t}\right|_{OFF} = \frac{W\mu C_{OX}}{L}\left(V_{GS} - V_{TH}\right)\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{OFF} \tag{2b}$$

The dV_{GS}/dt at turn-on & turn-off transients of cascodes can be determined by solving the circuit shown in [6]. During turn-on, the gate current flows through the gate inductance and the source inductance, inducing a voltage on the gate-source capacitor. During turn-off, the charged capacitor will discharge through the gate terminal. The rate of this charging and discharging can be calculated as:

B. Turn-ON Transients

The alterations of the drain currents and drain voltages per second versus gate resistances (R_G) for all different devices,

$$\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{ON} = \frac{2V_{GG}\cdot sin\left(\frac{t\sqrt{-C_{issHV}\cdot R_G^2+4(L_G+L_S)}}{2(L_G+L_S).\sqrt{C}}\right)\cdot exp(\frac{-R_G\cdot t}{2(L_G+L_S)})}{\sqrt{C_{issHV}\cdot(4(L_G+L_S)-C_{issHV}\cdot R_G^2)}} \tag{3a}$$

$$\left.\frac{\mathrm{d}V_{GS}}{\mathrm{d}t}\right|_{OFF} = \frac{V_{GG}}{C_{issHV}}\cdot exp(\frac{-R_G\cdot t}{2(L_G+L_S)})\times \left(cosh\left(\frac{t\sqrt{\frac{C_{issHV}\cdot R_G^2}{4}-(L_G+L_S)}}{(L_G+L_S)\cdot\sqrt{C_{issHV}}}\right)-\frac{\sqrt{C_{issHV}}\cdot R_G\cdot sinh\left(\frac{t\sqrt{\frac{C_{issHV}\cdot R_G^2}{4}-(L_G+L_S)}}{(L_G+L_S)\cdot\sqrt{C_{issHV}}}\right)}{2\sqrt{\frac{C_{issHV}\cdot R_G^2}{4}-(L_G+L_S)}}\right) \tag{3b}$$

such as SiC and GaN cascode devices, SiC MOSFET, super-junction and Si MOSFET have been illustrated in Fig. 8 at room temperature at turn-ON transient. As it is seen that the magnitude of dI_{DS}/dt for GaN Cascode is very high when compared to other devices at low R_G. On the other hand, the magnitude of dI_{DS}/dt is significantly decreases, when the gate resistance is increased from 10Ω to 220Ω, whereas the trends of other devices decreases gradually during the increasing of the gate resistance. Therefore, the GaN cascode device has better performance compared with the other devices due to the smaller input capacitance in the lateral structure of GaN cascode. The HEMT has a critical impact on fast switching of the device which results in great change of dV_{DS}/dt with R_G. This illustrates that the low gate resistance causes slower switching at turn-ON transient.

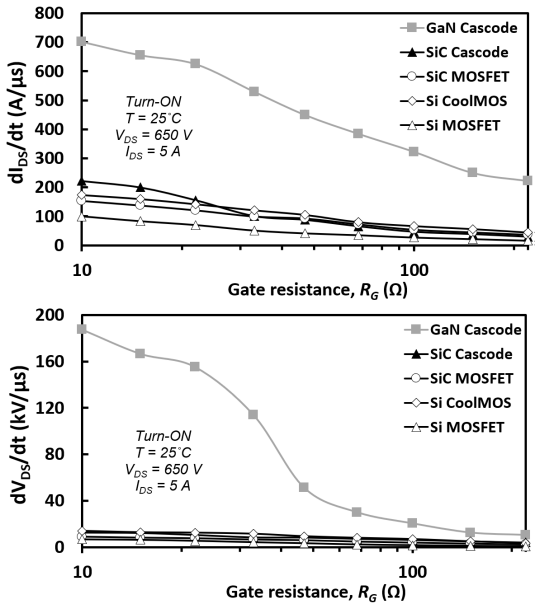

Fig. 8. Turn-on dI_{DS}/dt & dV_{DS}/dt of GaN, SiC & Si at 25°C.

The temperature sensitivity of dI_{DS}/dt and dV_{DS}/dt for both GaN and SiC cascode devices at turn-ON transient with different gate resistances, such as 22Ω and 220Ω, is normalized and demonstrated in Fig. 9. As it is shown in the plots, the switching rates of GaN reduces when the temperature is increased from 25°C to 175°C, whereas they increased slightly for the SiC cascode device. As regarding the GaN, it is mainly related to mobility degradation which is caused by increased phonon scattering with temperature in two dimensional gas layer of the GaN. It is more significant for GaN than SiC, due to the more decreasing of the doping concentration in GaN than SiC.

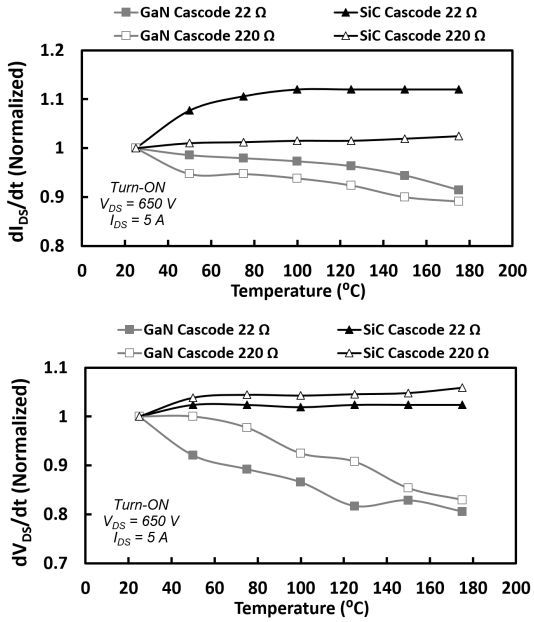

Fig. 9. Normalized turn-on dI_{DS}/dt & dV_{DS}/dt with temperature.

C. Turn-OFF Transients

The changes of the drain currents and voltages per second versus gate resistance for all devices at turn-OFF transient are shown in Fig. 10. There is a decreasing trend in dI_{DS}/dt for GaN, when the gate resistance is increased from 10Ω to 220Ω. The decrease of the dI_{DS}/dt for SiC cascode device is slighter than the GaN cascode device.

As regards the normalized dI_{DS}/dt and dV_{DS}/dt versus temperature with two gate resistances for GaN and SiC cascode devices, they are illustrated in Fig. 11. It is clearly seen that when the temperature is increased from 25°C to 175°C, the magnitude of dI_{DS}/dt for GaN cascode reduces with 30%,

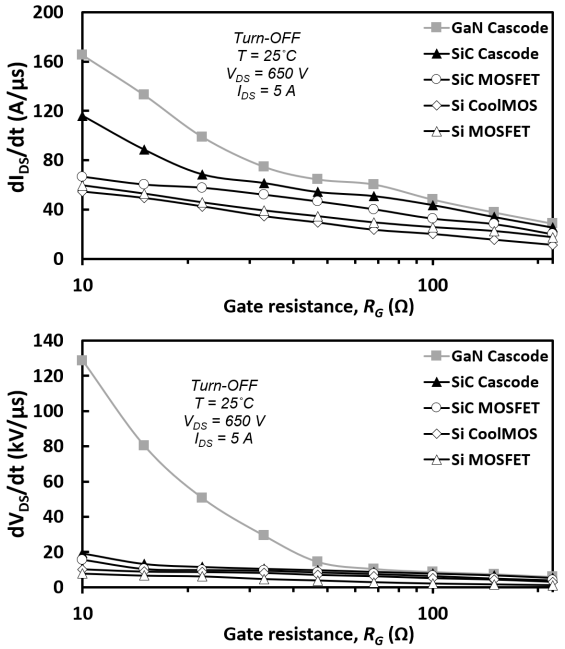

Fig. 10. Turn-Off dI_{DS}/dt & dV_{DS}/dt of GaN, SiC & Si at 25°C.

whereas it is only 15% for SiC cascode device. The negative trends for GaN device is more remarkable than SiC because of decreased carrier mobility and the threshold voltage with increasing temperature that prolongs the turn-OFF period.

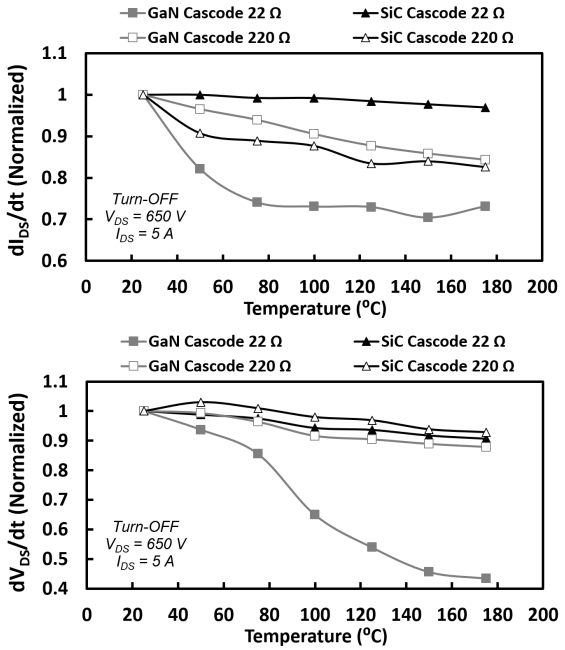

Fig. 11. Normalized turn-off dI_{DS}/dt & dV_{DS}/dt with temperature.

D. Model Outputs

The magnitudes of dI_{DS}/dt and $dI^2{}_{DS}/dtdR_G$ of both devices, GaN and SiC cascode from model outputs and the comparison with experimental measurements at turn-ON are demonstrated in Fig. 12, whereas at turn-OFF they are shown in Fig. 13.

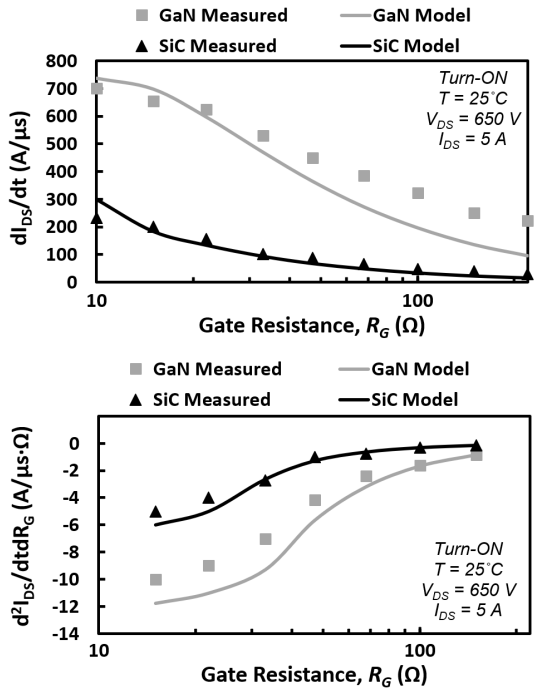

Fig. 12. Turn-on model outputs for dI_{DS}/dt and $dI^2{}_{DS}/dtdR_G$.

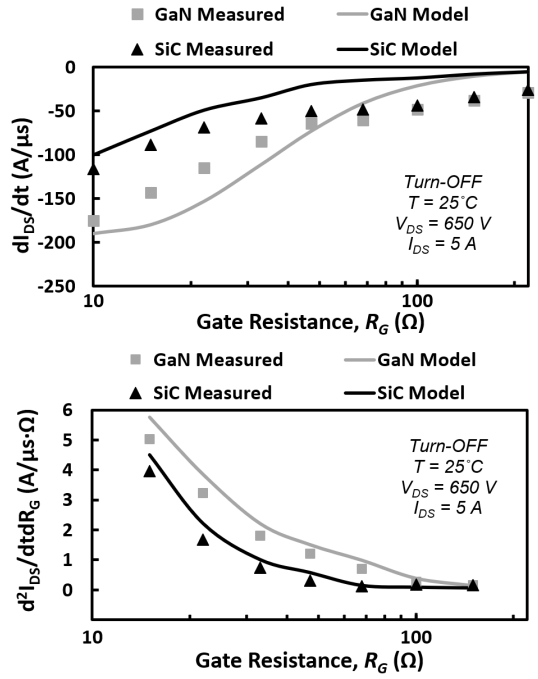

Fig. 13. Turn-off model outputs for dI_{DS}/dt and $dI^2{}_{DS}/dtdR_G$.

As it seen in both plots, the models for both devices predict the similar trends to experimental results. It is also shown that developed models match well for switching rate in both devices when the gate resistance is increased.

E. Reverse Conduction

The dynamic performance of the body diodes in reverse conduction is investigated and the reverse recovery current for four devices in third quadrant is illustrated in Fig. 14. As is seen in the figure, GaN and SiC cascode devices have very low reverse recovery compare to other SiC and super-junction MOSFET. Therefore, this can be attributed to low voltage MOSFET that is used as a driving MOSFET in cascode configuration that has such low recovery charge. The contribution of HEMT and JFET parts of the cascode devices on reverse recovery current can be ignored. This makes them an ideal choice when the reverse recovery is needed.

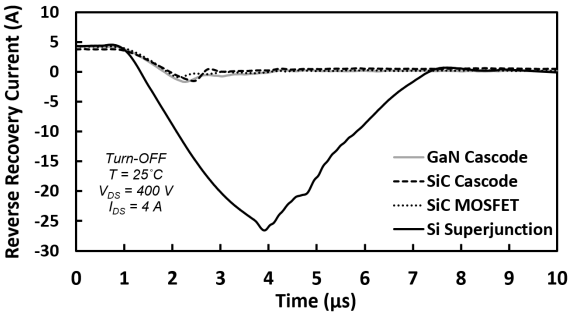

Fig. 14. Reverse recovery current of cascodes & standalone MOSFETs.

The reverse recovery charge is also plotted in Fig. 15 together with its zoomed version by taking integration of current over time and plotted as a function of temperature. It can be seen that the charge in cascode devices is temperature-invariant, thanks to the minimal amount of charge available in the body diode of the silicon MOSFET.

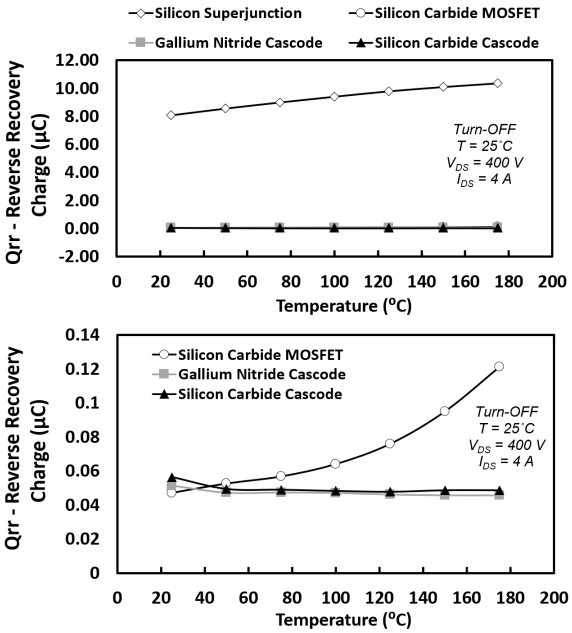

Fig. 15. The reverse recovery charge stored in the devices as a function of temperature.

Fig. 16 shows the share of the turn-on and turn-off switching energy for the GaN and SiC cascodes. It can be seen that overall GaN cascode exhibits significantly lower switching energy while the losses in both devices slightly increases as the temperature rises from room temperature to 175°C.

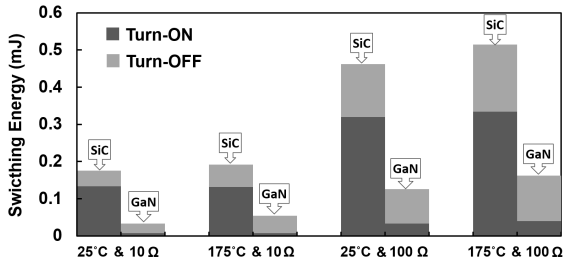

Fig. 16. The switching energy of GaN & SiC cascodes at turn-on and turn-off switching transients.

IV. AVALANCHE RUGGEDNESS

To evaluate the electro-thermal ruggedness of the devices, unclamped inductive switching (UIS) test circuit is used that is almost similar to double pulse test circuit which is illustrated in Fig. 6, however this circuit is not included the free-wheeling diode at high side of DPT circuit. Therefore, when the device is turn-ON, drain current charges the inductor at a linear rate. The drain current and the voltages is examined until device is failed. The inductor dissipates all stored energy when the device is turn-OFF and this causes the reaching of the breakdown rate for device. The pulse length of the gate driver is increased until avalanche is occurred in the GaN and SiC cascode devices.

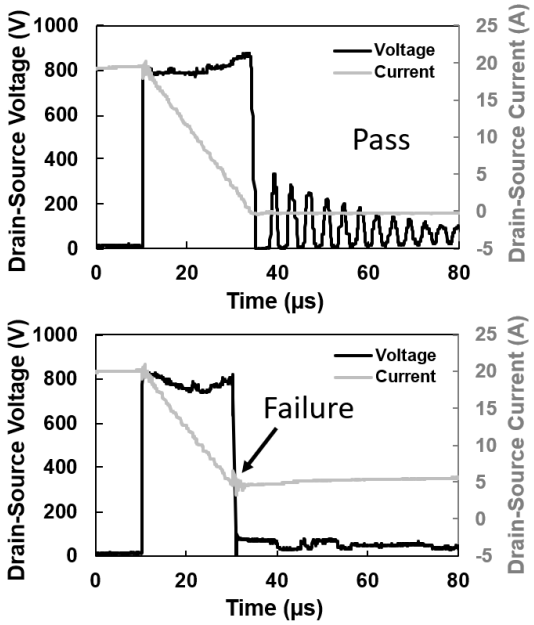

Fig. 17. The SiC cascode device fails the UIS test after current increase beyond 20 A.

The failure of the SiC FETs through impact ionization due to the latching of parasitic BJT or the limited temperature sensitivity in the junctions. However, the absence of the heat extraction capability for the holes created at the hetero-interface by the avalanche in GaN HEMT structure is the main failure [7], [8]. On the other hand, the removal of the holes is not yet available for the depletion-mode devices, whereas the electrons can be extracted from source to drain by 2DEG layer [9], [10].

The limit of the pulse length and the current is varied with increasing of the gate voltage pulse until failure is occurred. The peak values of the drain current and voltages for SiC cascode are demonstrated on Fig. 17, while for GaN cascode they are shown in Fig. 18 and Fig. 19. Before failure is happened, the peak current is around 1A and 20A for GaN and SiC cascode devices respectively, whereas the peak voltage is around 1200V for GaN and more than 800V for SiC. The results of the measurements illustrates that the SiC cascode devices has significantly more electro-thermal ruggedness under UIS than GaN which has almost no ruggedness.

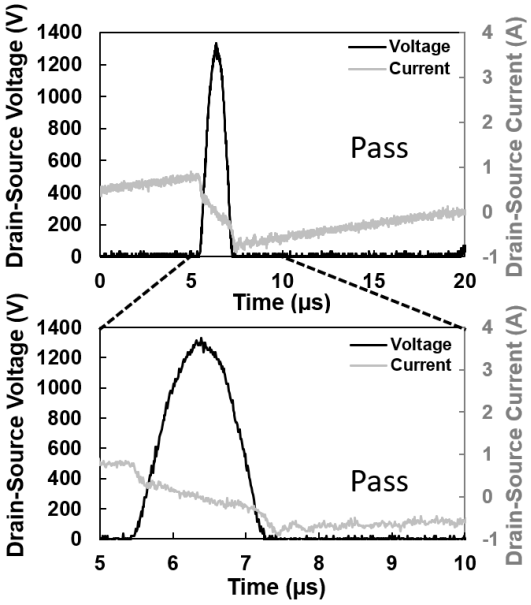

Fig. 18. GaN cascode device survives UIS test at 1 A at 1200 V.

V. Conclusion

The first systematic evaluation of SiC and GaN cascode structures considering the static, dynamic and avalanche performances. It is discussed here that SiC cascode device has better performance than the GaN cascode devices regarding to static on state losses, whereas regarding the on state resistance, the GaN cascode device has higher temperature coefficient. Furthermore, both devices have perfect reverse conduction performance due to small reverse charges. The analytical models show acceptable accuracy in trends in comparison with experimental measurements regarding the parasitic capacitor. With respect to avalanche ruggedness test with UIS, the GaN devices has no avalanche ruggedness whereas SiC cascode device withstands a level of electro-thermal stress.

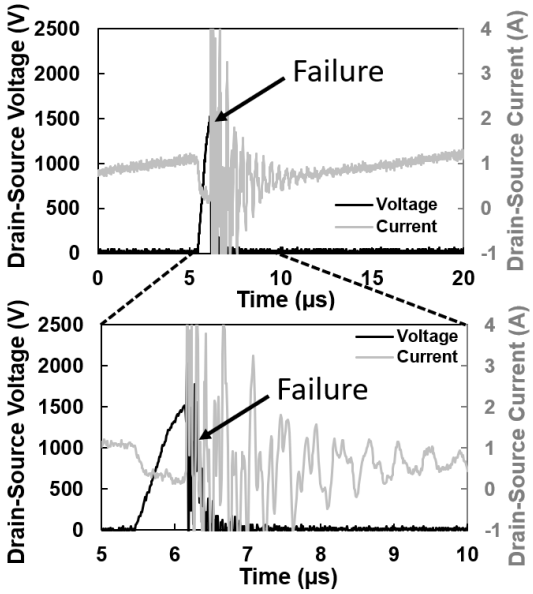

Fig. 19. Failure of GaN cascode device at UIS test at 1.5 A and 1500 V.

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