Efficient time-to-digital converters in 20 nm FPGAs with wave union methods

Wujun Xie, Haochang Chen, and David Day-Uei Li*

***Abstract*— The wave union (WU) method is a well-known method in time-to-digital converters (TDCs) and can improve TDC performances without consuming extra logic resources. However, an earlier study concluded that the WU method is not suitable for UltraScale field-programmable gate array (FPGA) devices, due to more severe bubble errors. This paper proves otherwise and presents new strategies to pursue high-resolution TDCs in Xilinx UltraScale 20 nm FPGAs. Combining our new sub-tapped delay line (sub-TDL) architecture (effective in removing bubbles and zero-width bins) and the WU method, we found that the wave union method is still powerful in UltraScale devices. We also compared the proposed TDC with the TDCs combining the dual sampling (DS) structure and the sub-TDL technique. A binning method is introduced to improve the linearity. Moreover, we derived a formula of the total measurement uncertainties for a single-stage TDL-TDC to obtain its root-mean-square (RMS) resolution. Compared with previously published FPGA-TDCs, we presented (for the first time) much more detailed precision analysis for single-TDL TDCs.**

Index Terms—**Carry chains, field-programmable gate array (FPGA), time-of-flight (ToF), time-to-digital converter (TDC)**

I. Introduction

A time-to-digital converter (TDC) is a critical time sensor, used in many industrial and scientific applications, including high-precision digital synthesizers in the enhanced Gigabit Ethernet [1], thermal management systems in very-large-scale integration (VLSI), automatic manufacturing, smart devices [2]–[5], and hardware security modules in Internet of Things devices [6], [7], positron emission tomography (PET), light detection and ranging (LiDAR), and time-resolved imaging & spectroscopy [8]–[13].

Since the dedicated adder circuits (fast carry chains) in modern FPGAs can be used as delay elements [14], [15], the tapped delay line (TDL) architecture has been the mainstream approach for FPGA-TDCs [16]–[18]. Compared with Xilinx 7-Series FPGAs, CARRY8 (CY8) modules in Xilinx UltraScale series can double the number of taps of a TDL. With CY8s, the resolution (least significant bit, LSB) of a dual-sampling (DS) TDL-TDC achieved 2.25 ps [19]. The Vernier delay line (VDL), the multi-phase and the multi-chain approaches can overcome process-related limitations [20]–[24]. These methods can achieve a better resolution than raw TDL architectures. However, they consume logic resources significantly, and the systems are in general complicated.

Digital signal processing (DSP) blocks in FPGAs can also build a TDL [25], [26]. However, the linearity is still low. The linearity of a TDC is a critical parameter; a low-linearity TDC usually causes severe measurement uncertainties, even with a high resolution. The linearity of a TDC can be characterized by the differential nonlinearity (DNL) and the integral nonlinearity (INL) [27] defined as:

$$DNL[i] = (W[i] - W_{ideal})/W_{ideal}, \quad (1)$$

$$INL[i] = \sum_{n=0}^{i} DNL[n], \quad (2)$$

where $W[i]$ is the width of the i-th bin and the W_{ideal} is the ideal bin width. We can obtain the DNL and the INL from code-density tests (CDTs) [27].

For FPGA-TDCs, the non-uniformity of carry-chains and clock skews are the two main reasons for nonlinearity [23]. Mismatched dedicated clock distributions in FPGAs cause clock skews, and large clock skews usually appear at the boundaries of clock regions [28]. The non-uniformity of carry-chains deteriorates the linearity of entire delay lines and generates ultra-small bins ($DNL \leq$ -0.90 LSB) and ultra-wide bins. We can merge ultra-small bins and abandon zero-width bins (DNL = -1.00 LSB; since they are unable to capture any information). However, ultra-wide bins deteriorate the precision of measurements and linearity significantly. To further improve the linearity and precision, calibration (for example, bin-by-bin calibration and bin-width calibration) techniques [29]–[32] have been used. However, these methods cannot ease ultra-wide bin problems.

Problems of Existing WU Methods in Advanced FPGAs: Wu and Shi proposed the wave union (WU) method to ease ultra-wide bin problems [33] in 2008. A wave union signal, containing several rising (0-1 transition) and falling (1-0 transition) edges, propagates through a single TDL, equivalent to adding more sampling taps and, therefore, improving the resolution. In the earliest WU-TDC works, only two rising edges were used [33]–[35]. Later, structures using both rising and falling edges were introduced [36], [37]. A smaller interval (between the rising and falling edges) ensures that the

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samplings at the two edges are correlated, and therefore provides better efficiency. Szplet *et al*. quantified the speed difference between the rising and falling edges in Spartan-6 FPGAs [38]. This speed difference varies with CMOS processes [39]. It was negligible in terms of the LSB in earlier TDCs. Later it became pronounced in high-resolution TDCs in more advanced CMOS technologies (due to more severe mismatches between carry-chains), leading to bubble problems (unexpected transitions of logic states) and resulting in encoding errors [17], [20]. Traditional de-bubble operations can reduce bubbles or recognize signal transitions; however, they are inefficient and introduce extra logic resources [20]. Bubble problems exacerbate and are prevalent in more advanced UltraScale FPGAs. Liu and Wang introduced a de-bubble method to solve the problem [40], but it is inefficient (the de-bubble method performed differently at rising and falling transitions). Unable to effectively solve bubble problems, Wang and Liu concluded that WU methods are not suitable for UltraScale FPGAs [19]. This conclusion has many followers (including us previously) [41]–[43], making the FPGA-TDC community believe that the WU method is not suitable for UltraScale FPGA devices. Therefore, since then, there is no efficient WU TDC reported in UltraScale FPGAs.

Our Approach: In 2018, the decomposition [17] and our sub-TDL [18] methods were proposed to efficiently remove bubbles and zero-width bins without consuming extra logic resources. Sub-TDL structures can even remove bubbles entirely [18]. In this paper, we would like to answer: A) whether the WU method is still not suitable for UltraScale FPGAs as suggested by Wang and Liu [19] if bubble-resistant sub-TDL structures are used; B) whether a combination of the sub-TDL design, DS and WU methods can achieve a resolution towards 1.0 ps LSB with maintained linearity. The main innovations of this work are:

1) We quantified the difference in the propagation speed between the rising and falling edges of a WU signal with an equation and a figure providing quantitative information for UltraScale FPGAs. Unlike the conclusion in [19], our study shows that the WU method is still powerful if we also use sub-TDL structures [18]. We presented the first efficient single-TDL WU/sub-TDL TDC in 20 nm UltraScale FPGAs. The outcomes can convince researchers to use the WU method in 20 nm FPGAs.

2) To present the efficiency of WU/sub-TDL TDCs, we also examined the other three different TDC structures. We proposed, implemented, and tested four TDCs (all with sub-TDLs):

a) WU/Sub-TDL TDC (denoted as WU TDC),
b) DS/Sub-TDL TDC (denoted as DS TDC),
c) DS/WU/Sub-TDL TDC (denoted as DSWU TDC),
d) Binned-DSWU TDC with a proposed binning method to improve the linearity.

The study confirms that WU methods are 'still' efficient.

3) Detailed analysis of measurement uncertainties for single-TDL TDCs was derived, and error sources for the proposed TDCs were identified. We found that the accumulated architecture-dependent jitters caused by delay elements are the main contributors to a TDC's precision. We also conducted

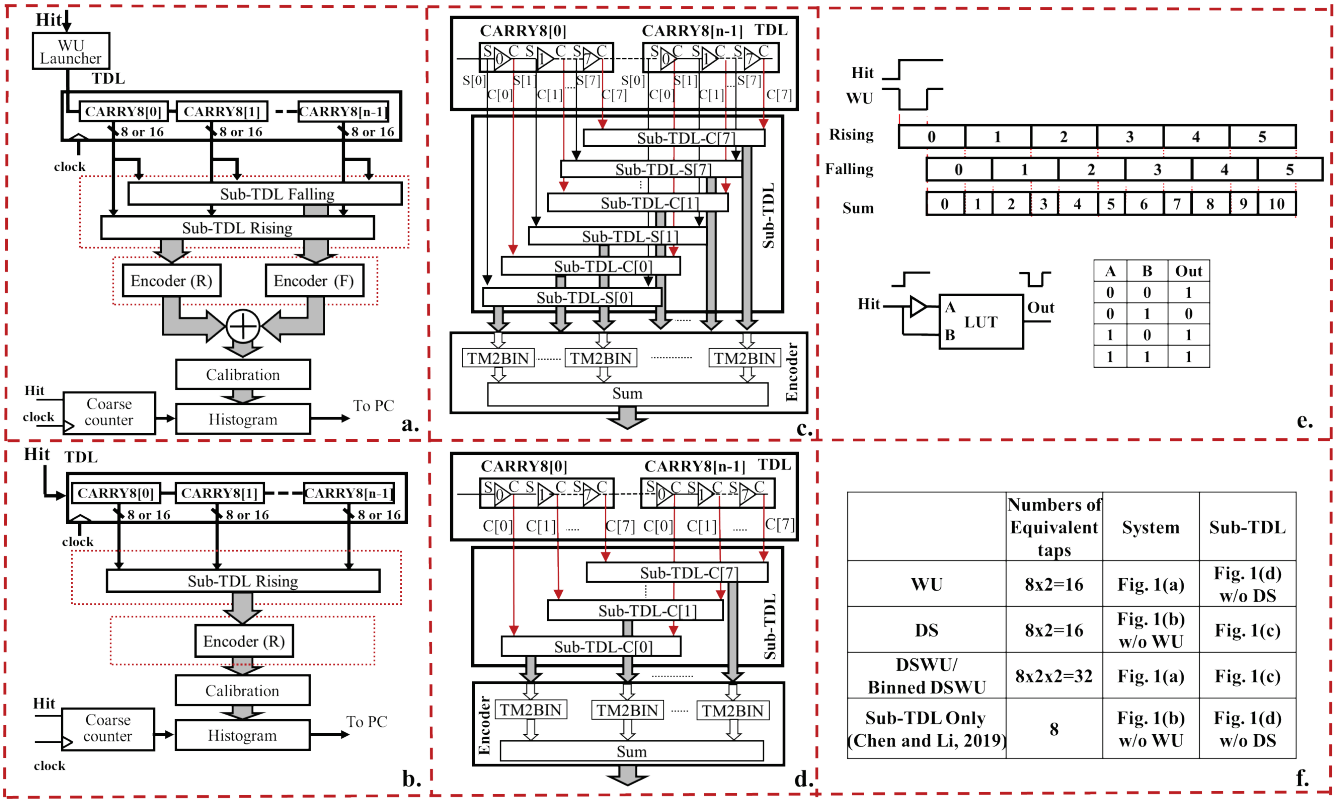

Fig. 1. Block diagrams of (a) the proposed TDC systems with the WU method, (b) the proposed TDC system without the WU method, (c) the sub-TDL structure with the DS method and the encoder, and (d) the sub-TDL structure without the DS method and the encoder. (e) The concept of the WU method and the look-up table (LUT)-based WU launcher. (f) Summary of the numbers of equivalent taps sampled from CY8 and the architectures used for the proposed TDCs.

a thorough comparison between the proposed TDCs and previously published TDCs with similar specifications (shown in Table V). The proposed single-TDL TDCs are easy to implement and stand out in terms of linearities and hardware resources, promising for multi-channel applications.

II. Design and Architecture

The TDL architecture was used for the proposed TDCs and implemented with CY8s in the UltraScale XCKU040 FPGA (KCU105 development board). Figure 1 contains the block diagrams of the structures used for the proposed TDCs (the sub-TDL [18] is the backbone for all TDCs). Figures 1a and 1b are the system architectures for WU-based TDCs and non-WU-based TDCs, respectively. For WU TDCs, a WU signal (with a rising and a falling edges) is fed into a TDL, and the delay taps are sampled twice, by Sub-TDL Rising and Sub-TDL Falling modules respectively (stored by flip-flops, FFs). For non-WU TDCs in Fig. 1b, the hit signal is fed to the TDL directly and sampled by the Sub-TDL Rising only, with the launcher, Sub-TDL Falling and the corresponding encoder removed. Figures 1c and 1d are the sub-TDL structures with and without the DS method. With the DS method, both carry C and sum S outputs of CY8 are sampled by a sub-TDL module, whereas non-DS designs only use C outputs of CY8. With sub-TDL techniques [18], the raw thermometer code generated by a TDL is split into several subsets. Sub-thermometer codes are converted to binary codes (by TM2BIN). Figure 1e shows the WU-A launcher implemented with a look-up table (LUT), and Fig. 1f summaries the numbers of taps from CY8 and the architectures used for the proposed TDCs.

A. Dual-sampling Structure with Sub-TDL

The DS TDL structure was proposed in [19]. Compared with CARRY4 structures in earlier FPGAs, CY8 structures in UltraScale FPGAs double the tap number or the equivalent bins of a TDL within a certain propagation delay. The theoretical resolution or the average bin size reduces by half. However, the linearity degrades when the resolution is enhanced. We implemented a DS TDC with sub-TDLs [18] achieving 2.53 ps resolution, and Figure 2a presents the linearity performance.

In Fig. 2a, the large clock skew results in a distinct step in the INL curve (~Bin 450) due to the clock distribution tree's bifurcation. Calibrations are required for solving this problem and correcting the accumulated offset. The bin-by-bin calibration is to calibrate the times aligned to bin centers to correct the INL. Besides, double-phase sampling [23] techniques can alleviate clock skew problems. Figure 2b presents the DS TDC's linearity performance (with 390 bins), with the INL_{pk-pk} (peak-to-peak INL) improved to 9.80 LSB.

B. Bubble Problems Introduced by Wave Union Methods

As shown in Fig. 1e, with rising and falling sampling edges, a WU TDC can perform like a TDC with two delay lines (rising and falling). The resolution of the WU TDC is:

$$LSB_{wu} = \frac{MR}{N_{wu}} = \frac{MR}{N_{rising}+N_{falling}} = \frac{LSB_{rising} \times LSB_{falling}}{LSB_{rising}+LSB_{falling}}, \quad (3)$$

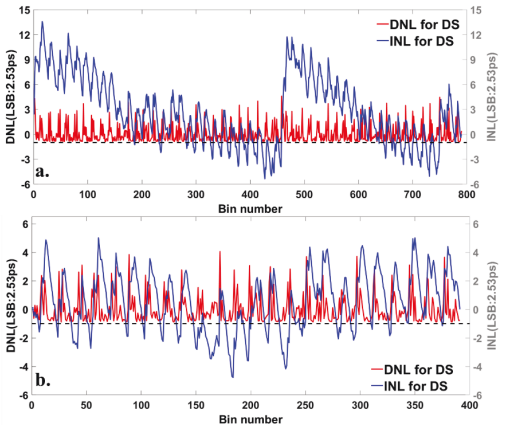

Fig. 2. a) DNL and INL curves for the 790-bin DS TDC. b) DNL and INL curves for the 390-bin DS TDC.

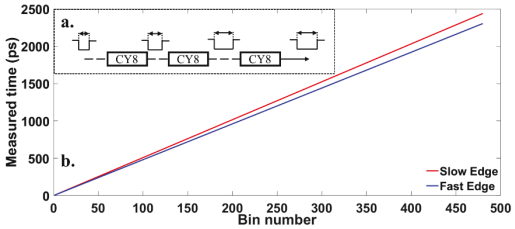

Fig. 3. (a) An example of the propagation speed difference between the rising and falling edges. (b) The bin number versus the measured time fitting curves for the rising and falling edge signals.

TABLE I.
INTERPOLATION EFFICIENCY ON RESOLUTION

	Device	Fast edge (ps)	Slow edge (ps)	WU signal (ps)
[39][1]	Virtex-5	35.90	37.43	18.23
	Artix-7	15.50	15.97	7.83
[38]	Spartan-6	15.20	16.10	7.82 [2]
This Work	UltraScale	4.79	5.08	2.46 [2]

[1] Averaged value in [39]. [2] Calculated values based on Eq. (3).

where MR is the measurement range of the delay line. N_{wu}, N_{rising}, and $N_{falling}$ are the bin numbers of the WU TDC, the plain TDC with the rising sampling, and the plain TDC with the falling sampling, respectively.

The WU interpolation efficiency on the resolution was revealed in several studies [38]–[40]. The propagation speed of the falling and rising edges in different FPGA devices (from 65 nm to 28 nm) were quantified in [38], [39] (included in Table I). We performed similar tests in UltraScale FPGAs and quantified the impact, feeding the rising edge and the falling edge to a TDL separately. The results do show the speed differences between the falling and rising edges. Figure 3a shows the principle of the propagation speed difference; the gap between the rising and falling edges varies when the WU signal propagates along the TDL. Figure 3b shows the fitting curves between the bin number and the measured time for the edge signals; the edges use different numbers of taps to convert a fixed time interval. In our tests, the LSB of the slower edge is 5.08 ps, whereas the LSB of the faster edge is 4.79 ps, see Fig. 3b. For the WU signal containing a pair of 0-1 and 1-0 transitions, the LSB should be 2.46 ps, according to Eq. (3), see Table I. Although the bin realignment [40] can remove most

bubbles, it performs differently for rising and falling transitions due to the speed difference. Therefore, bubbles cannot be removed easily in traditional WU TDCs [19].

C. Wave Union Method with Sub-TDL to Remove Bubbles

The mismatch [20] in tap timing along the TDL exacerbates when the tap interval is shorter, causing more severe bubble problems, especially in more advanced process technologies [42]. Because of this bubble problem and the speed difference between rising and the falling edges, Ref. [19] concluded: "The wave union method cannot be used in the UltraScale FPGA for further improving the time precision". However, we find that it is not the case in our designs combing sub-TDL structures.

As stated earlier, the bubble-free sub-TDL structure (or the decomposition developed independently at the same time [17]) can be used [18]. The main idea is to ease mismatch problems in the TDL by elongating the tap intervals [18]. With sub-TDLs, bubbles can be easily removed, and the WU method is 'still' efficient in UltraScale FPGAs. A TDC using an 8-edge WU signal was proposed [44]; however, the encoding process is much more complicated. The sub-TDL should be modified if more edges are used, but it is out of this study's scope.

D. Compensation Strategies

Uneven TDLs cause large nonlinearity (see Fig. 4, the actual TDLs). A fast calibration approach, called the bin compensation strategy, was used to improve linearity, aiming

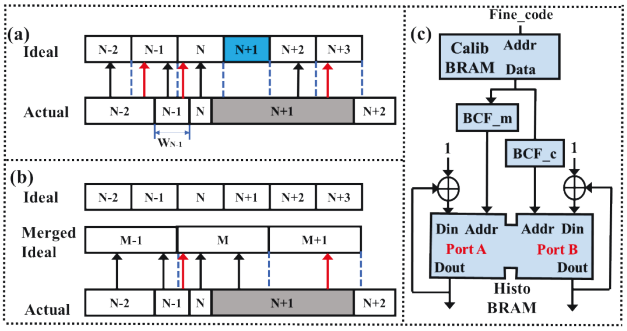

Fig. 4. Concepts of (a) the compensation strategy and (b) the binning method. (c) Hardware implementation of the compensation method.

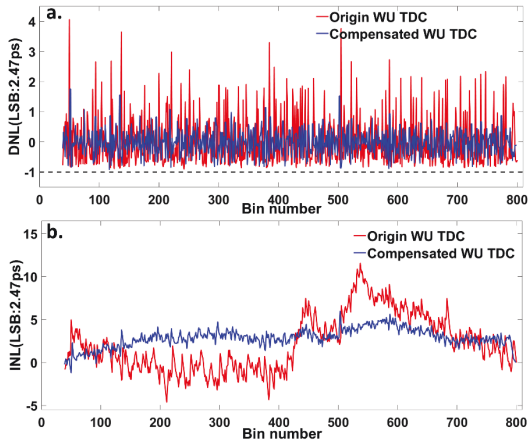

Fig. 5. DNL and INL performances. (a) DNL and (b) INL plots of the original WU TDC and the compensated WU TDC in the UltraScale FPGA (810 bins).

to compensate the bins with a nominal bin width [18]. In this method, two factors, the main bin calibration factor (BCF_m, highlighted in black arrow in Fig. 4) and the compensation bin calibration factor (BCF_c, highlighted in red arrow in Fig. 4), are introduced to reassign the TDC's fine codes to the corrected bins. We can calculate the addresses of corrected bins based on CDTs. $T[k]$ can be defined as:

$$T[k] = \sum_{n=0}^{k-1} W[n] = \sum_{n=0}^{k-1}\{LSB \times (DNL[n] + 1)\}, \qquad (4)$$

where $W[n]$ is the width of the n-th bin. BCF_m and BCF_c are calculated accordingly. For example, the uneven $\text{Bin}_{\text{actual}}$ *N-2* collects a larger count proportional to its bin width, and therefore it is necessary to assign a proportion of the count to $\text{Bin}_{\text{ideal}}$ *N-1* through BCF_c. This compensation strategy works well if the bin boundaries do not deviate from the ideal bin boundaries (highlighted in dash lines). As each bin only has at most one BCF_m and one BCF_c, this compensation method makes $\text{Bin}_{\text{ideal}}$ *N+1* receiving no count allocation (due to the ultra-wide $\text{Bin}_{\text{actual}}$ *N+1*, as $\text{Bin}_{\text{actual}}$ *N+1* has already assigned its contribution to $\text{Bin}_{\text{ideal}}$ *N+2* and *N+3*) and therefore resulting in a missing code. This method can remap and compensate bins at the same time without changing the resolution. A few missing codes can be ignored with a slightly degraded resolution, and the compensation process is simplified as the pseudocode below.

```
For k = 1: N
if (T_actual [k] < T_ideal [k])
    if (T_actual [k+1] < T_ideal [k])
        BCF_m = k − 1
        BCF_c = void
else if (T_actual [k+1] > T_ideal [k])
        BCF_m = k − 1
        BCF_c = k
else    continue…
```

We realized this method with two block-random-access memory (BRAM) modules (see Fig. 4c). The two factors are fetched from the calibration BRAM based on the fine code from the TDL and then are fed to the histogram BRAM, which is implemented by two BRAMs in the simple dual-port mode. With the on-board compensation method, the post-processing time can be reduced. However, more troublesome missing code problems degrade the INL and the performance significantly, especially for two-stage TDCs [45], [46]. A new compensation method is still to be developed. We will propose a simple approach in this study, see Sec. II-F.

Figure 5 presents the linearity performances of the original and the compensated WU TDCs. For compensated WU TDCs, the DNL is [-0.92, 1.75] LSB and the INL is [-1.20, 5.97] LSB.

E. Dual-sampling Wave Union TDC with Sub-TDL

As shown in Fig. 1e, the TDL taps are sampled twice (by the rising and the falling edges), doubling sampled taps. The DS structure also doubles sampled taps. Therefore, to achieve a better resolution, a TDC combining WU and DS denoted as DSWU TDC, was also implemented, see Fig. 1a and Fig. 1c.

The DSWU TDC can achieve 1.23 ps resolution. The linearity, however, degrades when the resolution is improved.

F. Binned Dual-sampling Wave Union TDC

We used a binning method to improve the DSWU TDC's linearity, inspired by the compensation strategy and the bin decimation method in [42]. As shown in Fig. 4b, a set of merged ideal bins are constructed by merging two consecutive bins into larger bins. Then the compensation strategy can improve the linearity. The central concept is to reduce the numbers of ultra-wide bins and ultra-small bins, hence improving both the DNL and the INL.

III. Experimental Results

The experimental setup is shown in Fig. 6. The proposed TDCs were implemented and tested in the Xilinx KCU105 development board, running at 500 MHz. The hit signal and the system clock were generated from the synthesized clock generator SRS CG-635 (Stanford Research Systems) and the jitter attenuator Si 5324-EVB (Silicon Labs), respectively. Both devices can generate low-jitter signals. CDTs aim to assess the linearity performances, whereas time interval tests (TITs) aim to obtain the measurement errors and the root-mean-square (RMS) resolution. Two independent signal sources were used for CDTs, and there is no correlation between the hit signal and the TDC clock [30]. In TITs, Si 5324-EVB and SRS CG-635 are synchronous to a 10 MHz signal (highlighted in red, see Fig. 6). With the phase-shifting function provided by SRS CG-635, we can obtain a controllable time interval between the hit signal and the system clock. For a fixed time interval, measurements were repeated 50,000 times.

A. Linearity Test Results

DNL, INL and their standard deviations (σ_{DNL} and σ_{INL}) are important parameters for evaluating a TDC's linearity. Two equations were derived to assess the equivalent bin width and its standard deviation, summarized in [47]:

$$\sigma_{eq}{}^2 = \sum_{i=1}^{N}\left(\frac{W[i]^2}{12} \times \frac{W[i]}{W_{total}}\right) \text{ where } W_{total} = \sum_{i=1}^{N} W[i], \quad (5)$$

$$w_{eq} = \sigma_{eq}\sqrt{12} = \sqrt{\sum_{i=1}^{N}\left(\frac{W[i]^3}{W_{total}}\right)}, \quad (6)$$

where w_{eq} is the equivalent bin width and σ_{eq} is the standard deviation of the equivalent bin width (named differently by other groups, for example, the quantization error σ_Q [48]).

The linearity performances of the proposed TDCs are listed in Table II. With the compensation strategy, the linearity of the WU TDC is much better. The DNL_{pk-pk} (peak-to-peak DNL) is enhanced from 4.96 to 2.67 LSB, whereas INL_{pk-pk} is also improved significantly after the compensation. Compared with the original WU TDC and the DS TDC, the WU method is still advantageous in easing ultra-wide bin problems. The DNL_{pk-pk} of the original WU TDC is 4.96 LSB, but that of the DS TDC is 5.52 LSB. The compensation strategy is less suitable for the DS TDC due to more ultra-wide bins.

Figure 7 shows DNL and INL curves for the DSWU TDC. The resolution of the DSWU TDC is 1.23 ps. The DNL_{pk-pk} is 8.77 LSB and the INL_{pk-pk} is 31.06 LSB. The DNL and INL curves for the binned-DSWU TDC are shown in Fig. 8. The DNL is [-0.93, 1.68] LSB and the INL is [-1.78, 2.67] LSB. Compared with the compensated WU TDC, the binning method is still advantageous, even though they have a similar resolution. The INL_{pk-pk} for the binned-DSWU TDC (4.45 LSB) is much smaller than the compensated WU TDC (7.17 LSB). The binning method can also improve linearity with less distortion. Figure 9 shows the bin width distributions of the compensated WU and the binned-DSWU TDCs. The binned-DSWU TDC has a more concentrated bin-width distribution. Figure 9 shows that σ_{DNL} of the compensated WU (0.43 LSB) and the binned-DSWU (0.35 LSB) TDCs also show that the binned-DSWU TDC can deliver more robust results.

B. Time-Interval Tests (TIT)

The precision can be estimated by the standard deviation of the distribution of repeated measurements. It can be affected by clock jitters, jitters of input signals, electronic noise, and process, voltage and temperature (PVT) variations [49].

The TIT results and the RMS resolutions for the proposed

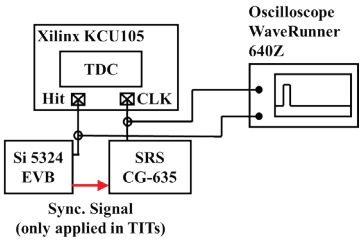

Fig. 6. Test setup for CDTs and TITs.

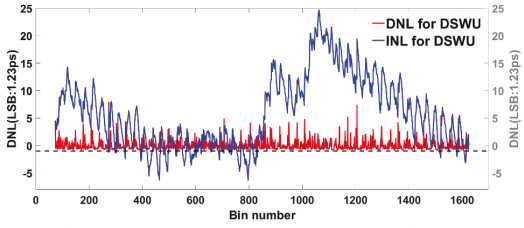

Fig. 7. DNL and INL curves for the DSWU TDC (1626 bins).

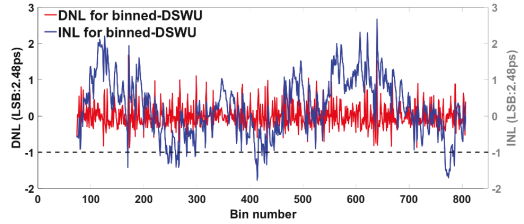

Fig. 8. DNL and INL curves for the binned-DSWU TDC (807 bins).

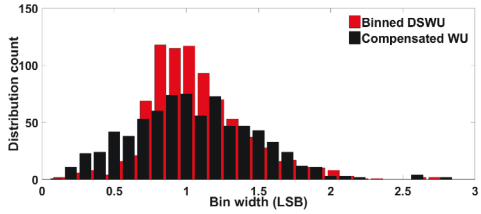

Fig. 9. Bin width distributions for the compensated WU TDC and the binned-DSWU TDC.

TABLE II.
COMPARISON OF THE LINEARITY PERFORMANCES BETWEEN FOUR DIFFERENT TDC DESIGNS IN ULTRASCALE 20 NM FPGAS

	Original WU	Compensated WU	DS	DSWU	Binned-DSWU
LSB (ps)	2.47		2.53	1.23	2.48
DNL	[-0.90, 4.06]	[-0.92, 1.75]	[-0.93, 4.59]	[-0.84, 7.93]	[-0.93, 1.68]
DNL_{pk-pk}	4.96	2.67	5.52	8.77	2.61
σ_{DNL}	0.82	0.43	1.07	0.93	0.35
INL	[-4.62, 11.58]	[-1.20, 5.97]	[-5.39, 13.57]	[-6.36, 24.70]	[-1.78, 2.67]
INL_{pk-pk}	16.20	7.17	18.96	31.06	4.45
σ_{INL}	3.26	1.06	4.01	6.42	0.80
w_{eq} (ps)	4.85	2.99	6.51	2.95	2.95
σ_{eq} (ps)	1.87	0.86	1.88	0.85	0.85

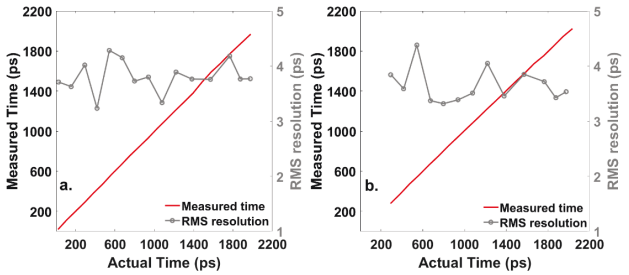

Fig. 10. TIT results and RMS resolutions for (a) the DS TDC system and (b) the WU TDC system.

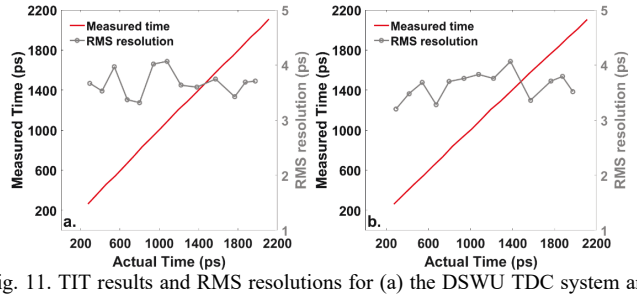

Fig. 11. TIT results and RMS resolutions for (a) the DSWU TDC system and (b) the binned-DSWU TDC system.

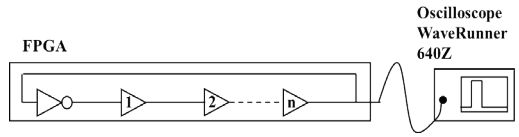

Fig. 12. Test setup for investigating jitters of LUT and the delay element.

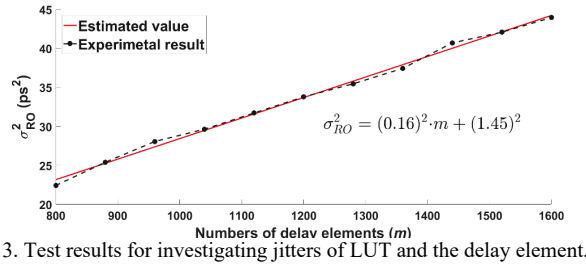

Fig. 13. Test results for investigating jitters of LUT and the delay element.

TDCs are shown in Figs 10 and 11. The averaged RMS resolutions for the DS, and the WU TDCs are 3.80 ps and 3.64 ps, respectively, whereas the averaged RMS resolutions for the DSWU and the binned-DSWU TDCs are 3.67 ps and 3.63 ps.

C. Analysis of Measurement Uncertainties

Szplet *et al.* estimated measurement uncertainties by analyzing error sources of two-stage multi-phase TDCs [50]. We extended their analysis approach for our single-stage TDCs, and the RMS resolution can be derived as:

$$\sigma^2_{system} = \sigma^2_{in} + \sigma^2_{sig} + \sigma^2_{eq} + \sigma^2_{clk}, \tag{7}$$

σ^2_{in} is the jitter introduced by the input signal. σ_{sig} is the jitter when a signal propagates along a delay line:

$$\sigma^2_{sig} = \sigma^2_{wu} + \sigma^2_{DL}, \tag{8}$$

where σ_{wu} is the jitter caused by the wave-union launcher and several delay elements in the tapped delay line (σ_{DL}) are involved. The wave union launcher contains a LUT and a CY8 (each CY8 contains eight delay elements (σ_{CY})), and therefore, σ_{wu} can be expressed:

$$\sigma^2_{wu} = 8\sigma^2_{CY} + \sigma^2_{LUT}, \tag{9}$$

It is difficult to predict how many delay elements of the TDL are involved in measurements. However, according to [50], a TDL with n delay elements can have σ_{DL} as:

$$\begin{aligned} \mathrm{E}[\sigma^2_{\mathrm{DL}}] &= \sum_{i=1}^{n} \sigma^2_{\mathrm{DL}i} \cdot p(\sigma^2_{\mathrm{DL}i}) = \sum_{i=1}^{n} i \cdot \sigma^2_{\mathrm{CY}} \cdot p(\sigma^2_{\mathrm{CY}}) \\ &= \sum_{i=1}^{n} i \cdot \sigma^2_{\mathrm{CY}}/n = (\sigma^2_{\mathrm{CY}}/n) \sum_{i=1}^{n} i \\ &= \frac{n+1}{2}\sigma^2_{\mathrm{CY}} \approx \frac{n}{2}\sigma^2_{\mathrm{CY}}, \end{aligned} \tag{10}$$

where σ_{DL_i} is the jitter caused by i-th delay element and the i-th delay element has the probability $p(\sigma^2_{\mathrm{DL}i})$ of hitting during a signal measurement. Because the delay element is CY8, $\sigma^2_{DL_i} = i\sigma^2_{CY}$ and $p(\sigma^2_{\mathrm{DL}i}) = p(\sigma^2_{\mathrm{CY}})$. From Eqs (7)–(10), the RMS resolution becomes:

$$\sigma^2_{system} = \sigma^2_{in} + \sigma^2_{clk} + \sigma^2_{eq} + \sigma^2_{LUT} + \left(\frac{n}{2} + 8\right)\sigma^2_{CY}, \tag{11}$$

To obtain an estimated value of σ_{LUT} and σ_{CY}, a ring oscillator (RO) was constructed, as shown in Fig. 12. There are m delay elements in the RO, and the jitter of the RO is:

$$\sigma^2_{RO} = \sigma^2_{LUT} + m\sigma^2_{CY}, \tag{12}$$

From Fig. 13, $\sigma_{CY} = 0.16$ ps and $\sigma_{LUT} = 1.45$ ps. The values of σ_{CY} and σ_{LUT} are slightly larger than those in 45 nm

Spartan-6 FPGAs, but the difference is minimal (see TABLE III, Ref. [50]). The results can be affected by experimental setups, including evaluation boards and instruments. Moreover, more advance CMOS manufacturing technologies might also contribute higher uncertainties with much smaller (width and length of gates) transistors, resulting in more thermal noise [51]. Therefore, it is reasonable that the presented results are slightly different from those in Ref. [50]. The four proposed TDCs have similar structures, and there is no WU launcher in the DS TDC, so $\sigma_{sig} =$ 2.74 ps (for WU, DSWU and binned-DSWU TDCs) and $\sigma_{sig} =$ 2.33 ps (for DS TDC).

Measured by the oscilloscope, the jitter caused by the clock signal (σ_{clk}, generated by SRS CG-635) is 1.49 ps and the jitter introduced by the hit signal (σ_{in}, generated by Si 5324-EVB) is 1.53 ps. We introduced σ_{TDC} to evaluate the RMS resolution of the TDC, and it can be expressed as Eq. (13). Hence, σ_{system} can be modified as Eq. (14). The measurement uncertainties of the proposed TDCs are listed in Table III (two previously published works in 45 nm and 20 nm FPGAs are also listed) with our analysis providing more detailed contributions from error sources. Additional jitters caused by input circuits are significant for some complicated structures [50]. However, the impact is negligible for our single-stage TDCs. The results (σ_{system}) obtained from the error source analysis agree with those obtained from TIT tests.

$$\sigma_{TDC}^2 = \sigma_{sig}^2 + \sigma_{eq}^2. \quad (13)$$

$$\sigma_{system}^2 = \sigma_{TDC}^2 + \sigma_{in}^2 + \sigma_{clk}^2. \quad (14)$$

D. Consumption of Logic Resources

The power consumption and the logic resources required for the proposed TDCs were calculated using the electronic design automation (EDA) tool (Vivado Design Suite) and summarized in Table IV. Extra logic resources were used when using the WU method and the DSs structure (more BRAMs needed to perform histogram functions). However, the usages of logic resources for the proposed TDCs are still low, showing great potential for multiple-channel applications.

The implementation layouts of the DSWU TDC are shown in Fig. 14. The TDL is confined within a central clock region (Slices X49Y120~X49Y179) to avoid large clock skews. The WU launcher is in Slice X49Y119. These constraints are also applicable to the WU TDC and the binned-DSWU TDC. For the DS TDC, the constraints for the WU launcher are not required.

Figure 14 shows that the layouts do not consume much hardware resources, and therefore the proposed TDCs are suitable for multi-channel applications. If a more extended measurement range is required, coarse counters can be easily included for the proposed TDCs.

IV. Discussions & Comparisons

Compared with previously published works with similar resolutions (see Table V), our TDCs are easy to implement and have better performances in the linearity or logic-resource consumption. Compared with our DS/Sub-TDL TDC with the DS TDC in [19], our sub-TDL structure can maintain the linearity by removing zero-width bins without extra logic resources. Compared with the multi-phase TDC in [24], the proposed DSWU TDC has better linearity. Consuming less hardware is essential, as a design achieving this goal is promising for multi-channel applications. In this aspect, the proposed TDCs stand out compared to the other methods in Table V. 5-core 2D-Vernier TDCs [22] achieved similar performances but used 28-fold more LUTs than our WU TDC. Multichain 0.3 ps resolution TDCs [52] had limited precision (< 8.50 ps), but their linearity was not revealed at all. 20-chain TDCs [53] used 8-fold (another multi-chain TDC [54] produced worse precision and used 3-fold more LUTs) LUTs, 2-fold flip-flops (FFs) and 6-fold BRAMs more than our DSWU TDC. Although 20-chain TDCs [53] could have better INL performances with offset corrections, they require 127 DSP blocks and are complicated to implement due to chain-by-chain and chip-by-chip corrections. 2-stage interpolation TDCs [55] (with much more complex structures) used at least 1- or 2-fold

TABLE III.
EVALUATION OF MEASUREMENT UNCERTAINTIES

	Spartan-6 (45 nm)	UltraScale (20 nm)				
	[50]-2019	[18]-2019	Compensated WU	DS	DSWU	Binned-DSWU
LSB (ps)	-	5.02	2.47	2.53	1.23	2.48
Error Source Analysis						
σ_{clk} (ps)	1.93	-	1.49			
σ_{in} (ps)	2.64	-	1.53			
σ_{CY} (ps)	0.153	-	0.16			
σ_{LUT} (ps)	1.33	-	1.45			
σ_{sig} (ps)	**-**	**-**	**2.74**	**2.33**	**2.74**	**2.74**
σ_{eq} (ps)	-	1.45	0.86	1.88	0.85	0.85
σ_{TDC} (ps)	**-**	**-**	**2.88**	**2.99**	**2.87**	**2.87**
σ_{system} (ps)	**10.19**	**-**	**3.58**	**3.68**	**3.58**	**3.58**
Time Interval Test						
σ_{system} (ps)	**-**	**7.8**	**3.64**	**3.80**	**3.67**	**3.63**

TABLE IV.
CONSUMPTION OF LOGIC RESOURCES

		w/o WU [18]	WU	DS	DSWU/ Binned-DSWU
Modules	Total	Used	Used	Used	Used
CY8	30300	80 (0.26%)	85 (0.28%)	76 (0.25%)	88 (0.29%)
LUT	242400	703 (0.29%)	1349 (0.56%)	1272 (0.52%)	2460 (1.01%)
FF	484800	1195 (0.24%)	1840 (0.38%)	2190 (0.45%)	3463 (0.71%)
BRAM	600	1.5 (0.25%)	4.5 (0.75%)	3.5 (0.58%)	7.5 (1.25%)
CLB*	30300	-	251 (0.83%)	211 (0.79%)	405 (1.37%)
Power	-	-	0.92	0.88	1.03

* Configurable logic block, including several LUTs, FFs and a CY8 [15].

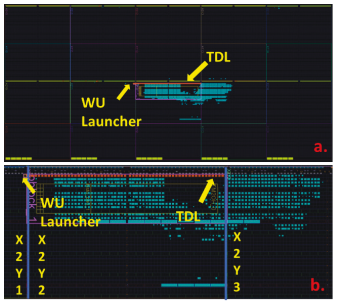

Fig. 14. Implementation layouts of the DSWU TDC. a) Overview. b) Clock regions (X2Y1 ~ X2Y3).

TABLE V.
COMPARISON OF PUBLISHED FPGA-BASED TDCS AND THE PROPOSED TDCS

Ref-Year	Methods	Device	LSB (ps)	RMS Resol. (ps)	DNL, DNL_{pk-pk} (LSB)	INL, INL_{pk-pk} (LSB)	CLB	LUT	FF	B-RAM	DSP
[55] **-16**	Multichain, TDL 2-stage, WU-A	Spartan-6	0.90	< 6.00	[-1.00, 6.25] [1]	[-26.20, 11.50], 37.70	N/S	N/S	4364 [4]	N/S	0 [4]
[16] **-16**	Tuned-TDL	Kintex-7	10.6	N/S	[-1.00, 1.45], 2.45	[-1.23, 4.30], 5.53	N/S	577	1641	N/S	0 [4]
		Virtex-6	10.1	N/S	[-1.00, 1.18], 2.18	[-3.03, 2.46], 5.49	N/S	577	1641	N/S	
		Spartan-6	16.7	N/S	[-1.00, 1.22], 2.22	[-0.70, 2.56], 3.26	N/S	261	787	N/S	
[19] **-16**	DS	UltraScale	2.25	3.90	[-1.00, 4.78] [1]	N/S	N/S	N/S	1810 [4]	N/S	0 [4]
[56] **-16**	Measurement Matrix	Virtex-5	7.40	6.80	[-0.74, 0.74], 1.48	[-1.52, 1.57], 3.09	1265	666	1410	2	0 [4]
[22]-**17**	2D-Vernier, Multi-core	Stratix IV	2.50	6.72	[-0.56, 0.46], 1.02	[-2.98, 3.23], 6.21	N/S	37420 5-core	N/S	N/S	0 [4]
[32] **-17**	Tuned-TDL Direct Histogram	Virtex-7	10.5	N/S	[-0.04, 0.04], 0.08	[-0.09, 0.04], 0.13	N/S	N/S	N/S	N/S	0 [4]
[53] **-17**	Multichain, TDL Offset-correction	Virtex-7 (250 MHz)	1.15	3.50	[-0.98, 3.50], 4.48	[-5.90, 3.10], 9.00	N/S	19666	7000 [4]	43	127 [5]
[24] **-18**	Multi-phase	Cyclone V	1.56	2.30	[-1.00, 5.60] [1]	[-8.00. 35.00] [1]	N/S	N/S	1300 [4]	N/S	0 [4]
[18] **-19**	Multi-channel Sub-TDL	UltraScale	5.02	7.80	[-0.12, 0.11], 0.27	[-0.18, 0.46], 0.59	271	703	1195	1.5	0 [4]
[44] **-19**	WU-A, TDL (eight edges)	Kintex-7	1.77	3.00	[-1.00, 4.50] [1]	[-37.70, 12.00] [1]	N/S	4010	7503	14	0 [4]
[54] **-19**	Multichain, WU, Multichannel	Artix-7	2.00	< 12.50	N/S	N/S, 2.10	N/S	7010	3738	1.5	0 [4]
[52] **-19**	Multichain, WU, Multichannel	UltraScale	0.30	< 8.50	N/S	N/S	3200	N/S	N/S	11.1	1
[57] **-20**	Bidirectional Vernier	Stratix III	24.5	28	[-0.20, 0.25], 0.45	[0.03, 0.82], 0.85	N/S	172	986	N/S	0 [4]
[58] **-20**	Gain & error cal., Moving average	Artix-7	4.88	2.90~ 8.03	[-0.10, 0.15], 0.25	[-0.23, 0.28], 0.51	N/S	2962	4157	N/S	0 [4]
[59] **-21**	Large scale parallel routing	Kintex-7	1.29	3.54	[-1.20, 1.40], 2.60	[-3.28, 3.78], 7.06	2200	1002	3900	2	0 [4]
This Work	**Sub-TDL, WU-A Compensation**	**UltraScale**	**2.47**	**3.64 [2] 3.58 [3]**	**[-0.92, 1.75], 2.67**	**[-1.20, 5.97], 7.17**	**251**	**1349**	**1840**	**4.5**	**0**
	Sub-TDL, DS		**2.53**	**3.80 [2] 3.68 [3]**	**[-0.93, 4.59], 5.52**	**[-5.39, 13.57], 18.96**	**211**	**1272**	**2190**	**3.5**	**0**
	Sub-TDL, DS WU-A		**1.23**	**3.67 [2] 3.58 [3]**	**[-0.84, 7.93], 8.77**	**[-6.36, 24.70], 31.06**	**405**	**2460**	**3463**	**7.5**	**0**
	Sub-TDL, DS WU-A, Binning		**2.48**	**3.63 [2] 3.58 [3]**	**[-0.93, 1.68], 2.61**	**[-1.78, 2.67], 4.45**	**405**	**2460**	**3463**	**7.5**	**0**

[1] Approximate values from figures presented in literature; [2] Data obtained from TITs; [3] Data obtained from the analysis of measurement uncertainties.
[4] Estimated values based on the architectures and encoding methods. [5] 20-chain TDCs require 127 DSP blocks and need much more LUTs, FFs, and BRAMs.

more FFs than our 1-stage DSWU TDC, whereas WU TDCs in [44] consumed 2-fold more LUTs and FFs than our DSWU TDC. Moreover, our TDCs are more cost-effective in configurable logic blocks than matrix TDCs [56] and TDCs with large scale parallel routing methods [59]; our TDCs are much more suitable for multi-channel applications.

For high-resolution (< 2.5 ps) TDCs, precisions can be easily affected by jitters caused by the system clock and the hit signal. Low jitter signal generators are essential in TITs for assessing high-resolution TDCs. However, the error source analysis is an effective way to obtain precision. For a fixed architecture (σ_{sig}), σ_{eq} is the only factor that varies when different methods are implemented and can be reduced by improving the resolution and the DNL, from Eq. (5). Therefore, the DSWU TDC (higher resolution) achieves similar precision with the WU TDC and binned-DSWU TDC (better DNL). From our study, the architecture-dependent jitter σ_{sig} is the main contributor to the measurement uncertainties of the proposed TDCs (σ_{TDC}: ~2.9 ps). The precisions of the proposed WU-related TDCs (σ_{eq}: ~0.85 ps) reach the upper limit of their structures, and the precision of DS TDC, however, can still be further improved with σ_{eq} = 1.88 ps. The architecture-dependent jitter σ_{sig} is also the main reason why previously reported high-resolution (< 2.5 ps) TDL-TDCs can only achieve limited precisions (> 3 ps) [21], [53], [55].

V. CONCLUSION

This paper proposed four new TDC architectures with the sub-TDL topology: DS, WU, DSWU and binned-DSWU TDCs. Different from previously reported studies [19], [41]–[43], we concluded that the WU method is still efficient in improving the resolution with maintained linearity in UltraScale FPGAs when the sub-TDL structure is also integrated. By combining the DS structure, the WU method and the sub-TDL architecture, a DSWU TDC with 1.23 ps resolution was implemented and evaluated. A binning method was also implemented to the

proposed binned-DSWU TDC to improve the linearity. Due to the single-TDL structure, our TDCs are easy to implement and have better linearity or resource consumption performances compared with previously published works with similar resolutions (see Table V). Hence, the proposed TDCs have great potential for multi-channel applications.

Moreover, with detailed error source analysis, we found that high-resolution TDCs have limited precisions, mainly determined by the architecture-dependent jitter (σ_{sig}). With a fixed structure, the precision can be improved by reducing σ_{eq} and σ_{clk}. However, the jitter σ_{sig} from delay elements has a decisive impact on the precision of a TDC. Therefore, low-jitter architectures are essential in future high-resolution TDC studies.

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REFERENCES

[1] W. Pan, G. Gong, Q. Du, H. Li, and J. Li, "High resolution distributed time-to-digital converter (TDC) in a White Rabbit network," *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 738, pp. 13–19, Feb. 2014.

[2] R. S. S. M. R. Krishna, A. K. Mal, and R. Mahapatra, "CMOS time-mode smart temperature sensor using programmable temperature compensation devices and ΔΣ time-to-digital converter," *Analog Integr. Circuits Signal Process.*, vol. 102, no. 1, pp. 97–109, Jan. 2020.

[3] W. Song, J. Lee, N. Cho, and J. Burm, "An Ultralow Power Time-Domain Temperature Sensor With Time-Domain Delta–Sigma TDC," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 64, no. 10, pp. 1117–1121, Oct. 2017.

[4] C. Chen, C. Chen, Y. Lin, and S. You, "An All-Digital Time-Domain Smart Temperature Sensor With a Cost-Efficient Curvature Correction," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 27, no. 1, pp. 29–36, Jan. 2019.

[5] Y. Chen *et al.*, "A +0.66/−0.73 °C Inaccuracy, 1.99-μW Time-Domain CMOS Temperature Sensor With Second-Order ΔΣ Modulator and On-Chip Reference Clock," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 67, no. 11, pp. 3815–3827, Nov. 2020.

[6] Z. Liang, H. Wei, and T. Liu, "A Wide-Range Variation-Resilient Physically Unclonable Function in 28 nm," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 817–825, Mar. 2020.

[7] D. R. E. Gnad, F. Oboril, S. Kiamehr, and M. B. Tahoori, "An Experimental Evaluation and Analysis of Transient Voltage Fluctuations in FPGAs," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 26, no. 10, pp. 1817–1830, Oct. 2018.

[8] R. K. Henderson *et al.*, "A 192x128 Time Correlated SPAD Image Sensor in 40-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1907–1916, Jul. 2019.

[9] P. Lecoq, "Pushing the Limits in Time-of-Flight PET Imaging," *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 1, no. 6, pp. 473–485, Nov. 2017.

[10] H. Song, W. Choi, and H. Kim, "Robust Vision-Based Relative-Localization Approach Using an RGB-Depth Camera and LiDAR Sensor Fusion," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3725–3736, Jun. 2016.

[11] D. D.-U. Li *et al.*, "Video-rate fluorescence lifetime imaging camera with CMOS single-photon avalanche diode arrays and high-speed imaging algorithm," *J. Biomed. Opt.*, vol. 16, no. 9, p. 096012, Sep. 2011.

[12] Q. Shen *et al.*, "An FPGA-Based TDC for Free Space Quantum Key Distribution," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 5, pp. 3570–3577, Oct. 2013.

[13] F. M. D. Rocca *et al.*, "Real-time fluorescence lifetime actuation for cell sorting using a CMOS SPAD silicon photomultiplier," *Opt. Lett.*, vol. 41, no. 4, pp. 673–676, Feb. 2016.

[14] Intel, "Designing with Low-Level Primitives User Guide." Accessed: Sep. 03, 2020. [Online]. Available: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_low_level.pdf.

[15] Xilinx, "UltraScale Architecture Configurable Logic Block User Guide (UG574)." 2017, Accessed: Nov. 05, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug574-ultrascale-clb.pdf.

[16] J. Y. Won and J. S. Lee, "Time-to-Digital Converter Using a Tuned-Delay Line Evaluated in 28-, 40-, and 45-nm FPGAs," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 7, pp. 1678–1689, Jul. 2016.

[17] Z. Song, Y. Wang, and J. Kuang, "A 256-channel, high throughput and precision time-to-digital converter with a decomposition encoding scheme in a Kintex-7 FPGA," *J. Instrum.*, vol. 13, no. 05, pp. P05012–P05012, May 2018.

[18] H. Chen and D. D. Li, "Multichannel, Low Nonlinearity Time-to-Digital Converters Based on 20 and 28 nm FPGAs," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 3265–3274, Apr. 2019.

[19] Y. Wang and C. Liu, "A 3.9 ps Time-Interval RMS Precision Time-to-Digital Converter Using a Dual-Sampling Method in an UltraScale FPGA," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 5, pp. 2617–2621, Oct. 2016.

[20] Y. Wang, J. Kuang, C. Liu, and Q. Cao, "A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 10, pp. 2713–2718, Oct. 2017.

[21] Q. Shen *et al.*, "A 1.7 ps Equivalent Bin Size and 4.2 ps RMS FPGA TDC Based on Multichain Measurements Averaging Method," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 947–954, Jun. 2015.

[22] P. Chen, Y. Hsiao, Y. Chung, W. X. Tsai, and J. Lin, "A 2.5-ps Bin Size and 6.7-ps Resolution FPGA Time-to-Digital Converter Based on Delay Wrapping and Averaging," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 25, no. 1, pp. 114–124, Jan. 2017.

[23] J. Y. Won, S. I. Kwon, H. S. Yoon, G. B. Ko, J. Son, and J. S. Lee, "Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 231–242, Feb. 2016.

[24] T. Sui *et al.*, "A 2.3-ps RMS Resolution Time-to-Digital Converter Implemented in a Low-Cost Cyclone V FPGA," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 10, pp. 3647–3660, Oct. 2019.

[25] P. Kwiatkowski, "Employing FPGA DSP blocks for time-to-digital conversion," *Metrol. Meas. Syst.*, vol. 26, no. 4, pp. 631–643, Dec. 2019.

[26] X. Qin *et al.*, "A high resolution time-to-digital-convertor based on a carry-chain and DSP48E1 adders in a 28-nm field-programmable-gate-array," *Rev. Sci. Instrum.*, vol. 91, no. 2, p. 024708, Feb. 2020.

[27] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, no. 1, pp. 17–32, Dec. 2003.

[28] P. Kwiatkowski and R. Szplet, "Efficient implementation of multiple time coding lines-based TDC in an FPGA device," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7353–7364, Oct. 2020.

[29] W. Pan, G. Gong, and J. Li, "A 20-ps Time-to-Digital Converter (TDC) Implemented in Field-Programmable Gate Array (FPGA) with Automatic Temperature Correction," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 3, pp. 1468–1473, Jun. 2014.

[30] J. Wu, "Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 3, pp. 1543–1548, Jun. 2010.

[31] N. Dutton *et al.*, "Multiple-event direct to histogram TDC in 65nm FPGA technology," in *2014 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jun. 2014, pp. 1–5.

[32] H. Chen, Y. Zhang, and D. D. Li, "A Low Nonlinearity, Missing-Code Free Time-to-Digital Converter Based on 28-nm FPGAs With Embedded Bin-Width Calibrations," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 7, pp. 1912–1921, Jul. 2017.

[33] J. Wu and Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay," in *2008 IEEE Nuclear Science Symposium Conference Record*, Oct. 2008, pp. 3440–3446.
[34] J. Wu, "On-Chip processing for the wave union TDC implemented in FPGA," in *2009 16th IEEE-NPSS Real Time Conference*, May 2009, pp. 279–282.
[35] J. Wu, Y. Shi, and D. Zhu, "A low-power Wave Union TDC implemented in FPGA," *J. Instrum.*, vol. 7, no. 01, pp. C01021–C01021, Jan. 2012.
[36] S. Wang, J. Wu, S. Yao, and W. Chang, "A Field-Programmable Gate Array (FPGA) TDC for the Fermilab SeaQuest (E906) Experiment and Its Test with a Novel External Wave Union Launcher," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3592–3598, Dec. 2014.
[37] J. Qi, H. Gong, and Y. Liu, "On-Chip Real-Time Correction for a 20-ps Wave Union Time-To-Digital Converter (TDC) in a Field-Programmable Gate Array (FPGA)," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 1605–1610, Aug. 2012.
[38] R. Szplet, P. Kwiatkowski, Z. Jachna, and K. Rozyc, "Several issues on the use of independent coding lines for time-to-digital conversion," in *2013 IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC)*, Oct. 2013, pp. 1–8.
[39] N. Lusardi, F. Garzetti, and A. Geraci, "The role of sub-interpolation for Delay-Line Time-to-Digital Converters in FPGA devices," *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 916, pp. 204–214, Feb. 2019.
[40] C. Liu and Y. Wang, "A 128-Channel, 710 M Samples/Second, and Less Than 10 ps RMS Resolution Time-to-Digital Converter Implemented in a Kintex-7 FPGA," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 773–783, Jun. 2015.
[41] G. Cao, H. Xia, and N. Dong, "An 18-ps TDC using timing adjustment and bin realignment methods in a Cyclone-IV FPGA," *Rev. Sci. Instrum.*, vol. 89, no. 5, p. 054707, May 2018.
[42] Y. Wang and C. Liu, "A 4.2 ps Time-Interval RMS Resolution Time-to-Digital Converter Using a Bin Decimation Method in an UltraScale FPGA," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 5, pp. 2632–2638, Oct. 2016.
[43] Y.-H. Chen, "Time Resolution Improvement Using Dual Delay Lines for Field-Programmable-Gate-Array-Based Time-to-Digital Converters with Real-Time Calibration," *Appl. Sci.*, vol. 9, no. 1, p. 20, Jan. 2019.
[44] Y. Wang, X. Zhou, Z. Song, J. Kuang, and Q. Cao, "A 3.0-ps rms Precision 277-MSamples/s Throughput Time-to-Digital Converter Using Multi-Edge Encoding Scheme in a Kintex-7 FPGA," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 10, pp. 2275–2281, Oct. 2019.
[45] R. Szplet, J. Kalisz, and Z. Jachna, "A 45 ps time digitizer with a two-phase clock and dual-edge two-stage interpolation in a field programmable gate array device," *Meas. Sci. Technol.*, vol. 20, no. 2, p. 025108, Jan. 2009.
[46] R. Szplet, P. Kwiatkowski, Z. Jachna, and K. Różyc, "An Eight-Channel 4.5-ps Precision Timestamps-Based Time Interval Counter in FPGA Chip," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 9, pp. 2088–2100, Sep. 2016.
[47] J. Wu, "Uneven bin width digitization and a timing calibration method using cascaded PLL," in *2014 19th IEEE-NPSS Real Time Conference*, May 2014, pp. 1–4.
[48] R. Szymanowski, R. Szplet, and P. Kwiatkowski, "Quantization error in precision time counters," *Meas. Sci. Technol.*, vol. 26, no. 7, p. 075002, Jun. 2015.
[49] A. Balla *et al.*, "The characterization and application of a low resource FPGA-based time to digital converter," *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 739, pp. 75–82, Mar. 2014.
[50] R. Szplet, R. Szymanowski, and D. Sondej, "Measurement Uncertainty of Precise Interpolating Time Counters," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 11, pp. 4348–4356, Nov. 2019.
[51] B. I. Abdulrazzaq, I. Abdul Halin, S. Kawahito, R. M. Sidek, S. Shafie, and N. A. Md. Yunus, "A review on high-resolution CMOS delay lines: towards sub-picosecond jitter performance," *SpringerPlus*, vol. 5, no. 1, p. 434, Apr. 2016.
[52] N. Lusardi, F. Garzetti, N. Corna, R. D. Marco, and A. Geraci, "Very High-Performance 24-Channels Time-to-Digital Converter in Xilinx 20-nm Kintex UltraScale FPGA," in *2019 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Oct. 2019, pp. 1–4.
[53] X. Qin, L. Wang, D. Liu, Y. Zhao, X. Rong, and J. Du, "A 1.15-ps Bin Size and 3.5-ps Single-Shot Precision Time-to-Digital Converter With On-Board Offset Correction in an FPGA," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 12, pp. 2951–2957, Dec. 2017.
[54] N. Lusardi, F. Garzetti, and A. Geraci, "Digital instrument with configurable hardware and firmware for multi-channel time measures," *Rev Sci Instrum*, vol. 90, no. 5, p. 14, May 2019.
[55] R. Szplet, D. Sondej, and G. Grzęda, "High-Precision Time Digitizer Based on Multiedge Coding in Independent Coding Lines," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 8, pp. 1884–1894, Aug. 2016.
[56] M. Zhang, H. Wang, and Y. Liu, "A 7.4 ps FPGA-Based TDC with a 1024-Unit Measurement Matrix," *Sensors*, vol. 17, no. 4, p. 865, Apr. 2017.
[57] K. Cui and X. Li, "A High-Linearity Vernier Time-to-Digital Converter on FPGAs With Improved Resolution Using Bidirectional-Operating Vernier Delay Lines," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 8, pp. 5941–5949, Aug. 2020.
[58] K. Choi and D. Jee, "Design and Calibration Techniques for a Multichannel FPGA-Based Time-to-Digital Converter in an Object Positioning System," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–9, 2021.
[59] M. Zhang, K. Yang, Z. Chai, H. Wang, Z. Ding, and W. Bao, "High-Resolution Time-to-Digital Converters Implemented on 40-, 28-, and 20-nm FPGAs," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–10, 2021.

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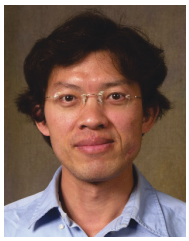

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