# FPGA Implementation of a Novel Oversampling DeadBeat Controller for PMSM Drives

***Abstract*—This paper presents a novel Oversampling DeadBeat (OS-DB) current control approach for Permanent Magnet Synchronous Motors (PMSMs) drives capable of operating at a controller sampling frequency multiple of the power converter switching frequency. Model based controllers suffer form heavy computational demand and performance degradation due to parameters uncertainties. The proposed controller concurrently with FPGA implementation permits to achieve a constant switching frequency and an optimal current ripple along with a high current loop bandwidth and robust behaviour to parameters variation. A disturbance observer has been added to the proposed controller in order to compensate for the converter voltage distortions. The proposed control strategy is tested through both simulations and experiments.**

***Index Terms*—DeadBeat Control, Model Predictive Control, Oversampling, Permanent Magnet Synchronous Motors.**

## I. Introduction

In the field of variable-speed AC drives PMSMs, compared to other motor types like induction motors, offer several advantages. They have higher efficiency, higher performance, compact construction and higher torque per volume ratio. High performance electrical drives require efficient inner current control loops due to the intrinsic relationship between current quality response and torque control. Among the controllers which can achieve high current loop bandwidth there are Predictive Controllers [1]. Of particular interest because of its dynamic performances is the DeadBeat (DB) control which is able to force the control error to zero in a short finite time resulting in a fast transient response. Compared to other predictive control approaches like Finite Control Set Model Predictive Controller (FCS-MPC), DB combines good dynamic performance with a constant switching frequency. FCS-MPC in fact, do not utilise a modulator leading to variable switching frequency and, often, to a suboptimal current ripple [2], [3]. Because of these reasons the DB controller has been chosen over other controllers in many applications such as uninterruptible power supply (UPS) [4], [5], PWM rectifiers, active filters control [6] and motor drive control [7]–[10]. When the MPCs are implemented in a full digital system it is well-known that one of their main limitations is their complex implementation [1] which often leads to an inevitable delay between measurements and control action to the inverter. For the DB controller this results in doubling the time necessary to bring to zero the current error. In one controller sample time it is necessary to measure, calculate and actuate the control actions, which is often not possible for standard DSP digital controllers, leading to the introduction of the sample time delay compensation. However, increasing the processing speed by using specific digital hardware technology such as field programmable gate arrays (FPGA) allows to significantly reduce the calculation time and enabling to measure, compute and actuate in a single controller sample time. The advantages of FPGA-based MPC have been investigated in [11]–[14]. The implementation of the standard DB controller on a FPGA controller can be found in [15], [16]. The other main limitation of predictive controllers as well as DB controllers is the strong dependency of their performances from model parameters. Machine parameters deviations from nominal ones or simply lack of knowledge of their values, results in a significant reduction of both transient and steady state performances as reported in [2], [6], [8], [17]–[19]. The DB controller performances are deteriorated not only by parameters uncertainties but also from the converter voltage non-linearities such as the dead times (DT), voltage drops and unideal turn-on and turn-off of the devices. Previous work has been done combining the DB controller with a standard PI to reduce the performance deterioration due to voltage non-linearities and parameters mismatches [7], while in [5] the control sensitivity from model uncertainties is reduced by introducing a disturbance observer for the DB controller.

This paper investigates a new DB approach in order to operate at an increased controller sampling frequency without increasing the commutation frequency of the power converter. The proposed OS-DB controller is obtained by discretizing the system equations over a variable sample time $T_s(i)$ resulting in an increased control sampling frequency. Although the proposed oversampling approach increase the robustness to machine parameters variation, on the other hand it introduces a distortion in the control voltages fed into the PWM. To eliminate this behaviour a compensation strategy has been developed and successfully validated. Furthermore, a reduced order Luenberger disturbance observer has been added to OS-DB controller to remove steady-state errors due to inverter non-linearities and parameters mismatch. The whole controller has been implemented in FPGA in order to increase the transient performances and avoid the step delay compensation. The proposed technique permits to achieve a constant switching frequency and an optimal current ripple along with a high current loop bandwidth and robust behaviour to parameter variation. The paper is organized as follows: in Section II PMSM model is presented. Section III presents the standard DBCC for a PMSM. Sections IV and IV-A illustrate the new variable sample time OS-DB while the disturbance observer is presented in Section V. Simulation and experimetal results are shown in Section VI and VII respectively. Finally, Section VIII reports the conclusions.

## II. PMSM Mathematical Model

The considered electrical system is a 3-phase, p-pole, wye-connected permanent magnet synchronous machine [20]. The

stator windings are identical sinusoidally distributed windings, displaced of 120° with resistance $R_s$. The magnetic axes of the stator windings are denoted by the $as$, $bs$ and $cs$ axes. The machine voltage and flux equations in the abc reference frame are reported in matrix form in (1)

$$\begin{cases} V_{abc} = RI_{abc} + \dot{\lambda}_{abc} \\ \lambda_{abc} = L_{abc}I_{abc} + \Lambda_r \end{cases} \tag{1}$$

where $V_{abc}$, $I_{abc}$, $\lambda_{abc}$ and $\Lambda_r$ are the stator phase voltages, phase currents, stator fluxes and the rotor permanent magnets flux linkage with the stator windings. R is a diagonal matrix with $R_s$ on the diagonal, $L_{abc}$ and $\Lambda_r$ are reported in (2) and (3) respectively. $\lambda_m$ is the peak flux linkage established by the rotor permanent magnets.

$\theta$ is the rotor angular position of the machine measured as the displacement of the quadrature axis (q) from the magnetic axis of phase $as$. The direct axis (d) is lagging of 90° behind the q axis. Transforming the machine phase voltages equations and the stator fluxes of (2) on the rotor synchronous reference frame the following system is obtained:

$$\begin{cases} V_q = R_s i_q + \omega\lambda_d + \dot{\lambda}_q \\ V_d = R_s i_d - \omega\lambda_q + \dot{\lambda}_d \\ \lambda_q = L_q i_q \\ \lambda_d = L_d i_d + \lambda_m \end{cases} \tag{4}$$

where $\omega$ is the machine electrical speed, $L_q$ and $L_d$ are the q and d axes inductances respectively. The relationship between $L_A$, $L_B$ and the machine's inductances $L_q$ and $L_d$ in the synchronous reference frame is reported in (5).

$$L_A = \frac{L_d + L_q}{3};\ L_B = \frac{L_d - L_q}{3} \tag{5}$$

In order to digitally implement the model based controller, the discretization of the plant equations is necessary. Firstly the system (4) is written in the standard state space form as

$$\begin{bmatrix} \dot{i}_q \\ \dot{i}_d \end{bmatrix} = A \begin{bmatrix} i_q \\ i_d \end{bmatrix} + B \begin{bmatrix} V_q \\ V_d \end{bmatrix} + \begin{bmatrix} -\dfrac{\omega\lambda_m}{L_q} \\ 0 \end{bmatrix} \tag{6}$$

where

$$A = \begin{bmatrix} -\dfrac{R_s}{L_q} & -\dfrac{L_d\,\omega}{L_q} \\ \dfrac{L_q\,\omega}{L_d} & -\dfrac{R_s}{L_d} \end{bmatrix} B = \begin{bmatrix} \dfrac{1}{L_q} & 0 \\ 0 & \dfrac{1}{L_d} \end{bmatrix}$$

The discretized state-space form of the plant (6) around a generic time instant k is presented in (7).

$$\begin{bmatrix} i^q_{k+1} \\ i^d_{k+1} \end{bmatrix} = \Phi \begin{bmatrix} i^q_k \\ i^d_k \end{bmatrix} + \Gamma \begin{bmatrix} V^q_k \\ V^d_k \end{bmatrix} + \begin{bmatrix} -\dfrac{\omega_k\lambda_m}{L_q} \\ 0 \end{bmatrix} \tag{7}$$

where

$$\Phi = e^{AT_s};\quad \Gamma = \int_0^{T_s} e^{A\tau}d\tau$$

Considering the Taylor expansion of $\Phi$ and $\Gamma$ and ignoring the quadratic and higher-order terms the final matrices of the PMSM state-space model used to synthesize the controller are obtained

$$\Phi = \begin{bmatrix} 1 - \dfrac{R_s T_s}{L_q} & -\dfrac{\omega_k L_d T_s}{L_q} \\ \dfrac{\omega_k L_q T_s}{L_d} & 1 - \dfrac{R_s T_s}{L_d} \end{bmatrix} \Gamma = \begin{bmatrix} \dfrac{T_s}{L_q} & 0 \\ 0 & \dfrac{T_s}{L_d} \end{bmatrix} \tag{8}$$

## III. Standard Dead-Beat Control

The standard Dead-Beat control can be obtained from the discretized plant equations (7) and (8). By substituting the desired q, d current references to the $i^q_{k+1}$ and $i^d_{k+1}$ terms and solving for the voltages $V^q_k$ and $V^d_k$

$$\begin{bmatrix} V^q_k \\ V^d_k \end{bmatrix} = \Gamma^{-1}\left\{ \begin{bmatrix} i^{qRef}_{k+1} \\ i^{dRef}_{k+1} \end{bmatrix} - \Phi \begin{bmatrix} i^q_k \\ i^d_k \end{bmatrix} - \begin{bmatrix} -\dfrac{\omega_k\lambda_m}{L_q} \\ 0 \end{bmatrix} \right\} \tag{9}$$

Note that the reference value $i^{Ref}_{k+1}$ is needed, but can be assumed to be equal to $i^{Ref}_k$ since $T_s$ is sufficiently small compared with the time constant of the system. Therefore the reference can be considered constant over $T_s$. The q, d voltage control actions calculated in (9) are the one that, if no saturation occurs, permit to reach the current references in one sample time $T_s$. The digital implementation of the standard DB control is possible only if the control action calculation time is negligible respect to the system sample time. Often this condition is not satisfied for standard microcontroller implementations leading to the necessity of taking into account one sample time delay as explained in [1]. The delay can be neglected in a real-time application only if the computational time is significantly reduced to be negligible compared to $T_s$.

$$L_{abc} = \begin{bmatrix} L_{ls} + L_A - L_B cos(2\theta) & -\frac{1}{2}L_A - L_B cos2(\theta - \frac{\pi}{3}) & -\frac{1}{2}L_A - L_B cos2(\theta + \frac{\pi}{3}) \\ -\frac{1}{2}L_A - L_B cos2(\theta - \frac{\pi}{3}) & L_{ls} + L_A - L_B cos2(\theta - \frac{2\pi}{3}) & -\frac{1}{2}L_A - L_B cos2(\theta + \pi) \\ -\frac{1}{2}L_A - L_B cos2(\theta + \frac{\pi}{3}) & -\frac{1}{2}L_A - L_B cos2(\theta + \pi) & L_{ls} + L_A - L_B cos2(\theta + \frac{2\pi}{3}) \end{bmatrix} \tag{2}$$

$$\Lambda_r = \lambda_m \begin{bmatrix} sin(\theta) & sin(\theta - \frac{\pi}{3}) & sin(\theta + \frac{\pi}{3}) \end{bmatrix} \tag{3}$$

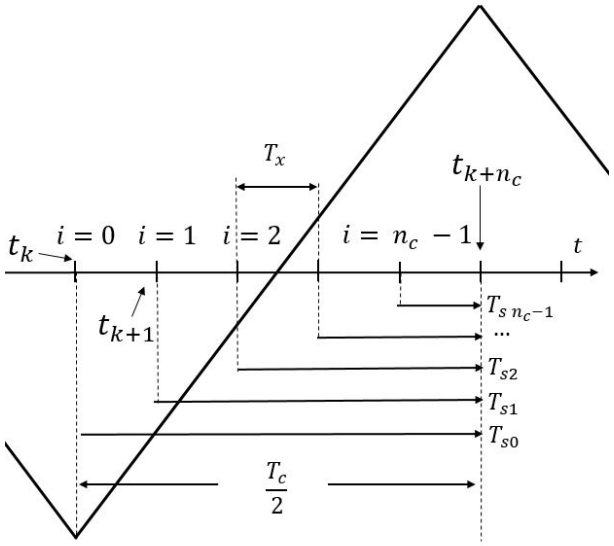


Fig. 1. Carrier and variable sample time for the OS-DB.

## IV. Oversampling Dead-Beat Control

The new DB approach here proposed operates at an increased controller sampling frequency without increasing the commutation frequency of the power converter. Referring to Fig. 1, $T_x$ is the controller sampling period while $T_c$ is the modulator carrier period. In order to increase the controller sampling time $T_x$ without changing the switching frequency (i.e. the modulator carrier frequency) some consideration should be done. If the control approach described earlier is simply implemented to a higher frequency, the system becomes quickly unstable as the ratio $\frac{T_x}{T_c}$ decreases due to the interaction with the modulator. The control voltages (9) in fact, are optimal only if they are equal to the inverter output voltages averaged on a $T_x$ period. Using a modulator however, this is guaranteed only on a carrier semi-period, i.e. $\frac{T_c}{2}$. The oversampling coefficient $n_c$ is defined as

$$n_c = \frac{T_c}{2T_x} \tag{10}$$

Fig. 1 shows a variable sample time $T_s(i)$ that depends on the oversampling coefficient $n_c$ and the modulator triangular carrier period and it is defined as

$$T_s(i) = \frac{T_c}{2} - iT_x = (n_c - i)T_x \tag{11}$$

where $i = 0, 1, 2, ..., n_c - 1$ and it is reset to 0 every $\frac{T_c}{2}$, i.e. at the end of each carrier segment. In order to take into account the variable sample time of the controller, (11) can be substituted to the discretized plant equations (7) and (8) to obtain

$$\begin{bmatrix} i^q_{k+n_c} \\ i^d_{k+n_c} \end{bmatrix} = \Phi_{T_s(i)} \begin{bmatrix} i^q_{k+i} \\ i^d_{k+i} \end{bmatrix} + \Gamma_{T_s(i)} \begin{bmatrix} V^q_{k+i} \\ V^d_{k+i} \end{bmatrix} + \begin{bmatrix} -\frac{\omega_{k+i}\lambda_m}{L_q} \\ 0 \end{bmatrix} \tag{12}$$

The matrices $\Phi_{T_s(i)}$ and $\Gamma_{T_s(i)}$ are identical to (8) where $T_s$ has been substituted with (11). Please observe that the time subscript $k$ of (12), according to Fig. 1, increases every $T_x$ by 1 according to the new oversampling coefficient $n_c$ . The DB-OS controller output voltages are obtained from (12) resolving for $V^q_{k+i}$ and $V^d_{k+i}$

$$\begin{bmatrix} V^q_{k+i} \\ V^d_{k+i} \end{bmatrix} = \Gamma^{-1}_{T_s(i)} \left\{ \begin{bmatrix} i^q_{k+n_c} \\ i^d_{k+n_c} \end{bmatrix} - \Phi_{T_s(i)} \begin{bmatrix} i^q_{k+i} \\ i^d_{k+i} \end{bmatrix} - \begin{bmatrix} -\frac{\omega_{k+i}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right\} \tag{13}$$

Therefore the controller voltages $k + n_c$ are calculated $n_c$ times, where each time the sample time is reduced by $T_x$. As already mentioned, one of the main problems of predictive controllers is the strong dependence by the model parameters. In fact, in real applications, both the stator resistance and inductance can vary causing a significant degradation in the DB controller performances. The oversampled technique investigated allows to compute the controller equations with higher frequency therefore reducing the effect of incorrect predictions due to parameters variation from the rated ones.

### A. Voltage distortion compensation

It can be seen in Section III the standard DB current loop controller is able to achieve one sample time dynamic response to a variation in current references if no variation of the PMSM parameters has happened. In the OS-DB controller voltages are computed every $\frac{T_c}{2n_c}$ with a reducing sample time. For a standard controller that operates at a frequency equal or double the converter switching frequency, it is true that the controller voltage computed will be equal to the average voltage applied by the converter over a sample time. Instantaneously, this relationship is not true, in fact due to their intrinsic discrete nature, power converters are able to output only a finite number of the voltage. For a standard three phase two level Voltage Source Converter (2L-VSI) the phase voltages can be equal to $\frac{V_d c}{2}$ or $\frac{-V_d c}{2}$ and they are modulated according to PWM principle to achieve, on average, the reference voltage. OS-DB controller runs $n_c$ times over half of a carrier period. It means that the reference voltage generated cannot be applied, not even on average, in a single controller sample time $T_x$. For this reason, a compensation term must be added to (13).

According to the PMSM model the qd currents at the time instant $k + i$ can be predicted from the previous time instant $k + i - 1$ as

$$\begin{bmatrix} i^q_{k+i} \\ i^d_{k+i} \end{bmatrix} = \Phi_{T_x} \begin{bmatrix} i^q_{k+i-1} \\ i^d_{k+i-1} \end{bmatrix} + \Gamma_{T_x} \begin{bmatrix} V^{qC}_{k+i-1} \\ V^{dC}_{k+i-1} \end{bmatrix} + \begin{bmatrix} -\frac{\omega_{k+i-1}\lambda_m}{L_q} \\ 0 \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} i^q_{k+i} \\ i^d_{k+i} \end{bmatrix} = \Phi_{T_x} \begin{bmatrix} i^q_{k+i-1} \\ i^d_{k+i-1} \end{bmatrix} + \Gamma_{T_x} \begin{bmatrix} V^{qR}_{k+i-1} \\ V^{dR}_{k+i-1} \end{bmatrix} + \begin{bmatrix} -\dfrac{\omega_{k+i-1}\lambda_m}{L_q} \\ 0 \end{bmatrix} \tag{15}$$

where the PMSM matrices $\Phi_{T_x}$ and $\Gamma_{T_x}$ correspond to (8), but discretized over a time $T_x$. Equations (14) and (15) predict motor currents at time instant $k+i$ assuming at the previous sample time $k+i-1$ has been applied the controller voltage $V^C_{k+i-1}$ or the real voltage $V^R_{k+i-1}$ respectively. By replacing (14) and (15) in (13) the controller voltages at the time instant $k+i$ in dependence of $V^C_{k+i-1}$ and $V^R_{k+i-1}$ are obtained as in (18) and (19).

A compensation terms for both q and d axis can be computed subtracting (19) to (18)

$$\begin{bmatrix} V^q_{c_{k+i}} \\ V^d_{c_{k+i}} \end{bmatrix} = \begin{bmatrix} \dfrac{R_s T_x}{L_q} + \dfrac{1}{i-n_c} & w_{k+i}T_x \\ -w_{k+i}T_x & \dfrac{R_s T_x}{L_d} + \dfrac{1}{i-n_c} \end{bmatrix} \begin{bmatrix} V^{qC}_{k+i-1} - V^{qR}_{k+i-1} \\ V^{dC}_{k+i-1} - V^{dR}_{k+i-1} \end{bmatrix} \tag{16}$$

The final equations of the OS-DB controller are the following

$$\begin{bmatrix} V^q_{k+i} \\ V^d_{k+i} \end{bmatrix} = \Gamma^{-1}_{T_s(i)} \left\{ \begin{bmatrix} i^q_{k+n_c} \\ i^d_{k+n_c} \end{bmatrix} - \Phi_{T_s(i)} \begin{bmatrix} i^q_{k+i} \\ i^d_{k+i} \end{bmatrix} - \begin{bmatrix} -\dfrac{\omega_{k+i}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right\} + \begin{bmatrix} V^q_{c_{k+i}} \\ V^d_{c_{k+i}} \end{bmatrix} \tag{17}$$

### *B. Real Voltages Calculation and OS-DB Controller Implementation*

As it can be seen from (16) in order to compute the compensation terms for the OS-DB it is necessary to know both the controller and real voltages applied at the previous time instant. The controller voltages $V^C_{k+i-1}$ can be stored in memory in order to be used at the actual time instant while the real voltages $V^R_{k+i-1}$ applied by the converter need to be computed. Fig. 2 shows the standard Pulse Width Modulation (PWM) for a generic phase $j$ and the correspondent converter leg voltage. The knowledge of the carrier and the phase reference signal are enough to calculate the phase voltage. Knowing the time instant $t_{sw}$ at which the modulating voltage crosses with the carrier the average voltage applied by the converter can be calculated as follows

$$\bar{V_j} = \frac{V_{dc}}{2}\frac{t_{sw}}{T_s} - \frac{V_{dc}}{2}\left(1 - \frac{t_{sw}}{T_s}\right) \tag{20}$$

TABLE I
MODEL PARAMETERS.

| | | | |
|---|---|---|---|
| $L_q$ | 4.1 [mH] | $L_d$ | 2.58 [mH] |
| $R_s$ | 1.35 [Ω] | $p$ | 4 [-] |
| $J_m$ | 31.685 [g m$^2$] | $\omega_m rated$ | 150 [$\frac{rad}{s}$] |
| $V_{dc}$ | 300 [V] | $DT$ | 2.2 [$\mu s$] |
| $f_{sw}$ | 10 [KHz] | $T_c$ | 100 [$\mu s$] |
| $T_x$ | 10 [$\mu s$] | $n_c$ | 5 [$-$] |

## V. DISTURBANCE OBSERVER

The performances of the DB control such as the dynamic behaviour and steady state offset are strongly dependant on the knowledge of the plant model and its parameters. Any mismatch in the modelization of the plant or uncertainty in the parameter will lead to a deterioration of the performances. It can be noticed from (9) and (17) that both for the DB and for the OS-DB control there is no integral action. Therefore any uncertainty in the stator resistance, flux established by the rotor permanent magnets, inverter non-linearities and influence of external disturbances would lead to a current steady state offset. To avoid this problem a reduced order estimator for the voltage disturbances has been modelled and implemented. The overall control block diagram with the reduced order Luenberger disturbance estimator is shown in Fig. 3. Assuming the disturbances as constants the continuous estimator equations are

$$\begin{cases} \begin{bmatrix} \dot{V}_{d_q} \\ \dot{V}_{d_d} \end{bmatrix} = A_d \begin{bmatrix} V_{d_q} \\ V_{d_d} \end{bmatrix} \\ \begin{bmatrix} w_q \\ w_d \end{bmatrix} = H_d \begin{bmatrix} V_{d_q} \\ V_{d_d} \end{bmatrix} \end{cases} \tag{21}$$

where

$$A_d = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}; \quad H_d = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$\begin{bmatrix} V^{qC}_{k+i} \\ V^{dC}_{k+i} \end{bmatrix} = \Gamma^{-1}_{T_s(i)} \left\{ \begin{bmatrix} i^q_{k+n_c} \\ i^d_{k+n_c} \end{bmatrix} - \Phi_{T_s(i)} \left[ \Phi_{T_x} \begin{bmatrix} i^q_{k+i-1} \\ i^d_{k+i-1} \end{bmatrix} + \Gamma_{T_x} \begin{bmatrix} V^{qC}_{k+i-1} \\ V^{dC}_{k+i-1} \end{bmatrix} + \begin{bmatrix} -\dfrac{\omega_{ek+i-1}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right] - \begin{bmatrix} -\dfrac{\omega_{ek+i}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right\} \tag{18}$$

$$\begin{bmatrix} V^{qR}_{k+i} \\ V^{dR}_{k+i} \end{bmatrix} = \Gamma^{-1}_{T_s(i)} \left\{ \begin{bmatrix} i^q_{k+n_c} \\ i^d_{k+n_c} \end{bmatrix} - \Phi_{T_s(i)} \left[ \Phi_{T_x} \begin{bmatrix} i^q_{k+i-1} \\ i^d_{k+i-1} \end{bmatrix} + \Gamma_{T_x} \begin{bmatrix} V^{qR}_{k+i-1} \\ V^{dR}_{k+i-1} \end{bmatrix} + \begin{bmatrix} -\dfrac{\omega_{ek+i-1}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right] - \begin{bmatrix} -\dfrac{\omega_{ek+i}\lambda_m}{L_q} \\ 0 \end{bmatrix} \right\} \tag{19}$$

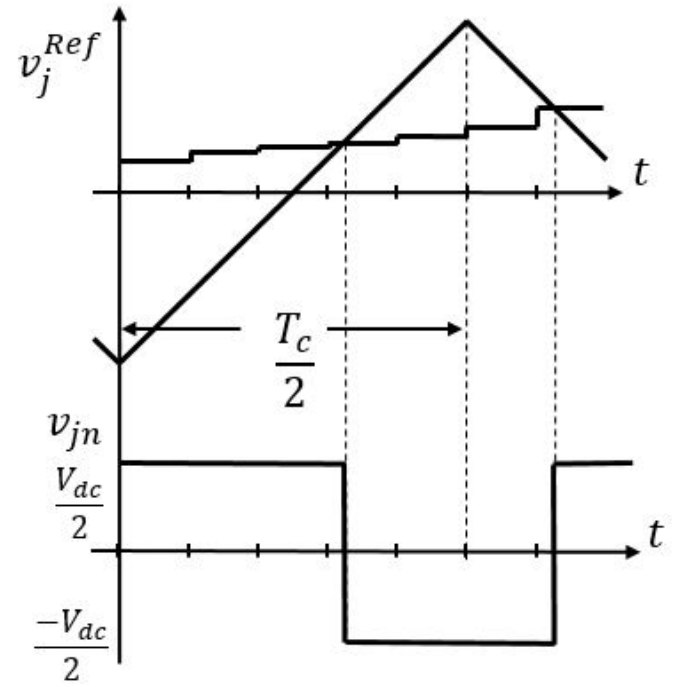


Fig. 2. PWM and phase leg voltage.

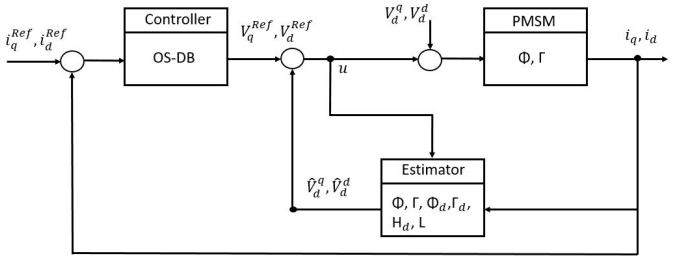


Fig. 3. Block scheme of the complete control structure.

and where $V_{d_q}$ and $V_{d_d}$ are the voltage disturbances. The discrete state space form of the disturbance equations are

$$\begin{bmatrix} V^q_{d_{k+1}} \\ V^d_{d_{k+1}} \end{bmatrix} = \Phi_d \begin{bmatrix} V^q_{d_k} \\ V^d_{d_k} \end{bmatrix} \tag{22}$$

where

$$\Phi_d = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

The plant discretized model in the state space form considering the voltage disturbances are

$$\begin{bmatrix} i^q_{k+1} \\ i^d_{k+1} \end{bmatrix} = \Phi \begin{bmatrix} i^q_k \\ i^d_k \end{bmatrix} + \Gamma \begin{bmatrix} V^q_k \\ V^d_k \end{bmatrix} + \begin{bmatrix} -\frac{\omega_k \lambda_m}{L_q} \\ 0 \end{bmatrix} + \Gamma_d \begin{bmatrix} V^q_{d_k} \\ V^d_{d_k} \end{bmatrix} \tag{23}$$

where

$$\Gamma_d = \begin{bmatrix} -\frac{T_s}{L_q} & 0 \\ 0 & -\frac{T_s}{L_d} \end{bmatrix}$$

The state of the plant is augmented by two by taking into account the disturbances as follows

$$\begin{cases} x_{k+1} = \begin{bmatrix} \Phi & \Gamma_d H_d \\ 0 & \Phi_d \end{bmatrix} x_k + \begin{bmatrix} \Gamma \\ 0 \end{bmatrix} u_k \\ \begin{bmatrix} i^q_k \\ i^d_k \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} x_k \end{cases} \tag{24}$$

where

$$x_k = \begin{bmatrix} i^q_k & i^d_k & V^q_{d_k} & V^d_{d_k} \end{bmatrix}^T; \quad u_k = \begin{bmatrix} V^q_k & V^q_k \end{bmatrix}^T$$

Finally the reduced order Luenberger estimator has been implemented for the augmented state plant equations (24) obtaining

$$\begin{aligned} \begin{bmatrix} \hat{V}^q_{d_k} \\ \hat{V}^d_{d_k} \end{bmatrix} &= \left(\Phi_d - L_r \Gamma_d H_d\right) \begin{bmatrix} \hat{V}^q_{d_{k-1}} \\ \hat{V}^d_{d_{k-1}} \end{bmatrix} \\ &+ L_r \left( \begin{bmatrix} i^q_k \\ i^d_k \end{bmatrix} - \Phi \begin{bmatrix} i^q_{k-1} \\ i^d_{k-1} \end{bmatrix} - \Gamma u_{k-1} \right) \end{aligned} \tag{25}$$

where $L_r$ is a 2x2 matrix representing the Luenberger gain which has to be calculated in order to obtain the desired estimator dynamic.

## VI. Simulations Results

The proposed method has been firstly analyzed in simulation using Matlab-Simulink and the Xilinx System Generator toolbox in order to test the FPGA code in closed loop with the entire system. The overall control structure implemented is presented in Fig. 3. The OS-DB block implements the controller described in Section IV and IV-A while the estimator block implements the equations described in Section V. The proposed OS-DB controller is not affected by the control strategy used to regulate the motor speed. Therefore, for clarity and simplicity, a standard proportional integral (PI) controller has been used for the speed loop. Furthermore since the focus of this work are the current loop performances, no current profiling technique like Maximum Torque Per Ampere (MTPA) has been implemented and the torque is generated using only $i_q$, while $i_d$ is controlled to zero. As reported in [21] the recursive least square method has been used to estimate both the electrical and mechanical parameters of the motor. The parameters used to simulate the model correspond to the real ones and are reported in Table I. The proposed oversampled predictive controller measures and computes every $T_x$ but actuates only once every $\frac{T_c}{2}$. Considering a PMSM drive with controller sample time of $50\mu s$, converter switching frequency of $10KHz$ and an oversampling coefficient $n_c$ of 5 then the sampling period $T_x$ of the OS-DB controller is $10\mu s$.

Firstly the performances of the OS-DB controller are compared with the standard DB controller when no parameter variation occurs. Fig. 4 shows the dynamic behaviour in response

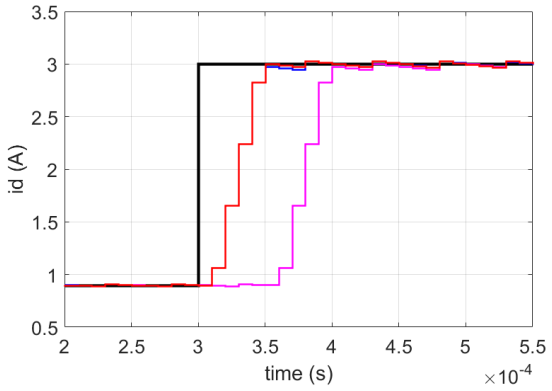


Fig. 4. System response to a reference $i_d$ step from 0.9 to 3 A. reference current $i_d$ (black line), DSP DB $i_d$ (magenta line), FPGA DB $i_d$ (blue line), OS-DB $i_d$ (red line).

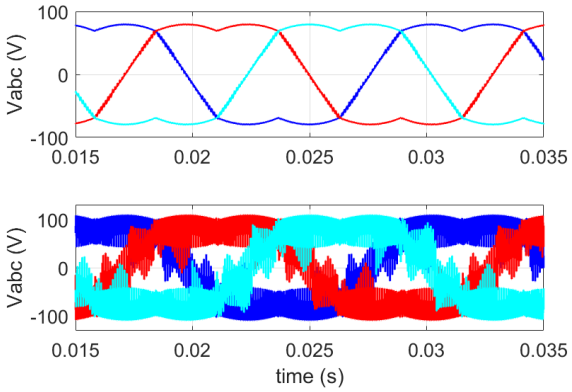


Fig. 5. OS-DB voltage references. Top panel: compensated OS-DB. Bottom Panel: uncompensated OS-DB.

to a $i_d$ step from 0.9 to 3 A at standstill of three different controllers: the standard DB controller implemented in DSP (with the step delay compensation), the FPGA implemented DB and the OS-DB, also FPGA implemented. It can be noticed how the DSP DB controller response is one sampling time $50\mu s$ slower compared to the other controllers. The ideal current response with only one sample time delay is achieved for both the FPGA DB and for the new proposed OS-DB controller (superimposed red and blue lines in Fig. 4). Since intrinsically the performances of the DSP implemented DB are inferior to the other controllers, it will not anymore be considered in the following. The voltage reference distortion introduced by the uncompensated OS-DB and the dynamic performances degradation are shown in Fig. 5 and Fig. 6 respectively. It is evident how the introduced compensation result to be necessary if low distortion and fast transient response want to be achieved. The main advantage of the proposed controller is the ability to achieve better transient performances when a machine parameter variation happens. The transient and steady state performances are evaluated for an $L_d$ reduction and increment from the rated parameter of 50%. Fig. 7 shows how the OS-DB maintains the same transient performances even when a significant parameter variation occurs. Fig. 8 shows instead how the phase current profile remains unchanged when the controller operates with and without parameter variation. It is clear how the proposed controller significantly improves the transient response under parameters uncertainties while not degrading the steady state behaviour. In Section VII a more in depth analysis of the controller performances under different working conditions is carried out.

## VII. Experimental Results

The proposed method has been finally tested on an experimental set-up composed by a PMSM coupled with a DC motor as shown in Fig. 9. The PMSM is fed by a two level IGBT converter while the control board specification can be found in [22]. The overall control performances have been tested under different operating conditions for two cases: rated parameters and parameters variation.

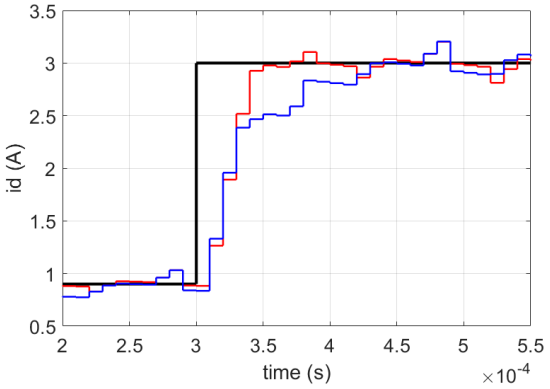


Fig. 6. OS-DB response to a reference $i_d$ step from 0.9 to 3 A. Reference current $i_d$ (black line), uncompensated OS-DB $i_d$ (blue line), compensated OS-DB $i_d$ (red line).

### A. Rated Parameters

When the OS-DB predictive controller parameters coincide with the PMSM ones it can be referred to as the rated parameter case. Fig. 10 shows how the same performances expected in simulation are obtained on the experimental set-up for an $i_d$ step from 0.9 to 3 A at standstill. The transient response of the OS-DB is equivalent to the one of the FPGA implemented DB. Fig. 11 shows the same $i_d$ transient comparison of performances of the DB FPGA implemented and the OS-DB at a mechanical speed $\omega_m$ of 150 $\frac{rad}{s}$. The controller performances on the quadrature axis are evaluated controlling the speed with the load dc motor and asking for an $i_q$ step on the PMSM. Fig. 12 shows a $i_q$ step from 0.9 to 3 A at $\omega_m$ of 130 $\frac{rad}{s}$.

### B. Parameters Variation

As already mentioned the main problem of predictive controllers is the strong dependency of the controller from the model parameters. In order to verify the robustness of the proposed controller to parameters uncertainties an experimental analysis has been carried out. In a real application both the stator resistance and the inductance can vary. The first

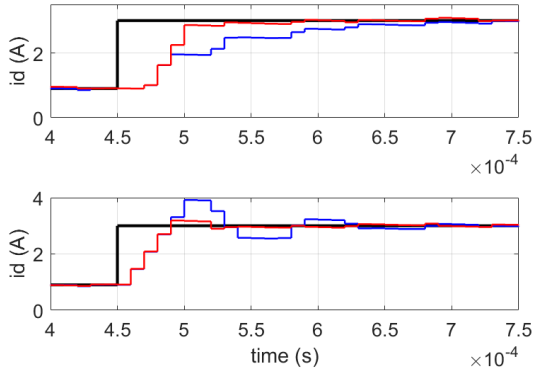


Fig. 7. OS-DB $i_d$ step from 0.9 to 3 A at $\omega_m$ 50 $\frac{rad}{s}$ . Top panel: 50% $L_d$ increment. Reference current $i_d$ (black line), DB FPGA implemented $i_d$ (blue line), OS-DB $i_d$ (red line). Bottom Panel: 50% $L_d$ reduction. Reference current $i_d$ (black line), DB FPGA implemented $i_d$ (blue line), OS-DB $i_d$ (red line).

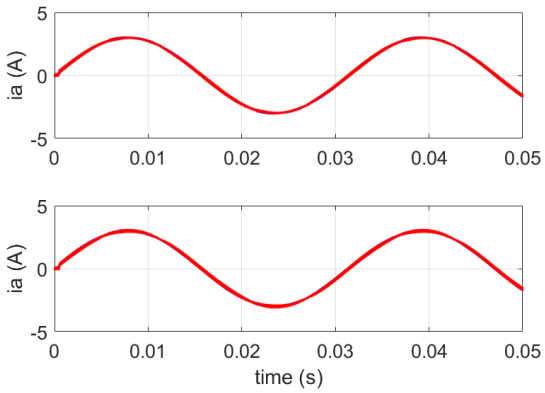


Fig. 8. OS-DB phase current steady state performances at $\omega_m$ 50 $\frac{rad}{s}$. Top panel: 50% $L_d$ increment. DB FPGA implemented $i_a$ (blue line), OS-DB $i_a$ (red line). Bottom Panel: 50% $L_d$ reduction. DB FPGA implemented $i_a$ (blue line), OS-DB $i_a$ (red line).

one is mainly affected by temperature with an uncertainty up to 30% while the latter can change due to ferromagnetic saturation. Variation in stator resistance or flux established by the permanent magnets mainly affects the steady state performances of the controller but since a disturbance observer has been implemented any possible steady state offset would be cancelled. In order to emulate the saturation of the ferromagnetic core the controller inductance is set to be higher of the machine one. In this way the controller will see a lower machine inductance as wanted. On the other hand a controller inductance lower than the machine one could represent the case of poor knowledge of the PMSM parameters. The test, whose results are reported in Fig. 13, has been performed with an increase of the controller $L_d$ inductance of 50% of the nominal value with respect to the PMSM one while Fig. 14 shows the test where a reduction of 50% has taken place. As it can be noticed the OS-DB achieves a faster transient compared to the standard implemented FPGA DB in both cases of inductance variation. Fig. 15 shows the experimental results for a $i_q$ transient derived from an increase of the controller

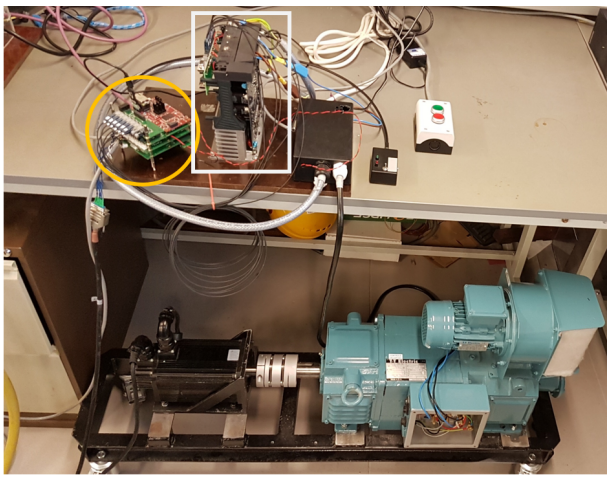

Fig. 9. Experimental set-up: 2L-VSI (white rectangle), control board (yellow circle) and motors.

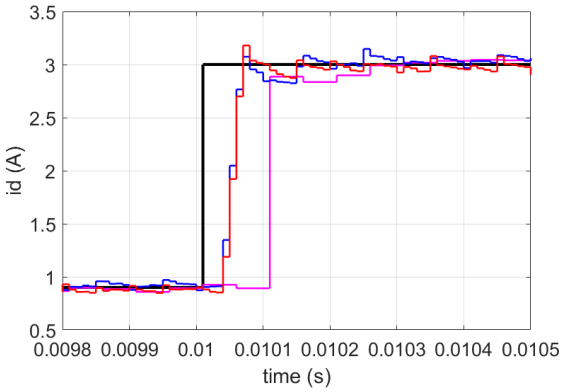


Fig. 10. System response to a reference $i_d$ step from 0.9 to 3 A at standstill. Reference current $i_d$ (black line), DSP DB $i_d$ (magenta line), FPGA DB $i_d$ (blue line), OS-DB $i_d$ (red line).

$L_q$ inductance of 50% while Fig. 16 shows the same transient at a different speed and for a reduction of 50% of the nominal value with respect to the PMSM one. Also for the quadrature axis inductance under any mismatch the OS-DB outperforms the standard FPGA implemented DB.

## VIII. Conclusions

In this paper a novel OS-DB current control approach for PMSMs drives operating at a controller sampling frequency multiple of the power converter switching frequency has been proposed. A disturbance observer has been implemented to estimate the converter voltage distortions. The FPGA implemented OS-DB controller permits to achieve a constant switching frequency and an optimal current ripple along with a high current loop bandwidth and robust behaviour to parameter variation. Both simulative and experimental results show that the proposed controller performs as a standard FPGA implemented DB controller when the controller parameters coincide with the machine parameters. The robustness of the model-based controller and observer with respect to parameter mismatching has been investigated showing that the performances largely increase when a OS-DB solution is adopted.

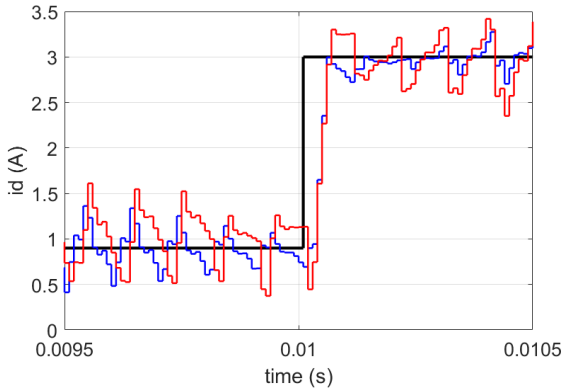


Fig. 11. $i_d$ step from 0.9 to 3 A at $\omega_m$ of 150 $\frac{rad}{s}$. Reference current $i_d$ (black line), FPGA DB $i_d$ (blue line), OS-DB $i_d$ (red line).

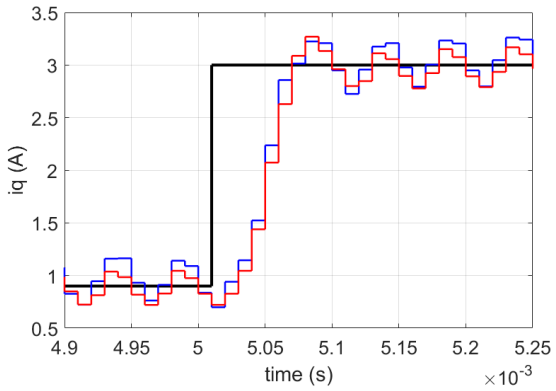


Fig. 12. $i_q$ step from 0.9 to 3 A at $\omega_m$ of 130 $\frac{rad}{s}$. Reference current $i_q$ (black line), FPGA DB $i_q$ (blue line), OS-DB $i_q$ (red line).

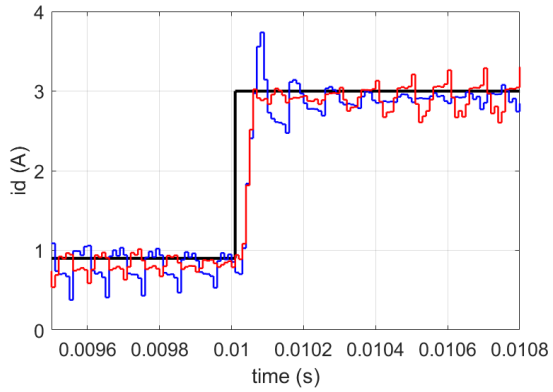


Fig. 13. $i_d$ step from 0.9 to 3 A at $\omega_m$ of 100 $\frac{rad}{s}$. Reference current $i_d$ (black line), FPGA DB $i_d$ (blue line), OS-DB $i_d$ (red line).

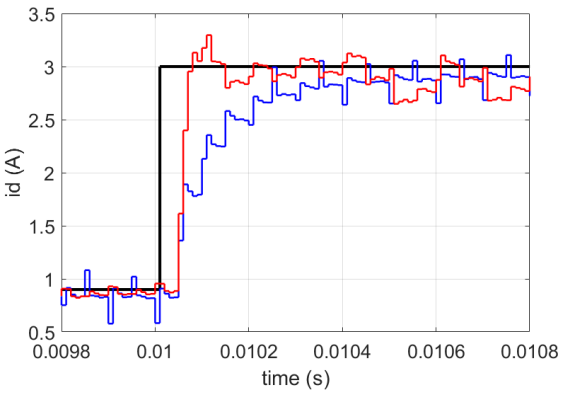


Fig. 14. $i_d$ step from 0.9 to 3 A at $\omega_m$ of 50 $\frac{rad}{s}$. Reference current $i_d$ (black line), FPGA DB $i_d$ (blue line), OS-DB $i_d$ (red line).

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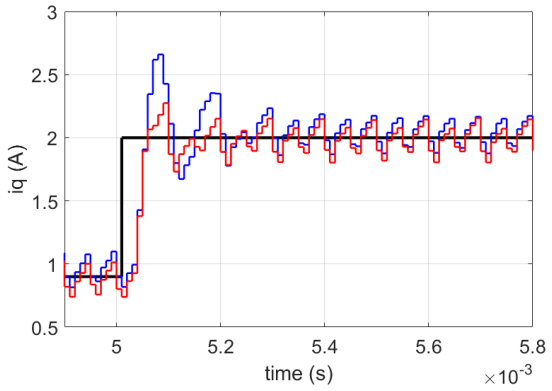


Fig. 15. $i_q$ step from 0.9 to 3 A at $\omega_m$ of 50 $\frac{rad}{s}$. Reference current $i_q$ (black line), FPGA DB $i_q$ (blue line), OS-DB $i_q$ (red line).

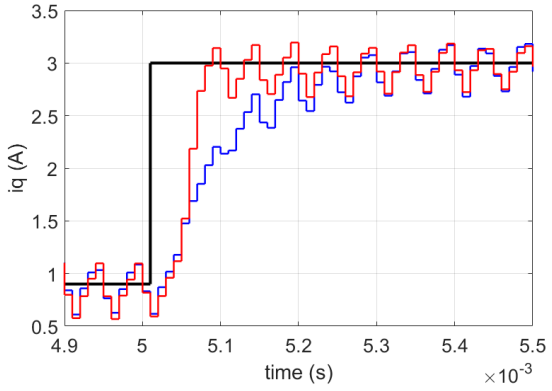


Fig. 16. $i_q$ step from 0.9 to 3 A at $\omega_m$ of 100 $\frac{rad}{s}$. Reference current $i_q$ (black line), FPGA DB $i_q$ (blue line), OS-DB $i_q$ (red line).

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