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How to cite:

Bush, Nathan; Heymes, Julian; Hall, David; Holland, Andrew and Jordan, Douglas (2021). Measurement and optimization of clock-induced charge in electron multiplying charge-coupled devices. *Journal of Astronomical Telescopes, Instruments, and Systems*, 7(1), article no. 016002.

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Version: Version of Record

Link(s) to article on publisher's website:  
<http://dx.doi.org/doi:10.1117/1.jatis.7.1.016002>

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# Measurement and optimization of clock-induced charge in electron multiplying charge-coupled devices

Nathan Bush,<sup>a,\*†</sup> Julian Heymes<sup>ORCID</sup>,<sup>a</sup> David Hall,<sup>a</sup> Andrew Holland,<sup>a</sup> and Douglas Jordan<sup>b</sup>

<sup>a</sup>The Open University, Department of Physical Sciences, Milton Keynes, United Kingdom

<sup>b</sup>Teledyne-e2v, Chelmsford, United Kingdom

**Abstract.** Electron multiplying charge-coupled devices (EMCCDs) are a variant of standard CCD technology capable of single-optical photon counting at MHz pixel readout rates. For photon counting, thermal dark signal and clock-induced charge (CIC) are the dominant source of noise and must be minimized to reduce the likelihood of coincident events. Thermal dark signal is reduced to low levels through cooling or operation in inverted mode (pinning). However, mitigation of CIC requires precise tuning of both parallel and serial clock waveforms. Here, we present a detailed study of CIC within Teledyne-e2v EMCCDs with a goal of better understanding the physical mechanisms that dominate CIC production in both noninverted and inverted mode operations (IMO). Measurements are presented as a function of parallel and serial clock timings, clock amplitudes, and device temperature. The effects of radiation damage and annealing are also discussed. A widely accepted view is that CIC is signal generated through impact ionization of energetic holes as the clock phase is driven high. While this explanation holds for IMO, we propose that the majority of CIC generated in noninverted mode is in fact due to a secondary effect of light emission from hot carriers. The information from this study is then used to optimize CIC on Teledyne e2v CCD201s operating at 1-MHz pixel rate in NIMO. For the CCD201, we obtained total CIC levels as low as  $6.9 \times 10^{-4}$  e<sup>-</sup>/pix/frame with  $\geq 90\%$  detective quantum efficiency. We conclude with proposals to further reduce CIC based upon modifications to clocking schemes and device architecture. © 2021 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: [10.1117/1.JATIS.7.1.016002](https://doi.org/10.1117/1.JATIS.7.1.016002)]

**Keywords:** electron multiplying charge coupled device; charge coupled device; clock-induced charge; defects; photon counting.

Paper 20093 received Jun. 28, 2020; accepted for publication Dec. 1, 2020; published online Jan. 8, 2021.

## 1 Introduction

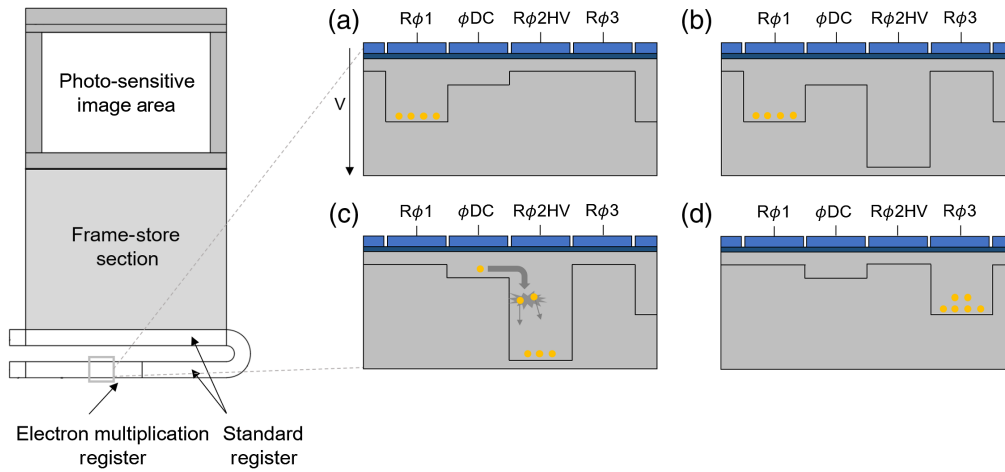
Electron multiplying charge-coupled devices (EMCCDs) allow single photon detection through use of an in-built gain mechanism that amplifies signals above the read noise of the output amplifier.<sup>1</sup> This is achieved through the inclusion of an electron multiplication (EM) register that is appended to the standard serial register and connected to its own output (Fig. 1). The device otherwise functions identically to a standard CCD, with an image area, frame store, and conventional output. Use of the EM register reduces the read noise by a factor equal to the applied EM gain, allowing the devices to be operated at high speed with a low effective read noise.<sup>2</sup> The multiplication process is stochastic and therefore adds noise to the output signal, quantified by the excess noise factor (ENF), converging to a factor  $\sqrt{2}$  increase in shot noise for high EM gain.<sup>3</sup> Operation with both high gain (typically  $\geq 1000$ ) and low incident photon flux (typically  $< 0.1$  photons/pixel/frame) allows operation in “photon counting mode,” whereby any event above a threshold (typically  $5\sigma$ ) is considered a single photon event.<sup>4</sup>

Operation in photon-counting mode renders the ENF irrelevant; however, the statistical nature of the multiplication process means that a fraction of the signal electrons will not be

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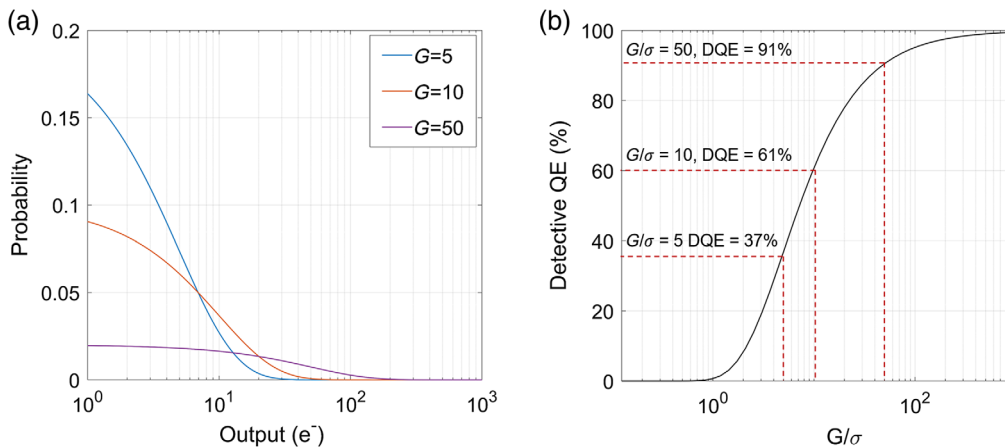
\*Address all correspondence to Nathan Bush, [Nathan.Bush@jpl.nasa.gov](mailto:Nathan.Bush@jpl.nasa.gov)

†Present Address: California Institute of Technology, Jet Propulsion Laboratory, Pasadena, California, United States



**Fig. 1** EMCCD schematic for the example of the Teledyne-e2v CCD 201,<sup>5</sup> with example clocking sequence: (a) charge stored beneath  $R\phi 1$ , (b)  $R\phi 2HV$  pulse is applied, (c)  $R\phi 1$  pulse low, charge moves beneath  $\phi DC$  and experiences high field, and (d) charge transferred to  $R\phi 3$ , ready to transfer to the next EM element.

multiplied above the detection threshold. The percentage of events above the threshold is referred to as the detective quantum efficiency (DQE) and is a function of the ratio between the applied EM gain and the base read noise of the detector, often referred to as the  $G/\sigma$  ratio. Figure 2 shows the output distribution of the EM register, assuming single electron input, for different values of EM gain. It may appear intuitive to increase the EM gain as high as possible and amplify more events above the threshold to maximize detection. In practice, the increase in amplitude of the  $R\phi 2HV$  clock results in increased noise due to clock-induced charge (CIC), and so a compromise must be achieved for optimal device performance. A  $G/\sigma$  ratio of 50 provides a DQE above 90% while maintaining acceptable background noise levels and is a significant improvement over operation in analog mode.<sup>6</sup> For the example of an EMCCD with  $80 e^-$  read noise, an EM gain of  $\times 4000$  is required. Based on this relationship, the baseline read noise always has a considerable effect on the photon-counting performance of the detector. Higher noise must be compensated with increased EM gain to maintain the same DQE, potentially leading to an unnecessary increase in serial CIC and degradation in serial charge transfer efficiency (CTE).<sup>7</sup> Optimization of EMCCDs in photon-counting mode should therefore begin with



**Fig. 2** Output distribution for the CCD201 EMCCD with a single electron input with EM gains of 5, 10, and 50. A fraction of photons will always be lost below the detection threshold since the output distribution always peaks at 1, regardless of EM gain. (a) Influence of  $G/\sigma$  ratio on the DQE of the detector. For the example of a CCD201 with  $80 e^-$  read noise, an EM gain of  $\times 4000$  is required to detect 90% of the incident photons using a  $5\sigma$  threshold.

minimization of the total system noise as much as practically possible, reducing the required EM gain for photon counting, followed by mitigation of the remaining noise sources: thermal dark signal and CIC.

In photon-counting mode, thermal dark signal and CIC cannot be distinguished from signal due to an optical source. The effect of each is to increase the background noise of an image and the likelihood of a “coincident event” whereby a CIC or dark signal electron is collected within the same pixel as an optically generated electron. Thermal dark signal is controlled by either cooling the detector or inverted mode operation (IMO), also referred to as pinning. The degree of cooling and/or whether pinning is required depends primarily upon the signal flux of the scene under observation. Thermal dark signal should be at least an order of magnitude lower than the signal flux to not meaningfully impact the cumulative integration time. Values below  $1 \times 10^{-4} \text{ e}^-/\text{pix}/\text{s}$  are easily achievable with temperature of  $\sim 165 \text{ K}$  in noninverted mode (NIMO).<sup>8</sup> Operation in IMO can reduce this value by over an order of magnitude but can give rise to a CIC penalty if the device is not optimized appropriately.

CIC is signal generated through the process of clocking the device, it is widely reported to have an exponential dependence on clock amplitude, a dependence on pixel rate, a dependence on the operating mode (IMO or NIMO), and a dependence on the waveforms used to drive the device.<sup>9–11</sup> The lowest levels of total CIC currently reported in the literature for a CCD201 are at the level of  $\sim 3.1 \times 10^{-3} \text{ e}^-/\text{pix}/\text{frame}$ ,<sup>6</sup> obtained at a  $G/\sigma$  ratio of 50, at 10 MHz, and in IMO. Values lower than this have been reported but at a lower  $G/\sigma$  ratio.<sup>8,12</sup> The low CIC is a result of both operation at high pixel rates and the use of highly tuned serial waveforms and is an impressive performance. However, even at this low level, CIC remains the dominant noise source for EMCCDs and can limit their sensitivity for certain applications.<sup>10</sup> Operation at high speed with tight requirements on waveform tuning also places constraints on instruments that could otherwise benefit, including but not limited to the complexity of electronics and thermal management. The aim of this study was to investigate CIC in a variety of CCD201 EMCCDs to understand the generation process and use this information to mitigate CIC at slower pixel rates and over a wide range of device operating temperatures.

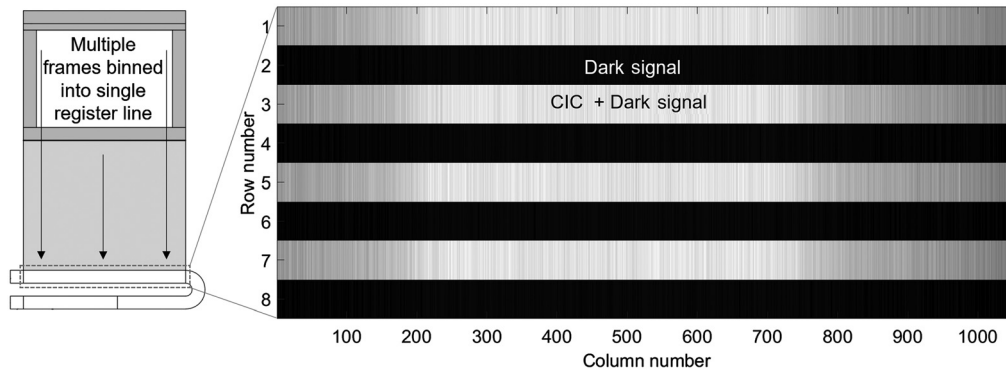
## 2 Experimental Methods

Three methods were used to measure CIC in this investigation: the “charge binning” method, the “pulsed phase” method, and the standard measurement in photon-counting mode. The charge binning method was used to measure parallel CIC, while the remaining two methods were used to measure parallel and serial CIC, independently and combined.

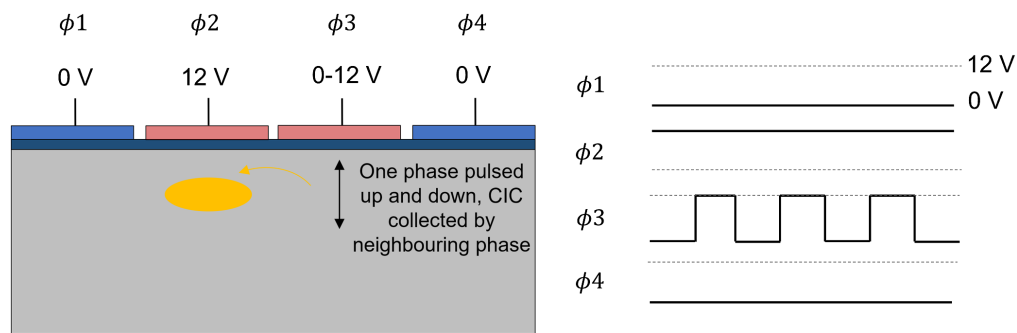
The charge binning method consists of binning many rows ( $>10^5$ ) into the serial register to create a single line of signal that is predominantly CIC due to image area clocking. This line is then read out of the device. The image area is then held with a frame integration time equal to the time taken to bin the chosen number of image rows, during which time dark signal collects in the array. This time is typically between 1 and 100 s. The single frame is then binned into the register and read out. Implementation of this method gives an image that consists of alternative lines of parallel CIC plus dark current and solely dark current (Fig. 3). The dark current is subtracted from the row containing both signal sources so only parallel CIC remains. Although a small amount of parallel CIC is present within the row of dark current signal, this can easily be removed in postprocessing since the number of parallel transfers is known (2069 for the CCD201-20). These rows of CIC with the dark current subtracted can then be averaged and divided by the number of parallel transfers binned into the register to provide a row-averaged value for parallel CIC in units of  $\text{e}^-/\text{pix}/\text{frame}$ .

For the pulsed phase method, individual image or register phases are pulsed many times ( $>10^5$ ) while a neighboring phase is also held high (Fig. 4). Any CIC generated by the pulsed phase is collected beneath the neighboring phase and read out when the acquisition is complete. The method gives phase-level resolution of CIC and can be used to identify “hot spots” within either the image area or serial register. For the EM register, the method can also be applied by pulsing the  $R\phi 2\text{HV}$  clock and keeping a neighboring phase high. A complication arises in that for high  $R\phi 2\text{HV}$  clock levels, the subsequent read out process can expose signals to EM gain. To





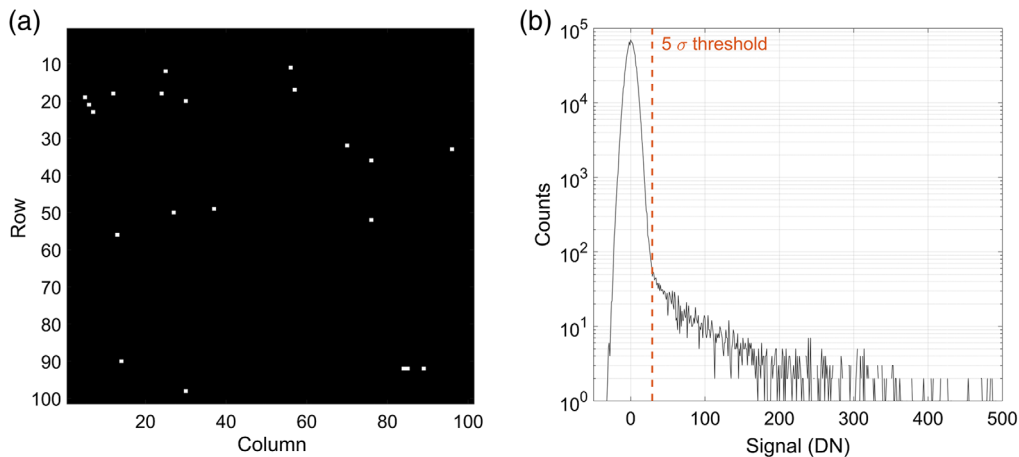
**Fig. 3** Example image obtained using the charge binning method showing eight alternate lines of signal due to CIC + dark signal and solely dark signal. Row-by-row subtraction gives a signal level that is due to CIC that can be used to calculate the parallel CIC generation rate in units of  $e^-/\text{pix}/\text{frame}$ .



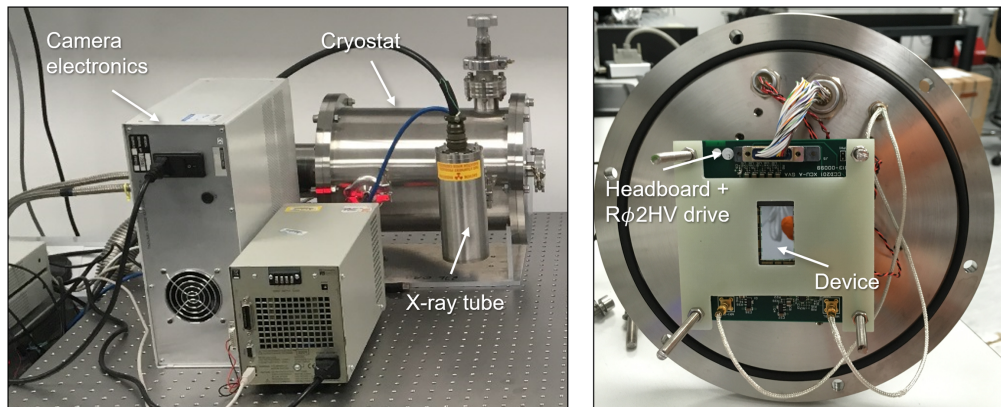
**Fig. 4** The “pulsed phase” method whereby individual phases are repeatedly clocked high and low, generating CIC that is then collected in the potential well of a neighboring phase. The phases that are clocked and held constant can be alternated to provide phase-level resolution of CIC generation sites. To the right is an example clocking sequence for this method for the image/store regions. Any CIC generated beneath  $\phi_3$  is collected beneath  $\phi_2$ .

avoid this, CIC measured in the EM register was back clocked and read through the standard high responsivity (HR) output. Finally, the photon-counting mode measurement used a fixed threshold ( $5\sigma$ ) above which any event was deemed either dark signal or CIC (Fig. 5). The CIC was separated into parallel and serial components through appropriate use of parallel and serial overscan.

Devices were controlled by an XCAM™ Scientific CCD camera drive system that provided customizable control over all bias lines and clock amplitudes (Fig. 6). The  $R\phi_2HV$  line was controlled by a circuit that provided a configurable amplitude and pulse length (phase time) ranging from 31.25 ns to 1 ms. Signal conversion and noise suppression were controlled by a clamp and sample CDS card with a 14-bit ADC. The default pixel rate was 1 MHz unless otherwise stated. Devices were cooled to a nominal operating temperature of 165 K through the use of a CryoTiger™ cooling system that was coupled to the device through a copper cold finger. The cryostat was held at a pressure of  $\sim 10^{-6}$  mbar using a Pfeiffer™ roughing and turbo-pump system. Temperature control was handled by PT-1000 temperature sensors mounted to the device package and linked to a Lakeshore Model 325 temperature controller with a resistive heater. Temperature measurement accuracy was within 0.2 K for the entire study. Each device was calibrated using an  $^{55}\text{Fe}$  source or PTC to derive the system calibration (k-gain) and confirm acceptable linearity over the useable dynamic range. The terminology used in this study includes phrases such as phase time; the time a clock phase is held in the high voltage state, and frame time; the total time to read out a frame (including integration time).



**Fig. 5** Example region of an image obtained at  $G/\sigma = 50$  of a CCD201 at 1 MHz, CIC events have variable signal due to the statistical nature of the gain process. A  $5\sigma$  cut is used, above which the pixel is considered to harbor an “event,” light shielded images can be used to measure CIC in this way. (a)  $5\sigma$  events. (b) A single image signal histogram with the threshold applied.



**Fig. 6** Experimental setup, consisting of a camera rack, cryostat, HV power supply for the  $R\phi 2$ HV line, an x-ray tube coupled with Mn fluorescence target to generate  $^{55}\text{Fe}$  x-rays.

### 3 Results

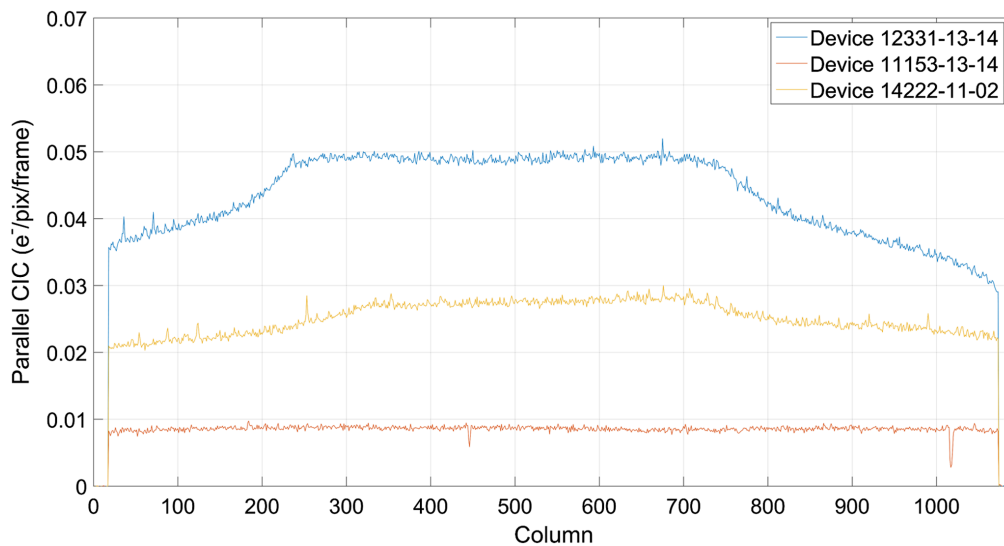
#### 3.1 Charge Binning Method

The charge binning method was used to investigate the impact of clock amplitude, operating mode, clock frequency, and irradiation on parallel CIC for multiple CCD201 EMCCDs. No attempt was made to minimize CIC at this stage of the study as the key focus was to investigate the dependence of CIC on the device operating parameters. Devices were operated with square waveforms according to the CCD201 datasheet “2-phase” clocking scheme with a default amplitude of 12 V, parallel frequency of 100 kHz, and serial frequency of 1 MHz, unless otherwise stated. For IMO,  $V_{SS}$  was set to the datasheet value of 4.5 V and image clock high and low were set to 7 and  $-5$  V, respectively. For NIMO,  $V_{SS}$  was set to 0 V and the clock high and low levels were 12 and 0 V, respectively. Measurements were performed on a total of five devices at identical voltage and clocking conditions to provide a measure in the device–device variance in CIC. Table 1 shows the row-averaged result under the default operating conditions, with an approximate factor of  $\times 5$  variation across devices from these batches. Devices from the same wafer showed an approximate factor  $\times 1.5$  difference.

Figure 7 shows the row CIC profile for three of the five devices when operated in IMO, where there is a clear trend of increasing CIC toward the center of the profile for two of the devices.

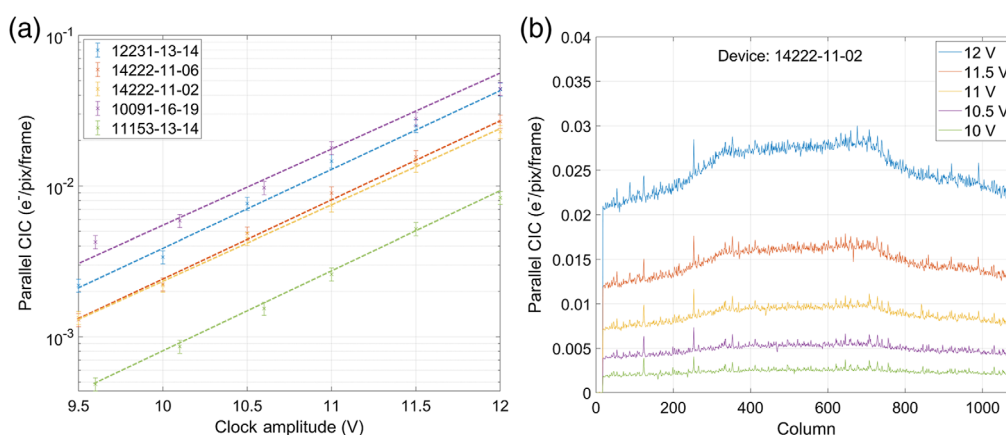
**Table 1** Summary of parallel CIC measured in IMO at standard datasheet voltages using the charge binning method. The measurement was performed at 165 K with a parallel frequency of 100 kHz and clock amplitude of 12 V. An approximate factor  $\times 5$  variation was observed across these devices.

Device S/N	Parallel CIC ( $e^-/\text{pix}/\text{frame}$ )
14222-11-02	$(2.29 \pm 0.22) \times 10^{-2}$
14222-11-06	$(2.42 \pm 0.14) \times 10^{-2}$
10091-16-19	$(4.47 \pm 0.24) \times 10^{-2}$
11153-13-14	$(8.80 \pm 0.38) \times 10^{-3}$
12231-13-14	$(4.38 \pm 0.15) \times 10^{-2}$

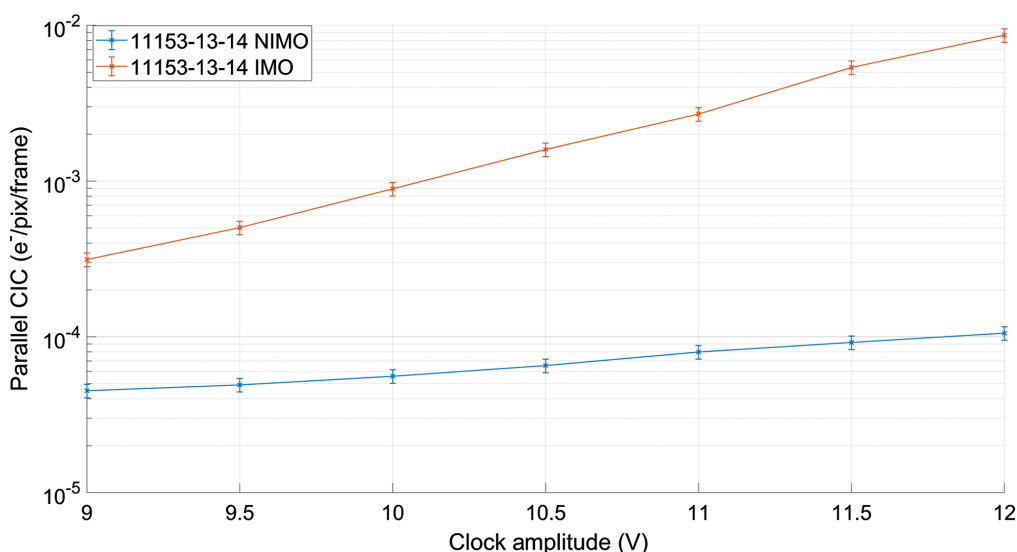


**Fig. 7** Comparison of the parallel CIC row profile for three devices, obtained under identical operating conditions (100,000 frames binned into the register). For two of the devices, CIC increases for the central columns compared with values measured at the edge.

Column “spikes” are also present that were observed to be consistent in their amplitude and location, and not due to transient effects. Each device showed an exponential increase in CIC with clock amplitude (Fig. 8), and the factor difference in CIC remained approximately constant at each amplitude value. While the datasheet recommended clock swing is 12 V for the CCD201, a reduction to 10 V resulted in an order of magnitude reduction in CIC or IMO operation with no CTE penalty. For a 12-V clock swing, moving from IMO to NIMO resulted in a decrease in CIC approaching two orders of magnitude (Fig. 9). For NIMO, the dependence on clock amplitude was much weaker, with only a factor  $\times 2$  reduction moving from 12 to 9 V under the same measurement conditions. The column profile of CIC is fairly uniform across a device when operated inverted; however, in NIMO the profile is dominated by the presence of signal “spikes” that increased in intensity and frequency with increasing clock amplitude (Fig. 10). The signal within these spikes spreads across multiple columns while remaining significantly below the well capacity of the device. We believe the generation mechanism of these signal spikes to be the same as those seen within the IMO profile of CIC (Fig. 7). However, it is only in NIMO where they appear to be the dominant source of signal.

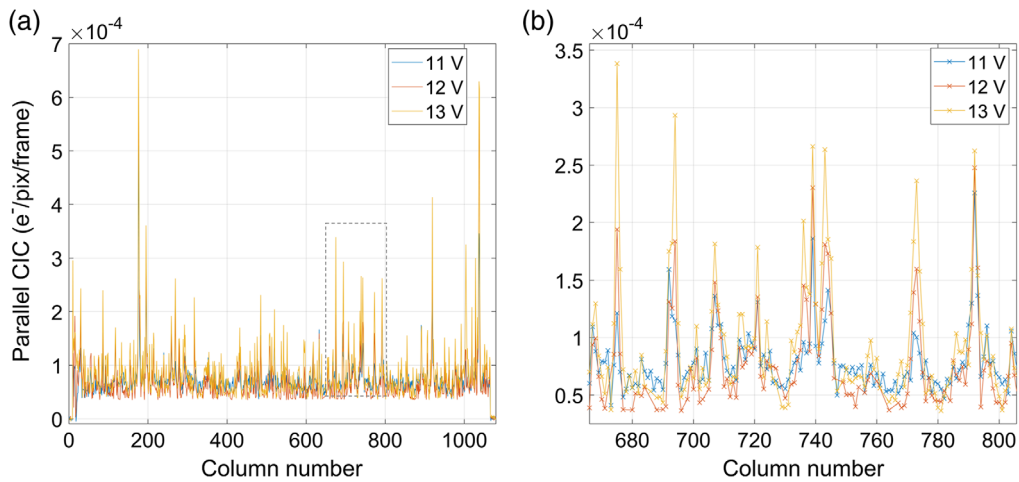


**Fig. 8** (a) Parallel CIC as a function of clock amplitude measured with  $V_{ss} = 4.5$  V and a parallel frequency of 100 kHz using the charge binning method (100,000 frames binned into the register). The average CIC increases exponentially with clock amplitude. An increase of 2 V results in approximately an order of magnitude increase in CIC for each device. (b) CIC profile for device 14222-11-02 as a function of clock amplitude. The “spikes” in signal (e.g., column 240) that can be seen were observed to be real and not due to transient effects.

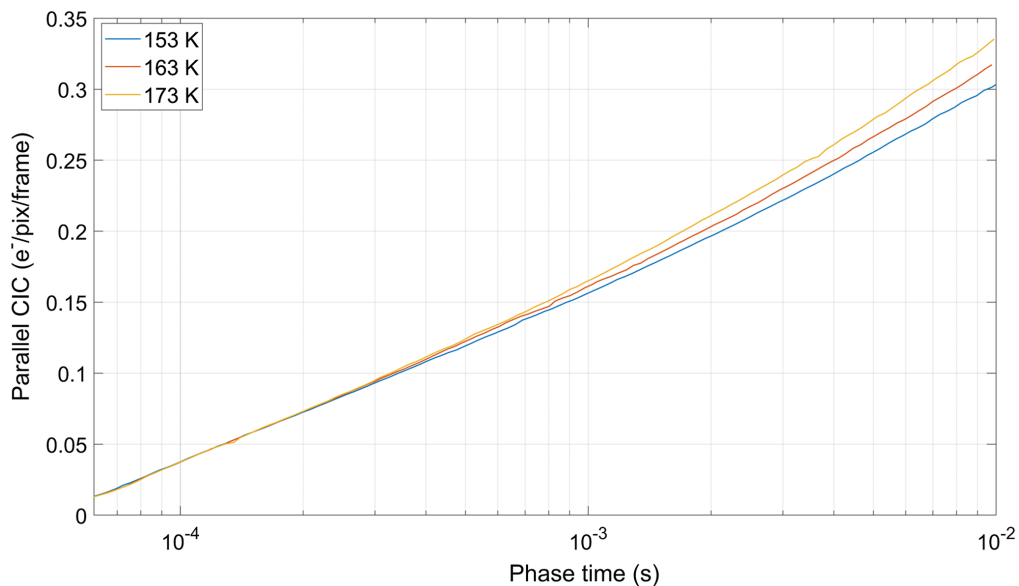


**Fig. 9** Comparison of CIC measured in IMO and NIMO for device 11153-13-14 measured at 100 kHz parallel frequency with square wave clocks. At 12 V amplitude, moving to NIMO provides almost a factor  $\times 100$  reduction in parallel CIC, this drops to a factor  $\times 10$  reduction at 9 V.

The dependence of CIC on phase time was found to be logarithmic (Fig. 11), supporting the reported result that faster parallel clock speeds result in decrease in CIC.<sup>2,13</sup> The measurement was repeated for three temperatures. At longer phase times, higher temperatures lead to a slight increase in CIC, with a 10% difference in the result at 153 K compared to 173 K for the  $10^{-2}$  s phase time. The measurement was repeated for temperatures ranging from 150 to 200 K (Fig. 12) with a shorter phase time of  $1.5 \times 10^{-4}$  s, where only a 5% change was noted. The interplay between phase time and temperature suggests the effect may be due to subtle changes in the emission characteristics of the interface states that are deemed to be responsible for parallel CIC in IMO. Since the differences due to temperature were small compared to the effects of phase time and clock amplitude, we conclude that temperature is not an important parameter for CIC optimization.

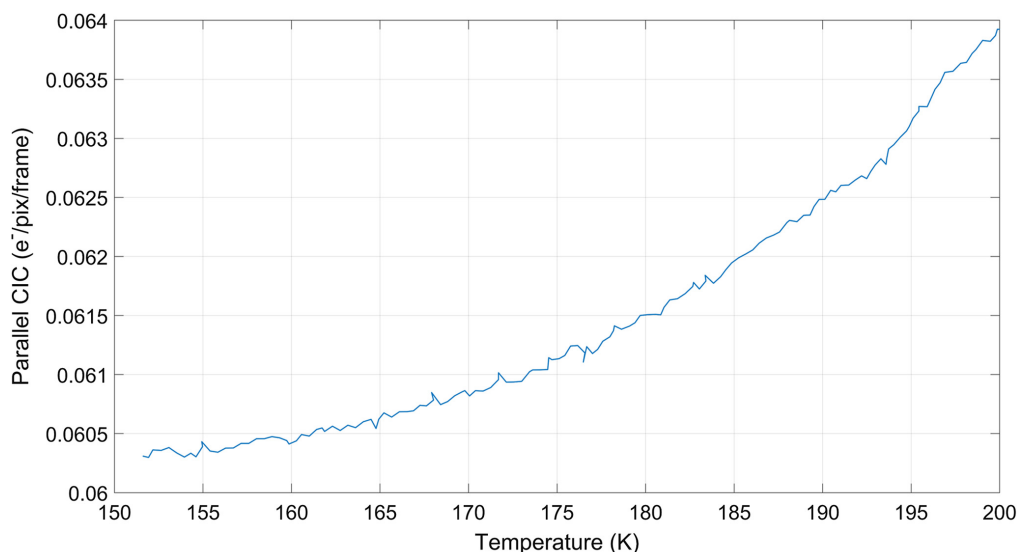


**Fig. 10** Column profile of CIC for device 11153-13-14 measured in NIMO using the pulsed phase method, with 100,000 pulses for this particular image. The CIC is dominated by “spikes” in signal that increase in amplitude and frequency as the clock amplitude is increased. (b) shows a zoomed region of (a).

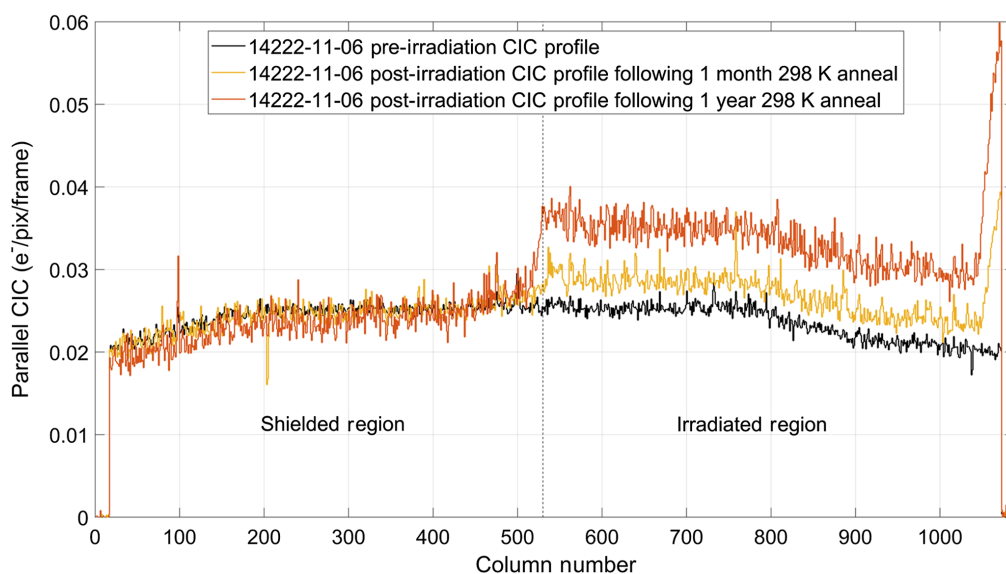


**Fig. 11** Parallel CIC as a function of parallel phase time and temperature measured in IMO, at 12 V for three temperatures. CIC increases logarithmically as a function of phase time and showed a small increase as a function of temperature for the longer phase times. Error bars have not been shown for clarity.

Device 14222-11-06 was irradiated with 74 MeV protons at the Paul Scherrer Institut (PSI), Switzerland. The irradiation was performed unbiased at room temperature to a fluence of  $(1.04 \pm 0.10) \times 10^{10}$  p/cm<sup>2</sup>, corresponding to a total ionizing dose (TID) of 1.2 krad (SiO<sub>2</sub>). The parallel CIC measurement was repeated following 1 month and a year at room temperature, shown by Fig. 13, where a factor increase of  $\times 1.1$  rising to a  $\times 1.5$  were measured, respectively. The profile also changed slightly, with the right-hand side of the device exhibiting a sharp increase in CIC that was also a function of the anneal period. Since the measurement was performed in IMO, the increase in CIC could be due to an increase in the number of interface states available for CIC generation throughout the anneal period. Such an explanation is consistent with the observations of dark current “reverse annealing” in earlier studies where CCDs



**Fig. 12** Parallel CIC as a function of temperature measured with a  $1.5 \times 10^{-4}$  s phase time, as 12 V in IMO. The difference in CIC between 150 and 200 K was  $\sim 5\%$ . Error bars are not shown, for clarity.



**Fig. 13** Parallel CIC profile for device 14222-11-06 preirradiation, postirradiation with a 1-month 298 K anneal and a 1-year 298 K anneal.

have been subject to a TID, and the surface component of dark current has increased.<sup>14</sup> The additional increase on the right-hand side of the CCD may be due to a damage enhancement effect whereby protons were scattered from the device package and hit this area of the device with reduced energy, resulting in a greater TID within the region. Surface dark current within the region was also elevated and explained by the same effect. The profile of bulk dark current remained unchanged.

### 3.2 Pulsed Phase Method

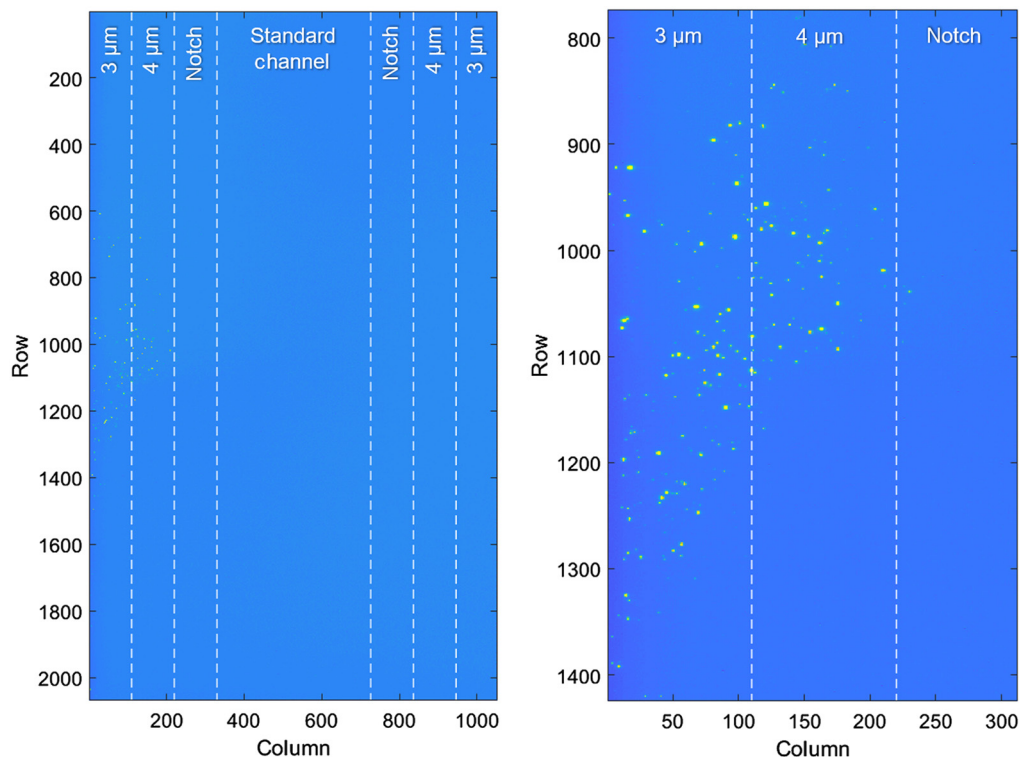
The pulsed phase method was used to investigate parallel CIC on a device that exhibited many signal “spikes” as highlighted by the parallel binning method. The device studied was a



CCD301, a variant of the CCD201 with modifications to the parallel section of the device for reduced susceptibility to radiation-induced trapping sites. The parallel section of this device is split into bands that are symmetric about the center of the device, with each band exhibiting a different parallel design: a 3- $\mu\text{m}$  channel, a 4- $\mu\text{m}$  channel, a standard 9- $\mu\text{m}$  channel with a 3- $\mu\text{m}$  “notch” implant, and the 9- $\mu\text{m}$  channel that is standard for the CCD201. Figure 14 shows an image obtained from CCD301 18011-09-11 with the banded regions labeled. The figure was obtained using the pulsed phase method whereby a single image clock phase was repeatedly pulsed with a neighboring phase held high to collect the signal. In this case,  $I\phi_1$  was pulsed to generate the CIC, while  $I\phi_2$  was held high to collect any generated signal. Multiple CIC-related “defects” are visible.

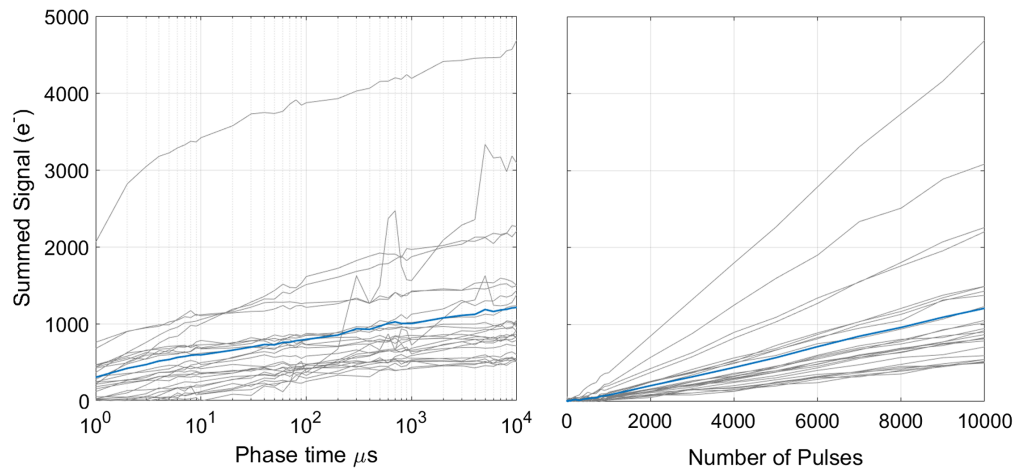
The defects were primarily located within the 3- and 4- $\mu\text{m}$  bands. However, this is assumed to be coincidental since a higher incidence was not noted on the opposite side of the same device or other CCD301s in the same batch. Instead, we believe that this effect is what was noticed during the investigation of NIMO CIC using the parallel binning method but is for some reason more pronounced on this device. The number and intensity of the defects were measured as a function of phase time and clock amplitude (Figs. 15 and 16). The dependence on phase time was logarithmic, similar to that observed for parallel CIC using the binning method, while the dependence on number of pulses was linear. There was no discernable temperature dependence of their intensity of number, and the dependence of generated signal on clock amplitude was found to be exponential.

The visual appearance of the defects is not dissimilar to a point spread function (PSF) due to a point source of light. Signal spreads to neighboring pixels within an approximate  $3 \times 3$  grid, sometimes more depending upon the intensity. A potential explanation for these observations is that there are in fact two mechanisms for CIC generation. Within individual pixels, signal can be generated due to the impact ionization of holes within a high field region as the clock transitions from a low to high state. This results in a localized region of high signal due to CIC that is confined to a single pixel. The other mechanism is that as the carriers pass through the region of

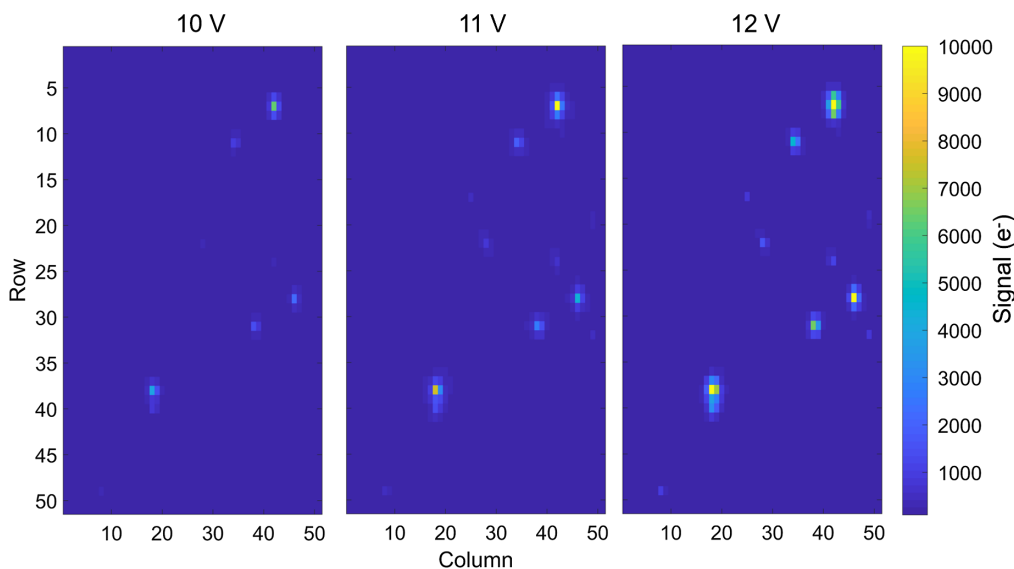


**Fig. 14** Image obtained from device 18011-09-11 using the pulsed phase method. The CIC “defects” are present toward the left-hand side of the device that are mainly contained within the 3- and 4- $\mu\text{m}$  bands. The right panel shows a magnified view of this region. The signal distribution due to these CIC defects is similar to that expected from a point source of light in the same region.





**Fig. 15** Summed signal within a  $3 \times 3$  grid as a function of time the phase was held high (10,000 pulses) and the number of pulses (phase time  $10^4 \mu\text{s}$ ). Each line is for a single defect identified within CCD301 18011-09-11, the blue line represents the mean for all defects. The dependence on phase time is logarithmic, while the dependence on number of pulses is linear. Error bars are not shown, for clarity.



**Fig. 16** Windowed region of device 18011-09-11 using the pulsed phase method at different clock amplitudes. The total amount of signal generated by each defect increased exponentially for each clock amplitude, and the total number of identifiable defects also increased.

high field, they are accelerated to energies sufficient for light emission to occur (“hot carriers”). This light is then collected within the central pixel and the nearest neighbors. Since the light is collected predominantly within a  $3 \times 3$  grid, the absorption length is expected to be or the order of 10 to  $20 \mu\text{m}$ , describing light with wavelength in a range of 700 to 900 nm. The lack of temperature dependence can be explained by the low change in mobility of holes across the temperature range of study, and the exponential dependence on clock amplitude explained by the increase in electric field strength, acceleration, and therefore light emission of the carriers.

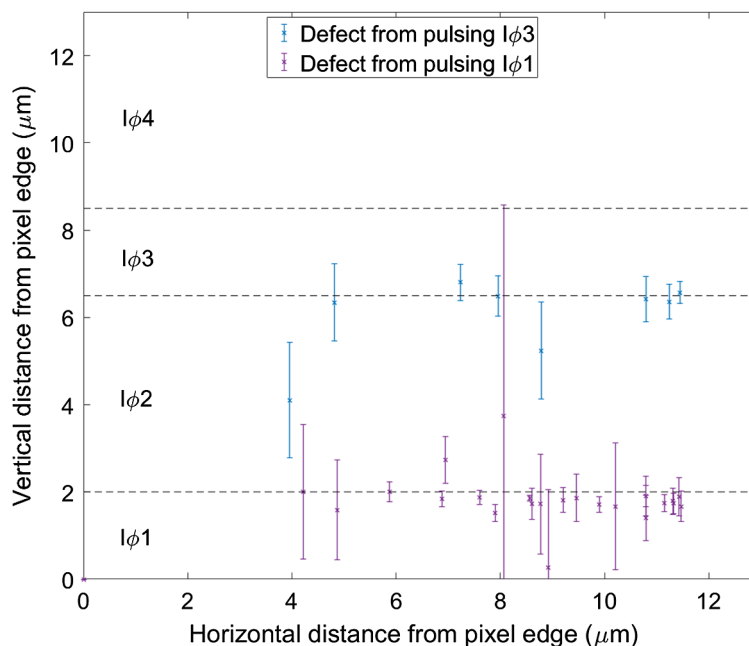
The logarithmic dependence on phase time is satisfied by the same explanation. For IMO parallel CIC, the signal was due to the emission of charge from trapping sites that followed an exponential decay curve. The mechanism here may be similar, where the signal within the central pixel is due to traps that are releasing charge within a high field region. The charge is then accelerated and emits light that is collected within the central pixel and its neighbors. Given

enough time, most of the traps have emitted their charge and so the total CIC begins to tend to a fixed value. The defects are stable in nature, fixed in their pixel location, and produced a consistent amount of charge for a given number of pulses or repeated measurements of phase time and clock amplitude. This implies that the CIC “defects” are due to fixed processing variations that may have resulted in a high hole concentration within a localized region of these pixels, even when operated in NIMO. Future investigations whereby the prevalence of the defects is explored as a function of the image clock low level could support the theory further. In principle, as the low level is increased, the measured intensity should drop.

Since the signal profile of these defects is well described by a PSF, it was possible to centroid the location of the defects with reasonably high precision. Figure 17 shows the result where the location of the defects is overlaid on a schematic of the CCD201 image pixel with phase locations labeled. Remarkably, most of the defects detected using this method appear to be close to the image phase boundaries. There is typically an oxide gap here that acts as a region of high electric field during clocking, and so this observation is consistent with the previous explanation of the signal generation due to the light emission of hot carriers within a region of high electric field. In this measurement, defects were only identified through the pulsing of  $I\phi 1$  and  $I\phi 3$ , none were detected through the same pulsing of  $I\phi 2$  and  $I\phi 4$ . The reason for this is unclear, since the pulsing should invoke the same regions of high field albeit with a switched collecting phase. This observation may therefore be an artifact of the measurement method rather than a property of the defect formation mechanism. Finally, it is worth restating that the specific device in question was a prototype device already considered defective, and no other devices were found to exhibit as many of these features. However, it proved useful as a test subject to further investigate the dominant cause of CIC in NIMO.

The pulsed phase method was applied to the register of a standard CCD201 to investigate register CIC generation. The standard operating conditions of the CCD201 dictate that even when the parallel section of the device is operated in IMO, the register is noninverted. All measurements of serial CIC were made with  $V_{SS}$  at 0 V and register clock amplitudes referenced to  $V_{SS}$  ranging from 0 to 12 V. The  $R\phi 2HV$  clock was operated at biases up to 50 V depending upon the required EM gain.

The EMCCD register is split into three sections that each have a different designs and functionalities. Adjacent to the CCD201 image area is a row of standard serial register elements. The

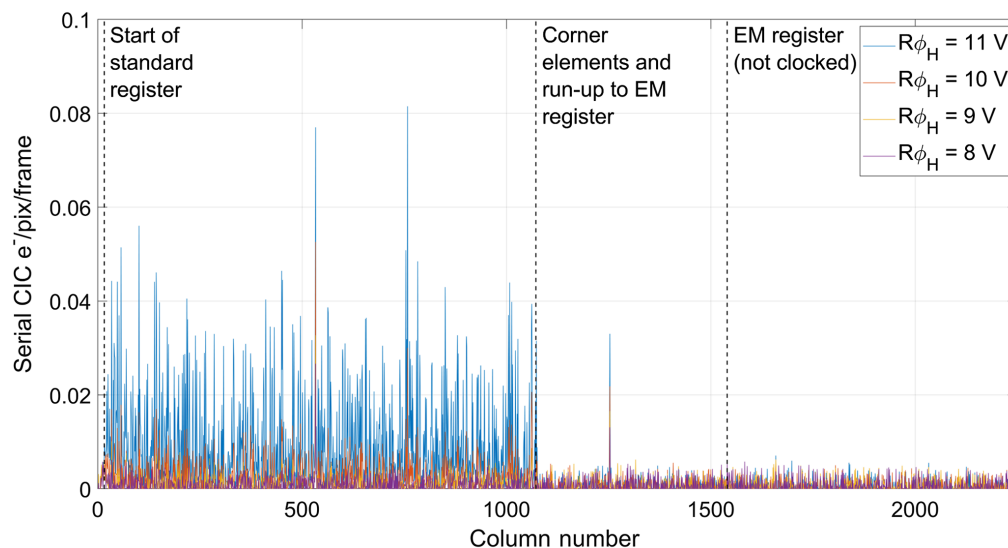


**Fig. 17** Estimated location of CIC defects identified using the pulsed phase method on CCD301 18011-09-11. The location of each defect was estimated by centroiding the signal profile and then scaling the pixel-level location according to the schematic of the CCD301 image/store pixels.

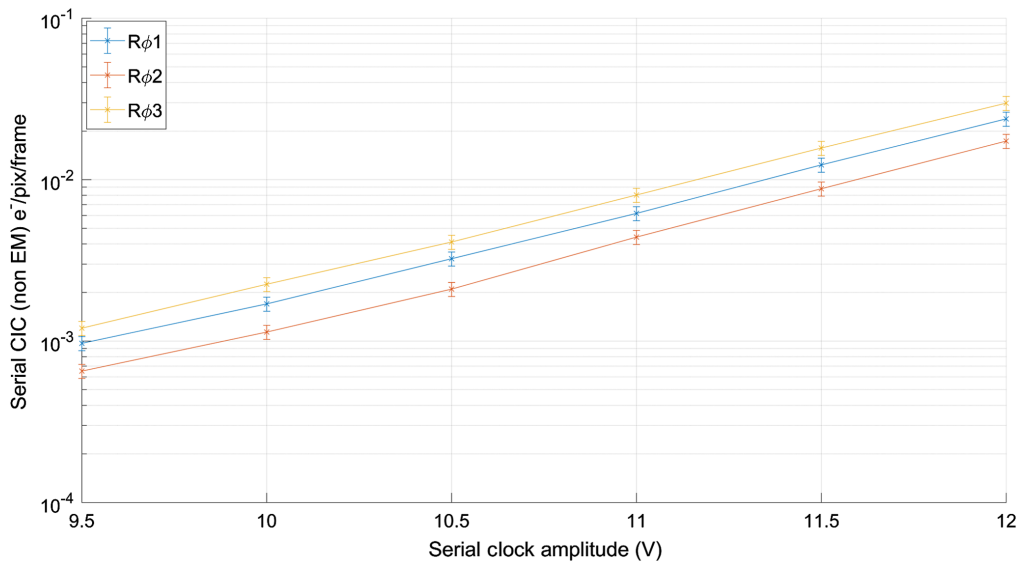
pixels are three-phase, with  $13\ \mu\text{m}$  pitch and  $24\ \mu\text{m}$  width. These register elements have a dump gate that runs parallel to the direction of a serial transfer. Following the standard serial register elements, further elements exist that are similar to those adjacent to the image area but do not have a dump gate. Instead, the pixel boundaries are defined by channel stops. There are also corner elements that act to rotate the direction of transfer by  $180\ \text{deg}$ ,  $\sim 20$  elements complete the full bend. The final stage of the readout chain is the 604 multiplication elements. The EM register pixels are four-phase, with  $16\ \mu\text{m}$  pitch and  $40\ \mu\text{m}$  channel width to allow a higher charge storage capacity.

Figure 18 shows a register profile of CIC for the CCD201 using the pulsed phase method within the register. For this measurement,  $R\phi_2$  was repeatedly pulsed while  $R\phi_1$  was held high as the collecting phase. The EM register does not contain the standard  $R\phi_2$  phase and so was not probed by this measurement. The profile is very similar to that seen for NIMO parallel CIC, whereby the signal is predominantly due to spikes isolated to certain pixels. The amplitude and number of these signal spikes were observed to increase exponentially with clock amplitude. The measurement was repeated for each of register phases and the profile used to calculate the generated CIC in  $e^-/\text{pix}/\text{frame}$  (Fig. 19). For this measurement,  $R\phi_3$  generated the most CIC within the standard register and  $R\phi_2$  the least. This observation may be due to the camera configuration rather than an underlying feature of the CCD201 design, since the serial waveforms were not specifically optimized for each phase and thus exhibited different rise and fall times.

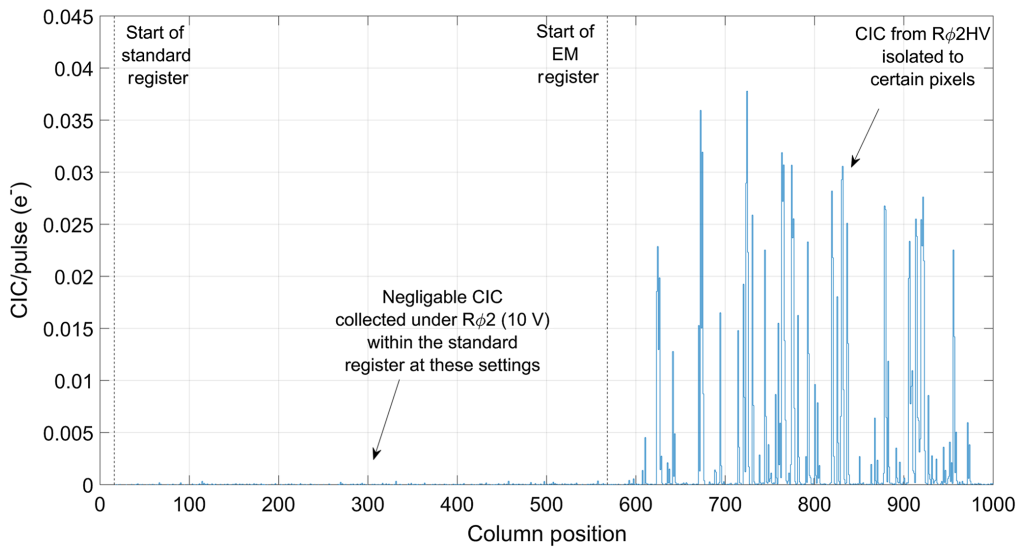
The  $R\phi_2\text{HV}$  phase is assumed to generate the most CIC when operating an EMCCD with high EM gain due to the high amplitude of the clock. The pulsed phase method was therefore applied to the EM register with a specific focus on  $R\phi_2\text{HV}$ , once again investigating amplitude and phase time. Figure 20 shows the profile of CIC obtained within the EM register when  $R\phi_2\text{HV}$  was repeatedly pulsed high to 40 V. Once again, most of the CIC was isolated to certain pixels, while some contained very little signal even at high amplitudes. The profile was averaged to provide a way to measure for CIC within this portion of the device as a function of clock amplitude and phase time. Figure 21 shows how the number and amplitude of the spikes change dramatically as a function of the clock amplitude, with the average value increasing exponentially. The dependence on pulse length was found to be approximately linear; with a factor  $\times 10$  reduction resulting in a corresponding CIC reduction (Fig. 22). The EM gain of the same device was measured across a similar voltage range to indicate relevance to standard operation. EM gain



**Fig. 18** Register profile of the CCD201 obtained using the pulsed phase method (100,000 pulses) within the serial register at different clock amplitudes. The EM register does not contain the standard  $R\phi_2$  phase and so was not probed by this measurement. The profile is very similar to that seen for NIMO parallel CIC, whereby the signal is predominantly due to spikes isolated to certain pixels. The amplitude and number of these signal spikes were observed to increase exponentially with clock amplitude.



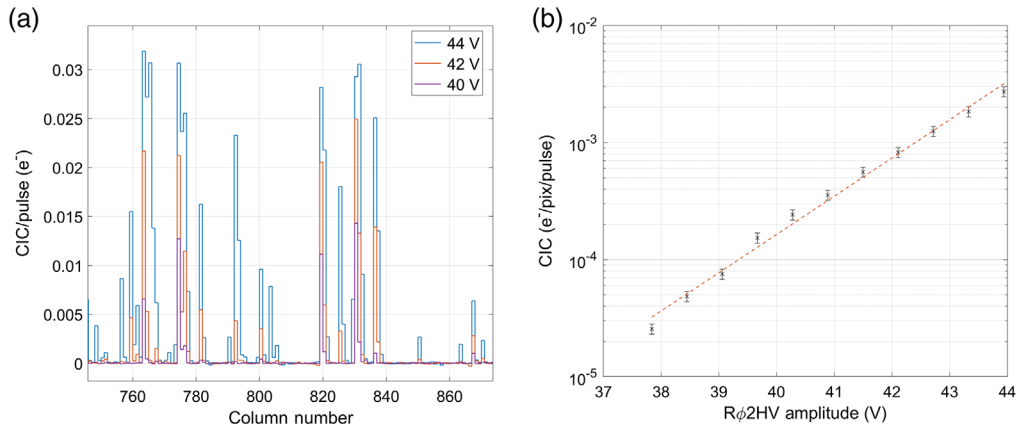
**Fig. 19** Average CIC generated by each phase of the standard register, measured using the pulsed phase method. R $\phi$ 3 exhibited the most CIC; however, this result may be due to the waveforms used to drive the device as opposed to a specific feature of the CCD201 design.



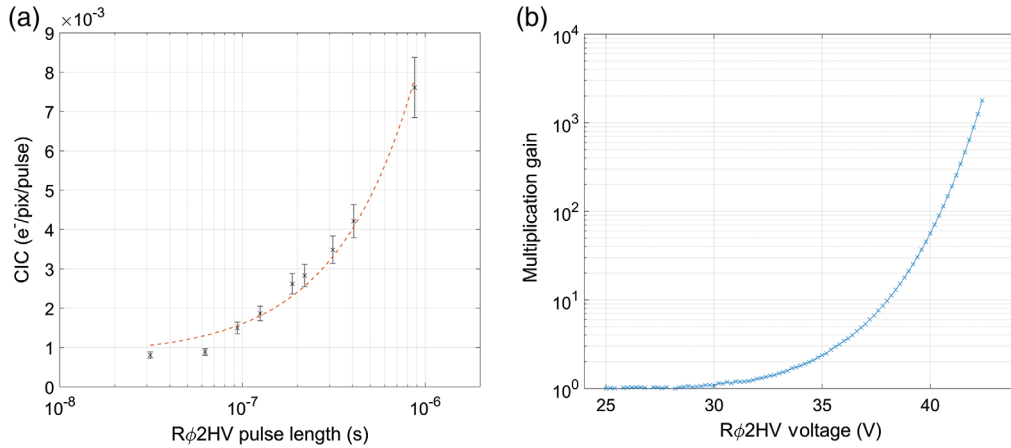
**Fig. 20** EM register CIC profile for R $\phi$ 2HV operated at 38 V. The CIC is isolated to certain pixels, similar to that seen for the image area defects.

values in excess of  $\times 1000$  were achieved with R $\phi$ 2HV in excess of 42 V. This measurement was performed at 165 K with  $\phi$ DC biased at 3 V.

CIC generated in the EM register has a different impact on the total noise performance of the detector when compared to signal generated elsewhere in the device. Any CIC generated partially through the EM register will not experience the full EM gain and is therefore more likely to fall beneath the  $5\sigma$  detection threshold in photon-counting mode. CIC defects toward the end of the register therefore impact performance less than those present at the start of the register. This means if the total CIC is dominated by the EM register component then there may be measurable device-to-device variation in CIC that is dependent on the distribution of these defects. The average EM gain,  $G$ , is a function of the average gain per element,  $g$ , and the number of elements the charge is transferred through,  $n$ :



**Fig. 21** (a) Enlarged region of Fig. 20 showing the effect of clock amplitude on the signal distribution. (b) The average CIC generated across the EM register as a function of clock amplitude.



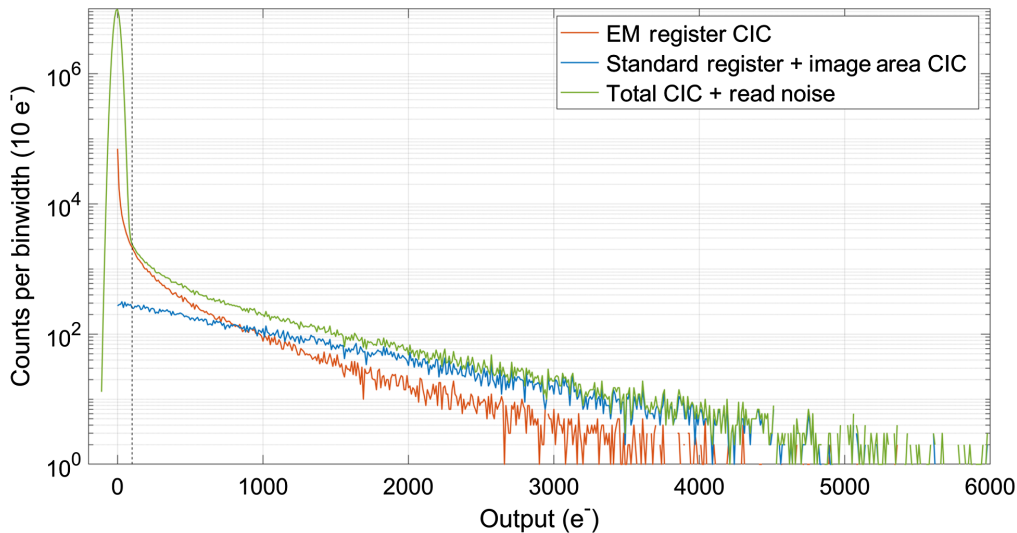
**Fig. 22** (a) EM Register CIC as a function of R $\phi$ 2HV pulse length. The relationship was found to be approximately linear, with a factor of  $\times 10$  reduction in pulse length reducing CIC by the same amount. (b) EM gain measurement for the same device where EM CIC was investigated.

$$G = g^n. \quad (1)$$

For simplicity, we assume that only a single electron of CIC is generated by any one pulse but with a probability that varies according to the location of the CIC defects. The output probability distribution for a single electron through the gain register with average gain  $G$  is

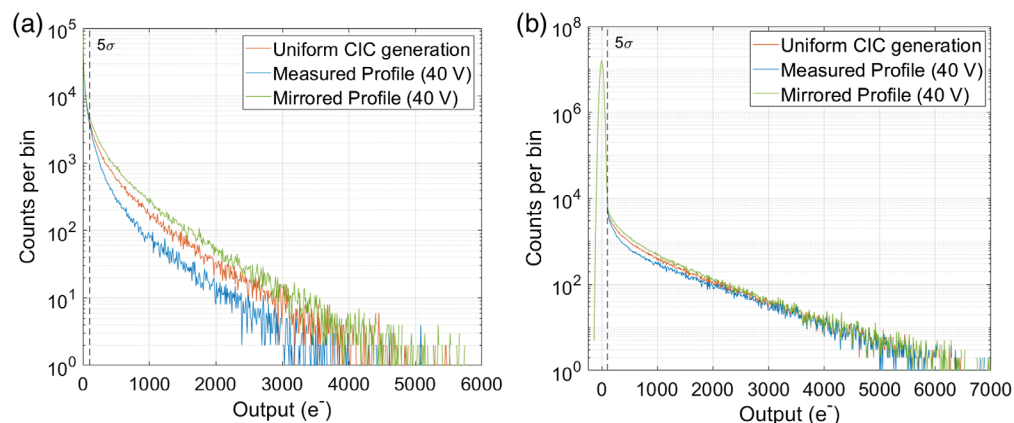
$$p(x) = \frac{e^{-x}}{G}. \quad (2)$$

Through this relationship, it is possible to estimate the functional form of EM CIC by simply applying the EM gain that any given CIC event will experience as it travels through the remaining fraction of the EM register. Figure 23 shows a simulated device output that consists of the read noise of the detector, CIC generated in the standard register and image section, and CIC generated within the EM register at random. For this simulation, it was assumed that 85% of the measured CIC was due to the EM register, based on the results described by Downing et al.<sup>15</sup>. The EM CIC dominates at the lowest signal levels and distorts the output distribution from the expected linear behavior (Eq. 2) approaching the detection threshold. Since EM gain calibration in photon-counting mode is reliant upon this linearity, care must be taken to consider this effect for cases where EM CIC dominates noise in the EMCCD. Figure 23 assumed uniform CIC



**Fig. 23** Simulated output distribution for an EMCCD operating at an EM gain of  $\times 1000$  with total CIC of  $4 \times 10^{-3} e^-/\text{pix}/\text{frame}$ , assuming uniform CIC generation in each element. 85% of the total number of CIC events were generated in the EM register, and these experienced varying levels of gain depending upon where they were generated. The output distribution of EM CIC follows a different relationship to that of CIC generated elsewhere in the device, and this can skew the measured output distribution when EM CIC is the dominant component. This effect should be considered when devices are calibrated in photon-counting mode.

generation, however, this study has shown that this is not a valid assumption, and so Fig. 24 shows the result where CIC generation is assumed to be nonuniform, for the specific defect distribution shown in Fig. 20, and a “mirrored” case where more prominent defects are now located toward the start of the register. There is a visible difference in the form of the output distribution, and imposing a  $5\sigma$  threshold on the simulated data shows that the measured CIC in within an image could differ dramatically depending on the location of these defects (Table 2). The greater the contribution of EM CIC to the total CIC, the higher the variation one may expect. If the standard register CIC or parallel CIC dominates performance, the potential variance due to



**Fig. 24** (a) Simulated output distribution for an EMCCD operating at EM gain of  $\times 1000$  with total CIC of  $4 \times 10^{-3} e^-/\text{pix}/\text{frame}$  assuming uniform CIC generation in each element, the case shown by Fig. 20 and a mirrored profile of Fig. 20 where more high-intensity defects are located towards the start of the register. The more defects near the start of the register, the higher the total detected EM CIC contribution. (b) Output distribution when the same total amount of CIC is considered, with 85% generated in the EM register and 15% generated in the standard register. The change in the EM register CIC component changes the shape of the output distribution, and this should be considered when using these profiles to calibrate the EM gain using photon-counted images.



**Table 2** EM register CIC and total CIC when a  $5\sigma$  threshold is applied to the distributions in Fig. 24.  $20 e^-$  of read noise was assumed. Note the total is below the  $4 \times 10^{-3} e^-/\text{pix}/\text{frame}$  input value since a fraction of signal is not multiplied above the detection threshold.

	EM register CIC ( $e^-/\text{pix}/\text{frame}$ )	Total CIC ( $e^-/\text{pix}/\text{frame}$ )
Uniform CIC generation	$8.96 \times 10^{-4}$	$1.44 \times 10^{-3}$
Measured profile (40 V)	$5.76 \times 10^{-4}$	$1.12 \times 10^{-3}$
Mirrored profile (40 V)	$1.20 \times 10^{-3}$	$1.74 \times 10^{-3}$

the location of these defects will not be noticeable. In short, the apparent nonuniformity of EM register CIC has implications for calibration and device-device performance variation in photon counting mode when EM register CIC is the dominant noise component.

For the image area defects, the generation region was implied to be a region of high field between polysilicon gates. The situation is expected to be no different for the EM register, as the interpoly oxides among the  $R\phi 2HV$ ,  $\phi DC$ , and  $R\phi 3$  gates will experience electric fields in excess of  $10^8$  V/m when operating with high EM gain. In normal operation,  $\phi DC$  is biased at a fixed value in the range of 2 to 5 V, while  $R\phi 3$  moves between the 0- and 10-V range. These conditions mean that the highest electric fields within the EM register are not between  $R\phi 2HV$  and  $\phi DC$ , but between  $R\phi 2HV$  and  $R\phi 3$  throughout the multiplication process. While the difference in voltage between each side of  $R\phi 2HV$  is small, the dependence of CIC on the field has been shown to be exponential in all cases, and so the primary CIC generation region is expected to lie between the  $R\phi 2HV$  and  $R\phi 3$  gates. Evidence for this was found in that the signal profiles of the CIC defects were skewed toward  $R\phi 3$  [Fig. 21(a)]. However, this may also be due to poor CTE from the backward clocking of the EM register, since this is not an intended operating mode of the device. A possible mitigation of EM register CIC highlighted by this method is reducing  $\phi DC$  as much as practically possible while maintaining good CTE. If  $\phi DC$  is reduced, a smaller value of  $R\phi 2HV$  is required to achieve a certain EM gain, and so the field between  $R\phi 2HV$  and  $R\phi 3$  is also reduced. The same effect can be achieved through raising of the  $R\phi 3$  low level at certain points during register clocking, however, this may negatively impact CTE if not carefully implemented.

### 3.3 Photon-Counting Mode Optimization

While the previous two methods were useful for highlighting trends in CIC generation, they do not provide representative performance values since they were not implemented with the device imaging as it would in a true photon-counting application. Measurements in photon-counting mode were required to implement the suggestions made in the previous sections and validate whether any reduction in CIC was possible through implementation of new clocking and optimization techniques. The results so far have shown that for parallel CIC, operating the device in NIMO provided the greatest level of mitigation, followed by reduction in clock amplitudes and operating at faster pixel rates. The serial register is operated in NIMO by default and so amplitude reduction remained the primary mitigation technique. The previous measurements implied most of the CIC appears to come from the EM register (Figs. 19–21), and so particular attention was paid to reducing the  $R\phi 2HV$  clock amplitude, for which two methods were implemented.

The first was to reduce the baseline read noise of the system. At the 1-MHz serial speed used in this study, the theoretical minimum read noise achievable with the sensor is  $14 e^-$  (RMS).<sup>5</sup> For photon counting with a DQE > 90%, this results in an EM gain requirement of  $\times 700$ . Values between  $20 e^-$  and  $22 e^-$  were achievable on the equipment used for this study, resulting in EM gains of approximately  $\times 1000$  to meet the DQE requirement. The reduction in read noise, and hence required EM gain, resulted in a lower  $R\phi 2HV$  amplitude. The exact reduction in required HV amplitude can vary according to the device; however, moving from an EM gain of  $\times 4000$  to  $\times 1000$  can equate to a reduction of 1 V—a significant difference given the exponential dependence of CIC on clock amplitude.



The second method was to reduce the  $\phi_{DC}$  bias as much as practically possible while maintaining adequate CTE. The electric field responsible for the multiplication process is a result of the difference between  $R\phi_{2HV}$  and  $\phi_{DC}$ , and so lowering  $\phi_{DC}$  reduces the required  $R\phi_{2HV}$  for a given EM gain. This optimization does not reduce the field between  $R\phi_{2HV}$  and  $\phi_{DC}$ ; however, it does reduce the field between  $R\phi_{2HV}$  and  $R\phi_3$  and can therefore reduce CIC generated in this region. The lowest possible  $\phi_{DC}$  bias varied according to the device under test, and higher device temperatures were found to correlate with a lower limit for the  $\phi_{DC}$  bias. This is believed to be due to the transfer mechanism beneath this phase; as the  $R\phi_1$  phase is brought low, charge flows beneath  $\phi_{DC}$  predominantly due to carrier drift. The strength of carrier drift will decrease as the device temperature decreases, and a higher  $\phi_{DC}$  bias is required to compensate. For the same reason, the operation at faster pixel rates may necessitate a higher  $\phi_{DC}$  bias to maintain CTE; however, this was not investigated.

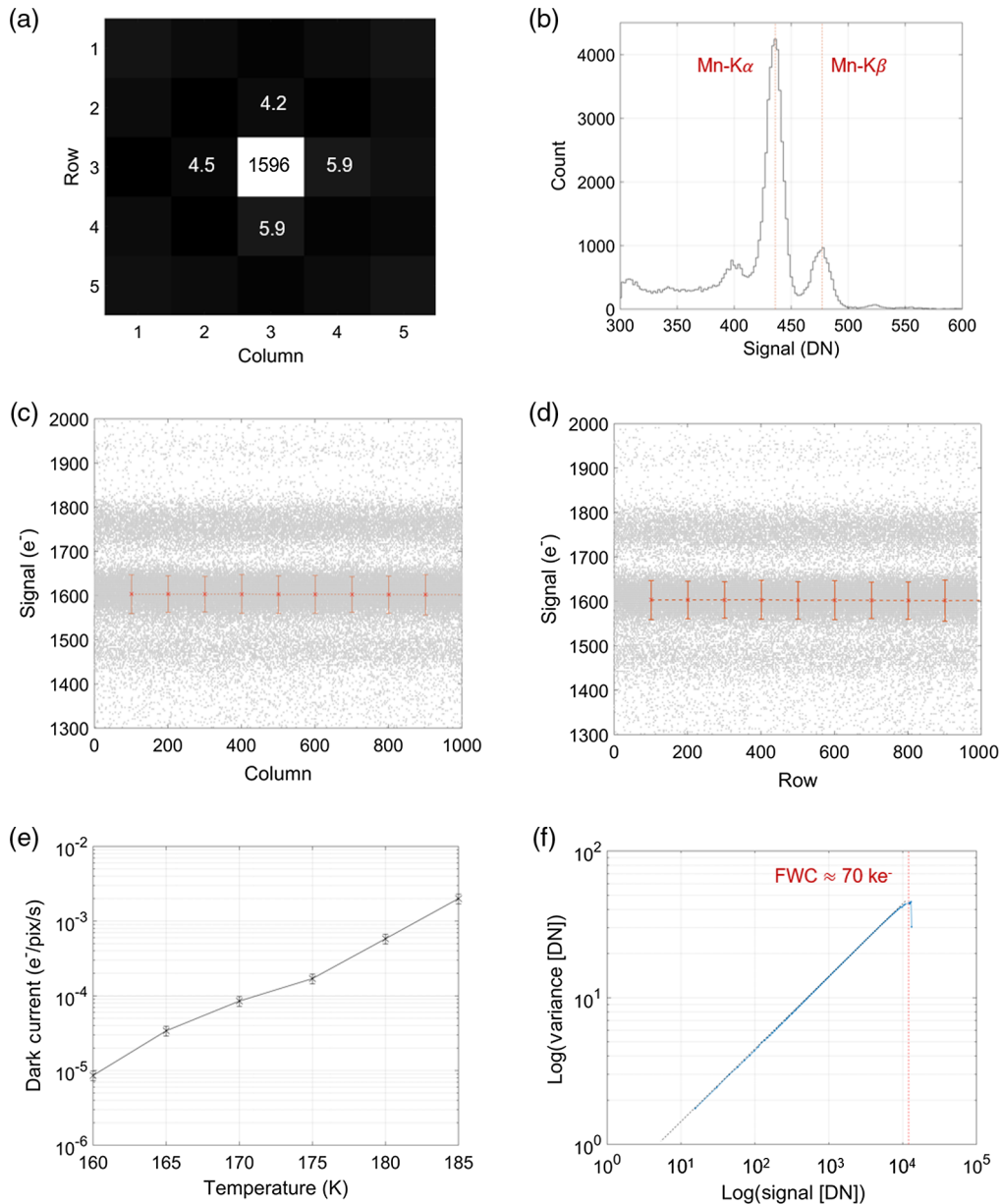
The amplitudes of the standard serial register were reduced as much as possible, and the rising edge of the serial clocks was controlled to reduce CIC generation. This was performed by attaching variable load resistors in series with each of the serial clock lines. The resistance to each line could then be tuned as needed to control the rising edge of the clock. The tuning was often repeated following an adjustment to the clock amplitudes to achieve the best possible CTE and lowest CIC. Changes in device temperature also required the clock edges to be tuned once more to either improve CTE or lower CIC. Often, a decrease in temperature required a slight increase in the  $\phi_{DC}$  level that then required some tuning of the rising edge of the serial clocks as a result.  $R\phi_{2HV}$  sometimes required an increase due to recover the loss in EM gain through a higher  $\phi_{DC}$  or an increase in temperature. The EM gain could also vary slightly as the  $R\phi_1$  clock was tuned, and so each device was constantly calibrated to be sure of the exact EM gain before any measurements were made.

In summary, the optimization procedure was as follows:

1. Reduce the system read noise as much as practically possible for a given device. Careful attention was paid to the reset pulse that was made as short as possible to maximize the sample time available for CDS circuitry.
2. Lower the  $\phi_{DC}$  bias amplitude as much as practically possible while maintaining adequate CTE. Values used in this study ranged from 1.5 to 2.2 V, depending on device and operating temperature.
3. Lower the register clock amplitudes and parallel clock amplitudes while maintaining adequate CTE. At 1 MHz, it was possible to operate with serial clock amplitudes as low as 8.5 V for some devices. Between 9.5 and 10 V was typical for parallel amplitudes operating at 1 MHz in NIMO.
4. Tune the rising edge of the clock using load resistors while monitoring CTE and CIC.

Often, tuning the rising edge of the clock allowed a lower clock amplitude for one or more of the phases. This would in turn facilitate a lowering of the  $\phi_{DC}$  bias. Steps 2 to 4 were therefore iterative in nature; however, after a few cycles the changes in performance were small. Three devices were operated in photon-counting mode at temperatures ranging from 155 to 185 K. Photon transfer curves were obtained to demonstrate device linearity and image full well capacity (FWC).  $^{55}\text{Fe}$  spectra were obtained to demonstrate adequate parallel and serial CTE, and the dark current was also measured at each temperature. The devices were typically operated in frame transfer mode, resulting in a  $1\text{k} \times 1\text{k}$  readout area. At times the entire image and serial register were read out with overscan to give better separation of parallel and serial CIC, here frames were  $\sim 2\text{k} \times 2\text{k}$  in size. The CIC results for each mode were consistent.

Figure 25 shows measurements of basic performance characteristics on one of the devices (12231-21-9) optimized for photon-counting mode. These measurements were made with no EM gain applied, except for dark current that was measured in photon-counting mode at high gain. Image FWC and parallel and serial CTE were found to be as expected. The dark current values are in-line with other reported values for the CCD201-20 measured at similar temperatures. The same measurements were performed on 11281-22-15 and 12231-21-10, where the performance was similar.



**Fig. 25** Performance measurements from device 12231-21-9. (a) The “average”  $^{55}\text{Fe}$  event from single events selected for CTE analysis. The signal level in electrons is labeled for the central and surrounding pixels. (b) An  $^{55}\text{Fe}$  spectra with the Mn-K $\alpha$  and Mn-K $\beta$  peaks labeled. (c) and (d) The parallel and serial  $^{55}\text{Fe}$  CTE profiles, with CTI measured as better than  $3 \times 10^{-6}$  in each direction. (e) and (f) a PTC, with measured image FWC in excess of 60,000 e $^-$ , and NIMO dark current measured in photon-counting mode as a function of temperature.

Tables 3–5 present the parallel and serial CIC measurements in photon-counting mode for devices 12231-21-9, 11281-22-15, and 12231-21-10. For 12231-21-9, the lowest parallel CIC was measured to be  $\sim 5 \times 10^{-4}$  e $^-$ /pix/frame in NIMO, with a frequency of 1 MHz and a clock swing of 10 V. There is an apparent rise in parallel CIC with temperature; however, this is thought to be due to the dark current accumulated within a single frame (read time 1.1 s) that becomes noticeable at higher temperatures. Serial CIC was seen to vary between 2 and  $3 \times 10^{-3}$  e $^-$ /pix/frame. Device optimization was repeated at each temperature and this impacted serial CIC value significantly. As the temperature was raised, it was possible to operate the device with a lower  $\phi_{\text{DC}}$  value, meaning  $R\phi_{2\text{HV}}$  could be lowered. This meant, however, the rising edges of the clocks needed to be retuned. For the same reason, the EM gain was not

**Table 3** Summary of the results obtained from device 12231-21-9 at different temperatures, operating at 1-MHz serial speed and 1-MHz parallel transfer frequency in NIMO. The parallel CIC values include any dark current that would have been accumulated during the frame readout time;  $\sim 1.1$  s for these test conditions, this explains the apparent increase in parallel CIC with device temperature.

$T$ (K)	Read noise ( $e^-$ )	EM gain	$G/\sigma$	PCIC ( $e^-/\text{pix}/\text{frame}$ )	SCIC ( $e^-/\text{pix}/\text{frame}$ )	Dark current ( $e^-/\text{pix}/\text{s}$ )	Bad event fraction (%)
160	$22.0 \pm 0.1$	$1165 \pm 100$	$53 \pm 5$	$(5.0 \pm 1.5) \times 10^{-4}$	$(2.0 \pm 0.1) \times 10^{-3}$	$(8.6 \pm 4.2) \times 10^{-6}$	$5.2 \pm 0.44$
165	$22.0 \pm 0.1$	$1230 \pm 110$	$56 \pm 6$	$(5.0 \pm 1.8) \times 10^{-4}$	$(1.9 \pm 0.2) \times 10^{-3}$	$(3.4 \pm 0.3) \times 10^{-5}$	$4.2 \pm 0.67$
170	$20.9 \pm 0.2$	$1046 \pm 80$	$50 \pm 5$	$(8.0 \pm 1.3) \times 10^{-4}$	$(3.0 \pm 0.2) \times 10^{-3}$	$(8.5 \pm 0.2) \times 10^{-5}$	$4.5 \pm 0.45$
175	$19.8 \pm 0.1$	$954 \pm 51$	$48 \pm 3$	$(9.0 \pm 3.3) \times 10^{-4}$	$(2.7 \pm 0.2) \times 10^{-3}$	$(1.7 \pm 0.1) \times 10^{-4}$	$4.6 \pm 0.50$
180	$22.5 \pm 0.1$	$750 \pm 30$	$33 \pm 2$	$(1.5 \pm 0.2) \times 10^{-3}$	$(2.6 \pm 0.2) \times 10^{-3}$	$(5.8 \pm 0.1) \times 10^{-4}$	$4.2 \pm 0.30$
185	$22.0 \pm 0.3$	$1194 \pm 110$	$55 \pm 5$	$(2.0 \pm 0.1) \times 10^{-3}$	$(2.4 \pm 0.1) \times 10^{-3}$	$(1.1 \pm 0.1) \times 10^{-3}$	$3.3 \pm 0.41$

**Table 4** Summary of the results obtained from device 11281-22-15 at different temperatures, operating at 1-MHz serial speed and 1-MHz parallel transfer frequency in NIMO.

$T$ (K)	Read noise ( $e^-$ )	EM gain	$G/\sigma$	PCIC ( $e^-/\text{pix}/\text{frame}$ )	SCIC ( $e^-/\text{pix}/\text{frame}$ )	Dark current ( $e^-/\text{pix}/\text{s}$ )	Bad event fraction (%)
160	$20.9 \pm 0.1$	$1400 \pm 120$	$67 \pm 7$	$(3.0 \pm 2.0) \times 10^{-4}$	$(9.9 \pm 3.0) \times 10^{-4}$	Not measured	$3.0 \pm 1.2$
165	$20.7 \pm 0.1$	$1200 \pm 110$	$58 \pm 6$	$(2.2 \pm 2.5) \times 10^{-4}$	$(6.6 \pm 2.5) \times 10^{-4}$	$(2.4 \pm 0.3) \times 10^{-5}$	$2.9 \pm 1.2$
170	$20.4 \pm 0.1$	$1188 \pm 110$	$58 \pm 6$	$(2.9 \pm 2.2) \times 10^{-4}$	$(9.1 \pm 2.7) \times 10^{-4}$	$(4.0 \pm 0.4) \times 10^{-5}$	$3.3 \pm 1.0$
175	$20.3 \pm 0.1$	$1250 \pm 120$	$61 \pm 5$	$(3.5 \pm 2.3) \times 10^{-4}$	$(9.1 \pm 2.8) \times 10^{-4}$	$(8.1 \pm 0.5) \times 10^{-5}$	$3.0 \pm 1.0$
180	$20.3 \pm 0.1$	$1327 \pm 130$	$65 \pm 7$	$(7.3 \pm 2.3) \times 10^{-4}$	$(1.1 \pm 0.3) \times 10^{-3}$	$(2.2 \pm 0.1) \times 10^{-4}$	$2.7 \pm 0.7$
185	$20.1 \pm 0.1$	$1480 \pm 150$	$74 \pm 8$	$(2.9 \pm 0.2) \times 10^{-3}$	$(1.5 \pm 0.2) \times 10^{-3}$	$(4.5 \pm 0.1) \times 10^{-4}$	$5.5 \pm 0.5$

**Table 5** Summary of results obtained from device 12231-21-10 at different temperatures, operating at 1 MHz serial speed and 1 MHz parallel transfer frequency in NIMO.

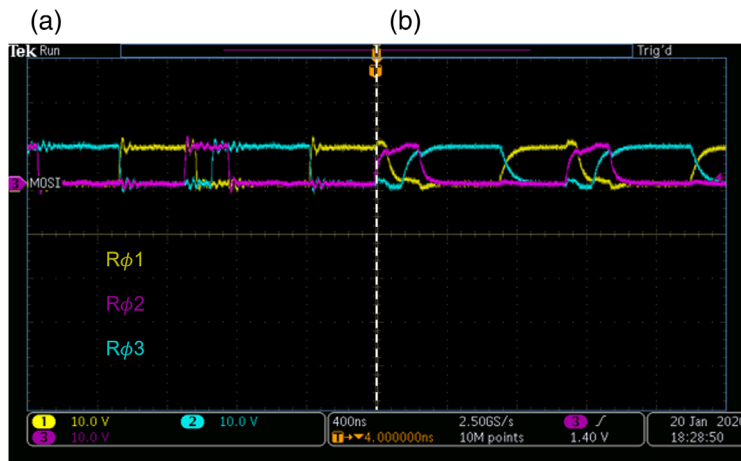
$T$ (K)	Read noise ( $e^-$ )	EM gain	$G/\sigma$	PCIC ( $e^-/\text{pix}/\text{frame}$ )	SCIC ( $e^-/\text{pix}/\text{frame}$ )	Dark current ( $e^-/\text{pix}/\text{s}$ )	Bad event fraction (%)
155	$22.6 \pm 0.2$	$1680 \pm 150$	$75 \pm 8$	$(1.9 \pm 0.7) \times 10^{-4}$	$(5.0 \pm 2.1) \times 10^{-3}$	$(9.6 \pm 6.8) \times 10^{-6}$	$2.5 \pm 0.3$
160	$22.2 \pm 0.2$	$1450 \pm 120$	$65 \pm 5$	$(2.0 \pm 1.1) \times 10^{-4}$	$(5.0 \pm 2.2) \times 10^{-4}$	$(9.90 \pm 7.6) \times 10^{-6}$	$2.1 \pm 0.3$
165	$21.4 \pm 0.2$	$1428 \pm 120$	$66 \pm 6$	$(2.6 \pm 1.3) \times 10^{-4}$	$(5.8 \pm 2.3) \times 10^{-4}$	$(2.8 \pm 1.2) \times 10^{-5}$	$1.4 \pm 0.2$
170	$21.6 \pm 0.1$	$1495 \pm 120$	$69 \pm 7$	$(2.5 \pm 1.5) \times 10^{-4}$	$(4.1 \pm 2.3) \times 10^{-4}$	$(2.8 \pm 0.4) \times 10^{-5}$	$1.0 \pm 0.2$
175	$21.4 \pm 0.2$	$1450 \pm 110$	$67 \pm 7$	$(3.4 \pm 1.0) \times 10^{-4}$	$(5.0 \pm 2.2) \times 10^{-4}$	$(4.72 \pm 0.2) \times 10^{-5}$	$0.2 \pm 0.1$

kept constant at each temperature but set at a target of  $>90\%$  DQE. The exception was the measurement at 180 K where the device was operated with a lower EM gain than intended and less time was spent tuning the waveforms for low CIC. CTE was quantified using the concept of a “bad event” first introduced by Daigle et al.,<sup>6</sup> where a bad event constitutes a photon-counted pixel trailing another. The target was 5% or below. At 160 K, 5.2% was the absolute minimum

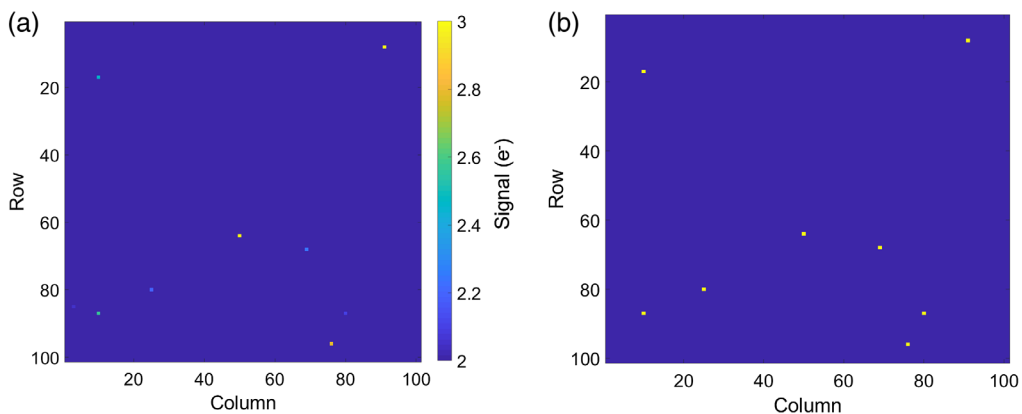
value possible for this device. At higher temperatures, better CTE was possible but at the expense of higher serial CIC.

Device 11281-22-15 (Table 4) exhibited improved performance compared with 12231-21-9 across all device temperatures. The parallel section was clocked at 9.5 V while maintaining FWC and CTE. It was also possible to operate the serial register with lower  $\phi_{DC}$  values than 12231-21-9. These characteristics, combined with a slightly reduced read noise, allowed much higher DQE values than originally anticipated, while maintaining low total background charge and good CTE. The lowest total CIC value was  $(8.8 \pm 0.7) \times 10^{-4} e^-/\text{pix}/s$  for this device, obtained at 165 K.

Device 12231-21-10 (Table 5) performed best out of the three devices tested, with the total CIC remaining below  $1 \times 10^{-3} e^-/\text{pix}/\text{frame}$  for all temperature tested. The charge transfer performance of this device was also superior, with a significantly lower fraction of bad events even at the lowest operating temperatures. It was charge transfer performance that limited the CIC reduction in each of the other devices; any further reduction in register clock amplitude or  $\phi_{DC}$  level pushed the bad event fraction above the 5% limit for this study. This device, however, tolerated lower amplitudes with very little CTE penalty with a corresponding reduction in serial CIC. This device also exhibited particularly low dark signal, and it is unclear whether these measurements are correlated, but worth noting (Figs. 26 and 27).



**Fig. 26** Example of waveform optimization for device 12231-21-10. (a) Initially the serial waveforms had sharp edges, overshoot, and ringing on each line. (b) Following the optimization and measurement at 155 K.



**Fig. 27** Example image from device 12231-21-10 obtained at 155 K. (a) Raw image and (b) photon-counted image.

## 4 Methods for Further Reduction of CIC

One of the key explanations for CIC reduction in this study is a reduction in the baseline read noise. This, in turn, led to a reduction in the required EM gain, leading to lower serial CIC and improvements in CTE at lower temperatures. Further reduction in read noise through modification of device design therefore appears to be a relatively straightforward way of reducing CIC in future photon-counting EMCCD instruments.

The read noise of the detector is dependent upon the amplifier design and the pixel rate. The commercially available CCD97 and CCD201 Teledyne-e2v EMCCDs manufactured have both a HR amplifier connected to the standard CCD output and a large signal (LS) output connected to the end of the multiplication register. The LS output has a low sense node capacitance, resulting in low responsivity:  $1.1 \mu\text{V}/e^-$  for the CCD97 and  $1.4 \mu\text{V}/e^-$  for the CCD201, with the advantage of high charge handling capacity (up to  $\approx 10^6 e^-$ ) and high bandwidth. This design provides a large degree of flexibility for operation; analog mode can still be used with EM gain and maintain a reasonable dynamic range at high pixel rates. The penalty, however, is higher than necessary read noise for applications that do not require either high output signals and/or the maximum pixel rate. For the photon-counting applications, there is a potential for substantial performance improvements through tailoring of the output circuit to provide the maximum sensitivity while maintaining adequate bandwidth and charge handling capacity for the application. For the example of a CCD201 operating at 1 MHz, the standard LS output provides far greater bandwidth than is necessary at the expense of the higher theoretical read noise of  $\approx 14 e^-$  RMS. Substitution of the standard HR output in its place reduces the theoretical read noise to  $6 e^-$  RMS (1% settling) at the same pixel rate. For a DQE requirement of 90%, the required EM gain now shifts down to just  $\times 300$ , likely providing a further reduction in CIC and improvement in serial CTE, as already evidenced by this study.

Not all applications can operate at lower serial speeds. The discussion here has so far been limited to two-stage output circuits with buried channel transistors. At high frequencies, white noise dominates, and so surface channel transistors can be used for faster switching speeds with no noise penalty compared with the buried channel counterpart. A three-stage DC-coupled output circuit is present on the Teledyne-e2v CCD351 with a responsivity of  $3.1 \mu\text{V}/e^-$  and theoretical noise of  $50 e^-$  RMS at the output data rate of 37 MHz. This output design offers a compromise between high speed operation and lower read noise; however, the disadvantage is that these output circuits are known to exhibit significant light emission and so require careful optimization of operating voltages in photon-counting mode. Nonetheless, appropriate placement and operation of these types of output amplifier may provide the opportunity for further CIC reduction if higher pixel rates are a necessity.

The second method used to reduce CIC was a reduction in the field between  $R\phi 3$  and  $R\phi 2\text{HV}$  through reduction in the  $\phi\text{DC}$  voltage. This should in principle reduce the component of EM register CIC significantly. It was not possible to fully verify whether this technique was responsible for the low levels of CIC reported here, or whether most of the benefit was due to read noise reduction. However, each method shows promise as means for CIC reduction in photon-counting mode.

## 5 Summary

This study has verified many of the known relationships between CIC and operating parameters of EMCCDs, including temperature, clock frequency, and clock amplitude. It has also highlighted a new mechanism for CIC generation in NIMO, believed to be light emission from the same hot carriers responsible for CIC generation in IMO. These defects were then also found to be present within the EMCCD gain register and appear to dominate CIC generation when operating at high gain.

Optimization of devices in photon-counting mode allowed CIC levels comparable with the best reported values in the literature, operating at 1-MHz serial speed and at a wide range of device temperatures. These results suggest EMCCDs can be operated across a wide range of operating conditions (temperatures and readout speeds) provided the readout noise of the detector is reduced to the lowest possible levels and that clock waveforms are optimized appropriately.

Moving forward, further verification of these optimization techniques and results is required on other camera systems with other devices and ideally across a wider range of readout speeds.

This study was limited to three devices in photon-counting mode, operating at a single serial speed, mainly because the optimization process was time consuming and needed to be repeated at each device temperature. We also note that no optical source was pointed at the device in photon-counting mode, and this is an important performance verification step that could not be performed with the experimental setup used in this study. However, photon transfer curves,  $^{55}\text{Fe}$  CTE measurements, and the presence of cosmic rays within images all indicated imaging performance was as-expected. An independent verification of the expected DQE through calibrated optical light sources is an important future step. With additional verification, and the implementation of additional measures to reduce CIC as suggested here, it may be possible to reduce CIC to levels where the noise performance of these devices is limited only by thermal dark current generation rate for most applications. The increase in sensitivity and flexibility in readout speed, operating temperature, and frame rate would allow additional future applications to benefit from the extraordinary sensitivity of these devices.

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**Nathan Bush** is a postdoctoral scholar at the NASA Jet Propulsion Laboratory, working on the flight implementation of EMCCDs for the Roman Coronagraph Instrument. Prior to this, he was

a research fellow at the Centre for Electronic Imaging, Open University, UK, where he worked on the development and characterization of customized image sensors for space applications.

**Julian Heymes** is a detector scientist at the CEI, the Open University, United Kingdom. He studied microelectronics at the Université de Strasbourg, France, before completing his PhD in physics at the same university in 2018, studying the depletion in CMOS pixel sensors. He is interested in the development and testing of high sensitivity silicon detectors optimised for scientific applications, especially in the ultraviolet and soft X-ray spectral ranges.

**David Hall** is a lecturer in physical sciences at the Open University. Over the past decade he has worked on the simulation and analysis of radiation induced damage to charge transfer in CCDs for the ESA Euclid and Gaia missions, the joint ESA and Chinese Academy of Sciences SMILE mission and NASA's WFIRST mission. He has developed new methods to characterise radiation-induced defects ("traps") in silicon, leading to a more fundamental understanding of how radiation damage affects charge transfer in CCDs.

**Andrew Holland** is a professor of electro-optics at the Open University, UK, and leads the Centre for Electronic Imaging (CEI). He is an expert in detector physics and has worked on the development of a number of successful space instruments. He has a wealth of knowledge and experience advising on instrument-related issues, in particular radiation damage effects and the prediction of orbital performance.

**Douglas Jordan** is the characterisation team leader at Teledyne e2v responsible for delivering characterisation activities for new CCD and CMOS imaging devices. He has 15 years of silicon R&D background, nine of which are on imaging devices at Teledyne e2v. He holds three international patents in silicon substrate technologies and has presented at several international conferences on both imaging devices and silicon physics. He is a Chartered Engineer and a Visiting Fellow at Centre for Electronic Imaging (Open University).