A Wideband Signal Conditioning System for High Voltage Measurements using a Transconductance Topology

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DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously in its entirety or in part been submitted at any university for a degree.

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SUMMARY

Recent research has shown that standard substation capacitive voltage transformers (CVTs) and current transformers (CTs) can be used for the measurement of wideband high voltage phenomena by employing these apparatus in a transconductance topology. With this topology the voltage waveform can be obtained by integration of the ground return current in the earth straps of the CVT and the CT. This technique does, however, impose unique requirements on the amplification and integration instrumentation due to large dynamic range requirements and the strict offset specifications required for accurate integration.

This thesis describes a programmable, wideband signal conditioning system for high voltage (HV) measurements using the transconductance topology. A suitable system topology, optimised to reduce the problems usually associated with grounding and electromagnetic interference (EMI) in HV environments, is proposed. This system consists of an analog signal conditioning subsystem, a digital signal conditioning subsystem and a high speed serial fibre-optic link.

The analog signal conditioning subsystem conditions the signals from a sensor to levels suitable for the digitiser of the digital signal conditioning subsystem. The high bandwidth specification of the application made it necessary to consider both discrete and integrated implementation of the analog signal conditioning subsystem. Based on the simulated and laboratory test results of both implementations, the optimum design was chosen for the developed system. The digital signal conditioning subsystem, which performs the integration, as well as the serial optic-fibre link control logic was implemented using programmable logic array (PLA) technology. The digital data is transmitted across the fibre-optic link. This data is then converted back to an analog signal.

Keywords: High voltage measurements, Transconductance topology.

OPSOMMING

Onlangse navorsing het aangetoon dat standaard substasie kapasitiewe spanningstransformators en stroomtransformators gebruik kan word om wyeband hoogspanningsverskynsels te meet deur hierdie apparatuur in 'n transkonduktansie topologie aan te wend. Met hierdie topologie kan die spanningsgolfvorm verkry word deur die integrasie van die aardstrome in die aardverbindings van die kapasitiewe spanningstransformators en stroomtransformators. Hierdie tegniek stel egter unieke vereistes vir die versterkings- en integrasieinstrumentasie te wyte aan groot dinamiese bereik vereistes en die streng afset spesifikasies wat benodig word vir akkurate integrasie.

Hierdie tesis beskryf 'n programmeerbare, wyeband seinkondisioneringstelsel vir hoog-spanningsmetings deur van die transkonduktansie topologie gebruik te maak. 'n Geskikte stelseltopologie, wat geoptimiseer is om probleme, wat gewoonlik met aarding en elektromagnetiese interferensie in hoogspanningsomgewings geassosieer word, te verminder, is voorgestel. Die stelsel bestaan uit 'n analoog seinkondisioneringsubstelsel, 'n digitale seinkondisioneringsubstelsel en 'n hoëspoed seriële optiese vesel koppelvlak.

Die analoog seinkondisioneringsubstelsel kondisioneer die seine vanaf 'n sensor na geskikte vlakke vir die versyferaar van die digitale seinkondisioneringsubstelsel. Die hoë bandwydte spesifikasie van die toepassing vereis die inagneming van beide diskrete en geïntegreerde implementerings van die analoog seinkondisioneringsubstelsel. Gebaseer op gesimuleerde en laboratorium toetsresultate van beide implementerings is die optimale ontwerp vir die ontwikkelde stelsel gekies. Die digitale seinkondisioneringsubstelsel wat die integrasie uitvoer, asook die seriële optiese vesel koppelvlak beheerlogika is geïmplementeer met behulp van programmeerbare logika skikking tegnologie. Die digitale data word gestuur oor die optiese vesel koppelvlak. Hierdie data word dan terug geskakel na 'n analoog sein.

Sleutelwoorde: Hoogspanningsmetings, Transkonduktansie topologie.

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CONTENTS

GLOSSARY OF PRINCIPAL SYMBOLS AND ABBREVIATIONS

Symbols

f_T	Current gain-bandwidth product of the BJT
C_{CE}	Capacitance between collector and emitter of the BJT
i_d	Drain current of the FET
i_g	Gate current of the FET
I_s	Saturation current of the BJT
V_T	Thermal voltage of the BJT
α	Common-base current gain of the BJT
A_d	Transfer function
f_c	Cut-off frequency
C_{ADC}	Internal capacitance of the ADC
REFT	Top reference connection used for external capacitive bypassing of the ADCs internal reference point
REFB	Bottom reference connection used for external capacitive bypassing of the ADCs internal reference point
CM	Common mode output voltage of ADC
V_{max}	Maximum voltage

Abbreviations

CT	Current transformer
CVT	Current voltage tranformer
HV	High voltage
EMI	Electro-magnetic interference
FET	Field effect transistor
BJT	Bipolar junction tansistor
ADC	Analog to digital converter

FPGA	Field programmable gate array
EPLD	Erasable programmable logic device
VHDL	Very high speed integrated circuit hardware description language
MSB	Most significant bit
LSB	Least significant bit
BTC	Binary two's complement
SOB	Straight offset binary
DAC	Digital to analog converter

LIST OF FIGURES

1 PROJECT MOTIVATION AND PROJECT DESCRIPTION

1.1 Introduction

The acquisition and analysis of the high frequency components of power system signals are of importance if one wishes to study the following applications:

- **System monitoring**
  The time- and frequency domain properties of high voltage phenomena are important for analysis of the performance and response of electrical transmission systems and equipment. These phenomena include harmonic distortion, switching transients, lightning impulses, corona noise, partial discharge and carrier signals [8, 17]. This data is also useful for the development of optimum equipment design practises.
- **Substation condition monitoring**
  Recent research has shown that diagnostic analysis and condition monitoring can be done using the time- and frequency domain characteristics of the high frequency electrical noise arising from Current Transformers (CTs) and other substation equipment [2, 18]. There is an increase in the use of wideband properties, especially those of transformers, to determine the condition of power system equipment [3, 5, 6, 22].

The applications mentioned above entail wideband monitoring of the following types of signals:

- The busbar voltages.
- The earth currents associated with an installation.
- Signals retrieved from special transducers e.g. capacitively coupled sensors [15], etc.

The signals of interest have bandwidths that can extend into the MHz range. The measurement of wideband High Voltage (HV) phenomena usually requires the installation

of special wideband transducers such as RC compensated dividers [13]. This is due to the bandlimited frequency responses of standard voltage transducers such as Magnetic Voltage Transformers (MVTs) [7] and Capacitive Voltage Transformers (CVTs) [1, 4, 10, 12, 26]. The installation of special measuring transducers is not only costly and time-consuming, but is also disruptive to normal operations, as de-energisation of the supply at the measuring point is required.

Recent research has shown that standard substation equipment such as the CVTs, CTs, insulator strings and capacitive bushing dividers can be used for the measurement of HV phenomena by employing these devices in non-standard topologies [14, 15, 16, 19, 20, 21, 23, 24, 27, 28, 29]. In some cases bandwidths of up to 500 kHz are achievable. Implementing these devices for voltage measurements is both feasible and easy. After the initial set up, the device can be used as a voltage transducer on a long-term basis.

The most viable technique for wideband HV measurements is to utilise CVTs and CTs in a transconductance topology. This entails sensing and integrating the ground return current in the earth strap of the device to obtain the HV signal [16, 19, 20, 21, 23, 24]. This approach does, however, impose unique requirements on the current sensing and signal conditioning instrumentation [21].

This thesis considers the development of a programmable, wideband hybrid analog and digital signal conditioning system for HV measurements using a CT or a CVT in the transconductance topology. The implementation and testing of the system is discussed and results presented.

1.2 Project motivation

There is growing interest, both locally and internationally, in the importance of measuring wideband phenomena in HV power system environments to monitor the behaviour and condition of substation equipment as well as to monitor HV phenomena. In many utilities across the world research is being done to investigate the responses of power systems and

power system equipment to wideband signals. Investigations are also being carried out on the generation of such signals by power systems and power system equipment. Currently CVTs are used to reduce the power system line voltage to values useable for steady state metering and protection applications. However, the inherent limitations of a narrow linear bandwidth of approximately 400 Hz [21] make them unsuitable for the measurement of wideband phenomena. Presently, a number of HV techniques are being implemented to do wideband HV measurements, e.g. portable RC dividers [9] or capacitive bushing dividers [28]. These techniques, although portable, are expensive and installations procedures are cumbersome and time-consuming. Furthermore, although accurate and reliable, they can not be employed in all transient measurements because of insufficient clearance for voltage dividers. The impracticality and expense incurred in insulating CTs from ground to form capacitive dividers are also drawbacks. Also of importance is the fact that the installation of special measuring transducers disrupts operations as de-enenergisation of the supply at the measuring point is required.

Recently, digital signal processing procedures for spectral estimation, parameter estimation and system identification have developed quite fast. The use of these methods for power systems has, however, been frustrated by the uncertainties about the wideband responses of the available transducers.

There is a niche for the development and evaluation of techniques and technology to use standard substation equipment for wideband voltage measurements on HV power systems. The applications of such research are manifold including the following:

- Monitoring of partial discharge signals to determine the condition of power system equipment.
- Determination of the condition of power system equipment by Frequency Response Analysis (FRA).
- Carrier frequency applications.
- Corona and interference studies.
- Determination of the wideband properties of power system networks and apparatus for

Flexible AC Transmission System (FACTS) applications.

- Determining the condition of power system apparatus by Frequency Response Analysis (FRA).
- Determining the severity and nature of harmonic distortion and high frequency noise.
- Monitoring transient overvoltages occurring across substation apparatus.
- Protection and metering applications.

There are four criteria that form the hub of the proposed field of application. These are harmonic distortion, carrier frequency applications, medium to fast transient phenomena and partial discharge noise. With the currently available technology, the higher harmonics such as those associated with the Flexible AC Transmission System (FACTS) devices with very high switching frequencies, seem unlikely to extend beyond the 100 kHz range [21]. Since the carrier frequency band ranges from 50 kHz to 500 kHz, it is sensible to utilise this study for carrier frequency applications such as EMC studies etc [21]. The medium frequency transient phenomena have time constants ranged from 5 kHz to 50 kHz [21]. Fast transients like lightning induced transients contain frequencies greater than 50 kHz [21]. The 500 kHz frequency bandwidth encompasses partial discharge applications, especially when studied together with the filtering effects of power system networks and apparatus [21]. From the above discussion it is apparent that 500 kHz is a realistic bandwidth for application purposes.

Recent research has shown that standard substation equipment such as CVTs and CTs can be used for the measurement of wideband high voltage phenomena by employing these devices in non-standard topologies [14, 15, 16, 19, 20, 21, 23, 24, 27, 28, 29]. The most viable topology is to use the transducers in a transconductance topology wherein the ground return current of the capacitive divider stack is sensed and integrated to obtain a signal representing the HV input signal [16, 19, 20, 21, 23, 24].

The transconductance topology evolved from the fact that the terminal impedances of the CVTs and CTs, as observed between the HV terminals and ground points, is representative of a capacitor at the frequencies of interest. Fig. 1.1 illustrates this more

clearly with a block diagram representation of the transconductance topology for a CVT.

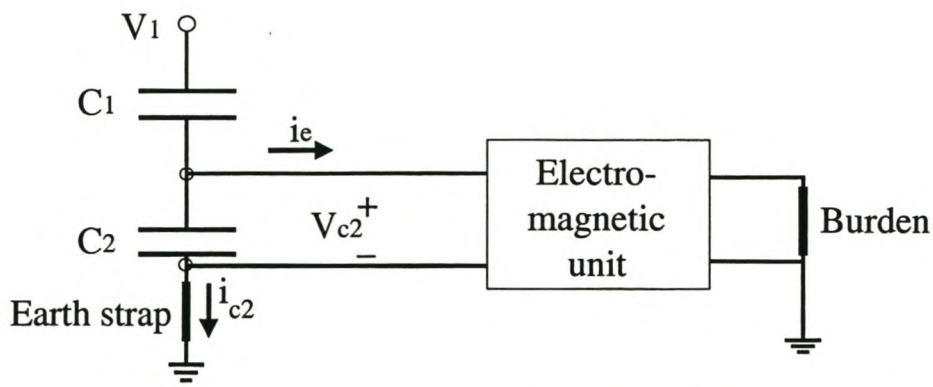


Fig. 1.1: ***Block diagram representation of the transconductance topology for a CVT.***

The HV signal that is of interest is V_1. At the higher frequencies i.e. > 100 Hz., the current i_e becomes negligible and the CVT can be treated as capacitors, C_1 and C_2 in series. The ground return current in the earth strap of the device, i_{c2} can be sensed and integrated to yield the voltage represented by the HV signal V_1.

$$i_{C_2} = C_n \frac{dV_1}{dt}, \qquad (1.1)$$

where $C_n = \frac{C_1 C_2}{C_1 + C_2}$.

Therefore,

$$V_1 = \frac{1}{C_n} \int i_{C_2} dt + c. \qquad (1.2)$$

Fig. 1.2 illustrates an equivalent circuit model for the terminal impedance (the impedance reflected between the HV terminals and the base) of a CT using the transconductance topology [19].

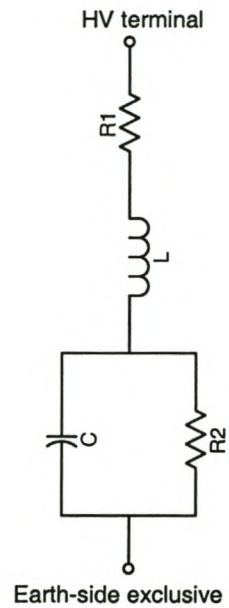


Fig. 1.2: Equivalent circuit model for a CT using the transconductance topology [19].

The parameters of figure 1.2 are

C: The equivalent capacitance reflected between the HV and ground terminals. This capacitance essentially reflects the capacitive coupling between the primary bar conductor and the conducting electric field grading wrapping which is grounded to the base.

L: The equivalent series inductance of the conducting paths associated with the primary bar and the base.

R_1: The resistance of the conducting current paths of the primary bar and the enclosure. This value is expected to be negligible.

R_2: The resistance that reflects the dielectric losses of the insulating material between the primary bar and the electric field grading wrapping. This value is expected to be dependent on frequency.

The conductance of the equivalent circuit is given by the relationship [19]

$$G(s) = \frac{s + \frac{1}{R_2 C}}{L(s^2 + s(\frac{L + R_1 R_2 C}{R_2 LC}) + \frac{R_1 + R_2}{R_2 LC})}. \qquad (1.3)$$

As per laboratory measurements, any measurement using an excitation frequency considerably below the resonant frequency, e.g. up to 100 kHz, will yield a good approximation for C [19].

An approximate value of L can be obtained from the approximate equation for the self resonant frequency of the circuit given by

$$L = \frac{1}{4\pi^2 f_c^2 C}, \qquad (1.4)$$

where f_c represents the resonant frequency of the device.

Using test measurements for a 400 kV CT the values obtained were [19]:

C = 1.082 nF,

f_c = 3 MHz

and L = 2.6 μH.

Obtaining values for R_1 and R_2, especially since it is assumed to be frequency dependent, is more complex and further research is required [21]. The equivalent terminal capacitance of the CT, i.e. C, is necessary to calibrate the voltage measuring arrangement for the transconductance topology. L is required to investigate the bandwidth achievable with a particular CT.

The use of CVTs and CTs for wideband HV measurements have been tested under laboratory [19] as well as field [20] conditions. Favourable results have been obtained for applications such as harmonic distortion, switching impulses, slower lightning impulses and fault waveforms. From a practical perspective, the transconductance topology seems most suitable [19, 20]. The advantages of the transconductance topology can be summarised as follows:

- For frequencies up to approximately 500 kHz, the transconductance ratio of the capacitive divider ground return current and the HV input signal is linear [27]. Judging from the complete transducer model, one can expect a similar result for frequencies up to 500 kHz [26].
- Measurements can be done without having to disrupt the grounding arrangement of the transducer, and without the need for galvanic coupling between the transducer and the data acquisition equipment. This is a non-intrusive measuring technique [27].

There are, however, certain drawbacks of the topology viz,

- Integration of the ground return waveform is required to obtain the HV input waveform [27].
- To conduct accurate non-intrusive sensing of a wideband ground return current, relatively complex current sensing equipment is required [27].
- In the immediate region of the rated frequency (50 Hz) of a CVT, research has shown that the frequency response of the transconductance ratio of the earth return current and the HV input signals exhibits non-linear behaviour [27].

The transconductance topology provides a safe, low cost, reliable and accurate measuring technique for transient and harmonic voltage measurements using existing substation equipment. In addition, there will be a wider availability of wideband, HV signals for the routine investigation of transmission system problems. There will also be a decrease in the number of outages by reducing the requirement of installing special wideband transducers for case studies.

This topology, however, does impose unique requirements on the amplification and integration instrumentation due to the extreme dynamic range of the output signals from the transducers and the strict offset requirements for accurate integration. The lack of suitable and affordable signal conditioning equipment makes the realisation of this topology difficult. The dynamic range, bandwidth and physical requirements imposed by the application makes current equipment unsuitable. This forces the need for the development of dedicated, wideband signal conditioning technology [20, 21].

1.3 Project description

Since the transconductance topology depends on sensing and integrating of the ground return current in the earth strap of the test device, it is important to have the correct signal conditioning instrumentation to exploit this topology successfully. This is due the following:

- The ground return current represents a differentiated version of the HV input signal. Integration of this current is therefore necessary to yield the HV input signal. The integration can be either done using digital or analog techniques.
- High frequency noise is amplified during the differentiation process. This suggests that the signal conditioning circuitry must introduce some form of low-pass filtering.

The transconductance topology requires for the amplification of relatively low-level wideband signal, low pass filtering to remove high frequency noise components and integration and scaling to obtain a signal that is representative of the HV input signal. A feasibility study was under-taken to determine the specifications of the signal conditioning technology [21]. The conclusions of the feasibility study can be summarised as follows:

- **Bandwidth**

  Since the bandwidth limitation of the transducer is approximately 500 kHz [21], this must be the minimum bandwidth of the signal conditioning circuitry. A higher value will ideally be better, and a bandwidth of 10 times the achievable bandwidth of 500 kHz is chosen, i.e. 5 MHz [21].
- **Amplitude accuracy and linearity**

  Using the characteristics of typical CTs, amplitude accuracy and linearity of the order of 3% is achievable over a 500 kHz bandwidth. To ensure that the specifications achievable using the transconductance topology are not substantially decreased, it stands to reason that the signal conditioning circuitry must be at least of the same order. Using availability and affordability as criteria, it is practical to consider accuracy and linearity of 2% [21].
- **Amplification technology**

Since most of the applications do not involve dynamic ranges that are too extreme for 12-bit digitising, linear amplification is sufficient. Applications that involve impulse measurements usually require less accurate amplitude specifications, since the most important is mostly related to the peak value

- **Anti-aliasing filters**

  All applications involving digital signal processing require anti-aliasing filters. Low-pass filtering is also necessary to attenuate the high frequency noise components that are amplified by the differentiating practice of the transducer [21].

- **Sampling rate**

  Since the maximum bandwidth of the system has been established to be of the order of 500 kHz, a sampling frequency of 5 to 10 times that is required to ensure that the Nyquist criterion is adhered to. A sampling rate of at least 5 MHz has been specified [21].

- **Integrator technology**

  There are a few options. Analog or digital integration may be used, but attention must be given to minimising dc offset problems. If the latter is chosen then either hardware or software implementation may be used. Real-time integration is preferred to post-processing integration. Other constraints are affordability, versatility and programmability [21].

- **Galvanic isolation and EMI**

  Galvanic isolation is necessary to eliminate the earthing problems associated with HV environments. Electro-Magnetic Interference (EMI) problems must also be minimised [21].

- **Versatility**

  The output of the signal conditioning system must be suitable to be used as an input for typical commercial equipment [21].

The above specifications will be discussed further in the system overview in Chapter 2.

1.4 Structure of thesis

Chapter 2 presents a system overview. The specifications of the system are discussed based on practical field results. A block diagram of the system topology is proposed and a brief functional description of each subsystem of the system follows. The three subsystems of the proposed topology are the analog signal conditioning subsystem, the digital signal conditioning subsystem and the high speed serial fibre-optic link.

Chapter 3 discusses the analog signal conditioning subsystem. The design of this subsystem is developed and the two methods of implementing it are described. The design process is of an iterative nature and *Pspice* simulations are included to justify the final design choices.

Chapter 4 discusses the development of the digital signal conditioning subsystem. This subsystem consists of an analog-to-digital converter and a Field Programmable Gate Array (FPGA). The major part of this subsystem is implemented using Very high speed integrated circuit Hardware Description Language (VHDL).

Chapter 5 discusses the high speed serial fibre-optic link. The serial link consists of three subsystems viz. the transmitter, the optical fibre and the receiver. Each subsystem is described in detail.

Chapter 6 reviews the test procedures, test results and performance of the developed system. Finally recommendations for further development are suggested.

2 SYSTEM OVERVIEW

2.1 Introduction

This chapter gives an overview of the complete programmable, wideband signal conditioning system by presenting a block diagram representation of the system topology and giving a functional description of each component.

2.2 Block diagram representation of the complete system

Figure 2.1 shows a block diagram representation of the system topology of the wideband signal conditioning system for HV measurements using the transconductance topology.

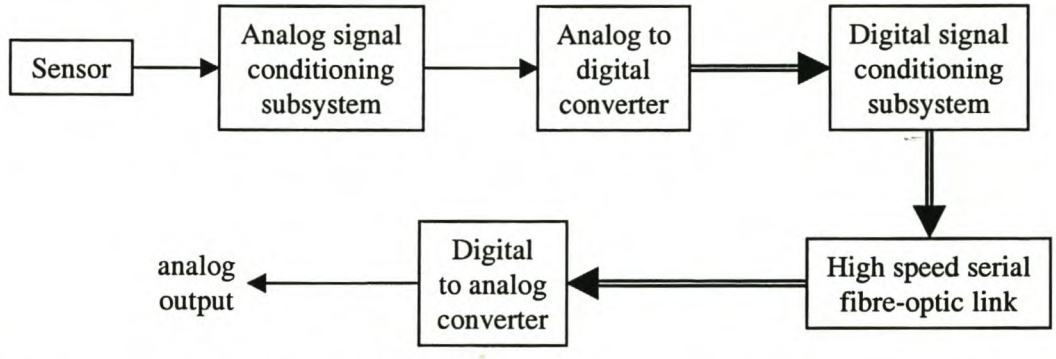


Fig. 2.1: Block diagram representation of the system overview.

The topology consists of a cascade arrangement of an analog signal conditioning subsystem, an Analog-to-Digital Converter (ADC), a digital signal conditioning subsystem, a high speed serial fibre-optic link and a Digital-to-Analog Converter (DAC). Typically the system receives its input from a current sensor located in the earth strap of substation apparatus such as CTs and CVTs.

2.3 Functional description of the subsystems

2.3.1 Analog signal conditioning subsystem

Due to the high bandwidth specifications, serious consideration was given to design this subsystem using discrete components rather than integrated circuits. A successful design using integrated circuits was, however, achieved.

The analog signal conditioning subsystem has a differential input, which reduces the EMI and earthing problems usually associated with HV environments. It serves as a linear amplifier, first-order low pass filter and level shifter that transforms the input signals to signal levels required by the ADC. It delivers a differential output signal centred around 2.25 V to the ADC.

It is in this subsystem that the gain of the system may be varied. The minimum bandwidth aimed for this subsystem is approximately 5 MHz, i.e. 10 times that of the transducer. Filtering is necessary to ensure that the high frequency noise components, which are amplified by the differentiating action of the transducer's terminal capacitance, are attenuated.

The analog signal conditioning subsystem features, at its input, an impedance matching network that has been designed to reflect the same input impedance as a typical oscilloscope. This is because most wideband commercial current sensing equipment is designed to interface to such specifications.

2.3.2 Analog to digital converter

The ADC is located between the analog and digital signal conditioning subsystems. It accepts a differential analog input signal from the analog signal conditioning subsystem and delivers the 12 bit digital output signal to the digital signal conditioning subsystem.

Since the main application of the system is for the measurement of impulse phenomena, the standard lightning impulse has been chosen as the reference impulse in determining the specifications of the system. The standard lightning impulse has an initial rise time of 1μs and a fall time of 50μs [11]. To obtain a resolution of the order of at least 10 sampling points on the rising edge of this impulse, a minimum sampling frequency of 10 MHz is necessary. In practice an even higher sampling rate prior to digital integration of the sampling signal is preferable.

Conversion resolution of 8 bits, that yields amplitude resolution of the order of 1% of the maximum reading, is usually regarded as adequate for impulse measurements. Phenomena involving high frequency noise superimposed on the fundamental waveform, however, require better resolution. Based on the above considerations, as well as factors such as price and availability, an ADC with conversion resolutions of 8 bits and 12 bits, and a maximum conversion speed of 40 MHz was selected.

2.3.3 Digital signal conditioning subsystem

The digital signal conditioning subsystem essentially features a programmable digital integrator, a programmable time-domain decimation processor and a range selector. A brief discussion on integrators follows to substantiate the choice of digital integration.

Analog integrators have offset problems, thus saturating if careful design and/or reset techniques are not applied. Programmable digital integration is preferable since it can be easily adjusted to perform optimally with the offset characteristics of the sensing and measuring system. Digital integration can be implemented using one of two techniques, viz. hardware implementation or software integration. The former involves real-time integration whilst the latter offers post-processing integration.

When using a substation CVT or CT as a voltage measuring device for impulse measurements, a sufficient number of sampling points for the pulse associated with the derivative of the rising edge of the impulse is required for accurate integration. This

enables the integration routine to determine the peak value of the impulse with good accuracy. If the standard lightning impulse, with its initial rise-time of 1μs [11], is used as the reference, a high sampling rate is necessary.

Hardware implementation is advantageous in that the output data sequence from the integrator can be decimated in time thereby reducing the rate of data transmission across the link. Implementation of the digital integrator can be readily done using FPGAs.

A primary drawback of digital integration is the fact that any offset in the analog subsystem signal will be integrated digitally, resulting in an error of which the absolute value increases proportionally to the length of the data sequence. Admittedly good electronic design techniques can minimise these offsets but it remains an important consideration for any waveform having a large dynamic range and a low average value, e.g. the differentiated impulse.

A solution for this problem would be to include digital high-pass or band-pass filtering between the digitizer and the integrator. This will, however, require strict adherence to the Nyquist criteria resulting in the need for anti-aliasing filters. Also if post-processing software rather than real-time hardware is used, sufficient pre-trigger data must be sampled in order to deal with the start-up transient of the filter used.

Digital integration offers the advantages of programmability and versatility. The programmable digital integration circuitry can be adjusted to perform optimally with the offset characteristics of the sensing and measuring system. With regards to using a software or hardware implementation, the less favourable option is digital integration via post-processing software. The severe problems experienced with this method during field measurements confirm this [21].

The entire digital signal conditioning subsystem is implemented on a single FPGA. In addition it also contains the control logic for the sampling clock of the ADC and the rate at which data is transmitted across the serial link. Before transmission across the link, the

data is decimated to reduce the data rate and the range selector reduces the data sequence length.

2.3.4 High speed serial fibre-optic link

The parallel digital output from the digital conditioning subsystem is transmitted serially via a high speed serial fibre-optic link to the DAC. On the transmitting side an encoder converts the parallel data into a serial stream. This link is essential in order to maintain optic isolation, which eliminates the earthing and EMI problems usually associated in HV substations and test environments. On the receiving side a decoder reconstructs the serially transmitted data into parallel data. The transmitter and receiver can work together in a test-mode to test the link as a whole.

2.3.5 Digital to analog converter

The parallel data that appears at the output of the link is converted into analog form via the DAC, thus making it suitable to be used as an input for commercial equipment. The DAC is a 12-bit device that provides outstanding speed and accuracy performance. Since the DAC interfaces between the noisy high speed digital logic and the sensitive analog environment, the output signal must be filtered before use and a de-glitching circuit must be included for precision waveform generation.

2.4 Conclusion

This chapter dealt with the high-level block diagram of the overall system topology. A functional description of each block was given and motivated. The following three chapters considers the development and implementation of each of the subsystems in greater detail.

3 ANALOG SIGNAL CONDITIONING SUBSYSTEM

3.1 Introduction

This chapter discusses the development of the analog signal conditioning subsystem. The primary function of this subsystem is to serve as an amplifier and a 1st order low pass filter that transforms the input signal levels from the sensor to those required by the ADC.

Since bandwidth is the crucial factor, serious consideration was given to the relative advantages and disadvantages of discrete versus integrated implementation of the analog signal conditioning subsystem. Both techniques are investigated, implemented and tested in this chapter, and the optimum one chosen for the final design.

3.2 Discrete implementation of the analog signal conditioning subsystem

3.2.1 Introduction

Although integrated circuits do exist, amplifiers often do not perform very well at such extreme bandwidths. The aim of this exercise was to attempt to design a discrete amplifier that could satisfy the specifications of the system. Figure 3.1 shows a block diagram representation of the discrete implementation of the analog signal conditioning subsystem. The design consists of two stages, viz. the input stage and the amplifier. The input stage is a source follower with high input impedance. The amplifier is the high gain, differential stage.

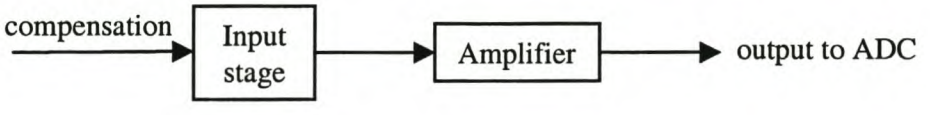


Fig. 3.1: ***Block diagram representation of the discrete implementation of the analog signal conditioning subsystem.***

Each stage of the design was simulated using *Pspice* software to verify biasing points to ensure that the circuit was optimally designed.

3.2.2 Input stage of the discrete implementation

A schematic representation of the complete circuit design for the input stage is shown in figure 3.2. It consists of a Field Effect Transistor (FET), J_1, with biasing performed by Q_1, Q_2 and Q_3 with Q_4 as an emitter follower output buffer. The circuit runs off ±15 V rails.

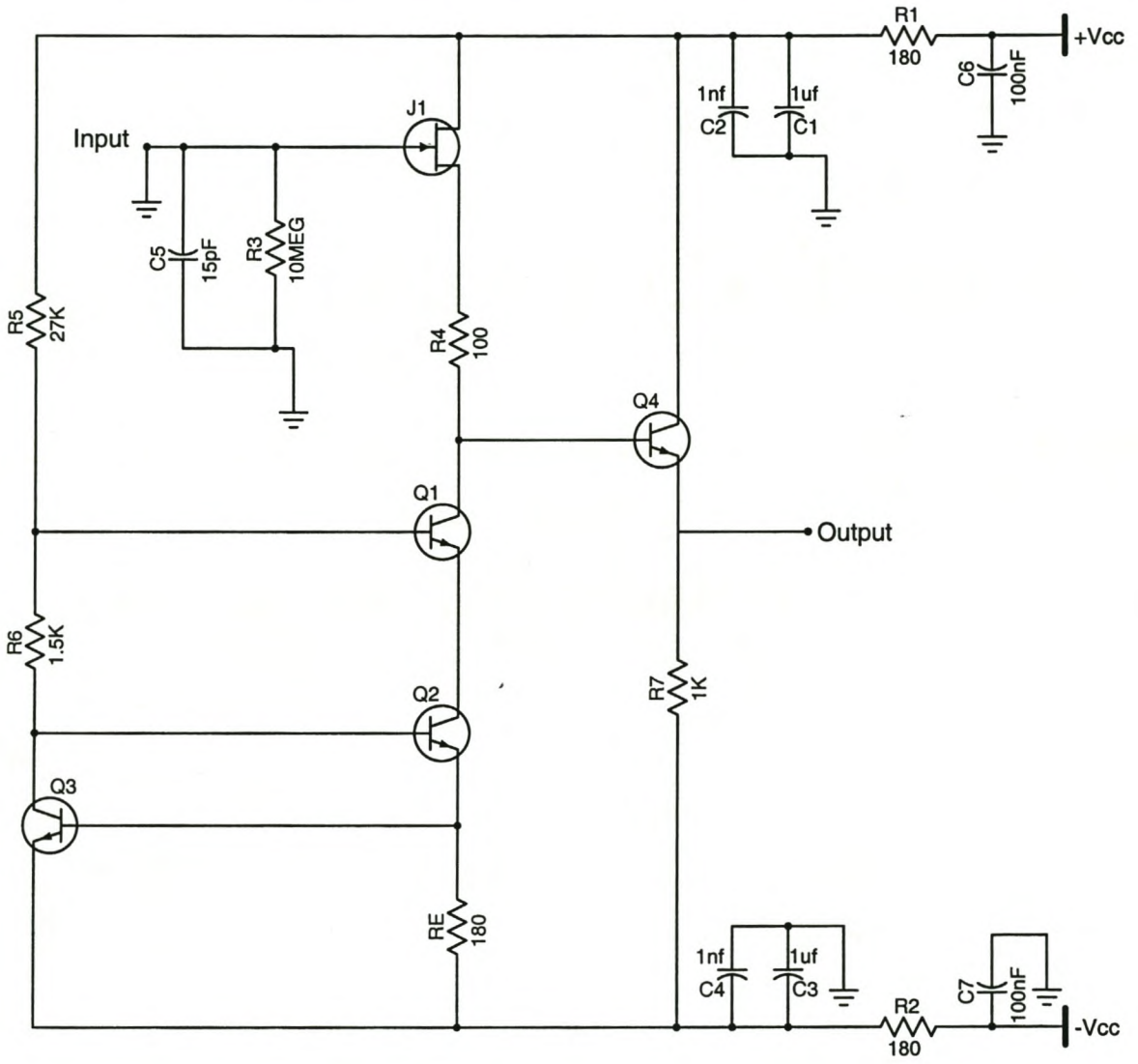


Fig. 3.2: ***Schematic representation of the input stage of the discrete implementation.***

Rather than using a common source FET directly, it is preferable to use a FET source follower as an input buffer to a standard Bipolar Junction Transistor (BJT) amplifier. This is due to the comparatively low transconductance (the ratio of output current to input voltage) of FETs. Furthermore, FET followers allow for high input impedance and have no dc input current [31]. The source follower with no drain resistor, like the emitter follower, also has no Miller Effect [31].

The primary criterion when choosing the FET was bandwidth. Considering price and availability, the choice lay between the 2N5486 and the 2N5245. Both are n-Channel RF amplifiers featuring similar characteristics [33, 34]. The 2N5486 was chosen as it displays a higher input impedance compared to that of the 2N5245. The *Pspice* simulation results for their respective input impedances are given in figures A.5 and A.6 in Appendix A. The input impedance of the 2N5486 as it appears in figure 3.2 is more than twice as large as that of the 2N5245.

The addition of Q_4 with resistor R_7 of 1 kΩ allowed for more bandwidth of the complete input stage. In addition, this emitter follower reduces the output impedance of the input stage. Q_2 and Q_3 with R_6 and R_E provide a current source for the circuit and Q_1 biases Q_4. Initially the 2N3904 general-purpose transistors were used for Q_1 to Q_4. Figure A.7 in Appendix A shows the results for an input sinusoidal waveform of 10V at 10 MHz using 2N3904s for Q_1-Q_4. The rising part of the sinusoidal input is followed, but the falling part is followed almost linearly. In the experimental situation this problem was more amplified than in the simulations. There are three factors that can affect the output signal that are not taken into account in a *Pspice* simulation:

- The capacitance between the collector and emitter (C_{CE}) of Q_1.
- The capacitance of the probe.
- The input voltage of the sinusoidal wave.

Although *Pspice* simulations take into account the C_{CE} of transistors, it was added as an external capacitance in the simulation to see the effect of the capacitance on the output signal.

Simulation results are given in figure A.8 in Appendix A. The experimental results compared well to the simulation results as they appear in figure A.8. Relative to figure A.7 there is much more distortion in the falling part of the output signal where after the output follows the input almost linearly. From this it was established that Q_1 had to be replaced by a better transistor with a higher current gain-bandwidth product (f_T) and smaller C_{CE} than the 2N3904s [35]. Since Q_1 biases Q_4, they should have the same characteristics. The current gain-bandwidth products (f_T) of suitable transistors were examined and considering price and availability the 2N3478 was chosen. The 2N3904s have a minimum f_T of 300 MHz whilst that of the 2N3478s is 1400 MHz [36]. Both the output capacitance and the input capacitance of the 2N3478 are much lower compared to that of the 2N3904. The final simulation results using these transistors are given in figures A.2 to A.4 in Appendix A.

Capacitors C_1-C_4 decouples noise from the power supplies. At high frequencies the impedances on the tracks of the board and in the leads increase. Since the larger capacitors are polarized and electrolytic they become inductive with increased input frequencies. This could result in signal amplitude errors or oscillation. Therefore to maintain a low AC-coupling impedance throughout the signal band, a small value ceramic capacitor is added in parallel to each polarized capacitor.

R_8 and C_5 serve as an impedance matching network, and values chosen to reflect the input impedance of a typical oscilloscope, i.e. a 10 MΩ resistor in parallel with a 15 pF capacitor. Calculations for R_E, R_1, R_2, R_5 and R_6 follow. The current flowing through R_E was chosen to be 4 mA as this was the typical operating current of the emitter of the 2N3904 [35]. Since there exists a forward diode drop of approximately 0.7V between the base and emitter of each of the transistors, i.e. also Q_3, and using Ohm's Law gives the relationship

$$R_E = \frac{0.7V}{4mA}$$
$$= 175\Omega \approx 180\Omega . \qquad (3.1)$$

The current flowing through R_6 was chosen as 1 mA as this provides a balance between low power dissipation and signal amplitude for noise not to be a factor. The base of Q_2 is at 1.4V. In order for Q_1 to be active, its base needs to be at least a volt higher than that of Q_2. Taking

Q_1s base to be at 2.8 V the value of R_6 is given by

$$R_6 = \frac{(2.8-1.4)V}{1mA}$$
$$= 1.4k\Omega \approx 1.5k\Omega . \qquad (3.2)$$

Assuming that the β of Q_1 is high enough for all the current from R_5 to flow through R_6 gives

$$R_5 = \frac{(30-2.8)V}{1mA}$$
$$= 27.2k\Omega \approx 27k\Omega . \qquad (3.3)$$

In addition to decoupling the power supplies, C_1 and C_2 with C_3 and C_4 form low pass filters with R_1 and R_2 respectively. The RC circuit filters high frequency content from the power supplies. Allowing a maximum of 13 V for the operation of the rest of the circuit, a 0.9 V drop across each of the resistors R_1 and R_2 is sufficient. Since there is 5 mA passing through the resistors,

$$R_1 = R_2 = \frac{0.9V}{5mA}$$
$$= 180\Omega . \qquad (3.4)$$

The gain of this stage can be determined using the transconductance specification of J_1. The FET source follower shown in figure 3.3 gives rise to the following relationships [31]

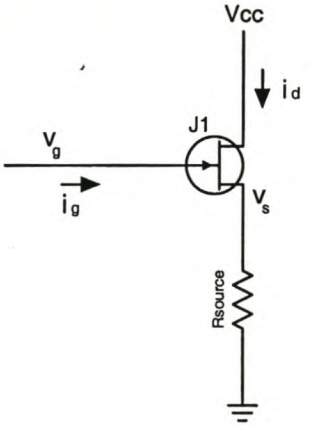


Fig. 3.3: Representation of the FET source follower [31].

Assuming that the current through the gate of the FET, i.e. i_g, is negligable,

$$v_s = R_{source} i_d \tag{3.5}$$

and

$$i_d = g_m v_{gs} = g_m (v_g - v_s), \tag{3.6}$$

where R_{source} represents the resistive load on the FET and g_m = transconductance specification of the FET.

Substitution of equation 3.6 into equation 3.5 yields the relationship

$$v_s = [\frac{R_{source} g_m}{1 + R_{source} g_m}] v_g . \tag{3.7}$$

For $R_{source} >>> \frac{1}{g_m}$, one obtains a good source follower ($v_g = v_s$) with gain approaching, but never equalling, unity [31]. The value of g_m, i.e. the ratio of the output current to the input voltage, is typically of the order of 3 mmhos for the 2N5486 [33]. Transistors Q_2 and Q_3 with resistors R_6 and R_E provide a current source with with a very high input impedance and can be treated as an open circuit. R_{source} is therefore the input impedance of the emitter follower Q_4, i.e. $(\beta+1)R_7 + R_4$. Since $(\beta+1)R_7$ is much greater than $\frac{1}{g_m}$, the value of R_4 does not influence R_{source} and is used more for the biasing of the FET. *Pspice* simulations show that R_4 should equal 100Ω.

The *Pspice* simulation results for inputs of 10 MHz, 1V and 10 MHz, 10V sinusoidal waveforms are given in Appendix A in figures A.2 to A.4. Figures A.2 and A.3 show the transient responses for a sinusoidal input of 1 V and 10 V respectively. For each graph the outputs follow the input almost perfectly. There are vertical offsets in both the graphs and this is more predominant in figure A.2. Figures A.2 and A.3 show that the gain of the input stage approaches, but is never equal to unity as predicted by equation 3.7. Figure A.4 shows the frequency response of the output relative to a 1V, A.C. input. The frequency response for a 10 V, A.C input is the same as in figure A.4. A –3 dB bandwidth of approximately 114 MHz is achieved with a peak at approximately 80 MHz.

3.2.3 Amplifier stage of the discrete implementation

Figure 3.4 shows a block diagram representation of the amplifier stage of the discrete implementation. This stage is the high gain differential stage and has high input impedance and low output impedance. A schematic representation of the complete circuit design for this stage is shown in figure 3.5. In the schematic representation component names and values are given. In addition, the numbers of nodes that are often referred to in the text are included within brackets. *Pspice* simulations were done to ensure that the circuit was optimally designed. Due to the relative complexity of the circuit, it will be discussed with reference to its three recognisable parts, viz. the intermediate stage, the voltage gain stage and the output buffer stage.

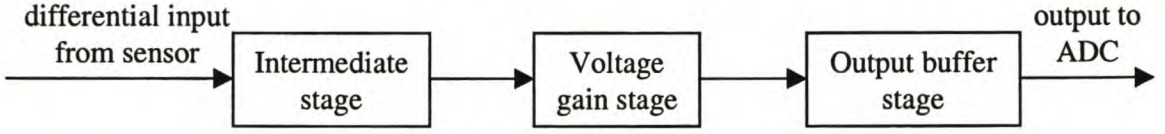


Fig. 3.4: ***Block diagram representation of the amplifier stage of the discrete implementation.***

Ultra high frequency transistor arrays were used to ensure that the transistors are closely matched. Matching of the transistors is important to ensure that the transistors are electrically and thermally alike, which guarantees that the transistors respond similarly to temperature fluctuations. The criteria used when choosing suitable arrays were high gain-bandwidth products, price and availability. The *Harris Semiconductor* chips were used, viz. the HFA3127, HFA3128 and the HFA3096. Each chip consists of five dielectrically isolated transistors (NPNs, PNPs or a combination of the NPNs and PNPs) [37]. The chips are optimally used considering board space and pricing. An HFA3128 is used for Q_7 - Q_{10}. Q_1 and Q_2 with Q_{11} - Q_{13} are implemented on an HFA3906 and Q_3 – Q_6 are implemented on an HFA3127.

The circuit runs off ±3.3 V rails. Ideally it would have been preferable to run the circuit off ±15 V rails as with the input stage. The limitations of the transistor arrays made this

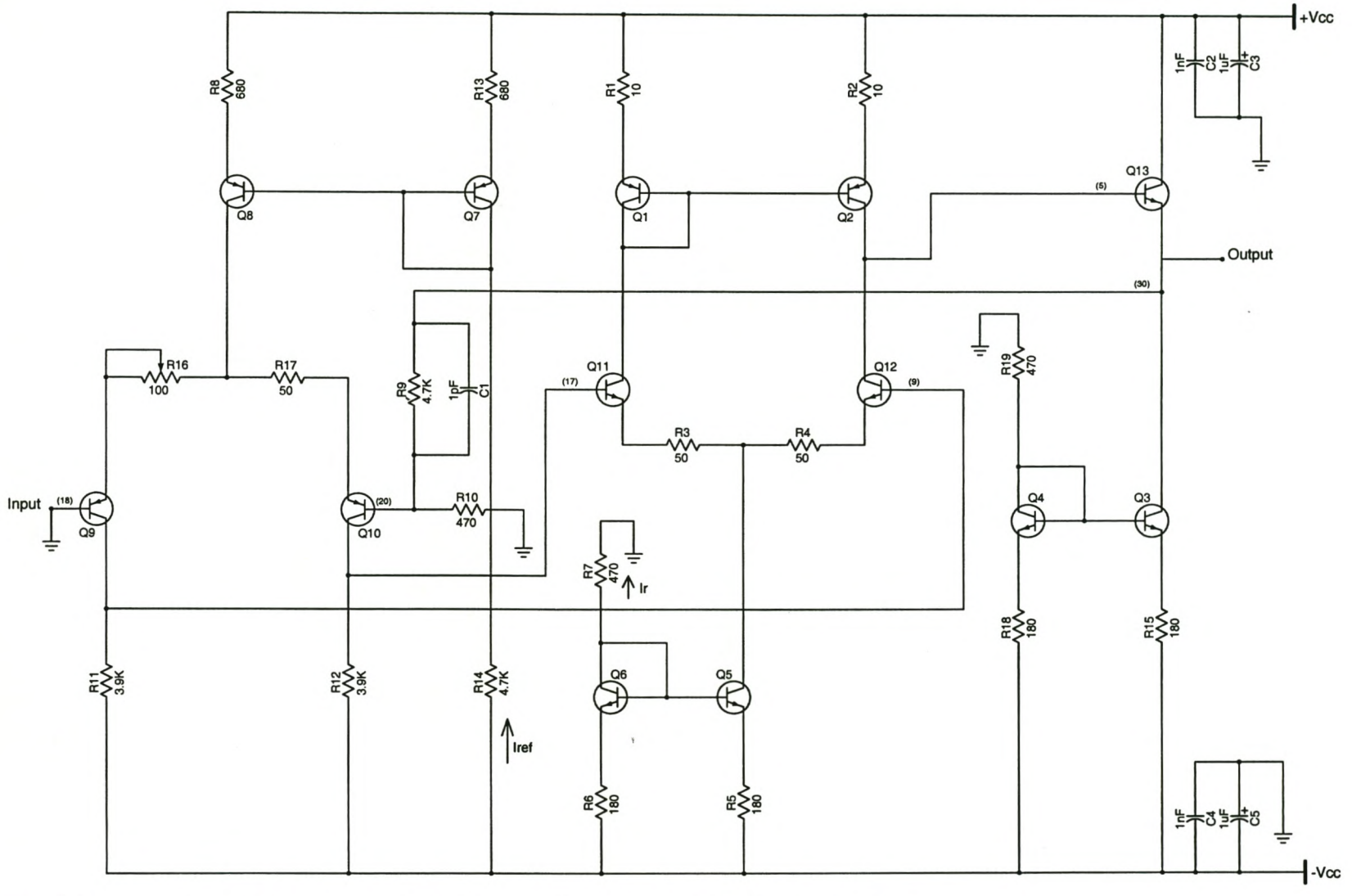


Fig. 3.5: ***Schematic representation of the amplifier stage of the discrete implementation.***

impossible since most of the suitable high frequency transistor arrays have very low breakdown voltages, thereby limiting the voltage rails and the magnitude of the input signal. The circuit has power supply bypassing capacitors as has been discussed in section 3.2.2.

3.2.3.1 Intermediate stage

The intermediate stage consists of transistors Q_8 and Q_7 with resistors R_8, R_{13} and R_{14} as shown in figure 3.5 forming a current source (current source 1). Transistors Q_9 and Q_{10} with resistors R_{16}, R_{17}, R_{11} and R_{12} form the input differential stage. The input differential stage loads the input stage of section 3.2.2 and provides it with a high input impedance. This stage acts as a level shifter and shifts the input signals to a lower voltage where the bases of the voltage gain stage operate and shift the signals up again. In addition, this stage contributes to the final open loop gain of the amplifier stage. It is assumed that Q_{12} and Q_{11} of the voltage gain stage do not load the intermediate stage. The external input to this stage is at node (18). The outputs are at taken at nodes (17) and (9) as shown in figure 3.5.

Q_8 and Q_7 are matched transistors having their bases connected together and their respective emitters connected via resistors to V_{CC}. Q_7 has its collector shorted to its base, thereby behaving as a diode. The input differential stage must ensure that the collector voltage of Q_8 is always lower than that of its base. It is assumed that the BJTs have high β values thereby making their base currents insignificant. The input current flows through R_{13} thereby creating a voltage at the bases of Q_7 and Q_8 corresponding to the input current. The V_{BE} values of Q_8 and Q_7 are dependent on the circuit temperature and the type of transistor. Since both the transistors are identical, the current flowing through the emitter of Q_8 will equal the emitter current of Q_7 and Q_8 is able to source that same amount of current to the input differential stage [31].

R_{14} is used to generate the control current. 1.3 mA has been chosen as the reference current that is to be sourced to the input differential stage. Resistors R_8 and R_{13} are used to counter the Early Effect [31]. The emitter resistors must have at least a few tenths of a volt voltage drop thus making the output current of the circuit not susceptible to small changes in V_{BE}.

Assuming that a 0.7 V drop exists across R_{13} and taking into account the diode drop across the base of the transistor Q_7, I_{ref} is given by

$$I_{ref} = \frac{(6.6-0.7-0.7)V}{R_{14}} \doteq 1.3mA. \qquad (3.8)$$

Therefore

$$R_{14} = 4k\Omega \approx 4.7k\Omega. \qquad (3.9)$$

R_8 and R_{13} are given by

$$R_8 = R_{13} = \frac{0.7V}{1.3mA} = 538\Omega \approx 680\Omega. \qquad (3.10)$$

The exact value of I_{ref} is given by

$$I_{ref} = \frac{(6.6-0.7)V}{4.7k\Omega + 680\Omega} = 1.097mA. \qquad (3.11)$$

Using the exact value of I_{ref}, the voltage drop each across R_8 and R_{13} is actually

$$V = 680\Omega(1.097mA) = 0.746V. \qquad (3.12)$$

The input differential stage amplifies the differential voltage between the bases of Q_9 and Q_{10} and converts it to a single–ended output signal. This is the most common configuration of a BJT differential pair and will be used again in a modified form in section 3.2.3.2. Q_9 and Q_{10} are matched transistors having their emitters joined via resistors R_{16} and R_{17} to the output of the constant current source, i.e. the collector of Q_8. The important function of R_{16} and R_{17} is to provide a balance or offset adjustment control. The important factor is to never allow the collectors of the transistors to enter saturation [30]. To understand the operation of the BJT differential amplifier, the large signal operation of it needs to be discussed.

The exponential relationship applied to each transistor is given by

$$i_{E_9} = \frac{I_s}{\alpha} e^{(v_{B9}-v_{C8})/V_T} \quad [30] \qquad (3.13)$$

and

$$i_{E_{10}} = \frac{I_s}{\alpha} e^{(v_{B10}-v_{C8})/V_T}, \quad [30] \qquad (3.14)$$

where I_s is the saturation current,

V_T is the thermal voltage,

α is the common-base current gain,

v_{B9} denotes the base voltage of Q_9

v_{B10} denotes the base voltage of Q_{10} and v_{C8} denotes the collector voltage of Q_8.

Combining equations 3.13 and 3.14 gives the relationship between the emitter currents of Q_9 and Q_{10}

$$\frac{i_{E9}}{i_{E10}} = e^{(v_{B9}-v_{B10})/V_T}. \qquad (3.15)$$

Equation 3.15 can be re-written as

$$\frac{i_{E9}}{i_{E9}+i_{E10}} = \frac{1}{1+e^{(v_{B10}-v_{B9})/V_T}} \qquad (3.16)$$

and

$$\frac{i_{E10}}{i_{E9}+i_{E10}} = \frac{1}{1+e^{(v_{B9}-v_{B10})/V_T}}. \qquad (3.17)$$

The additional constraint imposed on the circuit by the current source is given by the relationship

$$i_{E9}+i_{E10} = I_{ref}, \qquad (3.18)$$

where i_{E9} and i_{E10} denote the emitter currents of Q_9 and Q_{10} respectively.

Combining equations 3.18 with 3.16 and 3.17 yields the relationships

$$i_{E9} = \frac{I_{ref}}{1+e^{(v_{B10}-v_{B9})/V_T}} \qquad (3.19)$$

$$i_{E10} = \frac{I_{ref}}{1+e^{(v_{B9}-v_{B10})/V_T}}. \qquad (3.20)$$

Multiplication of the emitter currents in equations 3.19 and 3.20 with α (which is close to unity) will yield the collector currents, i_{C9} and i_{C10}, of Q_9 and Q_{10} respectively. Equations 3.19 and 3.20 explain the essential operation of the differential amplifier. There are two important observations to be made. Firstly, the amplifier responds only to a difference voltage. If $v_{B9} = v_{B10} = v_{CM}$, the current I_{ref} divides equally between the two transistors irrespective of the value of the common mode voltage. Secondly, a relatively small

differential voltage $v_d = v_{B9} - v_{B10}$ results in the current flowing almost entirely into one of the two transistors [30].

Following is a discussion on the small-signal operation of the BJT differential amplifier [30]. Referring to figure 3.5, equations 3.19 and 3.20 may be used to find the total currents i_{C9} and i_{C10}. Assume that there exists a differential voltage signal, v_d, between the bases and substitute this into equations 3.19 and 3.20 yields

$$i_{C9} = \frac{\alpha I_{ref}}{1 + e^{-v_d / V_T}} \tag{3.21}$$

and

$$i_{C10} = \frac{\alpha I_{ref}}{1 + e^{v_d / V_T}}. \tag{3.22}$$

Multiplying 3.21 by exp ($v_d/2V_T$) yields:

$$i_{C9} = \frac{\alpha I_{ref} e^{(v_d / 2V_T)}}{e^{(v_d / 2V_T)} + e^{(-v_d / 2V_T)}}. \tag{3.23}$$

Assuming $v_d << 2V_T$, the exponential may be expanded to give the relationship

$$i_{C9} \approx \frac{\alpha I_{ref} (1 + v_d / 2V_T)}{1 + v_d / 2V_T + 1 - v_d / 2V_T}. \tag{3.24}$$

Thus

$$i_{C9} = \frac{\alpha I_{ref}}{2} + \frac{\alpha I_{ref}}{2V_T} \frac{v_d}{2}. \tag{3.25}$$

Similarly 3.22 can be re-arranged to yield

$$i_{C9} = \frac{\alpha I_{ref}}{2} - \frac{\alpha I_{ref}}{2V_T} \frac{v_d}{2}. \tag{3.26}$$

Equations 3.25 and 3.26 confirms that when $v_d = 0$, the current is equally divided between the two transistors. However, when a small-signal voltage, v_d, is applied differentially, i_{C9} increases by an increment i_C given by

$$i_C = \frac{\alpha I_{ref}}{2V_T} \frac{v_d}{2}. \tag{3.27}$$

Since i_{C10} decreases by the same amount given in equation 3.27, the sum of the total currents in the transistors remains a constant.

The symmetry of the circuit dictates that v_d divides equally between the base-emitter junctions of the transistors. The voltages between the base and emitter of each transistor, v_{BE9} and v_{BE10}, are given by

$$v_{BE9} = V_{BE} + \frac{v_d}{2} \qquad [30] \qquad (3.28)$$

and

$$v_{BE10} = V_{BE} - \frac{v_d}{2}, \qquad [30] \qquad (3.29)$$

where V_{BE} is the dc voltage across the each base and emitter of Q_9 and Q_{10} relative to an emitter current of $I_{ref}/2$. It follows that i_{C9} increases by $g_m v_d/2$ and i_{C10} decreases by $g_m v_d/2$ where g_m denotes the transconductance of the transistors given by the relationship

$$g_m = \frac{i_C}{V_T} = \frac{\alpha I_{ref}/2}{V_T}. \qquad [30] \qquad (3.30)$$

Equation 3.27 then gives

$$i_C = g_m v_d/2. \qquad (3.31)$$

To calculate R_{12} and in essence R_{11}, (which equals R_{12}), Q_{11}, Q_5 and R_3 of the voltage gain stage of the amplifier needs to be considered. Allow for a maximum collector-emitter saturation voltage of 0.6 V (twice that of the specified maximum value for the HFA3127 [37]) for Q_5 to ensure that the transistor operates within its linear range. Allow for a 0.7 V drop across R_3, and consider the 0.7 V drop between the base and emitter of Q_{11}. This with the fact that the 1.097 mA that is sourced to the input differential stage divides equally between the Q_9 and Q_{10} yields

$$R_{11} = R_{12} = \frac{(0.6 + 0.7 + 0.7)V}{(1.097/2)mA} = 3.64k\Omega \approx 3.9k\Omega. \qquad (3.32)$$

Typically R_{16} and R_{17} are very small values and can be omitted entirely [31]. *Pspice* simulations showed that the optimal values were $R_{16} = R_{17} = 47\Omega$. In the developed system R_{16} is a variable potentiometer with maximum resistance of 100Ω.

From equations 3.25 and 3. 26 it has been established that for small difference input voltages ($v_d << 2V_T$), the collector currents are given by the following relationships

$$i_{C9} = I_C + g_m \frac{v_d}{2} \qquad [30] \qquad (3.33)$$

and

$$i_{C10} = I_C - g_m \frac{v_d}{2}, \qquad [30] \qquad (3.34)$$

where $I_C = \alpha I_{ref}/2$.

Thus the collector voltages, taking into account the dc voltages, are

$$v_{C9} = (V_{CC} - I_C R_{11}) - g_m R_{11} \frac{v_d}{2} \qquad (3.35)$$

and

$$v_{C10} = (V_{CC} - I_C R_{12}) + g_m R_{12} \frac{v_d}{2}. \qquad (3.36)$$

If the output is taken differentially and letting $R_{12} = R_{11}$ the differential gain of the amplifier is given by the relationship

$$A_d = (v_{C9} - v_{C10})/v_d = -g_m R_{11}. \qquad [30] \qquad (3.37)$$

For a differential amplifier with resistances in the leads, the differential output is given by the relationship

$$A_d = -\frac{\alpha(2R_{11})}{2r_e + 2R_E} \approx -\frac{R_{11}}{r_e + R_E}, \qquad [30] \qquad (3.38)$$

where $2r_e + 2R_E$ is the total resistance in the emitter circuit.

Typically, since $(r_e + R_E)$ is small and R_{11} is 3.9 kΩ, open-loop gains of a few hundred are obtainable [30].

3.2.3.2 Voltage gain stage

As the name suggests this stage contributes to the voltage gain of the entire amplifier stage. It consists of transistors Q_1, Q_2, Q_{11} and Q_{12} with resistors R_1 - R_4 as shown in figure 3.5 forming the active-load differential amplifier. Transistors Q_5, Q_6 with resistors R_5 - R_7 provide a current source (current source 2) that is a current mirror as shown in figure 3.5. The current mirror is a modified Widlar current source [30]. The differential inputs to this

stage are at nodes (17) and (9). The output of this stage is at taken at node (5) as shown in figure 3.5.

R_7 is used to generate the control current. 4 mA has been chosen as the reference current that is to be sourced to the active-load differential amplifier. Resistors R_5 and R_6 are used to counter the Early Effect [31]. Assuming that a 0.7 V drop exists across R_6 and taking into account the diode drop across the base of the transistor Q_6, I_r is given by

$$I_r = \frac{(3.3 - 0.7 - 0.7)V}{R_6} = 4mA. \qquad (3.39)$$

Therefore

$$R_{14} = 475\Omega \approx 470\Omega. \qquad (3.40)$$

R_5 and R_6 are given by

$$R_5 = R_6 = \frac{0.7V}{4mA} = 175\Omega \approx 180\Omega. \qquad (3.41)$$

The exact value of I_r is

$$I_r = \frac{(3.3 - 0.7)V}{(470 + 180)\Omega} = 4.000mA. \qquad (3.42)$$

The essential difference between the active-load differential amplifier and the input differential stage in section 3.2.3.1 is that the former features an additional current mirror stage. Transistors Q_{11} and Q_{12} form a differential pair biased with a constant current, I_r. The current mirror formed by Q_1 and Q_2 provides the active load that is needed for more output swing and higher voltage gains [30]. The output is taken single-endedly from the collector of Q_2 at node (5).

Consider a differential signal v_d applied at the inputs of the voltage gain stage, i.e. nodes (17) and (9). From equation 3.31 it is known that current signals $g_m(v_d/2)$ result in the collectors of Q_{11} and Q_{12} becoming oppositely polarised [31]. The current mirror reproduces the current signal $g_m(v_d/2)$ through the collector of Q_2. Thus at the output node, i.e. node (5), there are two current signals that add together to produce the total current signal of $g_m(v_d)$ [31]. Since the resistance presented by the subsequent output buffer stage is very large, the

voltage signal at node (5) is determined by the total signal current $g_m(v_d)$ and the total resistance between node (5) and ground. Letting this total resistance be represented by R_o, the output voltage, v_6, is given by the relationship

$$v_5 = g_m v_d R_o, \text{ [30]} \qquad (3.43)$$

where R_o is the parallel equivalent of the output resistances of Q_{12} and Q_2. Q_{12} is operating in the common-emitter configuration and its output resistance equals the transistor resistance, r_{o12} [31]. Also, r_{o12} equals the output resistance, r_{o2}, of Q_2. This gives rise to the relationship

$$R_o = \frac{r_{o12} * r_{o2}}{r_{o12} + r_{o2}}. \qquad \text{[30]} \qquad (3.44)$$

For $r_{o12} = r_{o2} = r_o$,

$$R_o = \frac{r_o}{2} \qquad (3.45)$$

The output voltage is then given by the relationship

$$v_5 = g_m v_d (r_o / 2). \qquad (3.46)$$

Therefore the voltage gain is represented by

$$\frac{v_5}{v_d} = \frac{g_m r_o}{2}. \qquad (3.47)$$

Substituting $g_m = I_C/V_T$ and $r_o = V_A/I_C$, where $I_C = I_r/2$ into equation 3.47 gives the relationship

$$g_m r_o = \frac{V_A}{V_T}, \text{ [30]} \qquad (3.48)$$

where V_A denotes the Early Voltage of the transistor.

Equation 3.48 is a constant for a given transistor. Typically, $V_A = 100$ V, resulting in $g_m r_o = 4000$ and a stage voltage gain of about 2000.

Figures A.10 and A.11 in Appendix A give the transient and frequency responses respectively of the voltage gain stage relative to the other two stages. A plot of V(18) and V(5) in figure A.10 shows the output of this stage relative to a 10 MHz, 0.1 V sinusoidal input. A gain of approximately 11 is achieved. Examining the plot of this stage relative to the other two stages shows that this is the stage that contributes to the final gain of the amplifier. A plot of V(5)/((V(17)-V(9)) in figure A.11 shows that gains of a few hundred are

achieved for this stage alone.

At this stage an iterative process making only slight changes to the design was conducted to ensure that the complete design of the intermediate and voltage gain stages was optimal. It had to be verified that both the current sources (i.e. current source 1 of 1.3 mA and current source 2 of 4 mA) and the current mirror formed by Q_1 and Q_2 were optimally designed. Replacing them with ideal *Pspice* models and comparing results achieved this. Ideal *Pspice* current sources [45] were used instead of current sources 1 and 2. A *Pspice* current-controlled-current source [45] replaced the current mirror formed by Q_1 and Q_2 in figure 3.5. Table 3.1 below shows the 8 simulations that were done in the iterative process. Results are given in figures A.13-A.20 in Appendix A.

The 8 graphs all have –3 dB bandwidths of approximately 20 MHz at gains of approximately 45 dB. Replacing the current sources and the current mirror with ideal *Pspice* models did not improve the bandwidth significantly. This confirms that the circuit design as it appears in figure 3.5 is optimally designed with regards to the current sources and the current mirror. Since the differential stages and the output buffer stage are standard configurations it is fair to conclude that the amplifier stage as a whole has been optimally designed.

Table 3.1: ***Iteration processes to optimise the amplifier stage of the discrete implementation of the analog signal conditioning subsystem.***

	Current source 1 (1.3 mA)	Current source 2 (4 mA)	Current mirror
1	Ideal	Ideal	Ideal
2	Non-ideal	Non-ideal	Ideal
3	Ideal	Non-ideal	Ideal
4	Non-ideal	Ideal	Ideal
5	Ideal	Ideal	Non-ideal
6	Non-ideal	Non-ideal	Non-ideal
7	Ideal	Non-ideal	Non-ideal
8	Non-ideal	Ideal	Non-ideal

A cascode stage using Q_{14} and Q_{15} was included since cascodes are usually useful in improving bandwidth significantly. Figure 3.6 shows the cascoded active-load differential amplifier.

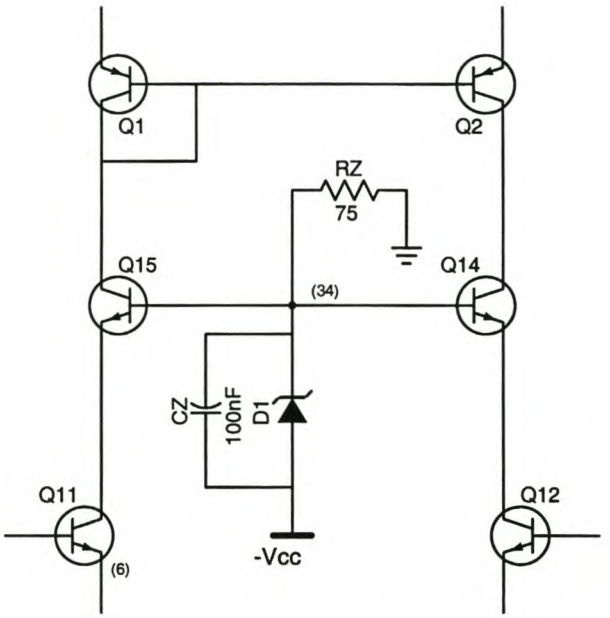


Fig. 3.6: ***Cascoded active-load differential amplifier of the amplifier stage of the discrete implementation.***

Q_{14} and Q_{15} form a differential common-base stage. A zener diode provides the cascoded stage with a constant current. For the zener diode to be active it must be 2.7 V higher that the emitter of Q_{11}. *Pspice* simulations show that node (6) is at –2.18 V. Node (34) should therefore be at approximately 0.52 V (i.e. -2.18 V + 2.7 V). The zener diode must operate at approximately 0.52 V – (-3.3 V) = 3.82 V. The D1N747 has a V_Z = 3.6 V at 20 mA. Using the D1N747, node (34) therefore is at 3.3 V – 3.6 V = -0.3 V. Considering that 4 mA is sourced to the differential cascode stage, the calculation of R_z is given by

$$R_z = \frac{0.3V}{4mA} = 75\Omega . \qquad (3.49)$$

The 8 simulations as in Table 3.1 were repeated including the cascode stage. Only simulation results for iteration 6 are given in figures A.22 in Appendix A. The graph is almost identical to figure A.18. A –3 dB bandwidth of approximately 20 MHz is achieved at

an approximate gain of 45 dB. From the 16 simulations it was concluded that the optimal result was to keep the current source and current mirrors as is and to not include a cascode stage. Cascodes improve bandwidths at the lower frequencies, but for the higher frequencies there are no improvements to achievable results.

3.2.3.3 Output buffer stage

The output buffer stage consists of transistors Q_3 and Q_4 with resistors R_{15}, R_{18} and R_{19} as shown in figure 3.5 providing a modified Widlar current source [31] sourcing 4 mA for the biasing of transistor Q_{13}. The Widlar current source has been discussed in section 3.2.3.2. This stage is the current gain stage and has unity voltage gain. It supplies a load on the output. The output (node (30) in figure 3.5) from the emitter provides the final feedback path to the intermediate stage. A transient plot of V(30), V(5) and V(18) in figure A.10 shows that the output buffer stage has unity gain and its output follows the output of the voltage gain stage. Plots of V(30)/V(5) and V(30)/V(18) in figure A.11 show that the buffer has unity gain and it's performance begins to degrade well past the 100 MHz mark.

3.2.4 Test results

Pspice simulation results for the complete amplifier stage as it appears in figure 3.5 are given in figures A.10 to A.12 in Appendix A. Figure A.10 gives the transient responses of each of the three stages of the circuit for a 0.1 V, 10 MHz sinusoidal input. Figure A.11 shows the frequency response of the three stages of figure 3.5 for a 0.1 V, A.C. input. In figure A.10 the outputs from each of the three stages follow the input almost perfectly. From plot V(30)/V(18) in figure A.11 an overall gain of approximately 11 is achieved. Figure A.12 shows that a –3 dB bandwidth of approximately 20 MHz is achieved for the entire amplifier stage for an A.C. input of 0.1 V. The practical results differed slightly from the *Pspice* simulation results but this was overcome by compensating for the probe capacitance by adding a 10 MΩ resistor in series with a variable capacitor ranged from 1.4 to 10 pF. *Pspice* simulations provided the optimal resistor and capacitor values.

3.3 Integrated implementation of the analog signal conditioning subsystem

3.3.1 Introduction

Figures 3.7 and 3.8 respectively show block diagram and circuit diagram representations of the integrated version of the analog signal conditioning subsystem. It receives a differential input from a sensor and conditions it to be suitable for acceptance by the ADC. It is designed to receive a maximum differential 0.1 V input signal and to allow for gains of 1.2, 2, 5 and 10.09. This subsystem runs off ± 5 V power supplies. In the schematic representation component names and values are given. In addition, the numbers of nodes that are often referred to in the text are included within brackets.

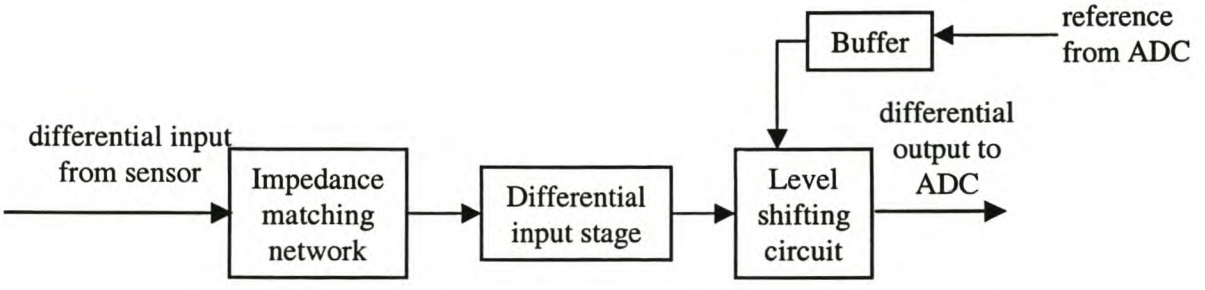


Fig. 3.7: ***Block diagram representation of the integrated implementation of the analog signal conditioning subsystem.***

The impedance matching network will be designed to reflect the same input impedance as a typical oscilloscope. The differential input stage is essentially the input stage of the classic instrumentation amplifier. It is at this stage that the gain of the subsystem can be adjusted by means of a single resistor, R_8. The inputs of the stage are denoted by nodes (1) and (4). The level shifting circuit centres the signals around the reference signal required by the ADC. The inputs to this stage are denoted by nodes (5) and (6). The reference signal is obtained from the ADC itself and is buffered before use. Node (20) denotes the input of the buffering circuit. Nodes (21) and (22) denote the output of the level shifting circuit and, in essence, the entire subsystem.

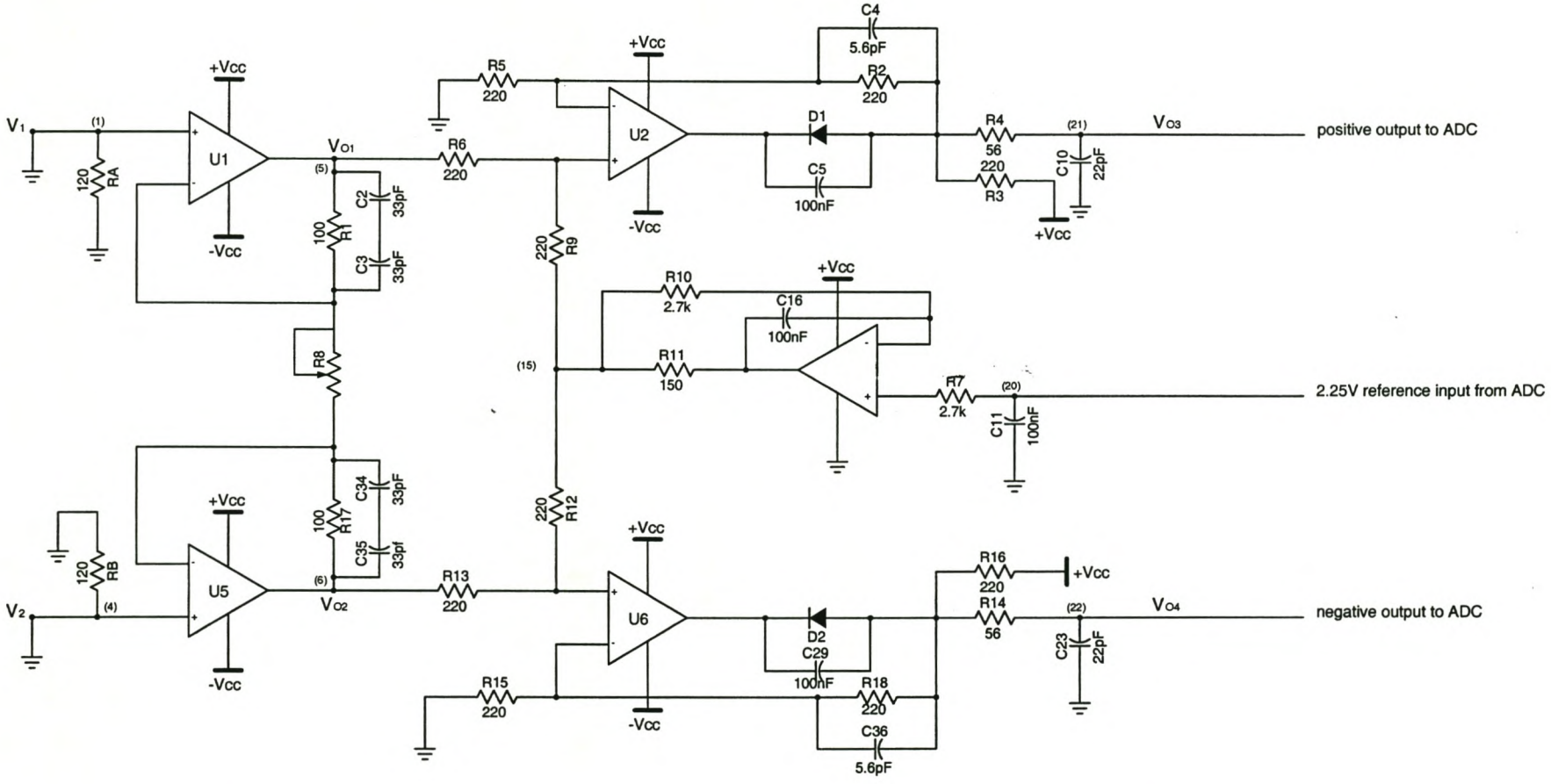


Fig. 3.8: ***Schematic representation of the integrated implementation of the analog signal conditioning subsystem.***

The circuit was extensively simulated for the four desired gains, but the printed circuit (p.c.) board was manufactured with R_8 as a fixed resistor (=1 kΩ) thus setting the gain of the subsystem to 1.2. The complete circuit design and p.c board layout of the analog signal conditioning subsystem is given in Appendix C, figures C.1, C.2 and C.6.

The high bandwidth specification of the application as discussed in Chapters 1 and 2 was the main criterion when selecting a suitable operational amplifier. However, since the application of this system is for a wideband signal conditioning system, the lower frequencies are also of importance. Most integrated designs, in being optimised for the higher frequencies, suffer from degraded DC performance. Factors like biasing and offset drifts are not minimised. In this system an overall adequate performance is required at the lower frequencies as well as the higher frequencies.

Another factor to consider was the ADC. The analog signal conditioning subsystem had to be of sufficient bandwidth to drive the chosen ADC. The 40 MHz ADS800 manufactured by *Burr Brown* was selected for the ADC. This component will be discussed in Chapter 4. The ADS800 datasheets [41] suggest a driving circuit for the converter. The operational amplifiers used in the suggested circuit are the OPA642s [48] for U_1, U_2, U_5 and U_6 and the OPA130 [47] for U_3. Since the OPA642s were not easily obtainable, alternate operational amplifiers had to be sought. The operational amplifiers that were finally chosen had to be extensively simulated to ensure that they performed suitably to drive the ADS800.

A thorough search [46] was done and two suitable operational amplifiers were found, viz. the HA2840 manufactured by *Harris Semiconductor* [39] and the AD811 from *Analog Devices* [38]. Both operational amplifiers offer wide bandwidth, low distortion and very high slew rate. The HA2840 requires ±10 V to ±20 V rails whilst the AD811 requires ± 5V to ±15 V rails. Figures 3.9 and 3.10 show *Pspice* simulation results of the analog signal conditioning subsystem as shown in figure 3.8 for a gain of 1.2 using HA2840s and AD811s respectively for U_1, U_2, U_5 and U_6. For simulation purposes the buffer was omitted and the level shifting circuit provided with a 2.25 V, D.C. source. The simulation programs are given in Appendix A.

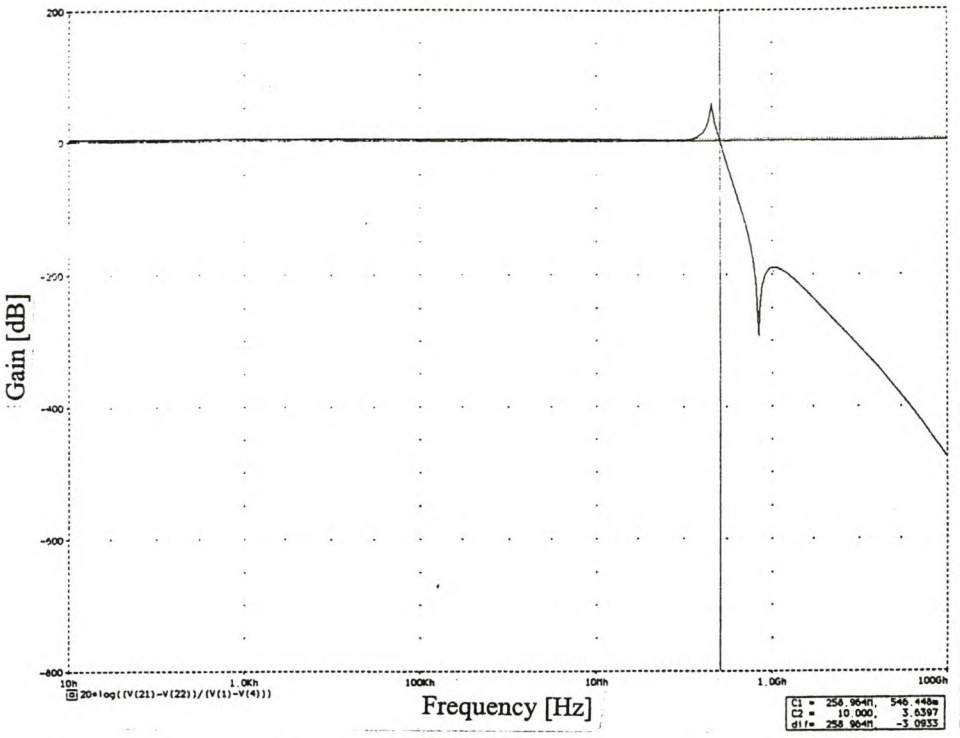


Fig. 3.9: ***Simulated frequency response of the output voltage relative to the input voltage of the integrated implementation using HA2840s (for a gain of 1.2).***

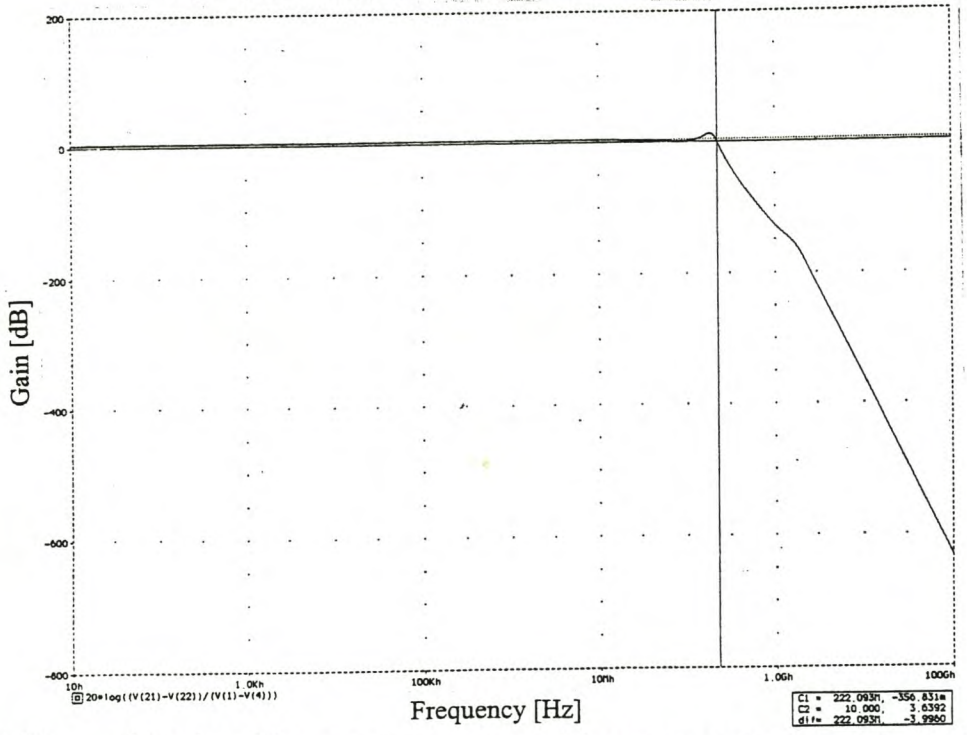


Fig. 3.10: ***Simulated frequency response of the output voltage relative to the input voltage of the integrated implementation using AD811s (for a gain of 1.2).***

For the given application, –3 dB bandwidths of approximately 260 MHz and 220 MHz are achieved using HA2840s and AD811s respectively. Peaks occur at approximately 207 MHz

and 190 MHz for the HA2840 and AD811 respectively. From these simulations, the HA2840 appears superior to the AD811 for the given application. However, the HA2840 requires higher power rails than the AD811 thus increasing the power dissipation of the circuit. Nevertheless, the HA2840 chips were not easily obtainable. Availability and feasibility therefore made the AD811 the optimum choice of the operational amplifier. All further simulations were done using AD811s in the differential stage and the level shifting circuit and an OPA130 in the buffering circuit. However, once the p.c. board was manufactured the OPA130 was unobtainable. An AD811 was used instead. The AD811, like the OPA130 is able to buffer the reference signal to drive the external circuitry. In addition, the OPA130 and AD811 are pin compatible.

The AD811 is a current feedback amplifier. It employs a current feedback architecture that results in a closed-loop –3 dB bandwidth which is dependent on the magnitude of the feedback resistors chosen for a particular topology. The 3 dB bandwidth also depends on the power supply voltage. As the voltage decreases, the magnitude of the internal junction capacitances increases. This results in a reduction in the closed-loop bandwidth. To compensate for this, smaller values of feedback resistors must be used at lower supply voltages [38].

The following aspects are of importance to obtain optimum performance:

- **Feedback and gain resistors**

  Careful consideration is required if gain flatness of better than 0.1 dB at frequencies above 10 MHz is needed. The relationship between the 3 dB bandwidth and the feedback resistor, as mentioned earlier, causes the fine scale gain flatness to vary with feedback resistor tolerance. To ensure flatness 1 % resistors should be used.

  - **Printed circuit board layout**

  P.C. board parasitic factors like stray capacitances and inductance loops can have a detrimental effect on the closed-loop performance of a wideband amplifier. Signal lines should be kept as short as possible to avoid inductance-related problems. Separate ground and power supply planes would be ideal. Figure C.6 in Appendix C shows the

p.c. board layout for the integrated implementation of the analog signal conditioning subsystem. For prototyping purposes a two-layer board was used. The analog signal conditioning subsystem has been implemented together with the digital conditioning subsystem and the transmitting module of the serial link.

- **Power supply bypassing**

This can become quite a crucial factor optimising the performance of a high frequency circuit. This has been discussed in section 3.2.2.

3.3.2 Impedance matching network

In the final implementation and p.c. board layout given in figures C.2 and C.6 in Appendix C, the impedance matching network hasn't been included. For prototyping purposes the circuit has been terminated with resistors R_A and R_B equal to 120Ω each as shown in figure 3.8. In the final developed system the circuit will be terminated with an impedance matching network that has been designed to reflect the same input impedance as a typical oscilloscope, i.e. a capacitance of ≈15 pF in parallel with a resistance of 10 MΩ. This will ensure that wideband commercial current sensing equipment can interface to the subsystem.

3.3.3 Differential input stage

The differential input stage consists of operational amplifiers U_1 and U_5 with resistors R_1, R_8 and R_{17} and capacitors C_2, C_3, C_{34} and C_{35} as shown in figure 3.8. This stage accepts a differential input V_1 and V_2 from the sensor and delivers a differential output, V_{O1} and V_{O2} to the level shifting circuit. The importance of this differential topology for EMI and earthing problems has been highlighted in Chapter 2. The differential input stage of the topology is the important gain stage of the entire subsystem. By varying resistor R_8 the gain of this stage and, in effect, the entire subsystem can be changed. The transfer function of the circuit is derived below. For this derivation the equivalent capacitance of C_2 and C_3 will be represented by C_2 and that of C_{34} and C_{35} by C_{34}.

For the sake of simplicity it was assumed that an ideal operational amplifiers were used

having infinite gain and infinite input impedance. Considering the combined resistance, R'', of R_1 and C_2 and working in the s-domain yields the relationship

$$\frac{1}{R''} = \frac{1}{R_1} + \frac{1}{1/sC_2} = \frac{1+sC_2R_1}{R_1}. \qquad (3.50)$$

Therefore

$$R'' = \frac{R_1}{1+sC_2R_1}. \qquad (3.51)$$

Similarly, the combined resistance, R', of R_{17} and C_{34} is given by

$$R' = \frac{R_{17}}{1+sC_{34}R_{17}}. \qquad (3.52)$$

The output voltage of the differential input stage at nodes (5) and (6) is given by

$$V_{O1} - V_{O2} = \frac{R_1}{sC_2R_1+1}\frac{V_1-V_2}{R_8} + \frac{R_{17}}{sC_{34}R_{17}+1}\frac{V_1-V_2}{R_8} + (V_1-V_2), \qquad (3.53)$$

where V_1 and V_2 denote the voltages at nodes (1) and (4) respectively.

The transfer function of the differential input stage is given by the relationship

$$A_d = \frac{V_{O1}-V_{O2}}{V_1-V_2} = \frac{R_1}{sC_2R_1R_8+R_8} + \frac{R_{17}}{sC_{34}R_{17}R_8+R_8} + 1. \qquad (3.54)$$

Simplifying equation 3.54 yields

$$A_d = \frac{R_1(sC_{34}R_{17}R_8+R_8) + R_{17}(sC_2R_1R_8+R_8) + (sC_2R_2R_8+R_8)(sC_{34}R_1R_8+R_8)}{(sC_2R_1R_8+R_8)(sC_{34}R_{17}R_8+R_8)}. \qquad (3.55)$$

Letting $R_1 = R_{17} = R$ gives the relationship

$$A_d = \frac{sC_{34}R^2R_8 + RR_8 + sC_2R^2R_8 + RR_8 + s^2C_2C_{34}R^2R_8^2 + R_8^2 + (C_2+C_{34})(sRR_8^2)}{s^2C_2C_{34}R^2R_8^2 + R_8^2 + (C_2+C_{34})(sRR_8^2)}. \qquad (3.56)$$

Simplifying equation 3.56 yields:

$$A_d = \frac{s^2C_2C_{34}R^2R_8^2 + sRR_8\{C_2R + C_{34}R + R_8(C_2+C_{34})\} + R_8^2 + 2RR_8}{s^2C_2C_{34}R^2R_8^2 + R_8^2 + (C_2+C_{34})(sRR_8^2)}, \qquad (3.57)$$

$$A_d = \frac{s^2C_2C_{34}R^2R_8 + sR\{C_2R + C_{34}R + R_8(C_2+C_{34})\} + R_8 + 2R}{s^2C_2C_{34}R^2R_8 + R_8 + (C_2+C_{34})(sRR_8)}, \qquad (3.58)$$

and finally,

$$A_d = \frac{s^2 C_2 C_{34} R^2 R_8 + sR\{(R+R_8)(C_2+C_{34})\} + R_8 + 2R}{s^2 C_2 C_{34} R^2 R_8 + (C_2+C_{34})(sRR_8) + R_8}. \qquad (3.59)$$

Consider equation 3.59 in the frequency domain, i.e. s→jω. As ω increases to infinity A_d approaches unity. As ω tends to zero A_d approaches a constant given by

$$\frac{R_8 + 2R}{R_8}, \qquad (3.60)$$

where as R_8 approaches 0 and R approaches infinity A_d tends to infinity.

The gain equation of the voltage gain stage and that of the complete amplifier is given by

$$G = 1 + \frac{2R_1}{R_8}. \qquad (3.61)$$

At the lower frequencies, the capacitors can be ignored. They only influence the circuit at the higher frequencies. Figure 3.11 is the frequency response of the differential stage as it appears in figure 3.8 with a gain of 1.2, with C_2, C_3, C_{34} and C_{35} absent.

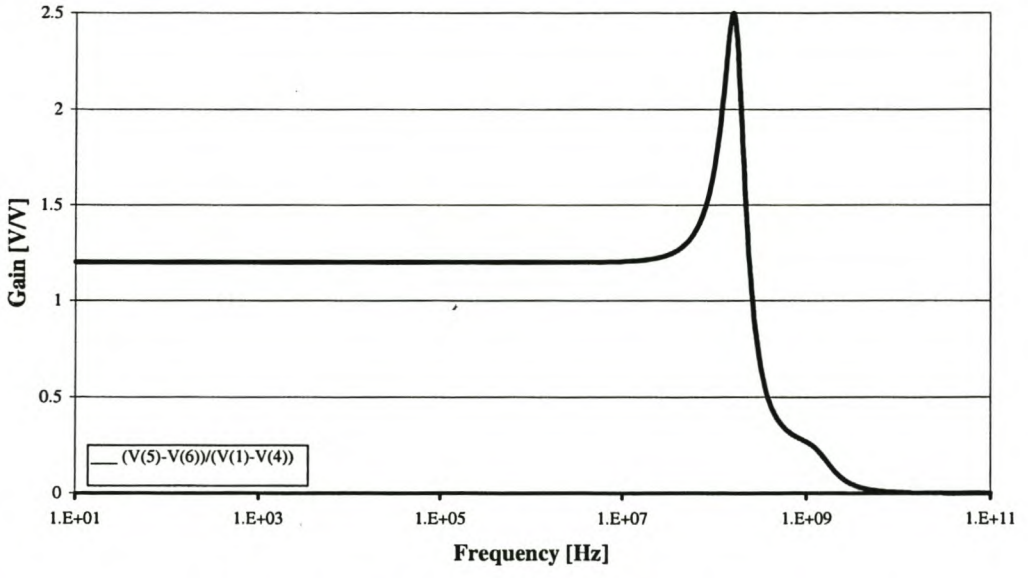


Fig. 3.11: ***Frequency response of amplifier stage without capacitors C_2, C_3, C_{34} and C_{35}.***

At the higher frequencies, there is a noticeable 2.5 V peak as the circuit moves away from its

ideal behaviour. This peak can be reduced significantly by putting capacitors C_2, C_3 and C_{34}, C_{35} in parallel with R_1 and R_{17} respectively. Simulations show that an overall capacitance of 15 pF was each required across R_1 and R_{17}. Since this value of a capacitor was not easily obtainable in surface mounts packaging, two 33 pF capacitors were used in series to obtain an equivalent capacitance of 16.5 pF. Figure 3.12 shows the frequency response of the differential stage with the four capacitors inserted. Although the –3 dB frequency bandwidths of figures 3.11 and 3.12 are approximately equal, there is a significant drop in the peak evident in figure 3.11 to approximately 1.4 V in figure 3.12.

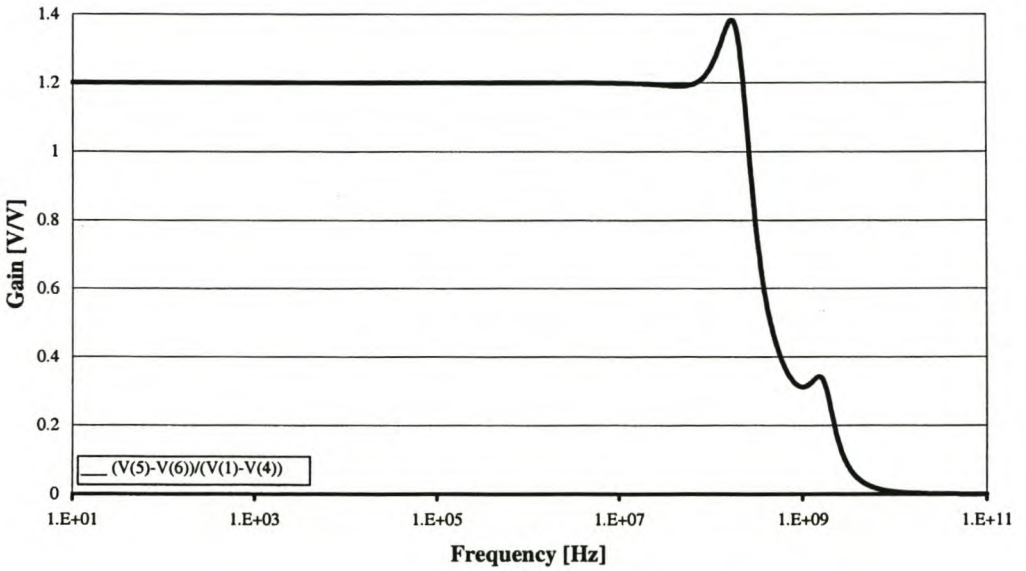


Fig. 3.12: ***Frequency response of amplifier stage with capacitors C_2, C_3, C_{34} and C_{35}.***

As mentioned before the 3 dB bandwidth also depends on the power supply voltage. As the voltage decreases, the magnitude of the internal junction capacitances increases which results in a reduction in the closes-loop bandwidth. To compensate for this, smaller values of feedback resistors must used at lower supply voltages [38]. This limits the resistors to a maximum value of approximately 1 kΩ. Considering this, R_1 and R_{17} were chosen as 100 Ω each. The matching of R_1 and R_{17} is important to maintain a good Common Mode Rejection Ratio (CMRR). R_8 is the variable resistor and it provides a means of adjusting the gain over

a wide range without degrading the CMRR.

Although the p.c. board was manufactured for a gain of 1.2, simulation results included in this chapter are for a gain of 5 (R_8 = 50Ω) to give an indication of the achievements of the subsystem. Figures 3.13 and 3.14 show transient and frequency responses of the circuit as it appears in figure 3.8 for a gain of 5. A 0.1 V, A.C. input was used for the frequency response and a 0.1 V, 10 MHz sinusoidal input was used for the transient analysis. The *Pspice* simulation programs are given in Appendix A.

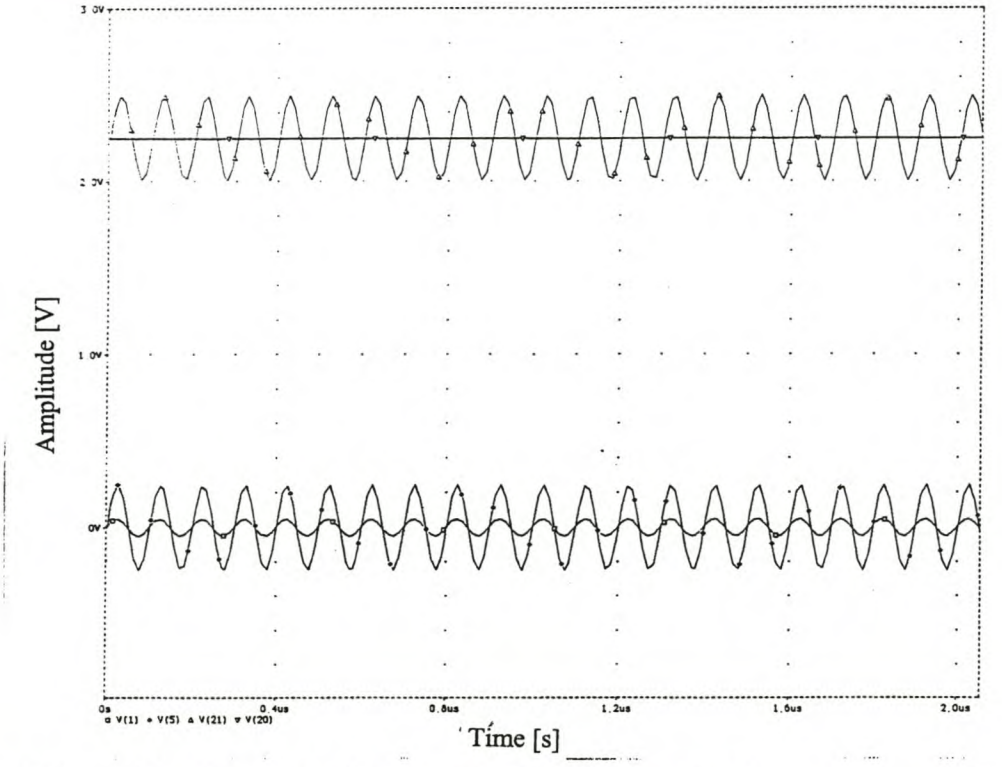


Fig. 3.13: ***Simulated transient response of the input and output voltages of each stage of the integrated implementation (for a gain of 5).***

Figure 3.13 shows the output of each stage of the amplifier for the top half of figure 3.8. The results are mirror-imaged for the bottom half of the circuit. A plot of V(1) and V(5) in figure 3.13 shows the transient response of the differential stage of the amplifier for a 0.1V, 10 MHz input. The differential input stage amplifies the 0.1 V input signal by 5.

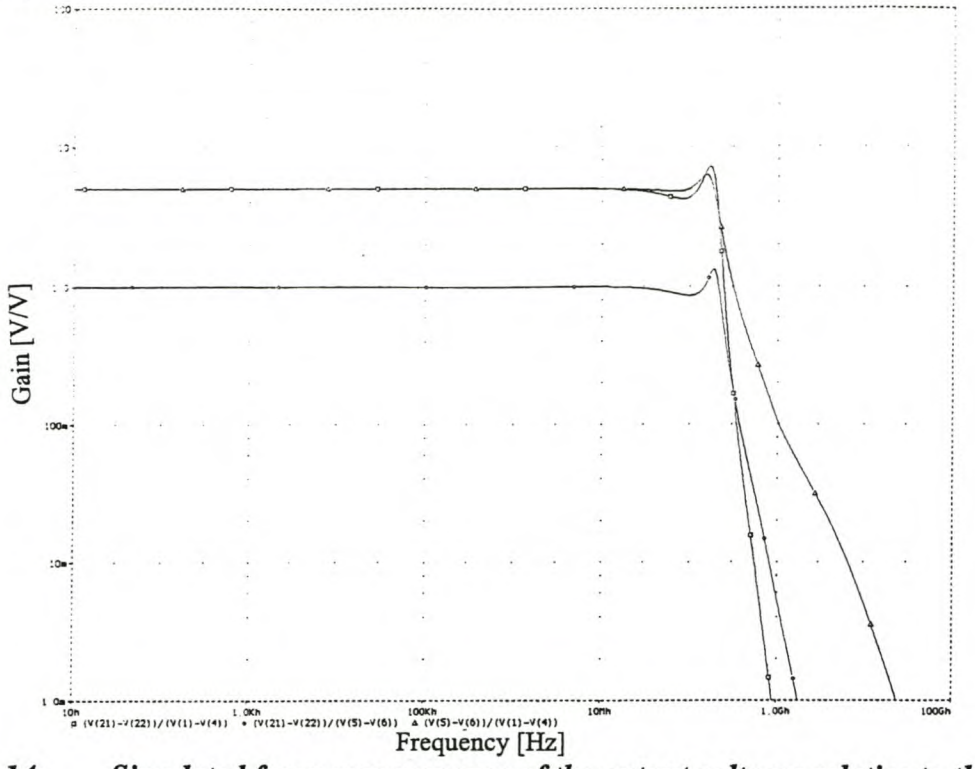


Fig. 3.14: ***Simulated frequency response of the output voltages relative to the inputs, for each stage of the integrated implementation (for a gain of 5).***

A plot of the voltages at the outputs of the differential input stage (denoted by nodes (5) and (6) in figure 3.8) relative to the inputs of the stage (denoted by nodes (1) and (4) in figure 3.8) i.e. (V(5)-V(6))/(V(1)-V(4)) in figure 3.14 shows that this stage of the amplifier contributes to the overall gain (approximately 5 in this simulation) of the subsystem

3.3.4 Level shifting circuit

This is a low distortion circuit that receives a differential input from the differential input stage and delivers a differential output, V_{O3} and V_{O4} (as denoted in figure 3.8), centred around +2.25 V to the ADC. The circuit consists of operational amplifiers U_2 and U_6, resistors R_2 - R_6, R_{12} - R_{16}, R_9 and R_{18}, capacitors C_4, C_{10}, C_{23} and C_{36} and diodes D_1 and D_2 as shown in figure 3.8. Besides the factors like offset and bandwidth as discussed in 3.3.1, the other important criterion when choosing U_2 and U_6 was to use operational amplifiers with low distortion. The AD811's distortion levels were sufficient for the level shifting circuit. The BAS32 diodes manufactured by *Philips* [40] have a high switching speed and are employed to guarantee a low distortion +3.35 V output swing. The suggested circuit given in

the ADS800's datasheets [41] was modified to achieve a gain of one for the level shifting circuit.

If the capacitors and diodes are ignored temporarily, one leg of the level shifting circuit can be represented as shown in figure 3.15.

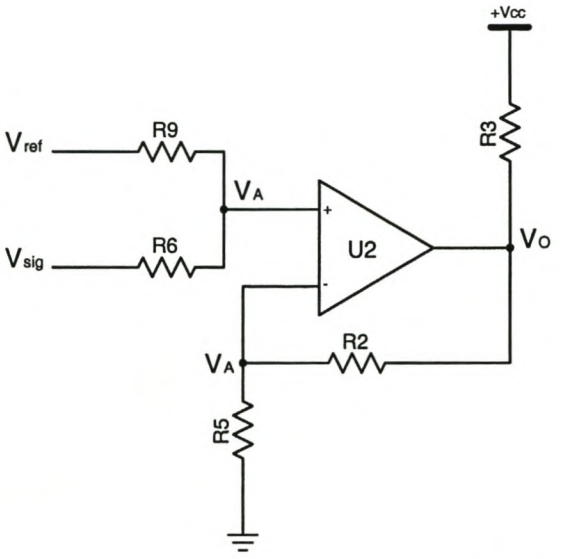


Fig. 3.15: Representation of the level shifting circuit of the integrated implementation.

A relationship between the resistors in question and the gain needs to be established. Assuming that U_2 is an ideal operational amplifier having infinite gain and infinite input impedance. A relationship between V_{ref}, V_{sig}, V_A, R_6 and R_9 is given by

$$\frac{V_{ref} - V_A}{R_9} = \frac{V_A - V_{sig}}{R_6} \qquad (3.62)$$

Therefore

$$V_{ref}R_6 - V_AR_6 = V_AR_9 - V_{sig}R_9 \qquad (3.63)$$

and

$$V_A = \frac{V_{ref}R_6 + V_{sig}R_9}{R_6 + R_9}. \qquad (3.64)$$

Also

$$V_A = (\frac{R_5}{R_2 + R_5})V_O \qquad (3.65)$$

and

$$V_O = V_A(\frac{R_2 + R_5}{R_5}). \tag{3.66}$$

Equating equations 3.62 and 3.64 yields

$$V_O = (\frac{V_{ref}R_6 + V_{sig}R_9}{R_6 + R_9})(\frac{R_2 + R_5}{R_5}) \tag{3.67}$$

and

$$V_O = (V_{ref}R_6 + V_{sig}R_9)\frac{R_2 + R_5}{R_5(R_6 + R_9)}. \tag{3.68}$$

If $R_2 = R_5 = R_6 = R_9$, then

$$V_O = (V_{ref} + V_{sig}). \tag{3.69}$$

This will hold true similarly for the other leg of the circuit since the two parts are identical. To ensure a gain of 1 and taking into consideration the requirement of small feedback resistors when using the AD811 [38], all the resistors were chosen as 220 Ω. Capacitors C_4 and C_{36} are used to reduce the peak ocurring at the outputs i.e. nodes (21) and (22) of figure 3.8. *Pspice* simulations proved that 5.6 pF were the ideal capacitance choice.

Capacitors C_{10} and C_{23} minimise current glitches resulting from the switching in the input track and hold stage of the ADC. It is also used to improve signal-to-noise performance. Values of 22 pF values have been suggested in the ADS800 datasheet [41]. These capacitors can also be used to create a low pass filter and effectively reduce the noise bandwidth. R_4 and R_{14} were added in series with the capacitors to establish a real pole. The matching of RC constants is essential to optimise the circuit. The RC constant of C_4 and R_2 is approximately 800 Mrad/s, which should also be the RC constant for R_4 and C_{10}. The same analogy can be drawn for R_{14} and C_{23} using R_{18} and C_{36}. The values of R_4 and R_{14} using the relationship

$$800 * 10^6 = \frac{1}{22 * 10^{-12} F.R} \tag{3.70}$$

Therefore

$$R_4 = R_{14} = 56\Omega. \tag{3.71}$$

The cut-off frequency, f_c, of the filter is given by

$$f_c = \frac{1}{2\pi R(C + C_{ADC})}, \tag{3.72}$$

where C_{ADC} is the internal input capacitance of the ADC (typically 4 pF).
Therefore

$$f_c = \frac{1}{2\pi 56\Omega(22pF + 4pF)} = 100MHz. \tag{3.73}$$

A plot of the voltage at node (21) i.e. V(21) in figure 3.13 shows that level shifting cicuit centres the output around 2.25 V. A plot of the voltages at the outputs of the level shifting circuit (denoted by nodes (21) and (22) in figure 3.8) relative to the inputs of the stage (denoted by nodes (5) and (6) in figure 3.8) i.e. (V(21)-V(22))/(V(5)-V(6)) in figure 3.14 shows that the gain of this stage is unity.

3.3.5 Buffer

This circuit buffers the reference signal that the level shifting circuit receives from the ADC. The buffer consists of operational amplifier U_3, resistors R_7, R_{10} and R_{11} and capacitors C_{16} and C_{11}. An AD811 was used instead of the OPA130 since it is also able to buffer the reference signal to drive the external circuitry and is pin compatible with the OPA130. The resistor values suggested in the ADS800 datasheet were used. The 2.25 V reference signal that the ADC supplies will be discussed in Chapter 4.

3.3.6 Test results

Figures 3.13 and 3.14 show transient and frequency responses of figure 3.8 for a gain of 5. A 0.1 V, A.C. input was used for the frequency response and a 0.1 V, 10 MHz sinusoidal input was used for the transient analysis. Figure 3.13 shows the output at each stage of the amplifier for the top half of the figure 3.8. The results are mirror-imaged for the bottom half

of the circuit. The differential input stage amplifies the input signal by 5 and the level shifting cicuit centres the output around the 2.25 V reference signal supplied by the buffer. Figure 3.14 shows that the differential stage only contributes to the voltage gain of the complete integrated implementation. All four stages of the amplifier begin to degrade well past the 10 MHz mark. Similar frequency and transient responses are achieved at gains of 1.2, 2 and 10.09.

Figure 3.10 gives the frequency response of the circuit for a gain of 1.2. A –3 dB bandwidth of approximately 220 MHz is achieved with a pole at approximately 190 MHz. When tested independently of the other subsystems appearing on the p.c. board the practical results achieved matched well with the simulated results in terms of bandwidth expectations. For a gain of 1.2, the frequency response of the practical circuit began degrading well past the 10 MHz mark. However, once the other subsystems were added onto the p.c. board the analog system began to show oscillations of 40 MHz and 25 MHz. Since a two-layer board was used for prototyping purposes, there are no separate ground and power planes. Also since routing on a two-layer board proved difficult, many ground and power connections were done externally using wires after the board was manufactured. This created many inductance loops. The 40 MHz and 25 MHz crystal oscillators on the board produced the oscillations present in the analog system. It is recommended that for future use a four-layer board needs to be used.

The outputs of the subsystem were not referenced around 2.25V as predicted by *Pspice*, but around approximately 2.1V instead. Node (15) is at approximately 2 V instead of the expected 2.25 V. It was evident that the 2.25 V reference signal from the ADS800 was attenuated thereby resulting in the level shifting circuit not referencing the output signals of the amplifier around 2.25 V, but 2.1 V instead. The AD811 datasheets confirm that the operational amplifier has a very low input impedance and loads the ADS800 thereby offsetting the 2.25 V reference signal. In future boards this needs to be considered and preferably the OPA130 used instead.

3.4 Conclusion

In this chapter both the discrete and integrated implementation of the analog signal conditioning subsystem were investigated. Both implementations were designed to serve as an amplifier and a 1st order low pass filter that transforms the input signal levels from the sensor to those required by the ADC.

From figures A.4 and A.12 in Appendix A, –3 dB bandwidths of approximately 114 MHz and 20 MHz are achieved for the input and amplifier stages respectively. Practical results compared well with the simulated results. By combining the input stage to the amplifier stage a good amplifier design is obtainable. Transistor arrays with higher breakdown voltages are required so that the input stage can be implemented using the free transistors in the arrays of the amplifier stage. Admittedly individual transistors having high breakdown voltages are easily obtainable but the circuit becomes too big and cumbersome with them. In terms of board space the design becomes much more expensive especially since the application of this system is for a portable sensor. Besides the cost factor, the transistors will also not be thermally and electrically matched as those in an array. Figure 3.10 gives the frequency response of the circuit for a gain of 1.2. A –3 dB bandwidth of approximately 220 MHz is achieved with a pole at approximately 190 MHz Practical results compared well with the simulated results.

From the simulated and practical results it appears that with regards to bandwidth expectations the integrated implementation of the analog signal conditioning subsystem is better than that of the discrete implementation for the given application. However, if higher bandwidths are required the discrete implementation needs to be examined more closely and optimised further by combining the input and amplifier stages utilising matched transistor arrays.

4 DIGITAL SIGNAL CONDITIONING SUBSYSTEM

4.1 Introduction

This chapter discusses the digital signal conditioning subsystem. An overview of the system is presented in block diagram form followed by a detailed, functional description of each block.

4.2 Block diagram representation

The purpose of this subsystem is to digitise the analog signal, to integrate and decimate the digitised data and to perform range selection. Figure 4.1 shows the block diagram representation of this subsystem.

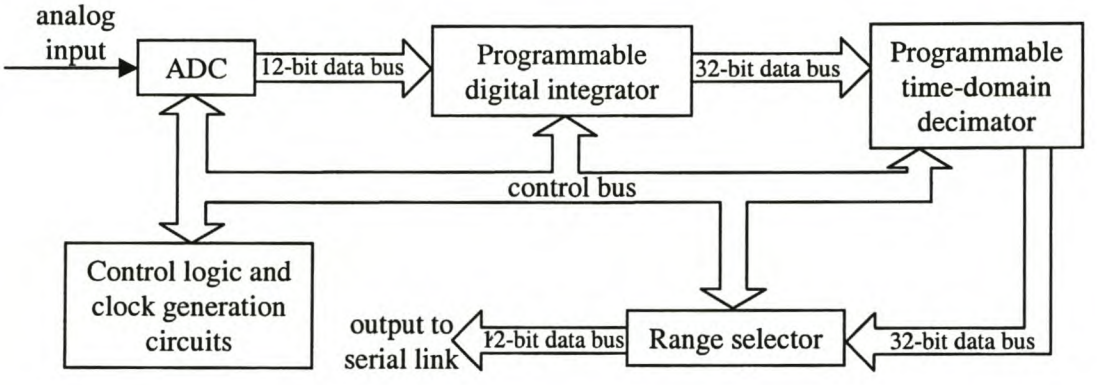


Fig. 4.1: ***Block diagram representation of the digital signal conditioning subsystem.***

The differential analog output from the amplifier as discussed in Chapter 3 serves as an input for the ADC. The ADC is a 40 MHz, 12-bit device which accepts differential input signals of ± 1 V centred around 2.25 V. It samples the input and converts it to a sequence to digital values at CMOS levels. A parallel, 12-bit output is delivered to the programmable digital integrator. Some control logic and clock generation circuits support

the system.

The programmable digital integrator, programmable time-domain decimator, range selector and the control logic and clock generation circuits are implemented on a single *Altera* Flex 10K FPGA. The Flex 10K devices operate with a 5 V supply voltage. The 10K family offers a range of FPGAs that varies in both speed and size. The Flex 10K10 is used with 84 pins and a speed rating of -4. Currently with the existing program, more than 80% of the available pins are used and the chip runs at 43.85 MHz. For easy routing of the p.c.board, many of the pins had to be pre-assigned on the chip. Since the maximum desired operational speed of the FPGA is 40 MHz, adding future logic changes to the program will result in the FPGA running out of pins and perhaps slowing down as well. Also of consideration is the fact that the bigger and faster the FPGA, the higher the power consumption of it. For prototyping purposes all unused pins have been reserved and routed to headers on the p.c.board in the event of further use of them for test purposes.

The programmable digital integrator adds the digitised data and the data is transferred to the programmable time-domain decimator. The programmable time-domain decimator controls the rate at which data is transmitted to the serial fibre-optic link. If sampling at the full sampling speed of 40 MHz or any speed greater than 8.391 MHz it is necessary to decimate the datastream from the integrator before transmitting it over the link. Each stage is controlled by the control logic and the clock generation circuits. The integrator delivers a parallel 32-bit output to the range selector wherein the 12 most significant bits are transferred to the serial fibre-optic link.

The FPGA was programmed using *Maxplus* software using VHDL. A design may be implemented in VHDL using behavioural architecture, structural architecture or dataflow or a combination of them [25]. Since this subsystem needs to be optimised for speed and board space, the behavioural architecture was used. VHDL is a descriptive language and the VHDL programs are self-explanative. In addition, the VHDL codes in this thesis have been thoroughly commented to simplify understanding of them further. In this chapter block diagram representations of the VHDL implementation are given as well to give an

idea of the implementation of the program. To understand completely the implementation of this subsystem, it is recommended that the VHDL code be used in conjunction with the block diagram representations. The VHDL program for the FPGA is given in Appendix B and its pin assignments are given in Appendix B, figure B.1. For prototyping purposes, provision has been made for programming the FPGA using two different configurations, viz. passive serial (using either an Erasable Programmable Read-Only Memory (EPROM) or an Electrically Erasable Programmable Read-Only Memory (EEPROM)) and Joint Test Action Group (JTAG). The complete circuit design and p.c. board layout of the digital signal conditioning subsystem is given in Appendix C, figures C.1, C.3, C.4 and C.6.

4.3 Functional description of the subsystem components

4.3.1 Analog to digital converter

The standard lightning impulse, with its initial risetime of 1 μs and falltime of 50 μs [11] has been chosen as the reference input signal. In order to obtain resolution of the order of at least ten sampling points on the rising edge of this impulse, a minimum sampling frequency of 10 MHz is required. Figure 4.2 shows the impulse (solid line) with its differentiated version (broken line). The impulse is magnified by a factor of 10^5 to allow the two graphs to be represented on the same set of axes.

The impulse can be represented by the relationship [11]

$$V(t) = V_o[\exp^{-t/\tau_1} - \exp^{-t/\tau_2}], \qquad (4.1)$$

where τ_1 and τ_2 are time-constants with $\tau_2 < \tau_1 << 1$,

t represents time in microseconds and V_o is an arbitrary constant related to the maximum voltage of the impulse.

Differentiating this impulse yields

$$\frac{dV}{dt} = -\frac{V_o}{\tau_1}\exp^{-t/\tau_1} + \frac{V_o}{\tau_2}\exp^{-t/\tau_2}. \qquad (4.2)$$

For a voltage V_o of 1 V, numeric calculations give approximate values of 72 and 16.5 μs

for τ_1 and τ_2 respectively.

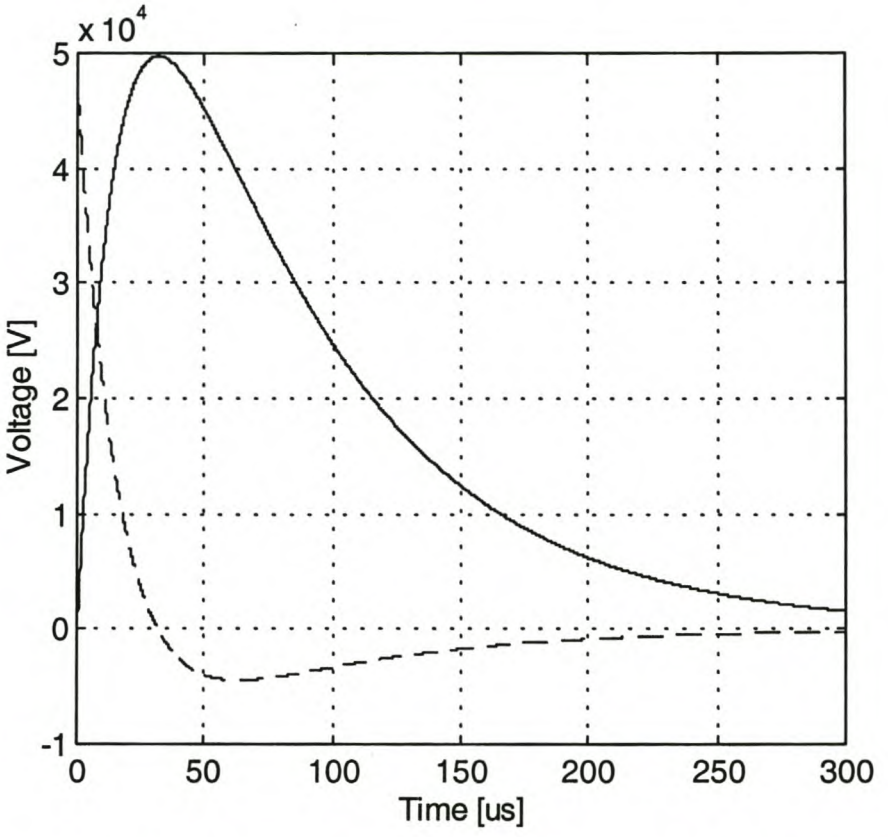


Fig. 4.2: ***Standard lightning impulse and its derivative. Solid line: impulse magnified by 10^5, dashed line: derivative of impulse.***

Figure 4.2 shows the dynamic range and offset problems that impose unique conditions on the integration instrumentation. Although in figure 4.2 the risetime of the differentiated version of this impulse appears to be infinite, in reality it is finite but extremely fast. A higher sampling rate, before digital integration, of the falling edge of the differentiated impulse is required to accurately represent the rising part and peak of the impulse. The peak of the impulse is of importance since the most information is mostly related to the peak value or a substantial percentage of the peak value of the signal.

Amplitude resolution of 8 bits (which yields resolution of the order of 1% of maximum reading) is normally regarded as adequate for impulse measurements. Phenomena

involving high frequency noise superimposed on the fundamental waveform, however, require better resolution.

Considering the above as well as price and availability, the ADS800 manufactured by *Burr Brown* was selected. It is a low power, high speed ADC offering a conversion speed of 40 MHz with 12-bit resolution. In terms of the Nyquist criteria for sampled signals, this allows an analog signal containing frequencies from DC to 20 MHz to be adequately sampled and reconstructed. Figure 4.3 illustrates the block diagram of the ADS800 [41]. Its implementation in the developed system is given in Appendix C, figures C.1 and C.3. It uses a fully differential architecture and digital error correction to ensure 12-bit resolution.

The ADS800 consists of 12-bit quantizer, wideband track/hold, reference and three-state output. It requires a single +5 V supply for operation and can be implemented to accept either a differential or single-ended input. The former has been chosen for the system under development.

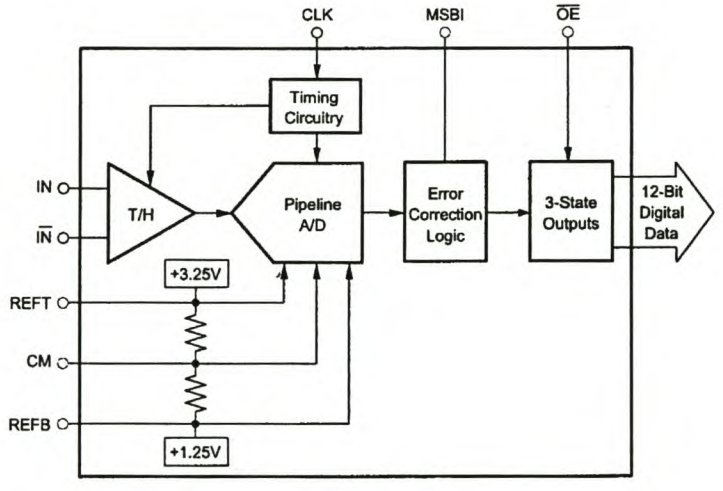


Fig. 4.3: Block diagram of ADS800 [41].

4.3.1.1 Analog input and internal reference

The analog input of the ADS800 can be configured in to receive either single-ended or

differential inputs and can driven with different circuits depending on the type of signal and the required performance of the ADC. In the developed system inputs *IN* and */IN* to the ADS800 are configured to accept differential ± 1 V signals centred around 2.25 V.

Figure 4.4 shows the internal reference structure of the circuit that sets the full-scale range of the ADC [41]. *REFT* is the top reference connection used for the external capacitive bypassing of the internal 3.25 V reference point. *REFB* is the bottom reference connection used for the external capacitive bypassing of the internal 1.25 V reference point. *CM* is the common-mode output given by $(V_{REFT}+V_{REFB})/2$.

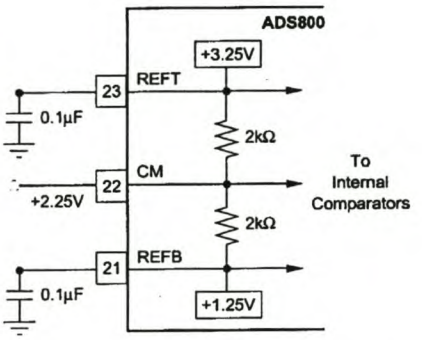


Fig. 4.4: ***Internal reference structure of ADS800 [41].***

As shown in figure 4.4, both the positive and the negative full-scale references are brought out for external bypassing with 0.1 µF capacitors. Further, the *CM* value is used as the reference signal for the analog signal conditioning subsystem. It provides the appropriate offset for the driving circuitry. The buffering of the signal before use has been discussed in section 3.3.5. Each input of the differential input range is centred around 2.25 V, thereby allowing each of the two inputs a full-scale range of 1.25 V to 3.25 V.

4.3.1.2 Track/hold circuit

Figure 4.5 shows the differential track/hold configuration with timing signals [41]. An internal clock controls the switches. The internal clock has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. In the first clock phase only the switches labelled $\phi 1$ are closed. The

input signal is sampled on the left plates of the input capacitors (C_I). The non-ideal properties of the operational amplifier cause the feedback capacitors (C_H) to be simultaneously loaded with the difference between the operational amplifier bias voltage and the common-mode voltage (V_{CM}). In the next clock phase the switches labelled $\phi 2$ close whilst those labelled $\phi 1$ are opened. The left plates of the input capacitors (C_I) are connected and the feedback capacitors (C_H) are switched to the operational amplifier output. At this time, the charge redistributes between C_I and C_H, thus completing one track/hold cycle [41].

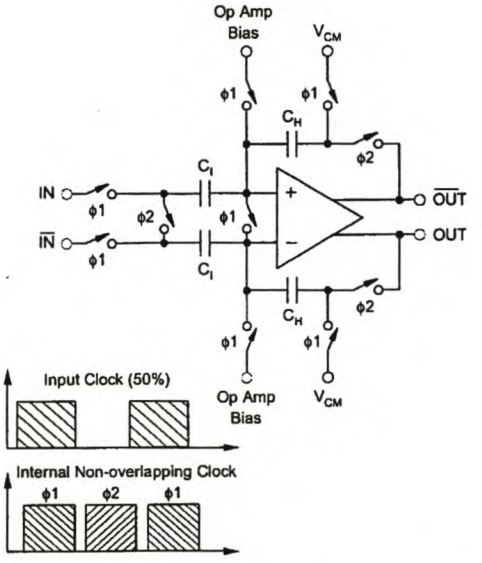


Fig. 4.5: Track/hold configuration with timing signals [41].

The above set-up ensures that the two feedback capacitors cancel each other, making the differential output independent of the operational amplifier bias voltage and V_{CM}. The differential output is a held DC equivalent of the analog input at the sample time and this is made available to the pipeline ADC.

4.3.1.3 Pipeline ADC and error correction logic

Figure 4.6 shows the architecture of the pipeline ADC with error correction logic [41]. It

has 11 stages, each consisting of a 2-bit flash ADC and a 2-bit DAC. Each 2-bit ADC digitises on the edge of the sub-clock. The sub-clock operates at twice the frequency of the externally applied clock (*CLK*) as shown in figure 4.3. The external clock receives its clock from *ADCLK*, which is derived from the 40.000 MHz crystal oscillator that clocks the FPGA. Although the ADC is a 40 MHz device, it may be used at lower speeds. Therefore to vary the sampling speed of the ADC *ADCLK* is a variable clock. It ranges from 40 MHz to one-fifteenth of 40 MHz. *ADCLK* follows the master clock, i.e. *MCLK*, which is generated in clock generation circuits implemented in the FPGA. This will be discussed in section 4.3.5. The *Maxplus* programming code for the generation of *ADCLK* is given in Appendix B.

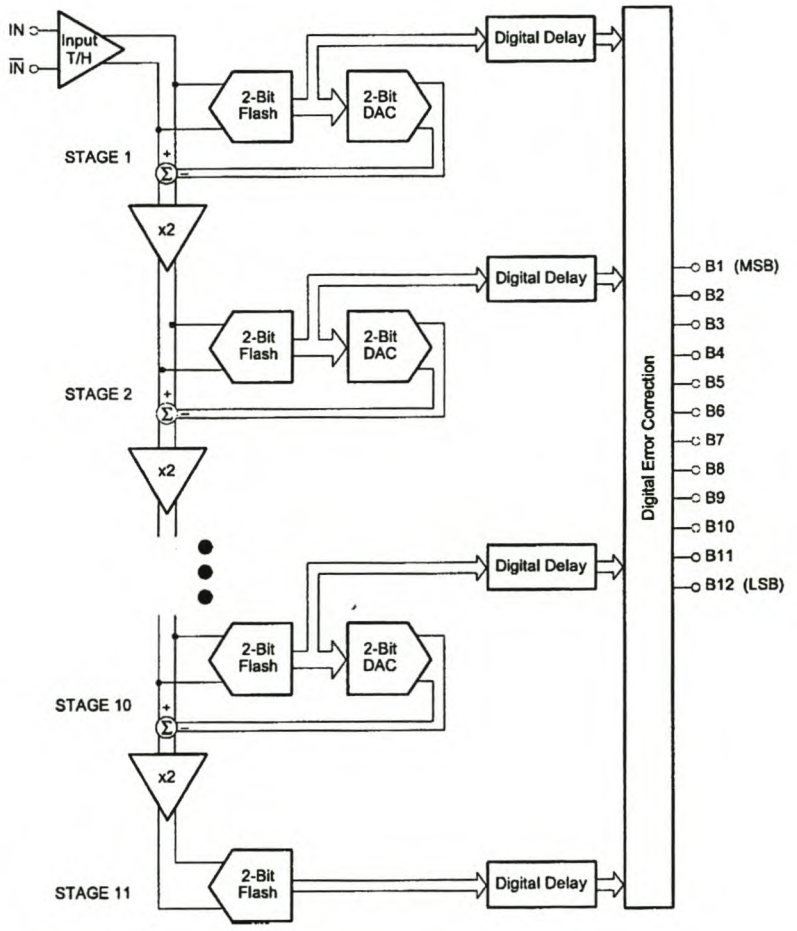


Fig. 4.6: Pipeline ADC and error correction logic [41].

The output of each ADC is delivered to its own delay line in order to synchronise it with

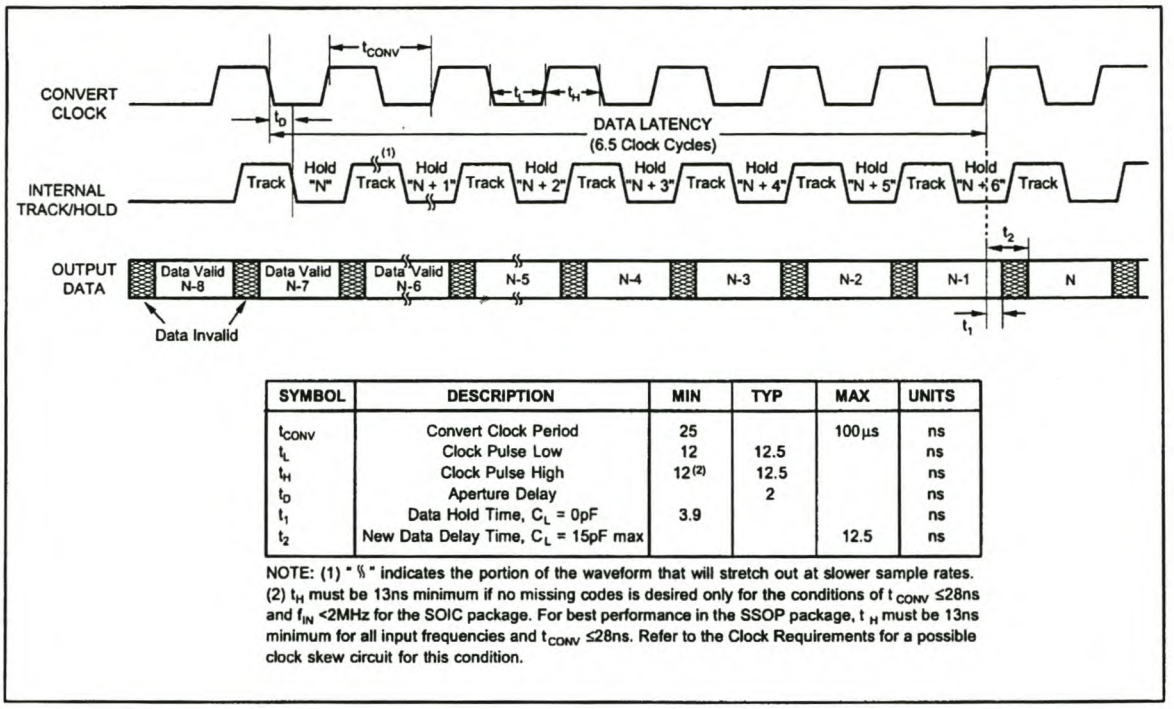
the data generated from the following pipeline stages. The rising and falling edges of the *ADCLK* control the interstage conversions in the pipeline. Various factors like clock signal jitter, rise and fall times and duty cycle can affect the performance of the pipeline. A 50% duty cycle is required and a minimum rise/fall time of 2 ns is optimal. Low clock jitter is also crucial. Once aligned, the data is transferred into a digital error correction circuit, which is able to adjust the output data on the basis of the information found on the redundant bits [41]. This conversion technique gives the ADS800 high performance and the pipeline technique gives the ADC excellent differential linearity and guarantees no missing codes at the 12-bit level.

4.3.1.4 3-state outputs

The 12-bit output data is generated at CMOS logic levels. The logic state of the most-significant-bit-inversion (*MSBI*) pin decides in which of the two possible coding schemes is used. When *MSBI* is held low, the output coding is in Straight Offset Binary (SOB). Here a full-scale input signal corresponds to all "1's" at the output. The alternative is Binary Two's Complement (BTC) coding, which occurs when *MSBI* is held high. Here the Most Significant Bit (MSB) is inverted. In the final system *MSBI* is tied to ground thereby forcing SOB coding. In the succeeding modules a stage has been included wherein this SOB formatting is converted into BTC coding. This will be discussed further in section 4.3.2.1.

4.3.1.5 Timing relationships

Figure 4.7 shows the timing diagram of the output data relative to the conversion clock, i.e. *ADCLK* and the internal track/hold [41]. On the falling edge of *CONVERT CLOCK*, i.e. *ADCLK*, the track and hold switches to hold after a time of t_D and data is available to be latched to the output. This current data is available for a time of t_1 after the next rising edge of *ADCLK*.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse Low	12	12.5		ns
t_H	Clock Pulse High	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTE: (1) " ⟆ " indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of t_{CONV} ≤28ns and f_{IN} <2MHz for the SOIC package. For best performance in the SSOP package, t_H must be 13ns minimum for all input frequencies and t_{CONV} ≤28ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

Fig. 4.7: Timing diagram for ADS800 [41].

4.3.2 Programmable digital integrator

As discussed before, the programmable digital integrator has been implemented on the FPGA using VHDL. The programming code is given in Appendix B. Figure 4.8 shows a high-level block diagram of the programmable digital integrator.

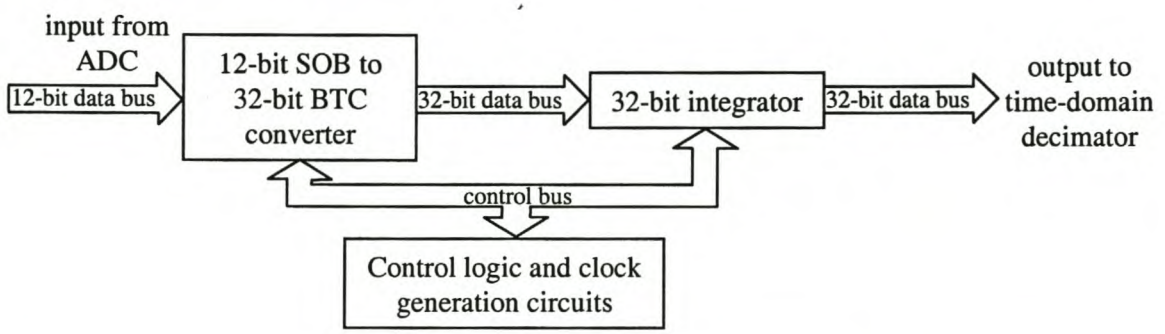


Fig. 4.8: Block diagram representation of the programmable digital integrator.

The 12-bit SOB output from the ADC is latched into the 12-bit SOB to 32-bit BTC

converter. The 32-bit output data from the converter is then integrated to yield a 32-bit data bus that is transferred to the time-domain decimator. Some control logic and clock generation circuits also support these sections. This will be discussed further in section 4.3.5.

4.3.2.1 12-bit straight offset binary to 32-bit binary two's complement converter

Before designing the integrator, it is necessary to calculate the maximum resolution that it should have. Consider a square wave with a maximum voltage of V_{max} as shown in figure 4.9. A square wave is used, as this is the worst case situation that can occur. The base frequency, ω_ω, is 50 Hz since the system has power system applications. The sampling frequency, f_s, is 40 MHz considering the maximum sampling frequency of the ADC. V_{max} denotes the maximum voltage obtainable.

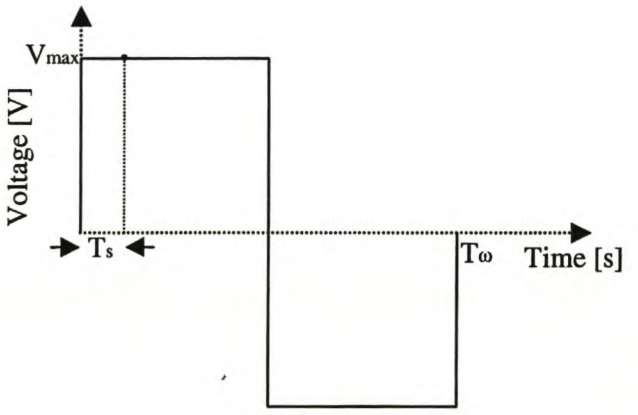


Fig. 4.9: ***Square wave representation of the input signal.***

For the sake of simplicity, and to maintain a worst case representation, it is assumed that the base period, T_ω, is an even multiple of the sampling period, T_s. The worst case will be obtained for a maximum ratio of T_ω/T_s. In practice, this translates to T_ω = 1/50 Hz and T_s = 1/40 MHz.

Consider one half of the square wave. Then the number of sampling points in $\frac{1}{2}T_\omega$ is

given by,

$$N_{T_s/2} = \frac{T_\omega}{2T_s}. \qquad (4.3)$$

The area contained within half the square wave gives the maximum integral that can be obtained. This is given by the relationship

$$\sum_{t=0}^{N_{T_s/2}} X(t) = \sum_{t=o}^{T_\omega/2T_s} V_{\max} = V_{\max}(T_\omega/2T_s - 1)$$

$$= V_{\max}(f_s/2f_\omega - 1). \qquad (4.4)$$

Substitution into equation 4.4 yields,

$$\sum_{t=o}^{T_\omega/2T_s} V_{\max} = V_{\max}(\frac{40MHz}{2*50Hz} - 1)$$

$$= V_{\max}(400000 - 1)$$

$$\approx 400000(V_{\max}). \qquad (4.5)$$

Since the ADC is a 12-bit device, the maximum voltage at a point is, in hexadecimal, 7FF. The MSB is the sign bit that will be ignored for now since only the positive half of the square wave is being considered. Since there are 400 000 sampling points,

$$\sum_{t=o}^{T_\omega/2T_s} V_{\max} = 400000(7FF)$$

$$= 61A80 * 7FF$$

$$= 30CDE580. \qquad (4.6)$$

Converting equation 4.6 to binary yields ,

$$\sum_{t=o}^{T_\omega/2T_s} V_{\max} = 11\ 0000\ 1100\ 1101\ 1110\ 0101\ 1000\ 0000. \qquad (4.7)$$

From equation 4.7 it can be concluded that the maximum integration sum obtainable consists of 30 bits disregarding the sign bit. Accounting for the sign bit, 31 bits are required. Rounding off to the nearest byte, a 32-bit integrator is required.

As mentioned in section 4.3.1.4, the ADS800 can be configured to code in either SOB or BTC and the former is chosen for the ADC in this system. For the ease of operation of the integrator the data from the ADC needs to be converted into BTC format before integration. The importance of BTC formatting will be discussed in section 4.3.2.2. The

12-bit SOB to 32-bit BTC converter is implemented on the FPGA using *Maxplus* software. Figure 4.10 gives a block diagram representation of the functioning of the BTC converter as implemented in the FPGA using VHDL. The programming code, given in Appendix B, can be used together figure 4.10 to understand the implementation of the converter.

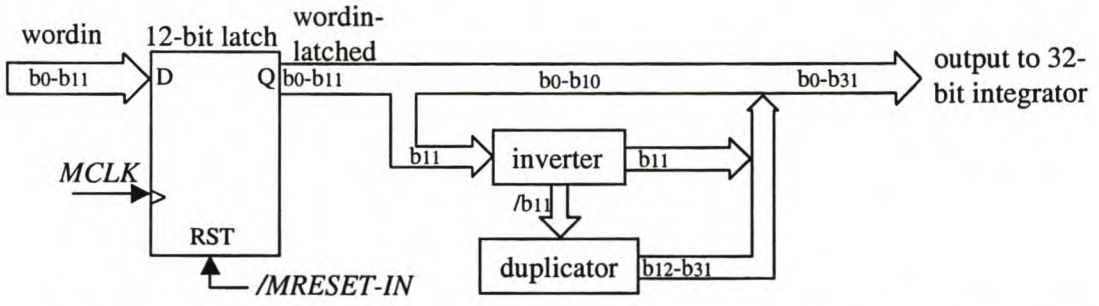


Fig. 4.10: Block diagram representation of the 12-bit SOB to 32-bit BTC converter.

The converter consists of a 12-bit latch, an inverter and a duplicator. During normal operation, on the first detected rising edge of *MCLK*, the 12-bit latch stores the SOB coded output from the ADC, i.e. wordin, and the inverter inverts the MSB of wordin-latched. The duplicator then sign-extends the inverted MSB to generate a 32-bit BTC word.

To convert a SOB number into BTC, the MSB of the SOB word must be inverted. Therefore the first 11 data bits are sent through as is and the MSB i.e. the 12^{th} bit, is inverted and sent through. This converts the 12-bit SOB word into 12-bit BTC. The 12-bit BTC word now has to be converted into a 32-bit word. Sign-extension makes it possible to convert an n-bit BTC number, X, into an m-bit number (where m>n) by padding X with m-n copies of either 1s or 0s depending on whether the number is negative or positive [32]. Sign-extension occurs as follows. The inverted, 12^{th} data bit is duplicated onto data bits 12 through 31 [32]. The 20-bit output generated by the duplicator is combined with the inverted MSB and the 11 bits of wordin-latched to create a 32-bit BTC word that serves as a 32-bit input for the integrator.

MCLK is generated from the 40 MHz crystal oscillator that clocks the FPGA. It may be divided down if desired. *ADCLK* mentioned in section 4.3.1.3 follows *MCLK*. This is

discussed in section 4.3.5. The */MRESET-IN* pin allows for the resetting of the 12-bit latch. A low on the master reset pin, i.e.*/MRESET-IN*, clears all information on the output of the latch and resets it to zero.

4.3.2.2 32-bit integrator

The 32-bit integrator is implemented on the FPGA using *Maxplus* software. Figure 4.11 gives a block diagram representation of the functioning of the 32-bit integrator as implemented in the FPGA using VHDL. The programming code, given in Appendix B, can be used together figure 4.11 to understand the implementation of the 32-bit integrator.

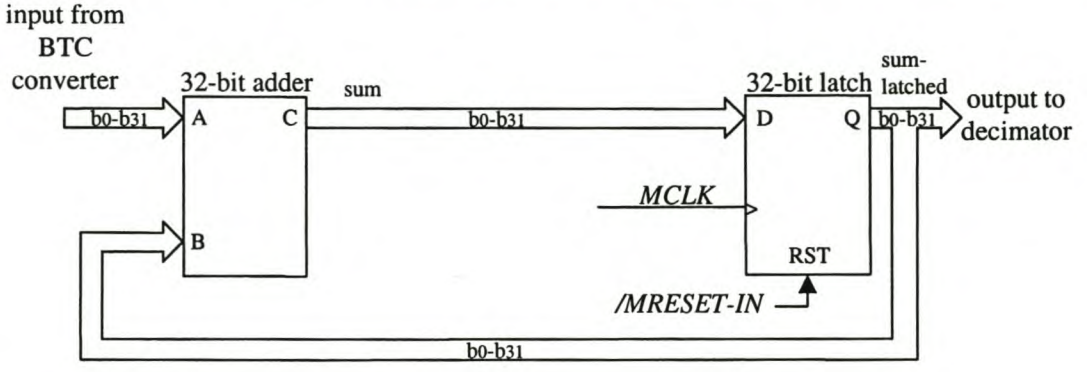


Fig. 4.11: Block diagram representation of the 32-bit integrator.

It essentially consists of a 32-bit adder and a 32-bit latch at the output interface. The adder adds the 32-bit input value from the BTC converter with the 32-bit word stored in the latch, i.e. sum-latched. On the first detected rising edge of *MCLK*, the 32-bit summed value from the adder, i.e. sum, is then latched and the summing continues. The value stored in the latch is set to zero at the start of a new integration cycle. A new integration cycle begins when the FPGA is reset with a low on the */MRESET-IN* pin.

BTC formatting has been chosen since it is preferred for arithmetic operation. In a two's complement number system numbers can be added directly without sign and magnitude checks[32]. In BTC if, for example, a 4 bit number is chosen from where to count upwards, each successive number can be obtained by adding one to the previous number

ignoring any carry overs beyond the fourth bit. Using any other formatting e.g. SOB and one's complements numbers will not allow this.

Applying this to addition, which is an extension of counting, BTC numbers can be added by ordinary binary addition, ignoring any carries beyond the MSB. This is true provided that the range of the number system is not exceeded. (The worst case situation was evaluated to determine the resolution of the integrator and it was established in section 4.3.2.1 that 31-bits are required to represent the maximum possible integrated sum.) Therefore two numbers in a complement system may be added directly. If two or more numbers are added in BTC format the MSB of the solution will indicate whether the resulting answer is either positive or negative. A number is negative if and only if its MSB is 1 [32]. In the developed system bit 32 is used to denote the sign of the integrated sum.

4.3.3 Programmable time-domain decimator

Since a 266 MBd serial link is used, at two bytes per sample (12-bit resolution with byte boundaries), this allows for a data rate of 16.625 Msamples/s. The maximum rate of transmission of data to the transmitting module of the link is actually 8.391 MHz and this will be discussed further in Chapter 5, section 5.3.1.2. The maximum speed at which data can be transferred from the FPGA is 8.391 MHz. Therefore it may be necessary to decimate the datastream if sampling at any speed higher than 8.391 MHz. The time-domain decimator and *MCLK* (which controls sampling speed of ADC) can be used together to control the rate at which data is delivered to the transmitter.

The programmable time-domain decimator is implemented on the FPGA using *Maxplus* software. Figure 4.12 gives a block diagram representation of the functioning of the time-domain decimator as implemented in the FPGA using VHDL. The programming code, given in Appendix B, can be used together figure 4.12 to understand the implementation of the programmable time-domain decimator. It essentially features a 32-bit latch. The output from integrator is latched and an output, decimated if necessary using WORDOUT-

CLK, is sent through the range selector to the serial link.

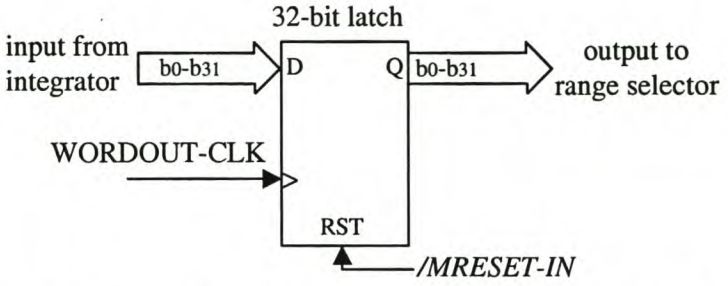


Fig. 4.12: ***Block diagram representation of the programmable time-domain decimator.***

The programmable time-domain decimator requires a decimated version of *MCLK*. This clock, WORDOUT-CLK is the variable decimation clock and controls the frequency at which data is transmitted over the link. WORDOUT-CLK ranges in integer value from *MCLK* to one-sixteenth of *MCLK*. The generation of WORDOUT-CLK is given in the VHDL program for the FPGA in Appendix B. It will be discussed further in section 4.3.5 with the clock generation circuits.

4.3.4 Range selector

The range selector is implemented on the FPGA using *Maxplus* software. The VHDL programming code for this is given in Appendix B. The range selector chooses the 12 most significant bits from the 32 bits generated by the programmable time-domain decimator. The choice of which 12 bits go over the serial link is controlled externally by means of a switch viz. *DIPSWB(0..7)*. Table 4.1 shows the selection process depending on the setting of the dipswitch.

Any higher setting on the dipswitch after "10011" results in the most significant 12 bits being selected. There are 21 possibilities beginning with the last 12 bits and ending with the first 12 bits. Only 5 bits i.e. *DIPSWB(0..4)* of the dipswitch are needed to allow for the 21 possibilities. This means that *DIPSWB(5..7)* is available for future use if further

modifications are required.

Table 4.1: Range selection process.

Dipswitchb(5..7)	12-bit data selection
00000	b0..b11
00001	b1..b12
00010	b2..b13
00011 : :	b3..b14 : :
10011	b19..b30
10100 :	b20..b31 :
11111	b20..b31

Upon resetting the FPGA, the data appearing at the outputs of the range selector is '000000000000'. During normal operation, on the first detected rising edge of WORDOUT-CLK the 12-bit data selected using the range selector appears at the output pins of the FPGA.

4.3.5 Control logic and clock generation circuits

The control logic and clock-generation circuits are implemented on the FPGA using *Maxplus* software. Figure 4.13 gives a block diagram representation of the control lines that are of importance. These control lines have been discussed briefly throughout the chapter. The programming code, given in Appendix B, can be used together with figure 4.13 to understand the implementation of the control logic.

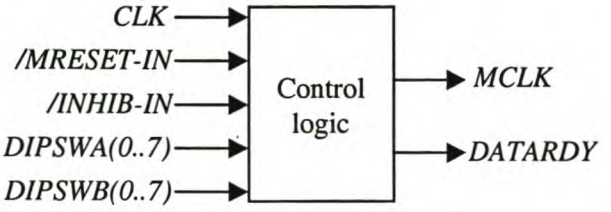


Fig. 4.13: Flex 10K FPGA with control lines.

4.3.5.1 Control logic

The external clock (*CLK*), not to be confused with that of the ADC, is a 40.000 MHz crystal oscillator. This external clock can be divided down by manually adjusting a dipswitch [*DIPSWA(0..7)*]. The operation of the FPGA may be stopped using the inhibit (*/INHIB-IN*) pin. Activating */INHIB-IN* results in the crystal oscillator being ignored, and *CLK* being set to zero, thereby stopping all activity within the FPGA and holding all information on the latches. For prototyping purposes */INHIB-IN* is operated with a jumper. Once integration has been inhibited, the master reset (*/MRESET-IN*) pin allows for the inputs and outputs of the FPGA to be set to zero to start a new integration cycle. This is also done manually using a switch. At the beginning of a new integration cycle */MRESET-IN* must be switched low to ensure validity of the new data. Upon resetting the FPGA *DIPSWA(0..7)* is set to '11111111'. Once valid data is ready to be transmitted over the link *DATARDY* is used to indicate to the link that new data is being received. The generation of *DATARDY* and *MCLK* using *DIPSWA(0..7)* is discussed in section 4.3.5.2. *DIPSWB(0..4)* is used for range selection as discussed in section 4.3.4.

4.3.5.2 Clock generation circuits

The clock-generation circuits are implemented on the FPGA using *Maxplus* software. There are two clock generation circuits, both of which are controlled externally using *DIPSWA(0..7)* to create internal counters. The programmable sampling clock generator essentially divides the 40 MHz external clock, *CLK,* to produce a master clock (*MCLK*). The sampling clock, *ADCLK*, follows *MCLK*. The sampling clock determines the rate at which the ADC samples the data as has been discussed in section 4.3.1.3. The

programmable decimation clock divides *MCLK* to create the decimation clock (WORDOUT-CLK) required by the programmable time-domain decimator and the range selector. The decimation clock determines the rate at which data is transmitted across the link.

Figures 4.14 gives a representation of the generation of the sampling clock as implemented using VHDL in the FPGA. Figure 4.15 shows the associated timing diagram assuming that *DIPSWA(4..7)* is set to "0011". CNTCLK is the internally generated counter within the FPGA that is set using *DIPSWA(4..7)*. The programming code, given in Appendix B, can be used together with figures 4.14 and 4.15 to understand the implementation of the sampling clock generator.

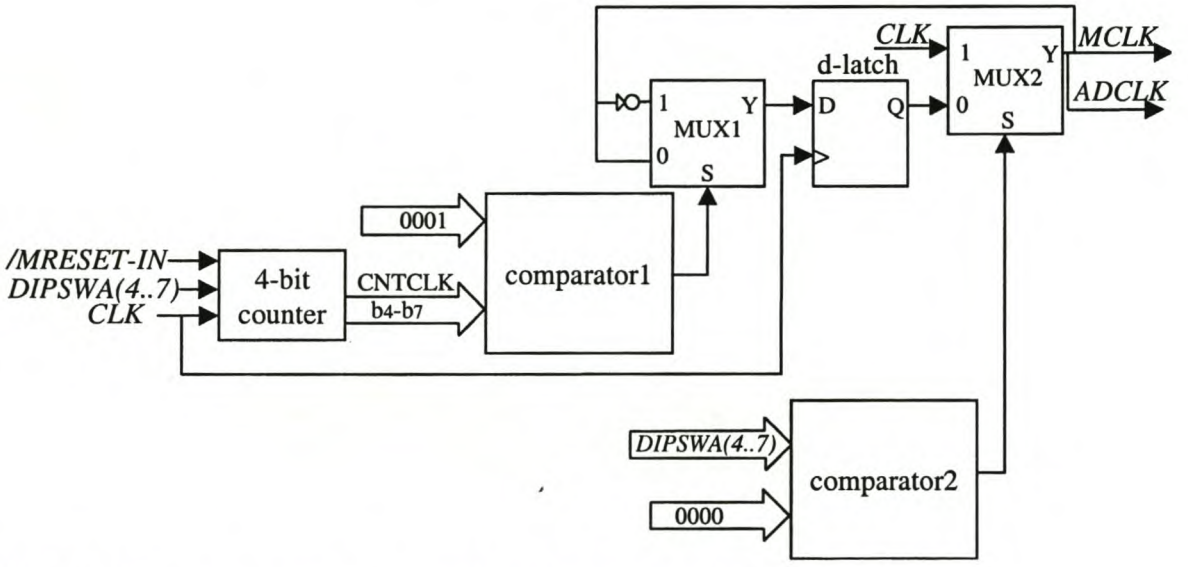


Fig. 4.14: Programmable sampling clock generator.

The counter, comparators and multiplexers are internally generated in the FPGA. They have not been defined as entities in the VHDL code. The counter is edge triggered and counts on the positive edge of *CLK*. When *DIPSWA(4..7)* is set to a value a comparator (comparator1) compares the dipswitch value to '0000'. If *DIPSWA(4..7)* has been set to '0000' (no counter generated), the select input (S) of a mutliplexer2 (MUX2) receives a '1'. This results in *MCLK* = *CLK*. If *DIPSWA(4..7)* is set to any other number,

comparator2 compares the value of CNTCLK to '0001'. In the event of the dipswitch being set to '0001' the select input of MUX1 receives a '1' and */MCLK* is selected, latched and sent to MUX2. . Since the dipswitch was not set to '0000', the select input of MUX2 is '0' resulting in */MCLK* being selected. In the event of the *DIPSWA(4..7)* being set, for example, to '0011' the counter will count from 1 to 3. When the counter is '0001' *MCLK* = */MCLK* as explained above. When the counter is '0010' the comparator compares this value with '0001'. The select input of MUX1 receives a '0' and *MCLK* is selected, latched and sent to MUX2. Since the dipswitch was not set to '0000', the select input of MUX2 is '0' resulting in *MCLK* being selected. The same process occurs when the counter goes to '0011', to be repeated again from '0001'. Upon resetting of the FPGA the CNTCLK is set to '1111'. The generation of *MCLK* is more clearly explained using the timing diagram given in figure 4.15 for *DIPSWA(4..7)* set to '0011'.

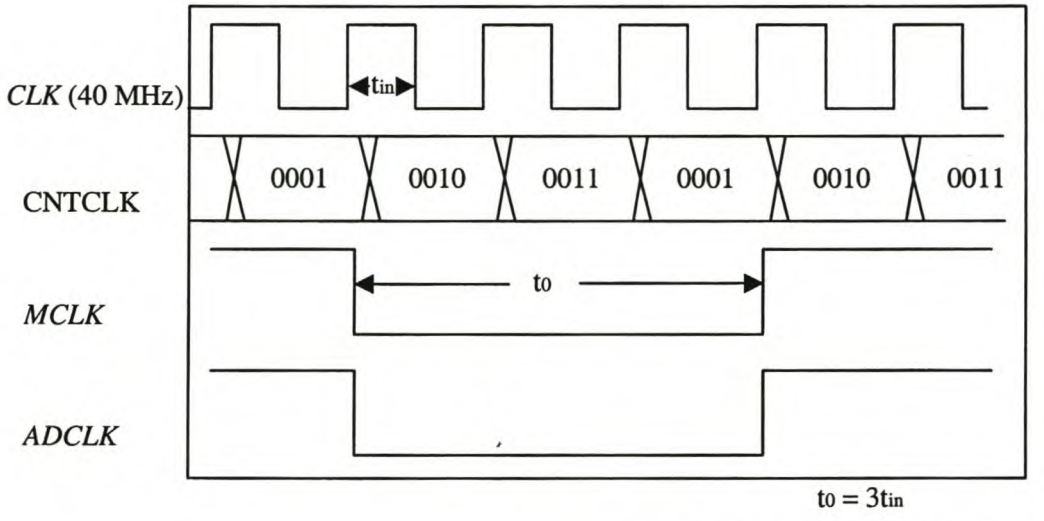


Fig. 4.15: ***Timing diagram of the programmable sampling clock generator (DIPSWA(4..7) set to '0011').***

Once an integration cycle begins, the counter (CNTCLK) begins to count from 1 on the first rising edge of the 40 MHz *CLK*. The counter counts from 1 to 3. On each subsequent rising edge, CNTCLK is incremented by 1 until it counts to its maximum after which it goes back to 1. On each rising edge of *CLK*, the value of CNTCLK is compared

with the value '0001'. If the two are equal then this results in the changing of logic level of *MCLK*. *MCLK* is held in this state until the values equal each other again. *ADCLK* follows *MCLK*. The frequency of *MCLK* is given by

$$f_{MCLK} = \frac{f_{CLK}}{DIPSWA(4..7)} \qquad (4.8)$$

Since *DIPSWA(4..7)* ranges from 1 to 15, f_{MCLK} ranges from 2.66 MHz to 40 MHz. 0 is not included in the counter since division by 0 is indeterminate. If the dipswitch is set to '0000', then the 40 MHz clock is not divided down, and *MCLK* = *CLK* as mentioned before. Since the counter can count from 1 to 15, a maximum of 15 clock cycles must pass if *DIPSWA(4..7)* is changed from the highest setting to the lowest to ensure valid data and so forth for any other decreases to the counter. Increasing the counter value should not require for a data latency period.

The remaining 4 switches on *DIPSWA(0..7)*, i.e. 0 to 3, are used to generate the decimation clock. The master clock, *MCLK*, is divided to yield the decimation clock, i.e. WORDOUT_CLK. Figures 4.16 gives a representation of the generation of the decimation clock as implemented using VHDL in the FPGA. Figure 4.17 gives the associated timing diagram assuming that *DIPSWA(4..7)* is set to "0011". The programming code, given in Appendix B, can be used together with figures 4.16 and 4.17 to understand the implementation of the decimation clock generator. The counter (CNT1) has not been defined as an entity in the VHDL code. CNT1 is the internally generated counter within the FPGA that is set using *DIPSWA(0..3)*. The counter is edge triggered and begins counts on the positive edge of *MCLK*.

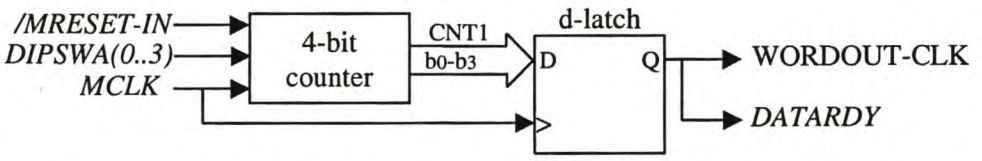


Fig. 4.16: Programmable decimation clock generator.

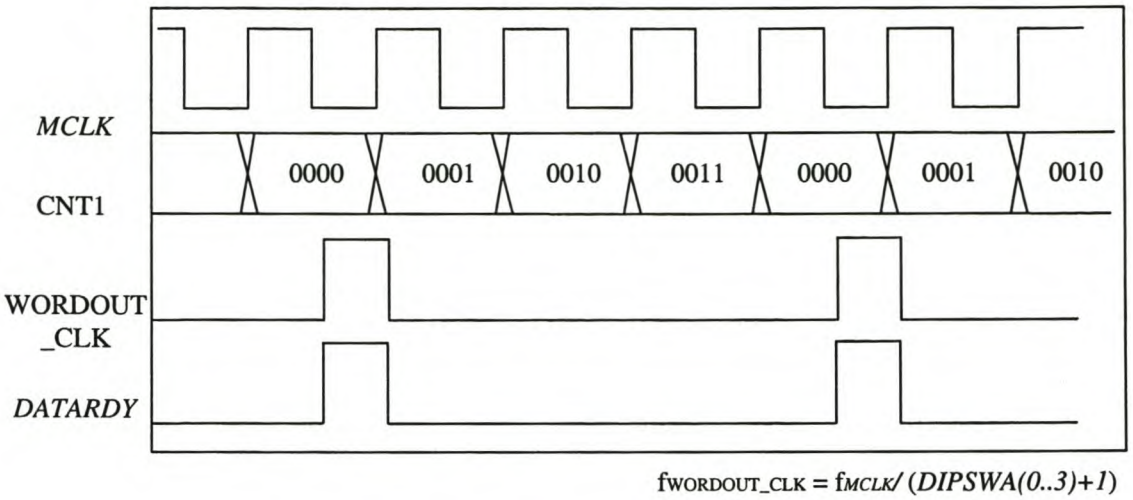


Fig. 4.17: ***Timing diagram of the programmable decimation clock generator (DIPSWA(0..3) set to '0011').***

Once a cycle begins, the counter (CNT1) begins to count from 0 on the first rising edge of the *MCLK*. The counter counts from 0 to a possible maximum of 15. On each subsequent rising edge, CNT1 is incremented by 1 until it counts to its maximum after which it goes back to 0. The maximum value of the counter is controlled by *DIPSWA(0..3)*. Since the counter can count from 0 to 15, a maximum of 16 clock cycles must pass if *DIPSWA(4..7)* is changed from the highest setting to the lowest to ensure valid data and so forth for any other decreases to the counter. Increasing the counter value should not require for a data latency period. Upon resetting of the FPGA, *DIPSWA(4..7)* is set to its maximum, i.e. '1111'.

When the dipswitch is, for example, set to "0011" then the counter will count from 0 to 3. When the falling edge of *MCLK* coincides with the value of "0000" on CNT1, the logic level of WORDOUT-CLK changes. WORDOUT-CLK is held in this state until the CNT1 changes to "0001" again. *DATARDY* follows WORDOUT-CLK. The frequency of WORDOUT-CLK is given by:

$$f_{WORDOUT-CLK} = \frac{f_{MCLK}}{DIPSWA(0..3)+1} \qquad (4.9)$$

Since *DIPSWA(4..7)* ranges from 0 to 15, $f_{WORDOUT-CLK}$ ranges from 166 kHz (i.e. one-

sixteenth 2.66 MHz) to 40 MHz.

4.4 Test procedures

The digital signal conditioning subsystem together with the high speed serial-fibre optic-link of Chapter 5 were tested independently of the analog signal conditioning subsystem. A test word, '100000000001', was programmed as an input to the FPGA to generate an output representing a counter that increases linearly with the clock. The output pins of the FPGA were monitored to verify that a counter was generated and the output of the DAC of Chapter 5 was monitored to see whether a ramp was obtained. In addition the dipswitches were set to different values and it was confirmed that the sampling clock generator, decimation clock generator and range selection were implemented correctly.

4.5 Conclusion

The digital signal conditioning has been successfully designed to digitise the analog signal, integrate and decimate (if necessary) the digitised data and to perform range selection. For prototyping purposes unrouted pins are routed to headers and two additional configurations for programming the FPGA were allowed for. Since the digital design has been optimised there is no further need for these components, but future modifications of the design may require a bigger, faster FPGA. A test program can be added such that *DIPSWB(5..7)* can be used to interchange between normal operation and test mode.

5 HIGH SPEED SERIAL FIBRE-OPTIC LINK

5.1 Introduction

This chapter discusses the transmission of the digitised data across the high speed serial fibre-optic link. An overview of the system is presented in block diagram form, followed by a detailed, functional description of each block.

5.2 Block diagram representation

The purpose of this subsystem is to encode the data from the digital signal conditioning subsystem, transmit it across the fibre-optic link and to decode the data on the receiving end. This data must then be converted back into analog form by the DAC. Figure 5.1 shows a block diagram representation of this subsystem.

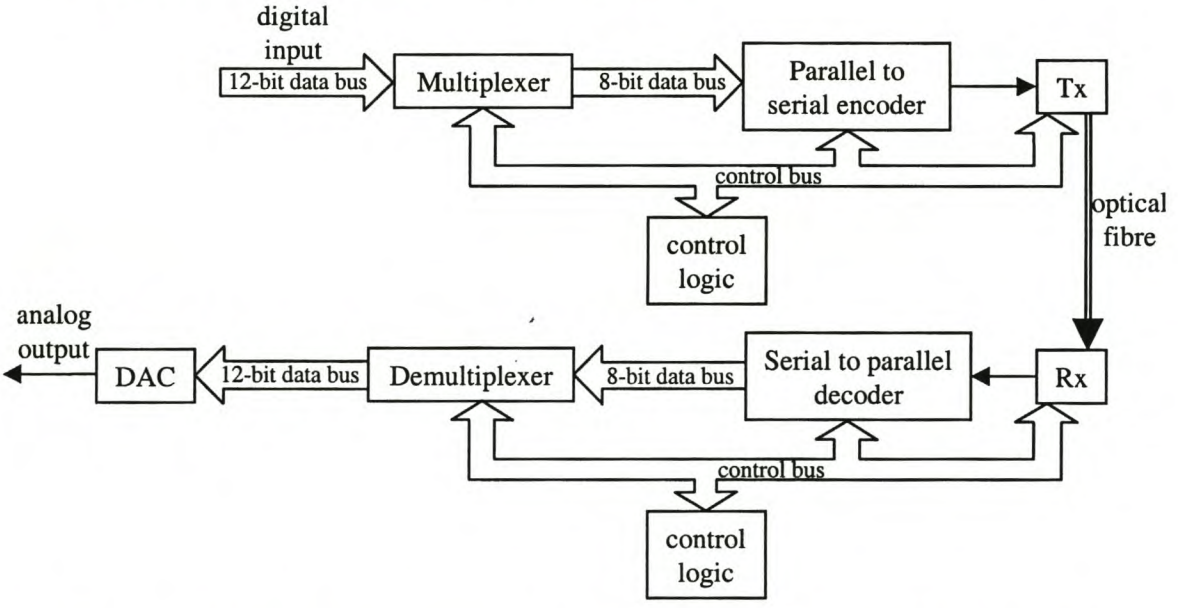


Fig. 5.1: Block diagram representation of the high speed serial fibre-optic link.

The digital signal conditioning subsystem is interfaced to the optic link via a parallel to serial encoder. The digital input is multiplexed into eight bit strings to the parallel to

serial encoder. Eight bits of data or protocol information (TTL logic) are loaded into the parallel to serial encoder at a pre-determined byte rate. The byte is encoded and shifted out as a PECL 10-bit stream to the fibre optic link at a bit rate that is ten times the byte rate of incoming parallel data. The conversion of the 8-bit parallel data into one, 10-bit serial stream is referred to as 8B/10B coding. The internally generated clock that controls this will be discussed further in section 5.3.1.2. The transmitting and receiving modules (Tx and Rx) are the fibre-optic control links. An Erasable Programmable Logic Device (EPLD) is used to generate the control logic for the multiplexer, parallel to serial encoder and the transmitter. On the receiving end of the fibre-optic link, a serial to parallel decoder reconstructs the data byte and presents it in parallel with a byte rate clock. The data is demultiplexed into 12-bit strings and transferred to the DAC. An EPLD here too implements the control logic to the demultiplexer, serial to parallel decoder and receiver. The data is converted back into its analog form by the DAC. Since the chosen DAC runs off ±15 V rails and the other components of the link require ±5 V rails, a voltage regulator has been incorporated.

The EPLDs were programmed using *Maxplus* software. The VHDL programs for the EPLDs are given in Appendix B and their pin assignments are given in Appendix B, figures B.2 and B.3. The complete circuit design and the p.c. board layout of the high speed serial fibre-optic link is given in Appendix C, figures C.1, C.4, C.5, C.6, C.7, C.8, C.9 and C.10.

5.3 Functional description of the subsystem components

5.3.1 Parallel to serial encoder

The digital signal conditioning subsystem delivers 12-bits of parallel data at CMOS levels. This data needs to be transmitted across a 266 MBd fibre-optic link to the DAC. The fibre-optic link accepts serial Positive Emitter-Coupled Logic (PECL) data. The optical transmitter is interfaced to the digital signal conditioning subsystem via a parallel to serial encoder. This encoder essentially serialises the digitised data and delivers it as PECL data

to the transmitter. The CY7B923 HOTLink™ transmitter manufactured by *Cypress* is used as the parallel to serial encoder. This is discussed in section 5.3.2. Figure 5.2 illustrates the logic block diagram of the CY7B923 transmitter [42].

Eight bits of data or protocol information are loaded into the transmitter at a byte rate determined by the clock (*CKW*) input and are encoded. Serial data is shifted out of the three differential PECL ports at a bit rate that is ten times the byte rate of incoming data. There are built-in test functions that enable the link to be tested in isolation of the rest of the system.

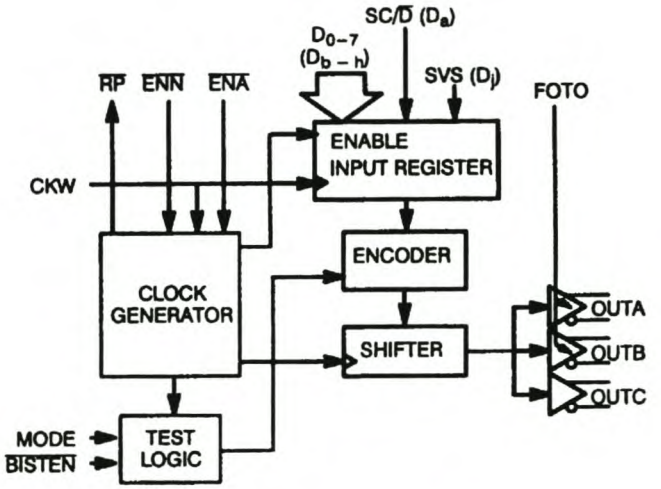


Fig. 5.2: CY7B923 transmitter logic block diagram [42]

5.3.1.1 Input register

The input register acts as a latch and holds the data that is to be encoded by the transmitter. On the rising edge of *CKW*, the input register is loaded with information on the data lines D_{0-7}, the special character/data (*SC//D*) line and the send violation symbol (*SVS*) line. The control logic supplies the *SC//D* and *SVS* inputs to the CY7B923. The user is allowed to choose when data is loaded into the register by utilising two enable inputs, viz. enable parallel data (*/ENA*) and enable next parallel data (*/ENN*). This will be discussed further in section 5.3.1.2. A high on *SC//D* results in the transmitter encoding the data as a control byte. A low on *SC//D* causes data to be encoded as a data byte. A

high on *SVS* results in a violation symbol being encoded and sent whilst the data on the data lines are ignored. This allows for the checking of transmission errors in the link. In the developed system the *SVS* input pin is not used and set low.

Since the digital conditioning subsystem delivers 12-bit input to the transmitter that is capable of handling only 8 bits at a time, the parallel data needs to be multiplexed first. The control logic EPLD handles this. The 8 MSBs first transmitted across the link and the 4 least significant bits (LSBs) are transmitted next along with four zeroes to fill up the byte space. The control logic that does this is discussed further in section 5.3.2.

5.3.1.2 Clock generator

The clock generator is an embedded PLL that creates the bit rate clock for the serial shifter. It takes the byte-rate reference clock (*CKW*) and by multiplying it by 10, it generates a bit rate clock for driving the serial shifter. *CKW* is the same clock that controls the flow of data into the input register. A 25.175 MHz crystal oscillator, viz *CLK* (not to be confused with those of the ADC and FPGA as discussed in Chapter 4), is used to generate *CKW* thereby allowing optical transmission of the data at a rate of 251.75 MBd. The clock generator controls the transfer of data between the input register and shifter.

/ENA and */ENN* control the loading of data into the input register. Asserting */ENA* (active low) causes the inputs to be loaded into the register on the positive edge of *CKW*. Asserting */ENN* on the rising edge of *CKW* will result in the data present on the inputs on the next rising edge of *CKW* to be loaded into the input register. If neither of the two enable inputs are selected, a special character comma K28.5 (*sync-bit*) is sent. In the developed system */ENA* is used to control the transfer of data or information into the input register. Since the read pulse (*/RP*) output is required only when $D_{0\text{-}7}$ is generated from an asynchronous FIFO, it is not used in this system. The control logic that supplies */ENN*, and */ENA* to the CY7B923 is discussed in section 5.3.2.

As mentioned before a 25.175 MHz crystal oscillator provides *CKW*. Although the maximum speed that the oscillator could be set at is 26.6 MHz (since Tx and Rx offer data transmission at a maximum rate of 266 MBd), a smaller one was chosen to ensure that the system operates within the allowed range. The link then operates at 251,75 MBd and this means that 251.75 Mbits/second can be transmitted across the link. The serial data from the encoder is sent across the link at 10 times the rate at which the encoder receives the parallel data. The data therefore can be delivered from the digital signal conditioning subsystem to the encoder at 25.175 Mbytes/second. Two 10 bit serial streams are required to transmit one sampled word across the link. The maximum sample speed that the encoder can handle is then halved, i.e. 12.588 MHz. However, in the developed system a *sync-bit* is sent between every two 10-bit serial streams, i.e. between every 12-bit parallel data bus, to maintain link synchronisation. Thus, another 10 bit serial stream is required to send one sampled word across the link thereby further reducing the sampling speed that the encoder can handle to 8.391 MHz. Subsequent tests showed that a *sync-bit* need not be sent through between every bit and that it was sufficient to send one across every 10 000 sampled words. This can be implemented in future development of the system. If this is the case then the maximum sampling speed is very close to 12.588 MHz.

5.3.1.3 Encoder

The encoder transforms the data held in the input register into a more suitable form for transmission across the fibre-optic link. Special tables are used for the encoding of data. The state of *SC//D* determines the type of encoding of D_{0-7} as discussed in section 5.3.1.1. A low on *SC//D* results in the data being encoded as a 10-bit serial stream using the Data Code Table [42]. A high on *SC//D* implies that the data represent a control code and are encoded using the Special Character Code Table [42]. In the developed system only the *sync-bit*, as mentioned in section 5.3.1.2, is used to maintain link synchronisation. If the inputs are disabled for the duration of a byte time, then the encoder will send the *sync-bit* that will maintain link synchronisation.

It is possible to bypass the 8B/10B coding function of the encoder if the system has an

external coder. This bypass is controlled by the *mode* input of the transmitter. Data is encoded only if *mode* is set low. When kept high, the data from the input register goes directly to the shifter. In the developed system *mode* is tied to ground thus forcing 8B/10B encoding.

5.3.1.4 Shifter

The shifter accepts the parallel data from the encoder and shifts it to the serial interface output buffers using a Phase Locked Loop (PLL) multiplied bit clock that operates at ten times the byte rate clock. A counter within the clock generator controls the timing and synchronisation of the transfer. It is independent of the signal levels and timing at the input pins.

5.3.1.5 Serial outputs

The serial interface PECL output buffers viz. *OutA±*, *OutB±*, *OutC±* drive the fibre-optic transmitter. They are all connected to the shifter and carry identical information. *OutA±* and *OutB±* are controlled by the fibre-optic transmitter off (*FOTO*) input. If *FOTO* is held low, then the data encoded by the transmitter will appear at the outputs continuously. A high on *FOTO* forces the 2 outputs to 'logic zero' states, causing the fibre-optic transmit module to extinguish its light output. *OutC±* is not controlled by *FOTO* thereby supplying a continuous data stream. In this application *OutC±* is the only serial output used and *OutA±* and *OutB±* are tied to V_{CC} to disable them and to reduce the power consumption.

5.3.2 Control logic

The operation of the CY7B923 HOTLink™ is controlled by an EPLD from *Altera's* 7000 family. The chosen EPLD has 44 pins and a speed of rating of -10. Currently with the existing program, less than 20% of pins are available for future use and the chip runs at 55.5 MHz. The unused input pins have been reserved and routed onto the board for future

use. The HOTLink™ transmitter and receiver may be tested independently to ensure that the link works. There are therefore two operational modes of the EPLD, viz. normal mode and test mode. The fully commented VHDL program for the control logic of the CY7B923 transmitter is given in Appendix B, and the pin assignments of the EPLD is given in figure B.2. Figure 5.3 shows the timing diagram for the control logic incorporated in the EPLD in its normal mode assuming that the digital signal conditioning subsystem is delivering data to the transmitter, using the *DATARDY* output, at a rate of 8 MHz. The VHDL program can be used with figure 5.3 to get a full understanding of the implementation of the transmitter's control logic. All inputs to the CY7B923 are generated by the EPLD.

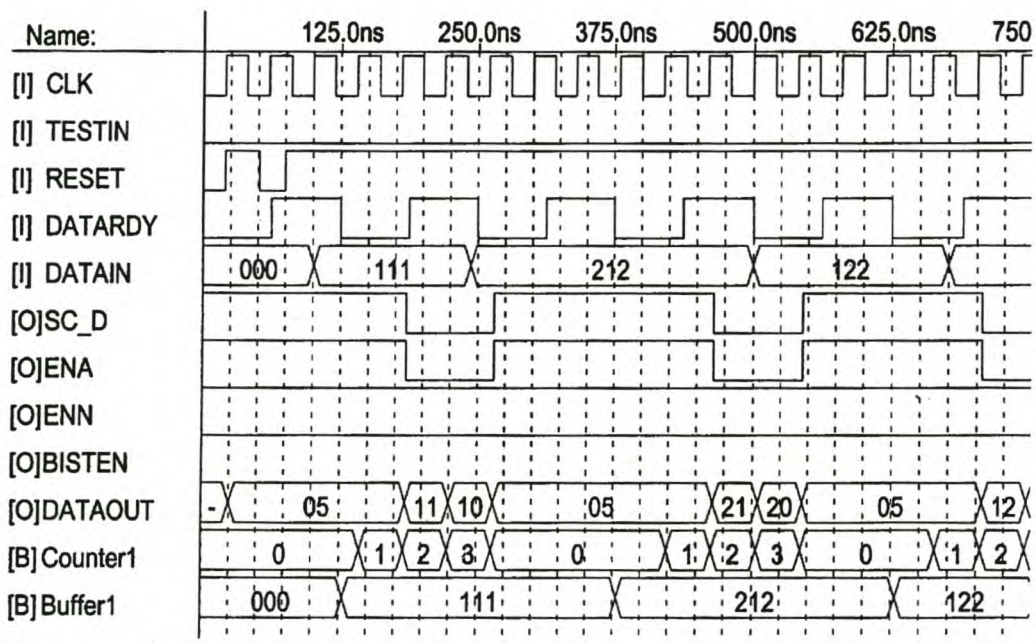


Fig. 5.3: ***Timing diagram of the control logic during normal operational mode of the CY7B923 transmitter.***

As discussed in section 5.3.1.1, the inputs */ENA*, *SC//D* and *CKW* of the HOTLink™ are used for data or information transmission across the link. *CKW* is obtained from an external 25.175 MHz crystal oscillator, *CLK*, which is used for the control logic module. This ensures synchronisation between the EPLD and the CY7B923. A low of */ENA* and *SC//D* on the rising edge of *CLK* results in the data on $D_{0\text{-}7}$ to be transmitted across the

link as a 10-bit serial stream. Since 12 bits of data are delivered to the encoder, the data needs to be multiplexed first. The eight most significant bits are sent across first. The four least significant bits are then sent across with four zeroes. Two 10-bit serial streams are therefore needed to transmit one 12-bit word. In between each of the 2 streams, a *sync-bit* is sent across as well.

Upon reset in normal operating mode, an internally generated counter, Counter1, is set to '0000'. When the first falling edge on *DATARDY* is detected, the data at the inputs $D_{0\text{-}11}$ are latched into a buffer, Buffer1, and Counter1 begins to count up in steps of 1 to 3. When the counter is at '0001', on the first detected rising edge of *CLK*, */ENA* and *SC//D* go low and the 8 most significant bits of the word latched in buffer1 are delivered to the 8 output pins of the EPLD, which are $D_{0\text{-}7}$ of the CY7B923. */ENA* and *SC//D* remain low until the counter goes to '0011'. When the counter is at '0010', on the first detected rising edge of *CLK*, the 4 least significant bits with zeroes are delivered to the 8 output pins of the EPLD. When the counter is at '3', on the first detected rising edge of *CLK*, */ENA* and *SC//D* are high and a *sync-bit* appears at the 8 output pins of the EPLD.

Since figure 5.3 shows the timing diagram of the EPLD during normal mode, *TESTIN* is low thereby deactivating */BISTEN*. As discussed before */ENN* is not used for data transmission and is set high. During test mode, the link can be tested independently of the other subsystems. There are various ways in which the built-in self-test may be implemented as referenced in the CY7923/CY7B933 datasheets [42]. In the developed system, a high on *TESTIN* causes */BISTEN* to go low and *ENA* to go high. Once */BISTEN* is low, the link is off-line and enters test mode. An alternating 1-0 pattern is sent that allows the transmitter and receiver to work together thus testing the function of the entire link. */BISTEN* has the same timing as $D_{0\text{-}7}$ of thc CY7B923.

5.3.3 Fibre-optic transmitter and receiver data links

The HFBR-1119T/-2119T series of data links, manufactured by *Hewlett Packard*, are high performance, cost-efficient 266 MBd devices used for the transmission of the serialised

data across the fibre-optic cable. Figure 5.5 shows a schematic representation of the implementation of the data links in the developed system with power supply filtering.

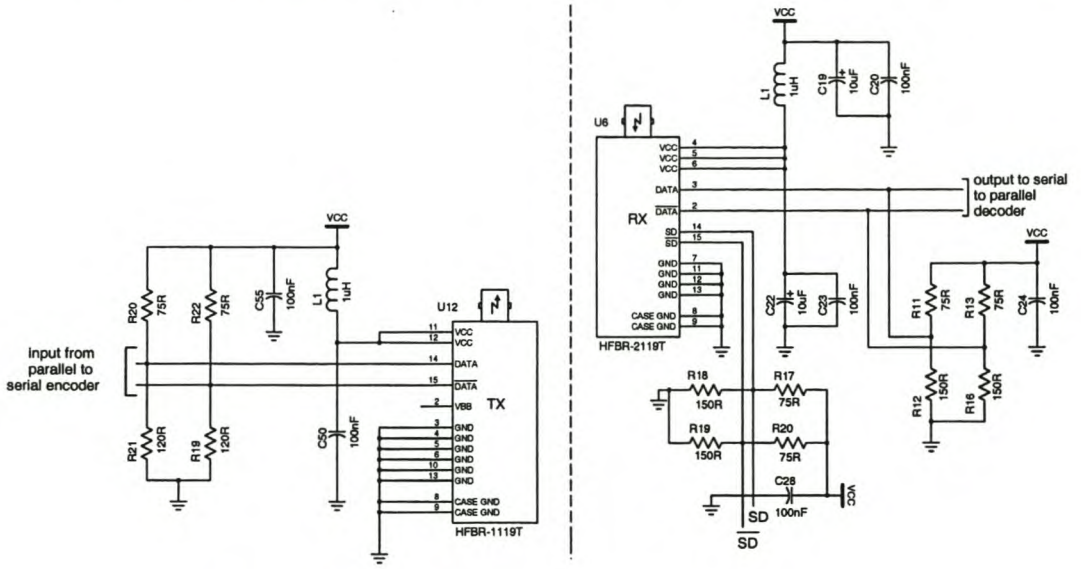


Fig. 5.4: ***Schematic representation of HFBR-1119T transmitter (a) and HFBR-2119T receiver (b) with power supply filtering [43].***

Once the digital data is encoded it is shifted out through the *OutC±* line of CY7B923 to *DATA* and */DATA* inputs of the HFBR-1119T. This chip accepts the differential input and transforms it into an optical signal that is transmitted across the fibre-optic cable.

On the receiving side the HFBR-2119T accepts the optical signal that has been transmitted across the fibre-optic cable and converts it back to the original PECL serialised form as required by the serial to parallel decoder. It delivers the output on its *DATA/DATA* lines to the serial to parallel decoder.

Figures C.1, C.5, C.6, C.7 and C.10 in Appendix C give schematic circuit diagram and p.c. board layouts of the fibre-optic transmitter and receiver data links as incorporated in the developed system. The tracks connecting the CY7B923's differential outputs to the transmitter must be short and of equal length to prevent signal skew. The optimal power supply filter as shown in figure 5.4 has been suggested in the HFBR-1119T/-2119T

datasheets [43]. These modules are designed for 50 or 62.5 μm core mutimode fibre-optic cable up to a distance of 1.5 km.

5.3.4 Serial to parallel decoder

The serial to parallel decoder accepts the serial data from the HFBR-2119T at its differential input lines and converts it into 8-bit parallel bytes. The matching CY7B933 HOTLink™ receiver manufactured by *Cypress*, illustrated in figure 5.5, is used as the serial to parallel decoder [42].

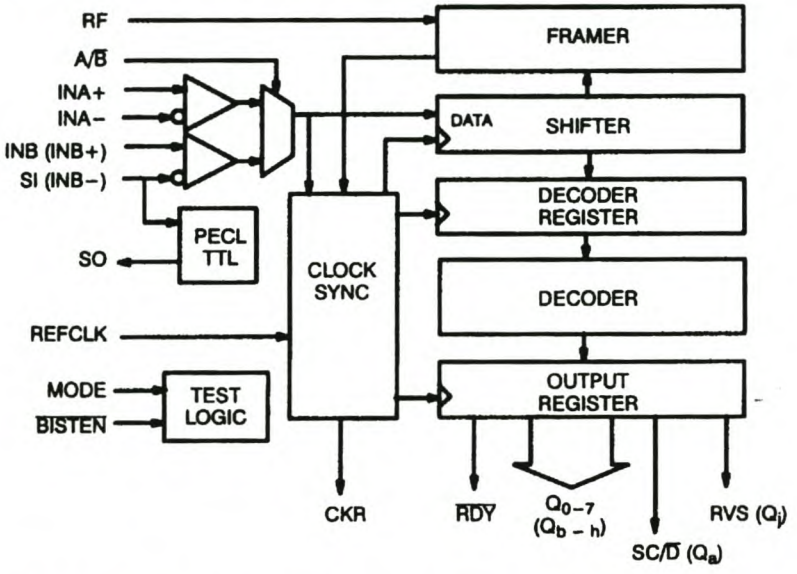


Fig. 5.5: CY7B933 receiver logic block diagram [42].

An EPLD offers the control logic to the CY7B933 chip. The receiver recovers the timing information required to reconstruct the data. It deserialises, decodes and checks the bit streams for errors. One of the two sets of differential inputs, viz. *INA±* and *INB±*,can be used to receive the serial data from the HFBR-2119T receiver. A reference clock, *REFCLK*, is used to indicate the rate at which data is received by the decoder. The serial data is reconstructed and delivered to the output pins $Q_{0\text{-}7}$.

5.3.4.1 Serial data inputs

There are two pairs of differential line receivers viz. serial data input A (*INA±*) and serial data input *B* (*INB±*). By using the serial data input select (*A/B*) pin the required input can be chosen. When *A/B* is high, *INA±* is selected and a low on *A/B* results in *INB±* being chosen. In the developed system, *INB±* has been chosen. *INA±* has been deactivated. The differential inputs are connected directly to the fibre-optic interface since the CY7B933 and HFBR-2119T both operate at PECL levels.

5.3.4.2 PECL-TTL translator

The status out (*SO*) pin defines the function of the *INB±* pins. Depending on the state of *SO*, *INB+* can be used as a single-ended PECL data receiver (*INB*) or half of the *INB* of the differential pair *INB±*. Also, depending on the state of *SO*, *INB-* can be used as a single-ended PECL status monitor input (*SI*) or half of the *INB* of the differential pair *INB±*. If a PECL/TTL translator is needed *SO* is normally connected and loaded. Then *INB+* will be referred to as *INB* and the *INB-* will be referred to as *SI*. Utilising this positive-referenced PECL/TTL translator eliminates the need for external logic between the PECL fibre-optic interface output and the TTL input in the control logic. In this system the status monitor translator is not required (since the CY7B933 and HFBR-2119T both operate at PECL levels) and *SO* is tied to V_{CC}. This is detected by a sensor and causes the *INB±* to be used as a differential line receiver.

5.3.4.3 Clock synchronisation

For correct decoding of data, the incoming bits need to be distinguished from each other and byte boundaries identified. The framer and clock synchronisation does this. Clock synchronisation is provided by an embedded PLL. The clock (*CKR*) output pin is phase and frequency aligned to the incoming serial data stream. It controls the transfer of data from the shifter to the decode register. This transfer is initiated by the framer logic. The buffered clock read (*CKR*) output stems from the bit counter that controls the decode

register and the output register transfers.

CKR logic is such that the when reframing of the data causes the counter sequence to be interrupted, the period and pulse width of *CKR* is never less than normal. The reference clock (*REFCLK*) is the clock frequency reference for the clock/data synchronising PLL. The 25.175 MHz crystal oscillator that is used to generate *REFCLK* must run within ±0.1% of the frequency of the clock, *CKW*, on the transmitter side.

5.3.4.4 Shifter

The shifter accepts the inputs from the serial data inputs and transfers it to the framer and decode register. The clock synchronisation logic controls the transfer of data. Each bit of data received by the shifter is transferred to the framer. Once a byte has been accepted by the shifter, a byte data is transferred to the decode register.

5.3.4.5 Framer

The framer is responsible for checking the incoming bit stream for the pattern that defines the byte boundaries. It has a combinatorial logic filter that awaits the *sync-bit*. Once it is found it frames the data correctly on the correct byte boundaries. This mechanism is implemented by a free-running bit counter which is reset to its initial state each time a *sync-bit* is found.

It is possible for random errors to occur in the serial data that will contaminate the data patterns. The reframe enable (*RF*) pin controls this. When *RF* is held low, the reframing logic is disabled. The incoming data stream is then deserialised and decoded using byte boundaries set by the internal byte counter. When *RF* is held high, each *sync-bit* detected in the shifter will frame the data that follows. If *RF* is held high for 2048 consecutive bytes, the internal framer switches to double-byte mode. This reduces the possibility of erroneously reframing to an aliased *sync-bit*. For this application *RF* is held high.

5.3.4.6 Decode register

The decode register accepts serial data from the shifter and is controlled by the clock synchronisation block. The data is delivered to the decoder and held until it is transferred to the output latch.

5.3.4.7 Decoder

The decoder transforms the 8B/10B coded data back into its original 'raw' form. A low on the *SC//D* output indicates a data character whilst a high on SC//D indicates a special character. *SC//D* has the same timing as Q_{0-7}. Disparity errors and unused patterns are signified as errors by a high on the received violation symbol (*RVS*) output pin. If a *RVS* is received, the control logic causes a light emitting diode to go on. *RVS* has the same timing as Q_{0-7}. As discussed in section 5.3.1.2, the *MODE* pin is tied to ground since 8B/10B decoding is required.

5.3.4.8 Output register

The output register holds the decoded data (Q_{0-7}) and information on the *SC//D* and *RVS* lines. It aligns this recovered data with the recovered byte rate clock (*CKR*). This synchronisation is necessary to ensure glitch free output behaviour. The output changes synchronously with a positive edge on *CKR*. A low on the data output ready (*RDY*) pin implies that new data has been received and ready to be transferred. A missing pulse on *RDY* indicates that a null character has been received.

5.3.5 Control logic

The operation of the CY7B933 HOTLink™ is controlled by an EPLD from *Altera's* 7000 family. The chosen EPLD has 44 pins and a speed rating of -10. Currently, with the existing program, less than 20% of logic the cells are available and the chip runs at approximately 100 MHz. The unused input pins have been reserved and routed onto the

board for future use. As mentioned before, the HOTLink™ transmitter and receiver may be tested independently to ensure that the link works. There are therefore two operational modes of the receiving device, viz. normal mode and test mode. The VHDL program of the control logic of the CY7B933 transmitter is given in Appendix B, and the pin assignments of the EPLD is given in figure B.3. Figure 5.6 shows the timing diagram for the control logic of the EPLD in its normal mode. The VHDL program can be used with figure 5.5 to get a full understanding of the implementation of the receiver's control logic.

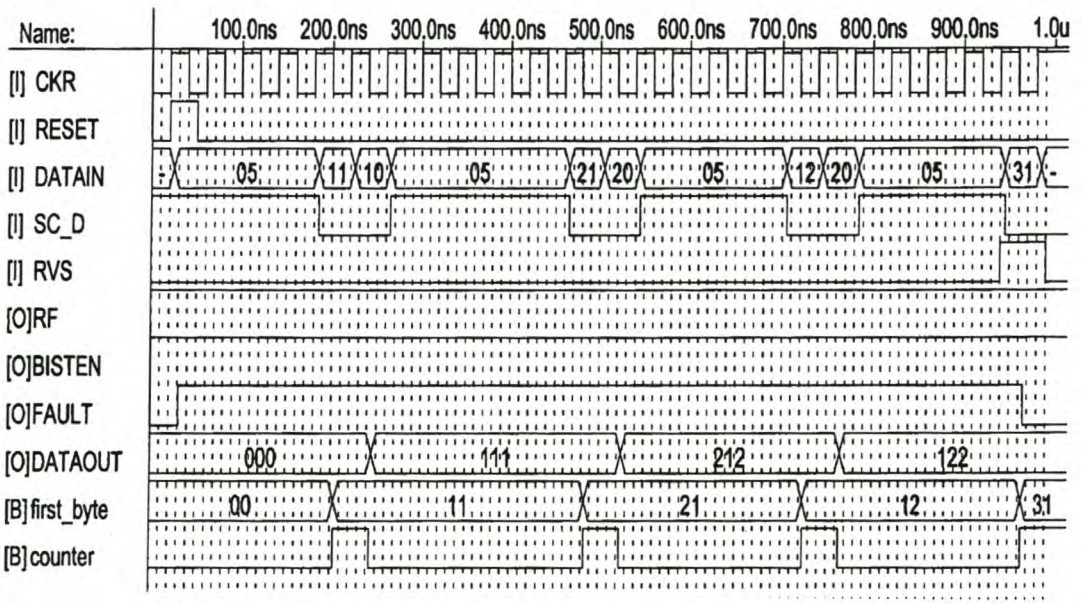


Fig. 5.6: ***Timing diagram of the control logic during normal operational mode of the CY7B933 receiver.***

As discussed in section 5.3.4.3, *CKR* is phase and frequency aligned to the incoming serial data stream. The decoder discussed in section 5.3.4.7 delivers 8 bits of parallel data with the *RVS* and *SC//D* lines to the control EPLD. It has been explained in section 5.3.2 that three serial streams are required to transmit each 12-bit parallel data bus (two for the word itself and one for the *sync-bit*). The control logic uses the inputs it receives to deliver 12 bits of parallel data to the DAC. Using the *SC//D* input it must use two 8-bit words from the decoder to construct the original 12-bit word that was transmitted across the link. The control logic must also be able to detect a *RVS*.

Upon reset in normal operating mode, an internally generated counter is set to '0'. A low on *SC//D* results the first 8-bits of data at the input pins of the EPLD, (Q_{0-7}), to be latched into a buffer, first_byte, upon the detection of the first falling edge of *CKR*. Then the counter is then set to '1'. On the next falling edge of *CKR*, the data in first_byte and the 4 most significant bits at the inputs of the EPLD (Q_{0-7}), are transferred to the 12 output pins of the EPLD. The counter is set to '0' again.

There is a */FAULT* line which is connected to a Light Emitting Diode (LED). If a violation symbol, *RVS*, is received whilst *SC//D* is low *FAULT* goes low upon detection of a falling edge on *CKR*. This results in the LED lighting up alerting the user of a violation during the transmission of data.

Since figure 5.6 shows the timing diagram of the EPLD during normal mode, */BISTEN* is inactivated. As discussed in section 5.3.4.5, *RF* is kept high to enable the framer. During test mode, the link can be tested independently of the other subsystems. A low on */BISTEN* will put the receiver into test mode and the alternating 1-0 test pattern that was sent by the transmitter in section 5.3.2 will be received. This allows the transmitter and receiver to work together thus testing the function of the entire link. */BISTEN* has the same timing as Q_{0-7} of thc CY7B933. Unlike in the CY7B923 where the transmitter can be put into test mode by a manual connection, the EPLD of the CY7B933 needs to be re-programmed to put the receiver into test mode.

5.3.6 Digital to analog converter

The AD668 manufactured by *Analog Devices* was chosen for the DAC [44]. The AD668 is an ultra high speed, 12 bit DAC providing outstanding speed and accuracy. Figure 5.7 shows a functional block diagram representation of the AD668[44].

The wideband reference input is buffered by an internal, high gain, closed loop reference amplifier as shown in as shown in figure 5.7. The reference input is a 1 V high impedance input, but trimmed resistive dividers accommodate 5V and 1.25V references. The

reference amplifier has a small signal bandwidth of 15 MHz [44].

Matched current sources and thin film ladder techniques are combined to produce bit weighting. The output range can be taken as a 10.24 mA current output or a 1.024V voltage output [44]. Bipolar outputs can be obtained, without additional external circuitry, by pin-strapping. Laser-wafer trimming ensures full 12-bit linearity and excellent accuracy [44]. The digital inputs are compatible with both TTL and CMOS logic families thus making it easily interfacable to the *Cypress* receiver.

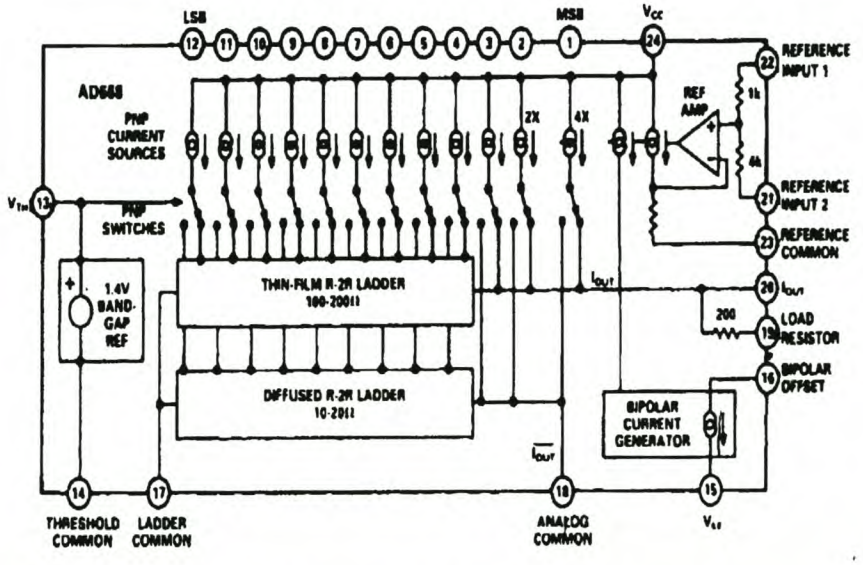


Fig. 5.7: ***Functional block diagram of the AD668 [44].***

The DAC can be used in a variety of different configurations depending on the required application. It can, be for example, be configured to deliver outputs that are either voltage or current, buffered or unbuffered, unipolar or bipolar. Figure 5.8 shows the AD668 with its pin assignments as configured in the developed system. The DAC runs of ±15 V rails and requires a +5V reference input.

The digital inputs received from the demultiplexer of as shown in figure 5.1 are DB(0..11). The digital inputs should be free of large glitches and isolated from analog outputs. The DAC uses both SOB and BTC coding. For unipolar outputs it uses SOB coding and for

bipolar outputs it uses BTC coding. Since the integrator, as discussed, in section 4.3.2 converted the digitised data into BTC format the DAC must be configured to produce a bipolar output. This is achieved by connecting the bipolar offset pin, IBPO, to the DAC output ie I_{OUT}. This produces a bipolar analog output from the digital inputs by offsetting the normal output current with a precision current source [44].

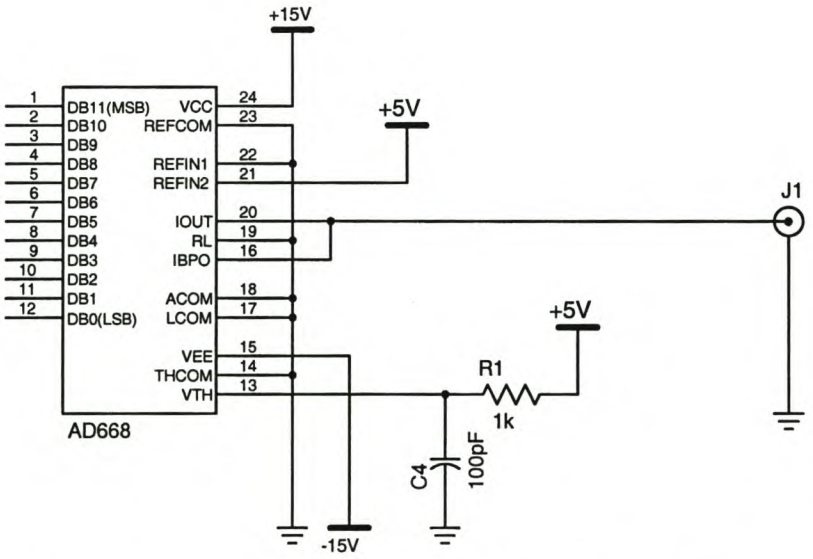


Fig. 5.8: ***Schematic representation of the AD668 as configured in the developed system.***

For the current output mode the DAC output, I_{OUT}, is connected to a virtual ground whilst for the voltage output mode, as required for this application, I_{OUT} is connected to a resistive load, R_{LOAD}, which consists of the parallel combination of R_L and the internal DAC output. In voltage output mode the DAC output voltage, V_{OUT}, is given by the relationship

$$V_{OUT} = I_{OUT} * R_{LOAD} \text{ [44]}, \qquad (5.1)$$

where I_{OUT} denotes the output current and R_{LOAD} denotes the load resistance connected to the DAC output mode.

For a voltage output R_L must be tied to ground producing a 100Ω DAC output resistance. Then the DAC output current generates a 1.024 V output when the DAC current is at its

full scale of 10,24 mA.

The threshold of the digital inputs is set at 1.4V and does not vary with supply voltage [44]. A band-gap generator provides the reference. The band-gap generator as shown in figure 5.7 requires 3 mA of bias current which is achieved by tying an external resistance, R_1, from the threshold control, V_{TH}, to the $+V_{CC}$ supply. R_1 is given by

$$R_1 = \frac{(+V_{CC} - 1.4)V}{3mA} = 1.2k\Omega \approx 1k\Omega. \qquad (5.2)$$

Threshold common, THCOM, is the ground point for the band-gap diode shown in figure 5.7. Tying THCOM sets the threshold voltage to 1.4 V. The reference common, REFCOM, provides the reference ground for the reference amplifier's current feedback loop. The output voltage may, if desired, be adjusted using the reference input pins named REFIN1 and REFIN2. REFIN1 has a 1 kΩ series resistance to the reference amplifier input and a 5 kΩ series resistance to REFIN2. REFIN1 may be used together with REFIN2 to provide a 5:1 voltage divider [44]. The input divider has been connected to produce a 5 V full-scale reference by shorting REFIN1 to ground and using REFIN2 as a reference input tied to +5 V.

5.4 Test procedures

When the test word, '1000000000001', discussed in section 4.4, was integrated and sent across the link, it was received by the DAC and correctly converted into its analog form. Since the digital integrator in Chapter 4 generated an output representing a linearly increasing counter, a ramp appeared at the output of the DAC. There were approximately 4000 points on each ramp whereafter it began to count again once it wrapped over. This meant that the DAC converted all 12-bits of the input data. However, there were many glitches in the output.

5.5 Conclusion

High speed data links can be difficult to design and to test. The CY7B923 and CY7B933 HOTLink™ transmitter and receiver not only simplifies the design problem, but it offers the user a simple method to test the completed link. The built-in self-test feature, which can be activated using the built-in self-test enable (*BISTEN*) pin, allows for a real-time, off-line test of the entire link.

6 CONCLUSIONS AND RECOMMENDATIONS

6.1 Introduction

The object of this project was to develop a wideband hybrid analog and digital signal conditioning system for HV measurements using a CT or a CVT in the transconductance topology.

The transconductance topology imposes unique requirements on the signal conditioning instrumentation because of dynamic range of the output signals from the transducers and the strict offset requirements for accurate integration. The following specifications apply to the signal conditioning system as discussed in Chapter 1 and Chapter 2:

- A 5 MHz bandwidth is required since a maximum upper bandwidth of 500 kHz can be obtained from the CT and CVT transducers in the transconductance topology.
- Low pass filtering is necessary to remove the high frequency noise components.
- A minimum sampling rate for the ADC of 5 MHz is required.
- The integrator technology must be optimised to minimise dc offset problems.
- The integrated data must be scaled and decimated to reduce the data storage rate and the data sequence length but still contain sufficient information to reconstruct the original HV signal.
- Galvanic isolation is needed to eliminate the earthing problems associated with HV environments. EMI must be minimised.

This chapter presents test procedures and results of the developed system and some of the conclusions on the achievements of the system. The test procedures, results and conclusions will be discussed with respect to each of the subsystems defined in Chapter 2. Recommendations for future research, with reference to the shortcomings of the system, are given.

6.2 Test procedures and results

The analog signal conditioning subsystem, digital signal conditioning and the transmitting part of the link were incorporated on one 2-layer p.c. board. The receiving part of the link and the DAC are incorporated on another 2-layer p.c. board. Each subsystem was tested independently first to ensure that it functioned correctly and then the entire system was tested together although these tests, to a certain degree, were unsuccessful as will be explained further. The test procedures and results follow with respect to the each of the subsystems.

6.2.1 Analog signal conditioning subsystem

Although appearing with other subsystems on the same p.c. board, the analog signal conditioning subsystem was first built and tested. When tested independently of the other subsystems appearing on the p.c. board the practical results achieved matched well with the simulated results in terms of bandwidth expectations. For a gain of 1.2, the frequency response of the practical circuit began degrading well past the 10 MHz mark for a sinusoidal input of 100 mV. However, the output of the buffer was not referenced around 2.25 V as expected. Once the other subsystems were added onto the p.c. board the analog system began to show noise of the same nature as the 40 MHz and 25 MHz crystal oscillators that were on the board. This is discussed further in section 6.3.1.

6.2.2 Digital signal conditioning subsystem

Testing of the ADC was limited because of the noise appearing at the outputs of the analog signal conditioning subsystem. The reference signals from the ADC were offset slightly. This is explained in section 6.3.1. A test program was used to verify if the programmable digital integrator, time-domain decimator and range selector were implemented correctly. A test word, '100000000001', was programmed as an input to the FPGA. With a fixed input, the integrator functions as a counter where the output increases linearly with clock cycles. The outputs of the FPGA were examined using a logic analyser

to ensure that the counter was generated correctly with the LSB and MSB appearing correctly. The values of the two dipswitches were changed to verify that the programmable sampling clock generator, decimation clock generator and the range selection were implemented correctly.

6.2.3 High speed serial fibre-optic link

To confirm that the transmitter and receiver work together, the built-in self-test feature, accessible via the built-in self-test enable (*BISTEN*) pin, was used to allow for a real-time, off-line test of the entire link. A test pattern of alternating 1s and 0s was sent from the transmitter and it was verified using a logic analyser that the pattern appeared on the receiving end of the link.

When the test word, '1000000000001', discussed in section 6.2.2 was sent across the link, it was received by the DAC and correctly converted into its analog form. Since the digital integrator generated a pattern representing the output of linearly increasing counter, a ramp appeared at the output of the DAC. There were approximately 4000 points on each ramp whereafter it began to count again once it wrapped over. This meant that the DAC converted all 12-bits of the input data. However, there were many glitches in the output.

6.3 Conclusions

6.3.1 Analog signal conditioning subsystem

The high bandwidth specifications of the system made it necessary to consider both a discrete and an integrated implementation of this subsystem. Although the integrated implementation was used in the developed system, the discrete implementation showed very promising results.
The achievements of the discrete implementation can be summarised as follows:

- A design was achieved with –3 dB bandwidths of approximately 114 MHz and 20

MHz respectively for the input stage and the amplifier stage of the discrete implementation.

- The main problem associated with the implementation was the unavailability of transistor arrays with higher breakdown voltages. Admittedly, individual transistors with high breakdown voltages are available, but they will not be thermally and electrically matched.
- In terms of board space the discrete implementation becomes quite costly especially since the system being developed is for a portable sensor.
- However, if higher bandwidths of the system are required, i.e. greater than 5 MHz, the discrete implementation needs to be more closely examined and optimised further.

The achievements of the integrated implementation can be summarised as follows:

- This design has been optimised to serve as a linear amplifier and a first order low pass filter that transforms the input signal levels from the sensor to those required by the ADC, i.e. ±1 V centred around 2.25 V.
- The differential inputs reduces the EMI and earthing problems usually associated with HV environments.
- Gain adjustment of the developed system can be done in this subsystem although the gain has been fixed to 1.2 on the p.c. board for prototyping purposes.
- A low pass filter allows for attenuation of the high frequency noise components, which are amplified by the differentiating action of the CT terminal capacitance. The low pass filter has a cut off frequency of 100 MHz, which is 20 times that of the highest frequency of interest.
- Simulations show that for gains of 1.2 and 5 respectively, -3 dB bandwidths of approximately 220 MHz and 195 MHz are achieved. Practically, for a gain of 1.2, the implemented circuit began degrading well past the 10 MHz mark.
- In the developed system, the signals were centred around 2.1 V instead of 2.25 V. This was due to the low input impedance of the operational amplifier used in the buffering stage of the amplifier. The AD811 loads the ADC thereby offsetting the

offset reference 2.25 V reference signal.

- When tested together with the other subsystems, the analog signal conditioning subsystem displayed noise of the same nature of the crystal oscillators on the board. Being a two-layer board with many external looped wire connections for ground and power, there were inductance loops created. This made it impossible to test this subsystem together with the others.

6.3.2 Digital signal conditioning subsystem

This entire subsystem was successfully implemented on a single FPGA. The achievements of the subsystem can be summarised as follows:

- This subsystem has been optimised to digitise the analog signals, integrate and decimate, if necessary, the digitised data and to perform range selection.
- The 40 MHz ADC used allows for the accurate integration of signals with standard lightning impulse specifications.
- Programmable digital integration is versatile and easily adjustable to perform with the offset characteristics of the sensing and measuring equipment.
- To ensure integration over a dynamic range, data was integrated at 32-bit resolution.
- Hardware implementation makes it possible to decimate the data sequence and to perform range selection after integration.

6.3.3 High speed serial fibre-optic link

This subsystem was successfully implemented using fibre-optic and Programmable Logic Array (PLA) technology. The achievements of the subsystem implementation can be summarised as follows:

- The link has been optimised to transmit the output from the digital signal conditioning subsystem serially to the DAC and to convert the digital data back into its analog form.

- The link maintains optic isolation, which eliminates the earthing and EMI problems usually associated with HV environments.
- Converting the data stream into analog form makes the data suitable to be used as an input for commercial equipment.
- The link can be tested in isolation from the other subsystems by using the test mode whereby a repetitive pattern is sent across the link to ensure that the transmitter, receiver and fibre-optic cable function together correctly.

6.4 Recommendations

Although the developed system shows very promising results, the system needs to be refined to be perfectly suitable for the given applications. Based on the problems encountered during implementation of the proposed topology, the following recommendations should be considered:

- In order for the entire system to be tested it is essential that a 4-layer board be manufactured. Separate ground and power planes are needed. A ground plane provides a way to access a low inductance ground from anywhere on the board. In addition, it minimises the effects of stray capacitances in the circuit by referring them to ground. This breaks up unintended and harmful feedback paths.
- The analog signal conditioning subsystem must be terminated with an impedance matching network designed correctly to reflect the same input impedance as that of a typical oscilloscope.
- Auto-gain selection can be incorporated in the subsystem by using a number of resistors in parallel that will switch depending on the desired gain. This will be useful if the transmitter is at a high potential and the user is unable to handle the boards.
- Since the AD811 has a low input impedance relative to that of the OPA130, it should be replaced by it in the buffering circuit of the analog signal conditioning subsystem. The AD811 loads the ADC thereby lowering the reference voltage resulting in the signal levels being delivered to the ADC not being correctly centred. In the developed

system the reference voltage was reduced to 2.1V.

- Prior to integration, a digital high-pass filter is needed to filter out any offset generated from the analog signal conditioning subsystem. This is important since even though good analog design techniques will minimise offsets, it is an important consideration for any waveform with a large dynamic range and low average value e.g. the differentiated version of the standard lightning impulse discussed in Chapter 4.
- The 3 unused switches on *DIPSWB(0..7)* may be used to incorporate different test modes.
- A latch is required to interface the link to the DAC since the ADS800 does not have one internally
- A de-glitching circuit is needed after the DAC for precision waveform generation. A filter is also required since the DAC interfaces between the noisy high speed digital logic and the sensitive analog environment.
- The additional features and headers included for prototyping purposes (as discussed throughout the thesis) may be omitted on future boards.
- The power consumption of the entire system needs to be critically examined since it is admittedly high with the transmitter having the highest power dissipation of all the components (approximately 1 W) when transmitting information and data.
- The performance of the system needs to be tested under field conditions.

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Appendix A

Pspice programs, simulation results and schematic representations

This appendix presents the *Pspice* simulation programs and results for the analog signal conditioning subsystem. Simulation programs and results for both the discrete and integrated implementations of the subsystem are given with relevant circuit diagrams.

Discrete implementation of the analog signal conditioning subsystem

Input stage

Overall subsystem performance

Figure A.1 shows a schematic representation of the input stage of the discrete implementation of the analog signal conditioning subsystem with node numbers corresponding to its *Pspice* simulations. *Pspice* transient and frequency responses of the complete input stage (for inputs of 1 V and 10 V) follow in figures A.2-A.4.

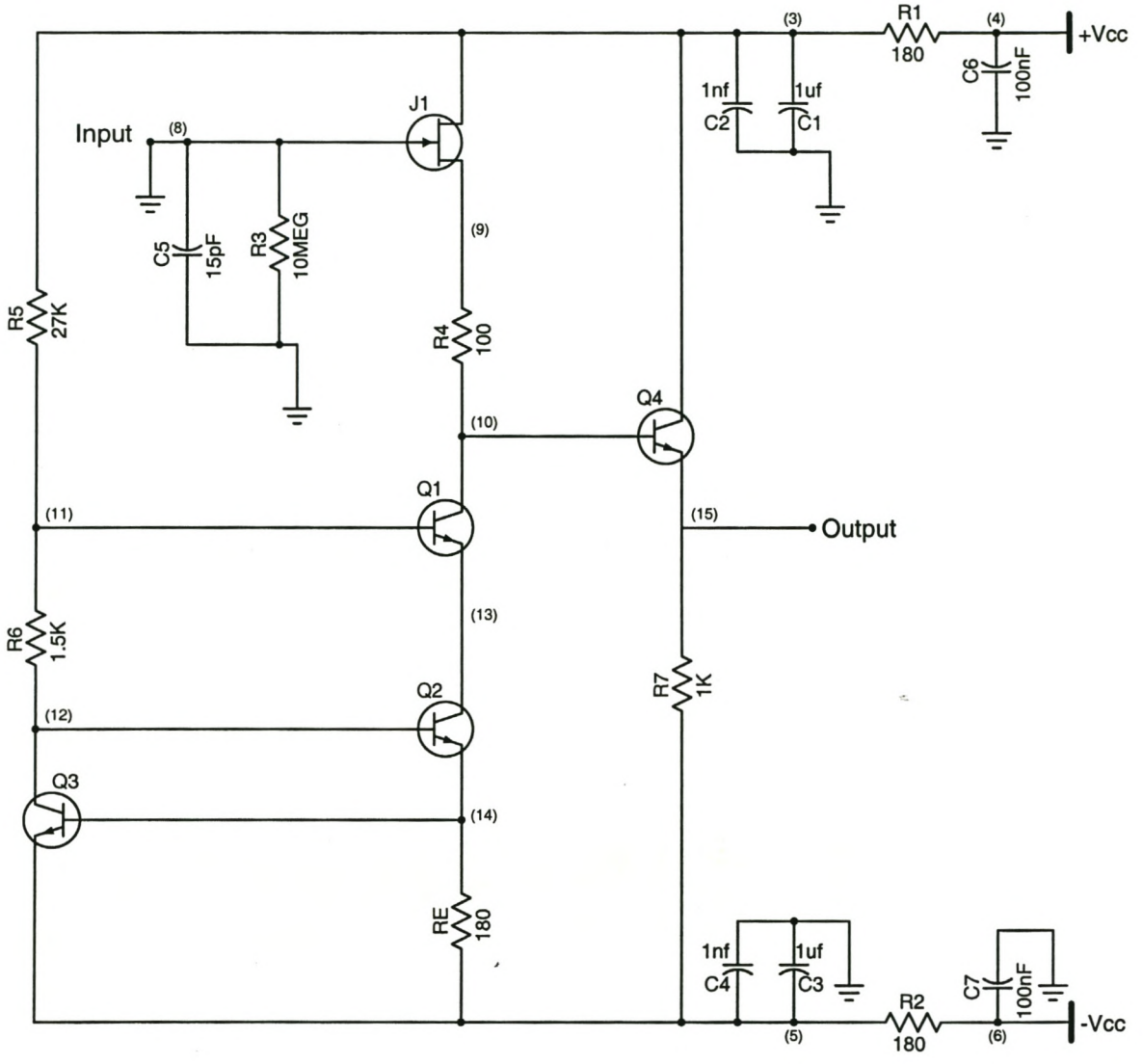

Fig. A.1: ***Schematic representation of the input stage of the discrete implementation.***

****

***Pspice* program for figure A.2**

```
***input stage of the discrete implementation of the analog signal conditioning subsystem
 **1V, 10MHz sinusoidal input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vsin 8 0 SIN(0 1V 10MEG 0 0 0)

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
```

```
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3478
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3478
R7 15 5 1K

.tran  100.000p  400.000n  0  100.000p  ; *ipsp*
.end
```

****

***Pspice* program for figure A.3**

```
***input stage of the discrete implementation of the analog signal conditioning subsystem
 **10V, 10MHz sinusoidal input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
```

```
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vsin 8 0 SIN(0 10V 10MEG 0 0 0)

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3478
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3478
```

```
R7 15 5 1K

.tran  100.000p  400.000n  0  100.000p  ; *ipsp*
.end
```

****

***Pspice* program for figure A.4**

```
***input stage of the discrete implementation of the analog signal conditioning subsystem
 **1V, A.C input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vin 8 0 AC 1

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
```

```
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3478
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3478
R7 15 5 1K

.ac dec   101  10   1000.000meg  ; *ipsp*
.end
```

****

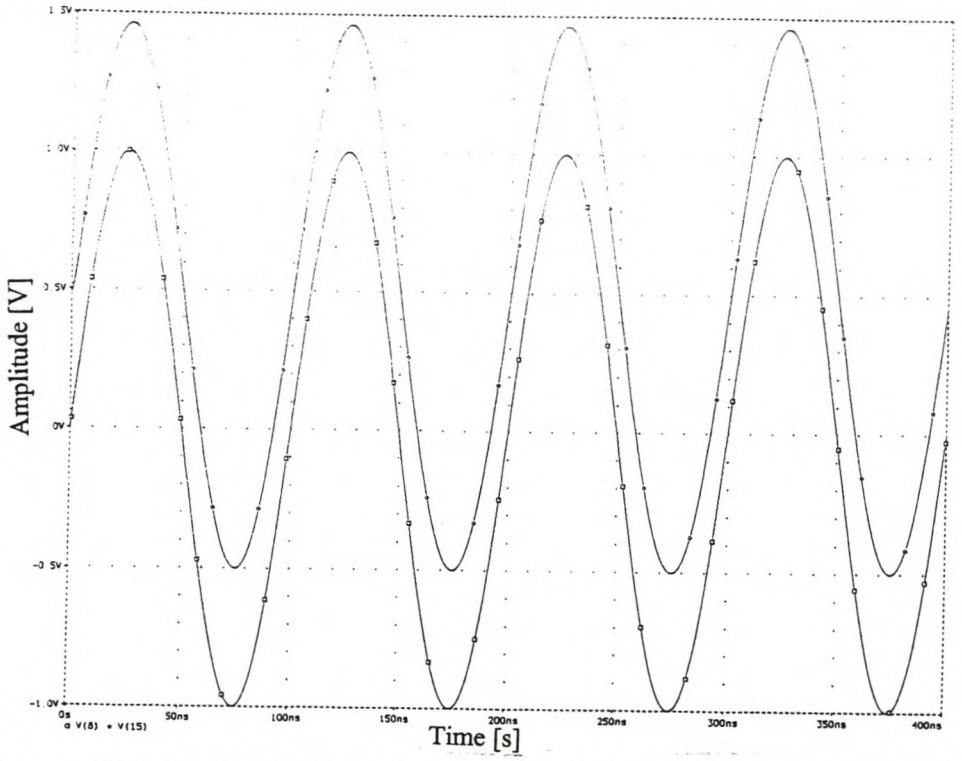

Fig. A.2: ***Simulated transient response of the input and output voltages of the input stage (for a 1V, 10MHz input).***

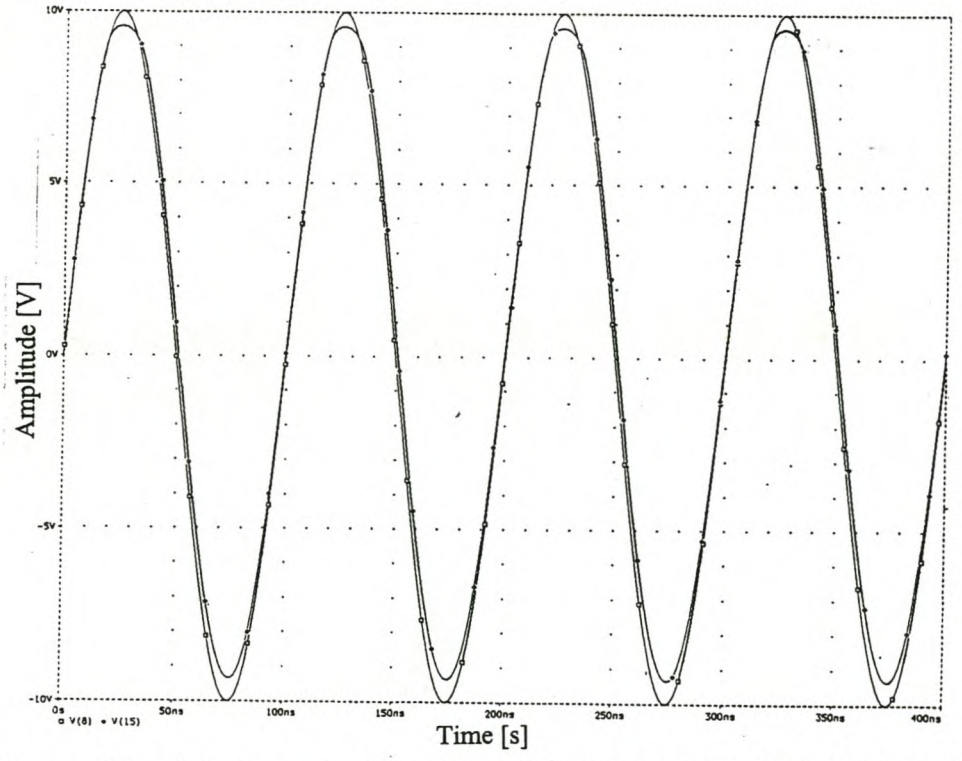

Fig. A.3: ***Simulated transient response of the input and output voltages of the input stage (for a 10V, 10MHz input).***

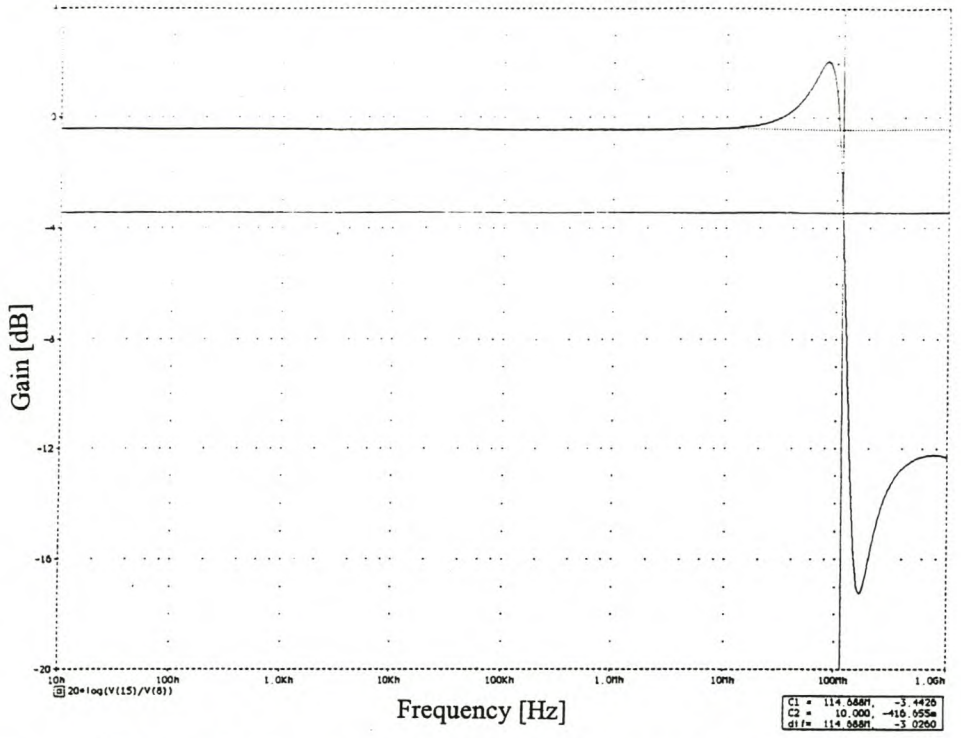

Fig. A.4: ***Simulated frequency response of the output voltage with respect to the input voltage for the input stage (for a 1V A.C. input).***

Optimisation of transistors

Pspice simulations for the optimisation of the FET and BJTs follow in figures A.5-A.8. Figures A.5 and A.6 show the input impedance of FET J_1 (for a 1 V, A.C. input) as it appears in figure A.1 using a 2N5486 and a 2N5245 respectively. Figures A.7 shows a transient response (for a 10 MHz, 10 V input) of the circuit with BJTs Q_1-Q_4 as 2N3904s. Figure A.8 gives a transient response (for a 10 MHz, 10 V input) of the circuit with Q_1-Q_4 as 2N3904s and an additional capacitance, C_{CE}, between the collector and emitter of Q_1.

****

***Pspice* program for figure A.5**

***input stage of the discrete implementation of the analog signal conditioning subsystem
**optimising FET J1 (2N5486), 1V A.C. input

*libraries

```
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vin 8 0 AC 1

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3478
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
```

```
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3478
R7 15 5 1K

.ac dec   101   10   1000.000meg  ; *ipsp*
.end
```

****

***Pspice* program for figure A.6**

```
***input stage of the discrete implementation of the analog signal conditioning subsystem
 **optimising FET J1 (2N5245), 1V A.C. input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vin 8 0 AC 1

 *power supply decoupling and LP filter
```

```
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5245
R3 8 0 10MEG
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3478
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3478
R7 15 5 1K

.ac dec   101   10   1000.000meg   ; *ipsp*
.end
```

****

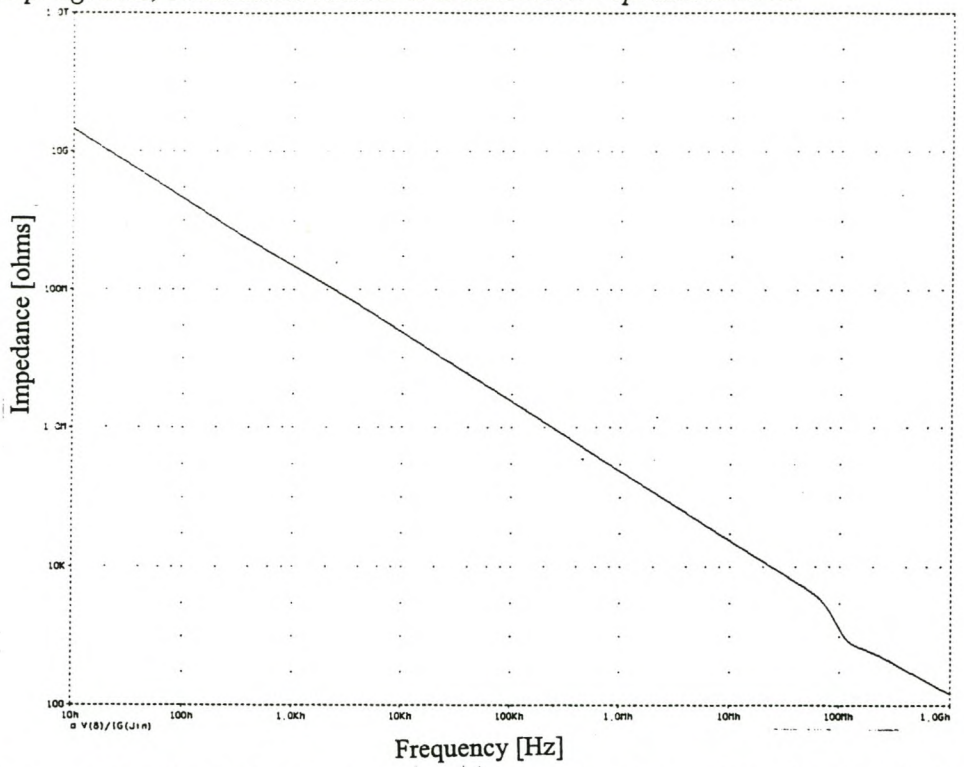

Fig. A.5: ***Simulated frequency response of the input impedance of J_1 using a 2N5486 (for a 1V, A.C. input).***

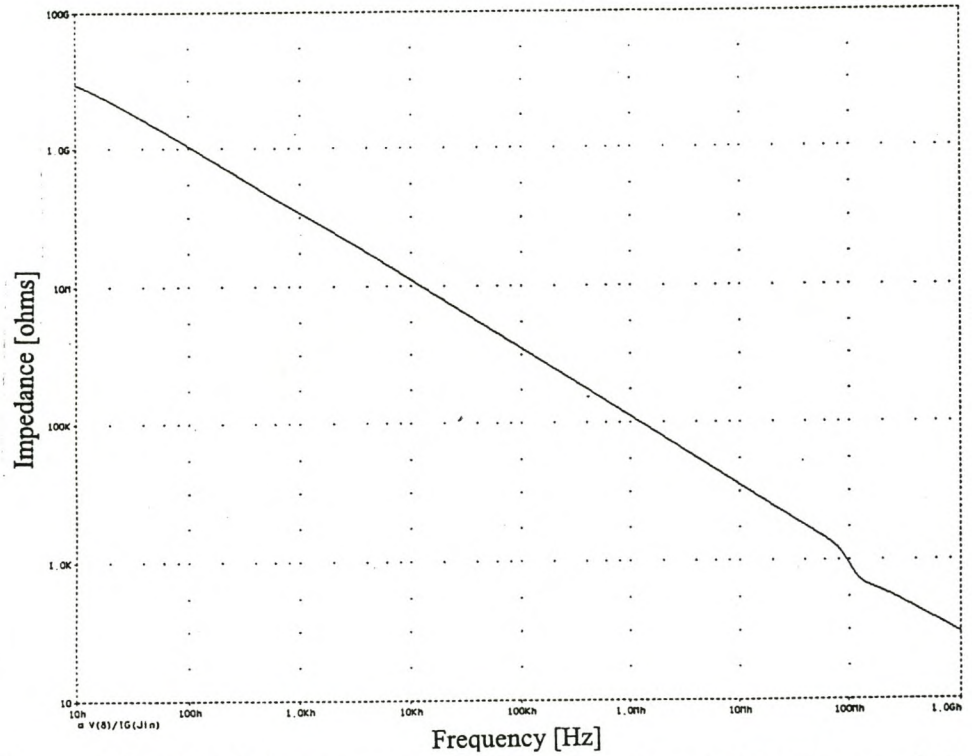

Fig. A.6: ***Simulated frequency response of the input impedance of J_1 using a 2N5245 (for a 1V, A.C. input).***

****

***Pspice* program for figure A.7**

```
***input stage of the discrete implementation of the analog signal conditioning subsystem
 **optimising transistors Q1-Q4 (2N3904s), 10V, 10MHz input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vsin 8 0 SIN(0 10V 10MEG 0 0 0)

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
```

```
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3904
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180

 *output buffer
Q4 3 10 15 Q2N3904
R7 15 5 1K

.tran  100.000p  400.000n  0  100.000p  ; *ipsp*
.end
```

****

***Pspice* program for figure A.8**

```
***input stage of the discrete implementátion of the analog signal conditioning subsystem
 **optimising transistors Q1-Q4 (additional capacitance between emitter and collector of
 Q1), 10V, 10MHz input

 *libraries
.lib d:\pspice5\lib\JFET.lib
.lib d:\pspice5\lib\BIPOLAR.lib

 *voltage sources
Vcc 4 0 15V
```

```
Vss 6 0 -15V
Ccc 4 0 100nf
Css 6 0 100nf

 *input signals
Vsin 8 0 SIN(0 10V 10MEG 0 0 0)

 *power supply decoupling and LP filter
R1 4 3 180
C1 3 0 1uf
C2 3 0 1nf

R2 6 5 180
C3 5 0 1uf
C4 5 0 1nf

 *FET source follower
Jin 3 8 9 J2N5486
R3 8 0 10MEG
C5 8 0 15pf
R4 10 9 100

 *biasing
Q1 10 11 13 Q2N3904
Q2 13 12 14 Q2N3904
Q3 12 14 5 Q2N3904
R5 11 3 27K
R6 12 11 1.5K
RE 14 5 180
Cce 13 10 10pf
```

```
 *output buffer
Q4 3 10 15 Q2N3904
R7 15 5 1K

.tran  100.000p  400.000n  0  100.000p  ; *ipsp*
.end
```

****

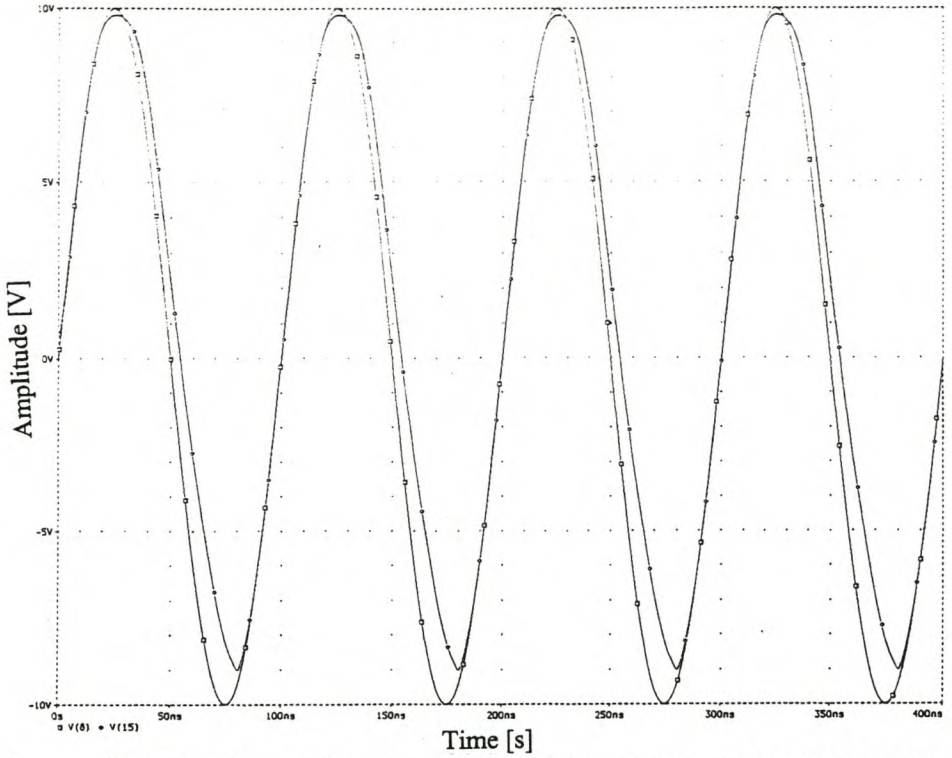

Fig. A.7: ***Simulated transient response of the input and output voltages using 2N3904s for Q_1-Q_4 (for a 10V, 10MHz input).***

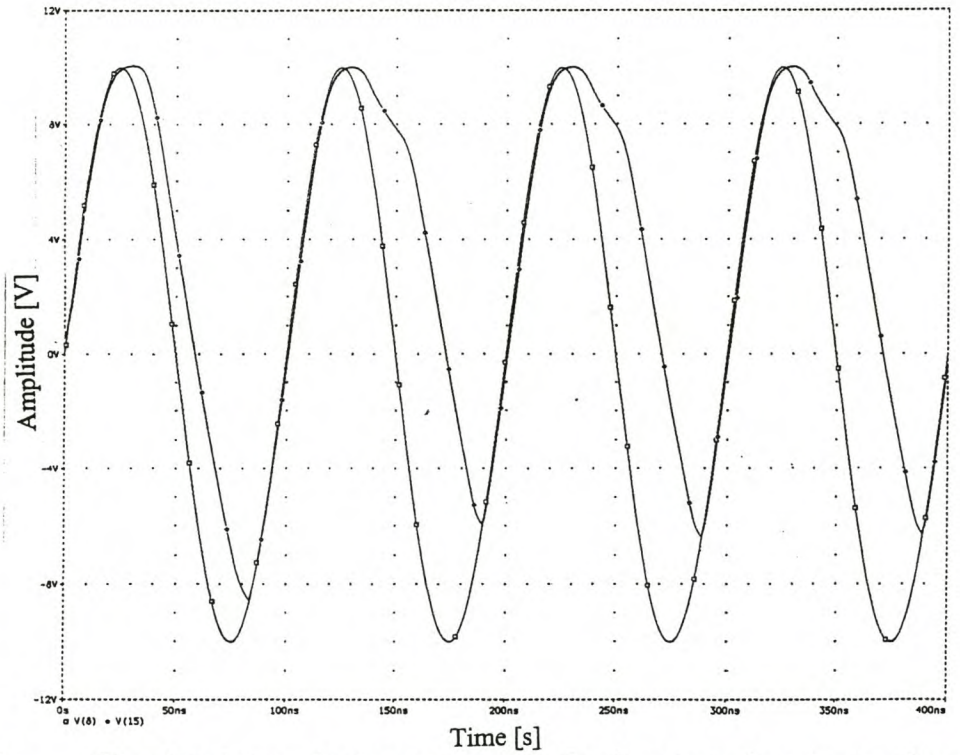

Fig. A.8: ***Simulated transient response of the input and output voltages using 2N3904s for Q_1-Q_4 with additional C_{CE} on Q_1 (for a 10V, 10MHz input).***

Amplifier stage

Overall circuit performance

Figure A.9 shows a schematic representation of the amplifier stage of the discrete implementation of the analog signal conditioning subsystem with node numbers corresponding to its *Pspice* simulations. *Pspice* transient and frequency responses of the complete amplifier stage (for inputs of 100 mV) follow in figures A.10-A.12.

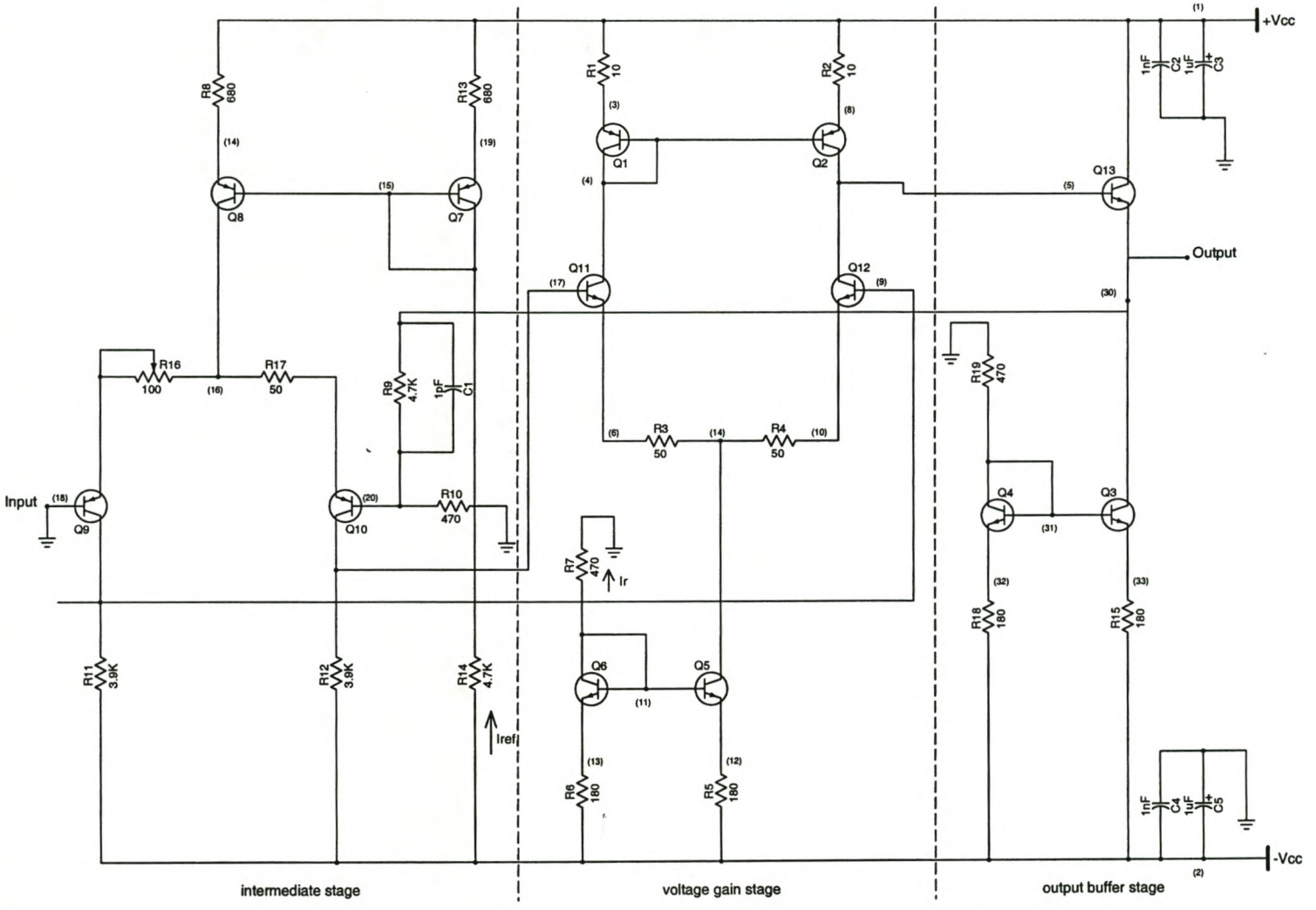

Fig. A.9: ***Schematic representation of the amplifier stage of the discrete implementation.***

****

***Pspice* program for figure A.10**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **0.1V, 10MHz sinusoidal input

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vsin 18 0 SIN(0 .1V 10MEG 0 0 0)

 *intermediate stage
  **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 9 2 3.9K
```

```
R12 17 2 3.9K

 **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
 **differential cascode stage
 **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
```

```
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.tran   1n   1.2u   0   1n  ; *ipsp*
.end
```

****

***Pspice* program for figures A.11 and A.12**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **0.1V, A.C. input

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
```

```
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
  **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 9 2 3.9K
R12 17 2 3.9K

  **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
  **differential cascode stage
  **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
```

```
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

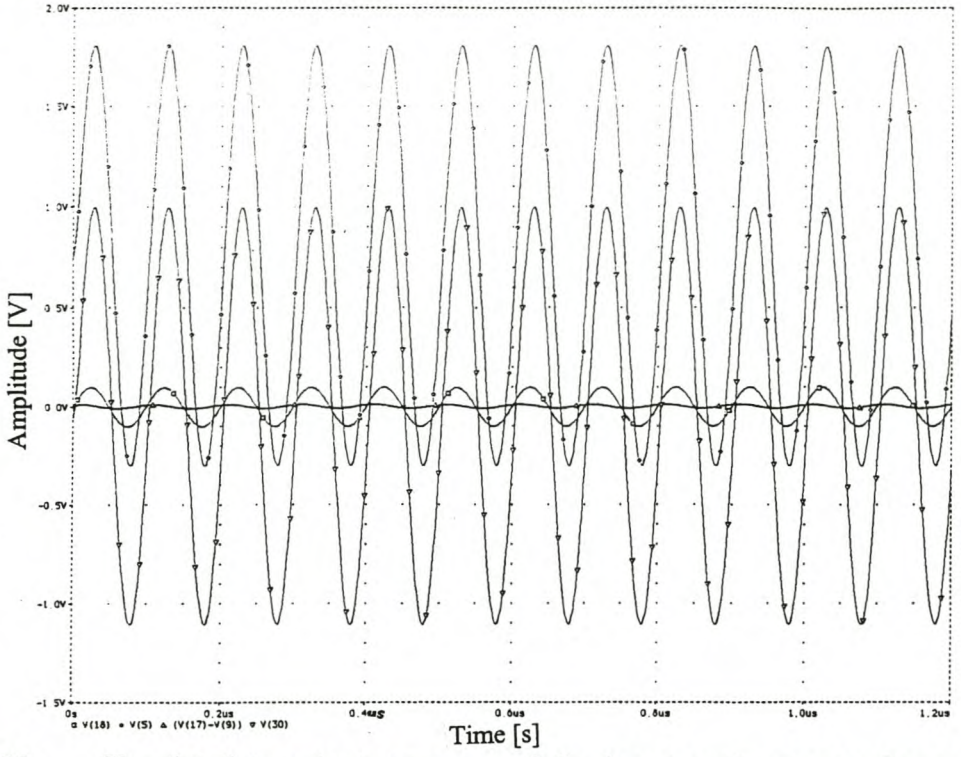

Fig. A.10: ***Simulated transient response of the input and output voltages of each stage of the amplifier stage (for a 100mV, 10MHz input).***

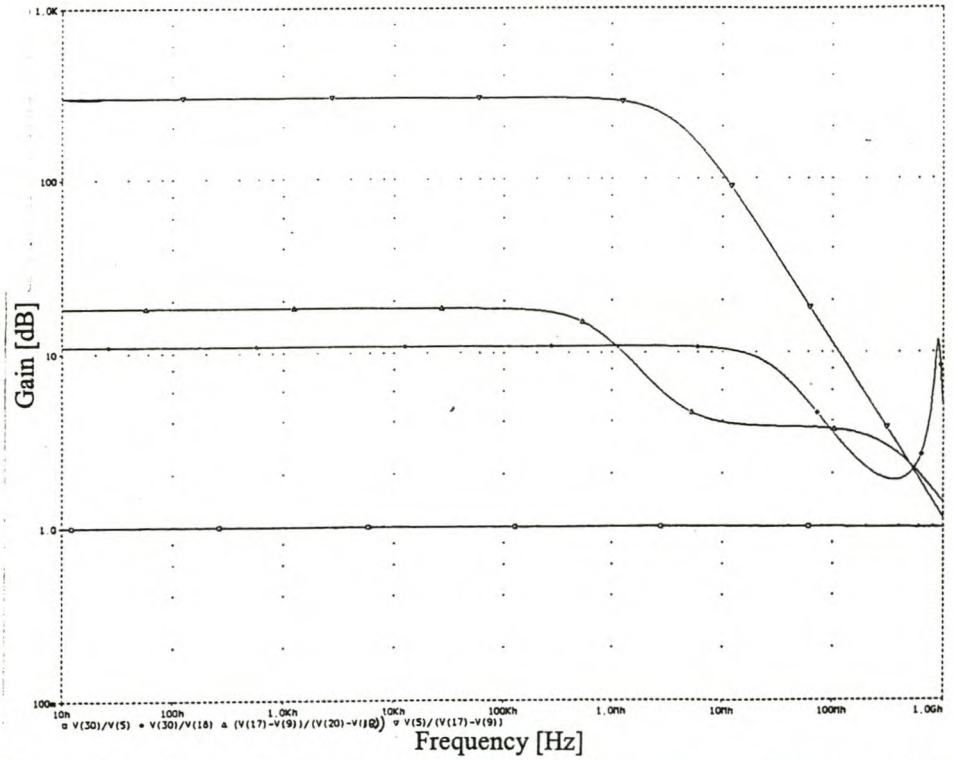

Fig. A.11: ***Simulated frequency response of the output voltages relative to the inputs, for each stage of the amplifier stage (for a 100mV, A.C. input).***

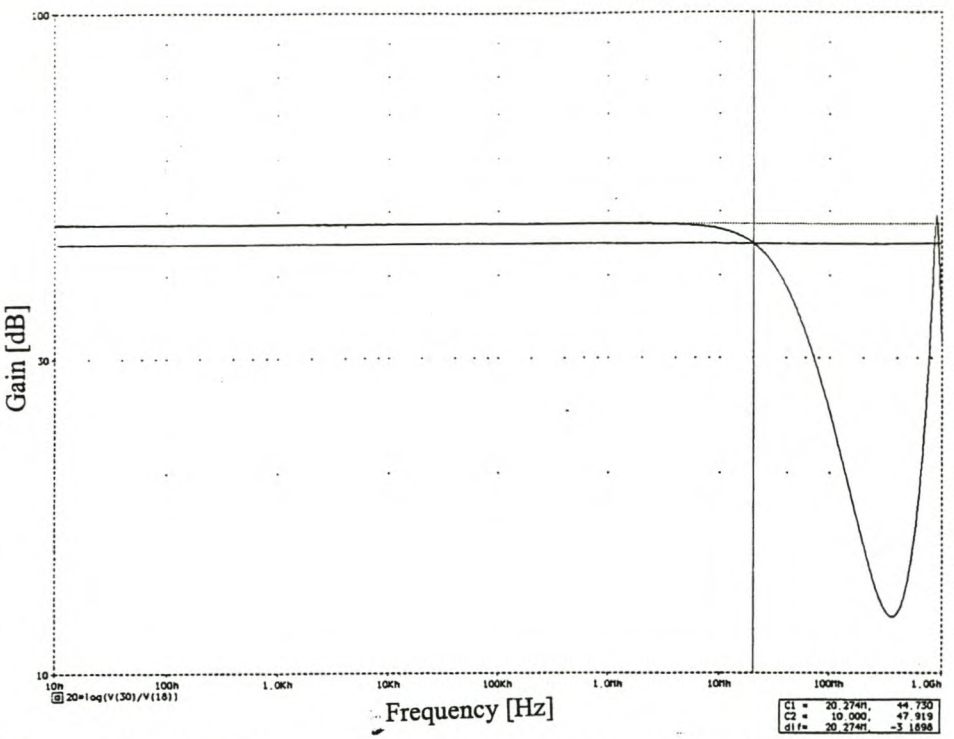

Fig. A.12: ***Simulated frequency response of the gain, in decibels, of the amplifier stage (for a 100mV, A.C input).***

Optimisation of the amplifier stage

Figures A.13-A.20 show frequency responses of the amplifier stage for the iterative processes shown in Table A.1 used to optimise the design of the amplifier stage.

Table A.1: ***Iteration processes to optimise the amplifier stage of the discrete implementation of the analog signal conditioning subsystem.***

	Current source 1	Current source 2	Current mirror
1	Ideal	Ideal	Ideal
2	Non-ideal	Non-ideal	Ideal
3	Ideal	Non-ideal	Ideal
4	Non-ideal	Ideal	Ideal
5	Ideal	Ideal	Non-ideal
6	Non-ideal	Non-ideal	Non-ideal
7	Ideal	Non-ideal	Non-ideal
8	Non-ideal	Ideal	Non-ideal

****

***Pspice* program for figure A.13**

***amplifier stage of the discrete implementation of the analog signal conditioning subsystem

**optimising design-iteration 1

*libraries

.lib d:\pfiles\lib\HFA3096b.lib

.lib d:\pfiles\lib\HFA3096.lib

*voltage sources

Vcc 1 0 +3.3V

Vss 2 0 -3.3V

*power supply bypassing

C2 1 0 1nf

C3 1 0 1uf

C4 2 0 1nf

C5 2 0 1uf

*input signals

Vin 18 0 AC .1

*intermediate stage

**input differential stage

Q9 9 18 24 PUHFARRY

Q10 17 20 25 PUHFARRY

R16 24 16 47

R17 25 16 47

R11 2 9 3.9K

```
R12 17 2 3.9K

 **ideal current source 1 (1.3mA)
I1 1 16 1.3mA

 *voltage gain stage
 **differential cascode stage
 **current-controlled-current source
V1 3 4 DC 0
Fsense 8 5 V1 1

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **ideal current source 2 (4mA)
I2 7 2 4mA

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
```

```
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.14**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 2

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
```

```
 **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

 **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

*voltage gain stage
 **differential cascode stage
 **current-controlled-current source
V1 3 4 DC 0
Fsense 8 5 V1 1

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
```

```
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.15**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 3

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib
```

```
*voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

*power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

*input signals
Vin 18 0 AC .1

*intermediate stage
 **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

 **ideal current source 1 (1.3mA)
I1 1 16 1.3mA

*voltage gain stage
 **differential cascode stage
 **current-controlled-current source
V1 3 4 DC 0
Fsense 8 5 V1 1
```

```
Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end

**********************************************************************
```

Pspice program for figure A.16

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 4

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
  **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K
```

```
 **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
 **differential cascode stage
 **current-controlled-current source
V1 3 4 DC 0
Fsense 8 5 V1 1

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **ideal current source 2 (4mA)
I2 7 2 4mA

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470
```

```
*feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.17**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 5

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1
```

```
*intermediate stage
 **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

 **ideal current source 1 (1.3mA)
I1 1 16 1.3mA

*voltage gain stage
 **differential cascode stage
 **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **ideal current source 2 (4mA)
I2 7 2 4mA

*output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
```

```
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.18**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 6

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
```

```
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
  **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

  **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
  **differential cascode stage
  **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
```

```
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.19**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
```

```
subsystem
 **optimising design-iteration 7

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
  **input differential stage
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

  **ideal current source 1 (1.3mA)
I1 1 16 1.3mA
```

```
*voltage gain stage
**differential cascode stage
**current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

**current source 2 (4mA)
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

*output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

*feedback path
R9 30 20 4.7K
R10 20 0 470
```

```
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

***Pspice* program for figure A.20**

```
***amplifier stage of the discrete implementation of the analog signal conditioning
subsystem
 **optimising design-iteration 8

 *libraries
.lib d:\pfiles\lib\HFA3096b.lib
.lib d:\pfiles\lib\HFA3096.lib

 *voltage sources
Vcc 1 0 +3.3V
Vss 2 0 -3.3V

 *power supply bypassing
C2 1 0 1nf
C3 1 0 1uf
C4 2 0 1nf
C5 2 0 1uf

 *input signals
Vin 18 0 AC .1

 *intermediate stage
  **input differential stage
```

```
Q9 9 18 24 PUHFARRY
Q10 17 20 25 PUHFARRY
R16 24 16 47
R17 25 16 47
R11 2 9 3.9K
R12 17 2 3.9K

 **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
  **differential cascode stage
  **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 4 17 6 NUHFARRY
Q12 5 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

  **ideal current source 2 (4mA)
I2 7 2 4mA

 *output buffer stage
```

```
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end

**********************************************************************
```

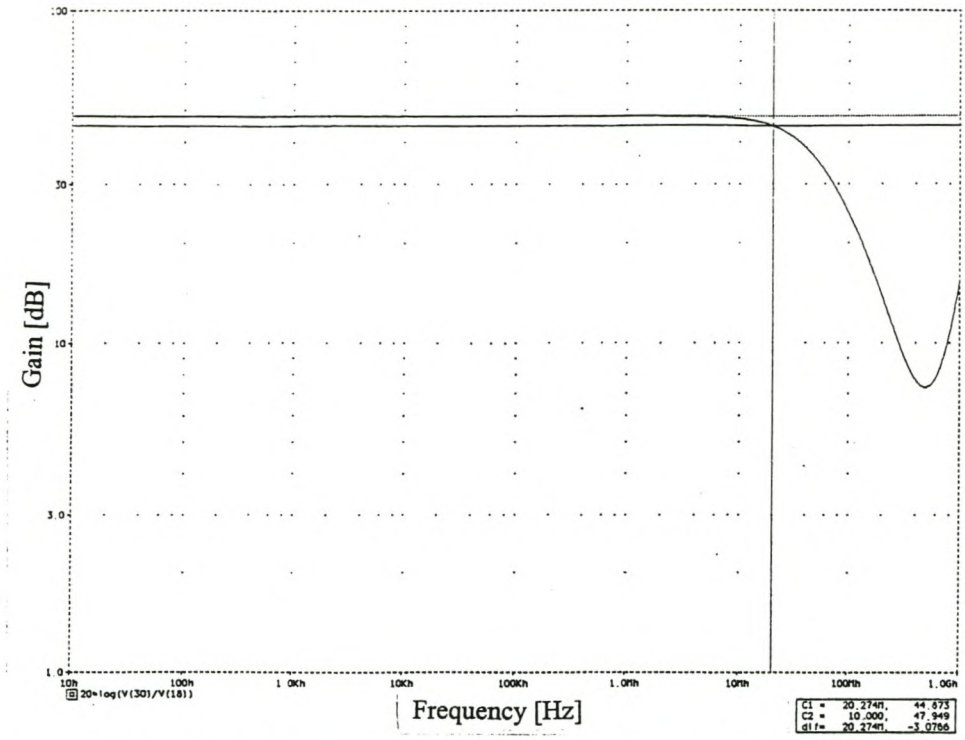

Fig. A.13: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 1.***

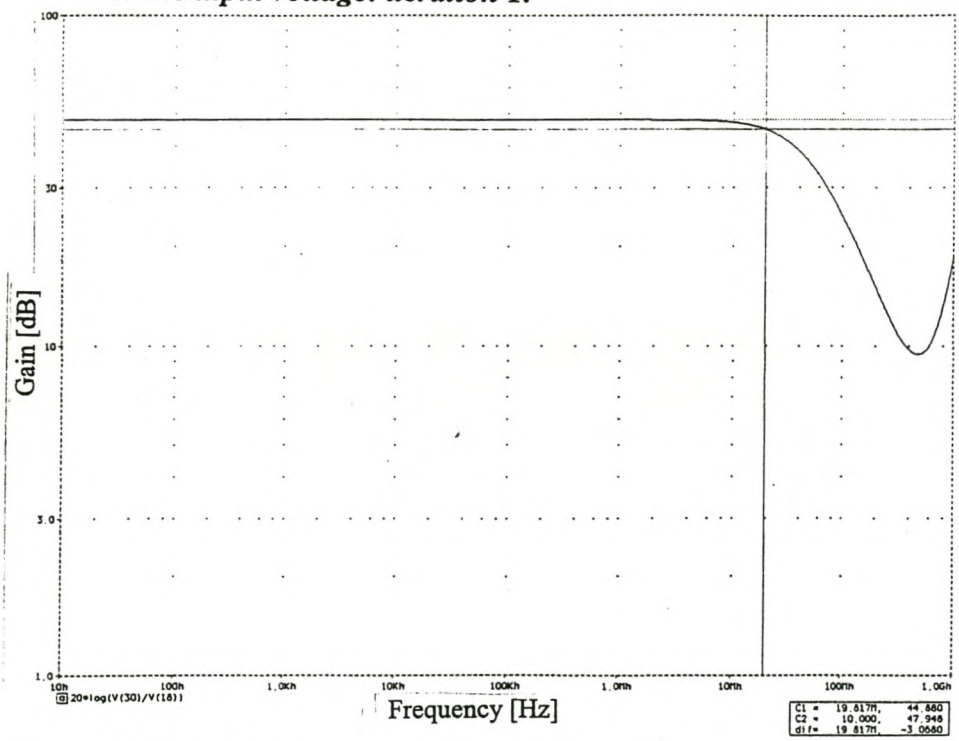

Fig. A.14: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 2.***

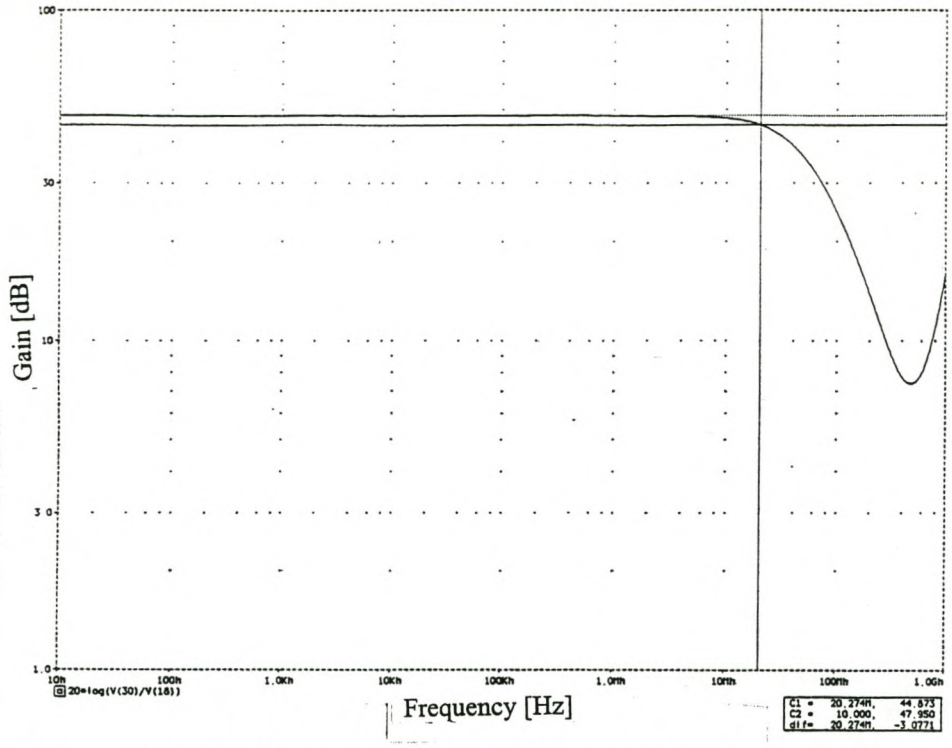

Fig. A.15: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 3.***

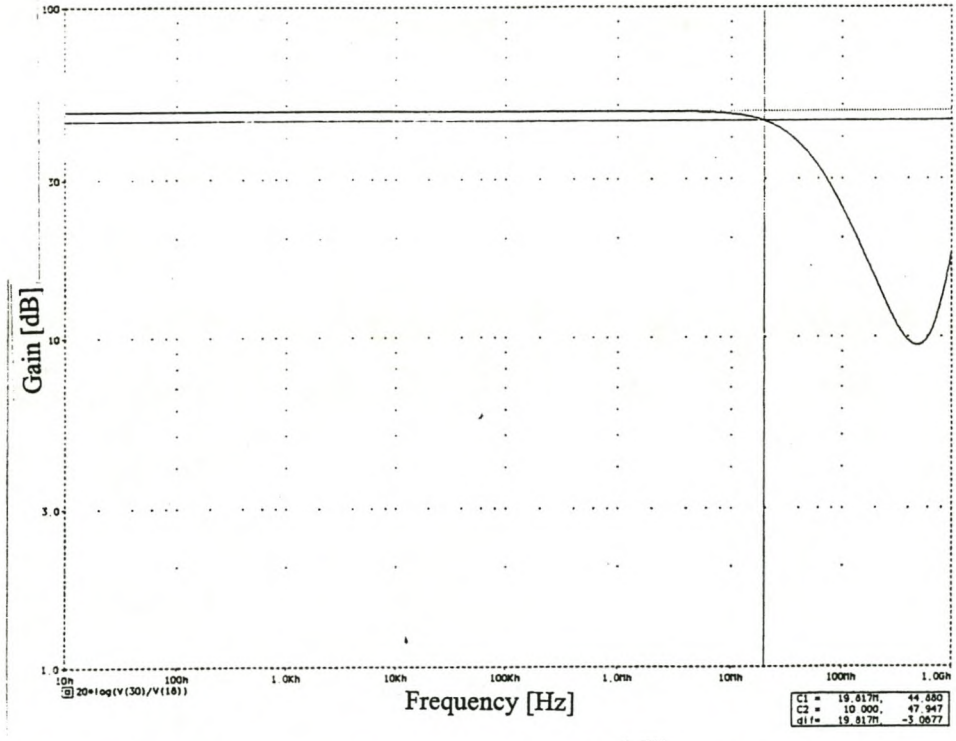

Fig. A.16: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 4.***

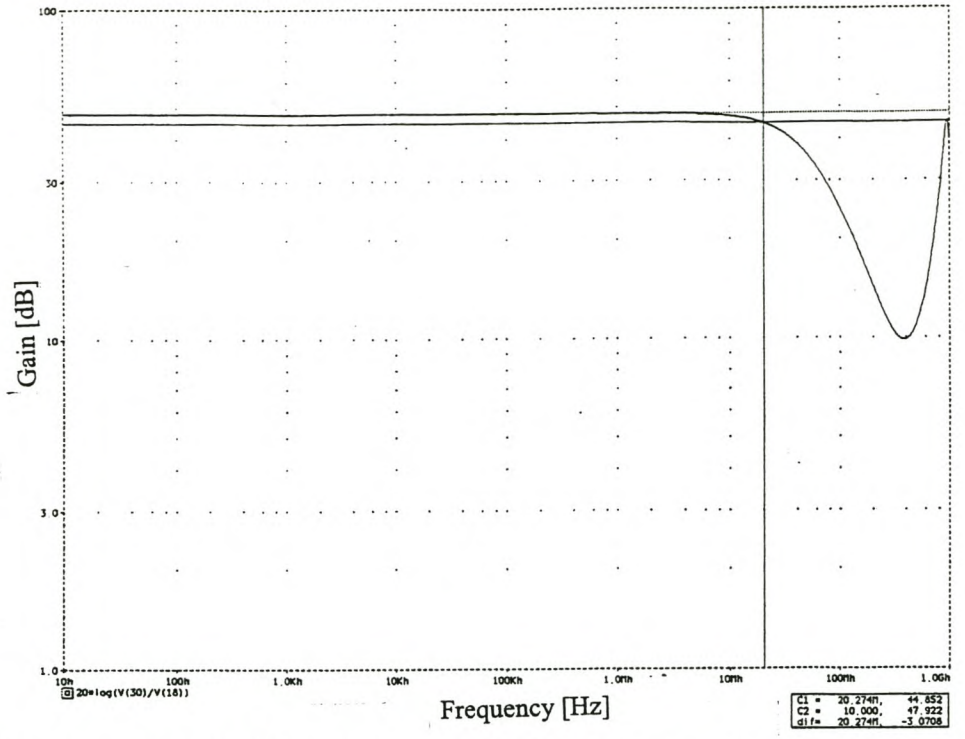

Fig. A.17: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 5.***

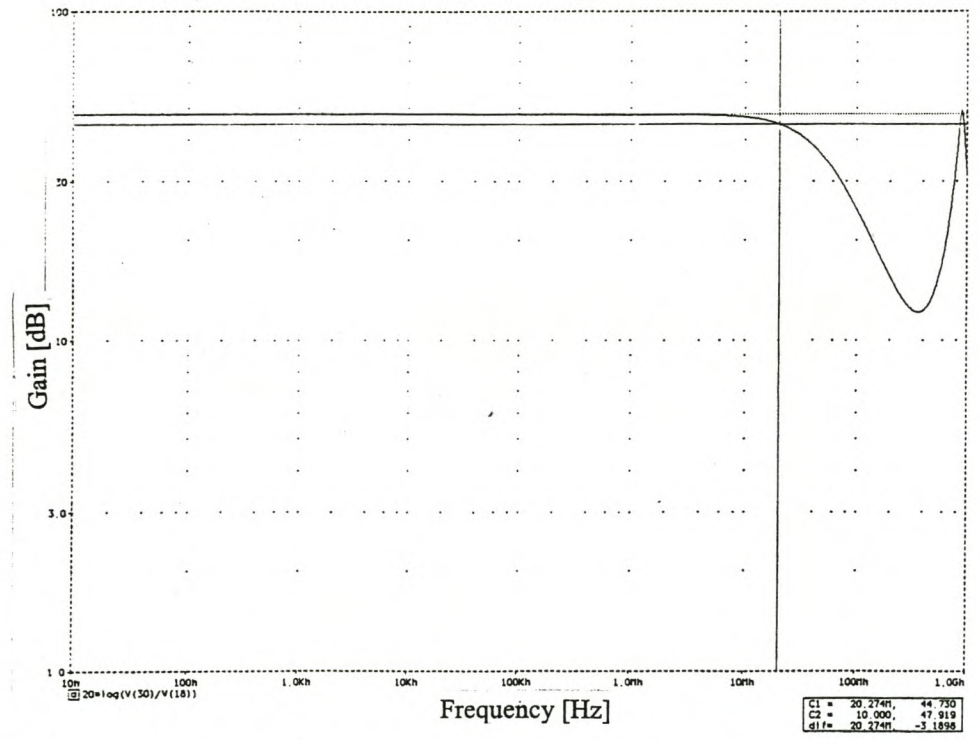

Fig. A.18: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 6.***

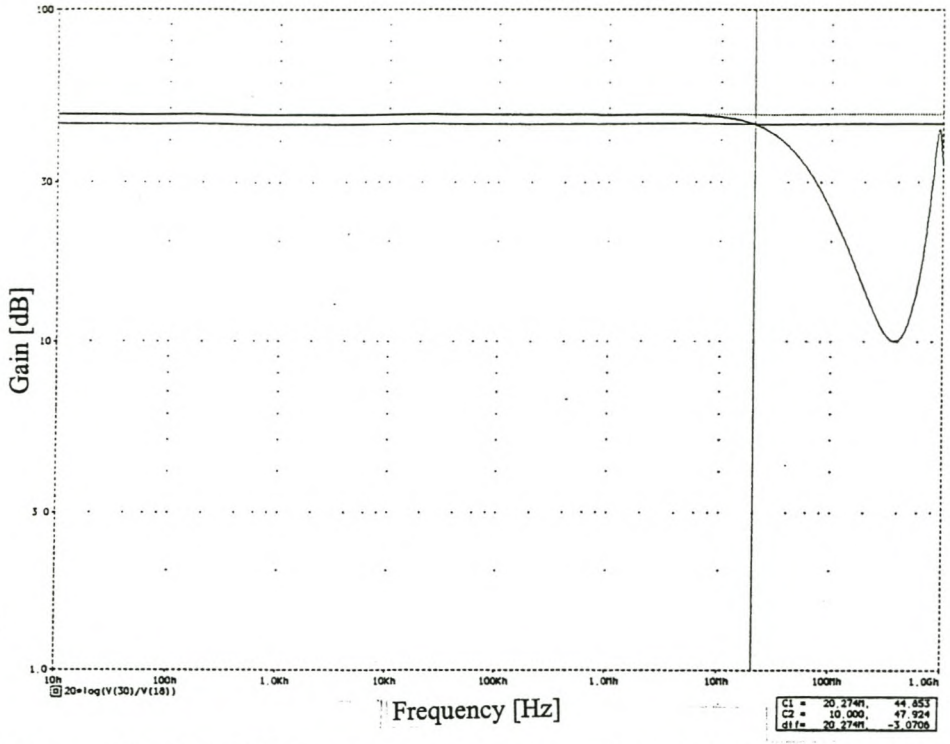

Fig. A.19: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 7.***

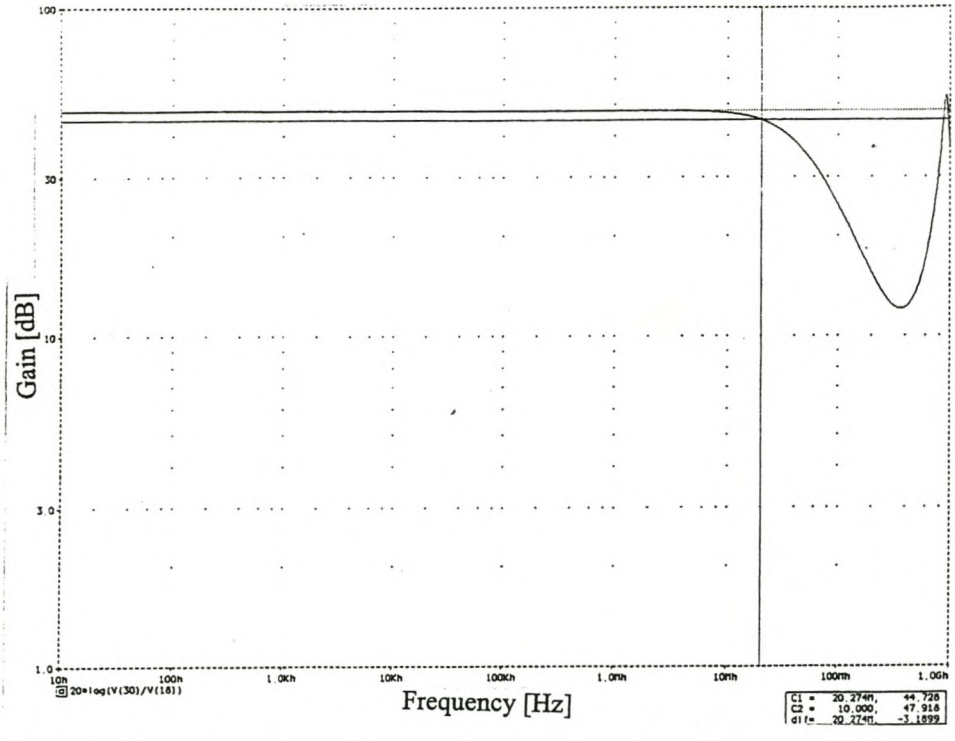

Fig. A.20: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage: iteration 8.***

Additional cascode stage

In an attempt to improve the bandwidth of the amplifier stage an additional cascode stage was included. Figure A.21 shows the amplifier stage with an additional cascode stage added to the voltage gain stage of the amplifier as it appears in figure A.9.

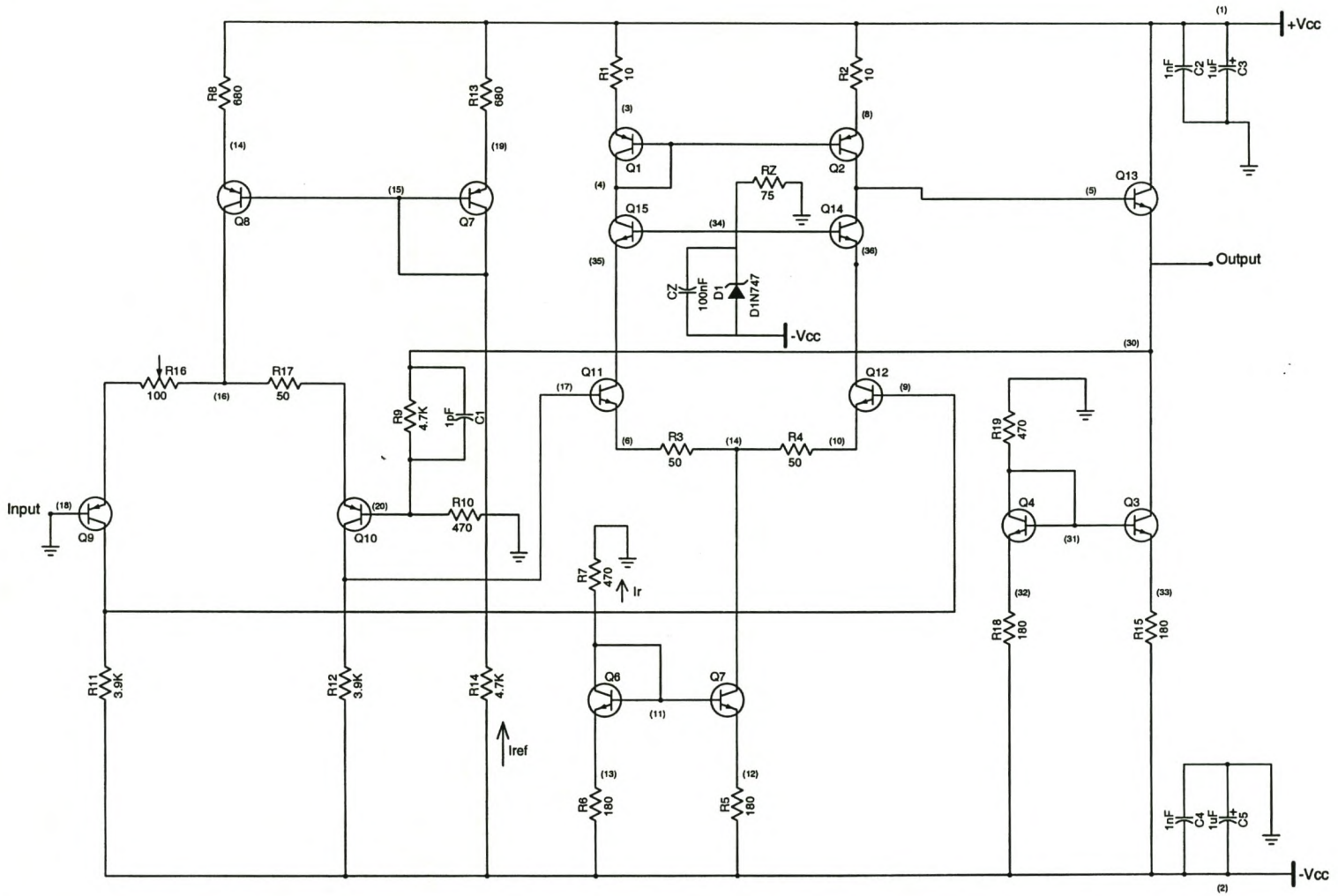

Fig. A.21: ***Schematic representation of the amplifier stage with additional cascode stage.***

****

***Pspice* program for figure A.22**

***amplifier stage of the discrete implementation of the analog signal conditioning subsystem

**additional cascode stage-iteration 6

*libraries

.lib d:\pfiles\lib\HFA3096b.lib

.lib d:\pfiles\lib\HFA3096.lib

.lib d:\pfiles\lib\DIODE.lib

*voltage sources

Vcc 1 0 +3.3V

Vss 2 0 -3.3V

*power supply bypassing

C2 1 0 1nf

C3 1 0 1uf

C4 2 0 1nf

C5 2 0 1uf

*input signals

Vin 18 0 AC .1

*intermediate stage

**input differential stage

Q9 9 18 24 PUHFARRY

Q10 17 20 25 PUHFARRY

R16 24 16 47

R17 25 16 47

```
R11 2 9 3.9K
R12 17 2 3.9K

 **current source 1 (1.3mA)
Q7 15 15 19 PUHFARRY
Q8 16 15 14 PUHFARRY
R8 14 1 680
R13 19 1 680
R14 15 2 4.7K

 *voltage gain stage
 **differential cascode stage
 **current mirror
Q1 4 4 3 PUHFARRY
Q2 5 4 8 PUHFARRY

Q11 35 17 6 NUHFARRY
Q12 36 9 10 NUHFARRY
R1 3 1 10
R2 8 1 10
R3 7 6 47
R4 10 7 47

 **additional cascode stage
Q15 4 34 35 NUHFARRY
Q14 5 34 36 NUHFARRY
D1 2 34 D1N747
Cz 34 2 100nf
Rz 34 0 75

 **current source 2 (4mA)
```

```
Q5 7 11 12 NUHFARRY
Q6 11 11 13 NUHFARRY
R5 12 2 180
R6 13 2 180
R7 11 0 470

 *output buffer stage
Q3 30 31 33 NUHFARRY
Q4 31 31 32 NUHFARRY
Q13 1 5 30 NUHFARRY
R15 33 2 180
R18 32 2 180
R19 31 0 470

 *feedback path
R9 30 20 4.7K
R10 20 0 470
C1 30 20 1pf

.ac dec   101   10   1000.000MEG  ; *ipsp*
.end
```

****

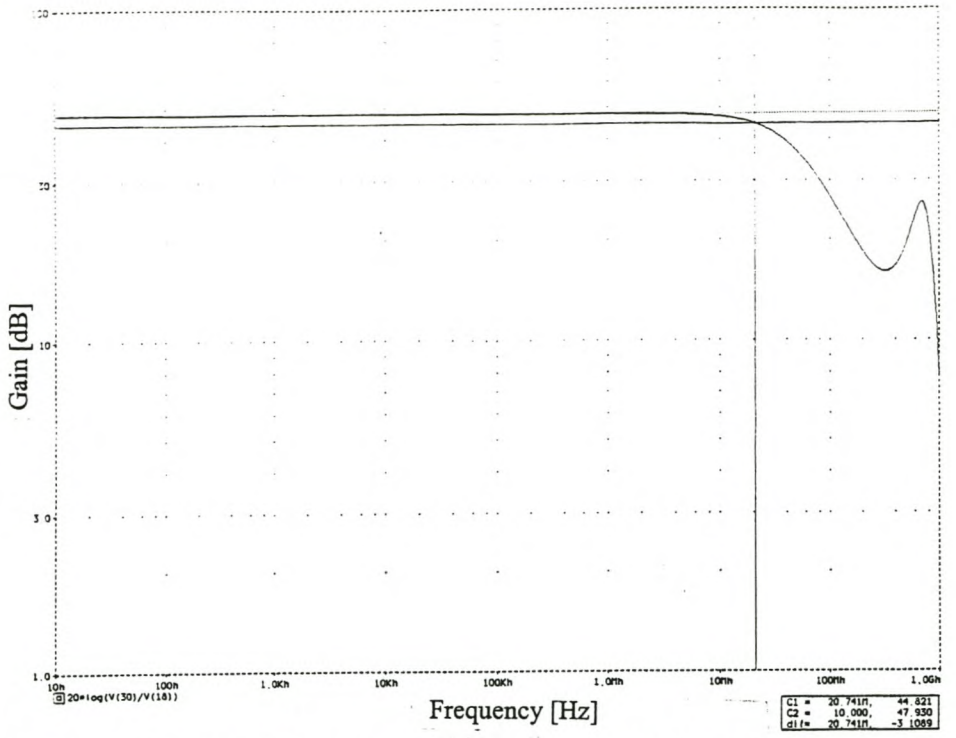

Fig. A.22: ***Simulated frequency response, in decibels, of the output voltage relative to the input voltage with the additional cascode stage: iteration 6.***

Integrated implementation of the analog signal conditioning subsystem

Overall subsystem performance

Figure A.23 shows a schematic representation of the integrated implementation of the analog signal conditioning subsystem with node numbers in brackets corresponding to its *Pspice* simulations. *Pspice* transient and frequency responses of the complete input stage (for an input of 0.1 V and a gain of 5) are given in figures 3.13 and 3.14 in Chapter 3. Simulation programs for these responses follow.

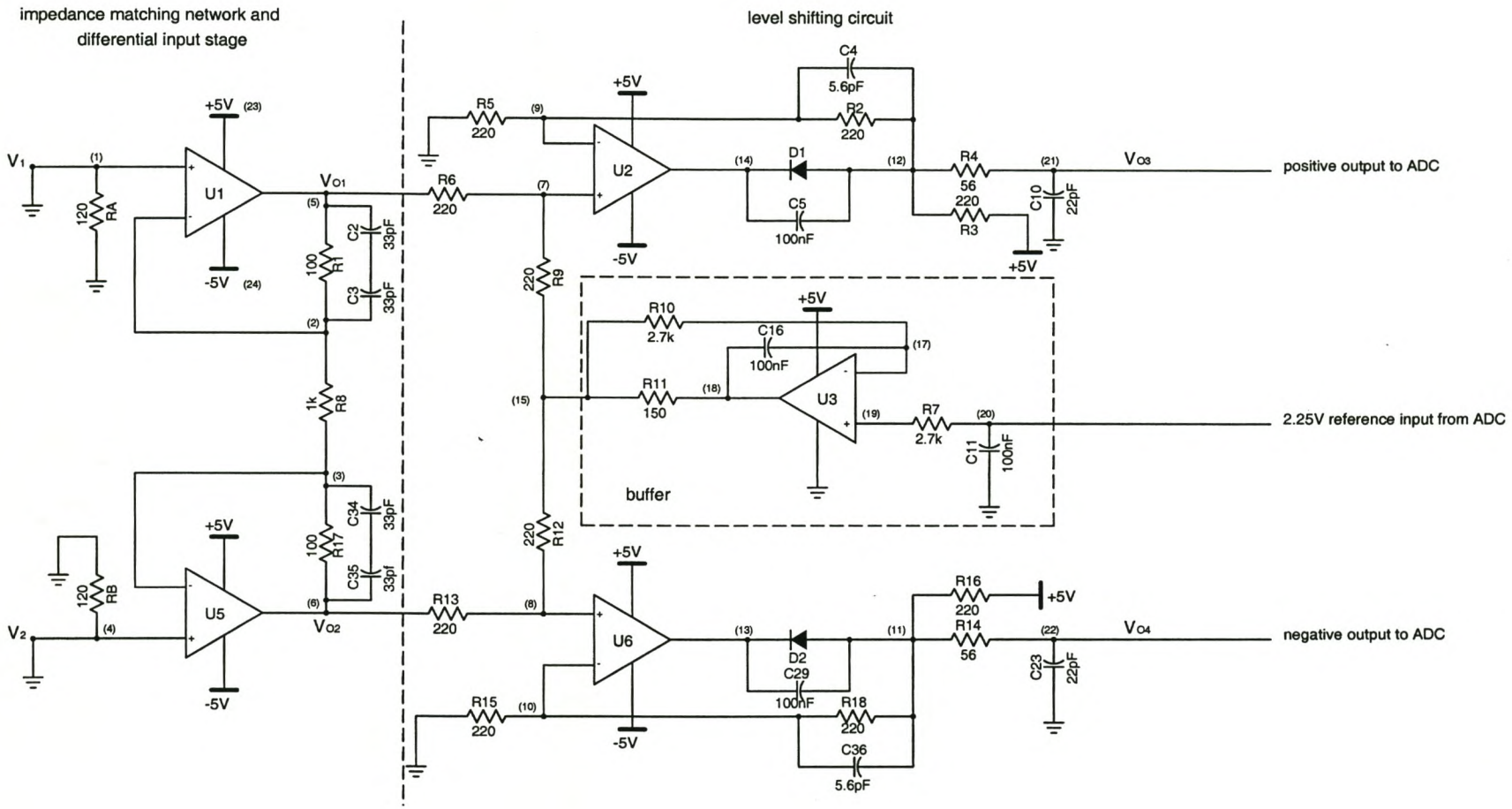

Fig. A.23: Schematic representation of the integrated implementation.

Pspice program for figure 3.13

```
***integrated implementation of the analog signal conditioning subsystem
 **0.1V, 10MHz sinusoidal input

 *libraries
.lib d:\pfiles\lib\AD811b.lib
.lib d:\pfiles\lib\OPA130.lib
.lib d:\pspice5\lib\DIODE.lib

 *voltage sources
Vcc 23 0 +5V
Vss 24 0 -5V

 *input signals
Vcm 25 0 DC 0
Vsin1 1 25 SIN(0 .05 10MEG 0 0 0)
Vsin2 25 4 SIN(0 .05 10MEG 0 0 0)

 *impedance matching network
RA 1 0 120
RB 4 0 120

 *differential input stage
X1 1 2 23 24 5 AD811
X5 4 3 23 24 6 AD811
R1 5 2 100
R8 3 2 50; determines gain of differential stage-set to 5
R17 6 3 100
C2 5 2 16.5pF; equivalent capacitance of C2 and C3
C34 6 3 16.5pF; equivalent capacitance of C34 and C35
```

```
*level shifting circuit
X2 7 9 23 24 14 AD811
X6 8 10 23 24 13 AD811
R6 7 5 220
R13 8 6 220
R5 9 0 220
R15 10 0 220
R2 12 9 220
C4 12 9 5.6pF
R18 11 10 220
C36 11 10 5.6pF
R3 23 12 220
R16 23 11 220
R9 15 7 220
R12 15 8 220
C5 14 12 .1uF
C29 13 11 .1uF
D1 12 14 D1N4148; equivalent of BAS32
D2 11 13 D1N4148; equivalent of BAS32
C10 21 0 22pF
C23 22 0 22pF
R4 21 12 56
R14 22 11 56

*buffer
X3 19 17 23 0 18 OPA130
R11 18 15 150
R10 17 15 2.7k
R7 20 19 2.7k
C16 18 17 100nF
```

```
C11 20 0 100nF
V3 20 0 DC 2.25V; reference voltage from ADC

.OPTIONS RELTOL=.01 VNTOL=.01V ABSTOL=10NA
.tran   10m   12m   0   .001m ; *ipsp*
.end
```

****

***Pspice* program for figure 3.14**

```
***integrated implementation of the analog signal conditioning subsystem
 **0.1V, A.C. input

 *libraries
.lib d:\pfiles\lib\AD811b.lib
.lib d:\pfiles\lid\OPA130.lib
.lib d:\pspice5\lib\DIODE.lib

 *voltage sources
Vcc 23 0 +5V
Vss 24 0 -5V

 *input signals
Vdiff1 1 25 AC .05
Vdiff2 25 4 AC .05
Vcm 25 0 DC 0

 *impedance matching network
RA 1 0 120
RB 4 0 120
 *differential input stage
```

```
X1 1 2 23 24 5 AD811
X5 4 3 23 24 6 AD811
R1 5 2 100
R8 3 2 50; determines gain of differential stage-set to 5
R17 6 3 100
C2 5 2 16.5pF; equivalent capacitance of C2 and C3
C34 6 3 16.5pF; equivalent capacitance of C34 and C35

*level shifting circuit
X2 7 9 23 24 14 AD811
X6 8 10 23 24 13 AD811
R6 7 5 220
R13 8 6 220
R5 9 0 220
R15 10 0 220
R2 12 9 220
C4 12 9 5.6pF
R18 11 10 220
C36 11 10 5.6pF
R3 23 12 220
R16 23 11 220
R9 15 7 220
R12 15 8 220
C5 14 12 .1uF
C29 13 11 .1uF
D1 12 14 D1N4148; equivalent of BAS32
D2 11 13 D1N4148; equivalent of BAS32
C10 21 0 22pF
C23 22 0 22pF
R4 21 12 56
R14 22 11 56
```

```
*buffer
X3 19 17 23 0 18 OPA130
R11 18 15 150
R10 17 15 2.7k
R7 20 19 2.7k
C16 18 17 100nF
C11 20 0 100nF
V3 20 0 DC 2.25V; reference voltage from ADC

.OPTIONS RELTOL=.01 VNTOL=.01V ABSTOL=10NA
.ac dec   101   10   100g ; *ipsp*
.end
```

****

Optimisation of operational amplifiers

Figures 3.9 and 3.10 in Chapter 3 show frequency responses of the circuit (for gains of 1.2) as it appears in figure 3.8 for operational amplifiers U_1, U_2, U_5 and U_6 being HA2840s and AD811s respectively. For simulation purposes, the buffer was omitted and node (15) tied to a 2.25 V, D.C. source.

****

***Pspice* program for figure 3.9 ~~in Chapter 3~~**

```
***integrated implementation of the analog signal conditioning subsystem
 **optimisation of operational amplifiers-HA2840

 *libraries
.lib d:\pfiles\lib\HA2840.lib
.lib d:\pspice5\lib\DIODE.lib

*voltage sources
```

```
Vcc 23 0 +15V
Vss 24 0 -15V

*input signals
Vdiff1 1 25 AC 0.5
Vdiff2 25 4 AC 0.5
Vcm 25 0 DC 0

*impedance matching network
RA 1 0 120
RB 4 0 120

*differential input stage
X1 1 2 23 24 5 HA2840
X5 4 3 23 24 6 HA2840
R1 5 2 100
R8 3 2 1k; determines gain of differential stage-set to 1.2
R17 6 3 100
C2 5 2 16.5pF; equivalent capacitance of C2 and C3
C34 6 3 16.5pF; equivalent capacitance of C34 and C35

*level shifting circuit
X2 7 9 23 24 14 HA2840
X6 8 10 23 24 13 HA2840
R6 7 5 220
R13 8 6 220
R5 9 0 220
R15 10 0 220
R2 12 9 220
C4 12 9 5.6pF
R18 11 10 220
```

```
C36 11 10 5.6pF
R3 23 12 220
R16 23 11 220
R9 15 7 220
R12 15 8 220
C5 14 12 .1uF
C29 13 11 .1uF
D1 12 14 D1N4148; equivalent of BAS32
D2 11 13 D1N4148; equivalent of BAS32
C10 21 0 22pF
C23 22 0 22pF
R4 21 12 56
R14 22 11 56

V3 15 0 DC 2.25V; reference voltage from ADC
.OPTIONS RELTOL=.01 VNTOL=.01V ABSTOL=10NA
.ac dec   101   10   100g ; *ipsp*
.end
```

****

***Pspice* program for figure 3.10**

```
***integrated implementation of the analog signal conditioning subsystem
 **optimisation of operational amplifiers-AD811

 *libraries
.lib d:\pfiles\lib\AD811b.lib
.lib d:\pspice5\lib\DIODE.lib

 *voltage sources
Vcc 23 0 +5V
```

```
Vss 24 0 -5V

*input signals
Vdiff1 1 25 AC .05
Vdiff2 25 4 AC .05
Vcm 25 0 DC 0

*impedance matching network
RA 1 0 120
RB 4 0 120

*differential input stage
X1 1 2 23 24 5 AD811
X5 4 3 23 24 6 AD811
R1 5 2 100
R8 3 2 1k; determines gain of differential stage-set to 1.2
R17 6 3 100
C2 5 2 16.5pF; equivalent capacitance of C2 and C3
C34 6 3 16.5pF; equivalent capacitance of C34 and C35

*level shifting circuit
X2 7 9 23 24 14 AD811
X6 8 10 23 24 13 AD811
R6 7 5 220
R13 8 6 220
R5 9 0 220
R15 10 0 220
R2 12 9 220
C4 12 9 5.6pF
R18 11 10 220
C36 11 10 5.6pF
```

```
R3 23 12 220
R16 23 11 220
R9 15 7 220
R12 15 8 220
C5 14 12 .1uF
C29 13 11 .1uF
D1 12 14 D1N4148; equivalent of BAS32
D2 11 13 D1N4148; equivalent of BAS32
C10 21 0 22pF
C23 22 0 22pF
R4 21 12 56
R14 22 11 56

V3 15 0 DC 2.25V; reference voltage from ADC

.OPTIONS RELTOL=.01 VNTOL=.01V ABSTOL=10NA
.ac dec   101   10   100g ; *ipsp*
.end

**********************************************************************
```

Appendix B

Programming codes for the digital components

This appendix presents the *Maxplus* programs and pin assignments for the FPGA and EPLDs used in the digital signal conditioning subsystem and high speed fibre-optic link. Programmable digital integration, time-domain decimation, range selection and control logic and clock generation circuits are implemented on the FPGA. The chosen FPGA is the EPF10K10LC84-4. Its VHDL program is given with a layout in figure B.1. The EPLDs are used to supply the control logic to the transmitting and receiving modules of the high speed serial fibre-optic link. The chosen EPLDs are the EPM7064SLC44-10. The VHDL program for the transmitting and receiving EPLDs are given with respective layouts in figures B.2 (Txprobe) and B.3 (Rxprobe).

****

***Maxplus* VHDL program for the digital signal conditioning subsystem**

```
-- integration, decimation, selection, control logic, clock generation
library IEEE;
use IEEE.STD_LOGIC_ARITH.all;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;

entity ACCUM is
 port(
 CLK:                in STD_LOGIC;      --40.000 MHz crystal oscillator
 MRESET_IN:          in STD_LOGIC;      --active low, i.e. 0 implies reset
 INHIB_IN:           in STD_LOGIC;      --active high, i.e. 1 implies inhibit
 WORDIN:             in STD_LOGIC_VECTOR(11 downto 0);   --from ADC
 WORDOUT:            buffer STD_LOGIC_VECTOR(11 downto 0);       --to link
 MCLK_OUT            out STD_LOGIC;     --decimated version of CLK
 DATARDY:            out STD_LOGIC;     --to synchronise link with FPGA
 ADCLK:              buffer STD_LOGIC;  --sampling clock of ADC
 DIPSWA:             in STD_LOGIC_VECTOR(7 downto 0);
 DIPSWB:             in STD_LOGIC_VECTOR(7 downto 0);
--      pins reserved for future use
 A:                  in BIT;
 B:                  in BIT;
 C:                  in BIT);
 end ACCUM;

architecture A of ACCUM is

 signal MCLK_IN:          STD_LOGIC; --signal line for CLK
 signal MCLK:             STD_LOGIC; --signal line for MASTER CLOCK
```

```
 signal MRESET:              STD_LOGIC; --signal line for MRESET_IN
 signal INH:                 STD_LOGIC; --signal line for INHIB_IN
 signal INH_SYNCD:           STD_LOGIC;
 signal SUM_LATCHED:         STD_LOGIC_VECTOR(31 downto 0);--signal line
--                                                    for fed-back sum
 signal WORDIN_LATCHED:      STD_LOGIC_VECTOR(11 downto 0);--signal line
 --                                                   for latched input
 signal MSB_DUPLIC:          STD_LOGIC_VECTOR(19 downto 0);
 signal SUM:                 STD_LOGIC_VECTOR(31 downto 0);
 signal CNT1:                STD_LOGIC_VECTOR(3 downto 0);      --signal
--                                  for counter for decimation clock generator
 signal CNTCLK:              STD_LOGIC_VECTOR(3 downto 0);      --signal
--                                    for counter for sampling clock generator
 signal WORDOUT_CLK:         STD_LOGIC;
 signal WORDOUT_SRC:         STD_LOGIC_VECTOR(11 downto 0);
 signal WORDOUT_SRCSLCT:     STD_LOGIC_VECTOR(4 downto 0);
 signal WORDTEST:            STD_LOGIC_VECTOR(11 downto 0);

begin

 --      MCLK_IN
 MCLK_IN <= CLK when ( INH_SYNCD = '0' ) else '0';    --when operation of FPGA
--is not inhibited the CLK is 40 MHz.  When operation of FPGA is inhibited CLK is '0'

 --      MRESET
 MRESET <= '1' when ( MRESET_IN = '0' ) else '0';        --operation of FPGA is reset
--                  when MRESET_IN is '0'; during normal operation MRESET_IN is '1'

 --      INH
 INH <= INHIB_IN;   --operation of FPGA is stopped when INHIB_IN is '1'; during
--                                                  normal operation INHIB_IN is '0'
```

```
--      INH_SYNCD
process ( CLK, MRESET_IN )
begin
        if ( MRESET = '1' ) then        --if FPGA is reset then
                INH_SYNCD <= '0';  --operation of FPGA can not be inhibited
        elsif ( CLK'EVENT and CLK = '0' ) then
                INH_SYNCD <= INH
        end if;
end process;

--      generation of master clock, which is also the ADC sampling clock
--              CNTCLK, counter used for the generation of sampling clock
process ( MCLK_IN, MRESET )
begin
        if ( MRESET = '1' ) then        --if FPGA is reset then
                CNTCLK <= "1111"; --counter gets '1111'
        elsif ( MCLK_IN'EVENT and MCLK_IN = '1' ) then--if FPGA not reset then on
        --                                                      first rising edge of CLK
                if ( CNTCLK = DIPSWA(7 downto 4) ) then--if dipswitch has been set
                --                                                      then
                        CNTCLK <= "0001"; --counter gets '0001'
                else
                        CNTCLK <= CNTCLK + 1;  --if counter already counting, it
                        --increments by 1 on each rising edge of CLK til it reaches a
                        --maximum and starts again from 1
                end if;
        end if;
end process;

process ( MCLK_IN, DIPSWA )
begin
```

```
        if ( DIPSWA(7 downto 4) = "0000" ) then--if dipswitch has been set to '0000'then
                MCLK <= MCLK_IN;          --MCLK=CLK
        elsif ( MCLK_IN'EVENT and MCLK_IN = '1' ) then--if dipswitch set to any
        --other value but '0000'then on first rising edge of CLK
                if ( CNTCLK = "0001" ) then -- if counter is '0001'then
                        MCLK <= ( not MCLK );      --MCLK is inverted.
                else
                        MCLK <= MCLK;--for other values of counter master clock stays
                        --                          in its last state
                end if;
        end if;
end process;

--      AD_CLK
ADCLK <= MCLK;  --the ADC sampling clock follows MCLK

--      SUM_LATCHED
--      WORDIN_LATCHED
process ( MCLK, MRESET )
begin
        if ( MRESET = '1' ) then        --if FPGA has been reset
                SUM_LATCHED <= "00000000000000000000000000000000";--fed back
                --                                                  sum set to zero
                WORDIN_LATCHED <= "000000000000";--and latched input set to zero
        elsif (MCLK'EVENT and MCLK = '1') then --if FPGA not reset then on the first
        --                                          rising edge of MCLK
                SUM_LATCHED <= SUM;  --fed-back sum gets new sum and
                WORDIN_LATCHED <= ( (not WORDTEST(11)) & WORDTEST(10
                downto 0) );--conversion 12-bit BTC to 12-bit BTC by inverting MSB
        end if;
end process;
```

```
--      12-bit BTC to 32-bit BTC converter
--      MSB_DUPLIC, sign-extension
MSB_DUPLIC <= "00000000000000000000" when ( WORDIN_LATCHED(11) = '0' )
        else "11111111111111111111";--padding of 12-bit BTC word into 32-bit BTC
        --                              word by duplication of MSB inverted.

SUM <= SUM_LATCHED + ( MSB_DUPLIC & WORDIN_LATCHED );--new sum is
--                              fed-back sum + WORDIN-LATCHED padded into 32-
--                              bit BTC

--      WORDTEST
WORDTEST <= WORDIN;
-- WORDTEST <= "100000000001"; --      a test word is used to test the integrator and
                                                        --      the link

--      generation of programmable time-domain decimation clock
--      CNT1, counter used for generation of decimation clock
process ( MCLK, MRESET )
begin
        if (MRESET = '1' ) then --if FPGA is reset
                CNT1 <= "1111";--counter gets '1111'
        elsif ( MCLK'EVENT and MCLK = '1' ) then--if FPGA not reset then on the
        --                                      first detected rising edge of MCLK
                if ( CNT1 = DIPSWA(3 downto 0) ) then--if dipswitch has been set
                        CNT1 <= "0000";--counter set to '0000'
                else
                        CNT1 <= CNT1 + 1;--if counter already counting it increments by
                        --1 on each rising edge of MCLK til it reaches a maximum and
                        --starts again from 0
                end if;
        end if;
```

```
end process;

--      WORDOUT_CLK
WORDOUT_CLK <= '1' when ( CNT1 = "0000" and MCLK = '0' ) else '0';--when
--      counter is '0000' on next falling edge of MCLK WORDOUT_CLK gets '1'

--      range selector, selects 12 bits
--              WORDOUT_SRCSLCT
WORDOUT_SRCSLCT <= DIPSWB(4 downto 0);--operated by DIPSWB(0..4)

--              WORDOUT_SRC
with WORDOUT_SRCSLCT select
WORDOUT_SRC <= SUM_LATCHED(11 downto 0) when "00000",--when dipswitch
--                                              set to '000' choose sum-latched(11..0)
        SUM_LATCHED(12 downto 1) when "00001",--and so forth
        SUM_LATCHED(13 downto 2) when "00010",
        SUM_LATCHED(14 downto 3) when "00011",
        SUM_LATCHED(15 downto 4) when "00100",
        SUM_LATCHED(16 downto 5) when "00101",
        SUM_LATCHED(17 downto 6) when "00110",
        SUM_LATCHED(18 downto 7) when "00111",
        SUM_LATCHED(19 downto 8) when "01000",
        SUM_LATCHED(20 downto 9) when "01001",
        SUM_LATCHED(21 downto 10) when "01010",
        SUM_LATCHED(22 downto 11) when "01011",
        SUM_LATCHED(23 downto 12) when "01100",
        SUM_LATCHED(24 downto 13) when "01101",
        SUM_LATCHED(25 downto 14) when "01110",
        SUM_LATCHED(26 downto 15) when "01111",
        SUM_LATCHED(27 downto 16) when "10000",
        SUM_LATCHED(28 downto 17) when "10001",
```

```
                SUM_LATCHED(29 downto 18) when "10010",
                SUM_LATCHED(30 downto 19) when "10011",
                SUM_LATCHED(31 downto 20) when others;

--      transferring data to output pins
--      WORDOUT
process ( WORDOUT_CLK, MRESET )
begin
        if ( MRESET = '1' ) then--if operation of FPGA is reset then
                WORDOUT <= "000000000000";--WORDOUT is zero
        elsif ( WORDOUT_CLK'EVENT and WORDOUT_CLK = '1' ) then--if FPGA not
        --reset then on the first detected rising edge of WORDOUT_CLK
                WORDOUT <= WORDOUT_SRC;--WORDOUT gets word chosen by
                --                                                  range selector
                else
                        null;
        end if;
end process;

DATARDY <= WOROUT_CLK;--DATARDY follows WORDOUT_CLK to indicate to
--                                              link that new data is being transferred
MCLK_OUT <= MCLK;--clock at output is MCLK
end A;
```

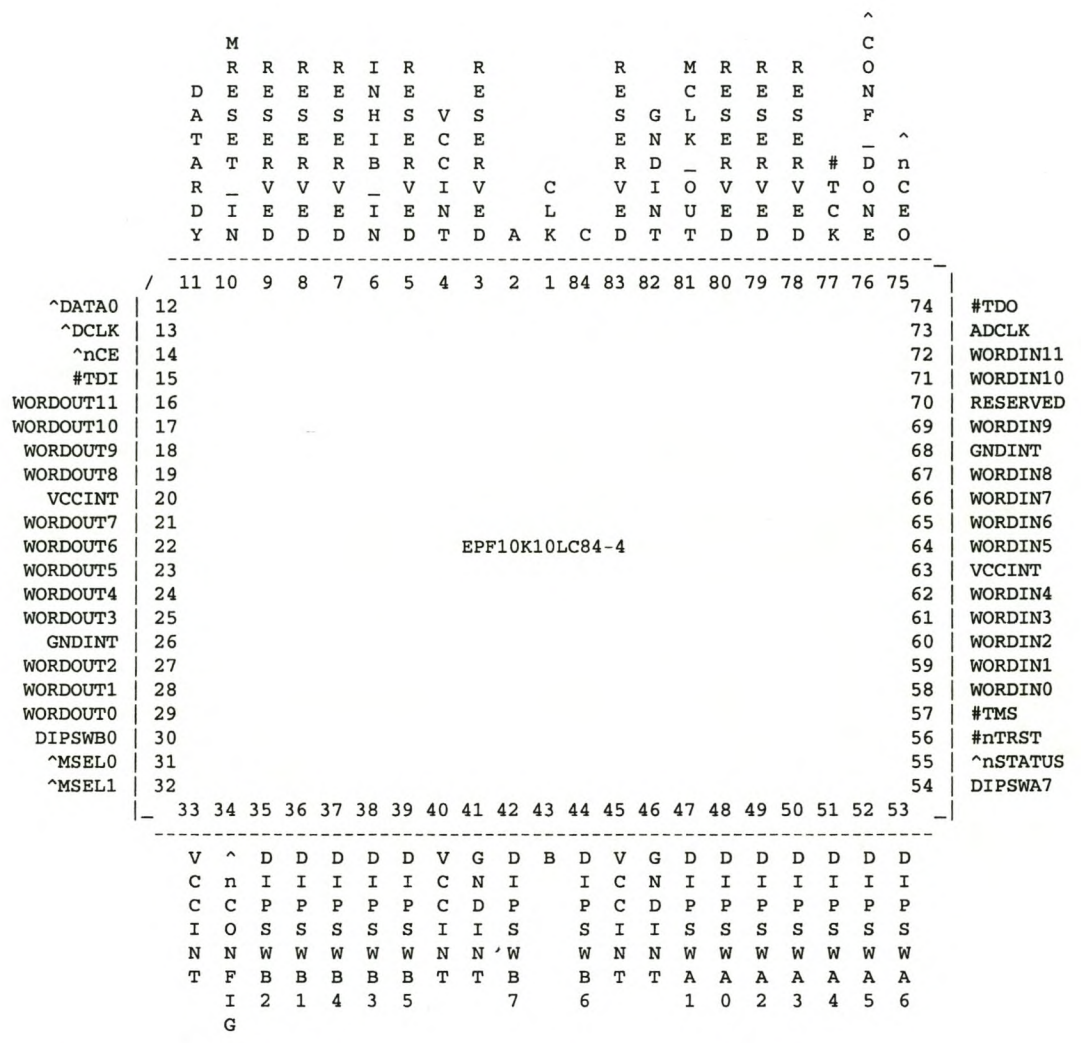

Fig. B.1: EPF10K10LC84-4 FPGA with pin assignments.

****

***Maxplus* VHDL program of control logic CY7B923 transmitter of high-speed serial link**

```
-- control logic for CY7B923 HOTLink transmitter
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity TXPROBE is
 port(
 CLK:            in STD_LOGIC;       --25.175MHz crystal oscillator
 TESTIN:         in STD_LOGIC;       --test pin, active high; 1 implies test mode
 --      integrator data bits and control line
 DATAIN:         in STD_LOGIC_VECTOR(11 downto 0);
 DATARDY:        in STD_LOGIC;
 --      CY7B923 control lines
 RESET:          in STD_LOGIC;       --active low; 0 implies reset
 DATAOUT:        out STD_LOGIC_VECTOR(7 downto 0);  --to  transmitter  link
SC_D:            out STD_LOGIC := '1';--special character/data line
 BISTEN:         out STD_LOGIC;      --built-in self test, active low
 ENA:            out STD_LOGIC := '1';--used for data transmission active low
 ENN:            out STD_LOGIC := '1';       --active low
 SVS:            out STD_LOGIC;      --used to detect violation symbol
 --      pins reserved for future use
 A:              in STD_LOGIC;
 B:              in STD_LOGIC;
 C:              in STD_LOGIC);
 end TXPROBE;

architecture BEHAVIOUR of TXPROBE is
```

```
signal COUNTER1:        internally generated counter INTEGER range 3 downto 0;
signal BUFFER1:         STD_LOGIC_VECTOR(11 downto 0);--signal line for
--                                                          DATAIN
signal FLAG:            STD_LOGIC; -- used so that when data is not be received
--                              from FPGA fast enough the counter doesn't restart

begin

process ( DATARDY, COUNTER1 )
begin
    if COUNTER1 = 3 then        --if counter is '0011' then
        FLAG <= '0';  --FLAG gets '0'; counter only begins to count again when
        --                      FLAG is '1'
    elsif DATARDY'EVENT and DATARDY = '0' then--if counter is not '0011'and
    --                                                  DATARDY is '0'
        BUFFER1 <= DATAIN;      --BUFFER1 latches DATAIN
        FLAG <= '1';  --and FLAG gets '1'
    end if;
end process;

process ( CLK )
begin
    if RESET = '0' then    --if EPLD is reset then
        COUNTER1 <= 0;     --counter gets '0000'
        elsif CLK'EVENT and CLK = '1' then--if EPLD not reset then on first
        --                              detected rising edge of CLK
        if FLAG = '1' then      --if FLAG is '1'
            COUNTER1 <= COUNTER1 + 1;--counter increments by 1
        else
            COUNTER1 <= 0;--if FLAG is '0' then counter is '0000'
        end if;
```

```
        end if;
end process;

--      define normal and test modes
process ( CLK, TESTIN )
begin
        if RESET = '0'then;    if EPLD is reset then
                BISTEN <= '1';          --built-in-self-test is inactivated
        elsif TESTIN = '1'then          --if EPLD not reset and TESTIN is '1'then
                BISTEN <= '0';          --BISTEN is activated
        elsif CLK'EVENT and CLK = '1' then      --if EPLD not reset and TESTIN is
        --                                      '0' then on rising edge of CLK
                BISTEN <= '1';          --BISTEN is inactivated
        end if;
end process;

process ( CLK, TESTIN, RESET )
begin
        if RESET = '0' then     --if EPLD is reset
                ENN <= '1';     --ENN is '1'
                ENA <= '1';     --ENA is '1'
                SC_D <= '1';    --and SC_D is '1' implies sync-bits are being transmitted
        elsif CLK'EVENT and CLK = '1' then--if EPLD not reset then the first rising
        --                                      edge of CLK
                if TESTIN = '1' then    --if TESTIN is activated
                        ENN <= '1';--system goes into test mode sending alternating 1's and
                        --              0's
                        ENA <= '1';
                else
                        ENN <= '1';     --if TESTIN is deactivated
                        if COUNTER1 = 1 then        --and if counter is '0001' then
```

```
                    ENA <= '0';    --ENA gets '0'
                    SC_D <= '0';   --and SC_D gets '0';implies data being sent
                elsif COUNTER1 = 3 then    --and if counter is '0011'then
                    ENA <= '1';    --ENA gets '1'
                    SC_D <= '1';   --and SC_D gets '1';implies sync-bit being
                    --                      sent
                end if;
            end if;
        end if;
end process;

--      data output
process ( CLK )
begin
        if CLK'EVENT and CLK = '1' then   --if a positive clock edge is detected then
            if COUNTER1 = 1 then          --if counter is '0001' then
                DATAOUT(7 downto 0) <= BUFFER1(11 downto 4);      --data in
                --                                                buffer is sent out
            elsif COUNTER1 = 2 then       --if counter is '0010' then
                DATAOUT(7 downto 0) <= BUFFER1(3 downto 0) & "0000";--
                --                  data in buffer is padded with zeros and sent out
                else
                    DATAOUT <= "00000101"; --if counter is any other value
                    --                                            sync-bit sent out
            end if;
        end if;
end process;

SVS <= '0'; -- INACTIVE
end BEHAVIOUR;
**************************************************************************
```

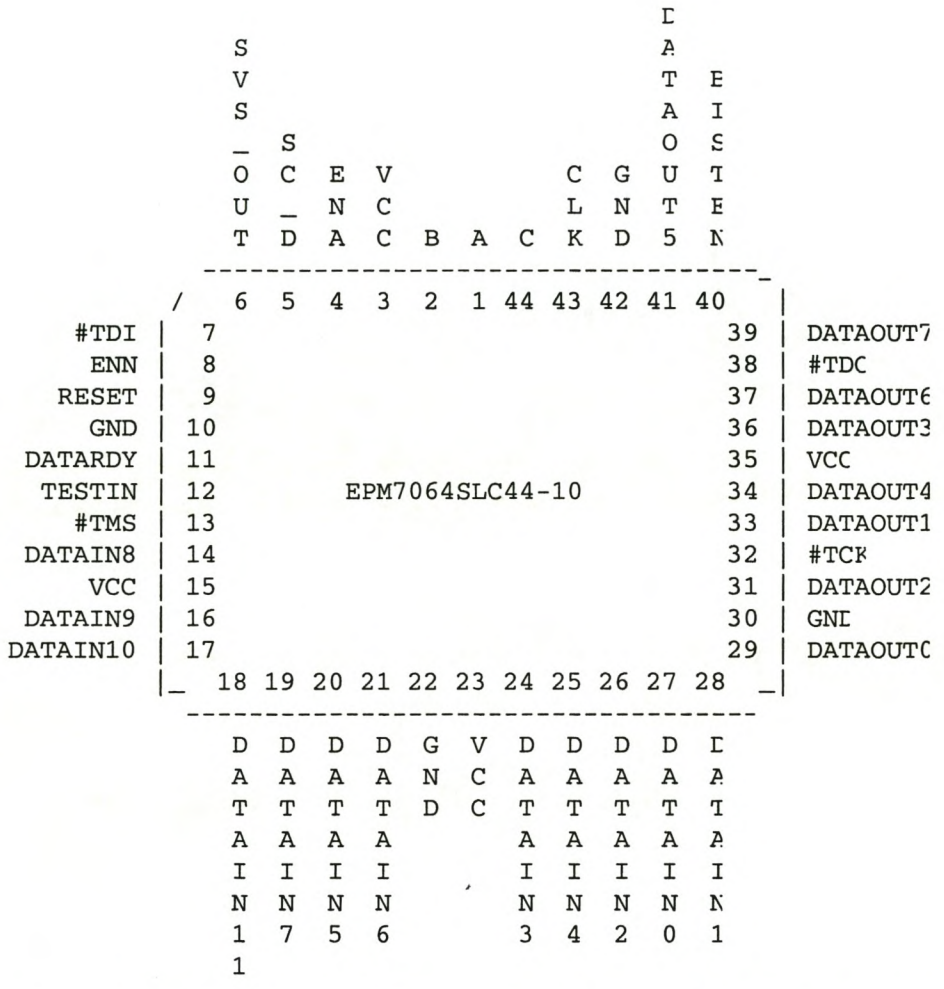

Fig. B.2: EPM706SLC44-10 EPLD with pin assignments for CY7B923 transmitter.

```
**************************************************************************
```

***Maxplus* VHDL program of control logic CY7B933 receiver of high-speed serial link**

```
-- control logic for CY7B933 HOTLink receiver
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity RXPROBE is
 port(
 DATAIN:          in STD_LOGIC_VECTOR(7 downto 0);--from transmitter
 DATAOUT:         out STD_LOGIC_VECTOR(11 downto 0);--to DAC
 BISTEN:          out STD_LOGIC;--built-in-self-test active low
 RF:              out STD_LOGIC;--re-frame enable,not used in system
 RDY              in STD_LOGIC;
 SC_D:            in STD_LOGIC;
 CKR:             in STD_LOGIC;
 RVS:             in STD_LOGIC;
 FAULT:           out STD_LOGIC;
 RESET:           in STD_LOGIC;
 A:               in STD_LOGIC;
 B:               in STD_LOGIC;
 C:               in STD_LOGIC;
 D:               in STD_LOGIC);
end RXPROBE;

architecture BEHAVIOUR of RXPROBE is
 signal COUNTER:          INTEGER range 1 downto 0;--internally generated
--                                                          counter
 signal FIRST_BYTE:       STD_LOGIC_VECTOR(7 downto 0);--buffer
--                                                          holding DATAIN
```

```
begin

process ( CKR, RESET )
begin
        if RESET = '1' then     if EPLD is reset then
                COUNTER <= 0;       counter gets '0'
        elsif CKR'EVENT and CKR = '0' then--if EPLD not reset then on first falling edge
        --                                          of CKR
                if SC_D = '0' then      if SC_D is low then
                        if COUNTER = 0 then         --if counter is '0'then
                                FIRST_BYTE(7 downto 0) <= DATAIN(7 downto 0);--
                                --                              buffer latches DATAIN
                                COUNTER <= 1;       and counter gets '1'
                        else
                                DATAOUT(11 downto 0) <= FIRST_BYTE & DATAIN(7
                                downto 4);      --if counter is '1'DATAOUT gets buffer
                                --      DATAIN(7..0); ignores extra zeros sent
                                COUNTER <= 0;       and counter gets '0'
                        end if;
                end if;
        end if;
end process;

process ( RVS,CKR )
begin
        if RESET = '1' then     if EPLD reset then
                FAULT <= '1';           fault gets '1' i.e. LED is OFF
        esif CKR'EVENT and CKR = '0' then--if not reset then on first falling edge of
        --                                          CKR
                if SC_D = '0' then      --if SC_D is '0'then
                        if RVS = '1' then       --if RVS is '1' i.e. violation received
```

```
                    FAULT <= '0';          --LED is on implying fault.
                end if;
            end if;
        end if;
    end process;

    BISTEN <= '1';--inactive
    RF <= '1';--active continuously; used to reframe the data

    end BEHAVIOUR;
```

****

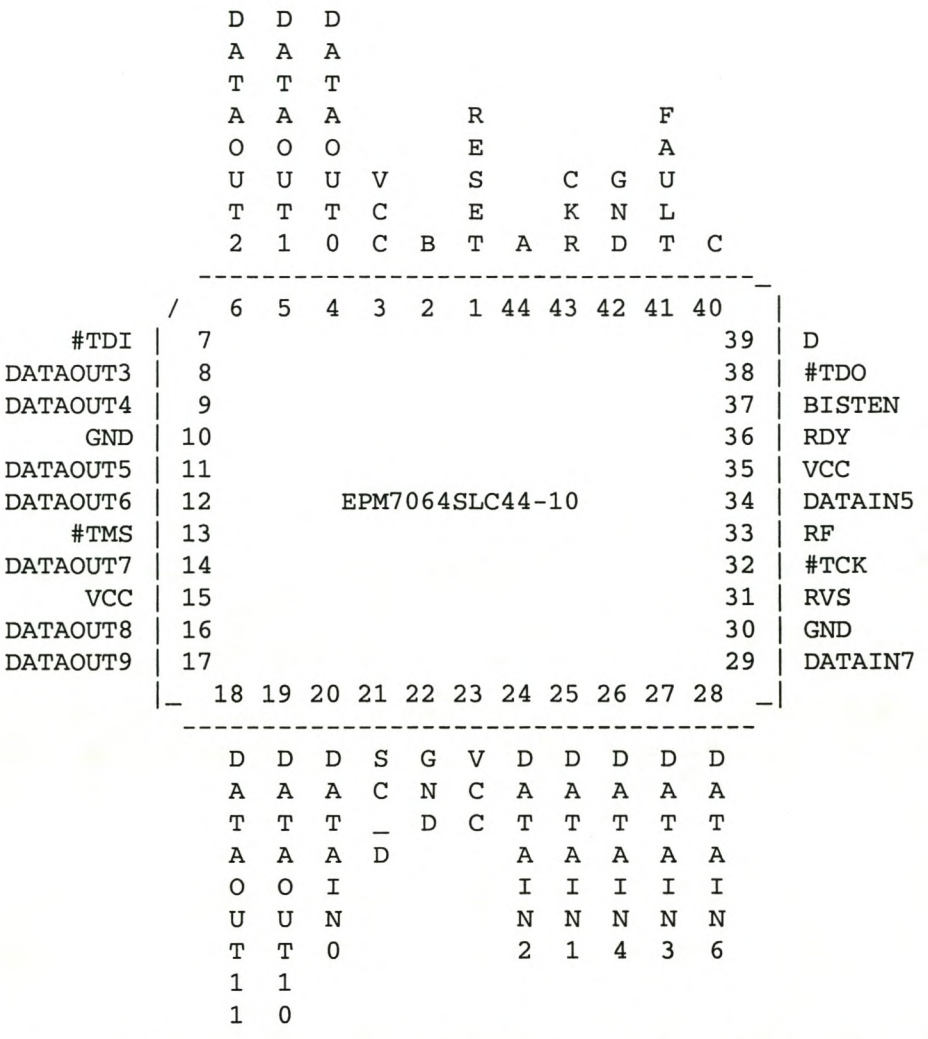

Fig. B.3: ***EPM706SLC44-10 EPLD with pin assignments for CY7B933 receiver.***

Appendix C

Implementation of the programmable wideband signal conditioning system

This appendix presents the circuit diagrams and p.c. board layout for the implementation of the developed system. The analog signal conditioning subsystem, digital signal conditioning subsystem and the transmitter of the high-speed serial link are built on one p.c. board (txprobe) and the receiving module of the high-speed serial link and the DAC are on another p.c. board (rxprobe). Both txprobe and rxprobe are two-layer boards.

Figure C.1 gives a schematic representation of the top level diagram of txprobe. Figure C.2 gives a schematic representation of the analog signal conditioning subsystem. Figure C.3 shows the schematic representation of the ADC. Figures C.4 and C.5 give schematic representations of the digital conditioning subsystem and transmitting module of the fibre-optic link. For prototyping purposes, there are three different ways implemented on the board by which to program the FPGA, viz. EPROM, EEPROM and JTAG. The p.c. board layout of txprobe is given in figure C.6.

Figure C.7 gives a schematic representation of receiving module of the fibre-optic link. Figure C.8 shows the control logic of the receiver and the DAC. The voltage regulator is given in figure C.9. The p.c. board layout of rxprobe is given in figure C.10

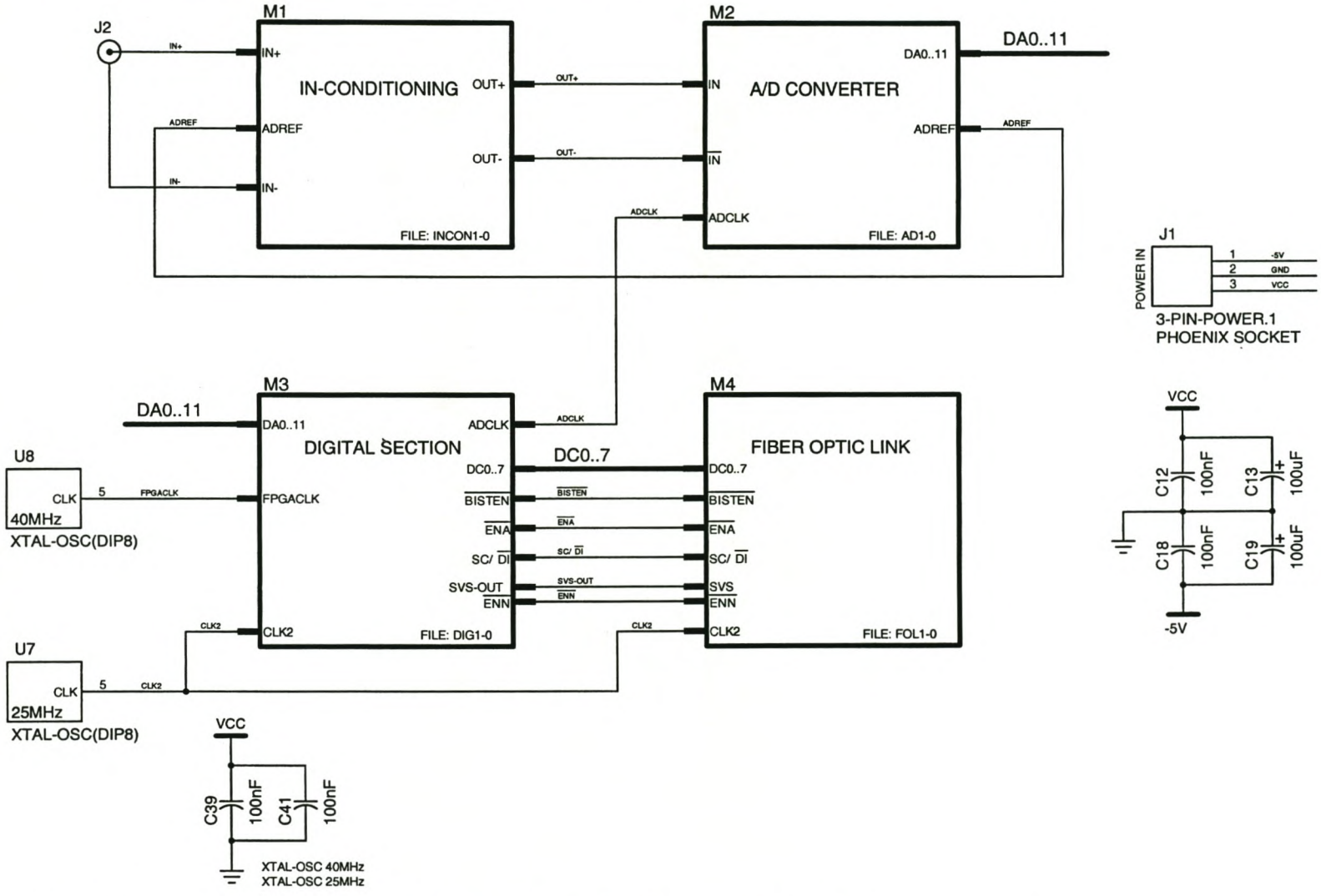

Fig. C.1: ***Schematic representation of the top level diagram of txprobe.***

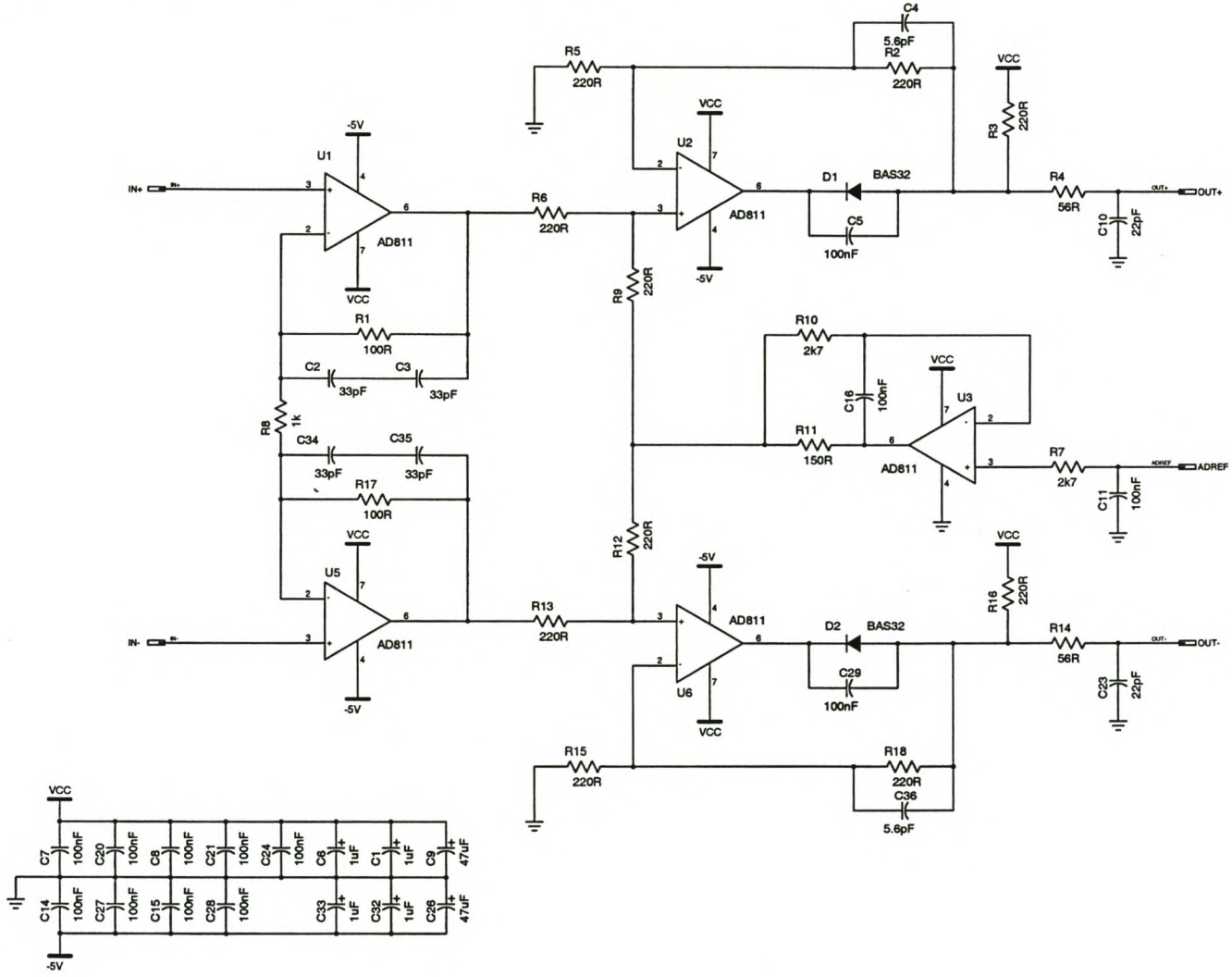

Fig. C.2: ***Schematic representation of the analog signal conditioning subsystem of txprobe.***

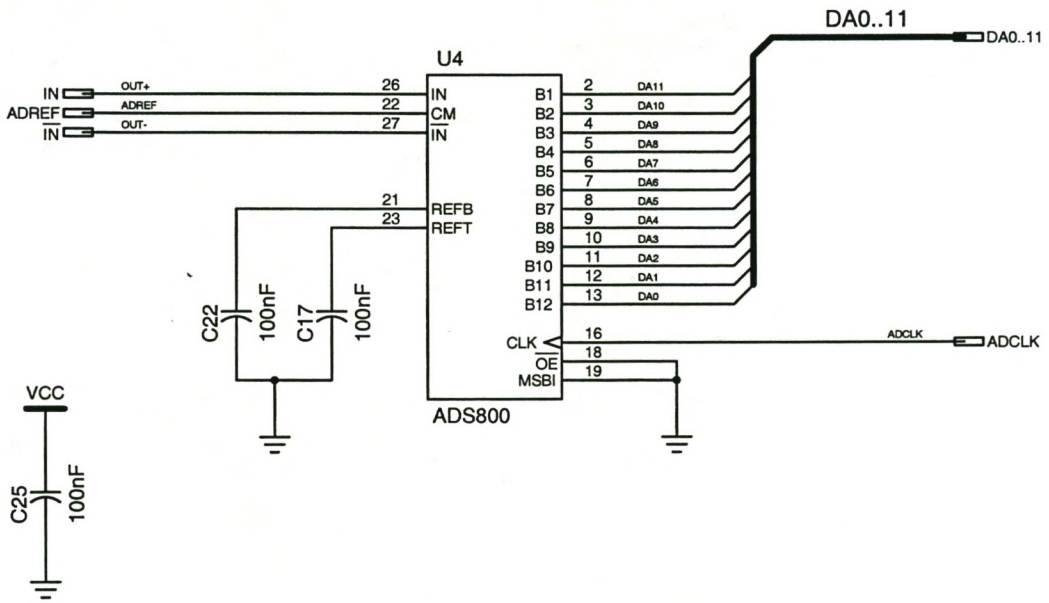

Fig. C.3: ***Schematic representation of the analog to digital converter of txprobe.***

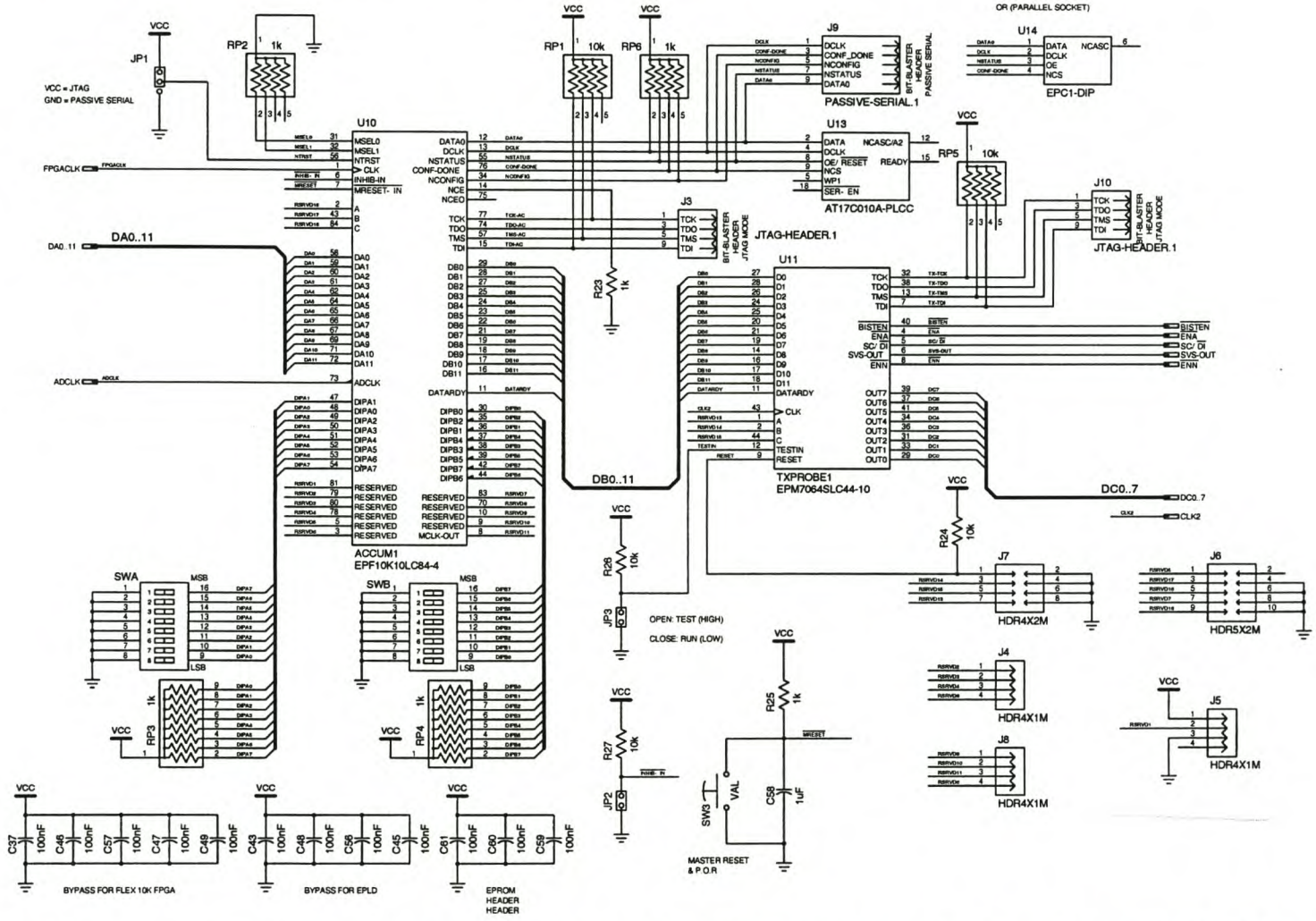

Fig. C.4: ***Schematic representations of the digital signal conditioning subsystem and control EPLD for the high-speed serial link of txprobe***

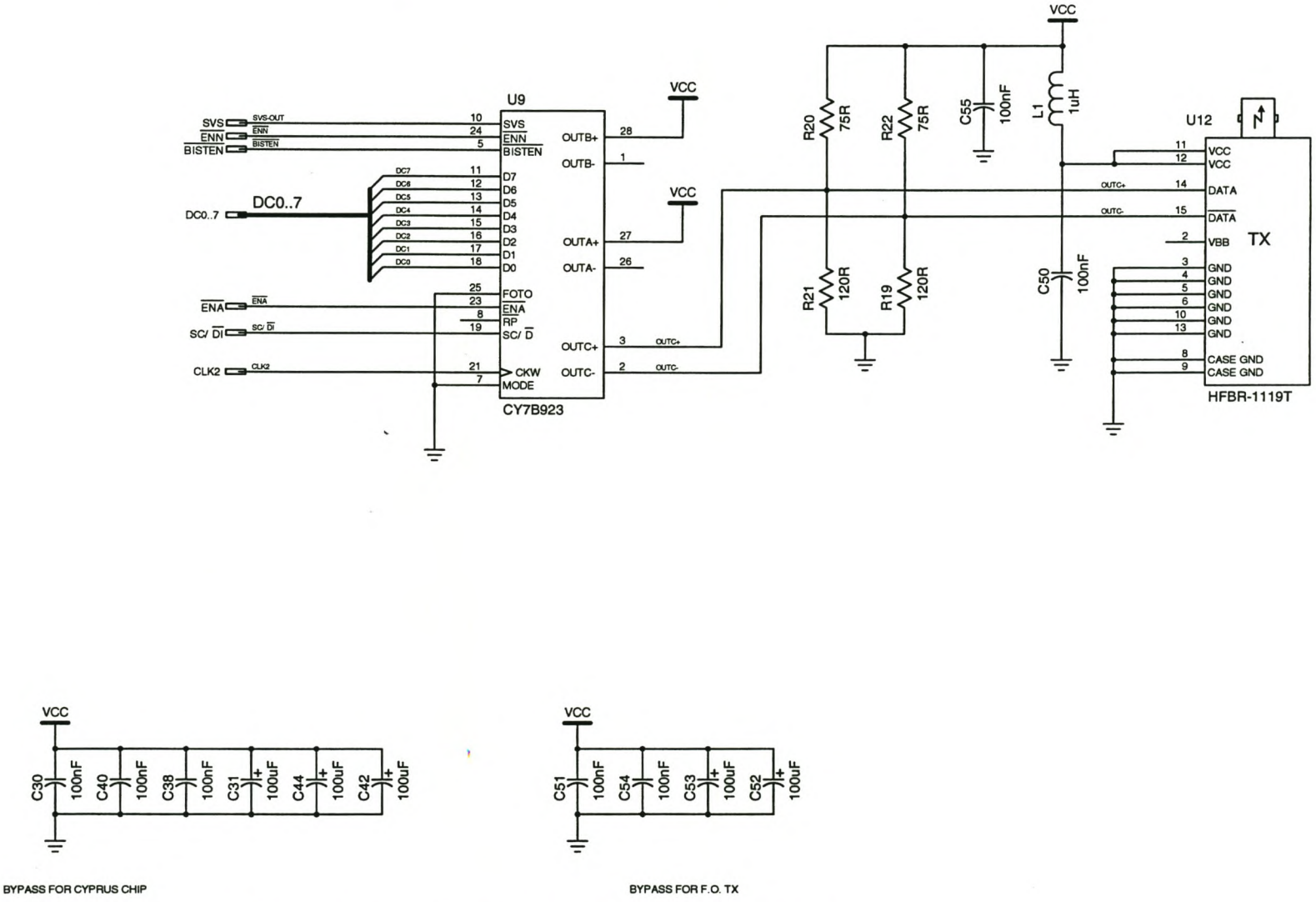

Fig. C.5: Schematic representation of the high-speed serial link of txprobe.

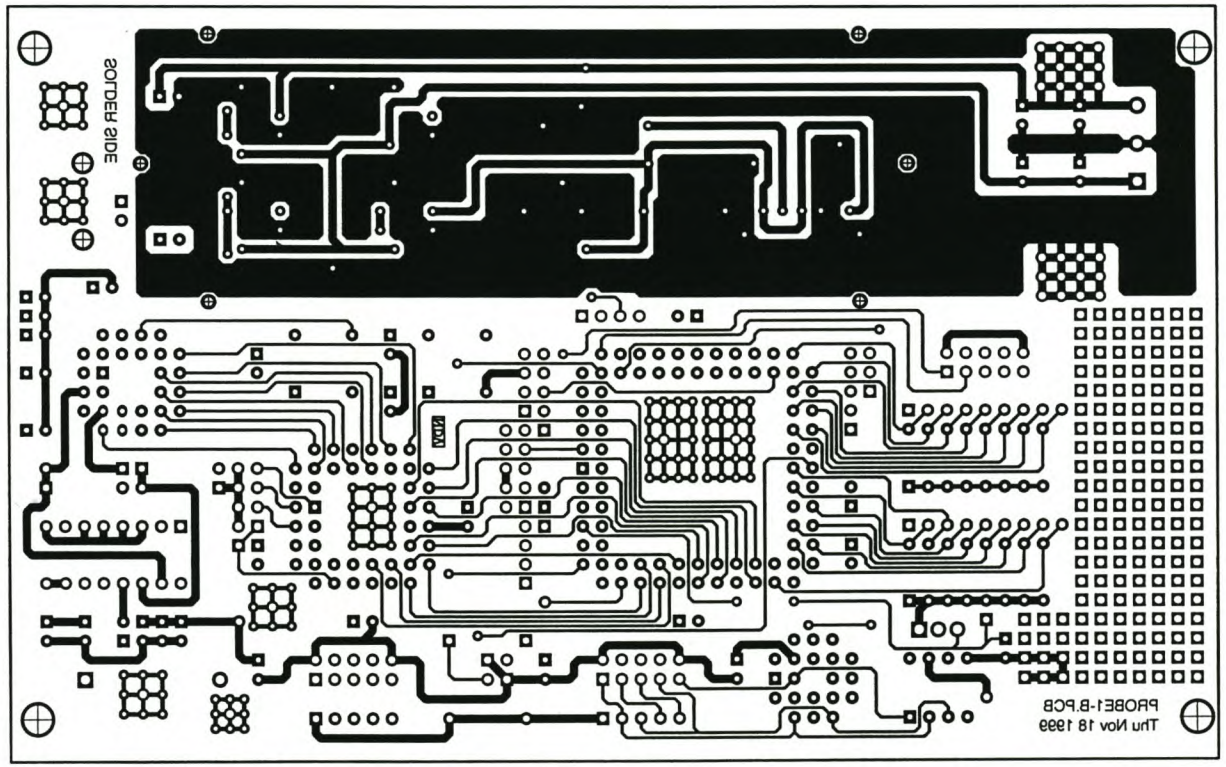

Fig. C.6: Schematic representation of the printed circuit board of txprobe.

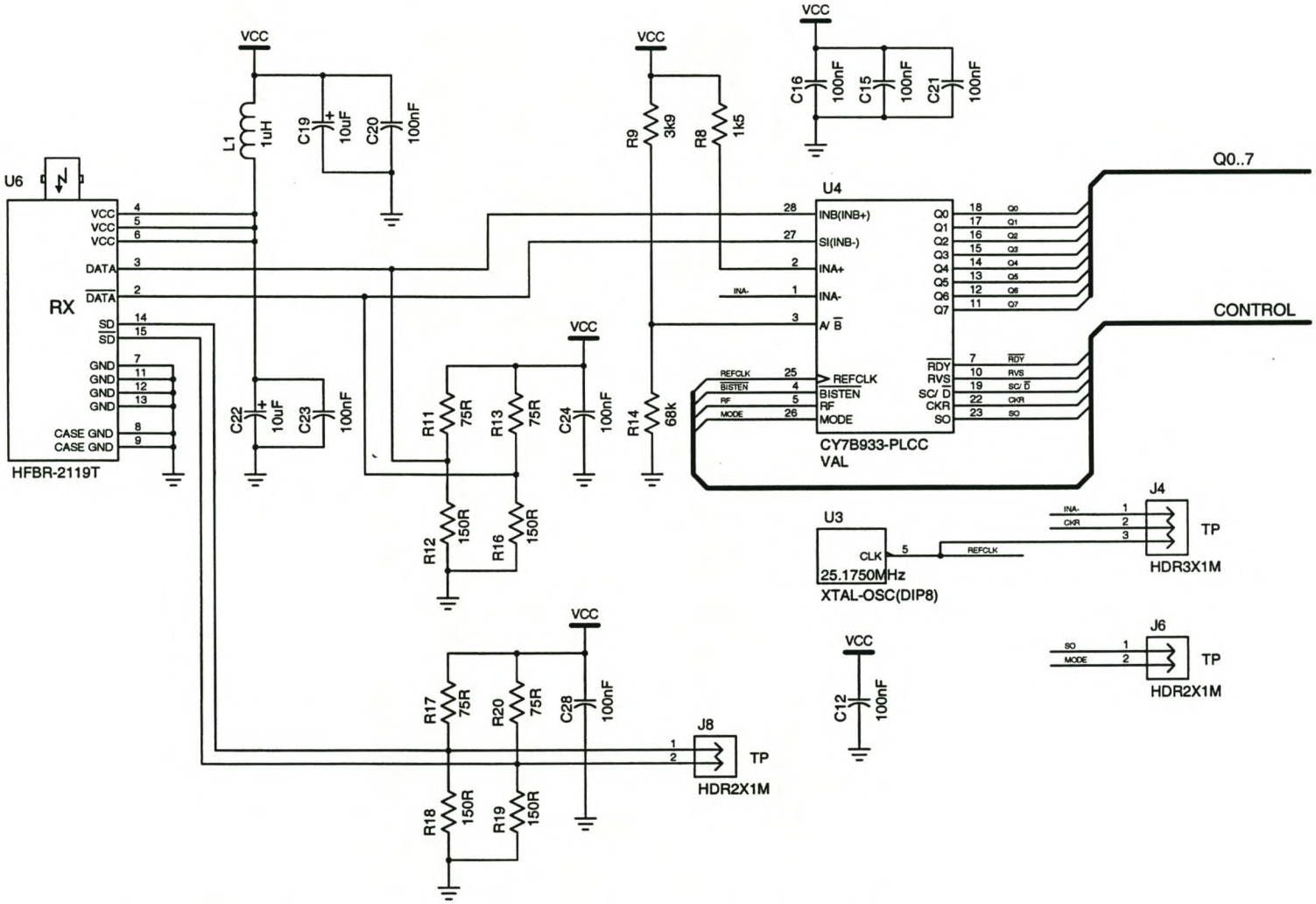

Fig. C.7: Schematic representation of the receiving module of rxprobe.

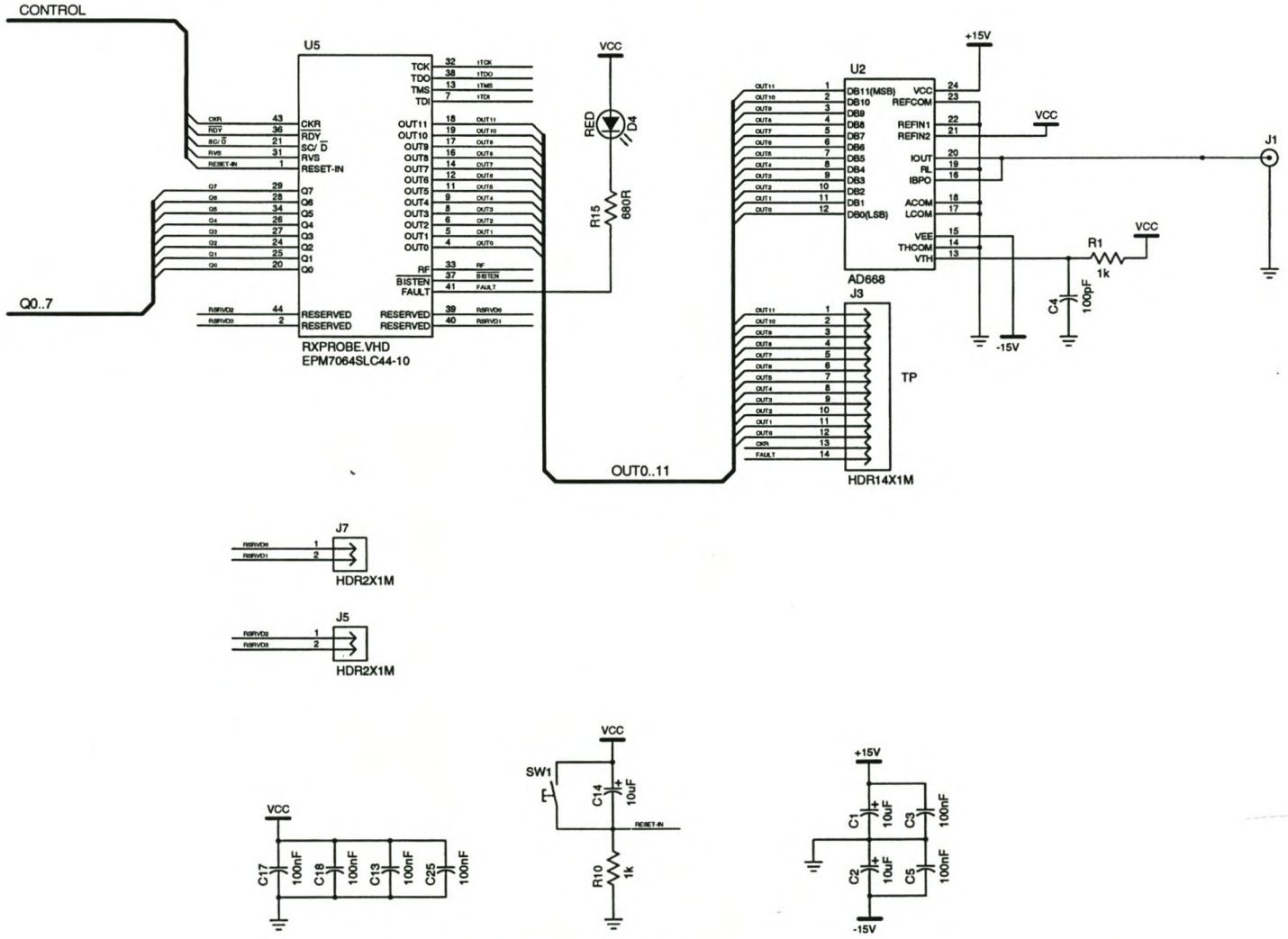

Fig. C.8: Schematic representation of the control logic and digital to analog converter of rxprobe.

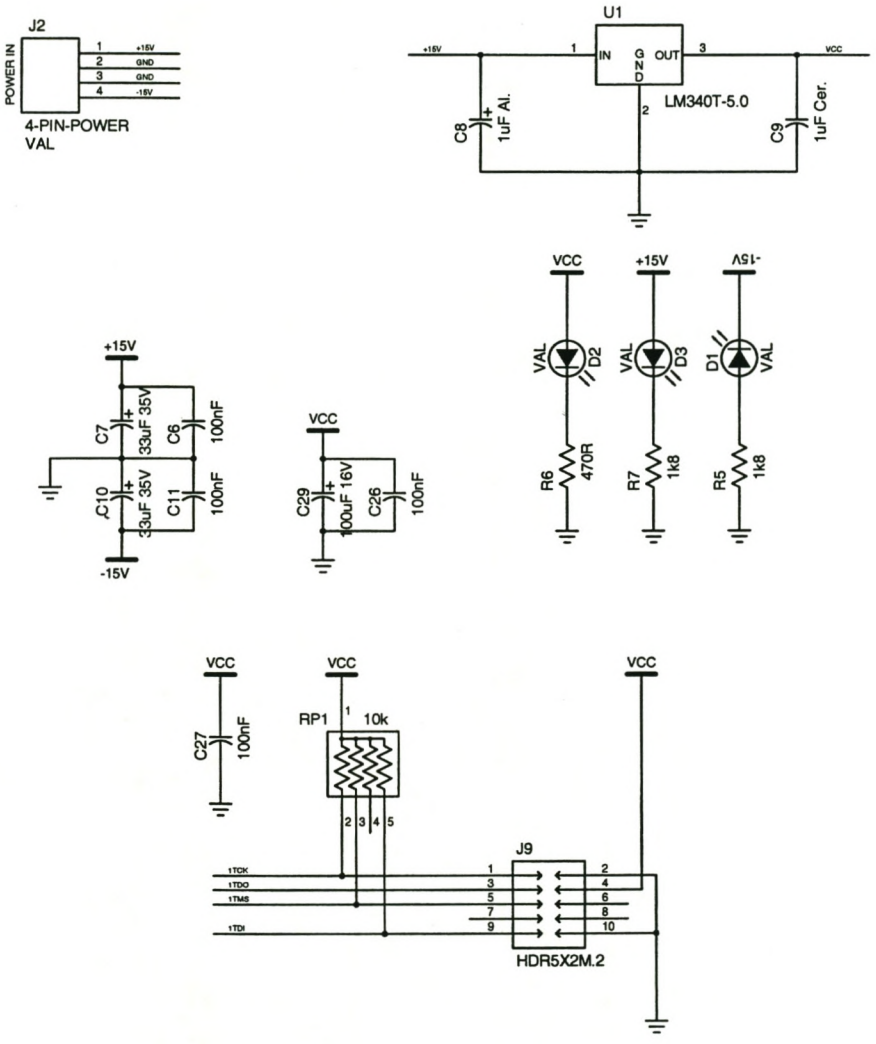

Fig. C.9: Schematic representation of the voltage regulator of txprobe.

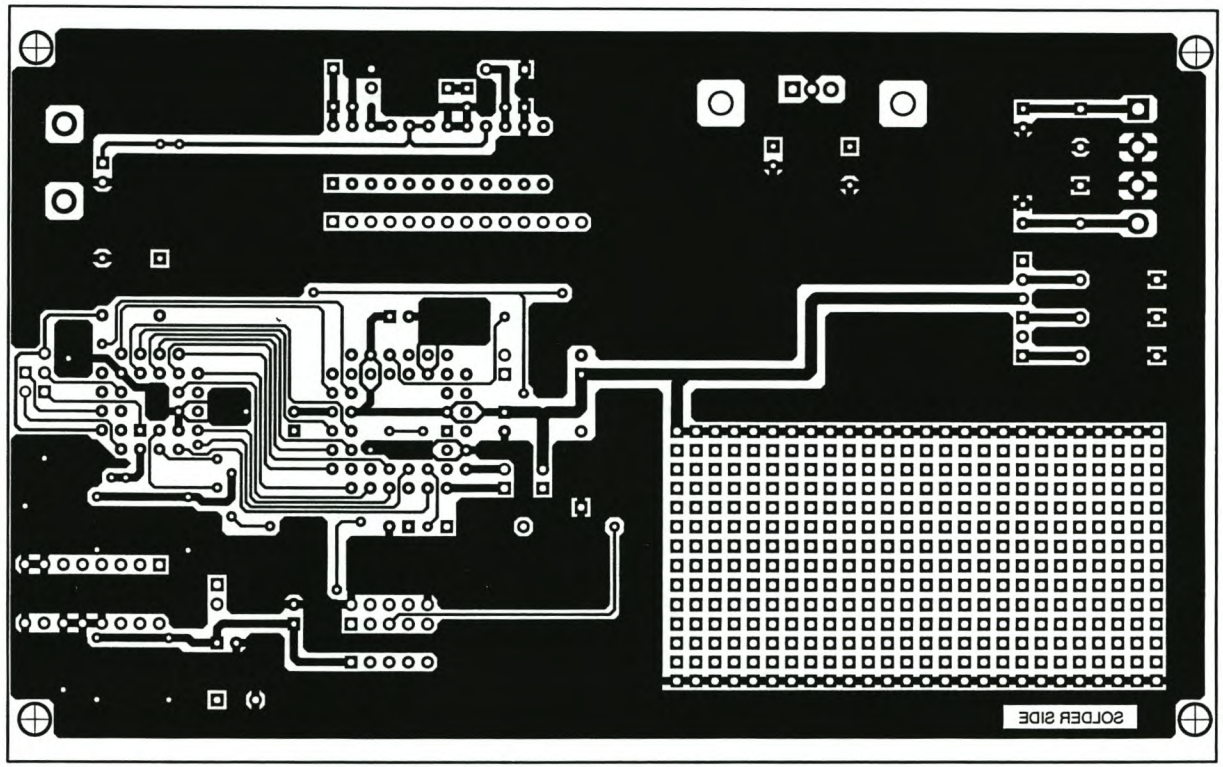

Fig. C.10: Schematic representation of the printed circuit board of rxprobe.