Implementation Oriented Two-Sample Phase Locked Loop for Single-Phase PFCs

ABSTRACT

A low-resource-consuming digital implementation of the Two-Sample (2S) Phase Locked Loop (PLL) for low cost single-phase Power Factor Correction (PFC) converters is proposed. The design replaces trigonometric functions with an oscillator and divisions with approximations, without reducing the 2S-PLL synchronization capability. The proposal is evaluated and validated by simulation and experimentally.

1 INTRODUCTION

Low-cost Power Factor Correction (PFC) stages require simple and effective controllers to achieve the cost and performance targets [1], [2]. The 2S-PLL, proposed in [3], provides synchronization to the electrical grid while keeping relatively low the associated computational burden. However, the characteristics of the quadrature signal generator (QSG) in the 2S PLL make it difficult to use with low sampling rates, as it will be shown. This proposal modifies the 2S-PLL in [3] maintaining the synchronization performance while sampling at low sampling rates, typically at the power converter switching period.

2 DIGITAL IMPLEMENTATION OF THE TWO-SAMPLE PLL

The QSG proposed in [3] obtains the virtual in-quadrature component, β, by applying finite differences around an operation point, which can be dynamically adjusted as a function of the PLL frequency, ω. Computational delays are compensated within the QSG. At instant k, β_k is generated with only two samples of the grid voltage acquired in three consecutive sample instants:

$$\beta_k = (\alpha_{k-2} - \alpha_k)\frac{1}{\sin\left(\frac{4\pi}{N}\right)} + \alpha_k \tan\left(\frac{2\pi}{N}\right) \quad (1)$$

$$N = \frac{2\pi}{T_s \omega} \tag{2}$$

where α_k is the sampled grid voltage, T_s is the sampling time and ω is the grid frequency provided by the PLL. This approach minimizes the memory requirements of the QSG and keeps the orthogonality in the case of frequency variations by adjusting N.

The trigonometric functions in (1) are simplified by applying Taylor series expansions, which are truncated at the second term, instead of the first one, due to the low sampling frequency approach, then (1) converts to

$$\beta_k = (\alpha_{k-2} - \alpha_k)\frac{3N^3}{12\pi N^2 - 32\pi^3} + \alpha_k\left(\frac{2\pi}{N} + \frac{8}{3}\frac{\pi^3}{N^3}\right), \tag{3}$$

which, applying the Taylor series expansion of $\frac{1}{1+x} \approx 1 - x$, is rewritten as

$$\beta_k = (\alpha_{k-2} - \alpha_k)K_1\left(1 - K_2\Delta\omega\right) + \alpha_k\left(\omega T_s + \frac{1}{3}\left(\omega T_s\right)^3\right) \tag{4}$$

where, $\Delta\omega$ is the frequency variation detected in the PLL with respect to the given nominal grid frequency, ω_o ,–the output of the PLL loop filter, typically a PI controller-, $K_1 = \frac{1}{\left(2T_s\omega_0 - \frac{8}{6}T_s^3\omega_0^3\right)}$, $K_2 = \frac{2 - 4T_s^2\omega_0^2}{2\omega_0 - \frac{8}{6}T_s^2\omega_0^3}$. As a result, from (1) and (4), two trigonometric functions plus one division are replaced by two additions and two multiplications.

The phase detector of the 2S-PLL [3] is based on the Park transformation. The phase error signal, i.e. the *q* component, is evaluated from the grid voltage phasor projections on the rotating reference frame synchronized with the PLL phase. In order to reduce the computational burden, while retaining the required accuracy at a low sampling rate, it is proposed to replace the trigonometric functions required for the Park transformation with a digital oscillator [4]:

$$\begin{aligned}(\sin\theta)_k &= A_2(\cos\theta)_{k-1} + (1 + A_1A_2)(\sin\theta)_{k-1} \\ (\cos\theta)_k &= (\cos\theta)_{k-1} - A_1\left((\sin\theta)_{k-1} + (\sin\theta)_k\right)\end{aligned} \tag{5}$$

where $A_1 = \tan\left(\frac{\pi}{N}\right)$ and $A_2 = \sin\left(\frac{2\pi}{N}\right)$.

If required, the computational burden associated to the normalization block of the PLL can be minimized by replacing the associated operations with a gain, whose value depends on the nominal grid voltage. With all the above proposed approximations, the 2S-PLL can be implemented, following the block diagram in Fig. 1, using sequentially only one addition/subtraction and one multiplication elements, given that T_s is large enough.

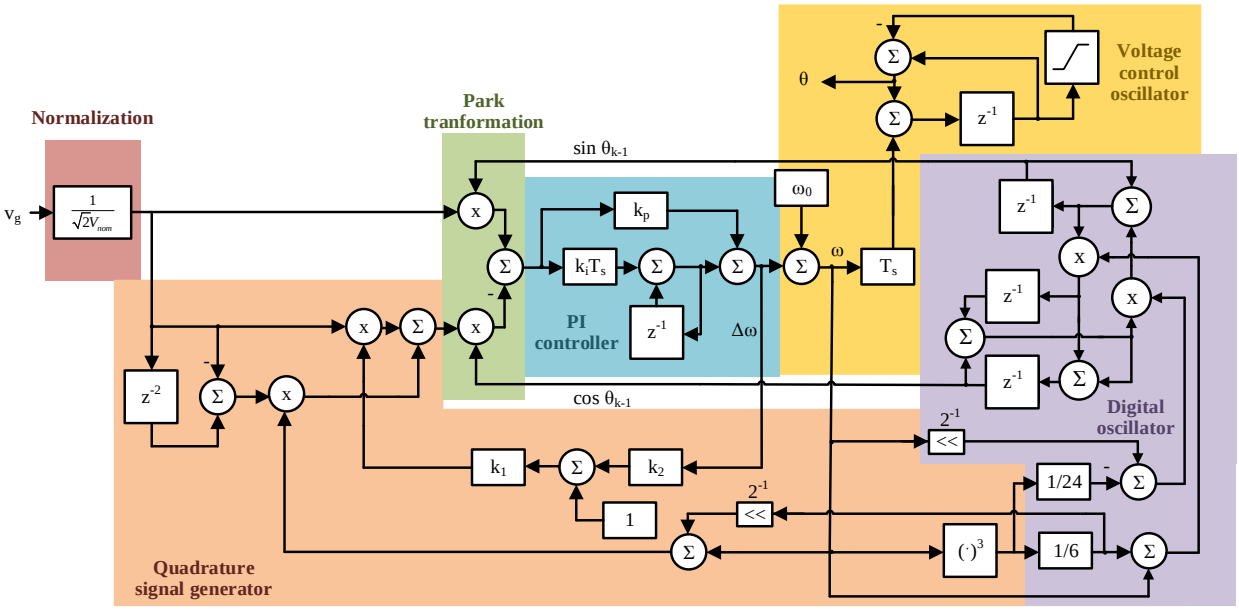


Fig. 1. Proposed 2S-PLL.

3 SIMULATION RESULTS

The original and proposed 2S-PLL are evaluated by simulation and their performances compared with the T/4 PLL one. These PLLs have been designed with the same PI controller parameters, according to [5] (proportional, $K_p = 46$ and integral gain, $K_i = 1024$). To obtain a first proof of concept, initial results are presented using the lowest sample rate in which the PLL obtains a response similar to the original 2S, demonstrating that the sample rate can be comfortably

adjusted to the switching frequency. The nominal frequency has been set to 50 Hz and T_s is 1/800 s.

The responses to a +10 Hz frequency step are shown in Fig. 2. The phase errors due to both 2S-PLL matches and are below the T/4 one in steady-state. The final manuscript will provide a detailed comparison in simulation.

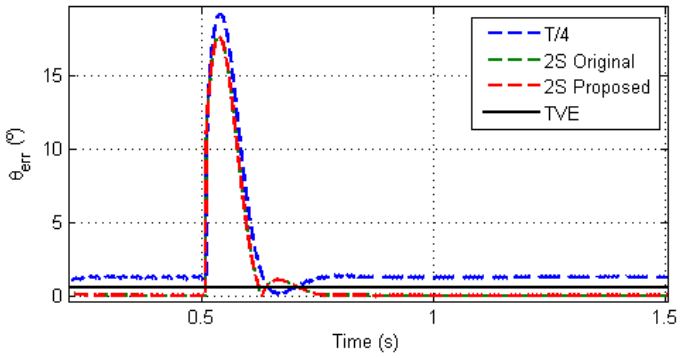


Fig. 2. Phase error due to a frequency step from 45 to 55 Hz.

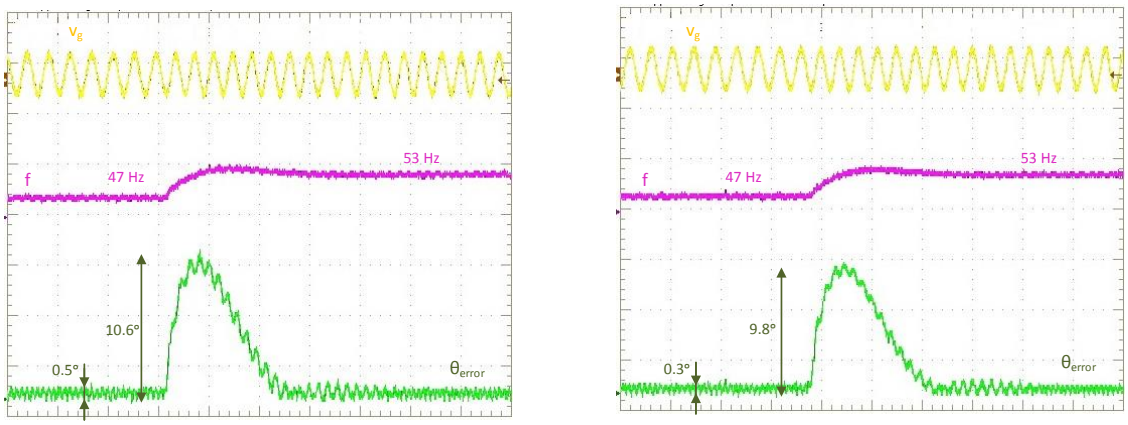
4 EXPERIMENTAL RESULTS

The proposed PLL has been implemented in a FPGA to assess the size of the circuits and synchronization capabilities. Table I summarizes the resources used by the proposed PLL in an Artix 7 FPGA (XC7A100T-1CSG324C, Nexys 4 board).

Table 1: Summary of the FPGA resources used by the PLLs using SysGen.

	Slice Registers	**LUTs**	**Occupied Slices**	**LUT Flip Flop pairs used**	**RAMB/ FIFOs**	**BUFG/ BUGCTROLs**	**DSP48E1s**
T/4 PLL	3472	4927	1697	5144	3	1	64
2S-PLL ORIGINAL	3488	5401	1746	5563	2	1	72
2S-PLL PROPOSED	238	1940	662	2033	0	1	32

In Fig. 3, the grid voltage, frequency and phase error signals are shown when a +6 Hz frequency step occurs, proving the effectiveness of the proposed PLL. In the final version, more results will be provided.



(a) (b)

Fig. 3. Grid voltage (yellow), frequency (green) and phase error (magenta) waveforms using proposed 2S-PLL under +6 Hz frequency step from 47 to 53 Hz. (a) T/4 and (b) 2S PLL.

5 CONCLUSIONS AND FUTURE WORK

A novel approach in digital implementation of 2S-PLL applied for low switching frequency to single-phase PFC has been presented in this work. The proposed methodology mainly focused on low cost implementation that allows a reduction of up to 65 % of the resources used in the FPGA with respect to the original 2S-PLL. Based on this approach, the PLL has been implemented, tested and verified that the phase error that occurs with the proposed PLL is lower, both at steady state and under frequency variations, than that obtained with one of the simplest strategies found in the literature, the T/4-PLL.

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