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Fabrication and Analysis of 4H-SiC Diodes

By

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Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author in School of Engineering of the University of Warwick.

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Publication List

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2. **Y. Bonyadi**, P. M. Gammon, O. Alatise, R. Bonyadi, and P. A. Mawby, "Lifetime Enhancement of 4H-SiC PiN Diodes Using High Temperature Oxidation Treatment," in Materials Science Forum, 2018, vol. 924: Trans Tech Publ, pp. 440-443.
3. Z. Davletzhanova, O. Alatise, R. Bonyadi, J. Ortiz-Gonzalez, C. Chan, **Y. Bonyadi**, M. Jennings, P. Mawby, "Impact of Leakage Currents on Voltage Sharing in Series Connected SiC Power MOSFETs and Silicon IGBT Devices," in 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), 2018: IEEE, pp. P. 1-P. 10.
4. **Y. Bonyadi**, P. M. Gammon, Y. K. Sharma, G. Baker, and P. A. Mawby, "An investigation into the impact of surface passivation techniques using metal-semiconductor interfaces," in Materials Science Forum, 2017, vol. 897: Trans Tech Publ, pp. 443-446.
5. **Y. Bonyadi** et al., "The impact of triangular defects on electrical characteristics and switching performance of 3.3 kV 4H-SiC PiN diode," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 2016: IEEE, pp. 1-5.
6. **Y. Bonyadi** et al., "Characterization of 4H-SiC PiN Diodes Formed on Defects Identified by PL Imaging," in Materials Science Forum, 2016, vol. 858: Trans Tech Publ, pp. 405-409.
7. C. Chan, **Y. Bonyadi**, P. A. Mawby, and P. M. Gammon, "Si/SiC substrates for the implementation of linear-doped power LDMOS studied with device simulation," in Materials Science Forum, 2016, vol. 858: Trans Tech Publ, pp. 844-847.
8. R. Bonyadi, O. Alatise, J. Hu, Z. Davletzhanova, **Y. Bonyadi**, J. Ortiz-Gonzalez, L. Ran, P. Mawby, "Compact electrothermal models for unbalanced parallel conducting Si-IGBTs," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), 2016: IEEE, pp. 253-260.

Abstract

Despite the excellent electrical and thermal properties of 4H-silicon carbide (SiC) and the advancements in the field of 4H-SiC epitaxial growth, the existence of defects in the material can considerably reduce the electrical performance of the SiC power devices. Defects can result in low carrier lifetime affecting the on-state resistance of bipolar devices, such as PiN diodes, and increased leakage current affecting the reverse blocking performance of power devices, such as Schottky diodes. A commonly found surface morphological defect in available 4H-SiC substrates is the triangular defect. In this thesis, the formation mechanism of this defect and its impact on the electrical performance of the fabricated 4H-SiC PiN diodes is discussed. 4H-SiC PiN diodes were intentionally fabricated on the triangular defects and in areas with no visible morphological defects. The devices were then packaged and tested to assess the impact of these defects on the resulting on-state and reverse leakage characteristics. It was shown for the first time the impact of triangular defects on switching characteristics of 4H-SiC PiN diodes fabricated on- and off-defects. Moreover, triangular defects were characterised using methods including AFM, SEM, Photoluminescence and HRTEM. Other complex structures were observed on the triangular defect using HRTEM such as double positioning boundary (DPB), which resulted in a leakage path through the drift region of the devices and increased the leakage current.

Furthermore, this thesis focuses on the fabrication and analysis of 4H-SiC power diodes for high voltage applications with particular focus on improving the performance of 4H-SiC SBDs using a novel metal-semiconductor interface treatment and 4H-SiC PiN diodes using high temperature processing techniques to improve the carrier lifetime, on-state resistance and conductivity modulation of the diode. Carrier lifetime enhancement in 4H-SiC PiN diodes in this thesis was achieved using a combined high temperature oxidation and successive argon annealing process at 1550°C for 1 hour. This resulted in an increase of nearly 45% of the reverse recovery current and approximately 40% of the carrier lifetime. The findings of this study could be potentially used for other 4H-SiC bipolar devices such as IGBTs, BJTs and thyristors.

This thesis has also investigated the impact of various surface passivation treatments to improve the quality of the 4H-SiC surface and the metal-semiconductor interface using Mo/Ti, and Ni-4H-SiC Schottky diodes. The most significant outcome of this investigation was the performance of P_2O_5 treated Mo/SiC Schottky diodes which retained a barrier height equivalent to that of titanium, but with a leakage current lower than any Ni diode, seemingly combining the benefits of both a low- and high-SBH metal. Furthermore, P_2O_5 treated Mo/SiC Schottky diodes were the only diodes to undergo any significant leakage current reduction after any of the pre-treatments exhibiting exceptionally low leakage, even at 300°C. XPS and SIMS analysis on all Mo/SiC SBDs revealed that the stoichiometry of the SiC underneath the contact was enhanced using P_2O_5 treatment and that traces of P_2O_5 were found after removal of the passivation layer and post-treatment metallisation. It was also found that the Mo-4H-SiC interface on the P_2O_5 treated sample was very sharp and uniform compared to the untreated sample where Mo-SiC interface looks uneven and cloudy. The developed novel metal-semiconductor interface treatment can be potentially used for MOS interface improvements.

List of Abbreviations

AFM	Atomic Force Microscopy
BPD	Basal Plane Dislocations
BJT	Bipolar Junction Transistor
CRT	Cathode Ray Display Tube
CVD	Chemical Vapour Deposition
CTE	Coefficient of Thermal Expansion
DLTS	Deep Level Transient Spectroscopy
DUT	Device Under Test
DBC	Direct Bonded Copper
DPB	Double Positioning Boundary
EV	Electric Vehicle
EELS	Electron Energy Loss Spectrometer
EDX	Energy Dispersive X-ray
FEG	Field Emission Gun
FIB-SEM	Focused Ion Beam Scanning Electron Microscope
GaN	Gallium Nitride
GTO	Gate Turn-Off Thyristor
HRTEM	High Resolution TEM
HTCVD	High Temperature Chemical Vapour Deposition
HVDC	High Voltage DC
HEV	Hybrid Electric Vehicle
ICP	Inductively Coupled Plasma
IGBT	Insulated Gate Bipolar Transistor
JBS	Junction Barrier Schottky

JTE	Junction Termination Extension
MPS	Merged PiN Schottky
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MP	Micropipes
NPT	Non-Punch-Through
PSG	Phosphosilicate Glass
PL	Photoluminescence
PV	photovoltaic
PDS	Planar Diffusion Source
PT	Punch-Through
RCA	Radio Corporation of America
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
SRH	Schockley-Read-Hall
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
SIMS	Secondary Ion Mass Spectroscopy
SM-JTE	Space-Modulated JTE
TE	Thermionic Emission
TFE	Thermionic Field Emission
TED	Threading Edge Dislocations
TSD	Threading Screw Dislocations
TRPL	Time Resolved Photoluminescence
TEM	Transmission Electron Microscopy
UHV	Ultra High Voltage
WBG	Wide Band Gap
XPS	X-Ray Photoelectron Spectroscopy

List of Symbols

Å	Lattice constant
A^{**}	Richardson's constant ($Am^{-2}K^{-2}$)
D_a	Ambipolar diffusion constant
D_n	Electron diffusion constant
D_p	Hole diffusion constant
D_{it}	Density of interface traps ($cm^{-2}eV^{-1}$)
E	Electric field (V/cm)
E_C	Bottom of conduction band (eV)
E_F	Fermi energy level (eV)
E_{FM}	Fermi energy level in metal (eV)
E_{FS}	Fermi energy level in semiconductor (eV)
E_G	Bandgap energy (eV)
Em	Peak electric field (V/cm)
E_0	Vacuum energy level (eV)
E_{00}	Characteristic energy (eV)
h	Planck constant (Js)
I_F	Diode forward current (A)
I_{RP}	Diode peak reverse current (A)
J_0	Reverse saturation current density (A/cm^2)
$J_{0,rec}$	Saturation recombination current density (A/cm^2)
J_{diff}	Diffusion current density (A/cm^2)
J_{drift}	Drift current density (A/cm^2)
J_n	Electron current density (A/cm^2)
J_p	Hole current density (A/cm^2)
L	Inductance (H)
L_a	Ambipolar diffusion length (cm)
m^*_T	Tunneling effective mass (kg)
N_A	Doping concentration (p-type) (cm^{-3})
N_D	Doping concentration (n-type) (cm^{-3})
N_{DP}	Doping concentration in the drift region (cm^{-3})
n_i	Intrinsic carrier concentration (MV/cm)
R_{drift}	Drift layer resistance (Ω-cm^2)
$R_{on,diff}$	Differential on resistance (Ω-cm^2)
R_{On}	Specific on resistance (Ω-cm^2)
T	Temperature (K)
t_{rr}	Reverse recovery time (s)
V_{ak}	Applied voltage (V)
V_B	Blocking voltage (V)
V_{bi}	Diode built-in voltage (V)
V_d	Width of depletion region (cm)
V_F	Forward voltage drop of overall PiN diode (V)

V_R	Reverse clamping voltage (V)
V_M	Forward voltage drop of modulated PiN diode drift region (V)
V_{sat}	Electron saturation velocity (cm)
V_T	Thermal voltage (V)
W_d	Width of the drift region (cm)
χ_S	Electron affinity for the semiconductor (V)
ε_0	Vacuum permittivity (F/m)
ε_r	Relative dielectric constant
η	Ideality factor
λ	Wavelength of light (cm)
μ_n	Electron mobility (cm^2/Vs)
μ_p	Hole mobility (cm^2/Vs)
τ	Carrier lifetime (s)
τ_{SRH}	Schockley-Read-Hall lifetime (s)
Φ_B	Metal-semiconductor barrier height (eV)
Φ_M	Work function of metal (eV)
Φ_n	Fermi potential measured from the conduction band (eV)
Φ_p	Fermi potential measured from the valance band (eV)
Φ_S	Work function of semiconductor (eV)

Chapter 1 Introduction

1.1 Introduction

Nowadays, the improvement of energy efficiency is one of the most critical problems due to limited non-renewable fuel resources and an increased consciousness regarding climate change. Climate change is due to the significant increase of greenhouse gas emissions. One of the means to reduce greenhouse emissions is by employing renewable energy generation solutions such as wind and photovoltaic (PV) solar cells. In 2010, the world average ratio of electrical energy consumption to total energy usage was around 20% [1]. This ratio is estimated to increase rapidly in the future as the global energy demand is continuously increasing. It is expected that over 50% of all electrical power is converted so that it can be supplied to the loads in an optimal form [1].

Generally, the performance of semiconductor devices are the main limiting factor of power electronics efficiency. Therefore, the development of high-voltage and low-loss

power devices is vital. Figure 1-1 shows the main application areas of power electronic devices as a function of rated voltage, such as power supplies, power transmission systems, Hybrid Electric Vehicle (HEV), Electric Vehicle (EV may also be referred to as BEV or battery electric vehicles), motor control, traction, and robotics. In addition to efficiency, cost and reliability are also crucial. Silicon (Si) is the most commonly used semiconductor in power electronics devices. Although the performance of Si power devices has been substantially improved, they are at their practical limit due to increasing demand of power devices in high power applications where higher power density (higher current handling capability and higher blocking voltage), higher operating temperature and substantially higher switching frequency is required. Therefore, to realise such requirements, research has shifted towards looking at using Wide Band Gap (WBG) semiconductor materials due to their superior material properties, including Silicon Carbide (SiC), Gallium Nitride (GaN) and diamond. At the moment, SiC is the most promising candidate for high voltage, high power applications with commercial devices already on the market. The work carried out in this thesis intends to further develop 4H-SiC high voltage power electronics technology to meet the above-mentioned requirements of the future power network.

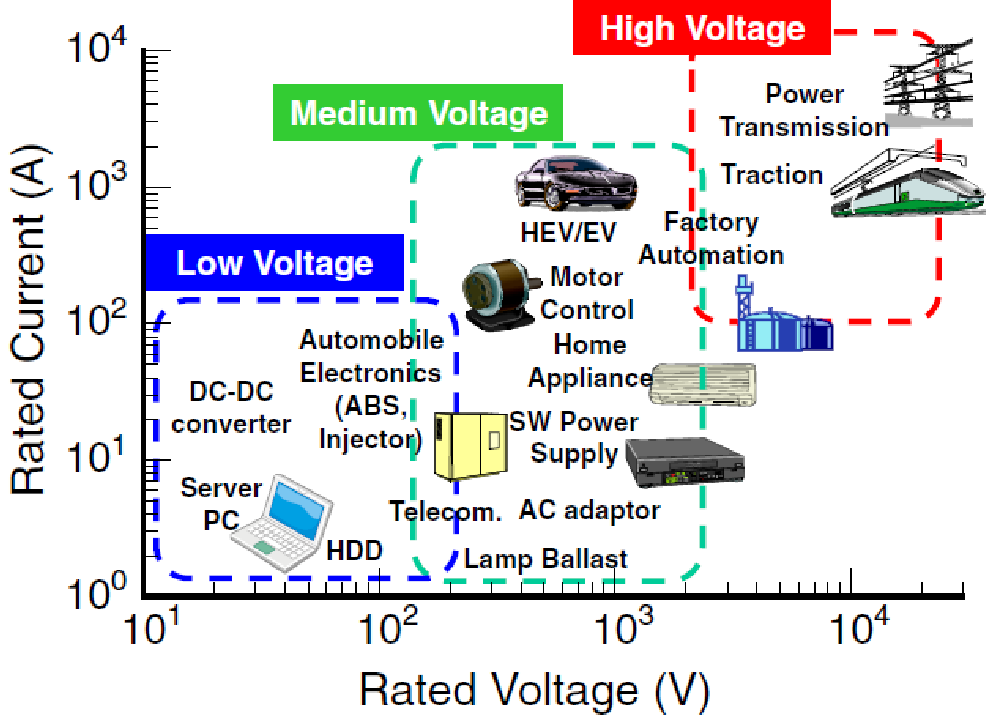


Figure 1-1: Main application area of power electronic devices as a function of rated voltage [1]

1.2 Background and Motivation

The aim of this thesis is to fabricate and characterise 4H-Silicon Carbide (4H-SiC) power diodes for high voltage applications with particular focus on improving the performance of 4H-SiC SBDs using novel metal-semiconductor interface treatment and 4H-SiC PiN diodes using high temperature processing techniques.

Despite the rapid development in the field of material growth over the past few years, reducing the defect densities of SiC substrate is still a critical challenge and is continuing to hinder the development of large area high current and high voltage

devices, such as low carrier lifetimes. Macroscopic defects, such as triangular defects, that are generated during epitaxial growth can also considerably reduce the electrical performance of the power devices. Triangular defects can be found in almost all commercial 4H-SiC epitaxial wafers. This has provided motivation to study the impact of this surface morphological defect on the electrical performance of fabricated 4H-SiC PiN diodes.

A critical issue in high-voltage bipolar devices is improving the carrier lifetime. Material defects in 4H-SiC result in low carrier lifetimes. In order to improve the electrical characteristics of bipolar devices such as PiN diode, sufficient carrier lifetime of 4H-SiC material is crucial for realising low forward conduction losses and reducing the on-resistance. As reported by Hiyoshi and Kimoto [1-3] high temperature oxidation treatments can be used to enhance the carrier lifetime in the semiconductor material by `repairing' carbon-vacancy related defects in high voltage PiN diodes. This is due to the removal of extra carbon atoms at the oxidising surface, which diffuse into the semiconductor bulk and reside on the vacant carbon locations. Therefore, the capability of performing high temperature oxidations is of great interest. In the study by Hiyoshi and Kimoto, they only explored thermal oxidation up to 1400°C, though, reassuringly, this was found to be significantly more effective at enhancing the carrier lifetime in the material for a certain oxidation time. The thermal oxidation Hitech furnace at Warwick enable research of thermally grown oxides at temperatures up to 1550°C which provided the motivation into further enhancing the carrier lifetime in high voltage 4H-SiC power devices as part of this thesis.

In addition to the above, further improvements to SiC SBDs are being sought by re-examining the Schottky metal contact. It has also been shown that [4] surface passivation treatments prior to metal deposition improve the electrical characteristics of the fabricated diode. There has been a recent increase in interest into molybdenum (Mo) Schottky contact [5, 6]. These have provided motivation for further research into the impact of various surface passivation techniques on Mo, Ni, and Ti based SiC Schottky diodes including the novel phosphorus pentoxide (P_2O_5) deposition treatment in order to enhance the electrical performance of the diodes [7]. The findings of this investigation can be potentially employed for MOS interface improvement.

1.3 Contribution of Knowledge

- It was shown for the first time the impact of triangular defects on switching characteristics of 4H-SiC PiN diodes fabricated on- and off-defects. Moreover, triangular defects were characterised using methods including AFM, SEM, Photoluminescence and HRTEM. Other complex structures were observed on the triangular defect using HRTEM such as double positioning boundary (DPB), which resulted in a leakage path through the drift region of the devices and increased the leakage current.

- Another particular novel contribution of this thesis is on improving the performance of 4H-SiC SBDs using a novel metal-semiconductor interface treatment and 4H-SiC PiN diodes using high temperature processing techniques to improve the carrier lifetime, on-state resistance and conductivity modulation of the diode. Carrier lifetime enhancement in 4H-SiC PiN diodes in this thesis was achieved using a

combined high temperature oxidation and successive argon annealing process at 1550°C for 1 hour. This resulted in an increase of nearly 45% of the reverse recovery current and approximately 40% of the carrier lifetime. The findings of this study could be potentially used for other 4H-SiC bipolar devices such as IGBTs, BJTs and thyristors.

- Another contribution of knowledge in the work presented in this thesis is improving the quality of the 4H-SiC surface and the metal-semiconductor interface using Mo/Ti, and Ni-4H-SiC Schottky diodes. The most significant outcome of this investigation was the performance of P_2O_5 treated Mo/SiC Schottky diodes which retained a barrier height equivalent to that of titanium, but with a leakage current lower than any Ni diode, seemingly combining the benefits of both a low- and high-SBH metal. Furthermore, P_2O_5 treated Mo/SiC Schottky diodes were the only diodes to undergo any significant leakage current reduction after any of the pre-treatments exhibiting exceptionally low leakage, even at 300°C. XPS and SIMS analysis on all Mo/SiC SBDs revealed that the stoichiometry of the SiC underneath the contact was enhanced using P_2O_5 treatment and that traces of P_2O_5 were found after removal of the passivation layer and post-treatment metallisation. It was also found that the Mo-4H-SiC interface on the P_2O_5 treated sample was very sharp and uniform compared to the untreated sample where Mo-SiC interface looks uneven and cloudy. The developed novel metal-semiconductor interface treatment can be potentially used for MOS interface improvements.

1.4 Thesis Outline

Chapter 2 gives a background on the application areas of the power devices being developed in this work and provides an insight into performance benefits that 4H-SiC can offer over existing technologies. In addition to the material advantages of 4H-SiC, its crystal structures, bulk growth challenges and the material defects are also discussed here. Then, finally, a discussion on the present status of SiC power diodes is given.

Chapter 3 provides an introduction into the physics of operation of PiN and Schottky diodes and the physics of the semiconductor. The fundamental operating principles of these devices are outlined which are important for design and optimisation of device structures. This includes the analysis of the on-state, switching, and reverse blocking behaviour of the diodes.

Chapter 4 presents the 4H-SiC fabrication technology for the fabrication of 4H-SiC PiN diodes and Schottky diodes in this thesis. Following this, the device packaging process of the fabricated devices is presented. Chapter 5 outlines the characterisation techniques that have been employed when characterising the high voltage 4H-SiC PiN and Schottky diodes. First, the electrical characterisation techniques are discussed including on-state characteristics and reverse blocking at a range of temperatures as well as switching behaviour of the PiN diodes. Subsequently, the physical characterisation techniques of the 4H-SiC wafers are discussed.

In Chapter 6, the impact of a surface morphological defect, the triangular defect, on fabricated 4H-SiC PiN diodes is explored. This Chapter provides a background on macroscopic defects in Silicon Carbide material and the importance of this study. This Chapter first discusses the electrical performance of devices fabricated in areas with no visible defects. It then uses the device fabrication process as a benchmark for characterising the devices with the same active area and fabrication process that are intentionally fabricated on the triangular defect. Following this, the Chapter provides detailed results on the material characterisation, and electrical performance of the fabricated 4H-SiC PiN diodes on and off-defects and clamped inductive switching tests results.

The optimised PiN diode fabrication process in Chapter 6 is then used in Chapter 7 to study the application of a combined high temperature thermal oxidation and annealing process to 4H-SiC PiN diodes with 35 μm thick drift regions, the aim of which was to increase the carrier lifetime in the 4H-SiC and improve their electrical performance. Diodes were fabricated using 4H-SiC material and underwent a thermal oxidation and argon anneal process. Reverse recovery tests indicated a significant carrier lifetime enhancement due to increase of minority carriers in the drift region. The switching results illustrate that the use of this process is a highly effective and efficient way of enhancing the electrical characteristics of high voltage 4H-SiC bipolar devices.

In Chapter 8, the impact of surface passivation treatments on both the SiC surface and the metal-semiconductor interface prior to the device fabrication is

investigated. The findings of this investigation can be potentially employed for MOS interface improvement. To do so, SBDs were fabricated on treated SiC surfaces, so that metal-semiconductor junctions could be used to evaluate the quality of this surface, using a range of metals including Mo, Ni, and Ti. Various surface passivation treatments were performed on 4H-SiC surface, including a novel surface passivation process. SBDs developed after the removal of these passivating layers were compared to those on untreated (control) surfaces and analysed physically using XPS, SIMS, TEM, and SEM, and electrically using I-V and I-V-T characteristics as well as inhomogeneity characterisation familiar to Schottky analysis.

Finally, Chapter 9 presents the conclusions of this thesis as well as suggestions for further work.

Chapter 2 Power Electronic Devices and Silicon Carbide

2.1 Background

The first power rectifier was invented in 1902 by Peter Cooper Hewitt which was a mercury-vapour rectifier used to rectify AC power into DC power. This device was used to drive industrial motors as well as high voltage DC (HVDC) lines used in electric railways in London. After the development of solid-state semiconductor technology, diodes in the form we know today replaced mercury-arc rectifiers. Nowadays, power diodes are used in almost all high voltage applications, such as, transportation and automotive applications, specifically in hybrid and electric vehicles as well as public transportation such as buses and trains, marine, aviation, motor drive applications and

in renewable energy such as on-shore and off-shore wind turbines, photovoltaic solar cells and in power lines such as HVDC, and so on. To improve the performance of a power converter system it is critical to enhance the performance of the power semiconductor devices within the system. The viability of HVDC systems is highly dependent on the performance of the required power electronics to convert between voltage levels. These can include rectifiers or switches that control the electric power (voltage, current, frequencies, etc.)[8].

Advancements in the processing of Silicon (Si) semiconductor technology has resulted in robust and cost-effective power electronic devices, which are the basis of the power industry today. The low defect density, high yield and large sizes of Si wafers have resulted in the high quality and low cost material that currently drives the power electronics industry. Since 1947, when the transistor effect was discovered by Bardeen and Brattain [9], an enormous number of fundamental studies were carried out focusing on material physics and process technologies in Si. Applications of Si power devices started in the mid-1950s using bipolar junction transistors (BJTs) [8] in medium power systems applications. This was followed by the development of thyristors [10] or Gate Turn-Off thyristors (GTOs) [11] in the 1960s for high power systems applications. Power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) were presented in the 1970s to substitute the low voltage BJTs offering fast switching speed [12, 13]. Later on, the Insulated Gate Bipolar Transistor (IGBT), which is the combination of BJT and MOSFET, was designed for high power applications [14]. Intrinsically, the oxidation of Si, forming silicon dioxide (SiO_2), results in promising

high quality MOS structures, which are widely used within switching devices such as MOSFETs, and IGBTs. Since the 1980s, enormous amount of work has been carried out to improve the performance of power Si MOSFETs and Si IGBTs [15-17], and today, they are utilised in both high power systems such as industrial motor drive or electric vehicles, and low power systems such as consumer electronics, home appliances, and medical equipment. In addition to the switching devices, diodes are also used in power electronics applications, such as rectification. The most common power diode in high voltage applications is the Si PiN diode, which has a high blocking voltage as well as low on-state voltage due to the conductivity modulation of this bipolar device.

However, the limitations of using Si-based power devices are exposed by the desire to increase power density, reduce losses and shrink power converters and inverters by increasing the switching speed of the power semiconductor devices, as well as a need to increase the operating temperature. Higher power density leads to generation of more heat in the same volume and hence results in a significant cooling challenge for power converters. Additionally, the thermal conductivity of Si is very low and hence, the thermal management of Si-based power converters becomes more challenging. With silicon power devices reaching their theoretical limit in terms of delivering high power and higher efficiency, while reducing the size of the system to meet the market demand, research has moved towards looking at new semiconductor material with wide-bandgap (WBG). The superior physical and electrical properties of WBG material are more suited for demanding market for high power density (power densities of 60 kW/kg or higher) in higher voltage applications, and to achieve lower

losses and higher working temperatures. In particular, Silicon Carbide (SiC) has become a promising candidate for the next generation of power electronic device materials [1, 18-20]. Section 2.5 details the physical and electrical properties of SiC.

2.2 Requirements for Power Electronics Devices

Power electronic devices are the main components in power conversion systems. Figure 2-1 shows a typical circuit of a three-phase power inverter used for motor control. An inverter functions in a way that the electric power delivered to the motor is regulated by the switching operation of a pair, involving a switching device (transistor) and a diode. In many applications, it is required that both the switching devices and the rectifiers (diodes) have the same voltage and current rating. Normally, power devices are either "on" or "off". During switching operation, a power device operates between the on-and off-states, however the switching frequency is typically ranging between 1 kHz to a few 100 kHz.

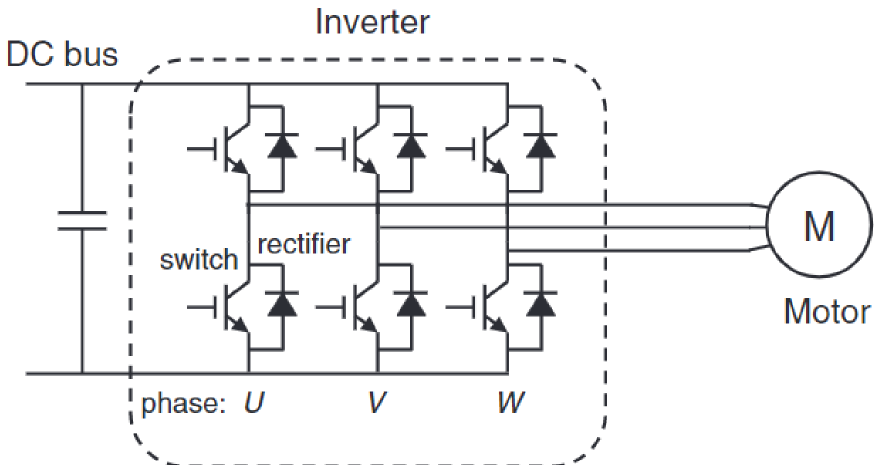


Figure 2-1: Three-phase power inverter circuit for motor control

The comparison between ideal and real I-V characteristics of a power switching device and a power diode is illustrated in Figure 2-2. When an ideal device is in the "on-state" it has "zero" voltage drop across it and when in the "off-state" it has "zero" leakage current and "infinite" breakdown voltage. Moreover, in an ideal switch, the switching between these two states should be instantaneous having zero power loss. However, real devices suffer from power loss in both the on and off-state and during the transition between these two states. There is also a finite on-resistance (R_{ON}), a voltage-drop at forward bias, and a finite leakage current at reverse bias as well as a maximum breakdown voltage. These are the key reasons for the on-state and off-state loss of the device. Therefore, when designing a power device, the following key requirements must be considered (i) low on-state voltage (low R_{ON}), (ii) low leakage current, and (iii) fast switching with minimum current/voltage transients. These have a direct impact on the on-state, off-state, and switching losses, respectively. Also, high blocking voltage can be a requirement depending on the applications. In all these aspects, SiC shows promising potential, as described in Section 2.5.

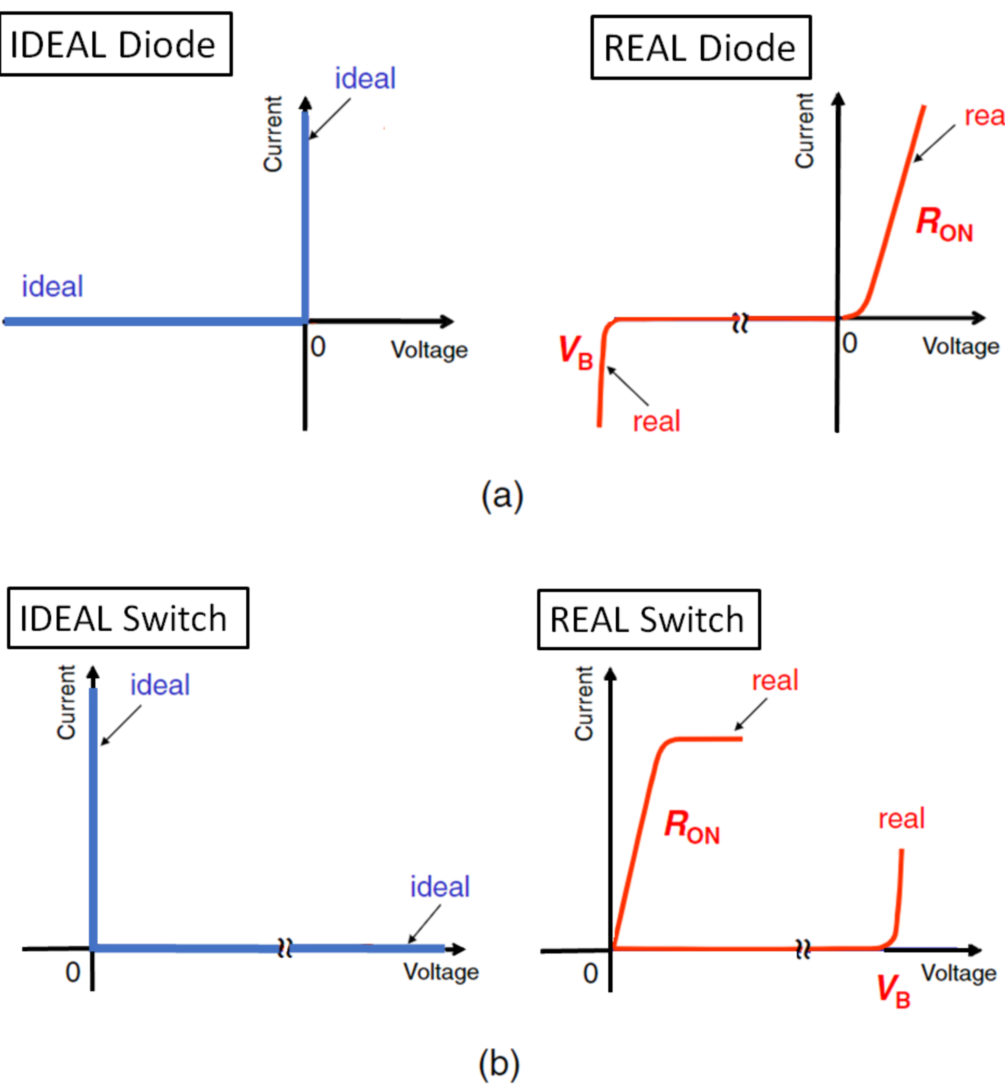


Figure 2-2: Current–voltage characteristics of (a) power diode and (b) power switching device, showing the comparison between the ideal and real I-V characteristics.

2.3 Silicon Carbide for Power Electronics

Wide-bandgap semiconductors are attracting much attention as a material for the next-generation power devices to overcome the performance limitation of Si power devices. Both SiC and gallium nitride (GaN) are wide-bandgap semiconductors that have attracted much interest for a new generation of power devices owing to their physical properties. Due to the readiness of reasonably high-quality epitaxial SiC wafers and the more mature process technology, the use of SiC power devices are more attractive for high voltage applications and has been the main topic of interest in research for the recent years. The manufacturing of high quality commercial freestanding GaN substrates is yet to be produced. GaN High Electron Mobility Transistor (HEMT) is a commercially available planar device with lateral current flow, suitable for high frequency, moderately low-voltage and low-power applications, up to 600 V [21]. GaN devices are fabricated on GaN heteroepitaxially grown on large Si wafers [22, 23]. Moreover, heat extraction from these devices is an engineering challenge that needs to be improved. Improvements in material growth and device fabrication technology of both SiC and GaN materials will determine the performance, reliability, and cost of these two materials. However, due to its physical and electrical exceptional properties (as will be discussed in section 2.5), SiC has been developed as a semiconductor material for high power and high temperature applications [24-27].

Silicon carbide is a group IV compound material. The extremely high hardness and chemical inertness of SiC material is due to the strong chemical bonding between Si and C atoms (4.6 eV) which also results in the wide-bandgap of SiC, 2.3–3.3 eV, dependent on the crystal structure, or polytype. Amongst several wide-bandgap semiconductors, SiC is remarkable as it can be simply doped to make either p-type or n-type with a wide range of doping densities (10^{14} —10^{19} cm^{-3}). Furthermore, due to SiC being the only compound semiconductor to have its native oxide, SiO_2, makes it possible to fabricate the complete family of MOS-based electronic devices using SiC, such as MOSFETs. In recent years, significant energy saving impacts of using SiC power devices (Schottky barrier diodes (SBDs) and power MOSFETs) in applications such as air conditioners, photovoltaic converters, industrial motor control, and railcars have been demonstrated. In this chapter, the superior physical and electrical properties of SiC, the current status of SiC power devices, and current and future challenges of SiC bulk and epitaxial growth is reviewed discussing the SiC growth process, its challenges and defects in SiC material.

2.4 Crystal Structure and Polytypes of Silicon Carbide

SiC is a covalently bonded semiconductor where both Si and C atoms are tetrahedrally bonded (as shown in Figure 2-3) and share electron pairs in sp^3– hybrid orbitals to form a SiC crystal [28]. SiC exists in various structures with diverse stacking sequences (known as polytypism) [29]. However, existence of over 200 known polytypes

was historically a major difficulty in growing electronic-grade SiC crystals [29]. The Si-C pairs can reside in three different locations labelled A, B, and C as shown in Figure 2-4. Each layer is comprised of tetrahedra in only one location.

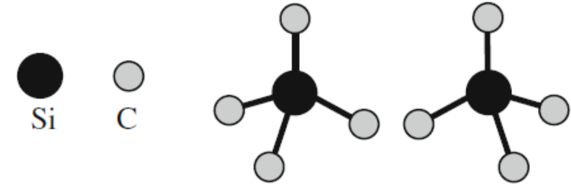


Figure 2-3: Two types of tetrahedrons creating the basis of all SiC crystals where each Si atom in the tetrahedron is covalently bonded to four adjacent C atoms. Each type must be rotated around its c-axis (vertical here) by 180° to obtain the other type

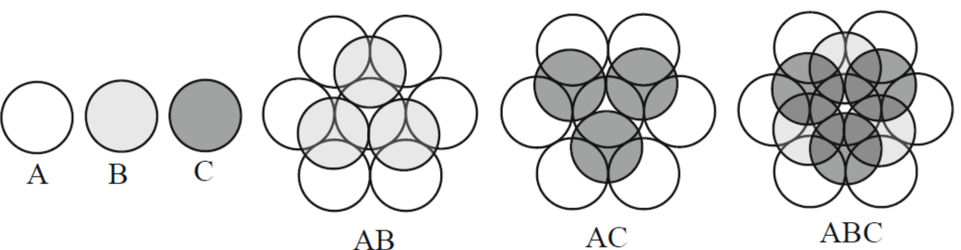


Figure 2-4: In the hexagonal packing system, the Si-C pairs can reside in three different locations labelled A, B, and C.

Figure 2-5 [28] shows the stacking sequence of three major SiC polytypes, known as 3C-SiC, 4H-SiC, and 6H-SiC, where the open and closed circles represent the Si and C atoms, respectively. According to Ramsdell notation [29], "C" denotes the cubic crystal structure, "H" refers to the hexagonal crystal structure and the number before "C" and "H" refers to the number of double-atomic layers in one repeating unit cell. Other types

of SiC crystals exist, for example, 15R-SiC where "R" refers to the rhombohedral crystal structure. The hexagonal unit cell of SiC is illustrated in Figure 2-6, where the major crystal faces, labelled as (0001), $(000\bar{1})$, $(11\bar{2}0)$, and $(1\bar{1}00)$, are shown. The (0001) crystal face is called the "Si face" which is almost entirely the typical face of commercial SiC wafers and $(000\bar{1})$ is referred to as the "C face".

SiC substrates and epitaxial layers in polytypes of 3C, 4H and 6H-SiC are available from a wide range of manufacturers such as CREE, Dow Corning, Novasic, Nitride Crystals Groups, PAM-XIAMEN, TankeBlue Ltd., Showa Denko, SiC Systems, SiCrystal AG, and NSSMC [30-36].

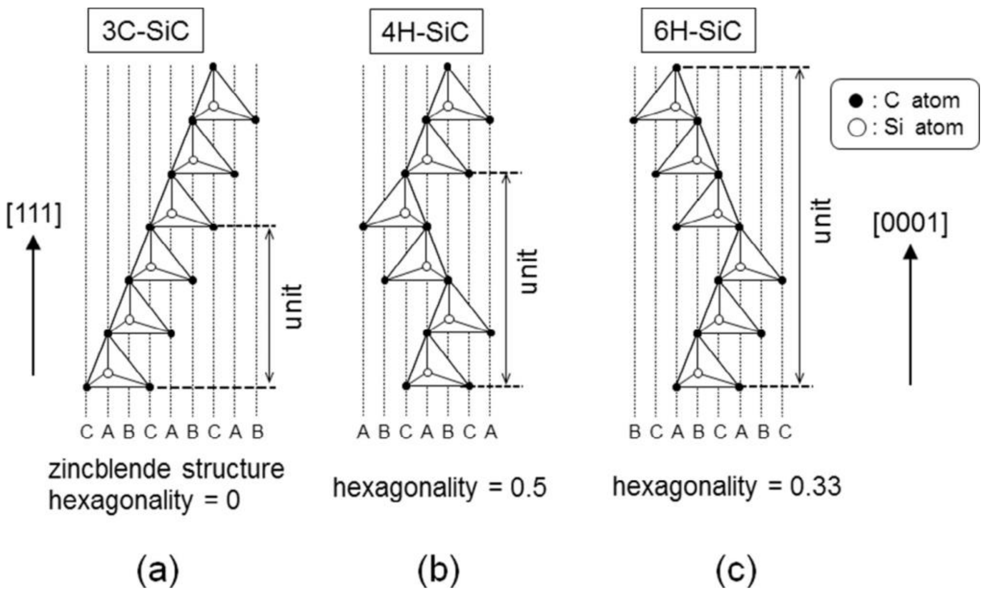


Figure 2-5: Three most common polytypes of SiC (a) 3C-SiC, (b) 4H-SiC and (c) 6H-SiC where the c-axis denotes the stacking direction. The letters A, B, and C refer to the three potential locations of a closely-packed structure. Si and C atoms are indicated by open [28].

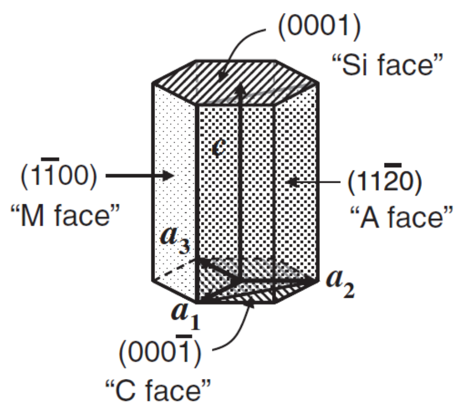


Figure 2-6: Hexagonal cell of SiC showing the major crystal faces labelled as (0001), (0001), (112 0), and (11 00).

The electronic properties of the different SiC polytypes give rise to different electronic band structures and resulting in different optical and electronic properties. Some physical properties of SiC polytypes, such as the stability and nucleation probability, significantly rely on temperature. For instance, it is found that 3C-SiC polytype is unstable, and changes its form into hexagonal SiC polytypes such as 6H-SiC at high temperatures over 1900–2000°C [37] resulting in a very challenging growth process of large 3C-SiC boules at a commercial growth rate. However, 3C-SiC polytype has gained excessive interest in recent years due to its cubic nature, as it can be heteroepitaxially grown on Si substrates, and therefore theoretically offers a low cost alternative to 4H-SiC. However, it contains a large number of extended defects which result on high leakage currents in 3C-SiC/Si devices [38].

As seen in Figure 2-5(b), 4H-SiC polytype is found to have the four layer repeating stacking sequence ABCB, with a crystal structure consisting of 1/2 hexagonal

(zincblende) and 1/2 cubic (wurtzite) positions, while 6H-SiC is found to have a stacking sequence of ABCACB, and 1/3 hexagonal to 2/3 cubic positions.

2.5 Physical & Electrical Properties of Silicon Carbide

Superior electrical and thermal properties of SiC have made it a promising material for power electronics applications. Table 2-1 presents the key physical properties of 3C- and 4H-SiC polytypes against Si and other wide-bandgap semiconductor materials at room temperature. 4H-SiC demonstrates around ten times higher critical (break-down) electric field strength, three times larger bandgap, and three times higher thermal conductivity compared to silicon, making it particularly attractive for high-power and high-temperature applications [1, 18, 24, 39]. It should be noted that in 4H-SiC polytype, the electron mobility along the < 0001 > direction is around 15–20% higher than electron mobility perpendicular to < 0001 >. This is an advantage for the vertical power devices on standard SiC < 0001 > wafers [1, 40].

Table 2-1: Key physical properties of 3C- and 4H-SiC polytypes together with other common semiconductor materials at room temperature [41]

Property	Units	3C-SiC	4H-SiC	Si	GaN
Lattice constant, Å		4.36	a=3.09 c=10.08	5.43	a=3.19 c=5.19
Bandgap, E_G	eV	2.3	3.26	1.12	3.42
Electron mobility, μ_n	cm^2/Vs	1000	1000 (⊥ c) 1200 (// c)	1350	1500
Breakdown field, E_B	MV/cm	1.5	2.8	0.3	3
Intrinsic carrier concentration, n_i	cm^{-3}	$\approx 10^{1}$	$\approx 10^{-8}$	$\approx 10^{10}$	$\approx 10^{-10}$
Hole mobility, μ_p	cm^2/Vs	50	120	450	50
Electron saturation velocity, V_{sat}	10^7 cm/ Vs	2.7	2.2	1	2.7
Thermal conductivity	W/cmK	4.9	4.9	1.5	1.3
Relative dielectric constant, ε_r		10	9.7 (⊥ c) 10.2 (// c)	11.9	10.4

As seen in Table 2-1, Si has a considerably larger intrinsic carrier concentration compared to the wide-bandgap semiconductors, due to its narrower bandgap. This limits Si device operating temperature to around 150°C [42]. At this temperature, the number of electron-hole pairs that are thermally generated begins to surpass the number of existing free carriers due to the intentional doping of the Si material. This is when the material becomes intrinsic and the device fails. On the contrary, 4H-SiC can reach temperatures of around 700°C before operating in the intrinsic region owing to its wide-bandgap. However, this temperature far exceeds the temperature handling capability of any semiconductor device packaging, as it is very close to or higher than the melting point of typical metals utilized for wire bonding, such as aluminium, copper

and gold. Currently, the restraint for high temperature applications of SiC is due to these packaging technology limitations.

Another key observation from physical properties comparison in Table 2-1is the high critical electric field for 4H-SiC, which is almost ten times higher than that for Si. For a semiconductor material, the value of critical electric field is related to its bandgap energy. Therefore, in a semiconductor with a wider bandgap, a higher energy is needed to break a chemical bond. Hence, larger electric fields must be applied before avalanche breakdown happens. This is illustrated schematically in Figure 2-7 showing the electric field distribution in a one-sided abrupt junction for SiC and Si at the same breakdown voltage.

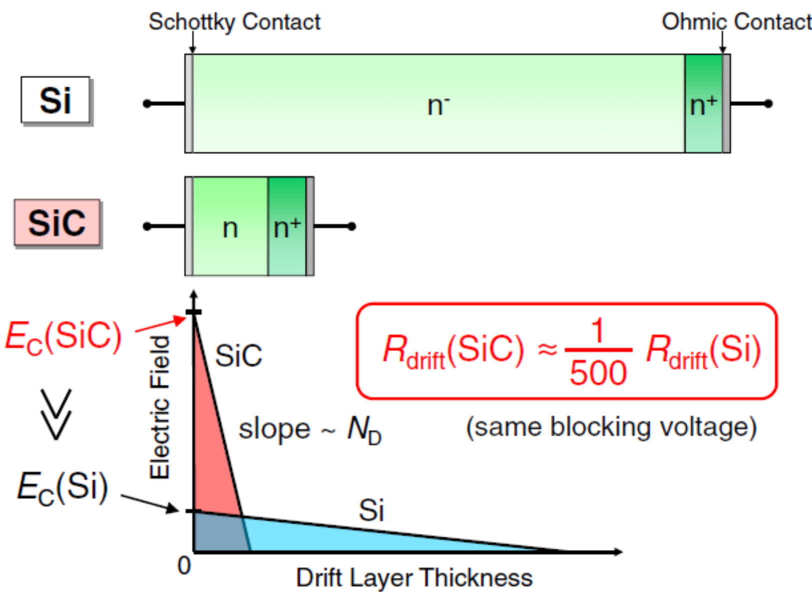


Figure 2-7: Electric field distribution in a one-sided junction for Si and SiC at the same voltage [1]

The higher critical electric field strength of 4H-SiC compared to Si means that the thicknesses of the voltage-blocking layers in 4H-SiC power devices can be one-tenth of those in Si devices, and the doping concentrations of the 'drift' region can be two orders of magnitude higher than their Si equivalents without compromising blocking voltage capability. Hence, in unipolar devices by employing SiC instead of Si, the drift layer resistance can be decreased by 2–3 orders of magnitude at any specified blocking voltage. This is mostly important for high-voltage devices as the drift-layer resistance (R_{drift}) increases with the blocking voltage (V_B) and is the main factor defining the total specific on-resistance (R_{ON}) of power devices [1, 43, 44]. The on-state loss (P_{ON}) of a power device without a built-in voltage is given by:

$$P_{ON} = R_{ON} J_{ON}^2 \tag{2-1}$$

where J_{ON} is the on-state current density and is normally around 100–300 A/cm^2 at the rated current. Hence, lower on-state losses in SiC power devices is due to the exceptionally low drift resistance. Figure 2-8 illustrates the theoretical minimum specific R_{ON} (drift-layer resistance) against the blocking voltage for Si and SiC unipolar devices. The minimum specific on-resistance is given by [1, 24, 44].

$$R_{drift} = \frac{4V_B^2}{\eta \varepsilon_r \mu E_B^3} \tag{2-2}$$

where ε_r is the dielectric constant, μ, is mobility, E_B is the breakdown field strength, and η is the ionization ratio for the dopants at room temperature. As shown in Figure 2-7, for the same breakdown voltage, the specific on-resistance of Si devices are of the order of 350 times higher than their 4H-SiC counterparts. In addition,

electron saturation velocity of 4H-SiC is approximately an order of magnitude greater than that for Si which also aids low switching losses.

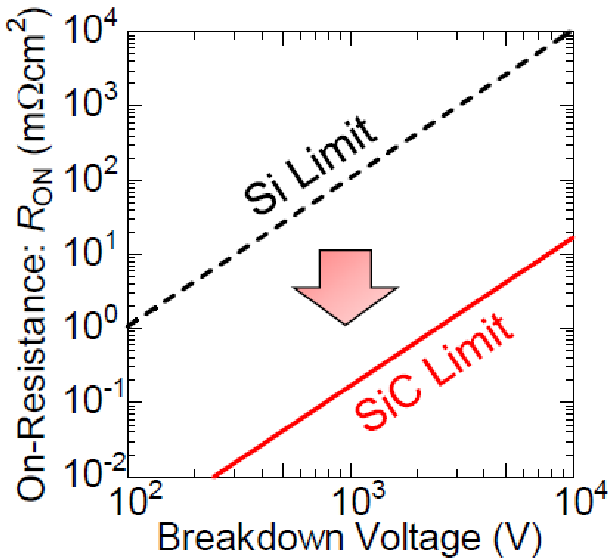


Figure 2-8: Relationship between on-resistance and breakdown voltage for Si and SiC unipolar devices.

For applications where power electronics devices with high blocking voltages are required, such as HVDC systems, a thick, low doped (and hence resistive) drift region is required to block the voltage in the off-state. In order to achieve a high blocking voltage whilst at the same time delivering an acceptably low forward resistance, the use of bipolar devices, such as PiN diodes and IGBTs, are preferable to unipolar devices, such as Schottky barrier diodes and MOSFETs. This is because, in the case of bipolar devices rated above 600V in Si devices, the background resistance of the drift region is reduced by a high concentration of injected minority carriers. In unipolar devices, no carrier injection occurs and the background resistance of the drift region remains high

in the on-state. However, the trade off in this process is that in bipolar devices, the process of removing the injected charge via electron-hole recombination is relatively slow resulting in significantly lower switching speeds compared to unipolar devices. Thus, Si-based bipolar power devices consequently have a very low switching speed, typically up to 20 kHz, and this is the main limiting factor in downsizing Si-based power converters. Assuming the use of Si devices, in high voltage applications, it becomes necessary to use bipolar devices such as IGBTs, thyristors and PiN diodes at any voltage rating above 600 V. However, with commercial SiC devices now providing an alternative, the unipolar voltage range extends to thousands of volts, resulting in a fast switching alternative to the Si bipolar technology. Moreover, SiC bipolar devices have the potential to operate at greater voltage ratings in the future (up to 20 kV) and as discussed earlier, could offer fast switching because the drift region is about ten times thinner and thus the stored charge in the region is about ten times smaller compared with Si bipolar devices [24, 26].

Another key observation from the above comparison is the high thermal conductivity of 4H-SiC which is approximately three times higher than Si. This is another significant benefit of 4H-SiC material for power electronics applications enabling 4H-SiC devices to operate at higher power densities while dissipating heat much more readily, consequently reducing the necessity for large, bulky heat sinks and cooling systems. Finally, as stated above, the very low intrinsic carrier concentration of 4H-SiC also benefits high temperature operation of power devices.

It is evident from Table 2-1 that the drawback of 4H-SiC when compared to Si is the lower carrier mobility (for both electrons and holes) in the material. As previously explained, higher on-state resistance results in higher on-state losses, but in 4H-SiC unipolar devices, the higher on-state resistance can be aided by employing thinner, more lightly doped drift region, which in turn can mitigate this disadvantage. The values of mobility in Table 2-1 are for the bulk material. Due to the poor quality of 4H-SiC/SiO_2 interface, the surface mobility in 4H-SiC is considerably lower than in the bulk material [45]. This causes substantial complications especially for MOS devices, since the low surface mobility results in a high channel resistance, and therefore high on-state losses.

Figure 2-9 shows the voltage rating of unipolar and bipolar power devices for both Si and SiC [1]. Due to extremely small transient loss of unipolar devices, Si bipolar devices, such as IGBTs are under threat from SiC unipolar devices, such as SBDs and MOSFETs in the blocking range of 600 V-1700 V today, and maybe yp to 10 kV in the future. SiC bipolar devices are attractive for ultrahigh-voltage devices (>10 kV) where Si power devices can offer no alternative. However, in a normal environment, at low voltage region (<600 V), Si will remain dominant because Si can gscale down its on-resistance in this region, which SiC cannot. However, within a harsh environment, such as high temperature or high radiation, SiC devices may be promising.

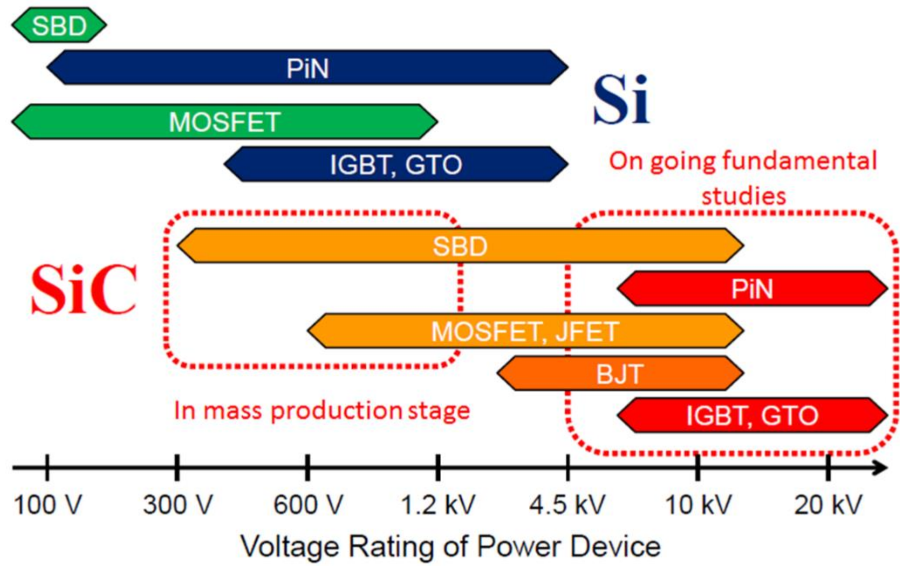


Figure 2-9: Voltage rating of Si and SiC power devices.

The behaviour of defects in the SiC material and their effect on the performance of power devices and their reliability are under investigation. Therefore, regardless of the exceptional electrical and thermal properties of 4H-SiC, the existence of defects can extremely reduce the performance of high-voltage devices that are fabricated from them, it is important to understand the growth process of SiC, formation defects in the SiC material and their impact on SiC power devices.

2.6 Bulk Growth of Silicon Carbide and Its Challenges

Conventional crystal pulling methods of growing Si are proved to be impractical to grow single crystal SiC, as extremely high pressures and temperatures are needed [46]. At present, the typical method for SiC bulk growth is the seeded sublimation (or modified Lely) method which has been reported in [47-51]. Since no stoichiometric SiC liquid phase exists, it is not possible to utilise congruent melt growth for SiC bulk growth at technically feasible system pressures [28]. Instead, sublimation growth of SiC is possible given that SiC sublimes at temperatures beyond 1800°C-2000°C [1]. The sublimation growth process of SiC involves three steps; the first step is the sublimation of the SiC source, the second step is mass transport of the sublimed species, and the third step is surface reaction and crystallization. This growth technique is also referred to as "Physical Vapour Transport" or PVT process. Any variations in the temperature profile and pressure can cause constitutional supercooling (such as formation of silicon droplet), graphitization of the surface, and carbon (C) inclusions which can all result in the creation of macro- and micro-defects in SiC boules [28, 49, 52]. Substantial attempts and extensive research in sublimation growth of SiC has resulted in remarkable improvement in the size and quality of SiC wafers in the last decade [53, 54]. Using this method, 4H-SiC <0001> wafers with a diameter of 150 mm (6 inch) are currently commercialized by several semiconductor manufacturers. Even in research phase, 200 mm (8 inch) wafers were demonstrated in 2015 [54] as well as ultra-high quality SiC single crystals in [55].

However, a few other growth methods have been developed which have demonstrated much potential of high quality and high purity, respectively. Epitaxial growth is needed for the development of SiC power devices in order to grow active layers with the preferred doping density and thickness. The word “epitaxy” comes from the Greek words meaning “above” and “order”, and indeed the growth process occurs above a substrate with its crystallographic order maintained in the new layer formed. If the chemical and physical characteristics of the substrate and epitaxial layer (epilayer) are the same, the growth process is referred to as homoepitaxial growth. However, if the chemical identity or crystallographic structure of the substrate and epilayer are different (for example 3C-SiC on 4H-SiC), then the process is called heteroepitaxial growth. The high-quality homoepitaxial growth of SiC was first realised by employing step-flow growth on off-axis <0001> SiC substrates using Chemical Vapour Deposition (CVD) [56, 57] where a mix of gases is flown inside a chamber. Perfect duplication of the SiC polytype without any polytype mixing is essential in the epitaxial growth of SiC. This was first realised by Matsunami et. al in 1987 by using step-flow growth technique, called “step-controlled epitaxy” [19, 56, 58]. The use of this technique has accelerated device development since the 1990’s. This is due to the ease of growing a wide range of n- and p-type doping as well as the capability to grow 4H- and 6H-SiC without any inclusions of other polytypes at a low growth temperature of 1500°C, which is over 300°C lower than preceding techniques [19, 56, 58]. Moreover, high-quality homoepitaxial growth technology using High Temperature Chemical Vapour Deposition (HTCVD) has progressed [59-62]. The first successfully grown SiC crystal

by HTCVD was introduced in 1996 [63]. Figure 2-10 illustrates a reactor and temperature profile used for HTCVD of SiC bulk, where the SiC boule is grown in a vertical crucible made of graphite and the seed crystal holder is located at the top. The precursor gases (SiH_4 and a hydrocarbon, such as C_2H_4 and C_3H_8, diluted in a carrier gas) are fed upward through a heating region to reach the seed crystal. The geometry of the vertical HTCVD reactor is similar to that of the vertical CVD, but the typical growth temperature is very high, around 2100–2300°C. The main benefits of using HTCVD compared to the sublimation technique are attaining high purity material, deliberately control of C/Si ratio, and constant supply of the source materials. Increasing the C/Si ratio [64, 65] and decreasing the growth pressure [66, 67] are the main means of attaining high purity grown material.

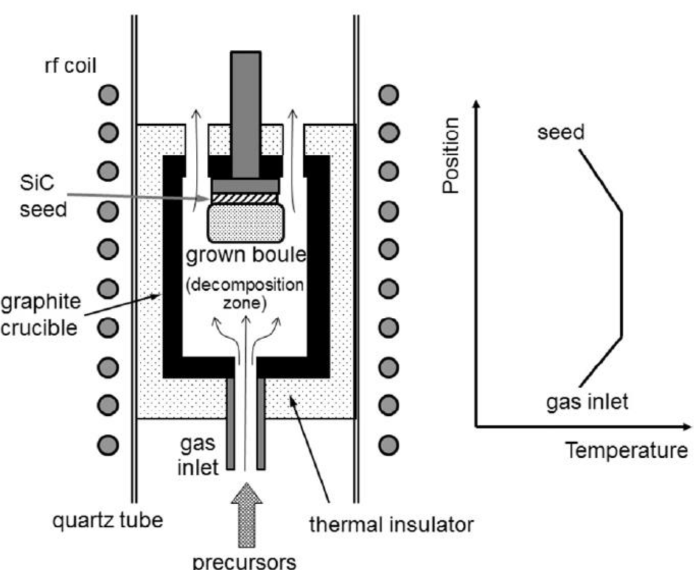


Figure 2-10: Core part of reactor and temperature profile used for SiC bulk growth by HTCVD.

Although the field of material growth has been significantly improved over the past few years, enormous dissimilarities in wafer quality are still present. Reducing the defects in wafers, improving the quality and uniformity of epitaxial layers and increasing the wafer size and thus driving down the price of SiC devices are the challenges that SiC wafer manufacturers are facing. Reducing the defect densities of SiC substrate is still a critical challenge and is continuing to hinder the development of large area high current and high voltage devices.

2.7 Extended Defects in SiC

A range of crystal imperfections, both extended defects and point defects (discussed in section 2.8), exist in SiC epitaxial wafers used for power device fabrication. The majority of extended defects in an epitaxial layer are duplicated from the bulk wafer (the underlying substrate), but a few are formed throughout the epitaxial growth process. In contrast, the substrate quality does not affect any of the point defects in an epitaxial layer. Instead, they are determined by the epitaxial growth conditions. However, additional extended and point defects are formed during various stages of device processing, for example during ion implantation and dry etching. To ensure the high performance of SiC power devices and their reliability, it is necessary to understand and control these defects.

Various extended defects are known to be detrimental to the reliable performance of SiC power devices such as micropipes (MP), basal plane dislocations (BPD), threading

screw dislocations (TSD) and threading edge dislocations (TED), which will be discussed in this chapter. Table 2-2 presents useful information on these main extended defects in SiC epilayers [1]. Figure 2-11 illustrates the schematic representation of dislocations in 4H-SiC epilayers which are grown on off-axis using CVD [24]. As the majority of dislocations in SiC epilayers originate from the substrates, the most important dislocations in SiC boule crystals are discussed in section 2.7.1.

Table 2-2: Major extended defects in SiC epilayers, TSD: threading screw dislocation, TED: threading edge dislocation, BPD: basal plane dislocation

Extended defects	**Major direction**	**Density in bulk wafers (cm^{-2})**	**Density in epitaxial wafers (cm^{-2})**
Micropipe	<0001>	0 – 0.1	0 – 0.1
TSD	<0001>	300 – 500	300 – 500
TED	<0001>	2000– 5000	2500 – 6000
BPD	in <0001> plane (mainly <11$\bar{2}$0>)	500 – 1000	0.1 – 1

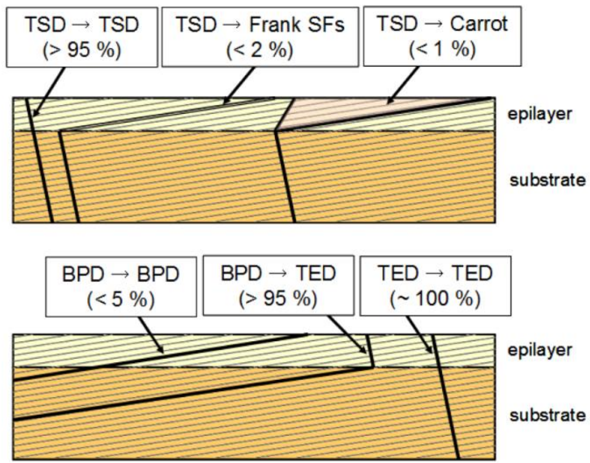


Figure 2-11: Schematic illustration of dislocation propagation in 4H-SiC epilayers grown on off-axis by chemical vapour deposition [24]

2.7.1 Dislocations in SiC Boule Crystal

A micropipe defect is the hollow core of a large screw dislocation [68, 69] and is a micron or submicron-size pinhole that penetrates along the ⟨0001⟩ direction through the entire SiC wafer. Micropipe defects are referred to as a `killer defect', since the SiC power devices that contain a micropipe display significantly degraded performance, such as an enormous leakage current and premature breakdown [70]. Hence, they have been eliminated or reduced to a reasonable level (<0.1 cm^{-2})[53, 71-73], and micropipe-free wafers are now commercially available from many vendors.

Dislocations result in energy levels within the bandgap, changing the recombination properties of the semiconductor material. It was first suggested by Shockley [1] that dangling bonds in the dislocation core could act as traps that

correspond to intermediate energy levels among the bonding states and free-electron states [74]. As discussed in [74], dislocations influence carrier transport properties of SiC epilayers such as carrier lifetime and diffusion length.

The two major types of dislocations in hexagonal SiC are: (1) “threading” dislocations, with the direction of dislocation line along <0001> and (2) “basal plane” dislocations with the direction of dislocation line being along $<11\bar{2}0>$. Thus, a BPD and threading dislocations have the same basic nature; the difference being the dislocation direction. Threading edge dislocation (TED) spreads from the surface of a strained layer, passes through the layer and penetrates the substrate or bends at the interface [75]. Basal plane dislocations are fairly easily generated in the growing boule (plastic deformation) when the set shear stress surpasses a certain (critical) value [76]. This stress is mainly due to developing thermal stress during sublimation growth of the material when the temperature profile is not suitable. Additionally, since the thermal expansion coefficients of SiC and graphite parts are different, major thermal stress occurs during cooling [74]. SiC epitaxial layers are normally grown on substrates that are cut 0.5 to 8° (typically 4°) off-axis in order to benefit from step-flow growth process. This means that with regard to the surface of the wafer, the basal plane of the crystal is tilted. As shown in Figure 2-11, BPDs can spread from the substrate into the epitaxial layer and are detrimental defects for bipolar 4H-SiC devices since they can act as the source of a Shockley-type stacking fault during carrier injection. This results in a significant reduction in the carrier lifetime, increasing on-resistance and giving rise to leakage current, thus compromising the reliability of 4H-SiC bipolar devices [1, 77]. It

is found that BPD to TED and TED to BPD conversions are normally seen inside boule crystals during epitaxial growth [1, 78, 79]. It was reported in [80] that conversion of BPDs into TEDs in epitaxial layers can be enormously decreased using “conversion epitaxial growth process” [74, 80].

The impact of threading screw dislocations (TSD) and TEDs on characteristics of power devices have been studied by several research groups. As illustrated in Figure 2-11, TSDs can spawn other defects. A TSD is placed at the centre of spiral growth throughout sublimation growth process on a SiC <0001> surface and typically propagates along the <0001> direction [28]. Available experimental data has revealed the impact of TSDs (as well as TEDs) on 4H-SiC power devices. It was reported in [81] that on SiC(0001) pn diodes, when the diode contained one TSD, the abrupt increase in the leakage current at a bias voltage slightly lower than the breakdown voltage was observed. Together with the increase in leakage current, a microplasma was instantaneously seen at the location of the TSD. Nevertheless, the existence of a single TSD barely had any impact on breakdown voltage of the device. Additionally, it was shown in [74, 81, 82] that the existence of a TSD fault in low-voltage pn and high voltage Schottky diodes results in high reverse leakage current and low reverse breakdown voltage and that both TEDs and TSDs act as recombination sites, therefore degrading the carrier transport properties of the material. It has also been reported that BPDs and TSDs have a negative impact on the gate oxide reliability of SiC MOSFETs by triggering the dielectric breakdown of the gate oxide and considerably damage the long-term reliability of SiC MOSFETs [83].

2.8 Point Defects

2.8.1 Major Deep Levels in SiC Epitaxial Layers

Another major defect in SiC epilayers is the point defect (also referred to as intrinsic defect), which creates a deep level in the SiC bandgap. Deep level transient spectroscopy (DLTS) measurements are usually carried out on SiC Schottky devices (or pn structures) to characterise deep levels. The density of deep levels in lightly-doped as-grown SiC(0001) epilayers can vary between $5 \times 10^{12} - 2 \times 10^{13}$ cm^{-3}, depending on the growth condition [1]. This is quite a low value for a compound semiconductor and is tolerable for the fabrication of unipolar devices, but it is not low enough for bipolar device applications, particularly when a long carrier lifetime is needed (around 5μs for thick epilayer). In the fabrication of power MOSFETs, deep levels formed by ion implantation are more relevant.

Figure 2-12 shows the energy levels of major deep levels detected in as-grown n- and p-type 4H-SiC epitaxial layers [84]. Among these levels, the $Z_{1/2}$ (EC – 0.63 eV) and $EH_{6/7}$ (EC – 1.55 eV) centres are the most prevalent defects and are extremely stable against annealing at high temperatures (~1700°C) [1]. These defects are generally witnessed with the maximum concentration of $(0.3 - 2)*10^{13}$ cm^{-3} in all as-grown epilayers grown by CVD. Other deep levels that can be observed in the bottom half of the bandgap are the HK2 (EV + 0.84 eV), HK3 (EV + 1.24 eV), and HK4 (EV + 1.44 eV) [85, 86] with typical densities in the range of $(1–4) \times 10^{12}$ cm^{-3} [1]. These centres almost

disappear when annealing at temperatures around 1450–1550 °C. Hence, the $Z_{1/2}$ and $EH_{6/7}$ centres are very important. Moreover, the HS2 centre (EV + 0.4 eV) converts to a main deep level when SiC is annealed and irradiated [86, 87].

As well as these levels, a few impurity-related levels (also referred to as extrinsic defects) are frequently seen in as-grown SiC epitaxial layers, such as boron and titanium (Ti). Boron is a typical impurity that can be unintentionally doped from reactor parts (such as graphite susceptors). Boron contamination generates the boron acceptor level [Ev + (0.28–0.35) eV] [88] and the boron-related "D center" (Ev + 0.55 eV)[1, 88]. Titanium is also created from graphite parts or pumping oil and generates very shallow electron traps (Ec − 0.11–0.17 eV) in 4H-SiC [89]. In CVD grown SiC epilayers, the typical impurity density for boron is around (0.5–5) × 10^{13} cm^{-3} and for titanium is about (0.5–5) × 10^{12} cm^{-3}.

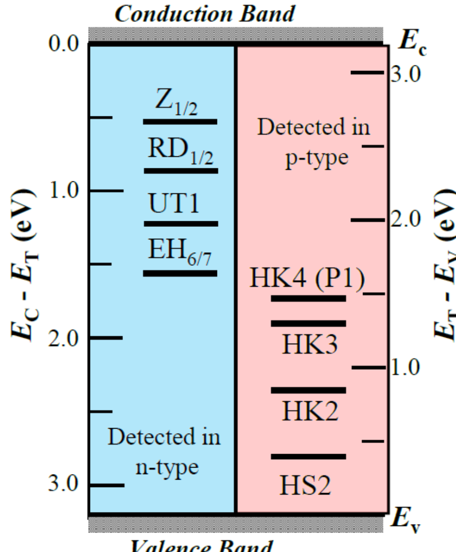


Figure 2-12: Energy levels of the main deep levels seen in as-grown n-type and p-type 4H-SiC epilayers [24]

Among the intrinsic defects seen in 4H-SiC, the main lifetime killing defect, at least for n-type 4H-SiC, is the $Z_{1/2}$ defect, which is considered to be a carbon vacancy-related defect, where no atom is present on the atomic sites [90]. In addition, the source of the $EH_{6/7}$ centre has also been recognized as a carbon monovacancy (V_C) with various charge states as discussed in [91-94]. It has been found that at $Z_{1/2}$ densities above (1–2) × 10^{13} cm^{-3}, there is an inverse correlation between the carrier lifetime and the $Z_{1/2}$ density, demonstrating that Shockley–Read–Hall (SRH) recombination governs the lifetime via the $Z_{1/2}$ centre[1]. However, the relationship between the $Z_{1/2}$ density and the carrier lifetime is not clear when the $Z_{1/2}$ density is in the range of 10^{11}–10^{12} cm^{-3}. Several recombination processes take place in a semiconductor, such as SRH recombination and multiple other recombination processes (discussed in Appendix C). The following equation (2-3) can be used to express the carrier lifetime (τ):

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{other}} \qquad (2\text{-}3)$$

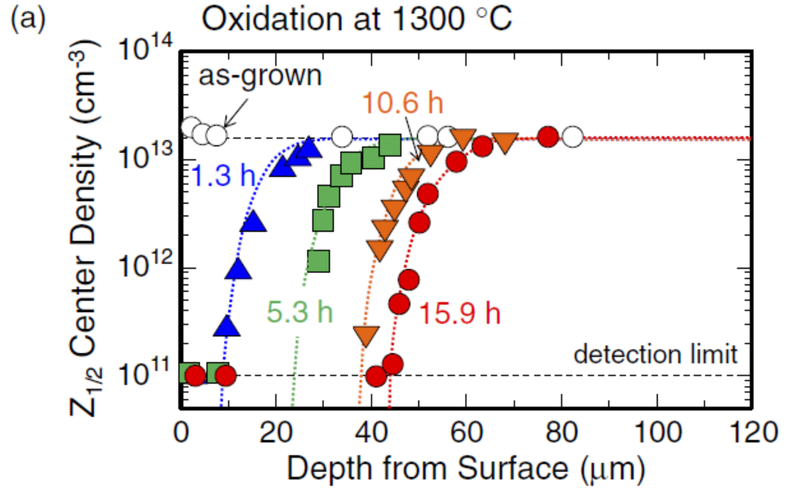
where τ_{SRH} is the SRH lifetime governed by recombination centres, and τ_{other} is the carrier lifetime governed by other recombination processes, such as surface recombination, Auger recombination, and recombination at extended defects [1].

Achieving a long carrier lifetime in bipolar devices results in the reduction of on-resistance. This can be attained by decreasing the density of the $Z_{1/2}$ centre to the order of 1 × 10^{12} cm^{-3} or lower. Two successful methods have been suggested to eliminate the $Z_{1/2}$ centre (or carbon vacancy). The first technique introduces extra carbon atoms from the outside (by carbon ion implantation) and the diffusion of these carbon atoms into

the bulk region is achieved using successive high temperature Ar annealing at 1650–1700 °C [95, 96]. As reported in [96], by using this technique, the $Z_{1/2}$ and $EH_{6/7}$ centres are both eliminated to below the detection limit (about 1×10^{11} cm^{-3} in this case). Since at temperatures above 1400–1500 °C, the diffusion coefficients of the generated carbon interstitials are large, the additional carbon interstitials diffuse and occupy the carbon vacancies, resulting in the elimination of the $Z_{1/2}$ and $EH_{6/7}$ centres from the surface region of 4H-SiC epilayers to the bulk. After the annealing process, the defective implanted area close to the surface is removed using plasma etching.

The second technique involves the elimination of the $Z_{1/2}$ and $EH_{6/7}$ centres using thermal oxidation of SiC under suitable conditions as discussed in [1, 2, 97]. A great number of the carbon atoms are eliminated during the thermal oxidation process due to the production of carbon monoxide (CO). However, some of them are emitted into the bulk area and diffuse very deep into the SiC material. Similar to the carbon ion implantation case, since the diffusion coefficient of the carbon interstitials is very large, the $Z_{1/2}$ and $EH_{6/7}$ centres can be eliminated to the depths exceeding 100 µm. This can be achieved by the combination of oxidation process and successive high-temperature Ar annealing or by high-temperature oxidation process at temperatures at the range of 1300–1400 °C [3]. Due to the exceptionally low diffusion coefficient in SiC, carbon vacancies (or $Z_{1/2}$ centre) are almost immobile during high-temperature oxidation or annealing process [1, 98]. Figure 2-13 illustrates the depth profile of $Z_{1/2}$ density obtained from an n-type 4H-SiC epilayer after thermal oxidation at 1300°C and 1400°C for different periods. According to these results, by increasing the oxidation time or the

oxidation temperature, the "$Z_{1/2}$-free" region spreading from the surface becomes thicker (to the depth of 100 μm or even higher) [3].



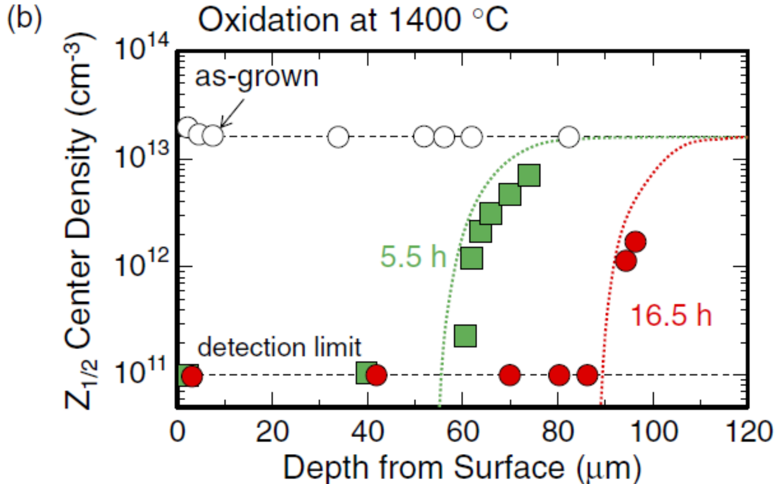


Figure 2-13: (Colour online) Depth profile of the $Z_{1/2}$ density for SiC epilayers after thermal oxidation at (a) 1300 and (b) 1400 °C for various periods. By increasing the oxidation time or the oxidation temperature, the "$Z_{1/2}$-free" region spreading from the surfac [1]

The carrier lifetime in p-type SiC is more complex than n-type. Since in p-type SiC, the Fermi level is near the valence band, the carbon vacancy defect must be positively charged [VC(+): EH7 centre] in equilibrium and therefore it is anticipated that the defect will rapidly trap any surplus electrons, resulting in the change of the charge state to neutral. The carrier lifetime of as-grown p-type SiC epitaxial layers is normally around 1 μs, which has been reported to increase to about 2–3 μs after C implantation or high-temperature oxidation process (the carbon-vacancy reduction method)[1, 99, 100]. Unlike n-type SiC, the measured lifetimes appear to be more sensitive to the surface passivation. The work by Okuda et. al in [100] details that a long carrier lifetime of 10 μs has been achieved for lightly-doped p-type SiC epilayers using the carbon-vacancy reduction method and successive hydrogen annealing at 1000 °C for 10 min. It should be noted that due to the effect of surface recombination, the measured lifetimes are extremely underrated, particularly when the lifetime is long[101].

2.9 Present Status of Silicon Carbide Power Devices

As presented earlier, Figure 2.9 shows the voltage rating of Si and SiC power devices. It is anticipated that SiC unipolar devices such as Schottky barrier diodes and MOSFETs will offer a competitive alternative to Si bipolar devices such as IGBTs, as unipolar devices exhibit exceptionally low transient losses. SiC bipolar devices are promising for Ultra High Voltage (UHV) applications (>10 kV) where Si power devices

are impractical. However, in the low voltage region (<600 V), if the device is used in a normal environment, the use of SiC power devices is not promising due to the fact that Si can achieve a lower on-resistance. However, in harsh environment applications such as high temperature conditions or high radiation environment, SiC devices may still be attractive.

The diode is a fundamental semiconductor device, consisting in its simplest form, of a *pn* junction which allows the flow of current in one direction and blocks it in the reverse direction. In this work, the high voltage applications that are relevant to PiN and Schottky diode are studied. Being the subject of this thesis, a comprehensive discussion of the theory of high voltage PiN and Schottky diodes are given in Chapter 3.

2.9.1 Schottky Barrier Diodes (SBDs)

Schottky barrier diodes have a very simple structure as shown in Figure 2-14, where a Schottky contact is formed on an epitaxial layer. SBDs are expected to be used at voltages of 600V and over, replacing Si PiN diodes. Due to the unipolar nature of SiC Schottky device and the fact that there is a very little minority charge stored in these devices, their switching frequency is significantly higher than Si PiN diodes of equivalent voltage rating. In a comparative study between Si PiN diode and SiC Schottky diode, the reverse leakage current of SBD was 17 times less than in Si [24]. In addition, the on-state voltage drop of the SBD was significantly lower than that of

Si making the losses of this device much lower both in conduction and in blocking mode [24].

The first 400V rated 6H-SiC SBD was reported in 1992 [102] and in 1993, SBDs with breakdown voltage of over 1 kV were demonstrated [103]. In 1996, by changing the SiC polytype to 4H-SiC, SBDs with a breakdown voltage of 1.75 kV and specific on-resistance of 5 mΩcm^2 (far below their Si unipolar counterpart) were realized [104]. In 2001, the first SiC Schottky barrier diodes with blocking voltage of 600V and current rating of up to 10 A appeared on the market by Infineon. Nowadays, commercial SiC based Schottky diodes are available in the market for voltage ratings of 900 V, 1200 V, 1800 V, and up to 3300 V from a wide range of manufacturers such as Wolfspeed, Rohm, and ST microelectronics.

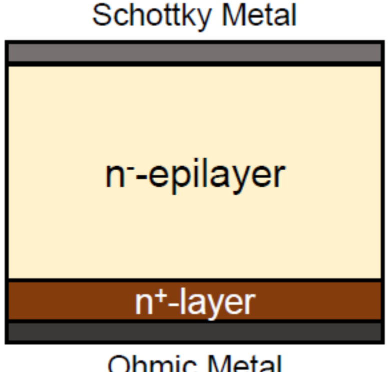


Figure 2-14: Schematic cross-section a Schottky barrier diode.

After SBD was first commercialization in 2001, various problems had to be resolved to improve its performance even more, such as the large reverse leakage current of this device. After reverse current-voltage measurement of SiC SBD was studied, it was found that the practical leakage current density was several orders of magnitude higher than the expected value using the thermionic emission (TE) model and barrier height lowering (which is the standard model for Si Schottky barrier diode and will be discussed in chapter 3) [105]. It was initially presumed that the high leakage current was due to the existence of defects in the crystal. However, Hatakeyama et al. reported in [106] that electron tunneling (discussed in detail in chapter 3) at the Schottky barrier interface is the predominant reason for the leakage current in SiC SBDs, as SiC has 10 times larger critical electric field strength compared to Si at Schottky interface. The leakage current was modelled using a Thermionic Field emission (TFE) model as it was determined that the leakage current in SBDs fabricated on high-quality GaN(0001) can also be replicated using the TFE model [107]. Therefore, the TFE current is dominant in SBDs formed on any wide-bandgap material that has a high electric field strength, such as SiC, GaN, gallium oxide (Ga_2O_3), and diamond [1]. As well as the TFE current, Fujiwara et al. have reported that the existence of threading dislocations at the Schottky interface also increase the leakage current [108, 109]. In this case, a threading dislocation itself does not result in an increase in the leakage current, but the shallow nano-pit (~45 nm-depth) detected right above the dislocation causes electric field crowding at reverse bias, which then results in a large leakage current.

Numerous studies have sought to improve the performance of high voltage SiC SBDs [110]. In April 2015, GeneSiC reported a small current rating SBD with voltage rating of 8 kV and a small Qrr of 8 nC. The on-state voltage drop of this device was reported to be 4.5 V at 50 mA which is far from the ideal values which makes them ideally suitable for low current applications. SiC Schottky diodes with 3300 V peak reverse voltage rating have recently been made available on the market by GeneSiC semiconductor, with 6.5 A continuous forward current (I_F at T_C=135 °C).

2.9.2 Junction Barrier Schottky Diodes (JBS)

As previously discussed, the reduction of the leakage current in SBDs to improve the device performance is vital. An effective approach to reduce the leakage current of SiC SBDs is to minimize the electric field strength near the Schottky barrier interface with the intention that the potential barrier does not get too thin. As such, the traditional Schottky diode has largely given way to a hybrid combination of the unipolar and bipolar diodes, known as the merged PiN-Schottky (MPS) or junction-barrier Schottky (JBS) [111, 112] as well as several other diode structures such as a trench Schottky barrier diodes (or trench JBS)[113]. In JBS diodes, the surface electric field at the metal-semiconductor interface can be reduced by forming regularly space P^+– regions under the Schottky contact. This will reduce the effect of surface defects which increase the leakage current in Schottky diodes until the device is no longer capable of blocking the required voltage [114]. Most commercial Schottky diodes are JBS diodes. Table 2-3 shows some of the commercially available SiC Schottky diodes today.

Table 2-3: Commercial SiC Schottky diodes with reverse blocking voltage range of 600 V to 3300 V. VF (max) and IR (max) are measured at 25°C.

Manufacturer	V_R	$V_{F\,(max)}$	I_F @ $V_{F\,(max)}$	$I_{R\,(max)}$ @ V_R
Wolfspeed	600 V	1.8 V	10 A	50 μA
	1200 V	1.8 V	5 A	150 μA
	1200 V	1.8 V	20 A	200 μA
	1200 V	1.8 V	50 A	500 μA
Infineon	600 V	2.1 V	12 A	100 μA
	1200 V	1.65 V	40 A	332 μA
On Semiconductor	650 V	1.75 V	10 A	40 μA
	650 V	1.7 V	20 A	40 μA
	1200 V	1.75 V	30 A	200 μA
	1200 V	1.75 V	50 A	200 μA
GeneSiC	3300 V	2.2 V	0.3 A	10 μA
	3300 V	3 V	5 A	10 μA @ 3 kV

2.9.3 Merged PiN-Schottky Diodes (MPS)

Since 2005, Infineon have employed the MPS device structure within their commercial 600 V SiC diodes [115] and their 1200 V SiC diodes since 2012 (5th generation SiC MPS diode with improved performance and ruggedness) reported in

[116]. In Figure 2-15 the structure of a SiC Schottky diode is compared with the 600 V concept where the MPS structure is considered as multiple parallel connected PiN and Schottky diodes, offering unipolar-like behaviour at low voltage before bipolar action becomes dominant at high voltage, effectively lowering the R_{ON}. The p-type islands (or stripes) are locally formed underneath the Schottky contact using aluminium ion implantation. At a high reverse bias voltage, the space-charge regions extending from the pn junctions (p-type island/n-type drift layer) merge, result in the reduction of the electric field strength near the Schottky interface [1]. The spacing and width the p-type island or trench are crucial, since otherwise the space-charge regions can extremely increase the on-resistance.

However, their benefit is greater than just this and Infineon have detailed at length in [115, 116], such as improved surge current capability and avalanche ruggedness. The further benefit that the p-type implants offer in maximising the breakdown voltage by shielding the metal-semiconductor interface from the peak of the field stress [113], and in introducing a stable and rugged avalanche behaviour.

There are however, several implementations of these MPS devices, all with varying architectures. For just the simple structure in Figure 2-15(b) alone, the proportion of p-type coverage varies the degree of bipolar action and the avalanche ruggedness. However, introducing higher n-type doping around the p-type implants can lower on-resistance and enhance current spreading [116].

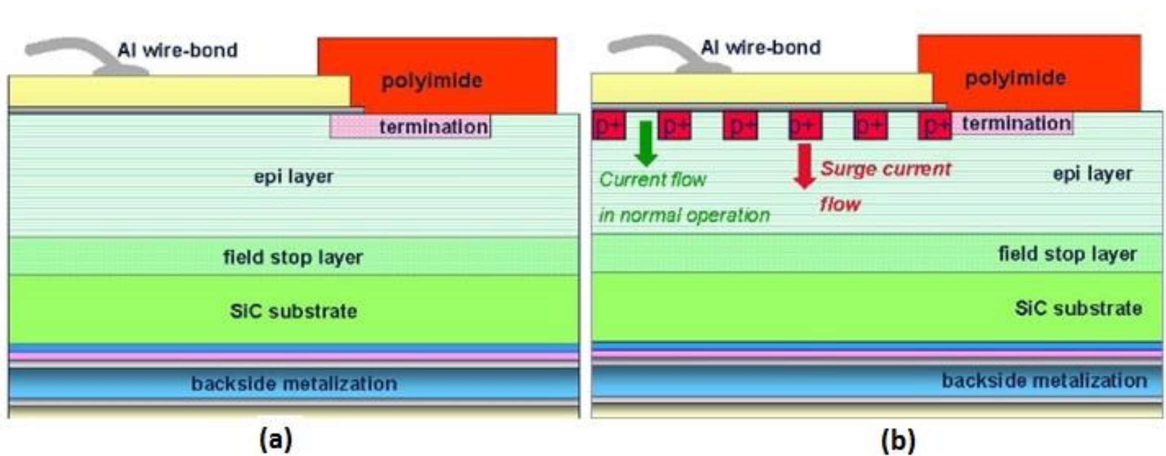


Figure 2-15: (a) Schematic cross section of conventional SiC Schottky diode, (b) SiC diode with merged p-doped islands (MPS diodes) [112]

Figure 2-16 shows the schematic drawing of 1200 V MPS diode by Infineon which employs a hexagonal MPS cell structure in the active area to deliver an improved shielding of the electric field from the Schottky interface. This subsequently allows a higher n-doping in the epi layer which results in a reduced differential resistance per chip area compared to Infineon's previous generation of SiC diodes [116]. Furthermore, surge current ability was tremendously improved rated up to 14 times the nominal current guaranteeing robust diode performance during surge current events in the application. Unlike other generations of 1200V SiC diodes, this is a more avalanche rugged device. This is because each cell contributes to the avalanche.

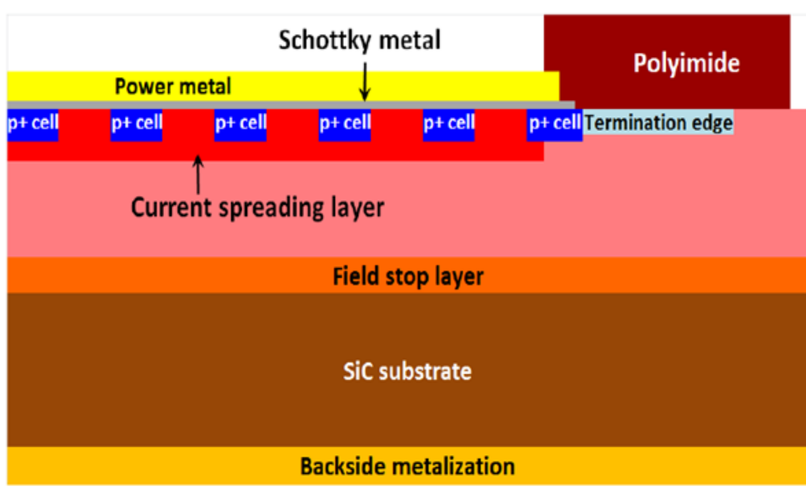


Figure 2-16: Schematic drawing of 1200V MPS with current spreading layer [113]

2.9.4 PiN Diodes

PiN diodes consist of ultra-low doped or intrinsic semiconductor sandwiched between two heavily doped P and N type semiconductors. 4H-SiC PiN diodes are desirable for high voltage power electronics given their potential to significantly decrease switching power losses and increase high voltage blocking ability compared to Si PiN diodes. On state losses will also be much lower at higher voltages, and current (power) handling capacity will be improved, as SiC can be operated at a higher current density. In UHV applications where breakdown voltages over 10 kV are required, even SiC SBDs cannot escape from a high on-resistance that results in large conduction losses. A schematic structure of a PiN diode is shown in Figure 2-17.

Ohmic Metal

p^+-anode

n^--epilayer

n^+-layer

Ohmic Metal

Figure 2-17: Schematic structure of PiN diode

The on-state resistance of these devices is low due to the conductivity modulation of bipolar devices which operate based on the high-level injection of minority carriers. In SiC material, the carrier lifetime of minority carrier, which dictates the density of minority carriers in the device, needs to be increased in order to reduce on-state losses. This is the main roadblock in the commercialisation of SiC PiN diodes, alongside the cost and throughput of the necessary thick epitaxial layers. There are a handful of reports on the development and early prototypes of PiN diodes with voltage rating exceeding 8 kV[117]. In 2013, CREE reported development of a PiN diode on 4H-SiC with voltage rating of 16kV. The current density reported was between 350-400 A/cm^2 and the die area was 10 mm^2 [118]. GeneSiC reported their work on development of 8 kV/1 A, 10 kV/2 A and 15 kV/2 A PiN diodes using 4H-SiC. Due to high defect density on the substrate of these devices, the power die area was limited to maximum of 2.4 mm^2 [117].

In 2015, Kyoto University also reported the development of 26.9kV PiN diode with current capability of 100 A/cm^2 [119], on-state resistance of 9.7 mΩ cm^{-2} and carrier lifetime of 3.3 µs which was achieved through lifetime enhancement techniques using thermal oxidation. The epi-layer thickness in this diode was 268 µm. In 2018, Nakayama et al. reported their work on fabrication of ultra-high voltage 4H-SiC PiN diodes with 27.5 kV breakdown voltage and Space-Modulated JTE (SM-JTE) [120]. This is by far the largest breakdown voltage reported for 20 A class 4H-SiC PiN diodes. Figure 2-18 shows the device structure of developed UHV 4H-SiC PiN diode with two-zone and space-modulated Junction Termination Extension (JTE). Moreover, Table 2-4 shows the state of the art 4H-SiC PiN diodes reported by both semiconductor device manufacturers and academic research groups.

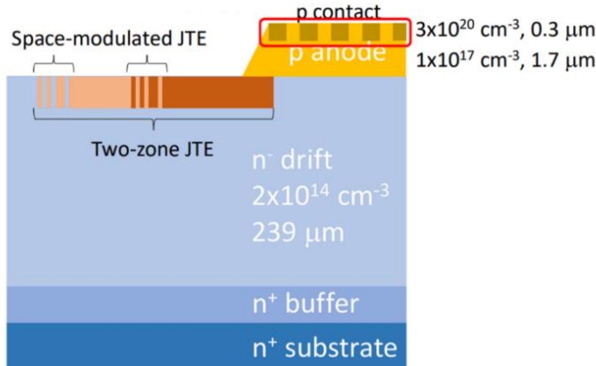


Figure 2-18: : Device structure of developed UHV 4H-SiC PiN diode with two-zone and space-modulated JTE. The active area of the diode is 5.75 mm2 [119]

Table 2-4: State of the art 4H-SiC PiN diode devices reported by device manufacturers and research institutes

Company						
Company	**Technology**	**V_{BR}**	**Current/ Current density A, A/cm²**	**Chip Size**	**Miscellaneous**	**Ref.**
GeneSiC	PiN diode on 4H-SiC	8 kV	1A	-	-	[117]
GeneSiC	PiN diode on 4H-SiC	10 kV	2A	-	-	[121]
GeneSiC	PiN diode on 4H-SiC	15 kV	2A	2.4mm²	-	[117]
Cree	PiN diode on 4H-SiC	16 kV	350-400 A/cm²	10mm²	120 µm n-type epi-layer	[118]
Research institute						
Acreo Swedish ICT	PiN diode on 4H-SiC	10 kV	-	3	110 µm n-type epi-layer used for soft-switching converter application	[122]
Kyoto University	PiN diode on 4H-SiC	26.9 kV	100 A/cm²	-	48 to 268 µm epi-layer	[119]
National Institute of Advanced Industrial Science and Technology	PiN diode on 4H-SiC	27.5 kV	20 A	-	5.75 mm² PiN diode active area	[120]

Chapter

3 Theory of High Voltage Power Diodes

In this Chapter, the theoretical concepts related to the design of PiN diodes and Schottky diodes are presented. The fundamental operating principles of these devices are outlined which are important for design and optimisation of device structures. These concepts will subsequently be applied in the following Chapters.

3.1 Power Diode Operation Principle

With the emergence of wide bandgap semiconductors such as SiC, high blocking voltage and fast switching Schottky diodes are becoming more common in power electronic applications where high switching frequency is important.

A cross section of a Schottky diode (or a junction barrier diode) is shown in Figure 3-1 illustrating its rectifying contact at one side of the device (Anode) and its Ohmic contact at the other side (Cathode). Ideally there is no potential between the

metal and the semiconductor on the bottom side of the device. The built-in potential across the open circuit Schottky barrier diode describes the characteristics of this type of diode. As shown in this Figure, in the open-circuit condition, the depletion region formed in the semiconductor at the metal-semiconductor contact depends on the doping of the semiconductor, the type of the metal used on the Schottky contact, and also explains the relationship between the built-in potential and the thickness of the depletion region in an open circuit condition.

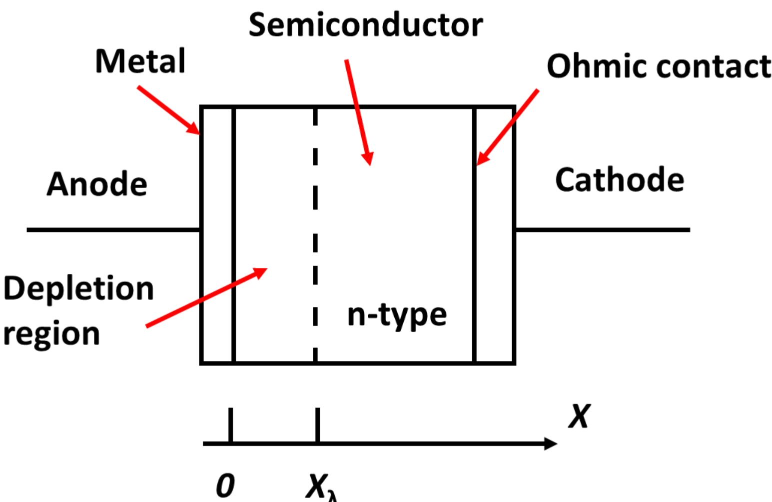


Figure 3-1: Cross-section view of a Schottky diode

During the on-state, the current flow consists only of majority carriers which are electrons in an N-type semiconductor. In power electronics, N-type Schottky diodes are preferred as the mobility of electrons is significantly higher than that of holes and this results in a much lower on-state voltage drop across the semiconductor. The current flowing through the Schottky diode consists of other components, such as: the diffusion current (due to the carrier concentration gradient for electrons), the tunnelling current

(due to quantum mechanical tunnelling through the Schottky barrier) and the thermionic emission current (due to thermal agitation of some carriers which cause them to have equal or larger energy than the conduction band energy to the metal-semiconductor interface). Current transport mechanism is discussed in detail in Section 3.3.1.

The PiN diode is an alternative device structure for high-voltage devices. These are vertical devices (the current rating of the device is proportional to its area, and the voltage blocking capability is achieved in the thickness of the die) with an extremely low doped N-type drift layer sandwiched between a highly doped P-type anode, and a highly doped N-type cathode. The drift layer is used to block the voltage during the off-state. There are effectively two junctions between these layers: P^+N^- and N^-N^+ junctions. Figure 3-2 shows a cross section view of a PiN diode.

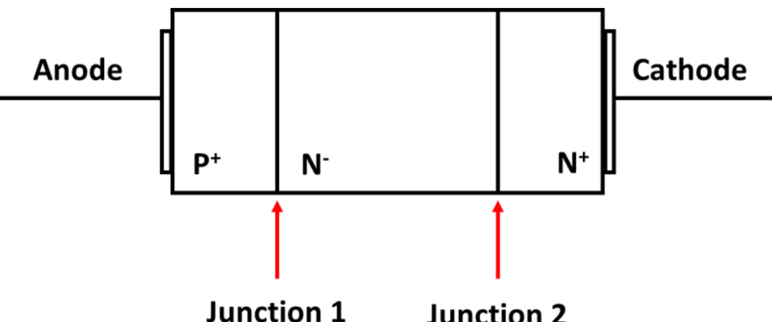


Figure 3-2: Cross section view of a PiN diode

When the diode is forward biased, the current is carried from Anode to Cathode by diffusion of electrons and holes from the highly doped N+ and P+ regions respectively. Due to the diffusion of carriers into the N-drift region and the high-level injection of minority carriers in this region, the on-state resistance of the device reduces significantly during the on-state operation of the PiN diode. This is known as conductivity modulation which is the basis of operation of bipolar devices such as PiN diode and IGBT. The amount of charge that is stored in the drift region of a PiN diode, depends on the diffusion length of the carriers and the lifetime of the minority carriers in this region.

During the turn-off process of a PiN diode, the charge stored in the drift region needs to be extracted from both ends of the drift region. During this charge extraction, the direction of current is reversed, and the current becomes negative. This is known as reverse recovery of the PiN diode which largely dictates the losses during the turn-off transient of a PiN diode. The reverse recovery of a PiN diode is also one of the main reasons that the switching speed of such devices can be a major issue. The reverse recovery of a PiN diode can be adjusted by reducing the carrier lifetime in the charge storage region. This reduction in carrier lifetime increases the on-state losses of the device due to lower concentration of minority carriers which are the dominant contributors in the on-state of the PiN diode. Hence, there is a trade-off between the optimisation of reverse recovery of the diode and the on-state resistance of the diode.

These were brief explanations of operation of PiN diodes and Schottky diodes. The detailed operation of these devices can be elaborated by explaining the physics of

semiconductors. The following section describes the physics behind the operation of a P-N junction which is the basic building block in any semiconductor switching device.

3.2 P-N Junction

A P-N junction consists of a P-type semiconductor in contact with an N-type semiconductor and allows a unidirectional current flow device. A one-dimensional structure of a P-N junction structure is shown in Figure 3-3.

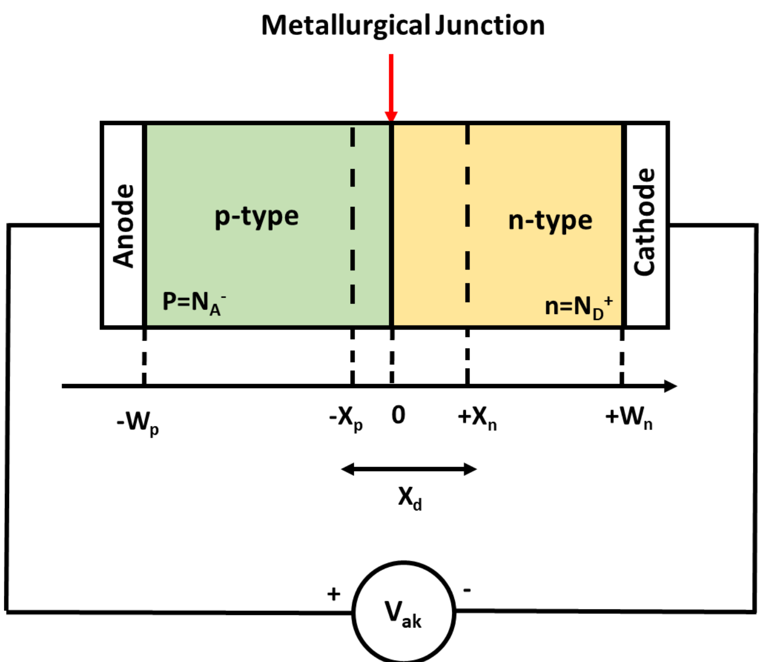


Figure 3-3: A diagram of P-N junction structure

This structure is a fundamental part of most power electronic devices. To simplify the operation of a P-N junction, it is assumed that the doping of N-type and P-type semiconductor is uniformed across the P and N regions and the transition between

the P-type and N-type semiconductor at the junction is abrupt. The metallic contacts shown at both ends of the device are Ohmic contacts. Three different scenarios can be assumed depending on the applied bias to simplify the operation of the junction in each case:

The voltage applied across the P-N junction is at equilibrium (V_{AK}=0V): in thermal equilibrium, electrons diffuse to the P-type semiconductor and holes diffuse to the N-type semiconductor region. Consequently, a region depleted from carriers is formed across the junction (referred to as depletion region). An electric field is thus established at the junction by the uncompensated charge of the remaining ions in the depletion region. This electric field opposes further transition of electrons and holes until an equilibrium state is achieved. The built-in voltage (V_{bi}) of a P-N junction depends on the doping of the N-type and P-type semiconductor (N_D and N_A respectively) and is temperature dependent. The following equation shows this relation:

$$V_{bi} = V_T ln \frac{N_A N_D}{n_i^2} \quad (3\text{-}1)$$

where both thermal voltage ($V_T = kT/q$) and intrinsic carrier concentration (n_i) are temperature dependent and thus V_{bi} is also temperature dependent. Therefore, the built-in voltage decreases with increasing temperature.

Figure 3-4 shows the energy band diagram of a p-n junction in thermal equilibrium where the depletion region is extending from $x = -x_p$ to $x = x_n$. While no external voltage is applied across the n-type and p-type material, there is an internal

potential, V_{bi} (built in potential), which is due to the difference in the work function between the n-type and p-type semiconductors.

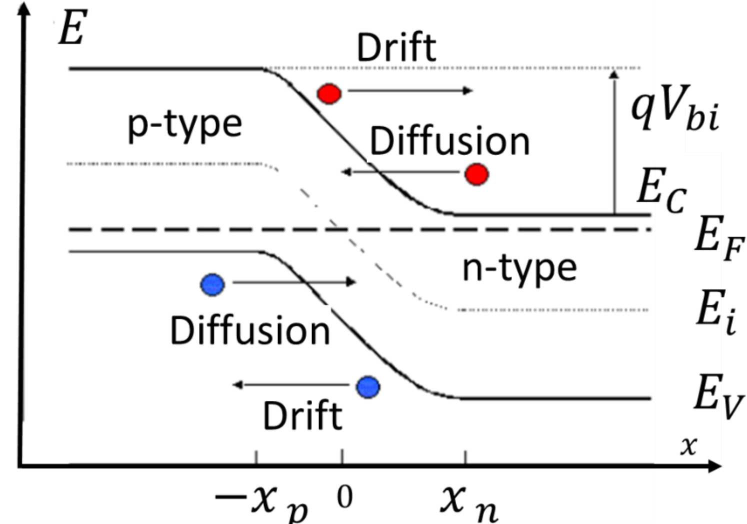


Figure 3-4: Energy band diagram of a p-n junction in thermal equilibrium.

As shown in Figure 3-5, the depletion width during equilibrium can be calculated using the peak electric field (E_0) at the junction as below:

$$E_0 = -\frac{qN_D x_n}{\varepsilon_s} = -\frac{qN_A x_p}{\varepsilon_s} \tag{3-2}$$

$$x_d = x_n + x_p = -\frac{\varepsilon_s E_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right) \tag{3-3}$$

In this Figure, it is assumed that the doping of the P-type is slightly higher than the doping on the N-type and hence, the depletion widths are different on each side of the P-N junction. The electrostatic potential can be calculated by integrating the area underneath the electric field across the P-N junction at equilibrium:

$$V_d = -\frac{E_0 x_d}{2} = \frac{q x_d^2}{2\varepsilon_s}\left(\frac{N_A N_D}{N_A+N_D}\right) \quad (3\text{-}4)$$

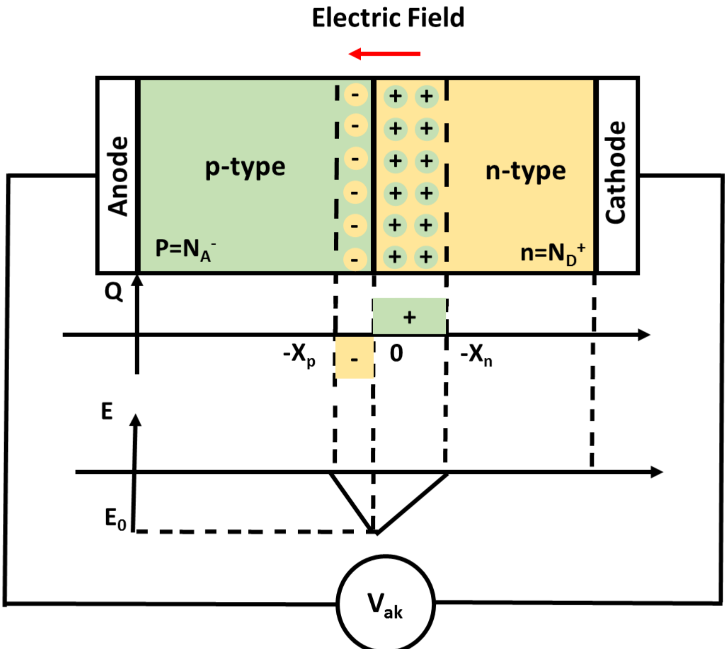


Figure 3-5: Built-in potential at P-N junction when no voltage is applied to the structure.

The voltage applied across the P-N junction forward biases the diode (V_{AK}>0V): under forward bias of a P-N junction, the depletion width starts shrinking and current starts flowing from Anode to Cathode. The width of the depletion region across the P-N junction during this transient is voltage dependent ($V_d = |V_{ak} - V_{bi}|$) and has the following relation with the voltage and doping of P and N regions:

$$x_d = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right).|V_d|} \quad (3\text{-}5)$$

The voltage applied across the P-N junction reverse biases the diode (V_{AK}<0V): in reverse bias, the P-N junction blocks the voltage across it by expanding the depletion

width across the device. Equation 3-5 is again applicable to the depletion width with respect to the voltage applied across the structure. The maximum blocking voltage across the device depends on the semiconductor permittivity, the doping of the material on each side of the junction as well as the width of the depletion region of the device. During reverse bias, impact ionisation process occurs where due to high electric fields in the depletion region, carriers gain enough kinetic energy to generate electron-hole pairs due to collisions with lattice atoms. The generated carriers gain sufficient energy to create further electron-hole pairs. This can increase carrier density and once the rate of this process tends to infinity, "avalanche breakdown" happens. At this point the electric field value is referred to as the critical electric field. Figure 3-6 shows the energy band diagram of a p-n junction under forward and reverse bias.

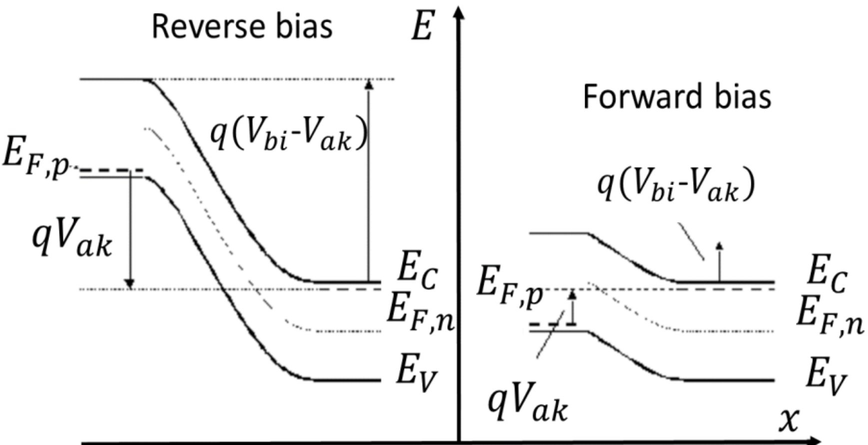


Figure 3-6: Energy band diagram of a p-n junction under forward and reverse bias

3.3 Schottky Diode

As discussed earlier, a Schottky diode is desirable for its low forward voltage drop and fast switching characteristic compared to PiN diodes. In particular, SiC Schottky diodes are increasingly being used in high power applications where faster switching speed is crucial in downsizing the system. A typical Schottky diode replaces the P-type semiconductor on a P-N junction with a metal contact to create a Schottky metal-semiconductor junction. Figure 3-7 shows the energy band diagram for a metal and N-type semiconductor in isolation. Generally, the position of the Fermi level in the metal and semiconductor will not have similar energy values, for example in Figure 3-7, the Fermi level in the metal lies below the Fermi level for the semiconductor.

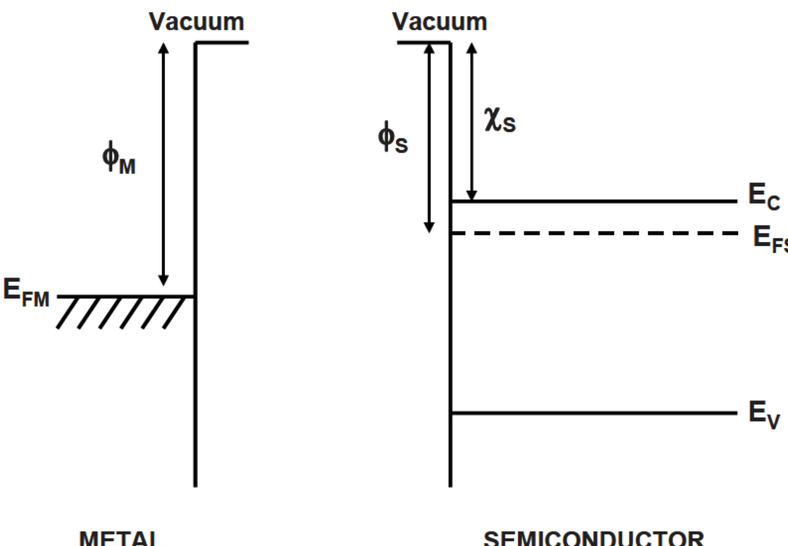


Figure 3-7: Energy band diagram for a metal and semiconductor when they are isolated from each other.

The work function of the metal (Φ_M) is the energy needed for an electron to move from the Fermi level position in the metal (E_{FM}) to a state of rest in free space outside the surface of the metal. The work function for the semiconductor (Φ_S) is the energy needed for an electron to move from the Fermi level position in the semiconductor (E_{FS}) to a state of rest in free space outside the surface of the semiconductor [44]. As no electrons are found at the Fermi level in the semiconductor, an electron affinity for the semiconductor (χ_S) is defined as the required energy required for an electron to move from the bottom of the conduction band in the semiconductor (E_C) to a state of rest in free space outside the surface of the semiconductor [44]. The equation below shoes the relationship between the work function and electron affinity for the semiconductor:

$$\Phi_S = \chi_S + (E_C - E_{FS}) \tag{3-6}$$

The potential difference between the Fermi level in the semiconductor and the Fermi level in the metal is referred to as the contact potential (V_C) which is expressed by the equation below

$$qV_C = (E_{FS} - E_{FM}) = \Phi_M - \Phi_S = \Phi_M - (\chi_S + E_C - E_{FS}) \tag{3-7}$$

After an electrical connection between the metal and the semiconductor is made, electrons are moved from the semiconductor to the metal as a result of their higher energy until thermal equilibrium is reached. This transfer of electrons from the semiconductor to the metal generates a negative charge in the metal and a positive charge in the depletion region created at the semiconductor surface. Figure 3-8 illustrates the metal-semiconductor band structure as the metal-semiconductor contact

is formed. The contact potential is now sustained within the depletion region created at the surface of the semiconductor, also known as the built-in potential of the metal–semiconductor contact. The Schottky barrier between the metal and semiconductor can be identified by an energy band diagram as shown in Figure3-8. The Fermi energy of the semiconductor and the metal when the junction is created yields this flatband diagram. The barrier height of the Schottky junction is the potential difference between the Fermi energy of the metal and the band edge where the majority of the carriers in the semiconductor reside. The relationship between the Schottky barrier height and the built-in potential can be expressed by

$$\Phi_{BN} = qV_{bi} + (E_C - E_{FS}) \tag{3-8}$$

The following equation shows the relationship between the barrier height (Φ_{BN}), the work function of the metal (Φ_M) and the electron affinity (χ_S)

$$\Phi_{BN} = \Phi_M - \chi_S \tag{3-9}$$

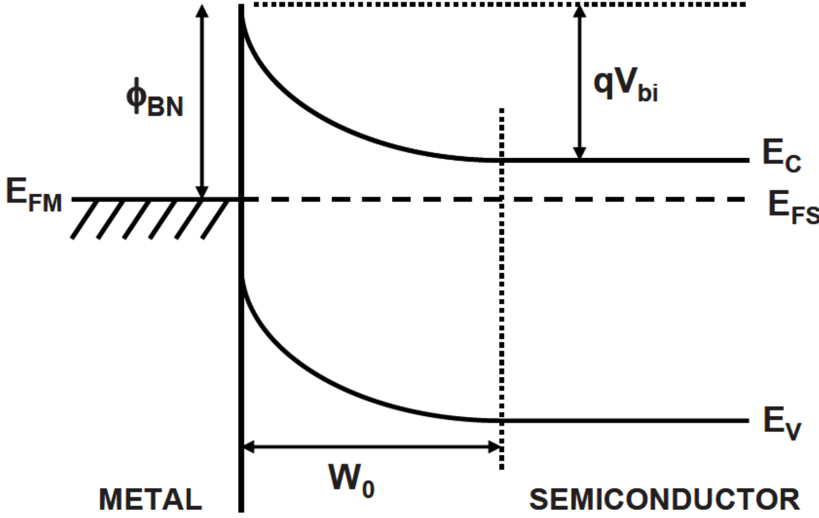


Figure 3-8: Energy band diagram for a metal and a semiconductor after the contact is made

In addition, a metal-semiconductor junction creates a barrier for carriers if the Fermi energy of the metal is between the conduction and valence band edge. The barrier height of a Schottky junction can be measured or calculated, however, there are slight differences between the measured values for different metals and calculated values. This is due to the detailed behaviour of the metal-semiconductor surface. To simplify the calculations, it is usually assumed that both materials at the metal-semiconductor junction are pure, there is no reaction between the two materials in contact and hence no unwanted interfacial layer exits. However, chemical reactions between the metal and the semiconductor at the interface affect the barrier height.

3.3.1 Current Transport Processes

Unlike the p-n junctions, Schottky contacts are unipolar and majority carriers are responsible for the vast majority of current flow. The current across a metal-semiconductor junction under forward bias is due to five distinct mechanisms: (1) thermionic emissions (TE) of carriers across the Schottky barrier. Thermionic emission is the transport of electrons from the semiconductor into the metal over the potential barrier and is the dominant process for Schottky diodes with moderately doped semiconductors (for example, Si with $N_D \leq 10^{17}$ cm^{-3}) operating at temperatures around 300 K. (2) quantum-mechanical tunnelling of the carriers through the Schottky barrier (vital for heavily doped semiconductors and responsible for most ohmic contacts), (3) the transport of electrons and holes into the depletion region followed by their recombination (referred to as the recombination current), (4) diffusion of carriers from the semiconductor into the metal (electrons travel from the bulk to take the place of those that have travelled over/through the barrier), (5) the transport of injected holes from the metal that diffuse into the neutral region of the semiconductor followed by recombination (referred to as the minority carrier current).

Thermionic emission (TE) is the dominant current transport mechanism in Schottky contacts at room temperature. The combination of the other current transport mechanisms results in a departure from ideal behaviour. According to thermionic emission theory, only carriers that have enough energy, higher than the potential barrier, can mount the barrier and generate the diode current, provided they move

towards the barrier. Although, some diffusion can also happen over the barrier, TE is the dominant factor to current flow. However, under reverse bias, the barrier that majority carriers have to overcome is too great, hence, only minority carrier leakage passes.

Under forward bias, the thermionic emission theory can be used to describe the current flow across the Schottky barrier interface for power rectifiers with low doping concentrations [42, 123]:

$$J = A^{**}T^2 \exp(-\frac{q\emptyset_{BN}}{kT})\left(\exp\left(\frac{qV_{ak}}{kT}\right) - 1\right) \quad (3\text{-}10)$$

where A^{**} is the Richardson's constant, T is the absolute temperature Boltzmann's constant, and V_{ak} is the applied bias. The saturation current is defined as

$$J_S = A^{**}T^2 \exp(-\frac{q\emptyset_{BN}}{kT}) \quad (3\text{-}11)$$

And the effective Richardson's constant for thermionic emission is given by [42, 123]:

$$A^{**} = \frac{4\pi q m^* k^2}{h^3} \quad (3\text{-}12)$$

where m^* is the mass of electron and h is the Planck's constant. For free electrons the Richardson's constant is 146 A/cm^2-K^2.

Electrons with energies lower than the barrier height can tunnel through the barrier by an effect known as the quantum-mechanical tunnelling. This phenomenon takes place in heavily doped semiconductors, used to make ohmic contacts, in which the Fermi level is above the bottom of the conduction band, and the depletion region is exceptionally thin, less than 3nm thick. This barrier appears invisible to the carriers

and they can pass through it in both the forward and reverse directions. Field Emission (FE) is a pure tunnelling process near the Fermi level. Thermionic Field Emission (TFE) is tunnelling of thermally excited carriers which see a thinner barrier than TE. TFE occurs at an energy level between TE and FE. This is shown in Figure 3-9 [42]. The tunneling probability rises with increasing temperature up until it reaches a maximum value at a certain energy level (E_m). From this point, if the temperature increases, TFE slowly decreases until it becomes insignificant, while the TE starts to dominate due to the increasing number of thermally excited electrons that are able to cross over the barrier [124]. In case of moderately doped semiconductor, quantum-mechanical tunnelling is only anticipated in reverse bias by means of TFE mechanism at the top of the barrier where the barrier thickness gets thinner and thinner with the applied voltage.

The characteristic tunneling energy of the semiconductor is given by[125]:

$$E_{00} = \frac{qh}{2}\sqrt{\frac{N_d}{m_T^* \epsilon_S}} \quad (3\text{-}13)$$

where h is Planck's constant, m_T^* is the tunneling effective mass and N_d is the donor concentration express in m^{-3}.

Hence the current due to field emission under forward bias can be expressed as [42, 123],

$$J_{FE} = \frac{A^{**}T\pi \exp[-q\ (\emptyset_{BN} - V_{ak})/E_{00}}{c_1 k \sin(\pi c_1 kT)}[1 - \exp(c_1 q V_{ak}) \quad (3\text{-}14)$$

where,

$$c_1 = \frac{1}{2E_{00}} \log\left[\frac{4(\emptyset_{BN} - V_{ak})}{-\emptyset_n}\right] \tag{3-15}$$

and $\emptyset_n$ is negative for degenerate semiconductors. And the current due to thermionic field emission is given by [42, 123]:

$$J_{TFE} = \frac{A^{**}T\sqrt{\pi E_{00} q(\emptyset_{BN} - \emptyset_n - V_{ak})}}{k\cosh(E_{00}/kT)} \exp\left[-\beta\emptyset_n - \frac{q(\emptyset_{BN} - \emptyset_n)}{E_0}\right] exp\left[\frac{qV_{ak}}{E_0}\right] \tag{3-16}$$

where the tunneling probability (E_0) is given by

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \tag{3-17}$$

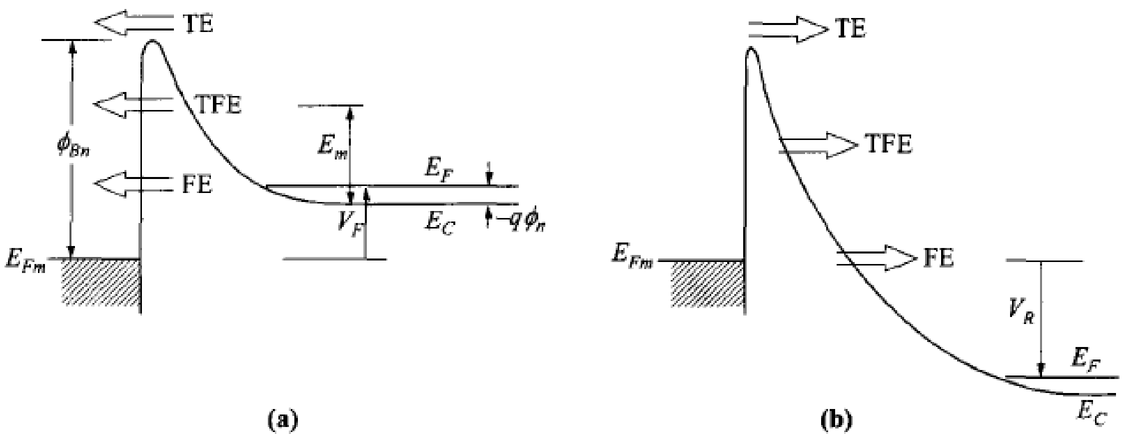


Figure 3-9: Energy-band diagram showing tunneling currents in a Schottky diode under (a) forward biad and (b) reverse bias. TE= thermionic emission, TFE, thermionic field emission, FE= field emission [42]

3.3.2 Schottky Diode Operation

To explain the behaviour of a Schottky diode, similar scenarios explained for a P-N junction is applicable to a Schottky diode:

The voltage applied across the Schottky Barrier junction is at equilibrium (V_{AK}=0V): in an unbiased Schottky diode, similar to P-N junction, free electrons move from the N-type semiconductor to the metal contact. This is illustrated in the energy band diagram of a metal-semiconductor contact in Figure 3-10.

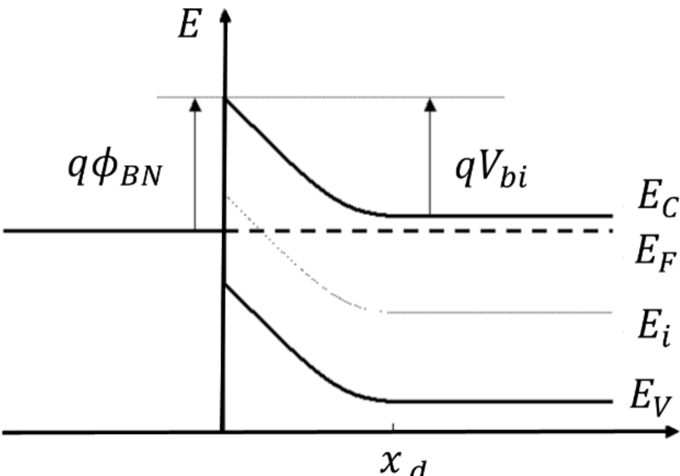


Figure 3-10: Energy band diagram of a metal-semiconductor contact in thermal equilibrium

This flow of electrons leaves positive ions on the semiconductor side close to the junction and vice versa and creates negative ions on the metal side of the junction. This charge generates a negative field and lowers the band edges of the semiconductor. This flow of electrons continues to establish a balance. The balance is characterized by a constant Fermi energy throughout the structure. The depletion region created at the

junction has a built-in potential in the negative direction and at thermal equilibrium, the width of this depletion region is sufficient to block further flow of carriers across the junction. Figure 3-11 shows that the non-rectifying metal-semiconductor junction forms a non-rectifying Schottky barrier.

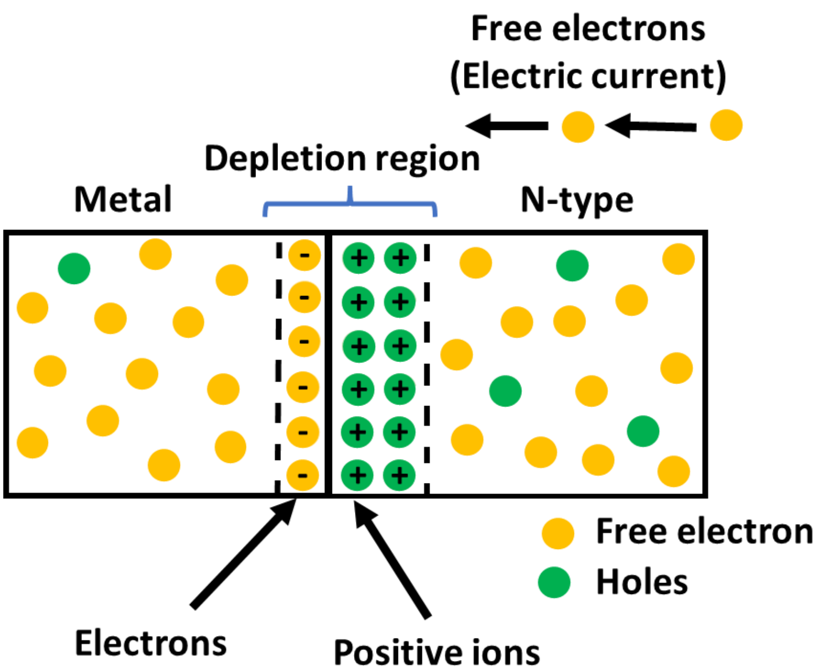


Figure 3-11: A non-rectifying Schottky barrier formed by a non-rectifying metal-semiconductor junction.

The voltage applied across the Schottky Barrier forward biases the diode ***(V_{AK}>0V):*** under forward bias of the Schottky diode, the width of the depletion region shrinks similar to a P-N junction scenario. With a forward bias, the Fermi energy of the metal is lowered with respect to the Fermi energy of the semiconductor. This results in a smaller potential drop across the semiconductor. The current then starts flowing from Anode towards the Cathode of the Schottky diode. The flow of current when the voltage

across the diode is comparable to the built-in potential of the Schottky barrier is due to the balanced distribution of diffusion and drift currents which leads to more electrons to diffuse towards the metal than the number of drifting electrons into the semiconductor. Operation of a metal-semiconductor junction under forward bias is illustrated with Figure 3-12. Figure 3-13 shows the Schottky diode structure under forward bias.

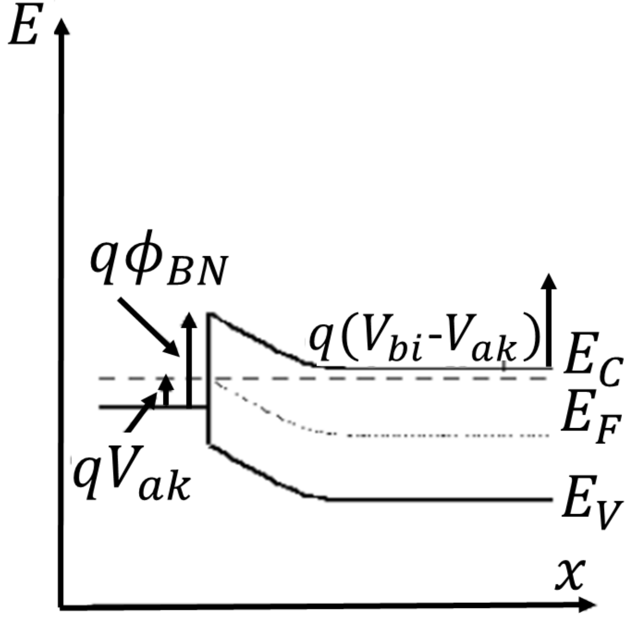


Figure 3-12: Energy band diagram of a metal-semiconductor junction under forward bias.

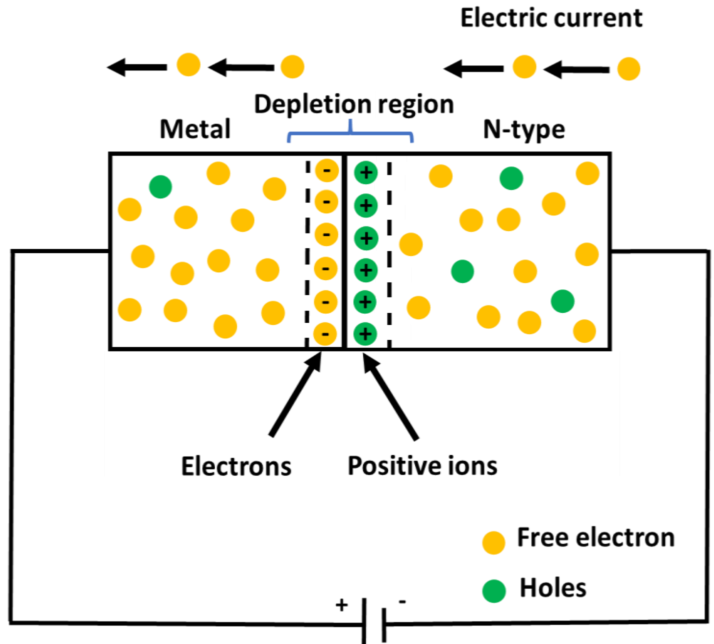


Figure 3-13: Forward biased Schottky diode structure

The voltage applied across the Schottky Barrier reverse biases the diode *(V_{AK}<0V):* as name suggests, during the reverse bias of a Schottky barrier, the negative voltage across the device rises the Fermi energy of the metal with respect to the Fermi energy of the semiconductor. The potential across the semiconductor increases and consequently, the depletion width across the junction increases. The electric field across the junction rises with increase of the reverse bias voltage. The barrier which was responsible to restrict the electrons to the metal during the off-state, remains unchanged so that the barrier, irrespective of the applied voltage, limits the current flow. This explains the rectifying behaviour of a Schottky barrier diode. Figure 3-14 shows the energy band diagram during the off-state. Figure 3-15 shows the one

dimensional device structure under reverse bias and formation of the depletion region that blocks the voltage across the device.

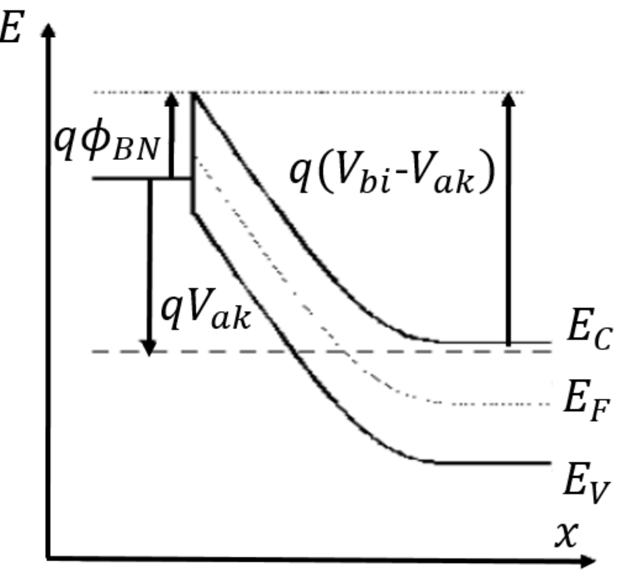


Figure 3-14: Energy band diagram of a metal-semiconductor junction under reverse bias.

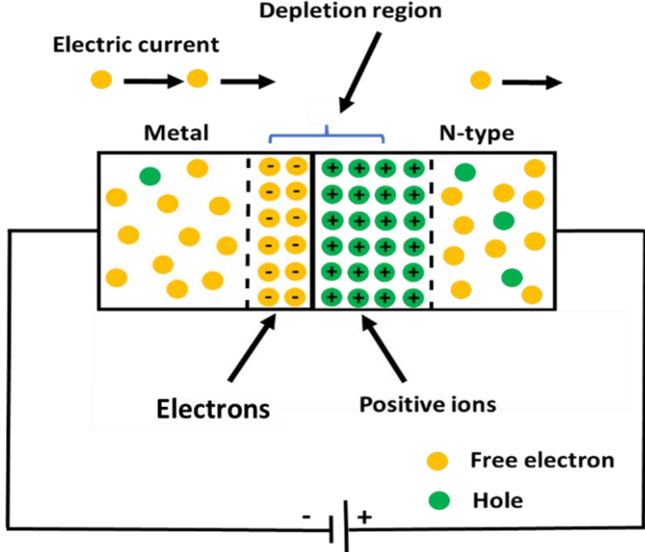


Figure 3-15: One dimensional device structure under reverse bias

3.4 PiN Diode

A PiN diode is a vertical device where a low doped N-type semiconductor is sandwiched between a heavily doped P-type Anode and a heavily doped N-type Cathode. Figure 3-16 shows a one-dimensional cross-section of a typical PiN diode used in power electronic applications along with the electric field across the device.

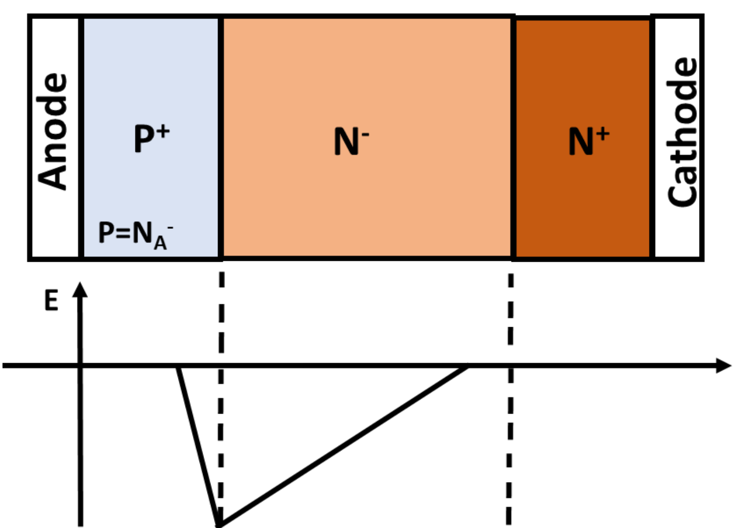


Figure 3-16: PiN diode structure and the electric field across the device.

When the diode is forward biased, there is a high-level injection of carriers in the drift region (N^- type) which causes conductivity modulation phenomena which reduces the on-state resistance of the device. As mentioned earlier, this phenomenon is specific to bipolar device such as PiN diode, IGBT and BJTs. When the diode is conducting and is forward biased, electrons are injected from the N^+ Cathode into the

drift region and holes are injected from the P^+ Anode into the drift region. The high level of carriers injected into the drift region creates a charge storage region in the N^- type drift layer. As the current density increases, the amount of charge stored in this region increases up-to a point where the concentration of the minority carriers in the drift region becomes greater than the background doping of the semiconductor in the N-drift region. The shape of the charge stored in this region during the on-state is in form of a catenary shape. This is shown in Figure 3-17. The shape of carrier depends on the high-level carrier lifetime in the drift region and the diffusion length of electrons and holes into the drift region. Due to charge neutrality, the concentration of electrons and holes in the drift region during the high-level carrier injection is equal. The shape of the catenary shape charge stored in the drift region can be explained using Ambipolar Diffusion Equation which is an equation that describes the concentration of minority carriers in the drift region in space and time:

$$D_a \frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_a} + \frac{\partial p(x,t)}{\partial t} \quad (3\text{-}18)$$

In this equation, D_a is the ambipolar diffusion constant which depends on the diffusivity of electrons and holes, and τ_a is the high-level carrier lifetime in seconds. The diffusivity of electrons and holes can be calculated using Einstein relation as below:

$$D_n = \mu_n \frac{kT}{q} = \mu_n V_T \quad (3\text{-}19)$$

$$D_p = \mu_p \frac{kT}{q} = \mu_p V_T \quad (3\text{-}20)$$

where $V_T = \frac{kT}{q}$ is the thermal voltage. D_n (electron diffusion coefficient) for Silicon is 36.17 cm²/s and 34.37 cm²/s for SiC at room temperature and D_p (hole diffusion coefficient) is 11.62 cm²/s for Silicon and 2.32 cm²/s for SiC at room temperature. Diffusion coefficients in SiC is smaller in comparison with silicon, however, the thickness of a SiC device is smaller than the thickness of a Si device due to its wider bandgap. Figure 3-18 [126] shows the catenary shape charge stored in the drift region which is explained using Ambipolar Diffusion.

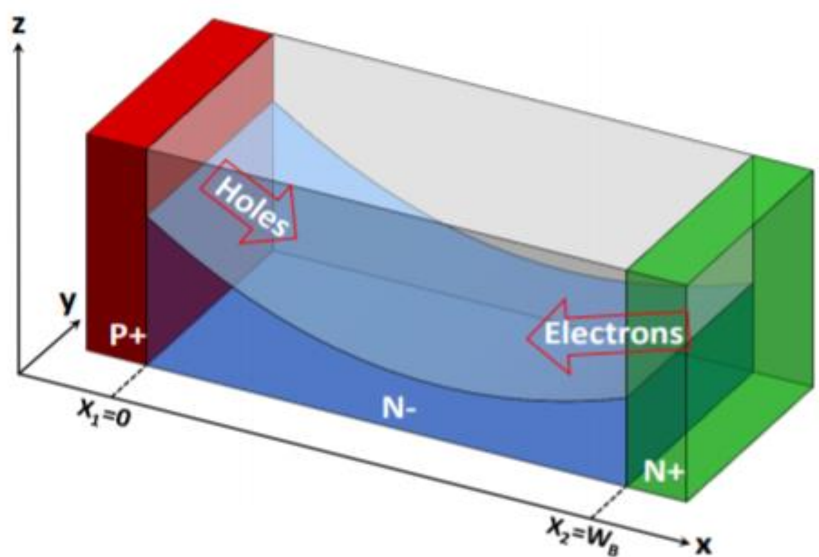


Figure 3-17: Formation of charge storage region in a PiN diode [126]

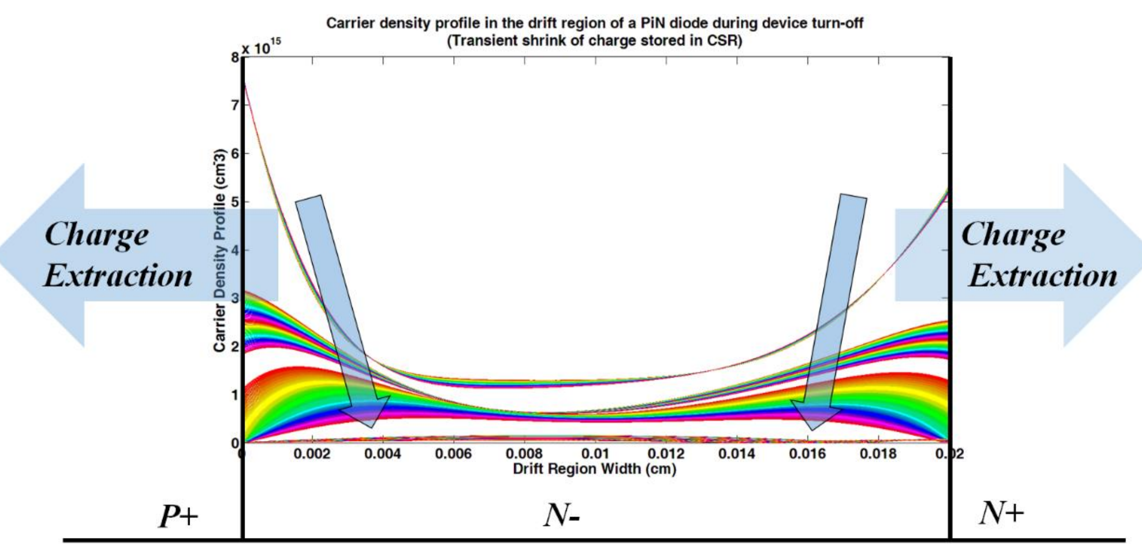


Figure 3-18: Extraction of charge from the drift region during turn-off of PiN diode [126]

The concentration of the minority carriers at the edges of the drift region is higher and the concentration reduces at the centre of the drift region. This shape can be changed by changing the diffusion length of the carriers into the drift region and by changing the high-level carrier lifetime in the drift region. The diffusion length is calculated as:

$$L = \sqrt{\tau D} \tag{3-21}$$

The diffusion length is the length that a minority carrier can travel into the drift region before it recombines. By increasing the diffusion length and carrier lifetime, the catenary shape will have shorter edges at the boundaries of the drift-region and has a flatter shape at the centre.

During turn-off of a PiN diode, the charge stored in the drift region needs to be extracted and the depletion regions needs to form in order for the device to block the

negative voltage across it. During the turn-off transient, the direction of the current reverses. This is known as the reverse recovery of the diode. During the reverse recovery, the electrons and holes are extracted from both ends of the drift region until the depletion region starts forming. Once the depletion region is formed at the P+N- junction and N-N+ junction, the remaining stored current in the drift region starts recombining until all the charge in this region is annihilated. At this point the current in the device reaches to zero and the device is switched-off.

The total current due to electrons is shown in equation (3-22) and the total current due to holes is shown in equation (3-23) in 1-D. The current is the sum of the electrons and holes densities multiplied by the semiconductor active area perpendicular to the current flow direction (3-24).

$$J_n = qn\mu_n E + qD_n \frac{\partial n}{\partial x_n} \tag{3-22}$$

$$J_p = qn\mu_p E + qD_p \frac{\partial p}{\partial x_n} \tag{3-23}$$

$$I_{tot} = A(J_n + J_p) \tag{3-24}$$

The forward current equation depends on the injection level of free minority carriers in the drift region and it depends on the drift and diffusion of electrons and holes:

$$J = J_{drift} + J_{diff} \tag{3-25}$$

$$J_{diff} = J_n - J_p = qD_n \frac{\partial n}{\partial x} - qD_p \frac{\partial p}{\partial x} = q\left(D_n - D_p\right)\frac{\partial p}{\partial x} = qV_T\left(\mu_n - \mu_p\right)\frac{\partial p}{\partial x} \tag{3-26}$$

$$\frac{J_{drift}}{E} = q(n\mu_n + p\mu_p + N_D\mu_n) \tag{3-27}$$

where D_n and D_p are the diffusion coefficients and are related to the electron and hole mobilities μ_n and μ_p according to Einstein equation (equations 3-19 and 3-20) and E is the electric field. In high level current injection during the forward conduction of a PiN diode, the last term of equation (3-27) can be neglected as the background doping of the drift region is negligible in comparison with the high level electron injection.

The current passing through a PiN diode during forward conduction can be expressed by replacing the drift and diffusion currents of equation (3-26) and equation (3-27) into equation (3-25). Equation (3-28) is the final form of current transport equation which explains the current density of a PiN diode in forward bias and depends on the electric field across the device, the mobility of electrons and holes as well as the background doping of the semiconductor and the space-dependent concentration of the minority carriers in the drift region.

$$J = qE\left(p\left(\mu_n + \mu_p\right) + \mu_n N_B\right) + qV_T\left(\mu_n - \mu_p\right)\frac{\partial p}{\partial x} \tag{3-28}$$

Figure 3-19 shows the transient switching characteristic of a PiN diode while the device is transferring from on-state to off-state. As explained earlier, the direction of current reverses to extract the additional current from the charge storage region. This negative current that passes through the device is referred to as the reverse recovery. Figure 3-19 is shows the current and voltage turn-off switching waveforms of a clamped inductive switching test, which is carried out to characterise the switching behaviour of the fabricated PiN diodes and IGBT/MOSFETs (body diodes) (more discussion is provided in chapter 5).

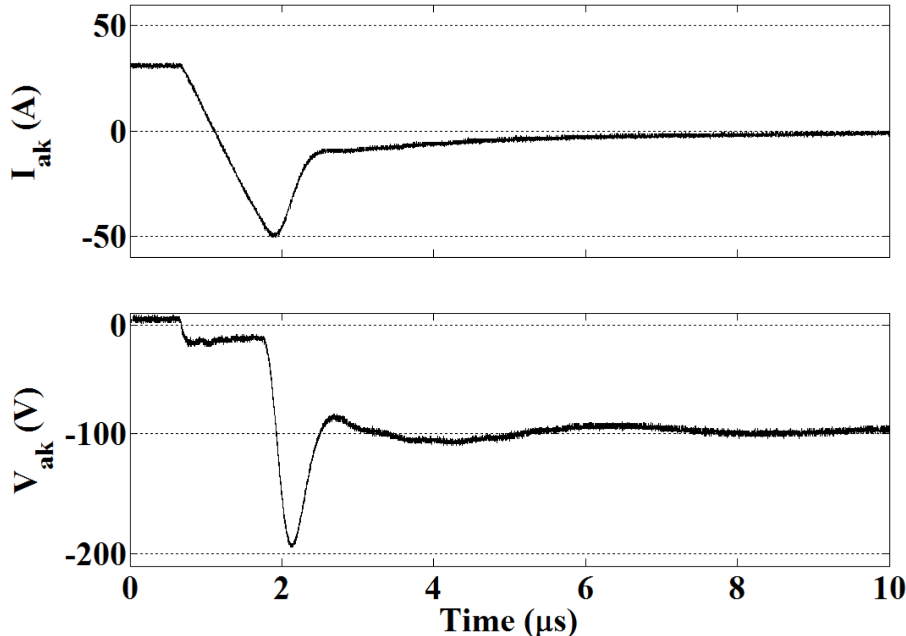


Figure 3-19: A typical PiN diode (IRF HF50D120ACE) current and voltage turn-off switching waveforms measured at Warwick.

As was explained, the blocking voltage during the reverse bias of a PiN diode is determined by the width and doping density of the drift region. Any reverse bias will cause the depletion region on the P+/N- junction to spread much further into the N- region. This is due to the significant difference in doping density on either side of the junction. With enough reverse bias, the depletion region may spread throughout the entire N- region, reaching the N-/N+ junction and causing "punch-through (PT)". For devices with PT structure, a trapezoidal electric field is formed instead of a triangular one, with a more evenly distributed electric field across the drift region, as shown in Figure 3-20. This approach can be employed to allow a thinner drift region for a given blocking voltage, which further reduces the forward voltage drop. Therefore, the use of a PT structure for PiN diodes can be beneficial, since low carrier lifetimes in 4H-SiC

can be a problem for high voltage PiN diodes and cause a high on-state voltage drop due to inadequate conductivity modulation. Devices with a PT structure typically have a lower doping density in the drift region compared with non-punch-through (NPT) devices. This will help with the evenly distribution of the electric field across the drift region.

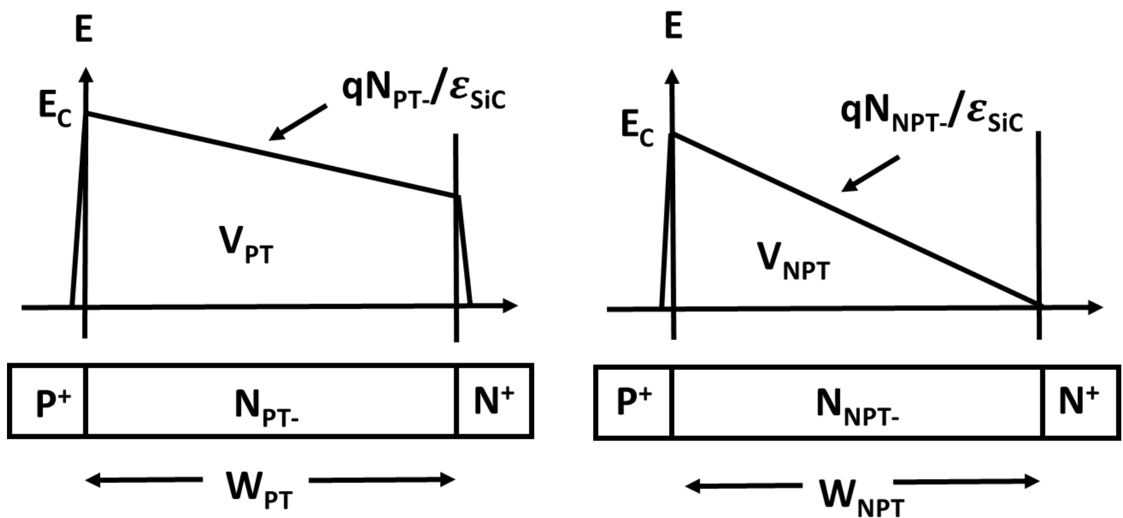


Figure 3-20: Electric filed profile at breakdown for punch-through (left) and non-punch-through (right) PiN diode structure with equal drift region length.

During reverse blocking mode of PiN diodes, the leakage current is increased with increasing temperature due to the carrier generation at elevated temperatures. For a punch-through design, the electric field at the interface between the N+ region and the N-type drift region is given by the Equation below [44].

$$E_1 = E_m - \frac{qN_{DP}}{\varepsilon_S} W_P \tag{3-29}$$

where E_m is the maximum electric field at the junction, N_{DP} is the doping concentration in the drift region and W_P is the width of the drift region.

The voltage supported by the PT diode can be approximated as

$$V_{PT} = \left(\frac{E_m + E_1}{2}\right) W_P \qquad 3\text{-}30$$

Using Equations 3-29 and 3-30, the breakdown voltage for the punch-through diode can be estimated using Equation 3-31. The PT diode experiences avalanche breakdown when the maximum electric field reaches the critical electrical field E_C for breakdown

$$V_{BR} = E_C W_P - \frac{q N_{DP} W_P^2}{2\varepsilon_S} \qquad 3\text{-}31$$

Chapter 4 4H-SiC Device Fabrication Technology

In this chapter the 4H-SiC fabrication technology that was used in this thesis for fabrication of 4H-SiC PiN diodes and Schottky diodes is presented. Following this, the device packaging process of the fabricated devices is presented.

4.1 4H-SiC Processing Techniques

The fabrication process flow for the 4H-SiC PiN diodes and Schottky diodes will be presented in Chapter 6, 7, and 8 of this thesis. The fabrication process technology discussed in this Chapter are needed for the fabrication of the 4H-SiC diodes.

In the studies presented in this thesis, 4H-SiC wafers with various epitaxial layer thickness were used. Wafers with 35 μm and 30 μm epitaxial layer were acquired from Dow Corning and Norstel AB respectively and wafers with 110 μm thick epitaxial layer were bought from Norstel AB. The starting point of all devices is an unprocessed 4H-

SiC wafer. The surface must be cleaned from any residual materials before device processing.

4.1.1 SiC Wafer Dicing

The wafers used for fabrication in this work were cut into quarters and each quarter was cut into 10 × 10 mm chips using a laser. Figure 4-1 shows the result of laser cutting of SiC wafer performed at University of Warwick, with the chips lined up as they were before dicing. As shown in Figure 4-1, the edges of each chip seem to have experienced a minimal damage yet a large amount of dirt and dust was evident across the wafer. To avoid this, prior to laser cutting, a thick layer of photoresist was used to cover the wafer. Even though the damage at the edges seems negligible, the diodes closest to the chip centre were used for electrical characterisation.

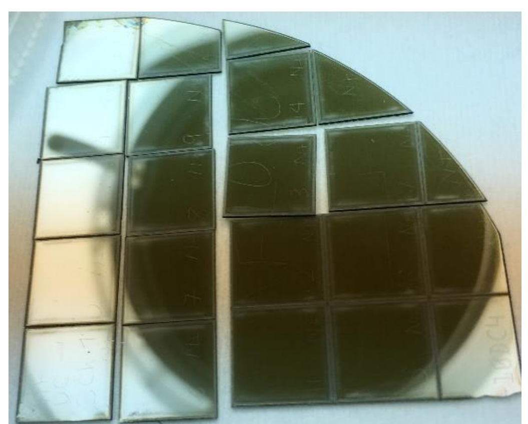


Figure 4-1: The results of laser cutting the 4H-SiC wafer into 10 × 10 mm chips

4.1.2 SiC Wafer Surface Cleaning Process

Any residual materials, impurities, dirt or dust can have a detrimental effect on the electrical performance of the fabricated devices. Hence, it is necessary to clean the surface of the wafer thoroughly prior to any device fabrication process. For example, samples in Figure 4-2 underwent thermal oxidation. The colour variation on the surface of 4H-SiC samples shows that the thickness of the grown oxide is not uniform which could be due to surface contamination, dirt or any residual materials from the previous fabrication processes. Hence, surface cleaning step is crucial.

Figure 4-2: 4H-SiC PiN diodes after thermal oxidation process. The variation in colour is due to surface contamination.

The cleaning process consists of three steps. First is solvent cleaning where the samples are soaked for 5 minutes in each of the following chemicals in ultrasonic bath

and then rinsed with DI water: 1) acetone, 2) isopropanol and 3) methanol. This removes some of the organic impurities [127].

Next, the samples are placed in 5% hydrofluoric (HF) acid solution for 1 minute and then rinsed with DI water. The samples are then cleaned with Radio Corporation of America (RCA) Standard Clean process [128] . The RCA cleaning process first removes any remaining organic impurities from the sample using RCA1 solution followed by RCA2 formulation where the metals and chemisorbed ions are removed from the substrate surface. RCA1 solution consists of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and DI water in the ratio of 1:1:5 at approximate temperature range of 75 to 80°C for 10 minutes followed by rinsing in DI water. The samples are then immersed in 5% hydrofluoric (HF) acid solution for 1 minute and then rinsed with DI water. Next is the RCA2 process which consists of hydrochloric acid (HCl), H_2O_2 and DI water in the ratio of 1:1:5 at approximate temperature range of 75 to 80°C for 10 minutes followed by rinsing in DI water.

The next step is called a “Piranha” clean which is used to remove any remaining organic material. Samples are dipped in sulphuric acid (H_2SO_4) and H_2O_2 in the ratio 3:1) for 10 minutes, then rinsed in DI water. Finally, the samples are soaked in 5% hydrofluoric (HF) acid solution for 1 minute and then rinsed with DI water.

4.1.3 Surface Passivation

Any Passivating the semiconductor surface is essential in reducing the leakage currents and exploiting the breakdown voltage of the power devices. It also ensures their long term reliability. Hence, it is necessary to remove any surface contaminants, such as organic particles, metals and oxides prior to surface passivation, as explained in the previous section.

The next step is to deposit a dielectric layer which helps to isolate the semiconductor surface from metallisation layers and packaging. In addition to passivating the surface, it ensures stable and reliable operation of the power device. SiO_2 is normally used as a passivation layer for both Si and SiC devices due to the easiness of its implementation and was used as a passivation layer in the fabrication process of both 4H-SiC PiN and Schottky diodes in this research. However, SiO_2 is vulnerable to breakdown under high electric fields due to its low dielectric constant ($k \sim 3.9$) compared to that of 4H-SiC emphasising the importance of using alternative, high k dielectrics such as aluminium nitride (ALN) and aluminium oxide (Al_2O_3). Significant literature has been reported on this [129-131], suggesting that dielectrics with higher dielectric constants are promising candidates to replace SiO_2 due to their high thermal conductivities, moderately higher k, similar bond lengths, as well as thermal expansion coefficients compared to that of 4H-SiC [132-134].

4.1.4 4H-SiC Oxidation Techniques

Silicon Carbide is the only wide band-gap semiconductor that can be thermally oxidized to form an oxide insulator with the same properties as SiO_2 on Si in SiC MOS structures. It can also be used as a surface passivation layer and edge termination. Also, to increase the carrier lifetime in 4H-SiC PiN diodes, it is necessary to reduce the concentration of the lifetime-killing defects in the material. So, some post-growth (of epilayer) processing needs to be applied. Various oxidation techniques that are of interest in this thesis are discussed in this section.

4.1.4.1 Thermal Oxidation Process

Growing SiO_2 on SiC is similar to Si, but the growth rate of SiO_2 on silicon carbide is much slower and needs higher temperatures. Thermal oxidation of silicon is typically done at temperatures below 1200°C, whereas for silicon carbide is usually performed at temperatures between 1000°C and 1300°C or higher [135]. The oxidation process can be performed in dry or wet atmosphere. The oxide growth rate and the breakdown strength of the oxide dielectric are the main differences between these two processes. The quality of the grown oxide in dry oxidation is much higher than wet oxidation. Therefore, the dielectric breakdown strength is also high, but the growth rate is much slower. Wet oxidation offers a poor interface and oxide quality, but faster growth rate [135]. As the quality of interface and the grown oxide are critical for the performance of SiC power MOSFETs, dry oxidation is the preferred oxidation process.

As outlined in Section 2.8.1, to increase the minority carrier lifetime in 4H-SiC PiN diodes, it is necessary to reduce the concentration of the lifetime-killing defects in the bulk material. The prevailing lifetime-killing defects in 4H-SiC are the $Z_{1/2}$ defect and the $EH_{6/7}$ defect, which are both known to be carbon vacancy-related defects. Therefore, approaches to "repair" the aforementioned defects comprise the diffusion of carbon interstitials from the surface of the semiconductor into the bulk of the material. Carbon implantation [95], or thermal oxidation [2] are the methods to generate the required carbon interstitials.

Authors in [95] reported the results of their study on the carbon implantation technique where a 250 nm carbon box profile was implanted into the 4H-SiC epilayer, forming an area with a surplus of carbon interstitials. Various annealing temperatures were explored (range from between 800°C to 1800°C) in order to diffuse the extra carbon interstitials into the semiconductor bulk. The samples were then characterised using deep level transient spectroscopy and time resolved photoluminescence (TRPL) to verify the defect concentration in the semiconductor. TRPL complements normal PL studies (discussed in Section 5.2.4) where a short laser pulse is used for excitation, and a fast detector is used to define the emission of a material as a function of time which occurs after excitation. TRPL provides further information about the recombination process. And can be used in both low and high temperatures to study the recombination properties of the various bound excitation emissions and to detect the PL decay corresponding to the lifetime of the minority carriers respectively. The results of the DLTS analysis showed that for both the $Z_{1/2}$ and $EH_{6/7}$ defects, at annealing

temperatures of 1600°C and above, the peaks of DLTS spectra fell below the detection limit. Also, the carrier lifetime of the material was doubled in the carbon implanted and annealed samples when compared to as-grown, non-implanted reference samples. In the work reported in [136], the same carbon implantation and annealing method was performed on thick (around 265 μm) epitaxial layers where the carrier lifetime was improved from around 3.5 μs in the unimplanted (control) samples to around 18.5 μs in the carbon implanted samples.

In the study by Hiyoshi and Kimoto [2], thermal oxidation was used to decrease the concentration of the $Z_{1/2}$ and $EH_{6/7}$ defects in 4H-SiC epitaxial layers and hence increase the carrier lifetime. Carbon interstitials are generated at the SiO_2/SiC interface as a result of the thermal oxidation process. During this process, the carbon interstitials diffuse into the bulk material and inhabit carbon vacancy regions related to $Z_{1/2}$ and $EH_{6/7}$ defect centres. The process consisted of two 5 hours 1300°C thermal oxidations, and the grown SiO_2 between the two stages were removed. As a result, the carrier lifetime of the material was improved from 0.73 μs in the as-grown sample to 1.62 μs after thermal oxidation. Moreover, the $Z_{1/2}$ defect centre found to be lower than the detection limit to a depth of 50 μm in the material.

Although the thermal oxidation process presented in [2] was effective in decreasing the $Z_{1/2}$ and $EH_{6/7}$ concentrations, it was discovered that an additional defect centre, HK0, is created in the process [97]. According to the resulted DLTS spectra, it was estimated that the defect centre is at an energy level of $E_V + 0.78$ eV. Surprisingly, the HK0 concentration was at its maximum close to the oxidised surface of the

semiconductor, moderately reducing with increasing depth into the bulk material. However, an opposite trend was seen in the $Z_{1/2}$ concentration. At the depth where the HK0 concentration was reduced to the detection limit (around 6-7 μm), the $Z_{1/2}$ concentration was increased to the value of the as-grown epitaxial layer. This suggests that there was interaction between the $Z_{1/2}$ and HK0 centres throughout the thermal oxidation process. The work in [85] reported that annealing the sample in an inert ambient at 1550°C could remove the HK0 defect centres; this was applied after the thermal oxidation process as reported in [97] and the carrier lifetime was enhanced from 2.54 μs after the thermal oxidation to 4.52 μs. This resulted in a seven-fold improvement of carrier lifetime when compared to as-grown sample.

Figure 4-3 shows the high temperature oxidation furnace at Warwick University cleanroom which was used for the study in Chapter 7 on carrier lifetime enhancement on 4H-SiC PiN diodes via thermal oxidation and successive annealing process. Moreover, the study in Chapter 8 on the impact of surface treatments on 4H-SiC Schottky diodes also involves surface oxidation treatment in O_2 and N_2O ambient which were both performed using the high temperature furnace in Figure 4-3. To carry out any oxidation processes in the Hitech furnace, wafers are loaded on to the SiC wafer carrier of the furnace at around 600°C with Ar flowing at 5 Lit/min to prevent any oxygen flow in the furnace. The temperature is then raised to the desired oxidation temperature and ramping rate per minute. The samples are held at the desired temperature for a set duration to grow the desired passivating oxide thickness. After the oxidation process is completed, the temperature is ramped down to 600°C at 5°C

per minute in Ar (5L/min). The detailed thermal oxidation processes used in the fabrication of the devices in this thesis is presented in the corresponding Chapters.

4.1.4.2 Post Oxidation Annealing

Annealing of the grown oxide layer can effectively passivate the interface traps between the SiC/SiO_2. Post oxidation annealing in various atmospheres have been reported in the literature, such as argon (Ar), hydrogen (H), helium (He), nitric oxide(NO), nitrous oxide (N_2O) and phosphorous [137-139].

Figure 4-3: High temperature oxidation furnace in the clean room

The effects of Nitrous oxide and phosphorous surface treatment in a P_2O_5 ambient on 4H-SiC material are explored in this thesis. During N_2O passivation, the Si≡N bonds that are generated at the SiO_2/SiC interface can passivate the interface traps due to dangling and strained bonds. They can also form a barrier for deduction of carbon-oxides and any other complex silicon oxides compounds at the interface. As discussed in [140], the large mismatch between 4H-SiC and SiO_2 can cause stress between SiC and the grown oxide. This stress can be reduced by using nitrogen during post oxidation annealing. It has been reported in [138] that passivation of phosphorous in a P_2O_5 ambient which changes the SiO_2 layer to PSG (phosphosilicate glass) yields the best result with peak mobility up to approximately 80 cm^2/V.s on 4H-SiC MOSFET (0001) face with Al+ implanted P-body. Hence, the motivation of the research in this thesis (Chapter 8) to investigate the effect of treating the surface of 4H-SiC material in N_2O and P_2O_5 ambient using metal-semiconductor interface as a characterisation tool.

4.1.4.3 N_2O Grown Oxide

Growing oxide under N_2O atmosphere has also been studied and compared with other post oxidation annealing methods. Authors in [141] have reported that oxides grown in N_2O ambient on 6H-SiC material exhibit superior reliability and better electrical properties under high-field stress compared to the samples annealed in N_2O. This result has also been supported by the study reported in [137]. However, [139] reports that D_{it} and the near-interface trap density were significantly improved in grown oxide on 4H-SiC in diluted N_2O ambient compared to the oxide grown in 100%

pure N_2O environment. This proposes that the rates of carbon build-up and carbon removal are closer in diluted N_2O compared to 100% pure N_2O environment. Diluted N_2O (20% N_2O and 80% Ar) was used in this work due to the flow rate limitation of N_2O gas (maximum 1 L/min) in Warwick University clean room facility. To avoid O_2 in the air flowing into the furnace, the N_2O oxidation process was mixed with Ar gas.

As reported in the literature [137, 141], oxide directly grown under N_2O ambient exhibits better electrical properties compared to that of N_2O post oxidation treatment under identical time and temperature conditions. In the study presented in Chapter 8, direct N_2O oxidation was performed in the Hi-Tech furnace in Figure 4-3. The N_2O oxidation profile was similar to thermal oxidation process, but the samples were held for longer at lower temperature in 20% N_2O (1 L/min) and Ar (4 L/min) ambient. After the N_2O oxidation process, the temperature was ramped down to 600°C at 5°C per minute in Ar (5L/min). The details of the N_2O oxidation process is presented in Chapter 8.

4.1.4.4 Phosphorus Pentoxide (P_2O_5) Deposition

Substantial advancement has been made regarding interface passivation over the last decade, especially with post oxidation annealing or direct growth in NO or N_2O environments, providing a channel mobility of around 20-35 $cm^2/V.s$ for 4H-SiC (0001) MOSFET [142-144]. Some studies have reported that phosphorous treatment is more effective than NO or N_2O passivation treatments, providing peak mobilities of 80-90 $cm^2/V.s$ [138, 145] and even up to 108 $cm^2/V.s$ [146] for 4H-SiC MOSFETs fabricated on

the conventional (0001) Si-face. Hence, the motivation to perform phosphorous treatment in this research (Chapter 8).

In Chapter 8, P_2O_5 deposition was used to treat the surface of 4H-SiC substrates before fabricating Schottky diodes to study the impact of this treatment on the SiC surface and metal/semiconductor interface. To perform the phosphorous treatment, SiC samples were mounted on a Si carrier wafer. First a layer of photoresist was deposited on the Si carrier, the samples were placed on the deposited photoresist and then baked at 200°C for 3 minutes. Phosphorous treatment in this work was performed using a solid SiP_2O_7 phosphorous planar diffusion source (PDS) supplied by Saint-Gobain that decomposes to produce a P_2O_5 passivating ambient. The treatment was performed in an annealing furnace, with the samples mounted on a Si carrier wafer vertically placed in front of the phosphorous diffusion source on a carrier boat as shown in Figure 4-4. They were then annealed at 1000°C for 2 hours in N_2 ambient (5 L/min). The furnace used for the passivation process is shown in Figure 4-5.

The SiP_2O_7 diffusion source decomposes into SiO_2 and P_2O_5 under high temperature as shown by the chemical reaction below:

$$SiP_2O_7 + 1000°C \rightarrow SiO_2 + P_2O_5 \quad (4\text{-}1)$$

As discussed in [138], after phosphorous treatment, the remaining oxide is not SiO_2 any longer, but is transformed to phosphosilicate glass (PSG) which can passivate the interface traps between SiO_2 and 4H-SiC.

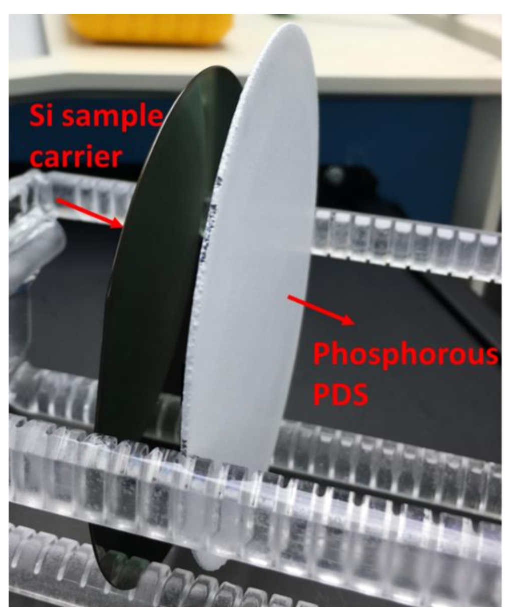


Figure 4-4: Samples mounted on a Si carrier wafer placed in front of the phosphorous PDS on a carrier boat

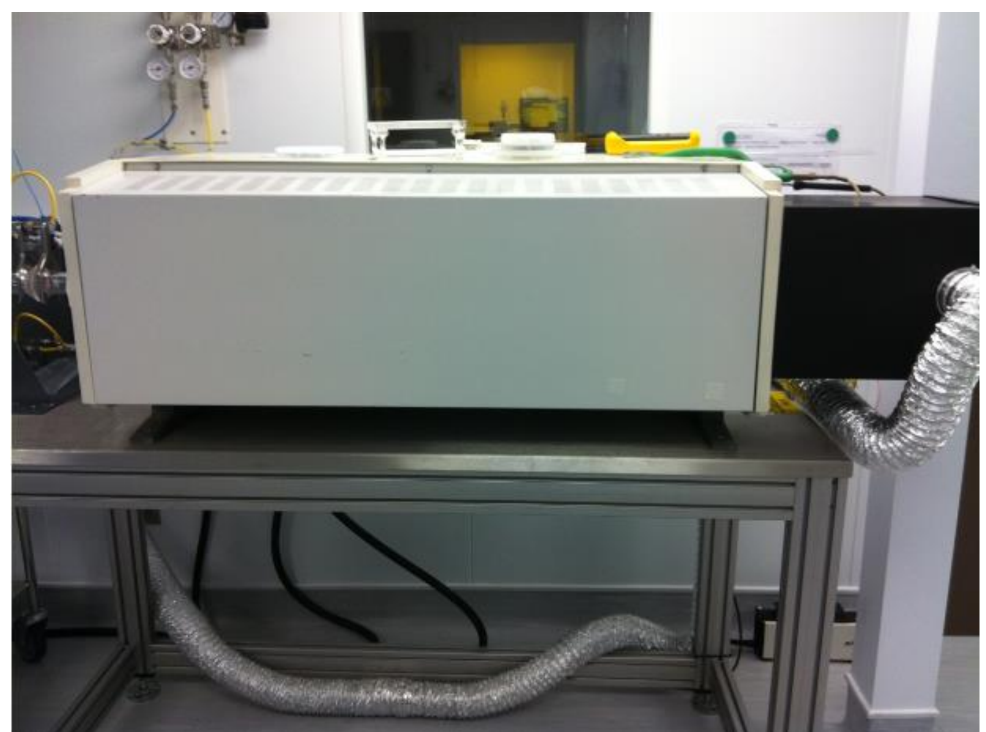


Figure 4-5: Annealing furnace used for phosphorous treatment

4.1.5 Etching of 4H-SiC

Unlike Si, it is quite challenging to etch 4H-SiC material using conventional acid or base solutions. This is due to chemical inertness of 4H-SiC. Molten salts, such as potassium hydroxide (KOH) or sodium hydroxide (NaOH), at temperatures around 600-800°C are needed for wet etching of SiC. Thus, employing dry, plasma-based etching methods are essential. Dry etching of SiC is similar to Si, as typical SiC dry etch chemistries are based on fluorinated plasmas such as tetrafluoromethane (CF_4). However, the optimisation of etch processes is slightly different than Silicon. This is because SiC is a source of C, which means different C:F ratios are needed. The reactive Ion Etching (RIE) technique is used for dry etching of SiC [147, 148]. However, to etch away the SiC surface during RIE process, the surface is physically bombarded by ions. This results in a relatively high surface damage, and hence recombination centres are generated. Hence, due to the increased surface recombination, the total carrier lifetime in the device is reduced. Therefore, techniques such as Inductively Coupled Plasma (ICP) etching that use high-density plasma source etching approach, has been preferred over RIE, and exceptional outcomes, regarding etch rates and surface roughness, have been published [149]. The work in [149], explored and optimised the use of a CF_4/O_2-based ICP etch process; this has subsequently been validated in the fabrication of a variety of high voltage 4H-SiC power devices [150, 151]. Thus, for the fabrication of 4H-SiC power devices of this study, ICP etching of the SiC material was used.

4.1.6 Ohmic Contacts to 4H-SiC

It is widely reported that forming reliable, low resistance ohmic contacts to 4H-SiC, mainly p-type 4H-SiC, is challenging. In order to minimise on-state power losses and achieve high switching speed, having low contact resistances are essential. In order to form ohmic contacts on 4H-SiC, suitable metals must be deposited on heavily doped n- or p-type device areas and then a post-deposition anneal process needs to be performed. A short high temperature annealing of most 'as-deposited' metals that form a rectifying (Schottky) contact to 4H-SiC, typically allows ohmic contacts to be attained. The contact resistance is reliant on numerous factors, such as the contact metal (or metals) used, surface treatment prior to metal deposition, the doping concentration of the semiconductor, and the annealing conditions used.

Formation of ohmic contacts to n-type SiC is very well investigated, studied and reported in recent years [152-154]. The most common method to form an ohmic contact is already described in Section 3.3.1. According to TFE model presented in [155], the specific contact resistance can be expressed as

$$\rho_c = \left(\frac{kT}{qA^{**}}\right)\frac{kT}{\sqrt{\pi(\emptyset_{BN}+V_n)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\left[\coth\left(\frac{E_{00}}{kT}\right)\right]\exp\left(\frac{\emptyset_{BN}+V_n}{E_0}-\frac{V_n}{kT}\right) \qquad 4\text{-}2$$

Where V_n is the energy between the conduction band edge and the Fermi level.

Although primary work mainly concentrated on ohmic contacts to 6H-SiC [156], the developments in 4H-SiC substrate and the quality of its epitaxial layers since then resulted in the shift of focus to this material. A considerable amount of the work on n-type ohmic contacts made use of nickel (Ni) and Ni-based alloys for the contact metal,

yet a choice of further metals, such as titanium (Ti), tantalum (Ta), niobium (Nb) and molybdenum (Mo), have also been effectively used [157].

Ohmic contacts to n-type 4H-SiC material is thoroughly reviewed in [157]. This work demonstrated that specific contact resistances of the order 10^{-6} Ω.cm^2 are generally achievable, with the lowest contact resistance stated being 2.7×10^{-7} Ω.cm^2. There have been some reports of studies in which ohmic contacts were formed to n-type 4H-SiC material without any post-deposition annealing procedures [157], but the larger number of reported works have elaborated an anneal procedure of some sort. Several parameters need to be considered for anneal processes such as temperature, duration and annealing atmosphere. These parameters vary depending on the types of metal contact. Annealing processes are normally carried out at temperature ranges between 900-1100°C, for duration of typically between 1-10 minutes. To prevent oxidation of the metal surface at these high temperatures, the anneal process is performed in an argon (Ar) atmosphere or under vacuum. For Ni contact, after high temperature annealing process, silicides (Ni_2Si) are formed. Ni silicides reduce the contact resistance by lowering the Schottky barrier height [157]. However, it is more favourable to use a multilayer metallisation arrangement rather than Ni-only ohmic contacts. This is due to poor morphology and long-term stability of Ni-only ohmic contacts [153, 158]. A few examples of the preferred multilayer metallisation arrangement are Ti/Ni/Al, Al/Ni/Al and Ni/Ti which provide a better morphology and long-term stability of the metal contact.

As stated earlier, low resistance ohmic contacts to n-type 4H-SiC are easier to form than for p-type 4H-SiC material. This is due to the wide band gap of 4H-SiC, which causes a large Schottky barrier height at the metal-semiconductor interface. This potential barrier is inevitable, as for 4H-SiC the valence band edge is nearly 7 eV below the vacuum level, and the highest work function of any well-known metal is lower than 6 eV [159]. Therefore, to encourage the ohmic behaviour, the semiconductor beneath the contact is heavily doped as to facilitate field emission current pass through potential barrier [155]. Nevertheless, in practice heavily doped p-type areas in 4H-SiC are challenging to achieve. This is due to the low dopant ionisation of acceptors at room temperature.

Since Al is a p-type dopant, it was assumed that using Al as an anode contact metal would help achieving low resistance ohmic contacts as a result of doping the 4H-SiC during a high temperature annealing process and consequently facilitating field emission through the metal-semiconductor interface [159]. Even though this has later been disregarded, Al is still extensively used in ohmic contacts to p-type 4H-SiC due to its capacity to encourage the formation of Schottky barrier-lowering compounds at the metal-semiconductor interface [160]. As reported in [161] and [162], metallisation schemes based on Ti/Al alloys have generated the best results in terms of specific contact resistance, for both epitaxial and implanted p-type 4H-SiC layers. With Al/Ti/Al metallisation scheme presented in [162] having the lowest specific contact resistance of 5×10^{-6} Ω.cm^2. However, looking at the studies reported in the literature, the resistance values that are presented by different research groups vary considerably even for

comparable metallisation schemes and annealing conditions. This suggests that the quality of semiconductor material and the pre-deposition surface treatment process both play a vital role in realizing low resistance ohmic contacts.

4.2 Device Packaging Process

Packaging of power electronic devices/modules provides mechanical and electrical interfaces for the device and allows the device to be utilized in a circuit to control the flow of the current. Direct bonded copper (DBC) substrate provides a rigid mechanical surface for the power electronic devices and allows an easier handling of the power electronic devices in any application. Additionally, this creates an interface which allows heat extraction from the device to the heatsink as well as providing an electrically insulating layer to isolate the high voltage side of the device from the cold plate on the cooling system. The DBC substrate is a layer of ceramic substrate sandwiched between two layers of copper. The ceramic is an electrically insulating material with a very high breakdown voltage. The most commonly used ceramic substrates are Al_2O_3 (Alumina or Aluminium Oxide), AlN (Aluminium Nitride) or Si_3N_4 (Silicon Nitride). Each of these materials have different properties and based on the application and type of the power electronic device, the appropriate material may be used in the packaging process. Al_2O_3 is the cheapest of the three, however, the coefficient of thermal expansion (CTE) of this material is not the closest to the CTE of SiC. In packaging of a power electronic devices, the most common failure mechanisms are wire bond lift-off or solder delamination. Solder delamination is due to the

mismatch CTE between the layers of materials that are used in the packaging which in return causes different rate of expansion and contraction of the materials stacked on top of each other. Throughout the life span of the power device, this uneven stress and strain on the solder layer brings about solder fatigue and eventually, degradation of the solder layer. This emphasises the importance of choosing materials that have the closest CTE. AlN has a closer CTE to Si (2.6) and SiC (2.2) and it also has a significantly higher thermal conductivity making this substrate a very suitable material for applications where downsizing of the power electronic devices is required. Due to higher thermal conductivity of AlN, a thinner layer of ceramic can be used which improves the heat extraction from the bottom side of the device. Si_3N_4 has the lowest CTE among these ceramics and the mechanical strength of this material is significantly higher than the other two materials. Hence, a thinner material can be used to achieve the same thermal performance of the Al_2O_3 based DBC substrates. Table 4-1 shows the material properties of these ceramics. In packaging of the 4H-SiC PiN and Schottky diodes in this work, a AlN substrate with thickness of 0.63mm was used which was adequate for the breakdown voltage of the diodes according to ISO-6469 part 3. The copper thickness was chosen to be 0.3mm.

Table 4-1: Ceramic DBC substrate material properties

Properties	AlN	Al_2O_3	Si_3N_4	Si
Bending strength/flexural strength (MPa)	350	320	689	
Dielectric constant (@ 1MHz)	8.8	9.8	4.5~7.4	
Coefficient of Thermal expansion ($*10^{-6}$/°C)	4.6	7.6	3.3	2.6
Thermal conductivity (W/m.K)	180~200	18	29	
Breakdown voltage (kV/mm)	14	15	100	

The top side of the DBC substrate is designed to contain different islands. This is achieved by etching the copper layer all the way down to the ceramic substrate. Each of these islands can be used as an Anode or a Cathode of the diode. The withstand voltage between each two island depends on the pitch and clearance of the two conductive copper on the surface of the DBC substrate. Each 4H-SiC die which was fabricated as part of this work had multiple diodes with different sizes. The design of the DBC substrate was carried out in such a way that the die was mounted in the middle of the substrate and this island was the Cathode of the device. The other islands around the Cathode island were designed to have equal lengths. This would eliminate the impact of parasitic inductances during the measurements. Figure 4-6 shows the layout of the DBC substrate. The minimum pitch between each track was 1 mm to prevent arcing between the tracks due to potential difference.

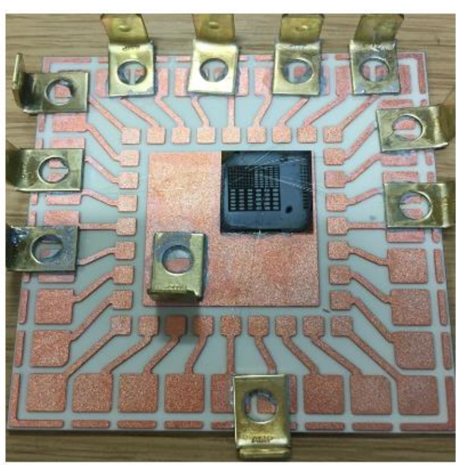


Figure 4-6: Layout of the designed DBC substrate used for packaging the fabricated dies

The reflow oven was programmed to follow a temperature profile and also vacuum was used to extract Oxygen from the chamber and insert Nitrogen to the chamber for the reflow process to complete. This also reduces the amount of voids under the solder due to the fumes and gasses trapped underneath the device. Once the soldering process was completed, very thin wire bonds were used to connect Anode of each device to the Anode island on the DBC substrate.

There are two main methods for mounting the die to the substrate: 1) soldering 2) sintering. Soldering is the most common method and was used to package the fabricated SiC PiN diodes in this study. Soldering process involves using a stencil (usually made from Aluminium of different thicknesses which controls the thickness of the solder layer beneath the device) to apply a solder paste to the surface of the DBC substrate before placing the die on the solder area. Several types of solder pastes exist for different applications based on their melting point and wetting profiles. The most common

solders used in the majority of automotive power inverters have the following particles: %95.5 Sn, %3.8 Ag and %0.7 Cu (which are lead free). This solder is in form of liquid at room temperature and after the reflow soldering process, the solder starts reflowing at around its melting point. After the soldering process is completed, the metallurgic bonding will have a melting point which is slightly higher than the reflow temperature of the solder layer and that is considered as the maximum junction temperature of the device before the packaging of the device fails. It is very important to have a uniform layer of solder across the die with identical thickness. A stencil was used to screen print the solder layer on the DBC substrate. Figure 4-7 shows the Al stencil used in this study to apply uniform solder with thickness of 6 thou (0.1524 mm). Figure 4-8 shows the solder screen printing machine at the power device packaging facility of University of Warwick.

Figure 4-7: Al stencil used for soldering process with a thickness of 6 thou

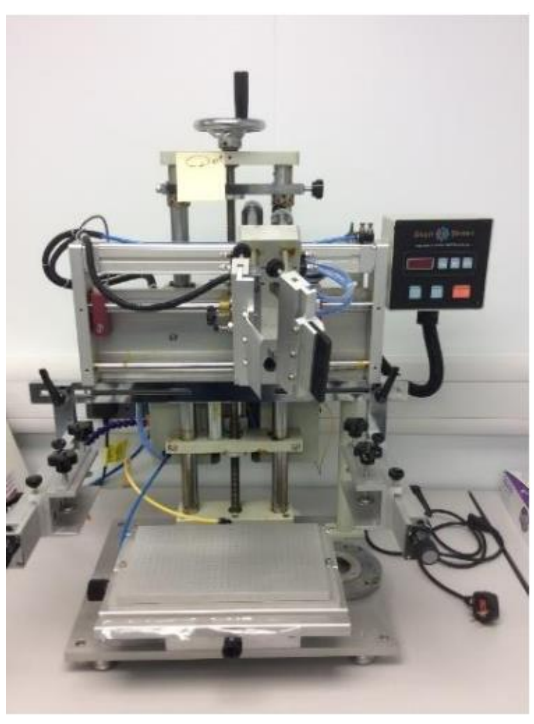


Figure 4-8: Bench-top Mascoprint S200HFC semi-automatic solder screen printing machine with stencil holder at the University of Warwick power device packaging facility.

Before placing the sample on the solder paste it must be cleaned with Isopropanol alcohol in case of contamination. Plasma etching process can also be used in case of oxidisation. The devices can then to be picked up and placed on the solder paste. Figure 4-9 shows the pick and place device used to place the die on the solder.

Figure 4-9: Cammax Precima EDB65 Eutetic pick and place die bonder, including N2 cover gas at the University of Warwick power device packaging facility

The soldering process can be done in a vacuum reflow oven where the substrate is heated to reach the melting point of solder. The melting point of the solder used in this study is 217°C. The reflow oven was programed to follow a temperature profile and also vacuum was used to extract Oxygen from the chamber and insert Nitrogen to the chamber for the reflow process to complete. The advantage of using a vacuum reflow oven is that it decreases the void area under the device and hence improves the reliability of the packaged device. This also reduces the amount of voids under the solder due to the fumes and gasses trapped underneath the device. The reflow oven can be programmed to create an optimised soldering profile to achieve the most optimal solder joint. The soldering process is completed after the solder is melted, the metallurgical contact between the back side metal contact of the sample and the

substrate is formed, and the device is cooled down to a pre-set temperature. Figure 4-10 shows the programmable ATV vacuum reflow oven used to package the fabricated SiC PiN diodes. The oven has two sensors, one that controls the temperature of the carbon sample carrier/plate and the second sensor controls the temperature of the top of the sample by directly sitting on top of the die. The pressure of the oven and valves that let the gases enter the chamber can all be controlled.

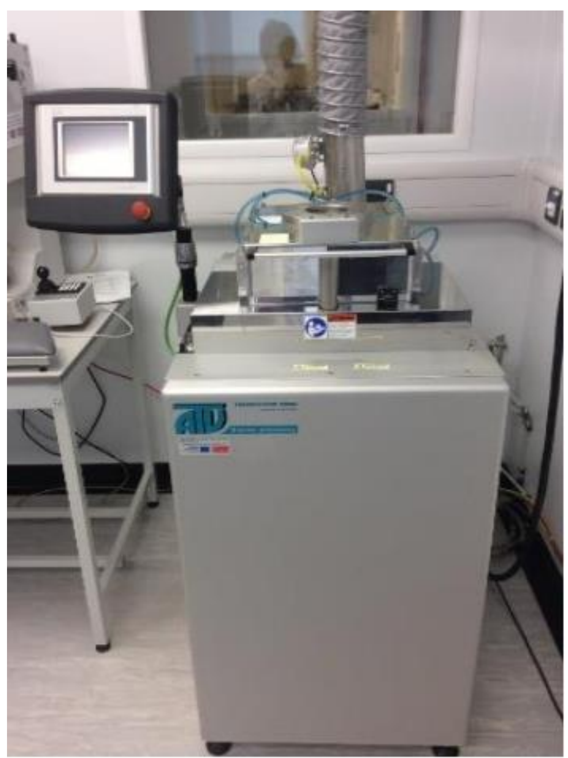


Figure 4-10: ATV SRO-704 programmable solder reflow/thermal processing, rapid thermal annealing (RTA) oven with 950°C processing capability at the University of Warwick power device packaging facility

Figure 4-11 shows a sample recipe (profile) that is mostly used for automotive soldering application, mainly for solders with %95.5 Sn, %3.8 Ag and %0.7 Cu particles. Indium 8.9HF Pb-Free solder paste is an example of this type of solder.

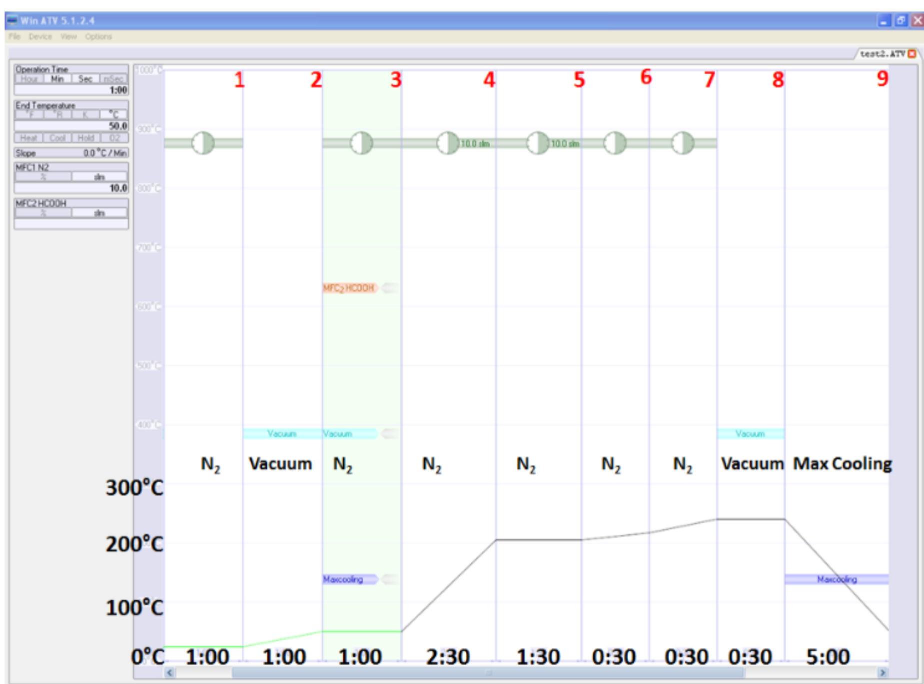


Figure 4-11: Reflow soldering profile for ATV reflow chamber.at the University of Warwick power device packaging facility.

The soldering profile used for packaging the samples in this study has 9 steps. It first starts with injecting N_2 in to the chamber for 60 seconds. Next all the gases in the chamber get vacuumed for a further 60 seconds. This is because void-free solder joints are progressively more needed for power electronics and high-reliability components. These void-free joints are created when the still molten solder is exposed to a vacuum process immediately after the creation of the solder joint. The vacuum stage (stage 2) also makes sure that all the Oxygen in the chamber is emptied and prevents the risk of

oxidising the sample in high temperatures. During this stage the pressure of the inside the reflow oven drops down to 2.3mbar. At the next step, the Nitrogen valve opens and lets the gas enter the chamber while the temperature rises to 50°C. At stage 4, the temperature ramps up to 204°C in a 2:30 mins period. Next stage is the soaking step where the sample is heated to 210°C and kept at that temperature for 30 seconds. This reduces the voids in the solder under the device. At the next stage the temperature ramps up to 217°C to melt the solder and form the metallurgic contact. There is a chance that the device moves during reflow. At the next step the temperature increases to 15-30°C above the solder's melting point and the sample is kept at this temperature for 30 seconds. This step is used to attain a good contact and wetting profile. In this period, the gases in the chamber get extracted to form a vacuum. This process decreases the formation of bubbles that are due to evaporation of the solvent from underneath the solder and helps to place the solder on top of the solder paste (in case it moved in the previous stage). Finally, the sample gets cooled down to room temperature and must be cleaned with Isopropanol to remove any residue of solder flux before wire bonding process.

In order to connect the active area of the device (Anode) to the DBC substrate and other parts of the circuit, wire bonds are used. Wire bonds are thin wires, typically Aluminium (Al), which are connected to the top side of the device using ultrasonic welding process. Before wire bonding process, the DBC pad surface needs to be milled or plasma etched to remove the oxidised surface layer (if there is any). As can be seen

in Figure 4-12, a power device is made from different layers of materials stacked on top of each other.

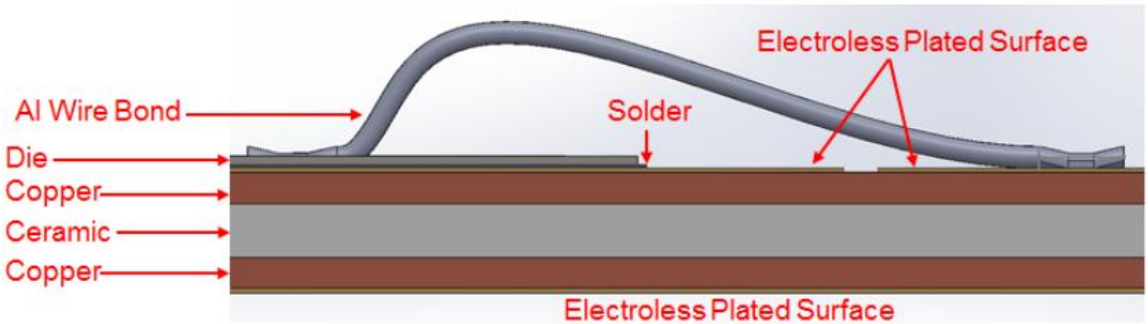


Figure 4-12: A cross section view of a conventional power module packaging showing stack of different materials on top of each other [126]

Figure 4-13 shows a semi-automatic Orthodyne heavy wire bonder used for wire bonding the fabricated SiC PiN diodes. The wire bonder works with Al wires of thicknesses from 0.127 mm (5 thou) to 0.508 mm (20 thou). Authors in [163, 164] have studied the reliability of wire bonding for power electronic modules for various wire thicknesses. It was reported that thick wires can handle less electro-thermal cycles compared to thin wires. The ultrasonic time, power through the first and second bond, force of the bonding tool, the wire's tail length, and height of the wire loop can be set in the wire bonder. In order to attain similar quality of wire bonds and increase the throughput of the process, automatic wire bond machines can be used. Figure 4-14 shows the automatic wire bond tool at Warwick University.

Figure 4-13: Semi-automatic Orthodyne model 20heavy wire bonder

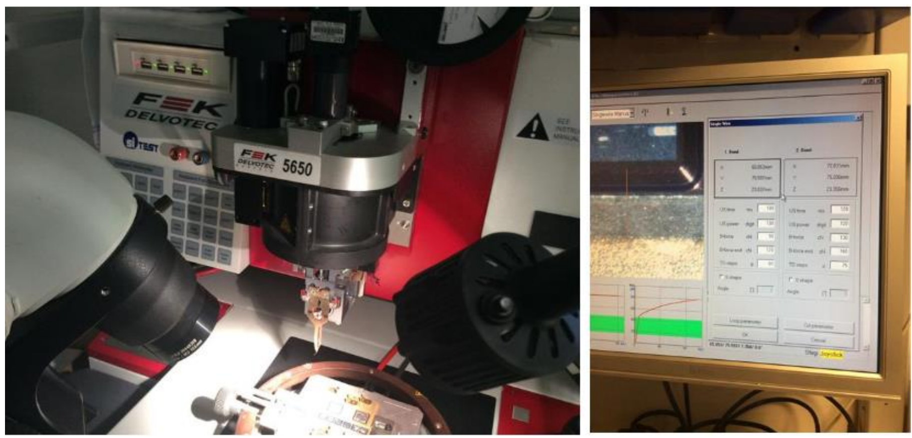


Figure 4-14: FEK Delvotec 5650 heavy automatic wire bonder

Chapter

5 Characterisation Techniques for High Voltage 4H-SiC PiN and Schottky Diodes

This chapter presents the characterisation techniques that were applied to the high voltage 4H-SiC PiN and Schottky diodes fabricated in this thesis. First, the electrical characterisation techniques are discussed including on-state characteristics and reverse blocking at a range of temperatures as well as switching behaviour of the PiN diodes. Moreover, the approach for extracting the carrier lifetime of the fabricated devices using reverse recovery characteristics and capacitance-voltage measurements for Schottky diodes are defined. Subsequently, the physical characterisation techniques are discussed.

5.1 Electrical Characterisation

5.1.1 Forward I-V Measurements

The most important and powerful semiconductor device characterisation tool is the current-voltage (I-V) measurement. I-V measurement can provide the reverse

saturation current, the ideality factor and the on-resistance of the forward-biased PiN and Schottky diode devices as well as the forward voltage drop (V_F), Schottky Barrier Height (SBH) and specific on resistance. Low-current (up to 100 mA) measurements have been carried out at the University of Warwick cleanroom facility using an Agilent Technologies B1500A Semiconductor Parameter Analyser together with a probe station. The probe station was setup for measurement of vertical devices and was equipped with four Karl-Saus probes providing two pairs of sense and force to remove probe resistance.

It was possible to perform on-die measurements at temperatures ranges between 25°C and 300°C using the equipment described here. During forward bias I-V testing, pulsed power measurements were utilised to prevent self-heating of the devices under test.

5.1.2 I-V Measurement at Varying Temperature

The Schottky Barrier Height (SBH) of an interface is a complex parameter that is reliant on temperature. However, the interface quality and the accumulation of imperfections can cause local SBH variations. Looking at the SBH alongside temperature is a useful method to find out information about the nature of the interface.

In order to extract this information at low temperatures, an environmental chamber is used to step down the room temperature 300 K down to 25 K. The die needs

to be mounted and wire bonded to a PCB board to be contacted from outside the chamber to the Agilent Technologies B1500A Semiconductor Device Analyser. The closed cycle cryostat was used to carry out this test, as shown in Figure 5-1. In this Figure, the vacuum chamber case must be removed to load and unload samples. The electrical interface box on the desk, the twin cryogen transfers tubes and the vacuum pipe can also be seen in Figure 5-1. Figure 5-2 shows the PCB mounted die using silver paint ready for testing. The PCB carrier is mounted on a copper block using GE low temperature varnish for heat transfer purposes. Figure 5-3 shows the disassembled chamber and the cold head assembly.

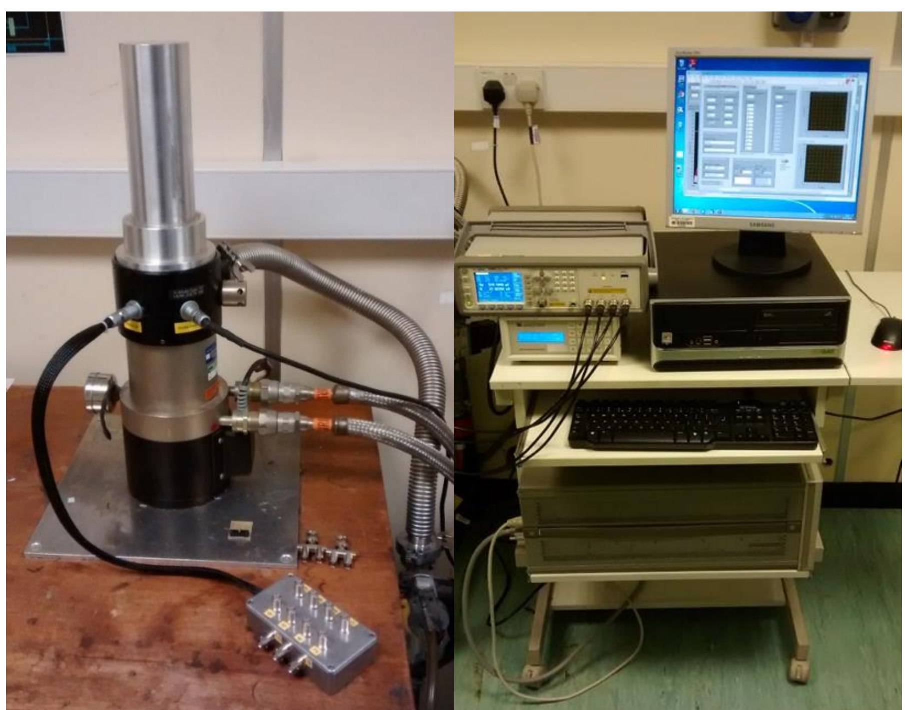


Figure 5-1: Cryostat chamber, electrical measurement and control setup.

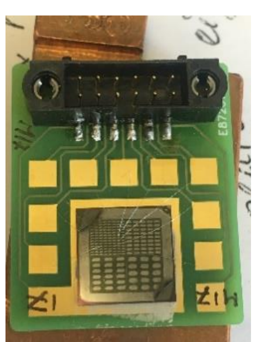


Figure 5-2: The die under test
wire bonded to a PCB.

Figure 5-3: Disassembled chamber and the cold head
assembly.

Figure 5-4 shows I-V-T curves of fabricated 4H-SiC Schottky diode (Chapter 8) taken at temperatures from 25 K up to 320 K with 2 K intervals. The temperature is seen to have a direct effect on the current-voltage curves due to the reliance on temperature of most of the Schottky diode's key parameters. The temperature is seen

to have a direct effect on the plot in Figure 5-4, due to the reliance on temperature of most of the key parameters of the device. For instance, carrier mobility of the device considerably drops with increasing temperature due to the increased vibrations of the lattice which means that there is more scattering phenomenon. This results in increase resistance observed above 1 V. In addition, thermionic emission current rises with increasing temperature, and the built-in potential reduces resulting in the variations in the reverse leakage current of the device and turn-on voltage respectively.

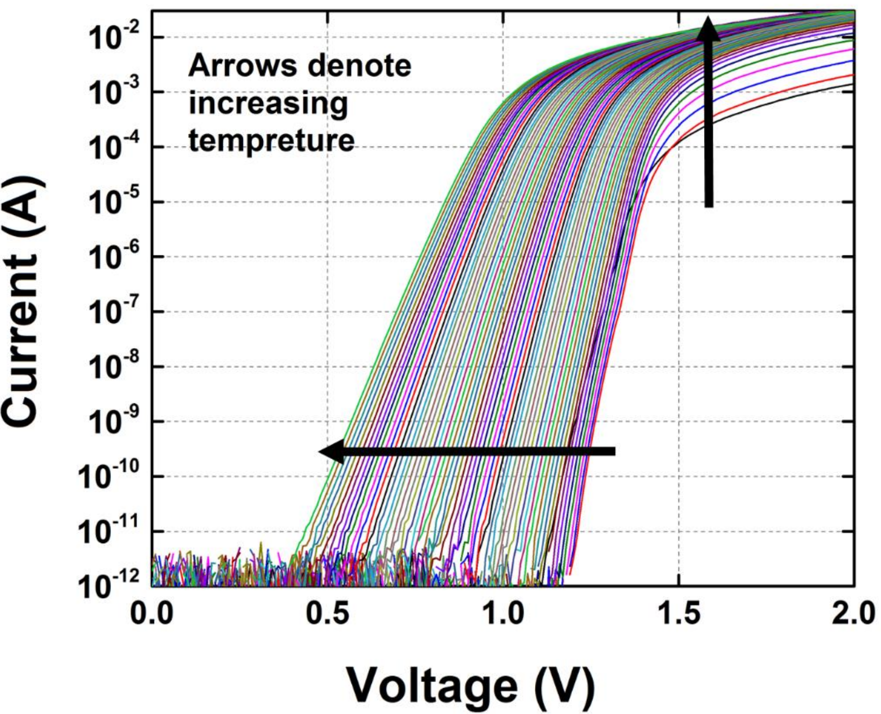


Figure 5-4: I-V-T curves of 4H-SiC Schottky diodes taken at temperature range of 25K to 320K with 2K intervals

The SBH, ideality factor and the saturation current can be extracted from each of the individual I-V plots of Figure 5-4. Although not instantly evident, the SBH and the ideality factor are both dependant on temperature to a similar degree.

5.1.3 Reverse Breakdown Characterisation

Although this is principally a current-voltage measurement, much higher voltages are needed and the current values are considerably lower. Thus, a custom-designed measurement test set-up was developed capable of testing the breakdown voltage of the fabricated devices. At such high voltages, the devices need to be immersed in an insulating liquid (oils or fluorinated hydrocarbons) to avoid arcing. However, the Schottky and PiN diodes fabricated in this work didn't have any Junction Termination incorporated in the design and fabrication, their breakdown voltage was found to be about 840 V. Hence, there was no need to use the insulating liquid when performing the breakdown voltage measurement. Figure 5-5 shows the setup used to achieve the reverse breakdown voltage measurements shown in Figure 5-6. Figure 5-6 shows that the fabricated 4H-SiC Schottky diodes with 35 μm drift region thickness in Chapter 8 are blocking the reverse voltage up to 840V.

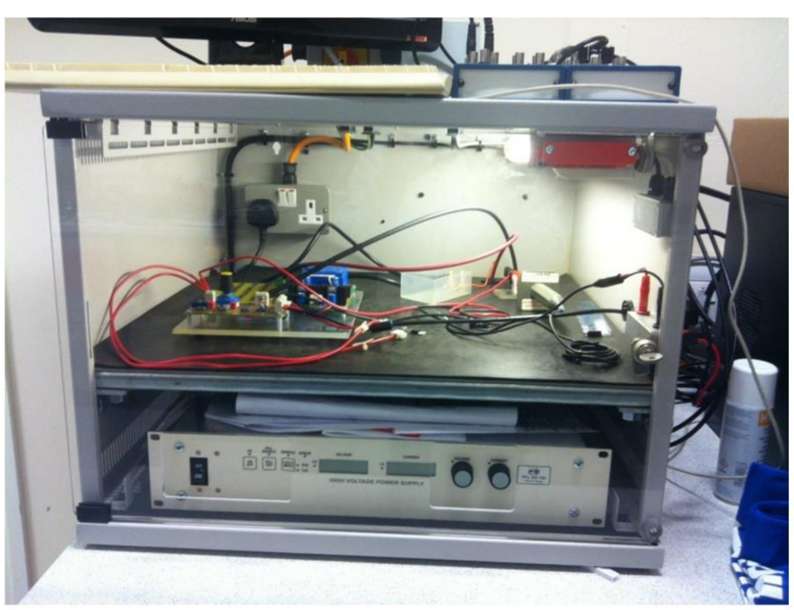


Figure 5-5: High voltage breakdown test rig capable of testing up to 10kV reverse voltages

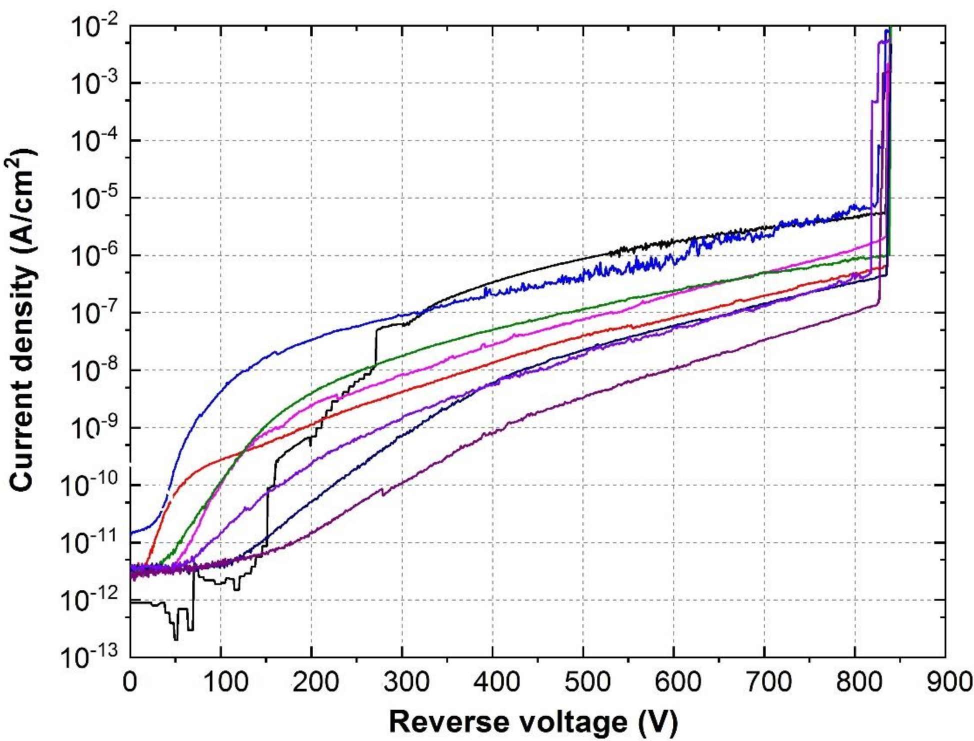


Figure 5-6: Reverse breakdown testing of fabricated 4H-SiC Schottky diodes with 35 μm drift region thickness (no junction termination implemented in the device structure).

5.1.4 Clamped Inductive Switching Test

A clamped inductive switching circuit is shown in Figure 5-7 (a). This test was used to evaluate the switching performance of the fabricated diodes. In this test, a 470 μF DC link capacitor, a 2 mH inductor, and a 1200V/10A rated SiC MOSFET with part number C2M0280120 is used. The gate driver voltage is 18 V. In this test, two pulses are applied to the gate of the switching MOSFET (or IGBT). The inductive load is charged during the first pulse, and the turn-off behaviour of the device under test (the freewheeling diode) is captured during the second pulse. During this test the current commutates from the PiN diode to the switching MOSFET which results in a negative current of the PiN diode. The rate of current commutation relies on the rate of voltage drop across the stray inductance of the switching device and its switching rate. The switching rate can be set using the gate resistance of the switching device, R_G. The stored charge in the device is equal to the area under the current curve in the negative section as shown in Figure 5-8 for the fabricated 4H-SiC PiN diode in this work. The stored charge in the device must be completely extracted for it to fully turn-off.

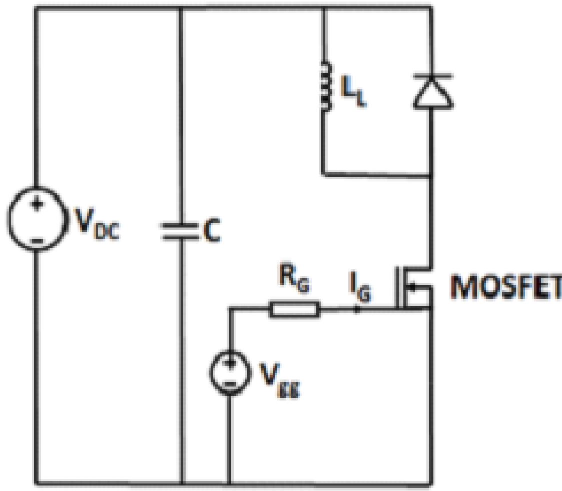


Figure 5-7: Clamped inductive switching circuit.

With regard to the equipment used in this test, a small heater was used for setting the temperature of the device under test (DUT). By leaving adequate time to attain thermal equilibrium, it can be assumed that the junction temperature of the DUT is equal to the temperature of the DBC substrate set by the heater. High voltage, high bandwidth probes were used to measure the diode voltage V_{AK} and the MOSFET drain-source voltage V_{DS}.

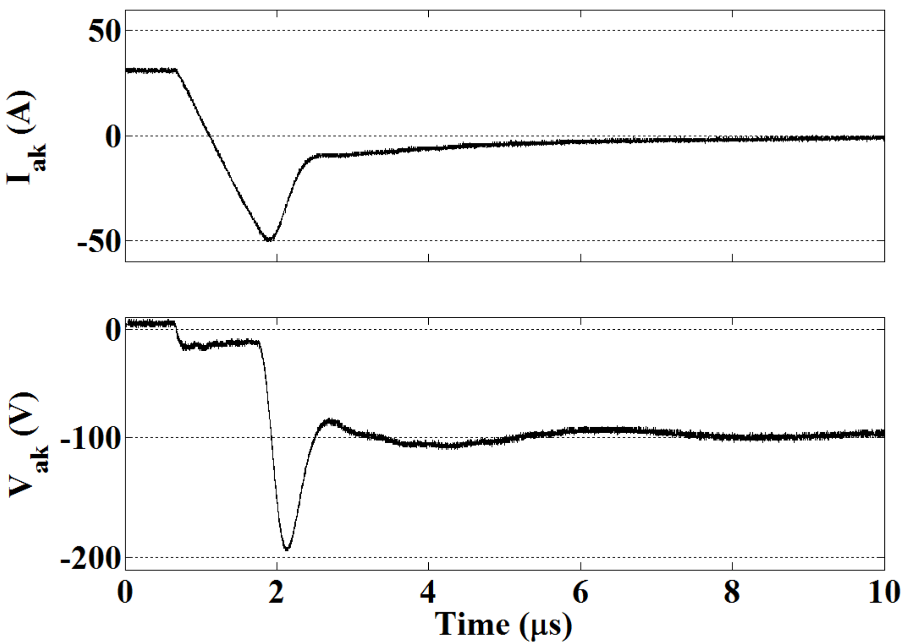


Figure 5-8: Reverse recovery waveform of the fabricated 4H-SiC PiN diode.

5.2 Physical Characterisation

In this Section, the physical characterisation methods that have been employed in the characterisation and analysis of the 4H-SiC PiN and Schottky diodes fabricated in this work are presented.

5.2.1 Scanning Electron Microscopy

In order to characterise the surface defects of 4H-SiC material affecting the electrical performances of fabricated PiN diodes scanning electron microscopy (SEM) has been employed. SEM is a reflection electron beam (ebeam) method that utilises this e-beam to create a magnified image of the sample. The advantage of utilising electron-

based microscopes over optical microscopes is that it permits considerably larger magnification, due to the electron wavelengths being a lot smaller than photon wavelengths, and the depth of field being much greater. According to Equation 5-1 the electron wavelength λe is reliant on the electron velocity v or the accelerating voltage V.

$$\lambda_e = \frac{h}{mv} = \frac{h}{\sqrt{2qmV}} \qquad 5\text{-}1$$

In Equation 5-1, h is Planck's constant, q is the electronic charge and m is the mass of an electron. For an accelerating voltage of 10 kV, the electron wavelength is 0.012 nm. This is much smaller than photon wavelengths of 400 to 700 nm. This assumption demonstrates the benefit of using electron microscopy over optical imaging for higher magnification sampling application. A cross-section of a scanning electron microscope is given in Figure 5-9 [165]. In this thesis, the Zeiss Supra 55-VP FEG-SEM placed in the Physics Department at the University of Warwick was used.

In order to acquire an SEM image, the sample must first be mounted on the stage in the chamber. Then a combination of pumps vacuum both the chamber and the column to facilitate free travel of electrons within the SEM. Typically these high vacuum levels are in the range of 10^5 to 10^7 mbar. Next the electron gun at the top of the column produces and releases a beam of incident electrons, which are accelerated down and passed through a combination of lenses and apertures. Then electron beams are focused using the condenser lenses and then scanned over the surface of the sample. As the electrons interact with the sample, they yield secondary electrons, backscattered

electrons, and specific X-rays. The secondary and/or backscattered electrons are detected to produce an image of the sample. Preferably, the electron beam must be luminous and have a slight energy spread. Of the diverse kinds of electron gun that are utilised in SEM, the field-emission gun (FEG) provides more brightness and energy spread, along with an extended life time.

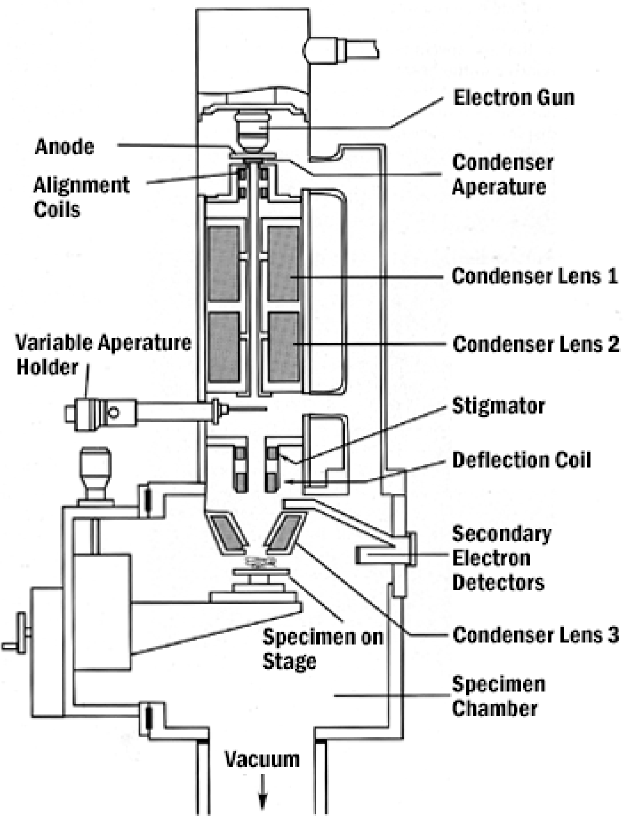


Figure 5-9: Schematic of a scanning electron microscope [165]

Usually incident electron beam energies between 10-30 keV are utilised for most types of sample. These electron energies are reliant on the used magnification.

But, for insulating samples, lower electron energies of the order of several hundred eV, are employed to reduce sample charging.

A typical SEM image is made when an EverhartThornley (ET) detector detects the secondary electrons that are emitted from the K-shell of sample's atoms. This occurs by means of inelastic scattering communications with the incident electrons. ET detector contains a scintillation material that produces light when hit by accelerated secondary electrons. This released light is passed through a light pipe. The emitted light then reaches a photomultiplier placed outside of the SEM column, where the light beam on a photocathode creates electrons that are duplicated and utilised to run the cathode ray display tube (CRT). When the CRT scan and the electron beam scan are synchronised, the morphology of the sample can be visualised. Furthermore, to enable the possibility of storing and seeing the SEM image digitally, the electrons created by the photocathode will be exposed to analogue-to-digital conversion instead of driving a CRT. The ratio of the length of CRT (or digital image) to the length of the sample scan dictates the SEM image magnification. Magnifications greater than 100,000× are achievable in SEMs, yet low magnifications are more challenging. Though the electron beam diameter of FEG-SEM devices are about 0.1 nm, in practice, the resolution that can be realised is normally of poorer quality to this. This is the result of interactions between the electron beam and the sample and the consequent scattering of these electrons [123]. An additional problem that can take place while examining semiconducting samples using SEM is surface charging, which results in the drifting of the SEM image and also its poor quality. This can be overcome by depositing a layer of

conductor to coat the surface of the sample as gold (Au), or by selecting a lower energy electron beam during SEM imaging.

5.2.2 Transmission Electron Microscopy

Transmission electron microscopy characterisation technique, or TEM, has been applied in this work for high resolution imaging of metal-semiconductor interfaces of 4H-SiC Schottky diodes (discussed in Chapter 8), characterisation of defects within a 4H-SiC material specimen and their effect on fabricated PiN diodes (discussed in Chapter 6), and the study of various 4H-SiC surface treatments (discussed in Chapter 8), using Jeol 2000FX TEM and Jeol ARM200F both located in the Physics Department at the University of Warwick. Jeol ARM200F is a Scanning Transmission Electron Microscope STEM with an image resolution <80 picometres. This allows atomic resolution imaging both in STEM and TEM modes. In principle, the TEM is very similar to an optical microscope, as it also uses a set of lenses to magnify the sample. Like the SEM, the TEM also utilises an election gun to create a beam of electrons. The electron beams are then focussed on the sample using condenser lenses. Unlike for the SEM, sample preparation for the TEM analysis is very difficult, time consuming and necessitates specialist equipment. This specifically applies to 4H-SiC material, due to its hardness and chemical inertness.

The Jeol 4500 FIB/SEM which is a Focused Ion Beam Scanning Electron Microscope (FIB-SEM) located in Physics department at the University of Warwick was used to prepare the TEM samples for this research. FIB-SEM uses a focused beam of

electrons to create images of a sample with resolutions higher than 1 nm. The Jeol 4500 has two columns, a 30 kV column with a LaB_6 electron gun used for taking SEM images, and a 30 kV ion column with a Ga^+ ion source to allow FIB cutting. The FIB provides the capability to very accurately cut the samples, and the SEM is capable to image the sample preparation process in real time to give good control to the user. The FIB-SEM is also fitted with a micromanipulator that allows the user to pick up individual particles of a few micrometers in size as well as making a TEM specimen (with nm precision) from a particular area on the sample. These prepared samples (specimens) can then be used in TEM for further characterisation of the material. The sample must be adequately thin, normally a few tens to a few hundred nm, to be transparent to electrons. This avoids the resolution restrictions due to beam spreading experienced in SEM, meaning that exceptionally high resolution, around 0.08 nm, can be realised.

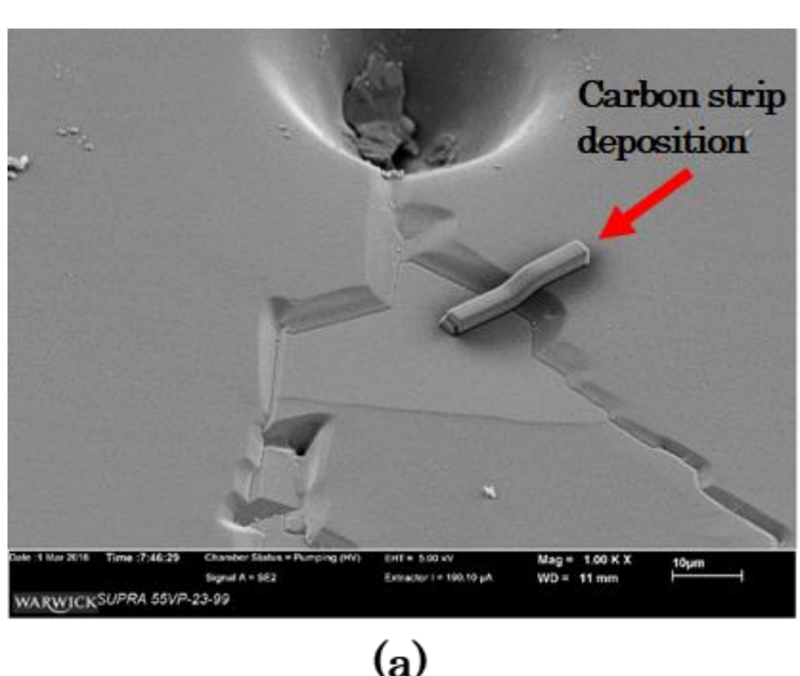
5.2.2.1 TEM Sample Preparation Process

To characterise the triangular defects on the 4H-SiC substrates in Chapter 6, TEM analysis was performed on the samples. In order to do this, the first step was to prepare the TEM samples.

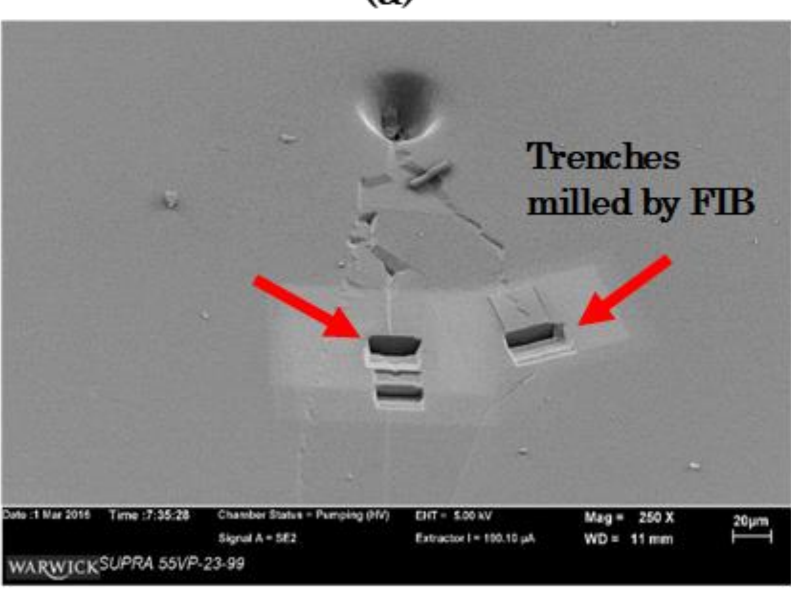
TEM samples were prepared using FIB-SEM. FIB systems operate in a similar technique to SEM, but instead of a beam of electrons, they use a finely focused beam of ions (usually gallium) that can be functioned at low beam currents for imaging or high beam currents for sputtering or milling a certain area. They can obtain 5nm imaging resolution. In integrated FIB-SEM instruments, the stage where the sample is located

is aligned in a way that both FIB and SEM view the same area on the sample. Therefore, the FIB process can be constantly monitored by SEM. Usually, the stage is tilted 52° so that the surface of the sample is perpendicular to the FIB. As a result, FIB can mill a trench perpendicular into the sample while the SEM can view the cross section. The first step in TEM sample preparation is to deposit a layer of carbon to protect the area of interest from the FIB during successive FIB operations. To do this, the defect region was located using the SEM and a strip of carbon was deposited on the area of interest on the defect using FIB, as shown in Figure 6-10 (a). STEM and TEM analysis need the sample to be electron transparent called "lamellas". In the next step, two trenches from either side of the area of interest are milled using the FIB. Figure 6-10 (b) shows several trenches that are milled on the defect area for TEM analysis. Typical dimensions of the trenches are 10-20 μm in width and depth. Following this, the area of interest gets almost separated from the substrate by FIB. As shown in Figure 6-11 (c), the area of interest is only attached from one side to the substrate. At this stage, the thick lamella is attached to a fine needle with a sharp tip, also called a manipulator, by carbon deposition so that it is secured. Subsequently, the thick lamella is completely separated from the substrate by FIB. This is shown in Figure 6-11 (d). The TEM sample grid shown in Figure 6-12 (e) is used for attaching the specimen (lamella) in place by carbon deposition and the FIB is used to completely separate the specimen from the manipulator as shown in Figure 6-12 (f). The specimen requires to be thinned out and polished to be electron transparent (10nm in this study). The final

thinning process is not shown in the TEM sample preparation process shown in Figure 5-12.

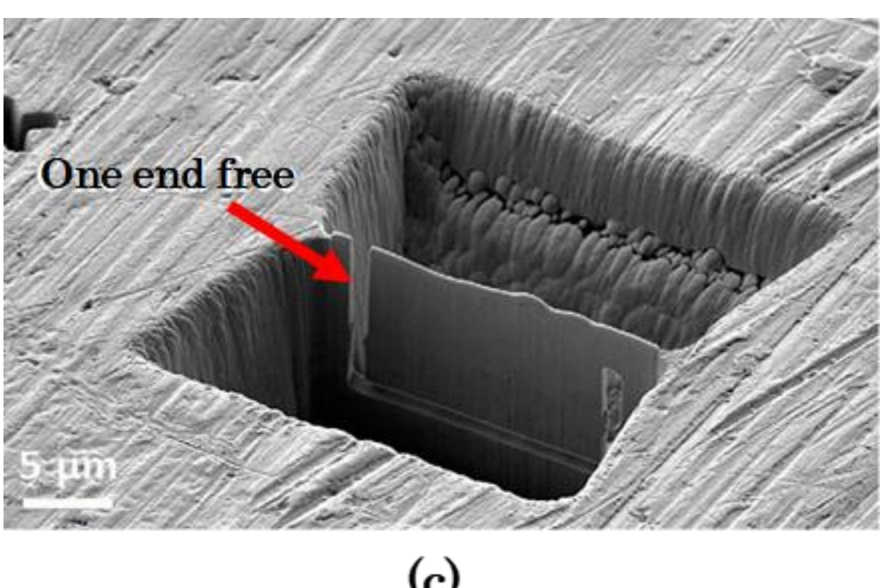


(a)

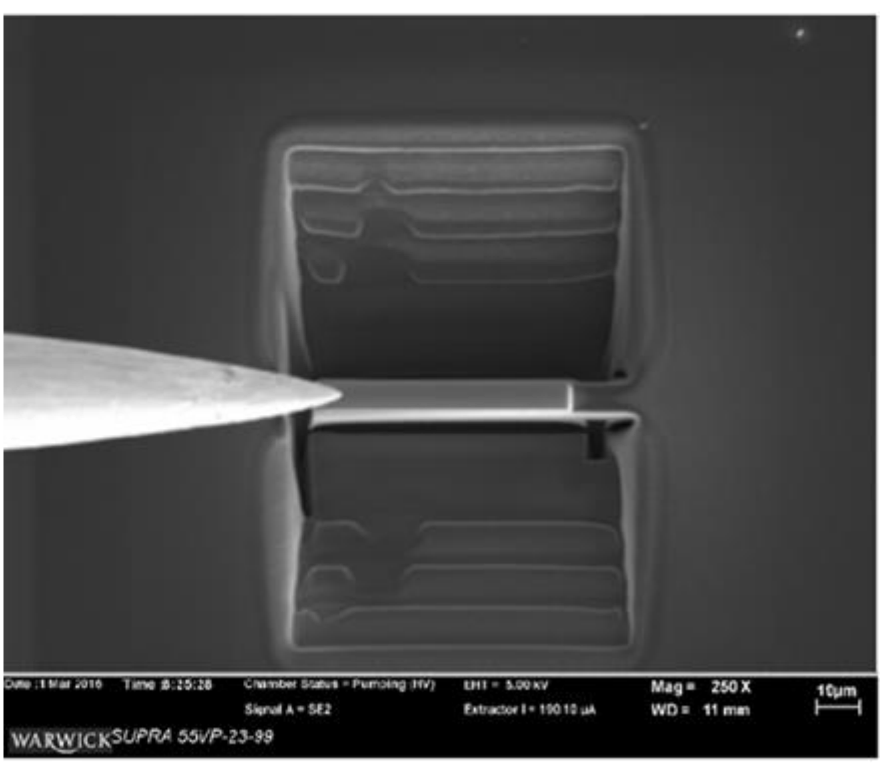


(b)

Figure 5-10: TEM sample preparation using FIB-SEM (a) strip of carbon deposited to protect the surface (b) trenches milled using FIB on either side of the area of interest.

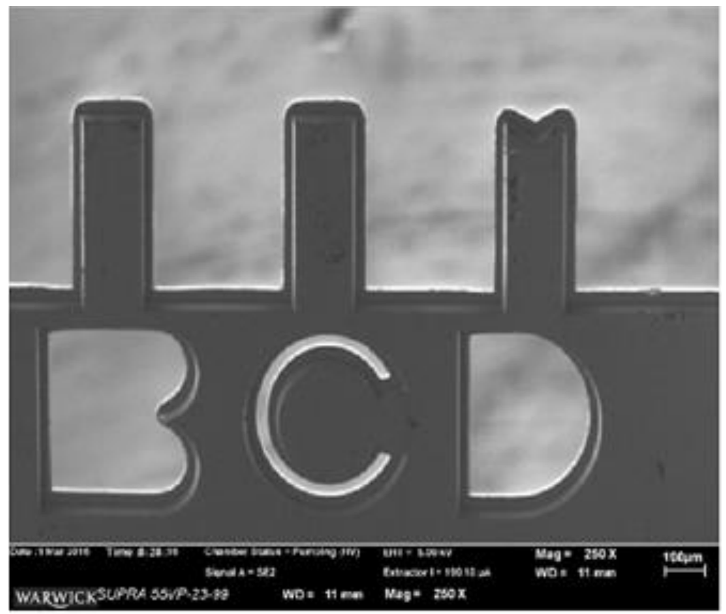


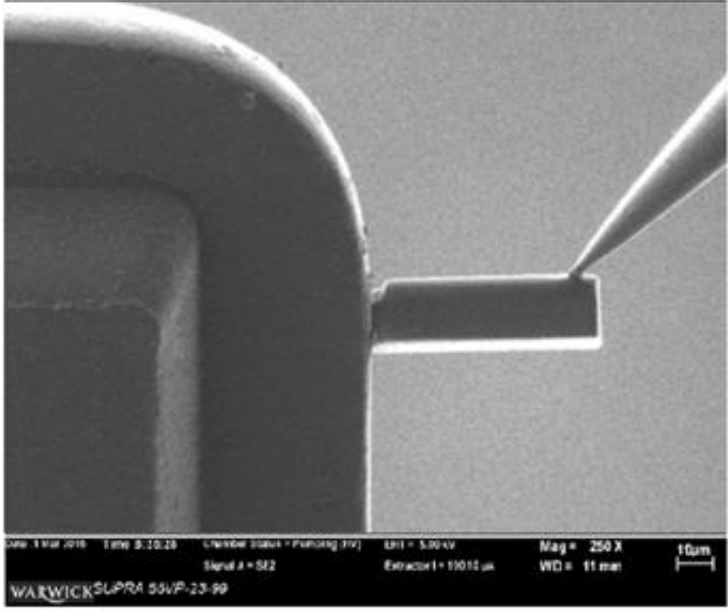
(c)



(d)

Figure 5-11: TEM sample preparation using FIB-SEM (c) the specimen is detached from the substrate from one end using FIB (d) the manipulator is attached to the specimen to lift it out.





(f)

Figure 5-12: TEM sample preparation using FIB-SEM (e) TEM sample grid for holding the specimen in place (f) the specimen is attached to the grid by carbon deposition. FIB is then used to separate the manipulator from the specimen. The specimen needs to be thinned.

5.2.2.2 Scanning Transmission Electron Microscopy (STEM)

In scanning transmission electron microscope images are formed by electrons passing through an adequately thin sample. A typical STEM is a conventional transmission electron microscope fitted with extra scanning coils, detectors and required circuitry. A Jeol ARM 200F microscope was used to perform scanning transmission electron microscopy imaging. In STEM the electron beam is focused to a fine spot (with the typical spot size 0.05 – 0.2 nm). The electron beam is then scanned over the specimen in a raster lighting arrangement assembled in such a way that at each point the sample is illuminated with the beam parallel to the optical axis. This makes STEM a favourable tool for analytical techniques such as Z-contrast annular dark-field imaging, and spectroscopic mapping by energy dispersive X-ray (EDX) spectroscopy, or electron energy loss spectroscopy (EELS). The Jeol ARM 200F microscope has a Gatan Quantum electron energy loss spectrometer EELS to facilitate detection and quantification of the elemental composition down to the atomic level. The microscope also currently has a 100 mm^2 Oxford Instruments windowless energy-dispersive X-ray (EDX) detector. This also provides composition maps with atomic resolution; both EDX and EELS spectra can be acquired at once at high data rates. High resolution scanning transmission electron microscopes need extremely stable room environments. To achieve atomic resolution images in STEM, the level of vibration, temperature variations, electromagnetic waves, and acoustic waves must be limited in the room housing the microscope [166].

5.2.2.3 Electron Energy Loss Spectroscopy (EELS)

Electron energy loss spectroscopy (EELS) uses the energy scattering of electrons that pass through a transparent sample to evaluate the content of the sample and generate images with distinctive contrast effects [167].

EELS equipment is typically integrated into a TEM or a scanning TEM that uses high energy electrons (60 – 300 kV normally) to evaluate the content of the sample. As the name suggests, the electrons must "transfer" through the sample and thus requires an electron transparent sample. The electrons can either interact elastically (with no energy exchange with the sample) or inelastically. EELS uses these interactions to obtain information about the sample.

EELS is known for being a complementary technique to energy-dispersive x-ray spectroscopy (also called EDX, EDS, XEDS, etc.), which is another common spectroscopy characterisation method existing on numerous electron microscopes. EDX is used to detect the atomic arrangement of a material, is relatively simple to use, and is predominantly sensitive to heavier elements. EELS has traditionally been a more challenging technique, but is generally able to measure atomic composition, chemical bonding, electronic properties of valence and conduction band, surface properties, and element-specific pair distance distribution functions [168]. EELS operates best at moderately low atomic numbers and is best established for the elements ranging from carbon through the 3d transition metals (from scandium to zinc) [169]. This technique can be studied to detect the oxidation states of the atoms [170]. The advantage of EELS

over EDX is that it is capable to "fingerprint" diverse forms of the same element. The dissimilarity is mostly due to the dissimilarity in energy resolution between the two techniques (~1 eV or better for EELS, possibly a few tens of eV for EDX).

5.2.2.4 Energy-Dispersive X-Ray Spectroscopy (EDX)

Energy-dispersive X-ray spectroscopy (EDX), is a technique used for the elemental analysis or chemical characterisation of a sample. It is dependent on an interaction of an X-ray excitation source and a sample. Each element has an exclusive atomic structure and hence a unique rage of peaks on its electromagnetic emission spectrum [171, 172]. EDX owes its characterisation abilities to this fundamental principle of spectroscopy.

A high energy beam of excited particles such as electrons or protons or a ray of X-rays needs to be concentrated on to the sample under test to motivate the radiation of characteristic X-rays from it. When a sample is at rest, its atom comprises ground state (or unexcited) electrons in separate energy levels or electron shells that are bound to the nucleus. An electron in an innermost shell may be excited by the incident beam causing it to be ejected from the shell. This creates a hole in the location where the electron used to be. Then the hole gets filled by an electron from an outer, higher-energy shell. Hence, the change in energy among the higher-energy shell and the lower energy shell will be omitted as an X-ray. The energy of this released X-ray from a sample can be measured using an energy-dispersive spectrometer. Since the energies of the X-rays are representative of the alteration in energy amongst the two shells and of the atomic

arrangement of the releasing element, EDX facilitates the measurement of the elemental composition of the sample.

5.2.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is a physical characterisation method that facilitates the measurement of the surface morphology of samples with atomic resolution in the z-axis, merging the characteristics of a stylus profilometer with surface force tool. Figure 5-13 illustrates the fundamental parts of an AFM. In this thesis, the AFM

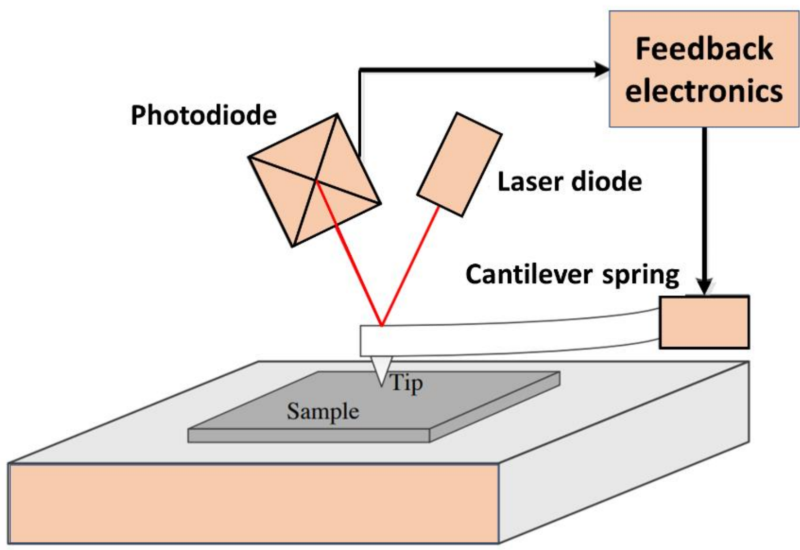


Figure 5-13: Schematic of an atomic force microscope showing the basic components of an AFM

characterisation has been performed using the Asylum Research MFP-3D AFM, located in the Physics Department at the University of Warwick.

An AFM image is obtained by scanning the cantilever tip over the surface of the sample, with the x- and y-axis scanning controlled using piezoelectric blocks. When the cantilever tip is brought into close proximity with the surface of the sample, forces between the tip and the sample result in a deflection of the cantilever, in accordance with Hooke's law. This deflection is measured using a laser beam, which is reflected off the top of the cantilever into an array of photodiodes, with any change in displacement of the cantilever resulting in a change of output signal from the photodiode array. This signal is passed to the feedback electronics, which controls the cantilever. There are several different methods for controlling the cantilever, though all AFM imaging performed in this work has been done using AC (or tapping) mode. This mode of operation involves driving the cantilever to oscillate up and down near its resonant frequency, and, due to the interaction of forces acting on the cantilever when the tip approaches the sample surface, the oscillation amplitude decreases with a decrease in distance between the tip and the sample. The height of the cantilever above the sample is controlled using a piezoelectric actuator, with the feedback electronics responsible for adjusting the cantilever height in order to maintain a set oscillation amplitude during the AFM scan. Using AC mode for AFM imaging is advantageous in that it circumvents the problem of the cantilever tip sticking to the sample surface, which can be problematic for non-contact AFM imaging when performed under normal ambient conditions. Furthermore, using AC mode minimises the damage done to the sample surface and the cantilever tip during AFM imaging.

5.2.4 Photoluminescence

Photoluminescence (PL) mapping or imaging technique allows simple and non-destructive recognition of dislocations and stacking faults in SiC specimens. It can be used for impurity levels and defect detection as well as assessing the material quality. PL has been applied in this work to characterise the 4H-SiC material quality and defect detection.

In PL a laser beam is directed on to the sample, where it is absorbed and the light generated from a substance is captured as it falls from the excited state to ground state. This process is called photo-excitation which causes the material to jump to a higher electronic state, it will then release energy in the form of photons as it relaxes and returns back to a lower energy level. The luminescence or radiation of light over this process is called *photoluminescence*. By assessing the luminescence spectrum, material imperfections and impurities can be observed. The results of PL analysis employed in this research in discussed in Chapter 6 where a PL spectrum is presented.

Individual dislocation types (TSD, TED, and BPD) can be easily identified by a non-destructive micro PL mapping technique. For example, it was reported in [173] that the PL density mapping on 4H-SiC epilayers intentionally doped to 1×10^{15} cm^{-3}. The image of micro PL intensity mapping at 390 nm (near band-edge emission) at room temperature is illustrated in Figure 5-14(a). This experiment was carried out on a 72 μm-thick n-type 4H-SiC epilayer. Three circular regions with less PL density can be seen. These regions represent the areas of non-radiative recombination centres.

Between these three circular regions, two of them are larger in size rather than the third region representing difference in defects. Figure 5-14(b) shows the optical microscopy image after molten KOH etching on the same surface of the sample at 480°C for 10 min. Three threading dislocations are revealed by characteristic etch pits. In these figures, there is a one-to-one correlation between the circular areas with reduced PL intensity and threading dislocations. It should also be noted that a TSD exhibits a larger and darker circular area in micro PL intensity mapping than a TED.

Authors in [173] monitored more than 200 dislocations by micro PL mapping and etch pits, and obtained a similar result. This result suggests that TSDs have a more pronounced impact on the non-radiative recombination activity than TEDs. Detection of BPDs is easy, because long dark lines along the off-direction can be observed in micro PL mapping, and in many cases, a BPD is dissociated into two partial dislocations and a Shockley-type stacking fault is formed between them during PL measurement, as reported in [173].

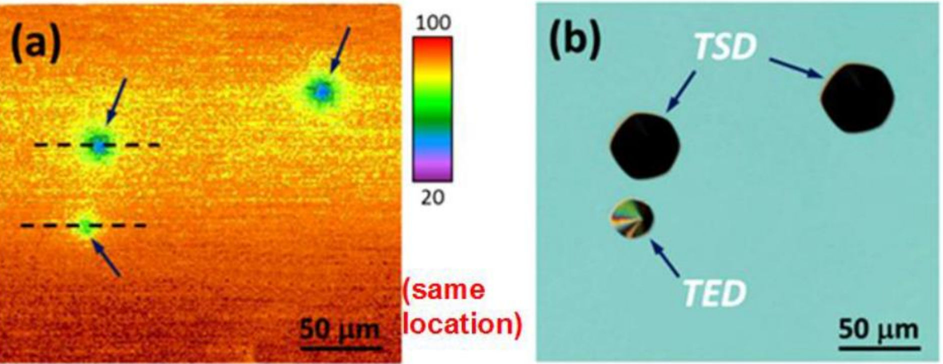


Figure 5-14: (a) Micro PL intensity mapping at 390 nm (near band-edge emission) at room temperature obtained from a 72µm thick n-type 4H-SiC epilayer intentionally doped to 1×1015 cm-3. (b) Optical microscopy image of the sample surface (same location) after molten [166]

Chapter 6 The Impact of Triangular Defects on Electrical Characteristics and Switching Performance of 3.3kV 4H-SiC PiN Diode

In this Chapter the impact of a surface morphological defect, a triangular defect on fabricated 4H-SiC PiN diodes is explored. Triangular defects are commonly found in commercially available 4H-SiC wafers available in the market (even prime grade wafers) and have a high enough defect density that if a device with a large enough active area is fabricated on them, the probability that it could contain such macroscopic defect increases and hence its electrical performance could be limited. In this Chapter several methods are introduced to characterise these defects before 4H-SiC PiN diodes are intentionally fabricated on the triangular defects (referred to as "on-defect") and in areas with no visible morphological defects (referred to as "off-defect"). They are then electrically characterised. Wafers with three epilayer thicknesses are used, namely 35 μm (PiN1), 30 μm (PiN2), and 110 μm (PiN3) in order to understand their impact on the resulting electrical characteristics and switching performance. It is shown for the

first time the impact of triangular defects on switching characteristics and electrical performance of 4H-SiC PiN diodes fabricated on and off-defects. Moreover, TEM images obtained from the defects were used to explain these electrical results and understand the formation mechanism of triangular defects. On-state behaviour and reverse characteristics of the PiN diodes fabricated on- and off- the defects were also analysed.

This Chapter provides a background on macroscopic defects in Silicon Carbide material and the importance of this study. It first discusses the electrical performance of devices fabricated in areas with no visible defects. It then uses the developed device fabrication process as a benchmark for characterising the devices with the same active area that are intentionally fabricated on-defect. Following this, the Chapter provides detailed results on the material characterisation, electrical performance of the fabricated 4H-SiC PiN diodes on- and off-defects and clamped inductive switching tests results.

6.1 Background

As discussed in Chapter 2, 4H-SiC commercial wafers that are employed for device fabrication contain a range of crystal imperfections which can affect the performance and reliability of semiconductor devices that are fabricated on them. Triangular defects are one of the most common surface morphological defect that can be found on 4H-SiC wafers. Triangular defects are usually generated due to technical problems during epitaxial growth such as downfall. The existence of these defects are

detrimental to SiC devices as they result in a considerable increase in leakage current and reduction in blocking voltage. TEM analysis has revealed that triangular defects exhibit a variety of structures, such as 3C-SiC. Since triangular defects can be found in all commercial 4H-SiC wafers and have high enough density, it is important to study the characteristics of these defects, their impact on the performance of the devices that are fabricated on them and understand the formation mechanism of these defects. To do this, 4H-SiC PiN diodes were fabricated on the defects to study their behaviour.

6.2 Experimental Details and Results

The PiN diodes used in this work were fabricated in-house using three different 4-inch n-type (0001) Si face, 4° off axis 4H-SiC wafers. The first wafer (forming PiN1) was acquired from supplier A, and consisted of a 1 µm p-type top contact doped at $1.5x10^{19}$ cm^{-3} on top of a 35 µm thick drift region of $2x10^{15}$ cm^{-3} n-type doping. The two other wafers were acquired from supplier B, both grown consecutively to avoid any significant differences Both wafers had a top contact layer of 1µm thick p-type doping up to $1x10^{19}$ cm^{-3}, whilst wafer one had a 30 µm thick drift region with $2x10^{15}$ cm^{-3} n–type doping (PiN2), while the other had an even thicker drift region of 110 µm with n–type doping of $6x10^{14}$ cm^{-3} (PiN3). All three wafers are prime grade.

6.2.1 Material Characteristics

In this Section, the results of the characterisation techniques that have been employed in the characterisation and analysis of the 4H-SiC material prior to device fabrication (on- and off the defects) are presented. The 4H-SiC material of all three samples were characterised using non-destructive characterisation methods such as AFM, photoluminescence, and SEM.

6.2.1.1 Atomic Force Microscopy

In order to examine the morphology of the surface prior to fabrication, several 20×20 μm AFM scans were performed on each SiC substrate, of which, two are shown in Figure 6-1 for wafers PiN2 and PiN3. AFM characterisation technique is discussed in detail in Chapter 5. The first image (a) shows the onset of step bunching and defect formation caused by epitaxial growth, whereas the thicker substrate (b) shows a definite step bunching and the surface steps are not visible. In Figure 6-1 (a), the PiN2 epilayer has an RMS surface roughness of 2.96 nm, compared to 13.43 nm for PiN3. The PiN1 substrate has an RMS of 1.4 nm.

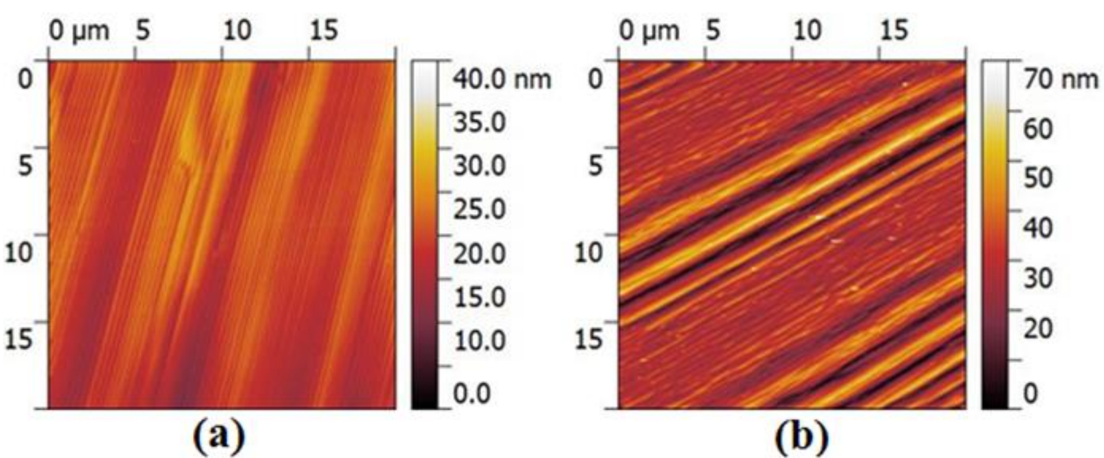


Figure 6-1: 20 x 20 µm2 AFM image taken of SiC surface of samples with (a) 30 µm epitaxial layer with RMS surface roughness of 2.96 nm (PiN2) (b) 110 µm epitaxial layer with RMS surface roughness of 13.43 nm (PiN3).

6.2.1.2 Photoluminescence

Photoluminescence spot analysis was performed in the triangular defect area and the bulk area using a 325 nm wavelength source, shown in the optical microscopic view of PiN2 in Figure 6-2. PiN1 and PiN 3 showed similar PL spectra to the one shown in Figure 6-2.

Photoluminescence spectroscopy technique is previously discussed in Chapter 5. A photon is characterised by either a wavelength (λ) or equally an energy (E). The relationship between the energy of a photon (E) and the wavelength of the light (λ) is shown again in the equation below for convenience:

$$E(eV) = \frac{hc}{\lambda(\mu m)} \quad \text{6-1}$$

where h is Planck's constant (6.626×10^{-34} joule·s) and c is the speed of light (2.998×10^{8} m/s):

The location of the defect can be specified using an optical microscope. The peak corresponding to 4H-SiC (380 nm) was detected in the spectra, both on-defect and in the bulk area. The spectra on the defect indicated the existence of stacking faults (SF from 420nm-564nm), Threading Edge Dislocations (TED range>700nm peaking at>900nm), Threading Screw dislocations (TSD from 600-1000nm), and other polytypes [174]. As discussed earlier, in some triangular defect the triangular area is actually 3C-SiC. For 3C-SiC crystal, the PL spectrum exhibits two distinctive peaks, one at 439nm and the other at 592 nm [175]. As shown in Figure 6-2, the PL spectrum of the defect area (shown using a red cross on the microscopic image and red trace on the PL spectra) shows a PL peak at 439nm, confirming the existence of a cubic (3C-SiC) region in the triangular defect, just below the downfall and the PL peaks around 592nm can also be seen. Hence, photoluminescence spectroscopy can be used as a non-destructive spectroscopic technique to detect the existence of triangular defects prior to device fabrication in device manufacturing industries. However, since state of the art 4H-SiC substrates still suffer from defects, due to the high cost of the wafer, it is not cost-effective for the whole wafer that contains macroscopic defects to be completely un-usable. Hence, manufacturers can continue to fabricate the power devices on the whole substrate, but at the end of the production line and in quality-check stage of the fabricated devices, the defective devices can be detected using their electrical characteristics. Therefore, it is vital to see the effect of these macroscopic defects on the electrical performance of the fabricated devices. Later on in this Chapter, the electrical

characteristics of the PiN diodes fabricated on and off the defective areas are assessed to distinguish devices that are fabricated on a defective wafer [115]. But, before device fabrication, SEM analysis, was performed on the defect area to analyse its physical characteristics.

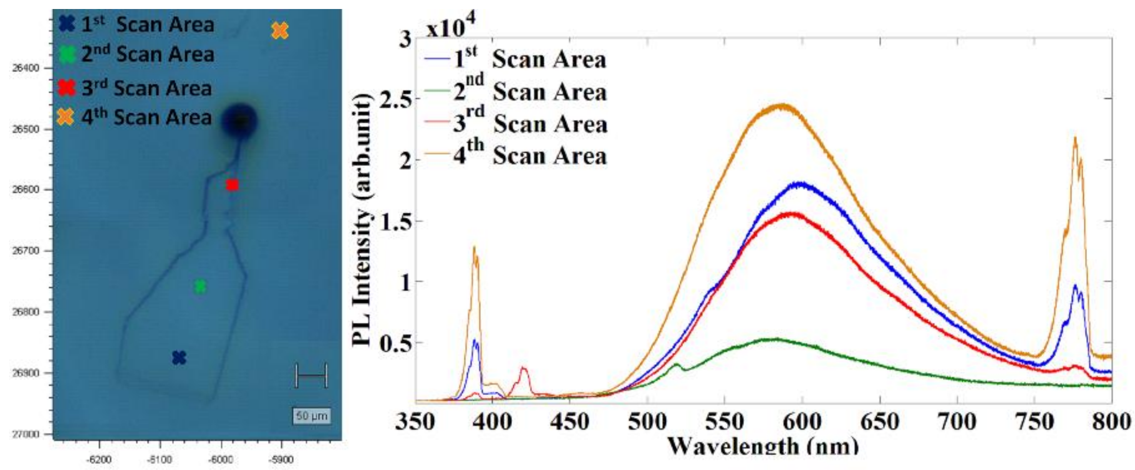
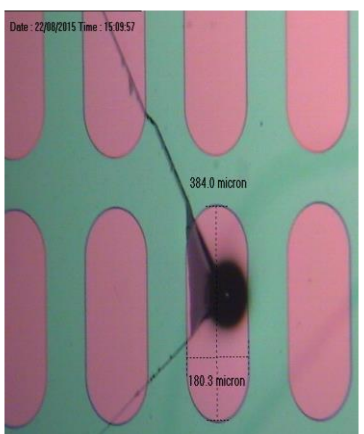


Figure 6-2: PL images using 325 nm wavelength source at the defect (1st, 2nd, and 3rd scan area) and bulk (4thscan area) area and the optical microscopic view of a 30 µm (PiN2) epitaxial layer sample.

6.2.2 Scanning Electron Microscopy

Figure 6-3 shows the microscopic pictures of fabricated diodes with different sizes on triangular surface defects. It can be seen that a single defect can spread across several diodes that are fabricated on them and could have detrimental effect on their electrical performance.



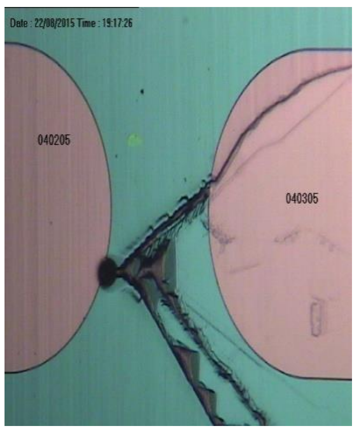
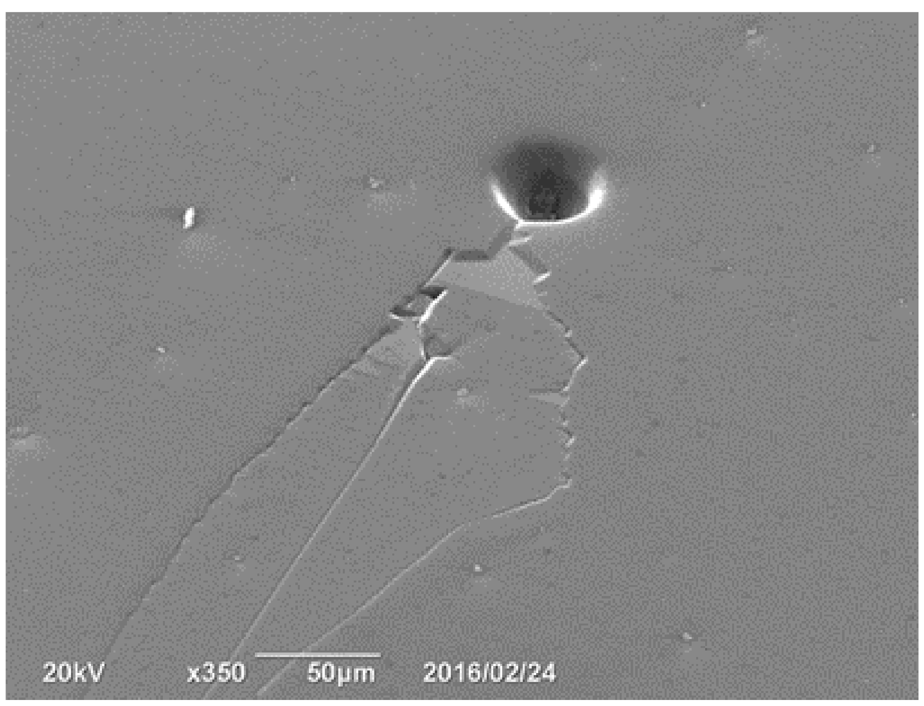


Figure 6-3: fabricated on triangular defects on PiN1 (left) and PiN3 (right).

Figure 6-4 shows SEM images of the triangular defects on PiN2 and Figure 6-5 shows the SEM image of a triangular defect on PiN3 with 110 μm drift region thickness. It can be seen in both Figures that the triangular surface defects have a large spherical pits located at the top of the triangular region which is due to a downfall particle. In the SEM image the foreign material (downfall) is also visible which is thought to have dropped from a CVD furnace environment at the initial stage of the epitaxial film growth process and are the origins of the surface defects. Bending, wavy and step-like vertical fine lines were observed on the surfaces as well (also seen in AFM results), as shown in Figure 6-6.



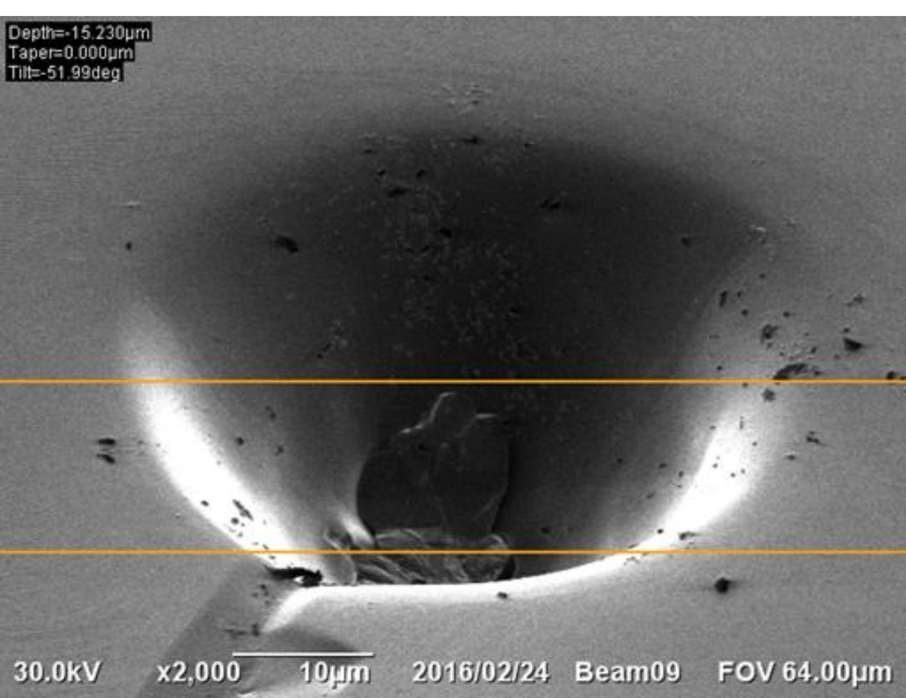


Figure 6-4: High resolution SEM images of a triangular defect on PiN2 showing the foreign particle which is the origin of the triangular defect.

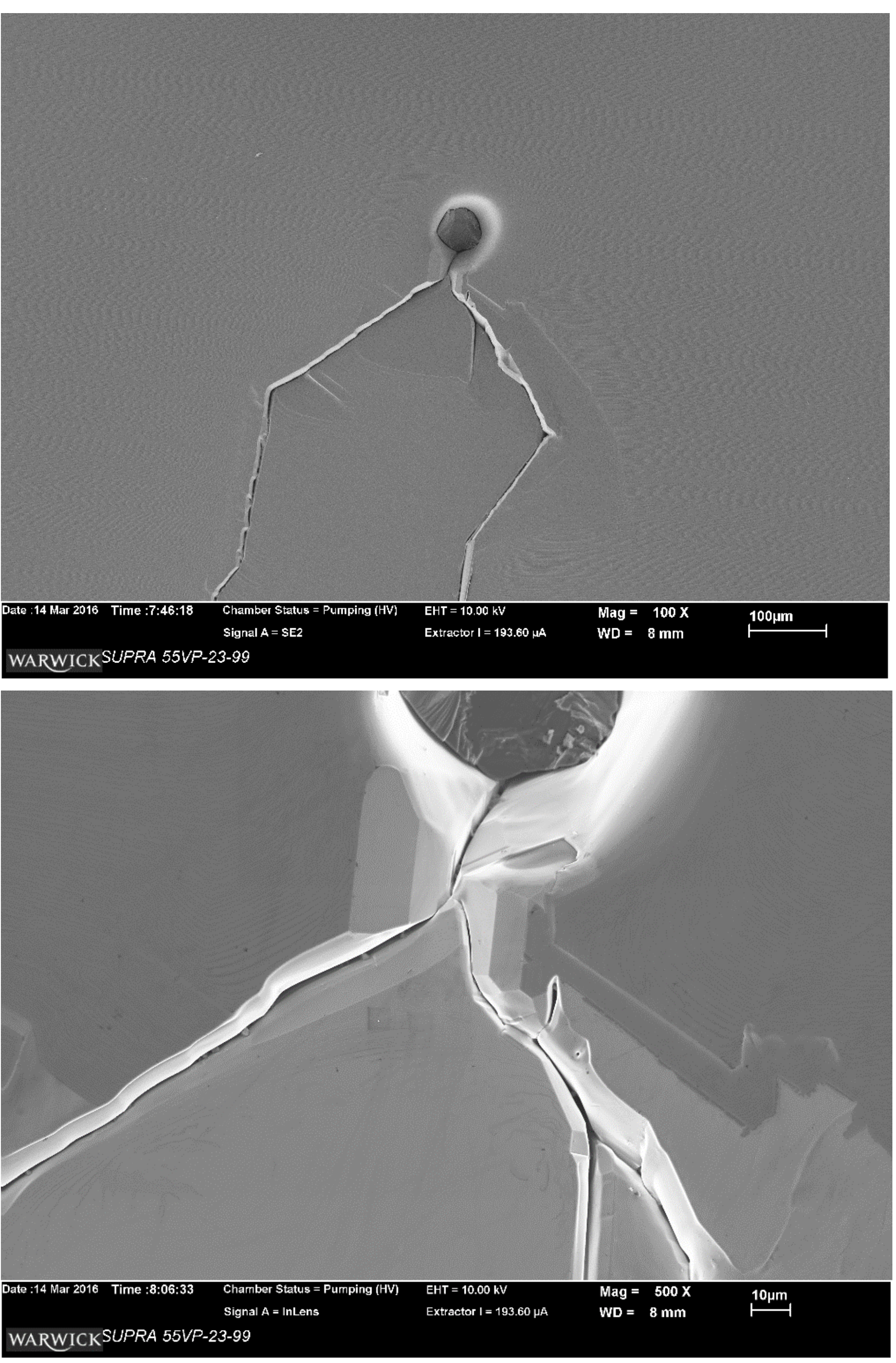


Figure 6-5: High resolution SEM images of a triangular defect on PiN3.

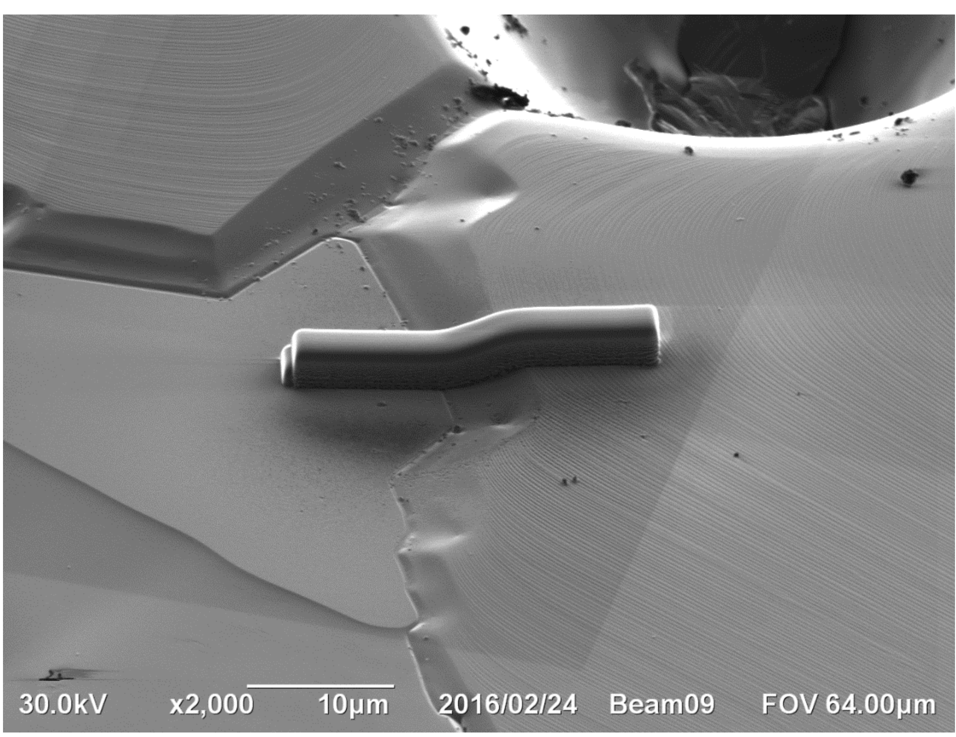


Figure 6-6: High resolution SEM image of PiN1, showing the step-bunching and bending, wave shape lines on the surface.

6.2.3 Device Fabrication

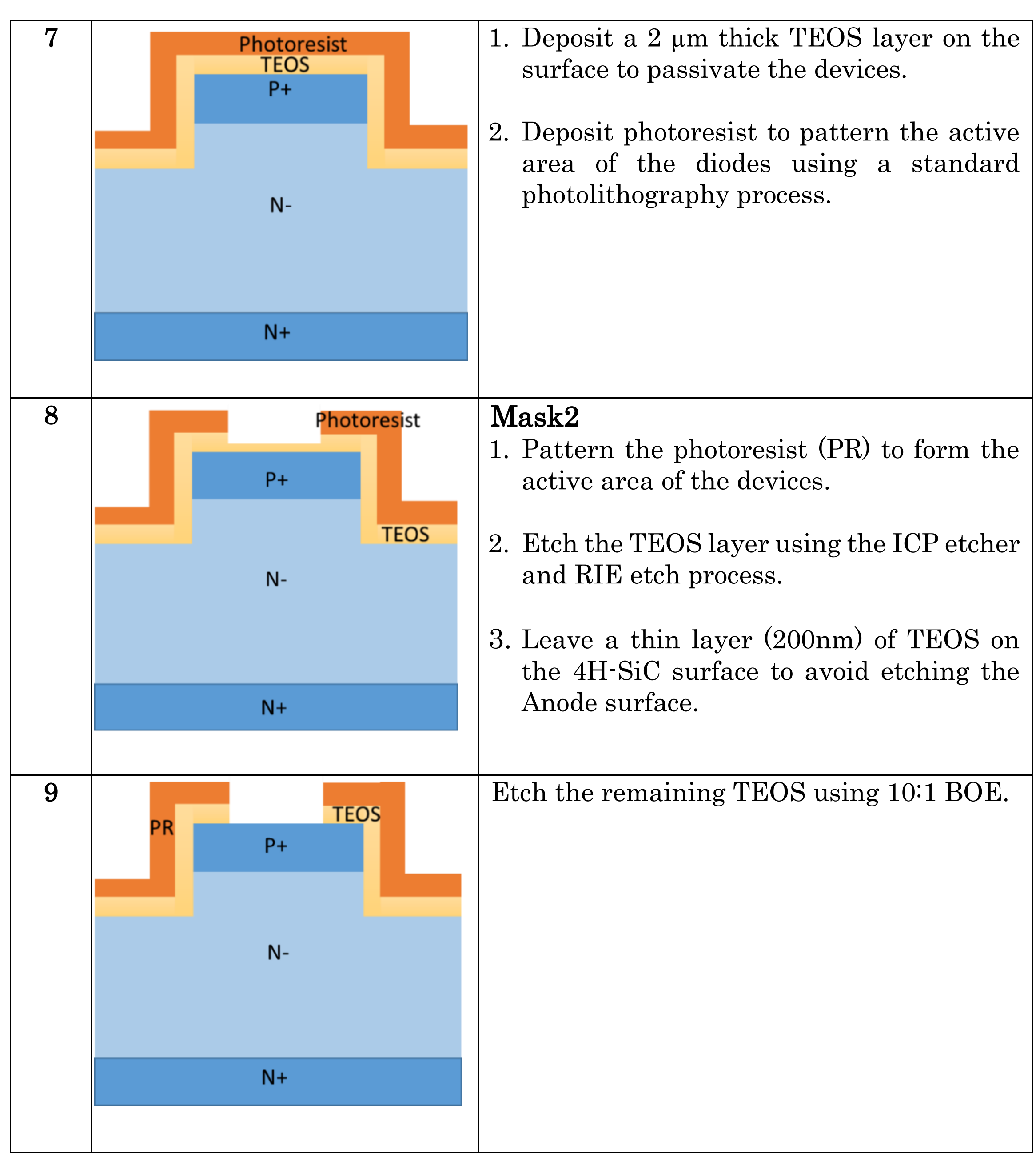
The fabrication process of the PiN diodes in this study is presented in the device fabrication process flow in Table 6-1. All the processing techniques that were used in the fabrication process (shown in Table 6-1), such as wafer cleaning process, surface passivation, etching of SiC, ohmic contacts to 4H-SiC, and device packaging process are previously explained in Chapter 4. During step 3 of the fabrication process, the active area of devices on-defect are intentionally placed on triangular defects and the active area of the rest of the devices are on areas with no visible defects (off-defect). The active

area of the small area devices was 4.53 x 10^{-4} cm^2. Figure 6-7 shows a cross-section view of a proposed DBC mounted PiN diode die and the electrical impact of triangular defect on the device. Each die contains over 90 PiN diodes of varying active areas.

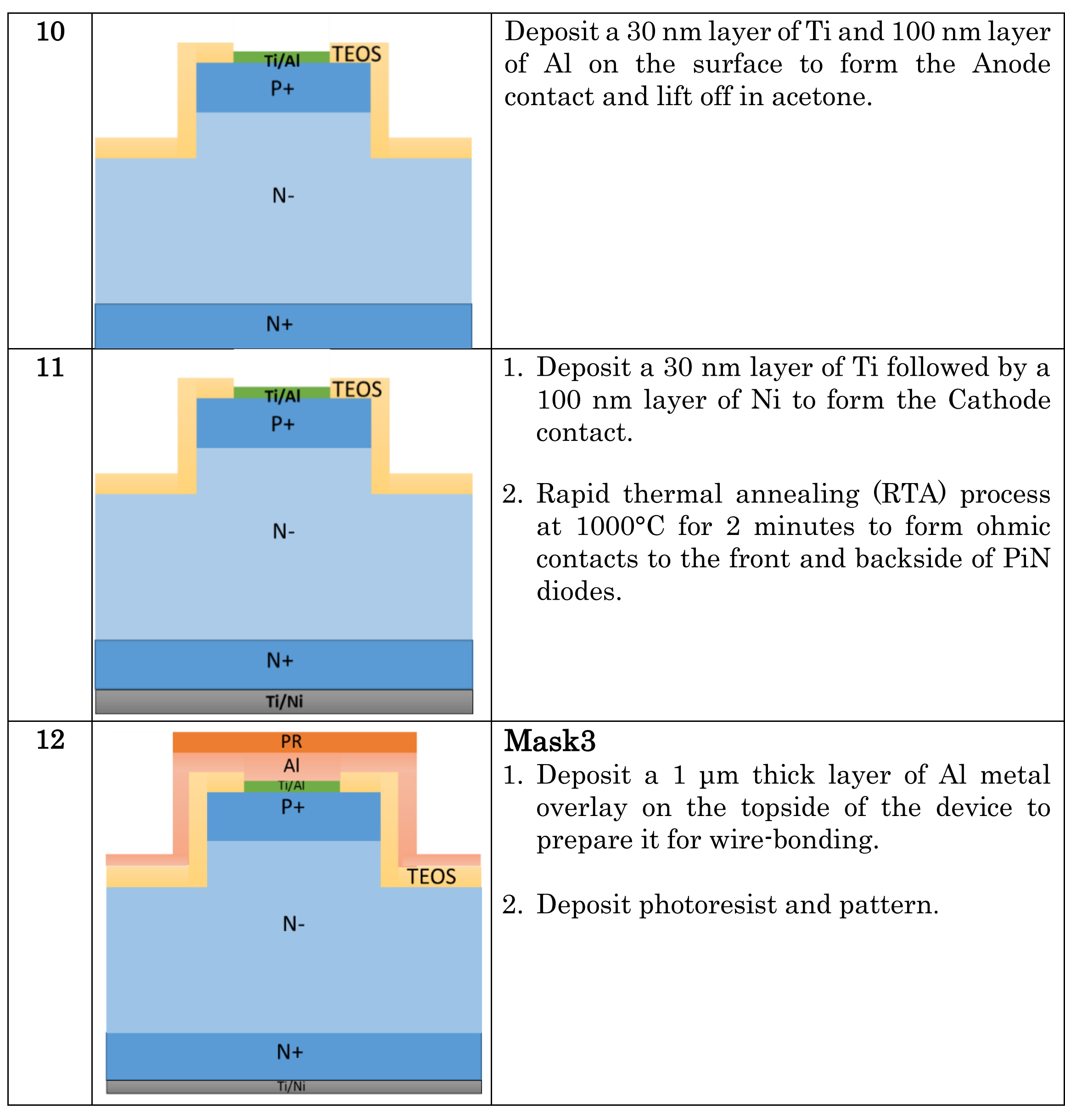
Table 6-1: 4H-SiC PiN diode fabrication process flow.

Step	Cross-sectional diagram	Fabrication process
1	P+ N- N+	Clean the samples using the wafer cleaning process as discussed in Section 4.1.2.
2	Ni TEOS P+ N- N+	• Deposit a 1 µm layer SiO_2 TEOS and 300 nm of Ni as masking layers for 4H-SiC etching process. Ni was deposited using E-beam evaporation system.

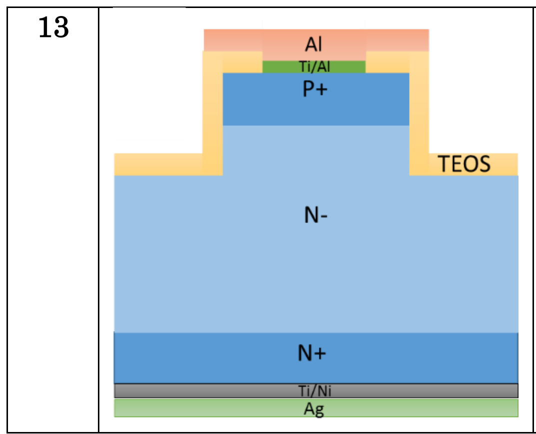
3	Photoresist Ni TEOS P+ N- N+	**Mask1** Deposit photoresist and pattern to mesa-isolate the individual Anodes.
4	Photoresist Ni Teos P+ N- N+	1. Etch the Ni layer in Ni wet etch solution (Nitric Acid (HNO_3), Acetic Acid (CH_3COOH), Sulfuric Acid (H_2SO_4) and DI waster in the ratio 4:4:1:10) for 30 seconds. 2. Etch the TEOS layer in the ICP etcher using RIE etch process to obtain a vertical sidewall profile.
5	Ni TEOS P+ N- N+	1. Remove photoresist in an O_2 plasma. 2. Etch the 4H-SiC to the required depth (1.6 μm in this case) to form the mesa-isolation of Anodes area (mesa etch) in the ICP etcher, using ICP etch process. The etch rate of the process was 700 nm/min.
6	P+ N- N+	1. Remove the Ni layer in Aqua Regia solution. 2. Remove the remaining TEOS layer in 10% HF.



Step	Diagram	Description
7		1. Deposit a 2 μm thick TEOS layer on the surface to passivate the devices. 2. Deposit photoresist to pattern the active area of the diodes using a standard photolithography process.
8		**Mask2** 1. Pattern the photoresist (PR) to form the active area of the devices. 2. Etch the TEOS layer using the ICP etcher and RIE etch process. 3. Leave a thin layer (200nm) of TEOS on the 4H-SiC surface to avoid etching the Anode surface.
9		Etch the remaining TEOS using 10:1 BOE.



Step	Cross-section	Description
10		Deposit a 30 nm layer of Ti and 100 nm layer of Al on the surface to form the Anode contact and lift off in acetone.
11		1. Deposit a 30 nm layer of Ti followed by a 100 nm layer of Ni to form the Cathode contact. 2. Rapid thermal annealing (RTA) process at 1000°C for 2 minutes to form ohmic contacts to the front and backside of PiN diodes.
12		**Mask3** 1. Deposit a 1 µm thick layer of Al metal overlay on the topside of the device to prepare it for wire-bonding. 2. Deposit photoresist and pattern.

13		1. Pattern the Al metal overlay using an Al wet etch solution. 2. Remove photoresist in acetone. 3. Deposit a 1 μm layer of Ag on the backside (soldered side) of the sample to facilitate soldering to DBC substrate when packaging the device.

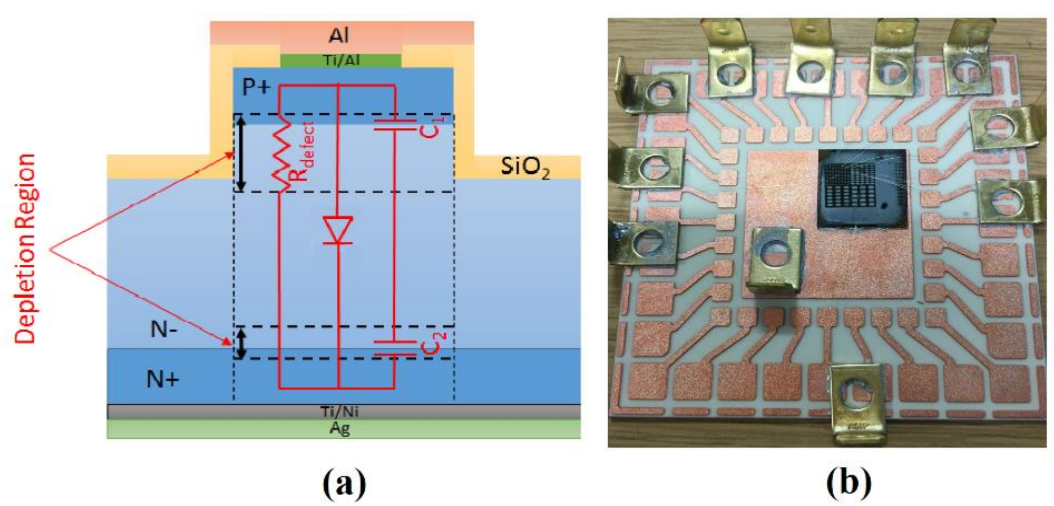


Figure 6-7: (a) Cross-section view of fabricated PiN diode showing the triangular defect on the device (b) Photograph of DCB-mounted 4H-SiC PiN diode die

6.3 Electrical Results and Discussion

In this Section, the forward I(J)-V, characteristics are presented for the fabricated PiN diodes on- and off the defects. The on-state behaviour of these devices has been

evaluated by means of forward and reverse I-V measurements at room temperature as well as characterisation of the devices using clamped inductive switching test.

6.3.1 I-V Characteristics

Since the aim of this Chapter is to study the impact of triangular defect, on 4H-SiC PiN diode performance, it was important to develop a 4H-SiC PiN diode fabrication process that yields satisfactory electrical performance, close to an ideal diode, in order to have a benchmark for fabrication and characterisation of PiN diodes that are fabricated on-defects on all substrates. In this section, first the on-state behaviour of a selected PiN diode fabricated off-defect on PiN1 is assessed using forward I-V measurements at room temperature. More than 40 diodes were tested, all demonstrating similar I-V characteristics to the diode in Figure 6-8. Using these measurements, the ideality factor (η) and differential on-resistance ($R_{on,diff}$) of the fabricated PiN diodes have been found, allowing a comprehensive study of the performance of the fabricated devices.

The forward log(J)-V characteristic of a selected PiN diodes off-defect for PiN1 at room temperature (25°C) is shown in Figure 6-8 which can be used to describe each of the forward bias operating modes of the PiN diode. As illustrated in Figure 6-8, at low forward bias, recombination current (which corresponds to the intrinsic carrier concentration n_i) dominates the J-V characteristic. Equation 6-2 can be used to estimate the total forward current in a P+/N- junction, where the concentration of holes

in the n-type semiconductor in equilibrium is higher than the concentration of electrons in the p-type semiconductor, and when $V_{Ak} \gg kT/q$, [42]:

$$J_F = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D}exp\left(\frac{qV_{AK}}{kT}\right) + \sqrt{\frac{\pi}{2}}\frac{kTn_i}{\tau_p E_o}exp\left(\frac{qV_{AK}}{2kT}\right) \quad 6\text{-}2$$

where E_o is the electric field at the location of maximum recombination and D_p is the hole diffusion constant. The other parameters in Equation 6-2 have been formerly described in Chapter 3. The empirical form given in Equation 6-3 can be used to express the experimental forward J-V characteristics of the fabricated PiN diode:

$$J_F \propto exp\left(\frac{qV_{AK}}{\eta kT}\right) \quad 6\text{-}3$$

In the area where the J-V characteristics is dominated by recombination current, the ideality factor is η=2. When the forward bias rises and reaches the built-in voltage of the PiN diode, diffusion current starts to dominate and above the built-in voltage the ideality factor is η=1. The built-in voltage is given by:

$$V_{bi} = \frac{kT}{q}ln\left(\frac{N_A N_D}{n_i^2}\right) \quad 6\text{-}4$$

When both recombination and diffusion currents are comparable, the ideality factor has a value between 1 and 2. While the forward bias is still high, recombination current in the PiN diode dominates once more owing to the high-level injections of carriers in the drift region and the ideality factor is η=2. Ultimately, the current conduction mechanism in the PiN diode is restricted by its series resistance, which not only involves the semiconductor, but also the ohmic contacts, the wire bonds and the

packaging of the device. Since the forward J-V characteristics of the PiN diode shown in Figure 6-8 is quickly dominated by the series resistance of the device, it is not easy to see the high-level injection mechanism in this Figure.

As seen in Figure 6-8, the voltage drop of the device is approximately 3.1 V at 100 A/cm². The differential on-resistance of the device was found to be 1.74 mΩcm² at 100 A/ cm² given by the equation below:

$$R_{on,diff} = \frac{dV(J_F)}{dJ_F} \tag{6-5}$$

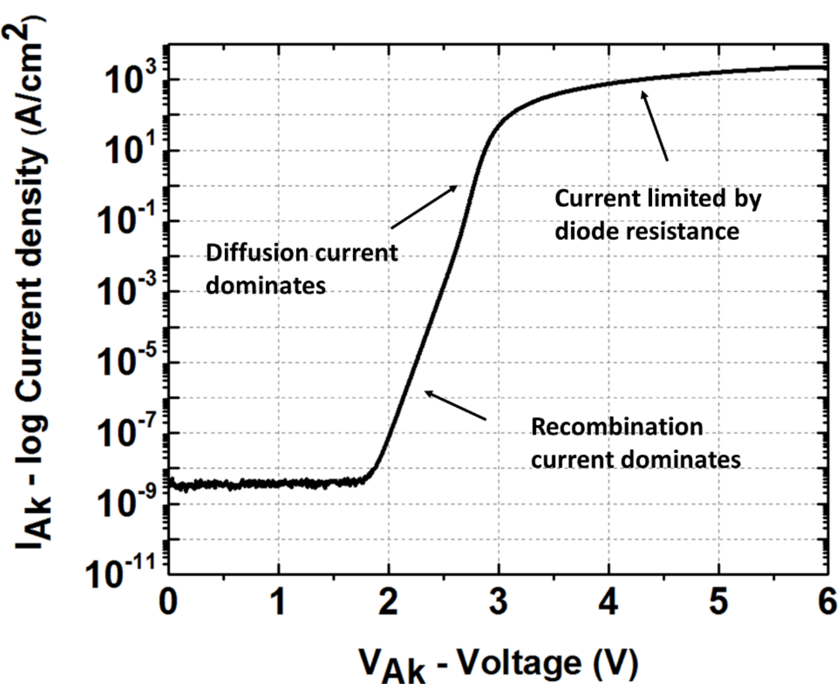


Figure 6-8: Forward log(J)-V characteristic of a selected PiN diode fabricated off-defect for PiN 1 at 25°C, illustrating the dominant current conduction mechanism for each area of the J-V characteristic of the device.

Figure 6-9 illustrates the differential on-resistance of the same device in Figure 6-8 as a function of currently density at 25°. It is evident from this Figure that the differential on-resistance is high at first, since the resistive drift region is unmodulated at low forward bias. As the conductivity modulation phenomenon starts to come into effect, the device resistance reduces.

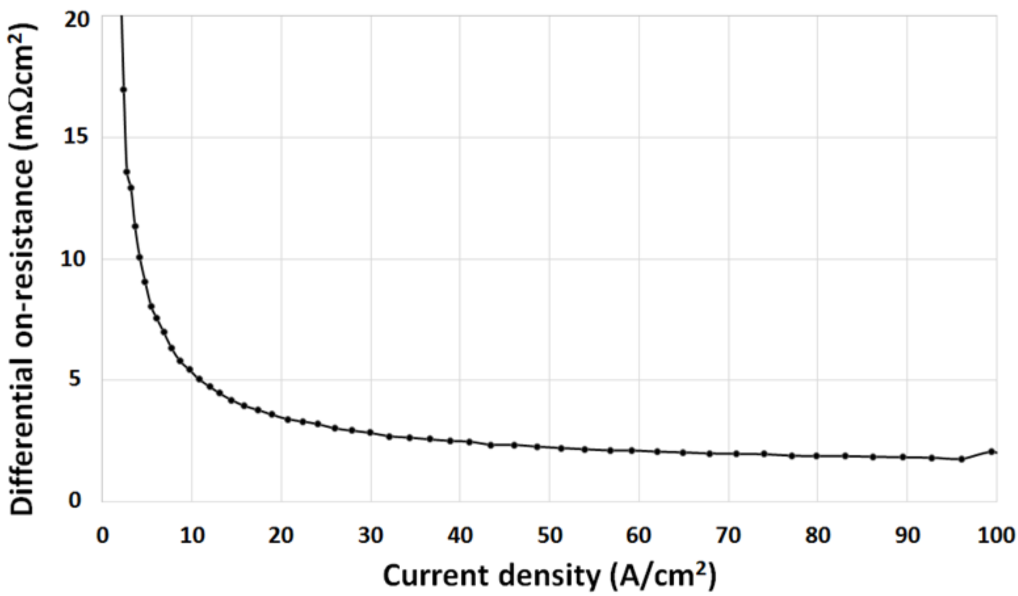


Figure 6-9: Differential on-resistance of the selected PiN diode fabricated off-defect on PiN1 at 25°.

The ideality factor (η) of the device was calculated based on the experimental data and the ideal diode equation below:

$$J_F = J_0(e^{\frac{qV_{AK}}{\eta}} - 1) \qquad 6\text{-}6$$

where

$$\eta = \frac{1}{S\frac{kT}{q}\ln(10)} \qquad 6\text{-}7$$

and

$$S = \frac{d\log(J_F)}{dV_F} \qquad 6\text{-}8$$

The ideality factor of the small area PiN diode fabricated off-defect in PiN1 against forward voltage in the turn-on region is illustrated in Figure 6-10. As anticipated, it can be seen in this Figure that before turn-on (below ~2.4V), the ideality factor value in the recombination region is around 2. After the device turns-on, the ideality factor drops down to around $\eta = 1.3$, just over the ideal value of 1. Therefore, it can be concluded that in the PiN diodes, as well as diffusion, recombination centres are actively involved in the current transport mechanism of the device.

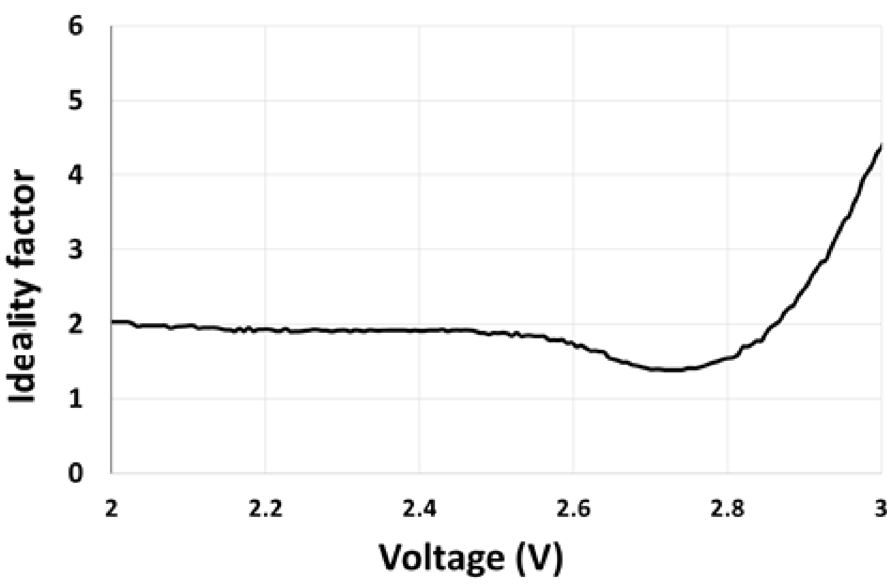


Figure 6-10: Idelaity factor against voltage of the PiN diode fabricated off-defect on PiN1 at room temperature.

The effective carrier lifetime of the PiN diode can also be found using its forward log(J)-V characteristics. This can be achieved by using the saturation recombination current density, $J_{0,rec}$, together with Equation 6-9 for forward recombination current of a pn diode [176].

$$J_{rec} = \frac{qW_D n_i}{2\tau_e} \exp(\frac{aV}{2kT}) \quad 6\text{-}9$$

where W_D is the drift region width, the intrinsic carrier concentration is denoted by n_i and τ_e is the effective carrier lifetime of the device. Equation 6-9 can be simplified by means of extrapolating to V=0 while keeping the ideality factor of the recombination current region $\eta \approx 2$. Equation 6-10 is the simplified version of Equation 6-9:

$$J_{0,rec} = \frac{qW_D n_i}{2\tau_e} \quad 6\text{-}10$$

By rearranging Equation 6-10, the effective carrier lifetime can be found by

$$\tau_e = \left(\frac{qW_D n_i}{2J_{0,rec}}\right) \quad 6\text{-}11$$

As such, by the effective carrier lifetime can be calculated by experimentally defining the value of the saturation recombination current density. The effective carrier lifetime for saturation recombination current density $J_{0,rec} = 3 \times 10^{-24}$ A/cm^2 (typical measured value) and $n_i = 5 \times 10^{-9}$ cm^{-3} at 300K is calculated to be 467 ns, which is a typical carrier lifetime for commercial 4H-SiC epitaxial wafers.

Now that on-state behaviour of 4H-SiC PiN diodes fabricated off-defect is assessed and ideality factor (η) and differential on-resistance ($R_{on,diff}$) have been found to be satisfactory, the same fabrication process was used to fabricate 4H-SiC PiN diodes on- and off the surface morphological defects on all three samples, PiN1, PiN2, and PiN3, to investigate the impact of the triangular defects on electrical performance of the fabricated devices on each substrate.

The forward characteristics of diodes on- and off-defect for PiN1 and PiN2 are shown respectively in Figures 6-11(a) and Figure 6-11(b). It can be seen that a small leakage path at <2V is present on-defect in Figure 6-11(a) resulting in a higher resistance in the device on-defect, 2.83 times higher (shown in Figure 6-13). This is due to the existence of the triangular defect, which appears to be as a high resistance short of the p-type region, causing the leakage, but restricting the effective device area as represented in Figure 6-7(a). Despite the leakage path and increased resistance, the action of the diode is maintained in PiN1 and PiN2, as seen by the significant overlap of the on- and off-defect characteristics from to 2 to 3 V in Figure 6-11. Compared to PiN1, the defects present in PiN2 result in higher leakage, but are likely much smaller, since the resistance of the diode remains similar on- and off-defect. Figure 6-12 shows the log(J)-V characteristics diodes on- and off-defect for PiN3. The defect appears to extend across the majority of the active area of the on-defect PiN3 device, with high reverse and forward leakage currents present and a 12 times increase in resistance.

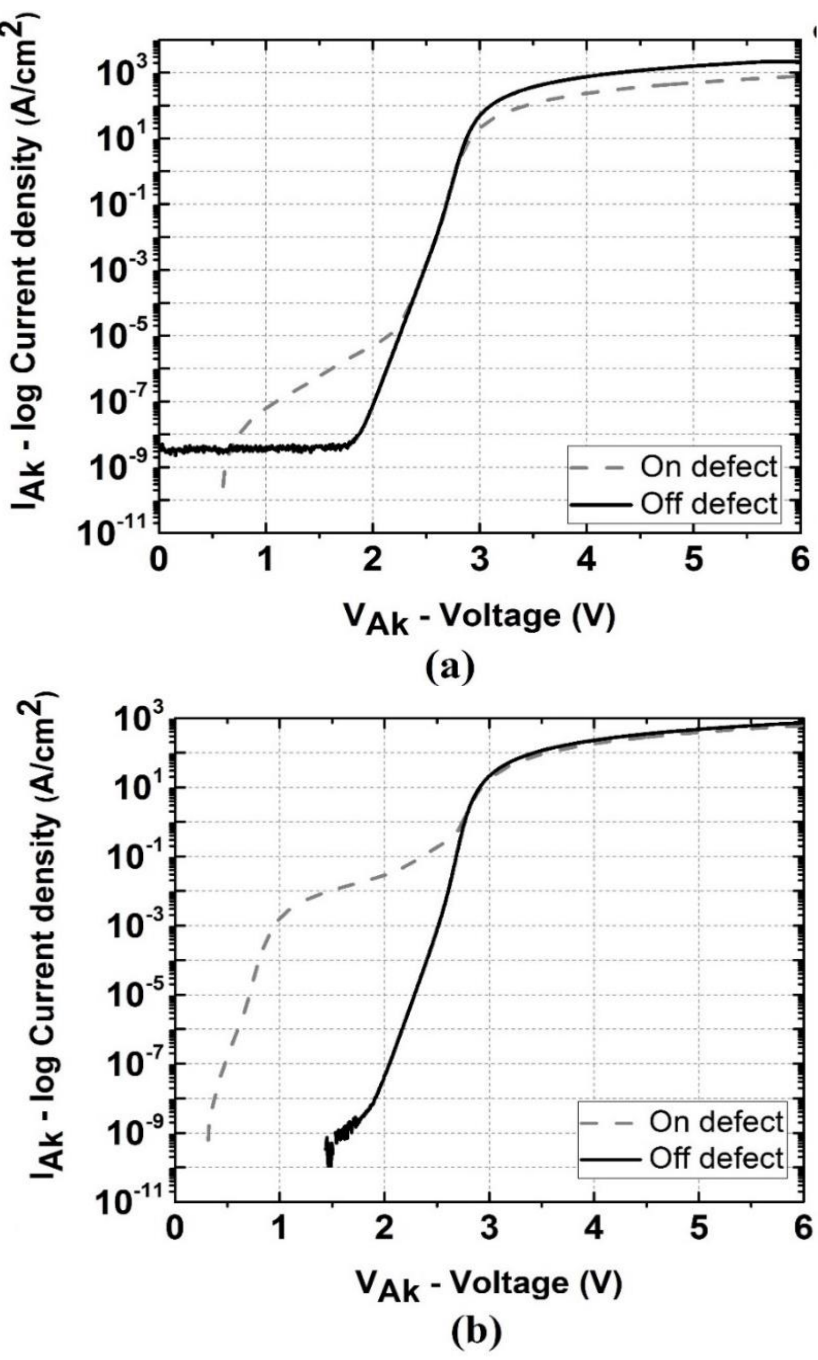


Figure 6-11: Forward log(J)-V characteristics for PiN diodes fabricated on and off-defect on (a) PiN1 (35 µm layer) and (b) PiN2 (30 µm layer) at room temperature.

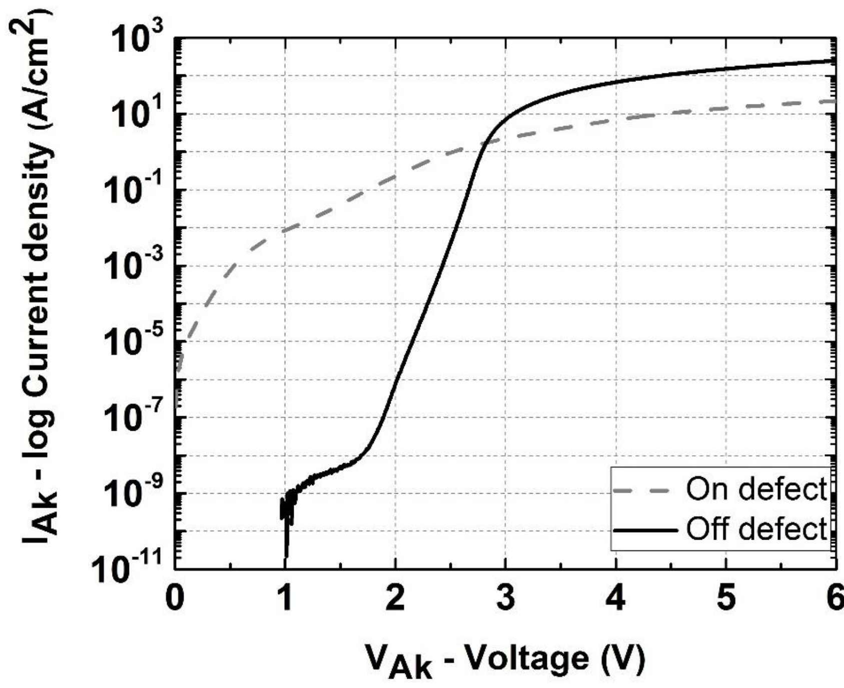


Figure 6-12: Forward log(J)-V characteristics for PiN diodes fabricated on and off-defect on PiN3 (110 μm layer).

Figure 6-13 and Figure 6-14 show the differential on-resistance as a function of current density for the devices fabricated on- and off- defects on PiN1 and PiN2 respectively. The differential on-resistance of the devices fabricated off-defect on PiN1 is around 1.74 mΩcm^2 at 100 A/ cm^2 at room temperature, increasing to approximately 4.8 mΩcm^2 at 100 A/cm^2 when the device is on-defect (Figure 6-13).

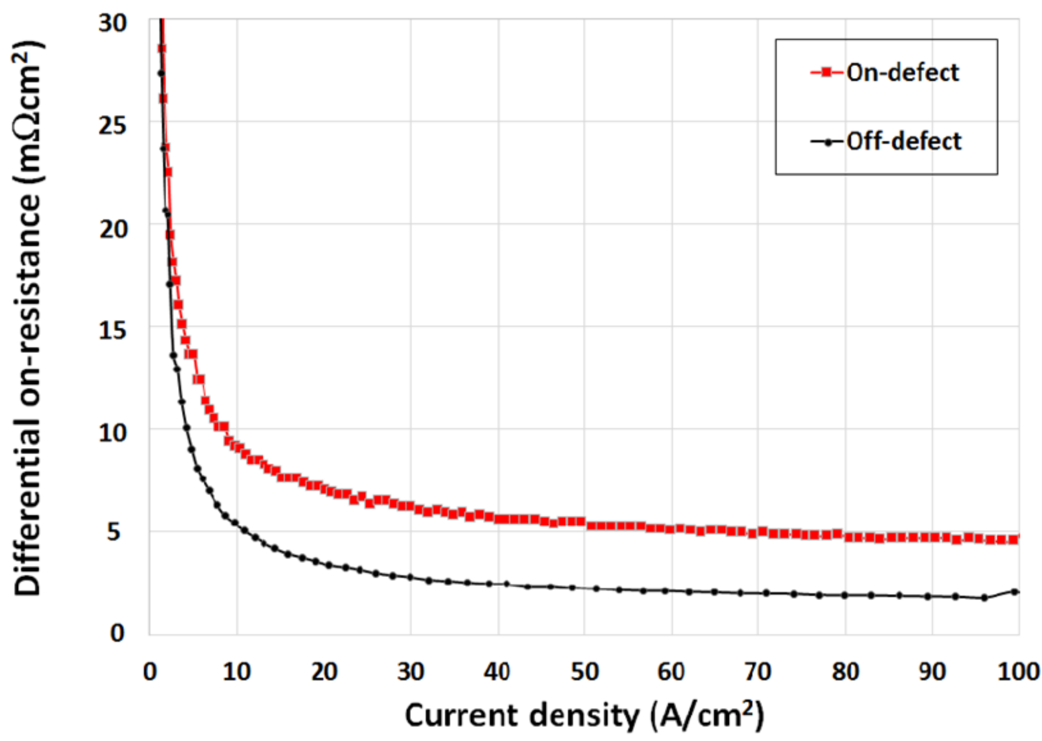


Figure 6-13: Differential on-resistance of PiN diodes fabricated on and off-defect on PiN1 at 25°.

As shown in Figure 6-14, the differential on-resistance of the PiN diodes fabricated off-defect on PiN2 is around 4.8 mΩcm^2 at 100 A/cm^2 which is approximately 3 times higher than the devices with the same active area off-defect on PiN1 (Figure 6-13). The differential on-resistance increases to 5.55 mΩcm^2 at 100 A/cm^2 for the devices fabricated on-defect on PiN2. PiN1 and PiN2 substrates have similar drift region thicknesses, but devices off-defect on PiN1 exhibit a much better forward J-V characteristics and lower differential on-resistance compared to off-defect diodes on PiN2. This suggests that other possibly conductive defects exist in PiN2 which was not seen in both PL and SEM images.

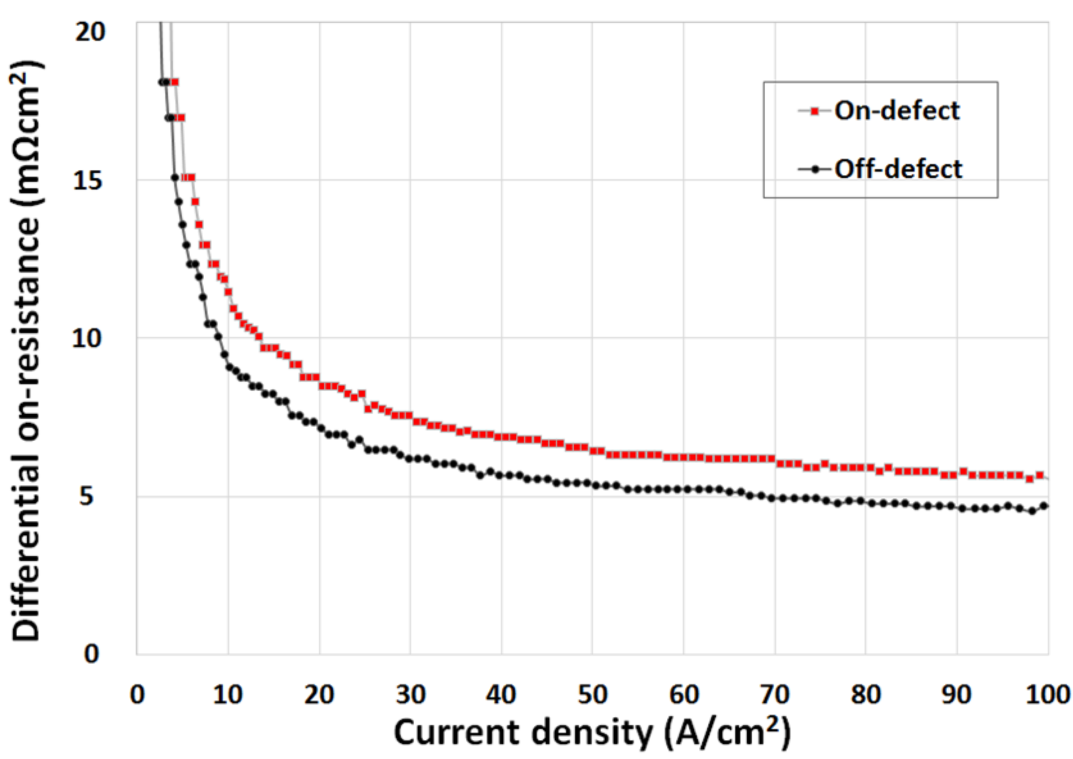


Figure 6-14: Differential on-resistance of PiN diodes fabricated on and off-defect on PiN2 at 25°.

Figure 6-15 shows the differential on-resistance as a function of current density for PiN diodes fabricated on- and off-defect on PiN3. For devices off-defect, the differential on resistance is around 12 mΩcm^2 at 100 A/cm^2. Since the defects are much larger on PiN3 and extend across the majority of the device active area, the resistance is significantly higher (around 77 mΩcm^2 at 77 A/ cm^2). In order to provide a direct comparison, the devices off-defect on PiN3 have a differential on-resistance of approximately 12.4 mΩcm^2 at 77 A/cm^2 room temperature.

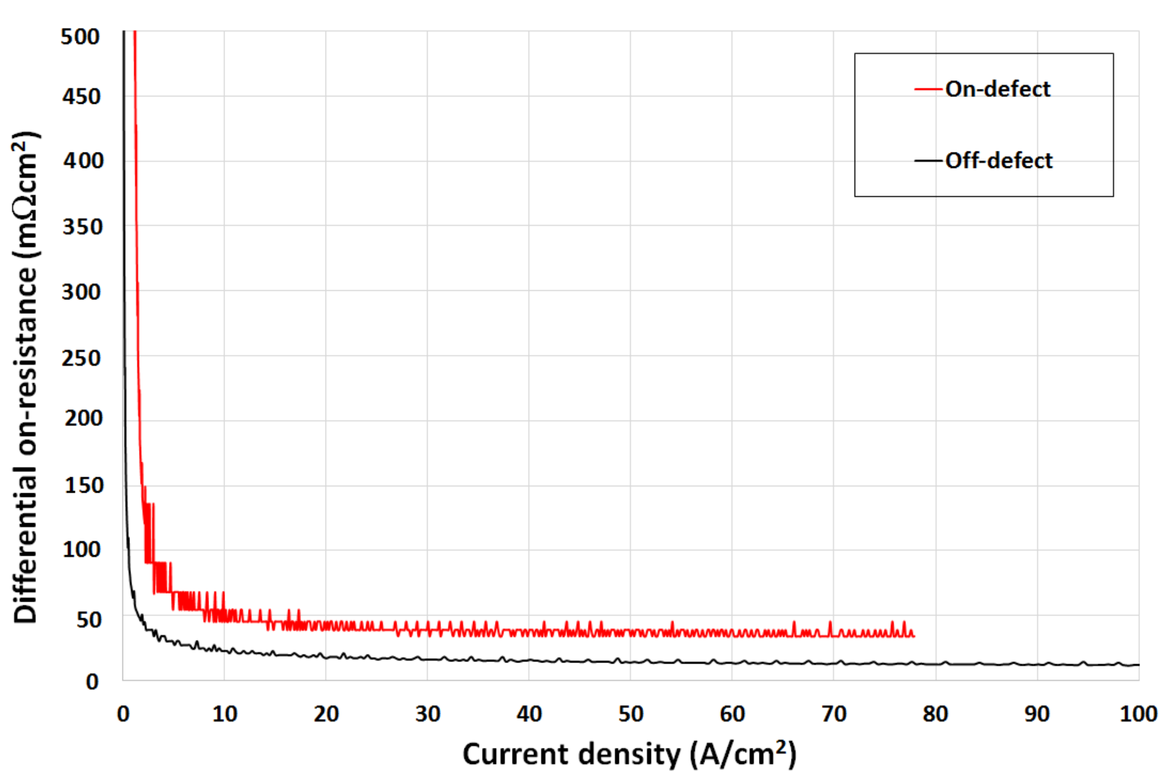


Figure 6-15: Differential on-resistance of PiN diodes fabricated on and off-defect on PiN3 at 25°.

Figure 6-16 shows the ideality factor against voltage for PiN1 and PiN2 devices, both on and off the defect at 25°. It is evident from this Figure that at low forward bias, the ideality factor of the devices on-defect, for both PiN1 and PiN2, are higher than $\eta = 2$. This is because idelaity factor is skewed due to the existence of leakage current paths through the drift region. The source of the leakage path is likely the short caused by the massive triangular defects. It can also be seen from Figure 6-16(b) that for PiN2, as the forward bias reaches the built-in potential of the diode, for devices off-defect, the ideality factor is around $\eta \approx 1.2$, which is slightly over the expected value of $\eta = 1$. However, for devices on-defect on PiN2, the ideality factor reaches very high values $\eta >$

8, suggesting the presence of leakage current paths. It is evident from these results that, for both PiN1 and PiN2, even at higher forward bias, in the high-level injection regime, the ideality factor exceeds the expected value of $\eta = 2$. This is due to the reasonably high series resistance of the PiN diodes, both on and off-defects. But, it can be seen from Figure 6-16(b) that although the defects in devices on-defect on PiN2 result in significantly high ideality factor ($\eta > 8$), the resistance of devices on and off-defect are similar, suggesting that the size of the defects on PiN2 are smaller than PiN1. Figure 6-17 shows the ideality factor against voltage for devices on and off-defect on PiN3 with highest drift region thickness amongst the three samples. It is evident from this Figure that the behaviour of the diodes on and off-defect on PiN3 are considerably worse than PiN1 and PiN2. At low forward bias, the ideality factor is slightly higher than $\eta = 2$ for devices off-defect and approximately $\eta \approx 12$ for devices on-defect. When the forward bias reaches the built-in potential of the device, the ideality factor reaches $\eta = 1.8$ for devices off-defect while the ideality factor is significantly higher for devices on-defect, $\eta > 20$. During the high-level injection regime, due to exceptionally high series resistance of devices on-defect on PiN3, the ideality factor rises above $\eta > 25$, while for devices off-defect, the ideality factor is considerably lower, but still exceeds the expected value $\eta = 2$. This is because the physical size of the surface morphological defect on PiN3 is much larger than PiN1 and PiN2 substrates, occupying the majority of the active area of the device.

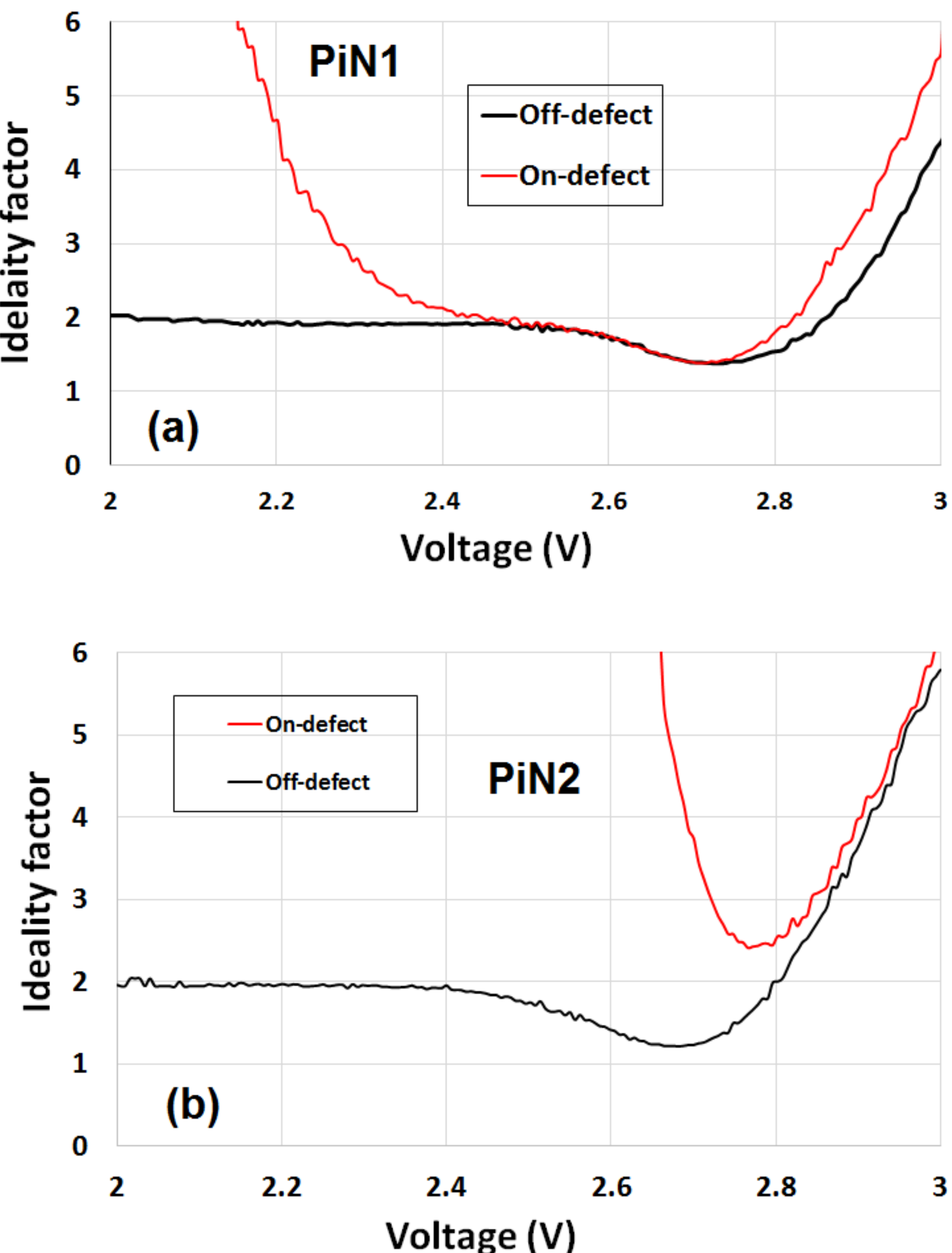


Figure 6-16: Ideality factor against voltage for (a) PiN1 and (b) PiN2 devices, both on and off-defect at 25°.

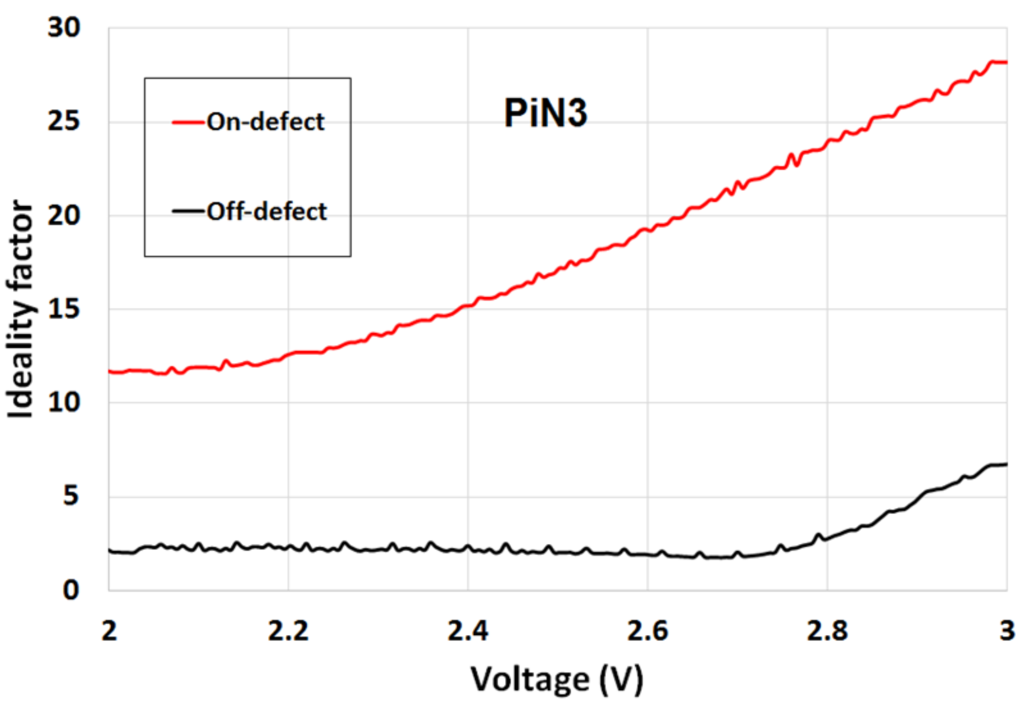


Figure 6-17: Ideality factor against voltage for PiN3 devices both on and off-defect at 25°.

One of the attractive properties of SiC devices is their inherently low leakage current even at low temperature. This is due to its wide bandgap, where the intrinsic carrier density (n_i), is extremely low, around 5×10^{-9} cm^{-3} at room temperature, compared to Si with the corresponding value of 1×10^{10} cm^{-3}. Generally, carrier generation is proportional to n_i^2 for band-to-band generation and n_i in the case of generation by means of a deep level. Hence, it is important to see the impact of these surface triangular defects on the leakage current and reverse I-V characteristics of the fabricated 4H-SiC PiN diodes. Figure 6-18 demonstrates the reverse characteristic of diodes, on- and off-defect on all three samples. During reverse bias, the high resistance leakage path results in a high leakage current. However, there are significant

differences between the diodes due to the material quality of each wafer. Differences between the "off-defect" (really, off triangular defects) diodes suggest the presence of other potentially conductive defects not seen in the PL or microscope images. As such, the leakage current of PiN1 off-defect is below the noise-base of the parameter analyser, whereas PiN2 and PiN3 have higher leakage. The devices on-defect have a leakage current 4-8 orders of magnitude greater than their off-defect counterparts. PiN2 and PiN3 suffered soft breakdown by the time reverse voltage reached 200V.

As shown in Figure 6-18, the most defective wafer is PiN3 with 110 µm epi and the highest defect concentration which showed high reverse (and previously forward) leakage currents, followed by PiN2 with 30 µm epi thickness and lower defect density. PiN1, the only one from supplier A, with 35 µm epi thickness, has the lowest defect density and a much better forward and reverse characteristics.

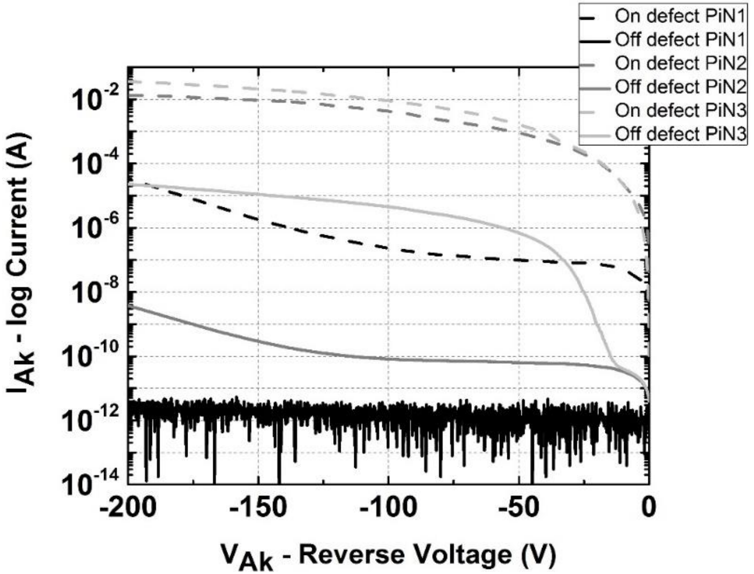


Figure 6-18: Reverse leakage current of PiN diodes fabricated on-and off-defect on all substrates.

6.3.2 Clamped Inductive Switching Test

The impact of 4H-SiC triangular defects on switching performance of the fabricated PiN diodes under inductive load conditions has been evaluated.

6.3.2.1 Experimental Setup & Discussion

The switching characteristic of SiC PiN diodes are evaluated using clamped inductive switching circuit Figure 6-19(b), which reproduces the current commutation between the high side diode and low side transistor. The switching rate of the transistor/diode pair is modulated by the gate resistance used during switching. The experimental setup and the equivalent circuit used in this experiment are shown in Figure 6-19. The test rig is shown in Figure 6-19(a) and it was used to capture the switching characteristic of the fabricated PiN diodes and the SiC MOSFET.

In this test, the SiC MOSFET is a 1200V/10A Cree device with part number C2M0280120. Two pulses are applied to the gate of the low side SiC MOSFET. During the first pulse, the inductor is charged and during the second short pulse the turn-on and turn-off waveform of the diodes are captured. When the MOSFET is off, the current is free-wheeling through the fully charged inductor and the diode. As the transistor is switching on, current commutates from the diode to the transistor at a rate that depends on the RC time constant of the MOSFET. The experiments here have been performed at room temperature with gate resistor of 10 Ω and the DC-link voltage of 40V. The value for the inductor is 2 mH and the DC link capacitor value is 470 µF.

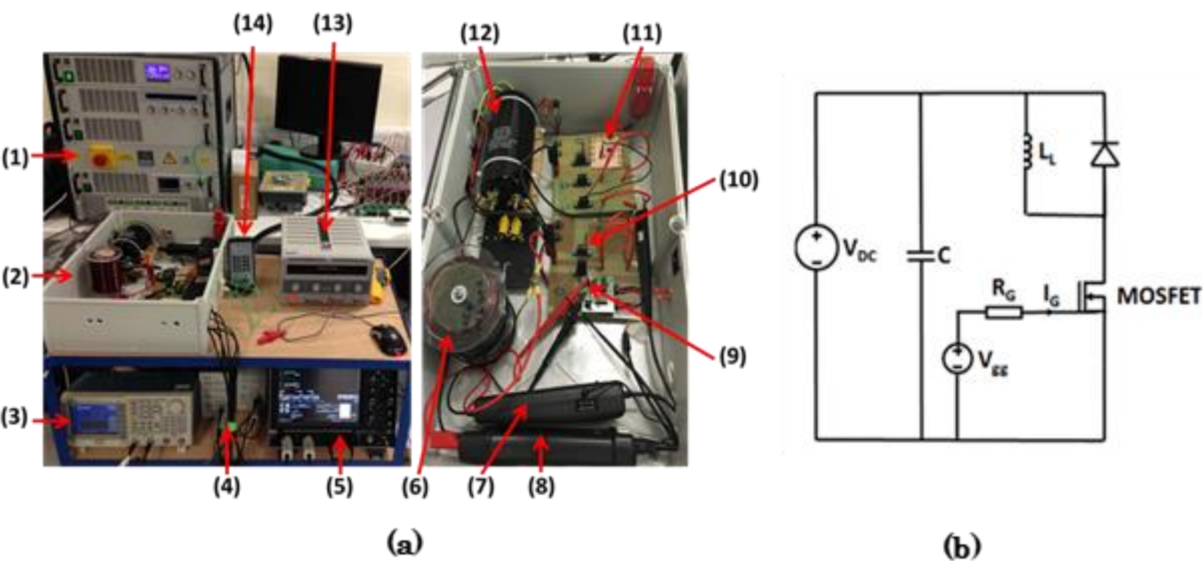


Figure 6-19: Clamped inductive switching test rig (b) Circuit diagram of a clamped inductive switching circuit.

The results shown in Figure 6-20 compare the reverse recovery waveform of the devices formed on and off of the defect with different currents for PiN1 and PiN2. Figure 6-20(a) indicates that when the ratio between the defect area and the active die area is small, the devices on and off defect switch in a similar behaviour; i.e. the leakage current is small and the reverse recovery shape for both on and off defect devices stays the same. No evidence of change in the carrier lifetime and hole recombination rate is observed. This indicates that the switching characteristic waveform of the PiN diode fabricated on an area containing triangular defects on the SiC substrate is not affected and the additional leakage current does not change the switching behaviour of the device. This is due to the fact that the leakage current of SiC is inherently low due to the wide band gap of the material and even further excessive leakage is still not

sufficient to affect the switching behaviour of the device. As the device is switched off and the excessive amount of minority carriers are extracted from the drift region, the depletion regions are formed as the slope of the current changes from the negative slope to positive. Consequently, both devices should block and prevent current from passing through. However, this is not the case for the devices on-defect. Due to the fact that the area of defect is a large portion of the effective die active area, there are significant amount of leakage current through the device.

This can also be confirmed by looking at the reverse I-V characteristics of the devices both on and off-defect shown in Figure 6-18. As can be seen in this graph, the leakage current of the devices on-defect are 4 orders of magnitude higher than the off-defect devices of the same size.

Figure 6-20(b) shows that the device off-defect has higher current ringing and oscillation in comparison to the device on-defect. The ringing is due to the rapid decrease of the junction capacitance due to formation of high reverse electric field across the device. This drop in device capacitance coupled with the stray inductance of the circuit causes oscillations in the device behaviour. Another side-effect of the leakage current induced by the defect on the device is that due to injection of carriers into the device through the defects, the depletion regions cannot form and block the voltage, hence the device capacitance does not drop down as rapidly as it does in the device off-defect. Hence, the ringing damps down quickly and the value of the current becomes equal to the leakage current of the device seen at Figure 6-18.

The work presented in [177] has suggested that compared to defect-free regions, the carrier lifetime is severely reduced by the presence of stacking faults corresponding to triangular surface defects and three-dimensional 3C-SiC inclusions. The switching measurements presented in Figure 6-20 show no decrease in stored charge, suggesting either that there are not many extra stacking faults present around the defect, or that their impact on recombination is minor. In fact, on the contrary, in Figure 6-20(b) there is some evidence (especially in lower current values shown in black) that the amount of stored charge is increased, though the reason for this is unclear, and dependent on the size and depth of the defect.

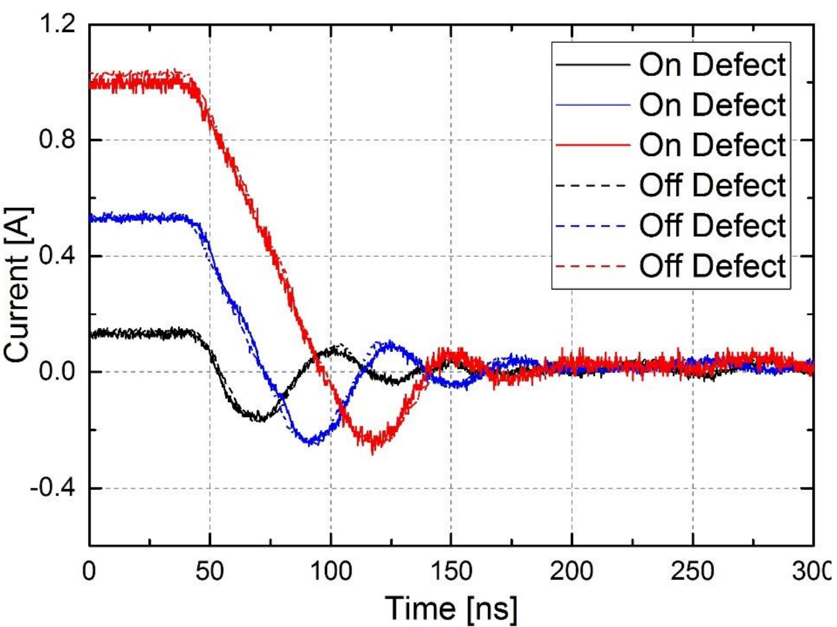


Figure 6-20: Reverse recovery current waveform for devices fabricated on and off-defect on PiN1 at room temperature conditions using 40V supply voltage and a 10 Ω gate

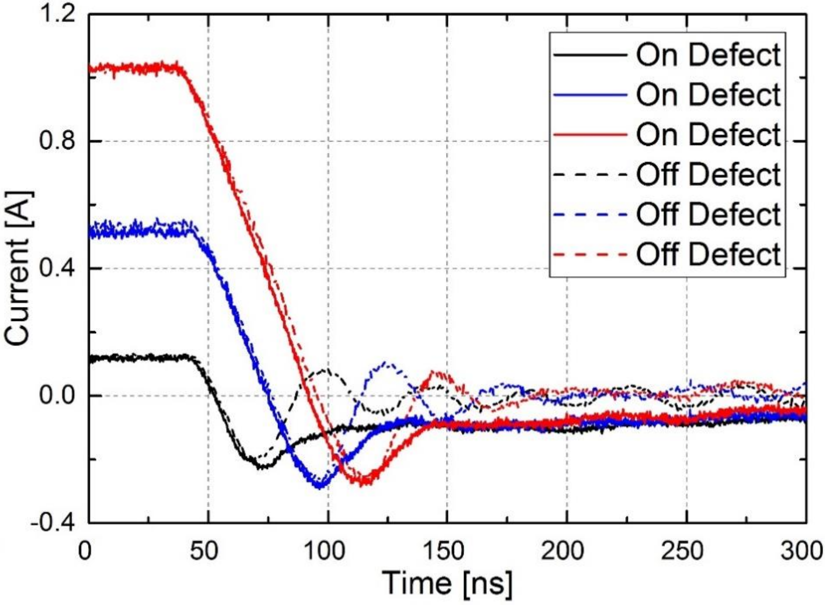


Figure 6-21: Reverse recovery current waveform for devices fabricated on and off-defect on (a) PiN1 and (b) PiN2 at room temperature conditions using 40V supply voltage and a 10 Ω gate resistance.

6.4 Verification of the Electrical Results Using Transmission Electron Microscopy

To verify the electrical results, TEM analysis was performed on the samples. In order to do this, the first step was to prepare the TEM samples. TEM sample preparation steps for these samples were previously discussed in Chapter 5, Section 5.2.2.1.

After the TEM samples were prepared from various areas of the triangular defects, they were analysed using TEM or high resolution TEM (HRTEM). Figure 6-22(a) shows a low resolution cross-sectional TEM image of the triangular defect. The HRTEM results shown in Figure 6-22(b) reveal that the triangular defect is actually a thick layer of 3C-SiC which is placed in between two 4H-SiC layers on top and bottom, where the "ABC" stacking sequence of 3C-SiC can be seen, rather than the ABAC sequence of 4H-SiC. According to Figure 6-22(b), during epitaxial growth of the 4H-SiC substrate, the 3C inclusion is finally overgrown by 4H step flow.

The formation mechanism of triangular defects have been reported in [178-180]. In the early stage of epitaxial growth, foreign particles on the surface of the substrate are either introduced during epitaxy such as downfalls which normally fall from the inner walls of the chamber during growth, or they may even exit on the substrate surface before the start of epitaxy growth. The presence of these downfalls on the substrate doesn't allow the step flow of 4H-SiC in a triangular area behind it resulting

in a triangular shape pit with a large area on-axis terrace. In the case of the triangular defect on PiN1 shown in Figure 6-4, the downfall is located around 15.2 μm from the substrate surface, suggesting that the particle was introduced in the middle of the epitaxy growth process. However, the foreign particles on some triangular defects on the samples in work (not shown in this Chapter) were introduced at the beginning of the epitaxy growth. If the triangular terrace area is large enough, due to supersaturation at the terrace, nucleation of cubic SiC can surpass the 2D nucleation onset and 3C nucleation can occur at various areas on the terrace. The 3C nuclei will then start to grow in all directions and individual islands of growth finally unite with each other and create faceted surfaces. Ultimately, the 3C-SiC layer will be entirely overgrown by constant flows of 4H-SiC growth steps resulting in a smooth surface.

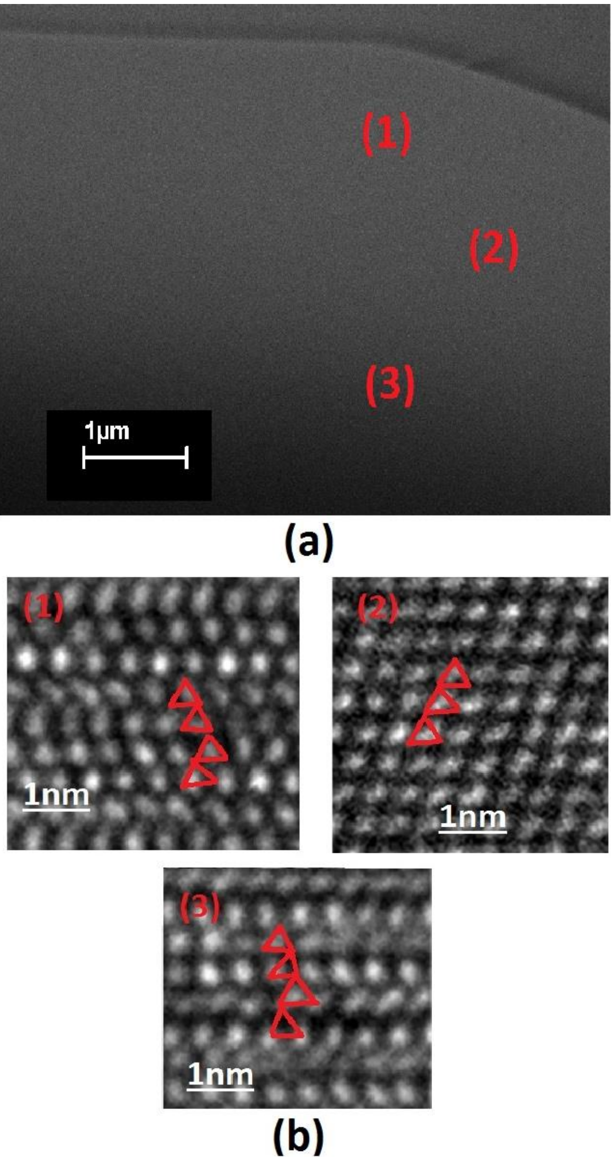


Figure 6-22: (a) cross-sectional TEM image obtained from a 4H-SiC sample of the triangular defect showing (b) top, middle and bottom layer of the sample is shown where a thick 3C-SiC layer is grown in between two layers of 4H-SiC.

A complex structure was observed on the triangular defect area during TEM analysis which is shown in Figure 6-23. This Figure shows an example of a double positioning boundary (DPB) on a triangular defect observed by TEM. DPB is a particular case of twin boundary which is the most frequently encountered grain boundary. A twin boundary occurs when the crystals on one side of a plane is a mirror image of the crystals on the other side of the plane. A grain boundary is the interface between two crystallites in a material. Figure 6-23 (a) shows the area of interest on the triangular defect and Figure 6-23 (b) shows a HRTEM image of the same area. A groove is shown on the surface of the substrate in Figure 6-23 (a). Grain boundary grooving is believed to develop at the surface of the substrate at elevated temperatures when atoms move [181]. The surface of the polycrystalline starts to develop grooves alongside triple junctions where the surface reaches the grain boundaries. The movement of atoms can be in many ways, some may diffuse in the lattice, on the surface or they may evaporate into the vapour phase. When the atoms diffuse on the surface away from the triple junction, they can make a dent beside the junction [182]. The grooving process is shown in Figure 6-24.

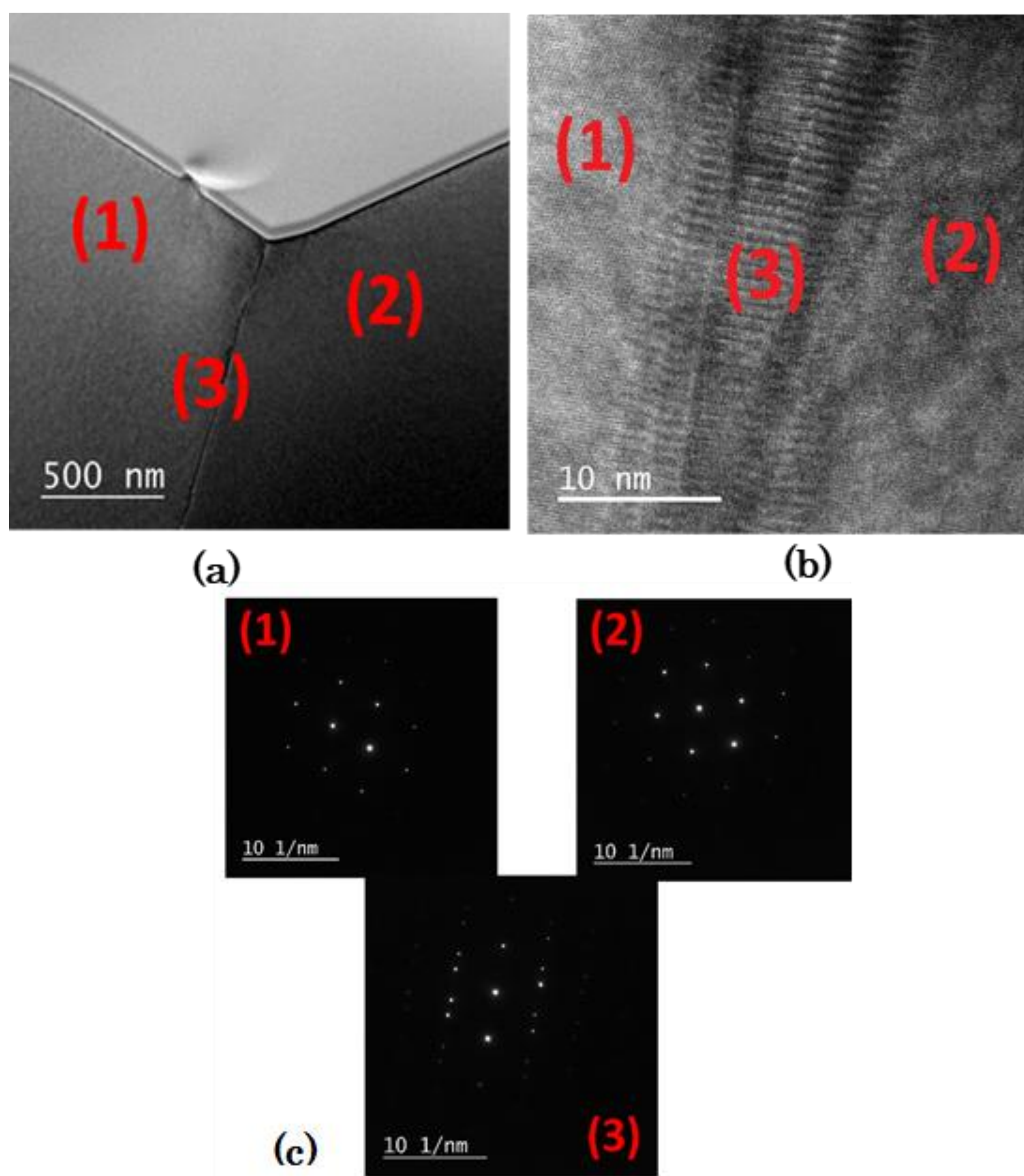


Figure 6-23: (a) TEM image and (b) diffraction patterns of the triangular defect area showing the grain boundary and the leakage path.

When 3C-SiC nucleates on 4H-SiC substrate, two orientations are probable, (1 1 1) and $(\overline{111})$. When two growth regions with opposite orientation (area 1 and area 2) finally combine, DPB will be formed between them (area 3). A DPB is typically a thick area with distorted atomic planes. Figure 6-23 (c) shows the diffraction pattern from the three different marked areas around the defect and BPD. It can be seen that the orientation of the 4H-SiC crystal is different in areas (1) and (2). Area (3) shows the diffraction pattern of the grain boundary.

In conclusion, TEM images shown in Figure 6-23 confirm that the presence of a grain boundary in these triangular defects are due to the nucleation of 3C-SiC at multiple areas in the substrate and the leakage path through the drift region is also observed. The leakage path is clearly shown in Figure 6-25 on PiN3.

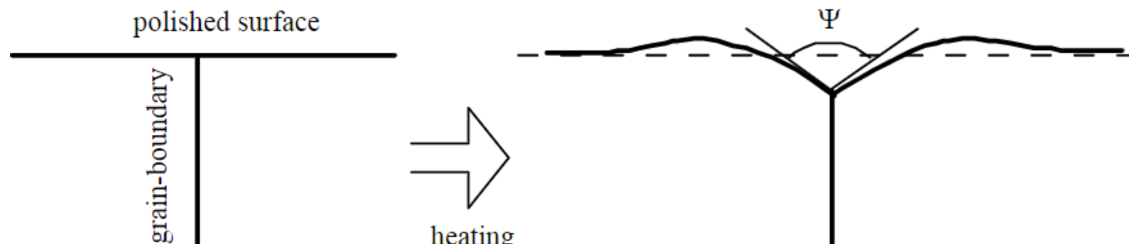


Figure 6-24: Grain boundary grooving process.

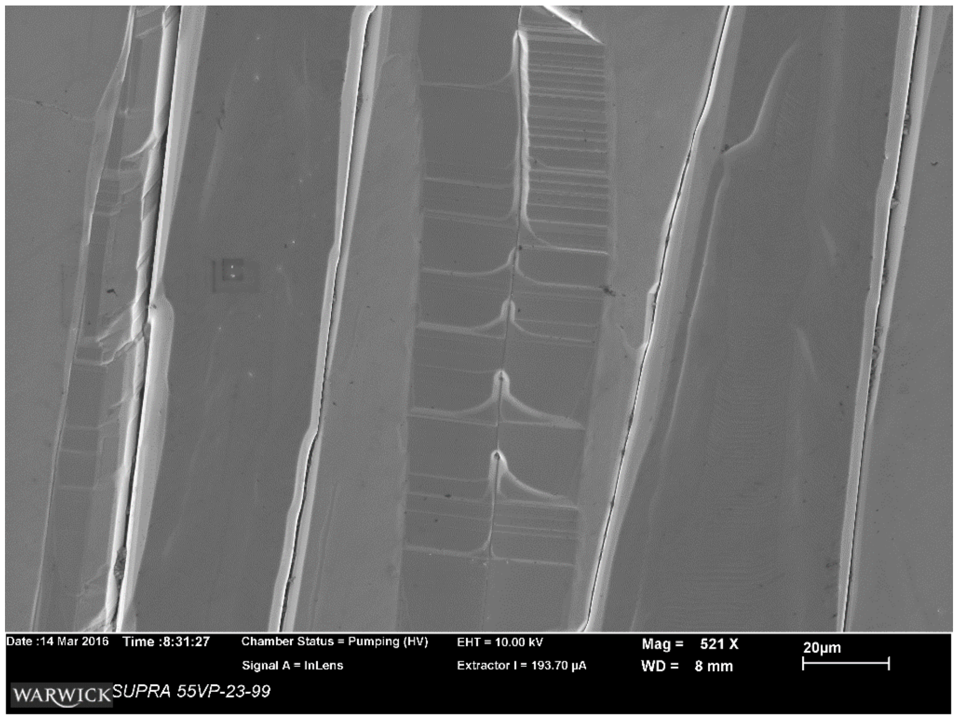


Figure 6-25: TEM image of the triangular defect on PiN3, clearly showing the grain boundaries and multiple leakage paths.

6.5 Summary

The triangular defect is one of the killer defects for 4H-SiC power devices. In this Chapter the impact of triangular defects on fabricated 4H-SiC PiN diodes is investigated. Diodes were formed on wafers with 30 µm, 35 µm and 110 µm 4H-SiC epitaxial layers. We have shown that the existence of these defects limit the active area of the devices and creates a short path through the drift region which increases the leakage current almost 10^8 times higher than the devices off-defect on PiN1 with low defect density. Hence, devices fabricated on epi layer with greater defects, show a very

poor forward and reverse characteristics. Also, the reverse bias shows that all substrates suffer from soft breakdown. However, in contrast, the devices on defect on PiN2 and PiN3 which have higher defect densities, have already suffered soft breakdown by the time reverse voltage reached 200V.

Using the forward I-V measurements, the ideality factor (η) and differential on-resistance ($R_{on,diff}$) of the fabricated PiN diodes were found, allowing a comprehensive study of the performance of the fabricated devices. It was shown that the differential on-resistance of the devices fabricated on-defect on PiN1 is around 4.8 mΩcm^2 at 100 A/ cm^2 at room temperature which is almost 3 times higher than the devices off-defect. It was also shown that the differential on-resistance of the diodes fabricated off-defect on PiN2 is around 4.8 mΩcm^2 at 100 A/cm^2 which is approximately 3 times higher than the same size devices off-defect on PiN1 and it increases to 5.55 mΩcm^2 at 100 A/cm^2 for the devices fabricated on-defect on PiN2. For PiN3, the differential on-resistance of devices fabricated on-defect was around 77 mΩcm^2 at 77 A/ cm^2 at 25°C which was almost 6 times higher than the devices fabricated off-defect at the same current density.

The ideality factor against voltage was plotted for devices on- and off-defect on all three substrates. For both PiN1 and PiN2, even at higher forward bias, in the high-level injection regime, the ideality factor exceeds the expected value of $\eta = 2$. This is due to the existence of triangular defects which act as a short through the drift region. However, the resistance of devices on and off-defect are similar, suggesting that the size of the defects on PiN2 are smaller than PiN1.

It was shown for the first time the impact of triangular defects on switching characteristics of SiC PiN diodes fabricated on and off-defects. In the switching results of the devices presented in this Chapter, the amount of stored charge in the devices on-defect is not decreased. This suggests that either there are not many extra stacking faults around the defect, or that their impact on triangular defects on recombination rate is minor. Switching characteristics of devices on- and off-defects on PiN3 revealed the opposite trend where it was shown that the amount of charge stored in the device on-defect is 60% smaller than the charge stored in the device off-defect. This is because, the triangular defects on PiN3 act as short through the entire width of the drift region, the carriers that enter the drift region, instead of forming the charge storage region and creating conductivity modulation, they leak out from the device. In addition, trap assisted recombination occurs in the semiconductor bandgap due to the existence of defects. Hence, the probability of electrons and holes getting recombined in the drift region increases with the increased thickness of the device resulting in smaller charge getting formed in the charge storage region compared to devices with thinner drift region (PiN1 and PiN2). Consequently, the on-state resistance of the device on-defect on PiN3 increases. This results in a significantly lower forward current passing through the device comparing to the device off-defect.

Moreover, in this study, triangular defects were successfully characterised in all three commercial 4H-SiC substrates using different methods including AFM, SEM, Photoluminescence and HRTEM. Formation mechanism of these defects was then developed based on the characterisation results by SEM, HRTEM and

Photoluminescence. SEM results showed the foreign particle and the depth of the pit that was created due to the downfall. It was shown that, the triangular defects are actually a thick layer of 3C-SiC which is sandwiched between two 4H-SiC layers on top and bottom. It was shown that the triangular defect originates from the downfall of foreign particles on the substrate in the initial stage of epitaxy growth which prevents the 4H-SiC step flow and creates a large triangular on-axis terrace. Next, the 3C-SiC crystals nucleate 2-dimensionally in every direction and are eventually overgrown by 4H step flow. Other complex structures were observed on the triangular defect using HRTEM called DPBs which resulted in a leakage path through the drift region of the devices and increase the leakage current, hence confirming the cause of increased leakage currents seen in all samples fabricated on-defect. The existence of 3C-SiC in the defect was also confirmed by photoluminescence that was performed on the on-axis terrace of the triangular defect, the triangular area just below the downfall.

Chapter 7 Lifetime Enhancement of 4H-SiC PiN Diodes Using High Temperature Oxidation Treatment

In this chapter, the application of a high temperature thermal oxidation and annealing process to 4H-SiC PiN diodes with 35 µm thick drift regions is explored, the aim of which was to increase the carrier lifetime in the 4H-SiC. Diodes were fabricated using 4H-SiC material and underwent a thermal oxidation in dry pure O_2 at 1450°C (Sample1) and at 1550°C (Sample2) followed by an argon anneal at 1550°C. Reverse recovery tests indicated a carrier lifetime increase of around 40% for the 1550°C oxidised/annealed sample and 10% for the 1450°C oxidised/annealed sample compared to the untreated sample, which is due to increase of minority carriers in the drift region. The switching results illustrate that the use of this process is a highly effective and efficient way of enhancing the electrical characteristics of high voltage 4H-SiC bipolar devices.

7.1 Background

In order to achieve the conductivity modulation of a thick drift region (for instance 3.3 kV, 35 μm drift region thickness), a high carrier lifetime is required. This is achieved by the injection of carriers from adjacent device regions into the drift region and is heavily dependent on the carrier lifetime of the thick voltage-blocking layers. Irrespective of the semiconductor material that is used in fabrication of power devices, an adequately long ambipolar (or high-level) lifetime is needed to provide an ambipolar diffusion length that is equivalent to half of the drift region thickness so that

$$\tau_{HL} = \frac{L_a^2}{D_a} \approx \frac{d^2}{D_a} \tag{7-1}$$

where the high-level carrier lifetime is denoted by τ_{HL}, L_a is the ambipolar diffusion length, D_a is the ambipolar diffusion constant and d refers to half the drift region thickness. According to this Equation, carrier lifetime can be plotted against various drift region thicknesses as shown in Figure 7-1. For instance, a carrier lifetime of about 5 μs is needed for a device designed to block 10 kV. The carrier lifetime of as grown 4H-SiC epitaxial layers is normally much lower than expected values due to the existence of lifetime killing defects in the material. For achieving longer carrier lifetimes, a reduction of lifetime killing defects is important. Hence, it is necessary to identify such defects and perform a carrier lifetime enhancement treatment to reduce the concentration of these deep levels and increase the lifetime for these high-voltage 4H-SiC devices.

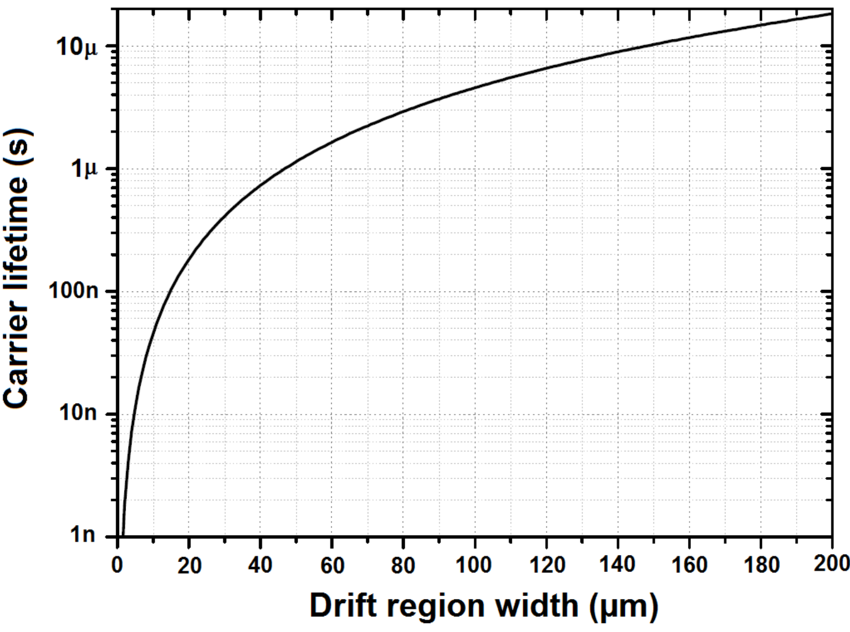


Figure 7-1: Optimal carrier lifetime against various drift region widths in 4H-SiC.

As discussed in Chapter 4, the presence of carbon vacancy (V_C) related $Z_{1/2}$ defect centres in the as grown 4H-SiC bulk material have been found to severely limit the carrier lifetime, the effect of which on the carrier lifetime has been reported in [183-185]. The strong correlation between the existence of $Z_{1/2}$ defect centre concentration and the carrier lifetime has been reported in [95, 97]. The density of the $Z_{1/2}$ defect centres in SiC epitaxial layers is significantly dependent on the growth conditions such as C/Si ratio and growth temperature. Kimoto and co-workers have reported in [66, 186] that, as expected, the $Z_{1/2}$ defect centres are considerably reduced under C-rich growth condition. The authors have observed that the density of $Z_{1/2}$ defect centres were rapidly increased when the epitaxial layers were grown at higher temperatures. It has been reported that both the $Z_{1/2}$ and $EH_{6/7}$ (also carbon vacancy-related) defect centres are

generated by annealing the SiC substrate in an inert (usually Ar) ambient at high temperatures above 1600°C-1700°C [187, 188]. Therefore, it becomes more challenging to attain low $Z_{1/2}$ and $EH_{6/7}$ centre densities when SiC epitaxial layers are grown at high temperatures at a given C/Si ratio. This is because the equilibrium V_C density exponentially grows with increasing temperature.

Several post epitaxial growth processes have been discovered to almost eliminate the V_C defects. A thermal oxidation treatment has been shown to reduce the number of carbon vacancy-related $Z_{1/2}$ defect centres in the bulk material [189]. This is due to the generation of carbon interstitials (C_i) near the oxidising surface, which diffuse into the semiconductor bulk and repair the carbon vacancy defects [189]. This is shown in Figure 7-2. Studies on thermal oxidation reported in the literature are normally performed at temperature range of 1200°C-1400°C due to the unavailability of oxidation furnace working above 1400°C [190].

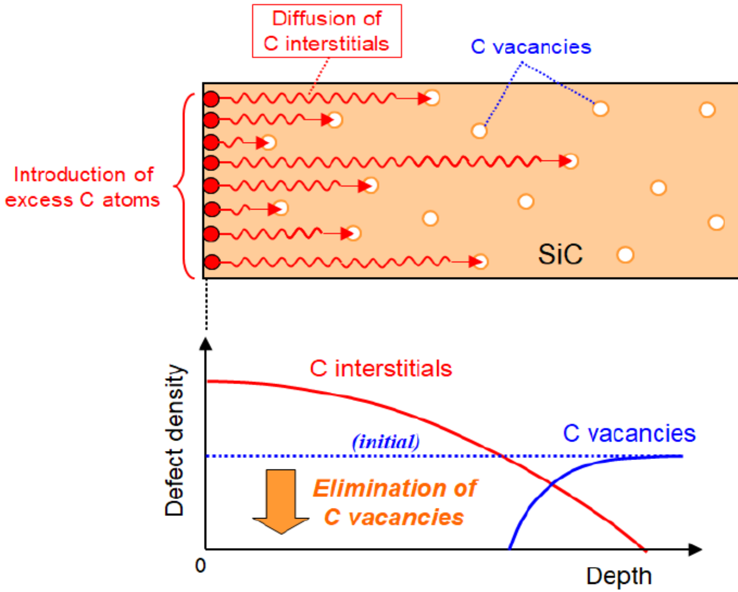


Figure 7-2: Elimination of VC defects in SiC showing the introduction of excess C atoms from the outside followed by diffusion of carbon interstitials using thermal treatment [148].

Higher oxidation temperatures used in carrier lifetime enhancement process increases the rate of oxidation and carbon removal at the SiO_2/4H-SiC interface which also increases the rate at which the $Z_{1/2}$ defect centres in the bulk material are repaired. Therefore, for a given epitaxial layer thickness, higher oxidation temperatures result in shorter oxidation time needed for repairing the $Z_{1/2}$ defect centres. In [190] it was shown that oxidation at 1400°C for around 72 hours results in an almost carbon vacancy free region as thick as 210 μm. It was also shown in [3] that by increasing the oxidation temperature from 1300°C to 1400°C, the oxidation time can be reduced from 50 hours to 16.5 hours to create an almost carbon vacancy free region as thick as 100 μm. While

it is evident that performing the thermal oxidation at higher temperatures is beneficial, thermal oxidation at temperatures above 1400°C are not explored in the literature.

Figure 7-3 shows the depth profile of $Z_{1/2}$ density obtained from a 240 µm n-type 4H-SiC epilayer after thermal oxidation at 1300°C and 1400°C temperatures [1]. Since the drift region thickness of the samples in the study in this Chapter is 35 µm, only the oxidation treatment durations that resulted in 35 µm $Z_{1/2}$ –free region are shown in Figure 7-3. It can be seen that by increasing the thermal oxidation temperature from 1300°C to 1400°C, the "$Z_{1/2}$ -free" region spreading from the surface becomes thicker and the amount of time needed to achieve a 35 µm $Z_{1/2}$ –free region is halved. Due to the capability of the Hi-tech furnace at Warwick University to perform thermal oxidations up to 1550°C, the use of thermal oxidation for carrier lifetime enhancement at temperatures up to 1550°C is explored. According to the results shown in Figure 7-3, it is expected that performing the thermal oxidation process at 1550°C for 1 hour yields a 35 µm $Z_{1/2}$ –free region. Thermal oxidation was also performed at 1450°C for the same duration to compare the amount of carrier lifetime enhancement in both samples to the control sample. There was also a concern that the oxidation rate at 1550°C and the successive consumption of the 4H-SiC would be high enough to consume all of the p-type anode epilayer.

Therefore, in this Chapter, the use of thermal oxidation for carrier lifetime enhancement at temperatures up to 1550°C is explored. In this work, we apply thermal oxidation treatment to 4H-SiC PiN diodes and present their electrical characteristics with and without the thermal oxidation for carrier lifetime enhancement.

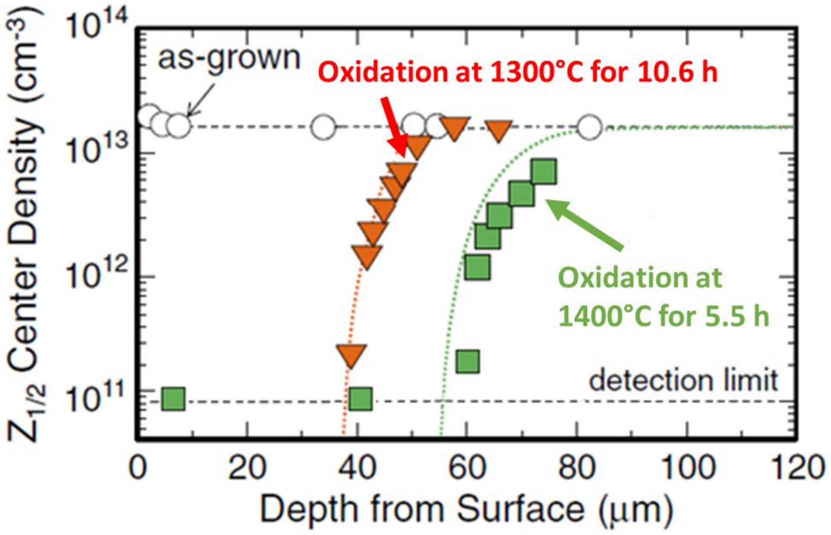


Figure 7-3: Depth profile of $Z_{1/2}$ density obtained from a 240 μm n-type 4H-SiC epilayer after thermal oxidation at 1300°C and 1400°C temperatures.

7.2 Device Fabrication

The PiN diodes used in this work were fabricated in-house using a prime grade 4-inch n-type (0001) Si face, 4° off axis 4H-SiC wafer with a top contact layer of 1μm thick p-type doping up to 1.5×10^{19} cm^{-3}, and a 35 μm thick drift region with 4×10^{15} cm^{-3} n-type. The highly doped P-type layer was used to reduce the anode ohmic contact resistance and to enable thermionic field emission at the metal-semiconductor interface.

The PiN diode fabrication process for the control sample is the same as the fabrication process shown in Table 6-1. The control sample did not undergo any thermal

oxidation process. In order to investigate the impact of thermal oxidation on carrier lifetime enhancement of PiN diodes, two samples were used. The first sample (Sample1) underwent thermal oxidation treatment at 1450°C and the other (Sample2) at 1550°C. For the thermally oxidised samples, two extra processing steps, immediately after the sample cleaning process (Step 1 in Table 6-1), were performed. Thermal oxidation was performed in dry pure O_2 at the desired temperature (1450°C or 1550°C) followed by an argon anneal at 1550°C. As reported in [97, 190], the HK0 defect centre increases due to the thermal oxidation process, which in turn limits the further enhancement of carrier lifetime. However, it has been found that this defect centre is reduced when the sample is annealed in Ar ambient at 1550°C for 30 minutes. This is due to the in-diffusion or/and out-diffusion of C_i during the Ar anneal process. In this work the Ar anneal process was carried out in a separate process to the thermal oxidation. Therefore, to save cost and time, in the fabrication process in this Chapter, a combined thermal oxidation and Ar annealing process has been performed using the Hitech dual purpose furnace at Warwick University.

The samples were first ramped up in temperature to the oxidation temperature. This was performed in an Ar atmosphere at a rate of 8°C/min (5 l/min) where they were held for 15 minutes. The samples were then oxidised in dry pure oxygen (O_2) for 1 hour at the oxidation temperature (1450°C for Sample1 and 1550°C for Sample2) under an O_2 flow rate of 0.5 l/min. After the oxidation process, the Ar flow was restored at 5 l/min, and the samples were held for an extra hour at 1550°C. In the case of Sample1, the dies were ramped up to 1550°C in Ar ambient and were held there for 1 hour. After the Ar

annealing process, the samples were ramped down, again at 8°C/min, to 600°C, again in an Ar ambient. After the oxidation and annealing process, thermally grown SiO_2 was removed in dilute HF solution and the samples were rinsed in DI water. The rest of the fabrication process steps are the same as Table 6-1. After the fabrication process, both devices were packaged on a DBC substrate using the same packaging technique and solder profile discussed in Chapter 4.

7.3 Forward and Reverse I-V Characterisation Results

The forward J-V characteristics of small-area thermally oxidised samples and the control sample at 25°C are shown in Figure 7-4. It can be seen from this Figure that the thermal oxidation process has improved the forward characteristics of the diodes, with the sample thermally oxidised at 1550°C showing the best on-state behaviour compared to the sample oxidised at 1450°C and the control sample (all measured at 25°C). As shown in [191], the oxidation rate increases with temperature, which in turn increases the diffusion rate of the carbon interstitials into the semiconductor bulk and hence repairing more V_C defects. Therefore, oxidation at 1550°C should yield the greatest improvement in the on-state J-V characteristics of the fabricated PiN diodes. As shown in Figure 7-4, the forward voltage drop of the control sample is around 3.12 V at 100 A/cm^2 and 25°C, for Sample1 the voltage drop is around 3.09 V and for Sample2 is approximately 3.06 V (all measured at 100 A/cm^2 and 25°C). For small-area diodes on Sample2, a reduction of 560 mV at 100 A/cm^2 and 25°C was seen, whilst for the

diodes on Sample1 the voltage drop reduction was around 240 mV. These results show that the combined thermal oxidation process and Ar annealing at 1550°C have reduced the voltage drop across the devices.

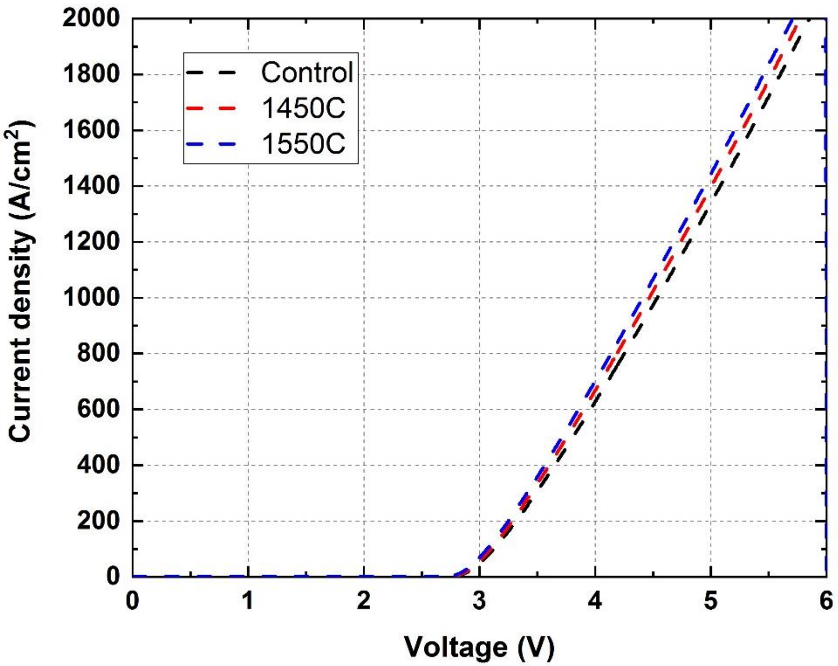


Figure 7-4: Forward J-V characteristics of the small-area thermally oxidised PiN diodes and the control sample measured at 25°C.

Figure 7-5 shows the forward J-V characteristics for large-area and small-area control samples at 25°C. It is evident from this Figure that the voltage drop for a given current density is higher for the device with a larger active area. The voltage drop of the large-area control sample is around 3.41 V at 100 A/cm^2 and 25°C which drops to around 3.12 V for the small-area control sample. These results are in contrast with the findings of the authors' in [174] who have observed a higher voltage drop in devices

with smaller active area. The authors' have reported that this is due to the higher recombination at the mesa perimeter, as the devices with smaller active area with higher perimeter to area ratio have higher forward voltage drop. Hence, it can be concluded that for the devices fabricated in this Chapter, recombination at the mesa perimeter has a negligible impact on the forward characteristics of the fabricated diodes, this therefore proposes that the mesa etch and passivation steps in the device fabrication process are effective in reducing the mesa surface recombination.

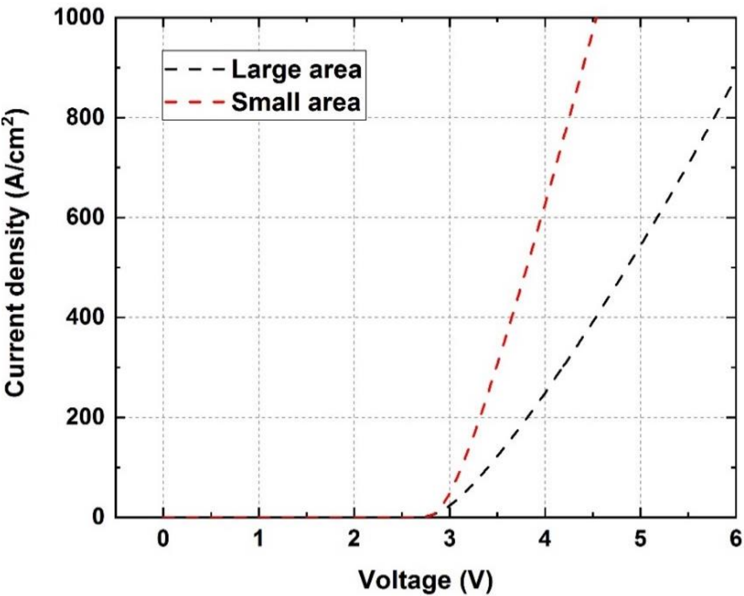


Figure 7-5: Forward J-V characteristics for large-area and small-area control samples at 25°C.

The differential on-resistance of the small-area control sample is around 2.07 mΩ-cm^2 at 100 A/cm^2 and 25°C compared to approximately 4.3 mΩ-cm^2 for the large-area control samples. The differential on-resistance of the small-area PiN diodes on Sample1 is around 2.04 mΩ-cm^2 at 100 A/cm^2 and 25°C compared to approximately 1.9 mΩ-cm^2 for the diodes on Sample2. Again, the decrease in on-state voltage with

temperature for all samples is suggestive of the rise in lifetime with temperature for a conductivity modulated device and a decrease in bandgap of the p-n junction. Though, it was seen that at higher temperatures, a reduction in carrier mobility results in an increase in the differential on-resistance across the drift region. The maximum power limit setting was used for the parameter analyser when testing both the large- and small-area devices. Consequently, for the devices with larger area the current density is smaller than the small-area device. Another possible reason for the increased $R_{on,diff}$ with increasing device active area could be due to the inadequate current spreading at the anode contact as a result of low metal overlayer thickness proportional to the size of the anode contact. Therefore, having a thicker layer, relative to the size of the device active area diameter is required.

The forward log(J)-V characteristics for the small-area PiN diodes on the control sample and Sample2 are shown in Figure 7-6 and Figure 7-7 respectively. As expected, the J-V characteristics of the PiN diode improves with increasing temperature, where both the turn-on voltage and the forward voltage drop decreases. This improvement is because the p-type dopant is not completely ionized at room temperature, and will be more so at increased temperature, therefore supplying more holes (and lower resistance). Moreover, the p-n junction barrier height changes with temperature due to the change in the Fermi level positions, which affects the subthreshold region, as shown. These phenomena come together to overcome the decreased mobility at higher temperatures, which in turn improves the on-state characteristics of the diode. As shown in Figure 7-6 and Figure 7-7, the on-state voltage drop of the small-area control

sample is reduced by approximately 10% to 2.85 V at 300°C, whilst for the diodes on Sample2, the on-state voltage drop is reduced by approximately 6% to 2.80 V at 300°C.

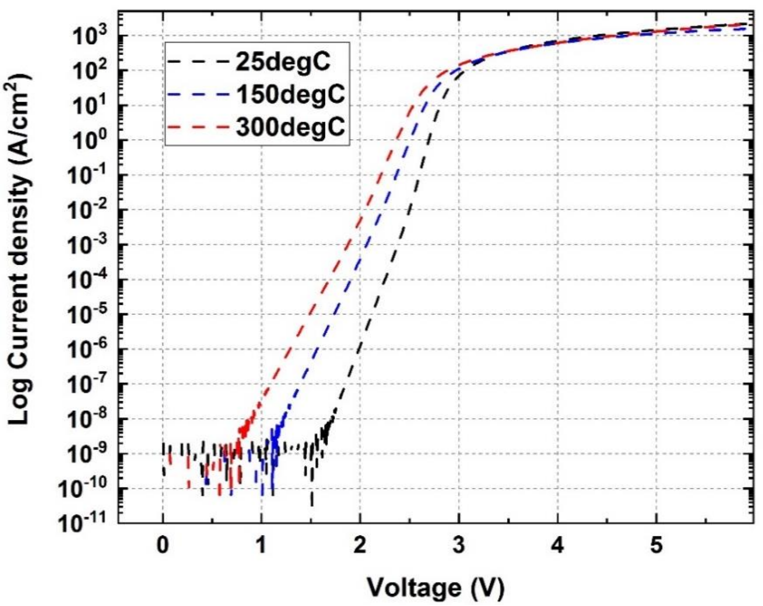


Figure 7-6: Forward Log(J)-V characteristics of small-area diodes on sample2 at 25°C, 150°C and 300°C.

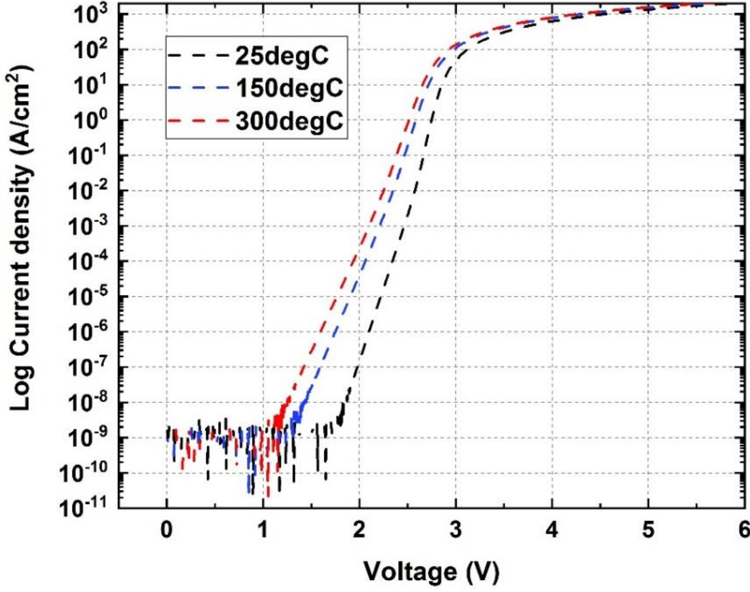


Figure 7-7: Forward Log(J)-V characteristics of small-area diodes on control sample at 25°C, 150°C and 300°C.

Figure 7-8 shows the ideality factor against voltage characteristics for small-area diodes on the control sample and Sample2 at 25°C. It can be seen that the low-level injection regime has an ideality factor of around 2, demonstrating that recombination current dominates in these samples. After the point of diode turn-on, where the diffusion current dominates the ideality factor is approximately η=1.4, which is slightly over the ideal value of 1. This is because resistance takes hold, obscuring the η =1 region.

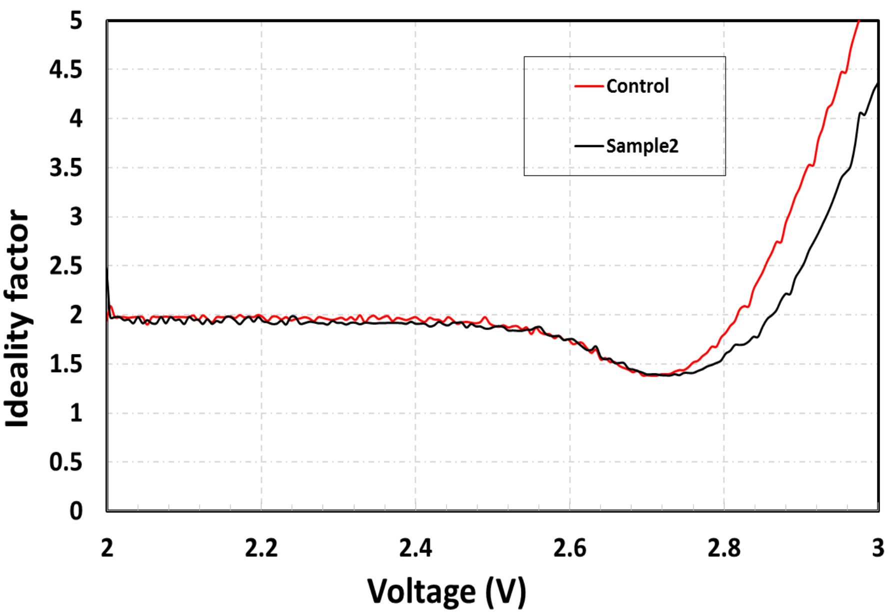


Figure 7-8: Ideality factor against voltage characteristics for small-area diodes on the control sample and Sample2 at 25°C.

I-V-T measurement was performed on both thermally oxidised samples and the control sample at temperature range of 25°C to 300°C. Figure 7-9 shows the forward I-V-T characteristics of Sample2. It can be seen that the on-state behaviour of the diodes

on Sample2 that underwent a combined thermal oxidation and Ar annealing at 1550°C improves with temperature.

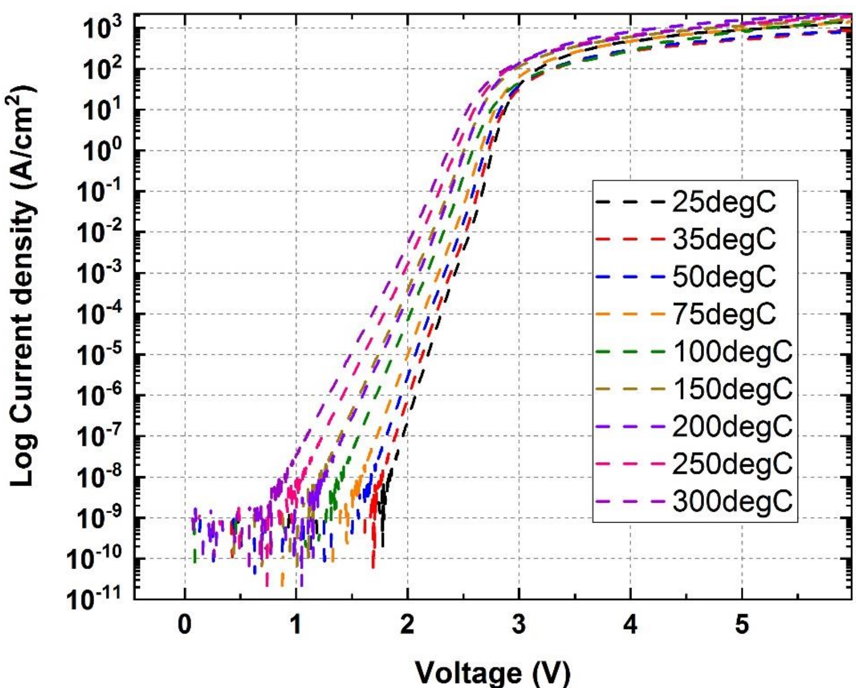


Figure 7-9: Forward I-V-T characteristics of thermally oxidised sample at the temperature range of 25°C to 300°C.

Figure 7-10 shows the reverse I-V characteristics for both control and thermally oxidised (Sample2) PiN diodes. It can be seen that the reverse leakage current of Sample2 is approximately 2 times higher than the control sample. To ensure that the leakage current at the mesa perimeter sidewall is negligible, a thick TEOS SiO_2 layer was used as a passivation layer in the fabrication process of the PiN diodes. The thickness of this layer was considerably higher than the mesa etch depth. Figure 7-11 shows the forward I-V characteristics of PiN diodes when a thin TEOS SiO_2 passivation layer was used. The non-ideal I-V behaviour of the diodes in the recombination current

region is due to the presence of a parasitic Schottky diode at the vertical surface of the mesa etched sidewall, resulting in high (>2) ideality factor in the low current regime, indicating that the TEOS SiO_2 layer has not completely passivated the surface. Hence, in the fabrication of the PiN diodes in this thesis, a thick TEOS SiO_2 passivation layer was used (>2 μm).

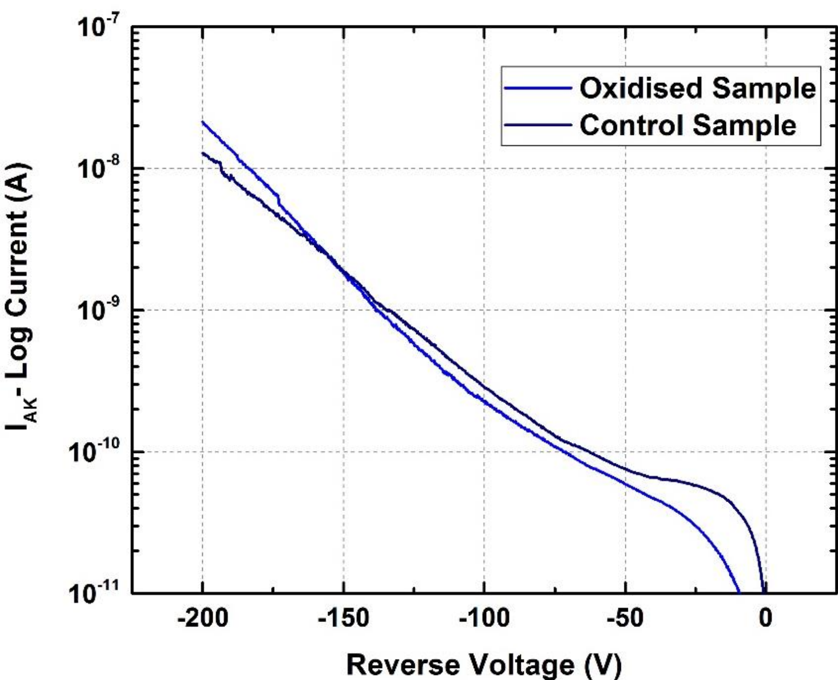


Figure 7-10: Reverse I-V characteristics for both control and thermally oxidised PiN diodes at 25°C.

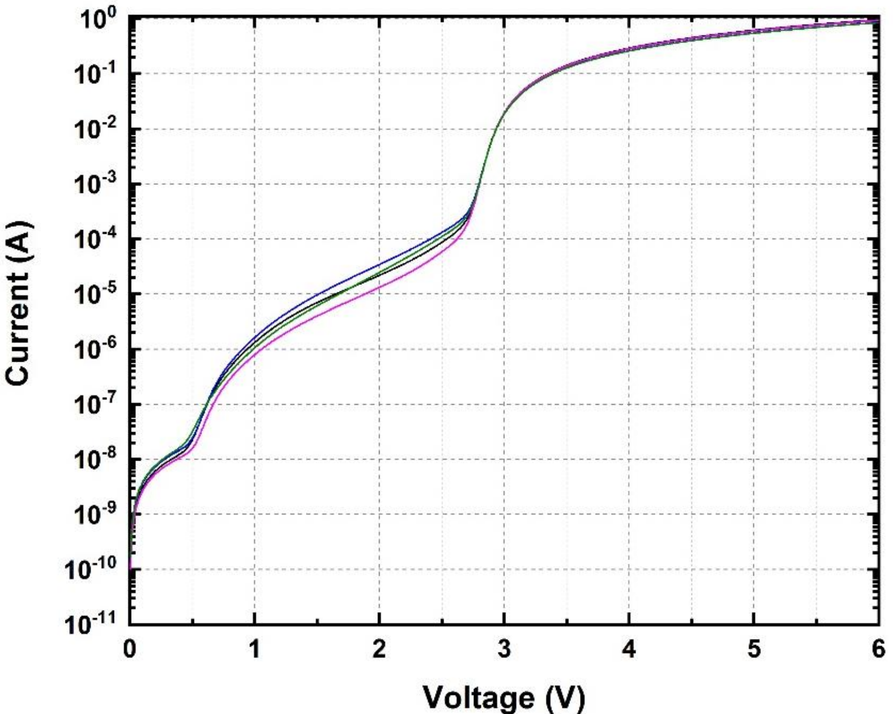


Figure 7-11: Forward I-V characteristics of PiN diodes at 25°C showing the non-ideal I-V characteristic in the recombination region due to the existence of parasitic Schottky diode in parallel with the pn junction.

7.4 Reverse Recovery Behaviour of PiN Diodes

Due to conductivity modulation, PiN diodes; exhibit low on-state losses compared to unipolar-type devices of comparable blocking voltage. However, this has the disadvantage of slow transient behaviour. PiN diodes have inherently slow turn-on and turn-off characteristics due to their physical operation. After the reverse blocking state, once a PiN diode is switched to the on-state, the injected carriers take a finite

amount of time to pass through the drift region. This means that for some time this high resistance region is not conductivity modulated. Therefore, instantly after a forward bias pulse is applied to the PiN diode, it can show a large forward voltage drop. As the charge in the drift region builds up, this forward voltage drop will slowly decrease, ultimately getting to its steady state value. The forward recovery power dissipation is normally much lower than the power dissipation rising from reverse recovery.

The stored charge in the drift region of the PiN diode must be removed as soon as the device is switched from the on-state to the reverse blocking state and before the device can handle a reverse voltage in the off-state. The injected carriers are extracted from the drift region, forming depletion layers at the $P+/N-$ and $N-/N+$ junctions, ultimately combining when the entire charge has been extracted. A reverse current flows throughout this finite time before all of the charge is extracted from the drift region. This is caused by a negative applied voltage which appears across external inductance as a result of the diode not being able to yet handle a reverse voltage. The reverse voltage only starts to accumulate after the depletion layers form, which is after the reverse current has started flowing. Hence, there is a time duration in which both the current and voltage are large and negative, therefore causing a large power dissipation at the reverse recovery time. This can enforce restrictions on the maximum switching frequency of the device, and also demand derating the device operating current. Moreover, a long diode recovery time, t_{rr}, can reduce the total circuit switching speeds.

Approximate reverse recovery waveforms of a PiN diode are shown in Figure 7-12 when it is switched-off with an inductive load. As can be seen in this Figure, a piecewise linear waveform is used to model the reverse recovery current [44]. The most common switching method for rectifiers in power electronics circuits, such as PiN diodes, is inductive switching. In clamped inductive switching test the existence of an inductive load results in a constant turn-off current slew rate, or di/dt. This is because the full reverse voltage is being applied across the inductor before the PiN diode is capable of blocking the applied voltage. As seen in Figure 7-12, the current slew rate, denoted as a, is controlled by the parameters of the circuit as specified by the equation below:

$$a = \frac{di}{dt} \approx \frac{V_{RP}}{L} \tag{7-2}$$

where V_{RP} is the peak inductive voltage overshoot due to parasitic inductance of the diode (L), and V_F is the forward voltage drop.

The stored charge in the drift region of the device governs the resulting reverse recovery behaviour. The time intervals illustrated in Figure 7-13 correspond with the times shown on Figure 7-12. Figure 7-13 illustrates the charge profile in the drift region of the PiN diode at designated time intervals throughout inductive load switching as well as the one-dimensional distribution of electric field.

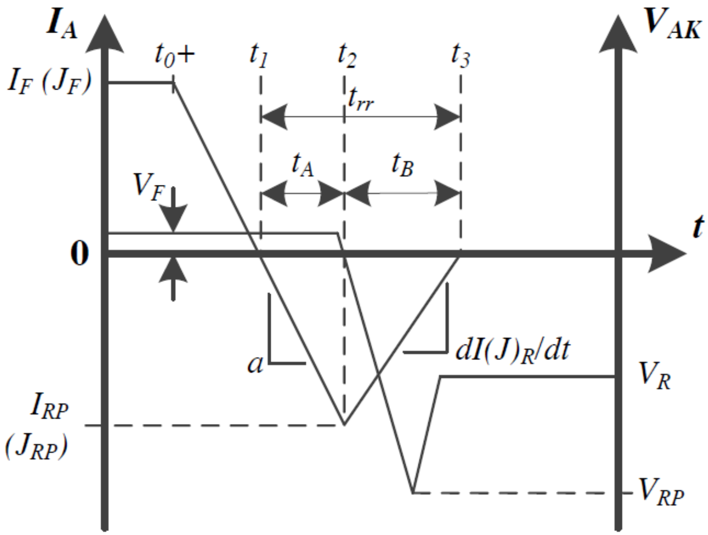


Figure 7-12: Reverse recovery approximation waveforms with inductive load switching

Before turn-off, $t = 0$, the charge profile exhibits a catenary shape. At $t = t_0 +$, the reverse recovery process starts as a reverse bias voltage is applied to the device and the stored charge in the drift region starts to be extracted. Next, at $t = t_1$, the current that flows through the device changes its polarity, and the diode starts to conduct reverse current. When the slope of the charge profile extends to zero at the borders of the drift region, the zero-crossing of the current happens. This can be seen in Figure 7-13. After $t = t_1$, the reverse current keeps on increasing as controlled by the constant a up until the diode is capable of supporting some of the reverse voltage at $t = t_2$. As illustrated in Figure 7-13, the peak reverse current I_{RP} (or J_{RP}) appears once the carrier concentration at the $P+/N-$ junction gets to zero, and hence resulting in the formation of a depletion layer. The reverse peak current density is found to be comparable to the gradient of the charge profile at the $P+/N-$ junction of a PiN diode; therefore, an

accumulation of charge at this junction can result in higher reverse peak current densities and as a result give rise to the switching losses of the device. In order to improve the reverse recovery characteristics of PiN diodes, procedures such as modifying the emitter injection efficiency and localised lifetime control can be used to decrease the charge accumulation close to the $P+/N-$ junction.

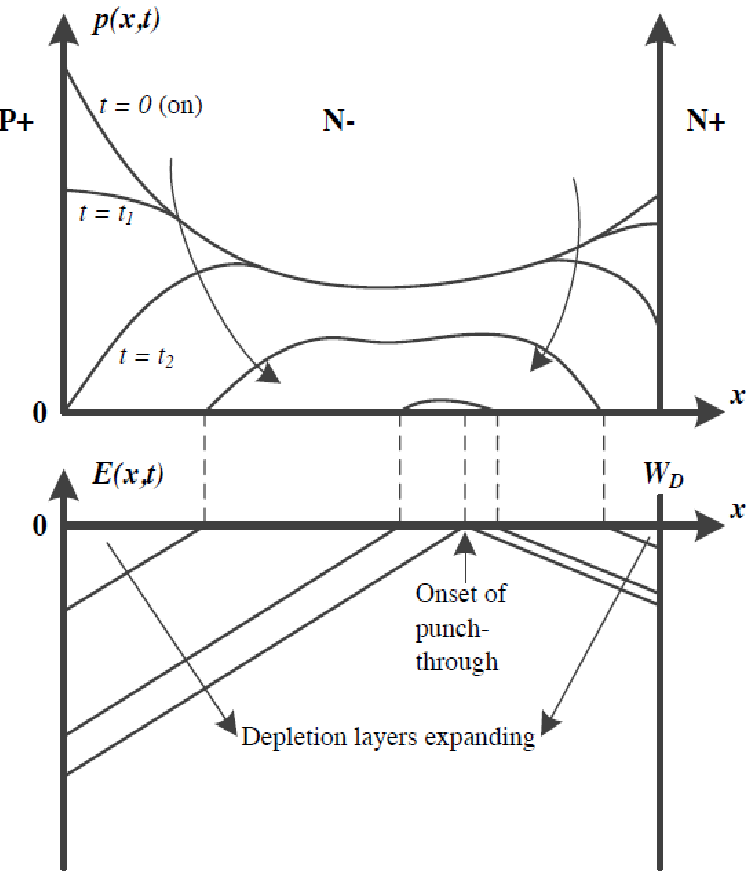


Figure 7-13: Charge profile in the drift region during inductive load switching and the one-dimensional distribution of electric field.

As illustrated in Figure 7-12, the first stage of the PiN diode reverse recovery process, denoted as t_A, is the time duration in which charge is extracted from the drift region before the diode is capable of blocking any of the reverse voltage. The second stage of the diode reverse recovery occurs after time $t = t_2$, and is referred to as t_B. During this period the outstanding charge is extracted from the drift region up to the time where it is completely vacant of any electron-hole plasma. This results in a decrease of the reverse current through the device while the reverse voltage across the diode increases up until the time when the recovery process is complete and the device is in the reverse blocking mode. This can be deduced from Figure 7-13, as the slope of the charge profile slowly reduces as the charge in the drift region is extracted.

The equation below describes the overall power dissipation of the PiN diode during reverse recovery according to Figure 7-12:

$$P_{D,rr} = f_{sw} \int_{t_0+}^{t_1} |V(t)||I(t)| dt + f_{sw} \int_{t_1}^{t_2} |V(t)||I(t)| dt + f_{sw} \int_{t_2}^{t_3} |V(t)||I(t)| dt = P_0 + P_A + P_B \quad 7\text{-}3$$

It is found that the majority of the power dissipation in the process of the reverse recovery happens throughout its second phase (t_B), when the diode is conducting reverse current while it supports an increasing reverse voltage as well. It is thus apparent that although a moderately large t_B (with regard to t_A) is desirable for realising soft reverse recovery characteristics and reducing spikes in transient voltage, it can cause a higher overall power dissipation for the device.

The extracted charge during the turn-off transient, referred to as Q_{rr}, is an important parameter in the reverse recovery when determining the turn-off switching characteristics of the PiN diode. Q_{rr} can be calculated by integrating the reverse recovery current waveform as shown below:

$$Q_{rr} = \int_{t_1}^{t_3} I(t)dt \tag{7-4}$$

According to Figure 7-12, at time $t = t_1$, the integrated charge profile in the drift region can be used to express Q_{rr}, hence

$$Q_{rr} = qA \int_{-d}^{+d} n(x)dx \tag{7-5}$$

With regard to the detailed analysis mentioned above, it is obvious that in order to enhance the switching behaviour of the PiN diode, the stored charge in its drift region must be reduced. Minimising Q_{rr} results in the reduction of the reverse recovery power dissipation $P_{D,rr}$, the peak reverse current I_{RP} and the reverse recovery time t_{rr}. Moreover, softer reverse recovery characteristics can be attained by modification of the charge profile in the drift region, as well as achieving a more enhanced on-state against switching loss trade-off, and reduced reverse peak current densities. Due to the improvement of high voltage PiN diodes, several techniques to tailor both the total charge and the charge profile in the device have been effectively utilised to enhance the on-state against switching loss trade-off, such as gold (Au) or platinum (Pt) diffusion in Si devices, or via electron irradiation in 4H-SiC as discussed in [192]. Electron irradiation is employed to instigate deep level recombination centres in the energy bandgap. Furthermore, methods to locally reduce the carrier lifetime can also be used to decrease charge build-up close to the $P+/N-$ and $N-/N+$ junctions [193, 194].

7.5 Clamped Inductive Switching Characterisation Results

The clamped inductive switching test were carried out on the control sample and sample2 to investigate the reverse recovery waveform. The test rig setup which was designed to capture the reverse recovery of the PiN diode and switching characteristics of the switching device and the PiN diode was previously shown in Chapter6, Figure 6-19(a). In this test configuration, the switching device was a 1200V/10A Cree SiC MOSFET with part number C2M0280120 and the current was limited due to the thickness of the wire-bonds used in the packaging process and the small active die area (4.53×10^{-4} cm^2). Moreover, due to the delicate wire-bond on the surface of the die, no silicone gel was applied to the surface; consequently, the voltage waveform was limited to 150 V prevent arcing as well as an excessive voltage overshoot. Moreover, these 3.3 kV devices have been fabricated with no edge termination. Although, this operating voltage is relatively low when compared to the blocking voltage of the fabricated PiN diode, it still shows a quantitative comparison of the switching characteristic of the control sample and the oxidised/annealed devices. During the clamped inductive switching test, a double pulse is applied to the gate of the bottom side switching MOSFET shown in the circuit schematic in Figure 6-19 (b). During the first pulse, the inductive load is charged and the current increases with a constant ramp rate which depends on the DC-link voltage and the inductance of the coil as well as the pulse width. In this experiment, the pulse width is adjusted in such a way that the inductor can

provide 2 A to the devices with a DC bus voltage of 150 V. In the next pulse, the turn-on and turn-off switching waveforms of the diode and MOSFET can be captured on the oscilloscope.

Figure 7-14 shows the reverse recovery current waveform of the SiC PiN diode before (control sample) and after thermal oxidation at 1450°C and 1550°C at 100 V DC link voltage. The negative part of the current waveform (reverse recovery of a bipolar device) indicates a change of direction in the flow of the current through the device. During the reverse recovery, the minority carriers in the drift region are extracted from both ends of the device and hence, a negative current can be seen. This introduces an additional switching loss in comparison with a unipolar device. The amount of reverse recovery is dependent on the carrier lifetime, temperature, minority carrier mobility, background doping of the drift region as well as the amount of current that passes through the device. The carrier lifetime of the PiN diode under high level injection condition can be calculated from the reverse recovery characteristics from Equation 7-6 [44]. This equation was discussed previously, but which for ease of use it is repeated in this chapter. This equation is simplistic and is used as an indicative way to show the percentage of increase in the carrier lifetime, repeated here for ease.

$$\tau_{HL} = 2\frac{I_{RP}}{I_F}t_{rr} \qquad \text{7-6}$$

In this equation, I_{RP} is the peak of the reverse recovery current, I_F indicates the forward current in which the device went under and t_{rr} is the duration of time in which the flow of the current was in the negative direction.

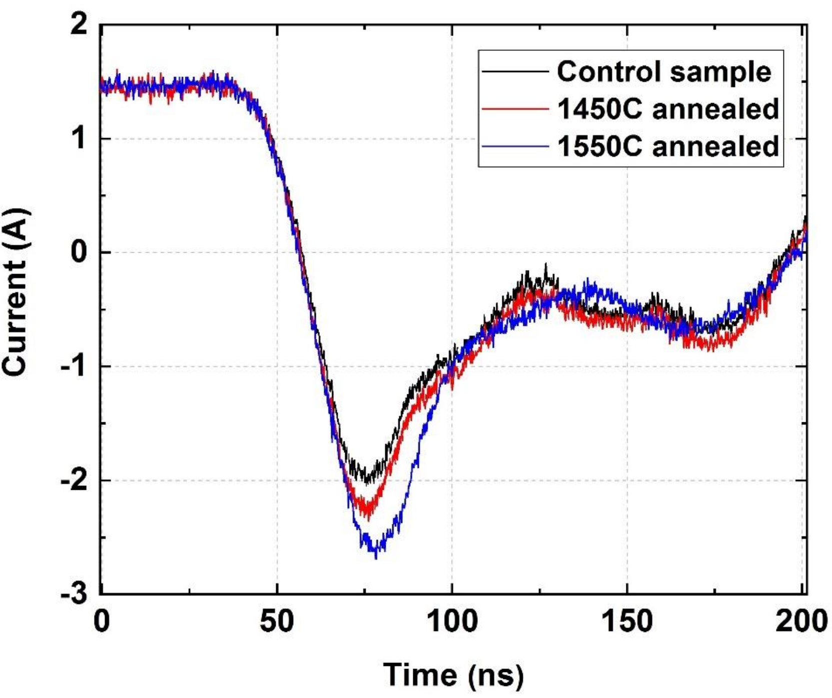


Figure 7-14: : Reverse recovery characteristics for control sample, 1450°C and 1550°C thermally oxidised PiN diodes at 25°C.

The results indicate an increase of 39% of the reverse recovery current for the 1550°C annealed sample compared to the control sample which is due to the increase of excessive minority carriers in the drift region. The 1450°C sample also exhibits a 14% increase of the reverse recovery current compared to the untreated sample. It can be seen that the 1550°C thermally oxidised and annealed sample (Sample2) has a higher reverse recovery peak (I_{RP}) than the control sample (2.71 A compared to 1.95 A) and the reverse recovery peak of the 1450°C thermally oxidised and annealed sample (Sample1) is around 2.22 A. From the reverse recovery characteristics, Q_{rr} for the Sample2 PiN diode is around 127 nC compared to 115 nC for the Sample1 diodes and 100 nC for the

control sample devices. Based on Equation 7-6, $\tau_{HL}$for the control sample is calculated to be around 400 ns, this compares to a value of around 440 ns for Sample1 and approximately 542 ns for Sample2. These results show an approximately 40% increase in the carrier lifetime for the 1550°C thermally oxidises/annealed sample compared with the control sample. This indicates that more oxidation time was required to further enhance the carrier lifetime of the 1450°C annealed sample. It can also be concluded that increasing the oxidation temperature and therefore the need for shorter treatment time is a cost effective and time saving process which is beneficial for commercial device fabrications. It must to be noted that the developed thermal oxidation and annealing process at 1550°C has resulted in obtaining the carrier lifetime necessary for the optimal performance of the PiN diode that are fabricated on the wafer with 35 µm drift region (Figure 7-1).

Figure 7-15 shows the reverse recovery waveform of the 1450°C oxidised/annealed PiN diode at different junction temperatures but with a fixed turn-off current commutation rate and fixed forward current. The DC link voltage was set to 150 V and the complementary SiC MOSFET was driven with a gate resistance R_G of 10 Ω. By allowing adequate time to reach steady-state, it can be presumed that the junction temperature is equal to the case temperatures. It can be seen that the peak reverse recovery current of the fabricated SiC PiN diode increases with temperature due to the positive temperature coefficient of the minority carrier lifetime which leads to higher reverse recovery charge during turn-off. This is a disadvantage of PiN diode rectifiers as it means that they demonstrate higher losses when the junction temperature

increases. The results shown in Figure 7-15 agree with the Forward J-V characteristics of the same sample in Figure 7-5.

When the temperature is increased, the peak reverse recovery increases, which leads to faster carrier extraction via higher recombination rates. If the positive slope of the recombination current is too high, the recovery of the diode is snappy (high *dI/dt*). This is because a high *dI/dt* from the recombination current coupled with parasitic inductance (from the MOSFET wire-bonds) can cause substantial over-voltages which can destroy the diode and even the complimentary transistor in the circuit.

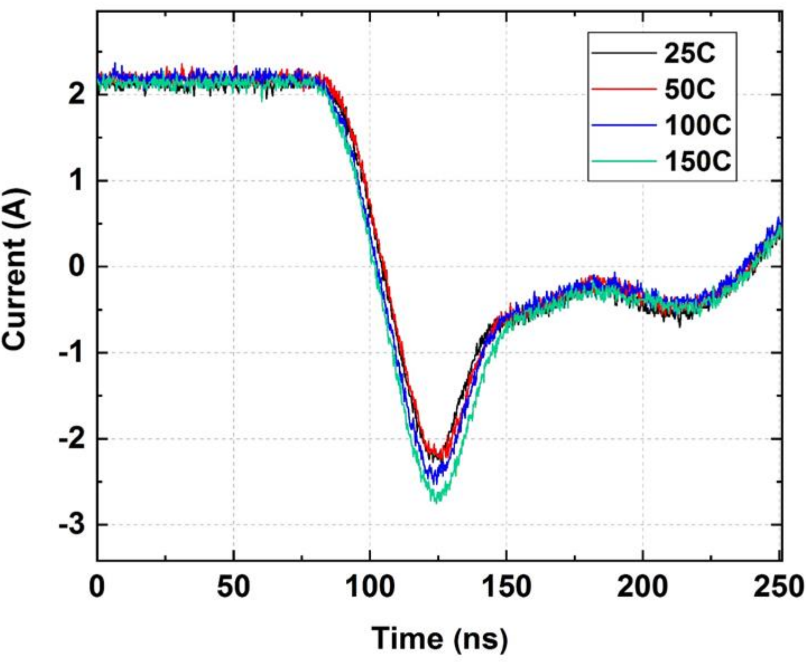


Figure 7-15: Reverse recovery characteristics of the1450°C oxidised / annealed SiC PiN diode at different junction temperatures. DC link voltage=150 V.

Figure 7-16 shows the reverse recovery characteristics of the 1550°C annealed sample with different supply voltages. It can be seen that the reverse recovery characteristics become snappier as the supply voltage increases. This is due to the fact that increasing the supply voltage increases the extension of the depletion width into the PiN diode, therefore causing faster charge extraction and recombination. Also shown in Figure 7-17 is the reverse recovery characteristics of the 1550°C annealed sample with different forward currents. In these test, the supply voltage (V_{DC}) was 150 V and the SiC MOSFET was driven with a gate resistance R_G of 10 Ω. It can be seen from this Figure that, as expected, the reverse charge increases with the forward current as the stored charge during the on-state of the device increases with the forward current.

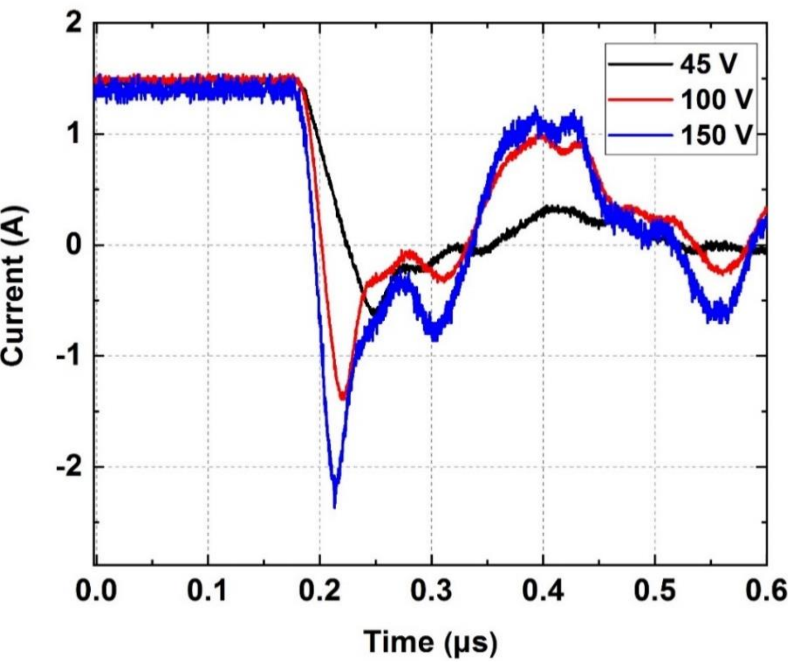


Figure 7-16: Reverse recovery waveform as a function of supply voltage for the 1550°C annealed sample at 25°C, RG= 10 Ω.

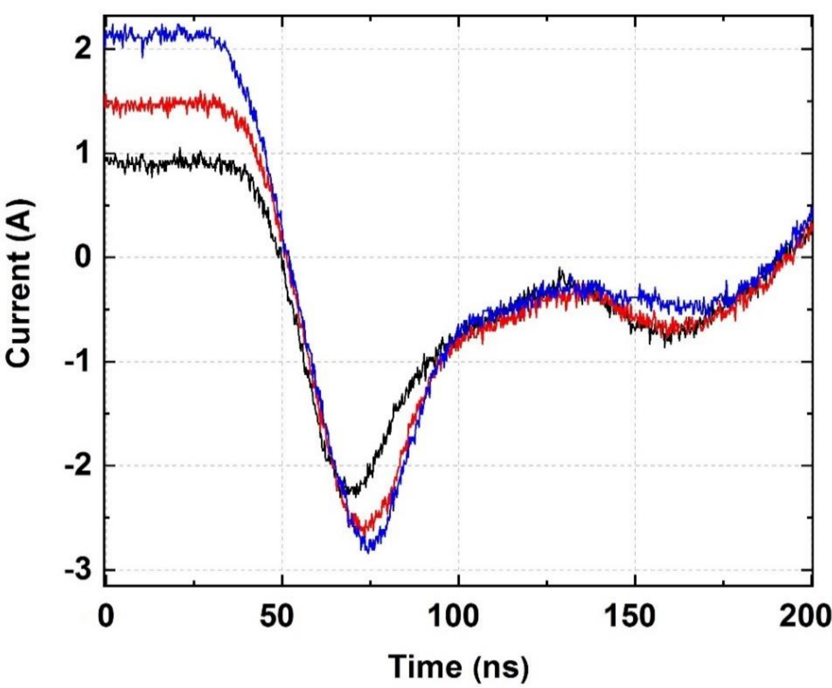


Figure 7-17: Reverse recovery waveform with different forward currents for the 1550°C annealed sample at 25°C, VDC= 150 V, RG= 10 Ω.

The gate resistance of the MOSFET sets the current commutation rate. The effect of gate resistance (or the switching rate) on the switching characteristics of the 1550°C annealed sample is shown in Figure 7-18. As expected, increasing the switching rate increases the snappiness of the reverse recovery characteristics of the PiN diode. The peak reverse recovery current increases with increasing the switching rate and the recovery current has a higher *dI/dt*.

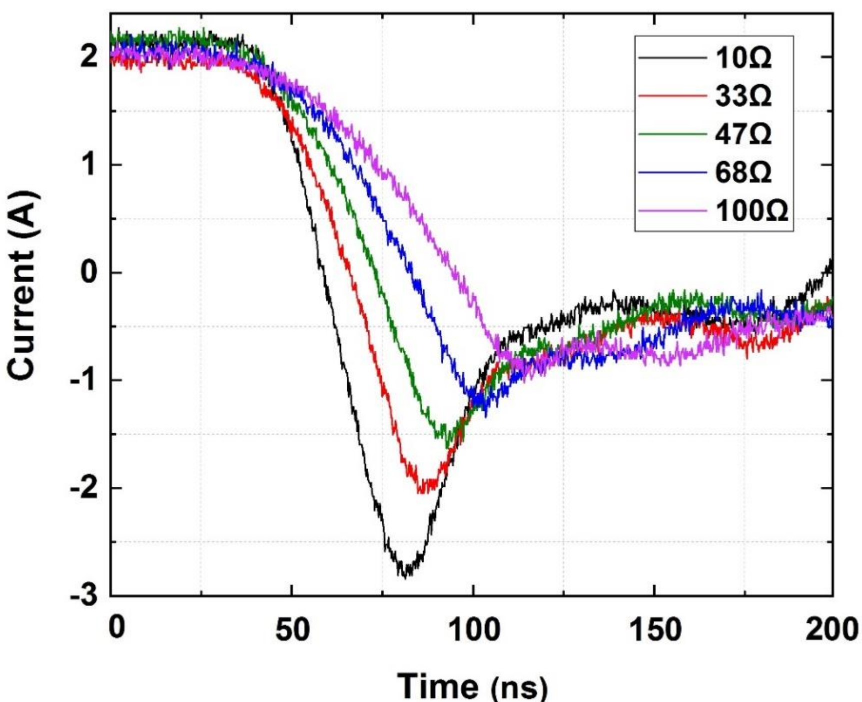


Figure 7-18: Reverse recovery waveform as a function of switching rate for the 1550°C annealed sample at 25°C, VDC=150 V.

7.6 Summary

In this chapter the results of lifetime enhancement of 4H-SiC PiN diodes with 35 µm drift region using high temperature oxidation/annealing treatment is presented. The fabricated diodes underwent thermal oxidation at 1450°C (Sample1) and 1550°C (Sample2) in pure dry O_2 followed by Ar annealing at 1550°C. The small-area diodes on the control sample showed a forward voltage drop of around 3.12 V at 100 A/cm^2 and 25°C with a corresponding differential on-resistance of approximately 2.07 mΩ-cm^2. The differential on-resistance of large-area PiN diodes on the control sample was

approximately 4.3 mΩ-cm^2 at 100 A/cm^2 and 25°C. The analysis of the I-V characteristics of the control sample revealed that the departure of I-V characteristics from the ideal diode behaviour in the low-current regime is due to the existence of conduction paths in parallel with the pn junction at the mesa sidewall exists. This was resolved by increasing the thickness of the passivation TEOS SiO_2 layer to higher than the mesa etch depth.

The forward I-V characteristics of both thermally oxidised/annealed samples were improved compared to the control sample, with the devices that were thermally oxidised at 1550°C (Sample2) yielding the best overall results. The forward voltage drop of devices on the 1450°C oxidised/annealed sample (Sample1) was around 3.09 V at 100 A/cm^2 and 25°C and for Sample2 was approximately 3.06 V. The differential on-resistance of the small-area PiN diodes on Sample1 was around 2.04 mΩ-cm^2 at 100 A/cm^2 and 25°C; this compared to approximately 1.9 mΩ-cm^2 for the Sample2 PiN diodes. Hence, it was seen that the differential on-resistance of the devices decreased with increasing the thermal oxidation temperature.

The forward log(J)-V characteristics of the PiN diodes revealed that under low-level current injection, the diodes exhibited an ideal characteristics ($\eta = 2$), confirming that the problem with the presence of conduction path in parallel with the *pn* junction had been resolved. But, in the diffusion current regime, the extracted ideality factor was $\eta = 1.4$ which was higher than the expected value of 1.

Finally, from analysis of the reverse recovery characteristics of all three samples, a larger I_{RP} and an improvement of the reverse recovery current was observed in the

1550˚C thermally oxidised/annealed PiN diodes in comparison with the other two samples. The reverse recovery characteristics also indicate an increase of 44% of the reverse recovery current for the 1550°C annealed sample compared to the control sample. This is due to the increase of excessive minority carriers in the drift region. The 1450°C oxidised sample also exhibits a 14% increase of the reverse recovery current compared to the untreated sample. Moreover, the reverse recovery charge of the control sample was 100 nC compared to 115 nC for the 1450˚C thermally oxidised/annealed sample and 127 nC for the 1550˚C thermally oxidised/annealed sample. A carrier lifetime of 542 ns was calculated from the reverse recovery characteristics for the 1550˚C thermally oxidised/annealed sample compared to around 440 ns for the 1450˚C thermally oxidised/annealed sample and 400 ns for the control sample. This shows an increase of around 40% in the carrier lifetime. These results indicate that the 1 hour oxidation time was not long enough for the 1450°C annealed sample to completely repair the carbon vacancy defects in the drift region and therefore further enhance the carrier lifetime. However, it was shown that the same treatment duration for the developed thermal oxidation and annealing process at 1550°C has resulted in obtaining the carrier lifetime necessary for the optimal performance of PiN diodes with 35 μm drift region thickness. Although it was seen that the developed thermal oxidation and successive Ar annealing process at 1550°C is highly effective in enhancing the carrier lifetime, it is evident that the quality of the starting material has an impact on the electrical performance of the devices. Moreover, it was shown that increasing the oxidation temperature reduces the overall carrier lifetime enhancement process time

and further repairs the lifetime-killing defects in the material. The developed high temperature oxidation and subsequent annealing process is a cost effective and time saving process which is beneficial for commercial device fabrication processes

In addition, it was shown that the reverse recovery characteristics of 4H-SiC PiN diodes are sensitive to increase of temperature where the peak reverse recovery current of the fabricated SiC PiN diodes increase with temperature. This is due to the positive temperature coefficient of the minority carrier lifetime which leads to higher reverse recovery charge during turn-off. It was also shown that, as expected, the reverse charge of the PiN diode increases with increasing the forward current as the stored charge during the on-state of the device increases with the forward current. It was experimentally shown that the reverse recovery characteristics become snappier as the supply voltage increases. This is due to the fact that increasing the supply voltage increases the extension of the depletion width into the PiN diode, therefore causing faster charge extraction and recombination. As expected, increasing the switching rate increases the snappiness of the reverse recovery characteristics of the PiN diode. The peak reverse recovery current increases with increasing the switching rate and the recovery current has a higher dI/dt.

Chapter 8 An Investigation into the Impact of Surface Passivation Techniques Using Metal-Semiconductor Interfaces

In this chapter Schottky barrier diodes were fabricated on SiC surfaces that had been treated with different surface passivation techniques, so that metal-semiconductor junctions could be used to evaluate the quality of this surface, using a range of metals including Mo, Ni, and Ti. The passivation treatments include the growth then removal of oxide layers formed in O_2, via direct N_2O growth and direct phosphorus pentoxide (P_2O_5) deposition. SBDs developed after the removal of these passivating layers were compared to those of untreated (control) surfaces and analysed physically, using TEM, X-ray Photoelectron Spectroscopy (XPS), and Secondary Ion Mass Spectroscopy (SIMS), and electrically using analysis techniques such as current-voltage-temperature (I-V-T) and inhomogeneity characterisation familiar to Schottky analysis as described in Chapter 3, Chapter 5, and Appendix B.

8.1 Background

Commercial device designs use junction barrier diode structure (JBS), which offers reduced leakage current and greater surge protection by integrating p-islands into the anode [195]. Further improvements to the SiC SBD are being sought by studying different Schottky contact metals. Until recently [196], titanium (Ti) and titanium-silicides have been preferred over nickel (Ni) and nickel-silicides, because of the low work function of Ti ($\varphi_{s,Ti}$=4.33 eV, $\varphi_{s,Ni}$=5.17 eV) resulting in lower Schottky barrier heights (SBHs) and thus minimal turn-on voltage, though at the expense of an increased leakage current compared to Ni. However, there has been a recent increase in interest into molybdenum (Mo) [5-7], a metal with a low work function similar to Ti ($\varphi_{s,Mo}$=4.46 eV [196]), but with a significantly higher melting point. This led in 2017 to Infineon integrating Mo into their 6th generation of SiC diodes [197, 198]. This results in a lower Schottky barrier height and hence reduced threshold voltage, though at the expense of higher reverse leakage currents [198]. Mo/SiC contact has been shown to have a very low ideality factor over a wide temperature range with a room temperature barrier height of 1.01 eV [5, 6].

Surface passivation treatments prior to metal deposition has been reported in the literature to improve the electrical characteristics of the fabricated diode. For example, it has been reported in [4] that prior to the deposition of Ni, post-oxidation annealing (POA) of SBDs in nitric oxide (NO) ambient forms C-N and Si-N bonds which passivate the 4H-SiC surface and carbon related defects and significantly reduce

leakage current. Trapped charge is also known to affect the homogeneity of a Schottky interface, with charge trapped at the semiconductor interface causing Fermi level pinning, and hence affecting the diode's Schottky barrier height (SBH), ideality factor and reverse leakage current [7].

Use of nitrogen, phosphorus or argon treatments have been employed in the fabrication of 4H-SiC MOSFETs, whereby the interface trap density (D_{it}) of the oxide-semiconductor interface is significantly reduced to enhance channel mobility after oxide growth [199-201]. Substantial advancement has been made regarding interface passivation over the last decade, especially with post oxidation annealing or direct growth in NO or N_2O environments, providing a channel mobility of around 20-35 $cm^2/V.s$ for 4H-SiC (0001) MOSFET [142-144]. It was also reported in [191] that thermal oxidation at 1500°C under low oxygen flow rate can decrease MOS interface D_{it} to around 2×10^{11} $cm^2/V.s$. Amongst these passivation techniques, annealing in N_2O ambient is reported to be the most effective technique [202]. However, as reported in [7, 138, 200, 203], direct phosphorus pentoxide (P_2O_5) deposition on SBDs and MOSFETs has resulted in improvement of both leakage current densities for SBDs and channel mobility of the MOSFETs. Some studies have reported that phosphorous treatment is more effective than NO or N_2O passivation treatments, providing peak mobilities of 80-90 $cm^2/V.s$ [138, 145] and even up to 108 $cm^2/V.s$ [146] for 4H-SiC MOSFETs fabricated on the conventional (0001) Si-face. Hence, it was shown that pre-treatments of SBDs have the potential to minimise the drawbacks of using gate metals

with low barrier heights and therefore the motivation to perform the SiC surface treatment in this Chapter.

In this chapter, the impact of surface passivation treatments on both the SiC surface and metal semiconductor interface prior to the device fabrication is investigated. SBDs (Ti, Ni and Mo) are then fabricated on the treated surfaces and are characterised. The passivation treatments include the growth then removal of oxide layers formed in O_2, via direct N_2O growth and direct phosphorus pentoxide (P_2O_5) deposition. SBDs developed after the removal of these passivating layers were compared to those on untreated (control) surfaces and analysed physically using XPS, SIMS, TEM, and SEM, and electrically using I-V and I-V-T characteristics as well as inhomogeneity characterisation familiar to Schottky analysis. The findings of this investigation can be potentially employed for MOS interface improvement.

8.2 Experimental Details

Schottky diodes were fabricated to analyse the effect of different passivation treatments. With no termination, these were designed to test the turn on and leakage current of the devices, but not the breakdown voltage. SBDs were formed on untreated 4H-SiC surfaces, and after the surface treatments have been performed, and the resulting oxides were removed. Then Mo, Ni, and Ti Schottky barrier diodes were fabricated as explained in the following section.

8.2.1 Device Fabrication

The Schottky diodes used in this work were fabricated in-house using a 4-inch 4H-SiC wafer with a 35μm thick epi layer of a 4×10^{15} cm^{-3} n-type doping. 12 samples were fabricated, each containing at least 90 SBDs. After dicing, the dies underwent standard RCA cleaning process to remove any residual materials, impurities, dirt or dust on the surface of the material, as explained in detail in Section 4.1.2. The next fabrication process was the passivation treatment. The 4H-SiC surface of the control sample was untreated and the other samples underwent surface passivation treatment, in each case to form 100 nm of passivating oxide:

- The thermal oxidation was performed in a Hi-Tech furnace (Figure 4-3) at 1400°C for 4 hours in O_2 ambient. Wafers are loaded on to the SiC wafer carrier of the furnace at around 600°C with Ar flowing at 5 lit/min to prevent any oxygen flow in the furnace. The temperate is then raised to the oxidation temperature with ramping rate of 5°C per minute. Oxidation process is then started with 20% oxygen (1 L/min) in Ar (4 L/min) ambient. The samples are held at the desired temperature for 4 hours to grow 100nm of the desired passivating oxide. After the oxidation process, the temperature is ramped down to 600°C at 5°C per minute in Ar (5 L/min).
- Direct N_2O oxidation was also performed in Hi-Tech furnace at 1300°C for 4 hours. The N_2O oxidation profile was similar to oxidation process, but the samples were held for 4 hours at 1300°C in 20% N_2O (1 L/min) and Ar (4 L/min) ambient. After

the N_2O oxidation process, the temperature was ramped down to 600°C at 5°C per minute in Ar (5L/min).

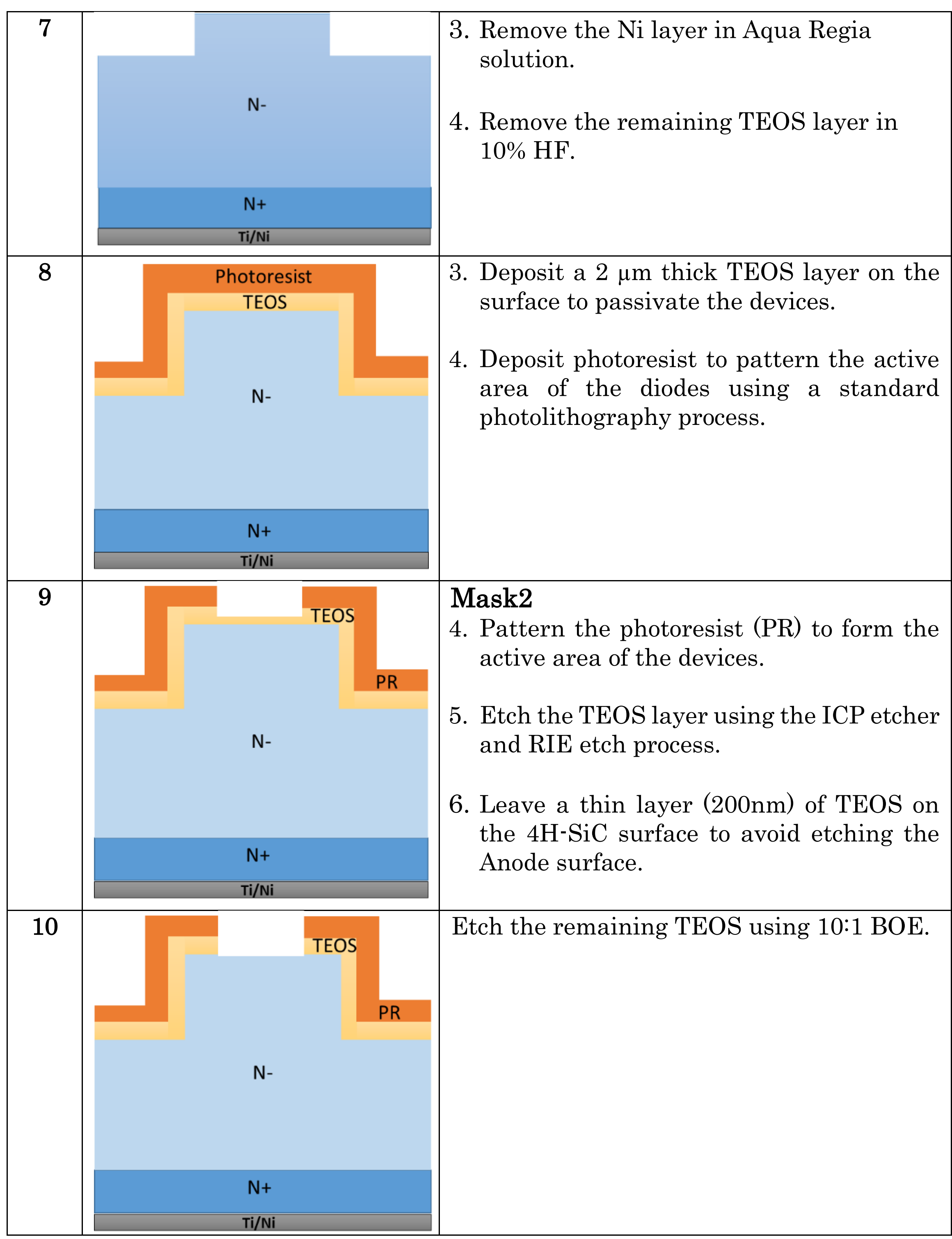
- P_2O_5 deposition process is discussed in detail in Chapter 4, Section 4.1.4.4. SiC samples were annealed in annealing furnace (Figure 4-5) at 1000°C for 2 hours in N_2 ambient (5 L/min) in front of a SiP_2O_7 source wafer.

In the next step, all the samples were cleaned in dilute HF to remove the grown oxide before the individual active areas of Schottky diodes were defined and mesa-isolated. The Schottky diode fabrication process is shown in Table 8-1. The active area of the devices was 4.53 x 10^{-4} cm^2.

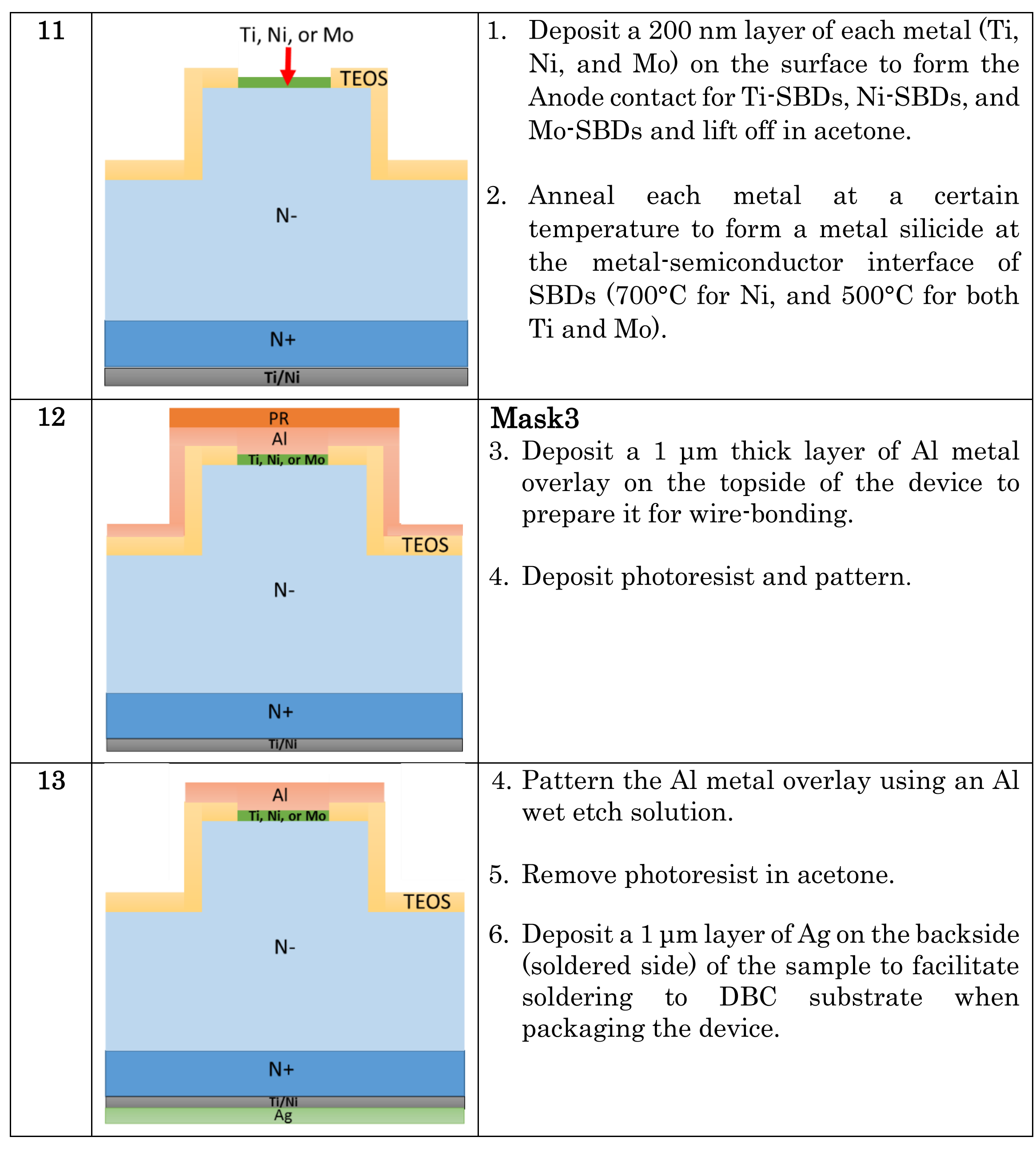
Table 8-1: 4H-SiC Schottky diode fabrication process flow.

Step	Cross-sectional diagram	Fabrication process
1	N- N+	Remove the grown oxide in dilute HF before the individual active areas of Schottky diodes are defined and mesa-isolated.
2	N- N+ Ti/Ni	3. Deposit a 30 nm layer of Ti followed by a 100 nm layer of Ni to form the Cathode contact. 4. Rapid thermal annealing (RTA) process at 1000°C for 2 minutes to form ohmic contacts to the backside of Schottky diodes.

3	Ni TEOS N- N+ Ti/Ni	Deposit a 1 µm layer SiO_2 TEOS and 300 nm of Ni as masking layers for 4H-SiC etching process. Ni was deposited using E-beam evaporation system.
4	Photoresist Ni TEOS N- N+ Ti/Ni	**Mask1** Deposit photoresist and pattern to mesa-isolate the individual Anodes.
5	Photoresist Ni TEOS N- N+ Ti/Ni	3. Etch the Ni layer in Ni wet etch solution (Nitric Acid (HNO_3), Acetic Acid (CH_3COOH), Sulfuric Acid (H_2SO_4) and DI waster in the ratio 4:4:1:10) for 30 seconds. 4. Etch the TEOS layer in the ICP etcher using RIE etch process to obtain a vertical sidewall profile.
6	Ni TEOS N- N+ Ti/Ni	3. Remove photoresist in an O_2 plasma. 4. Etch the 4H-SiC to the required depth (1 µm in this case) to form the mesa-isolation of Anodes area (mesa etch) in the ICP etcher, using ICP etch process. The etch rate of the process was 700 nm/min.



Step	Cross-section	Description
7		3. Remove the Ni layer in Aqua Regia solution. 4. Remove the remaining TEOS layer in 10% HF.
8		3. Deposit a 2 μm thick TEOS layer on the surface to passivate the devices. 4. Deposit photoresist to pattern the active area of the diodes using a standard photolithography process.
9		**Mask2** 4. Pattern the photoresist (PR) to form the active area of the devices. 5. Etch the TEOS layer using the ICP etcher and RIE etch process. 6. Leave a thin layer (200nm) of TEOS on the 4H-SiC surface to avoid etching the Anode surface.
10		Etch the remaining TEOS using 10:1 BOE.



11		1. Deposit a 200 nm layer of each metal (Ti, Ni, and Mo) on the surface to form the Anode contact for Ti-SBDs, Ni-SBDs, and Mo-SBDs and lift off in acetone. 2. Anneal each metal at a certain temperature to form a metal silicide at the metal-semiconductor interface of SBDs (700°C for Ni, and 500°C for both Ti and Mo).
12		**Mask3** 3. Deposit a 1 μm thick layer of Al metal overlay on the topside of the device to prepare it for wire-bonding. 4. Deposit photoresist and pattern.
13		4. Pattern the Al metal overlay using an Al wet etch solution. 5. Remove photoresist in acetone. 6. Deposit a 1 μm layer of Ag on the backside (soldered side) of the sample to facilitate soldering to DBC substrate when packaging the device.

8.3 Results and Discussion

In this Section, the forward I(J)-V, characteristics are presented for the fabricated Schottky diodes with different metal contacts and surface treatments. The on-state behaviour of these devices has been evaluated by means of forward and reverse I-V measurements at a range of temperatures.

8.3.1 Electrical Characterisation

The full set of electrical characteristics results obtained from all the SBDs with different passivation techniques are presented in Table 8-2. This shows the average reverse leakage current, ideality factor and SBH derived from I-V measurements before and after annealing, and SBH and doping profile from C-V measurements. Each result is the average of at least 20 of each diode tested. All the diodes were characterised using a Keysight B1505A parameter analyser and semiconductor probe station at room temperature. Extraction of SBH, ideality factor and doping density from C-V measurements is discussed in Appendix B. It was assumed that thermionic emission was the governing conduction mechanism at the Schottky barrier for the diodes.

After depositing a contact metal (Mo, Ni and Ti), but prior to contact annealing, current-voltage-temperature (I-V-T) and capacitance voltage (C-V) measurements helped assess the effects of the passivation treatments on the SiC surface. With no anneal, no silicides having been formed at the interface, these results give another

perspective on the impact of these treatments on the SiC/SiO_2 interface. However, we were mainly limited to C-V analysis prior to annealing, as the quality of the I-V data did not permit SBH or ideality factor extraction. However, it can be seen from Table 8-2 that before contact annealing, there is little difference between the SBH obtained from different treatments and different contact metals (with vastly different work functions). The barrier heights extracted from C-V analysis before contact annealing show just 0.17 eV variation across all the diodes, suggesting that the interface is Fermi-Level pinned, the result of significant interface traps. Fermi-level pinning for metal/semiconductor Schottky barrier refers to the phenomenon in which surface states of a semiconductor bring about a fixed barrier height, independent of metal [204]. Surface states can include inhomogeneities, surface abnormalities such as roughness, non-uniform doping or non-ideal surface preparation processes resulting in an unclean surface (contamination of the surface) or an interfacial oxide. Surface states can occur at any energy within the semiconductor bandgap. To sustain charge balance within the surface and the space charge region (depletion region), surface band bending happens which pins the Fermi level of the semiconductor to a point at the surface which is energetically neutral. For some semiconductors it has been found that band bending in the semiconductor metal contact is principally independent of the metal even for metals having very large differences in work function [204].

Table 8-2: leakage current, ideality factor and SBH derived from I-V measurements before and after contact annealing, and SBH and doping profile from C-V measurements. Each result is the average of at least 20 of each diode tested.

	Mo				Ti				Ni			
	As depo	Thermal Oxide	N_2O Oxidation	P_2O_5	As depo	Thermal Oxide	N_2O Oxidation	P_2O_5	As depo	Thermal Oxide	N_2O Oxidation	P_2O_5
SBH from C-V before anneal [ev]	1.61	1.59	1.59	1.58	1.75	1.72	1.74	1.68	1.73	1.68	1.67	1.67
SBH From C-V after anneal [ev]	1.15	1.24	1.2	1.16	1.23	1.23	1.19	1.23	1.81	1.84	1.84	1.84
Doping from C-V after contact anneal [cm^{-3}]	2.3×10^{15}	2.17×10^{15}	2.21×10^{15}	2.32×10^{15}	3×10^{15}	3.19×10^{15}	2.91×10^{15}	3.23×10^{15}	4.16×10^{15}	4.15×10^{15}	4.15×10^{15}	4.07×10^{15}
SBH from I-V after anneal [ev]	1.28	1.28	1.27	1.27	1.21	1.22	1.06	1.08	1.60	1.62	1.60	1.60
Ideality factor after anneal	1.04	1.06	1.04	1.05	1.08	1.06	1.34	1.36	1.06	1.05	1.07	1.08
Reverse Leakage @-200V [A/cm^2]	6.64×10^{-3}	3.05×10^{-3}	1.6×10^{-3}	4.44×10^{-5}	7.7×10^{-1}	1.04	3.27	1.02	8.79×10^{-3}	3.29×10^{-3}	5.54×10^{-3}	6.78×10^{-3}

After annealing the contacts and the formation of metal silicides at the interface, the same electrical characterisation techniques were used to examine the impact of these treatments on SBDs themselves. This process largely reduced the amount of charge at the metal-semiconductor interface and both I-V and C-V data showed the expected work function dependence. The difference between the SBH values taken from C-V measurements and the ones taken from I-V measurements after contact annealing could be explained by the method which these two techniques extract the barrier height (Chapter 3 and Appendix B). C-V and I-V SBH extraction methods are based on the assumption that there is one uniform or homogeneous barrier height across the interface. However, this is not true for most interfacial layers, where inhomogeneities at the surface results in a 2D variations in the SBH. As a result, a frequently reported phenomenon happens where the SBH value obtained from the C-V measurements are higher than that attained from I-V analysis [205-207]. This is due to the fact than by using I-V measurements, most of the current that goes through the layer only passes over the lower barriers (least resistive paths). However, the SBH values extracted using C-V measurements are an average across the entire interface.

According to Table 8-2, there is evidence that the surface treatments result in a lower SBH when measured prior to annealing the contacts, similar to [197], though by only 10-60 meV in our case. This should typically result in higher reverse leakage, however, a significant decrease in the leakage current using P_2O_5 treatment for Mo-SBD is achieved. After annealing the contacts, these differences are less pronounced in Ni/Mo SBDs. Only P_2O_5 and N_2O treated Ti-SBDs retain some variation, having very

high ideality factor values. Poor ideality factor and lower SBH are an indicator of a poor (inhomogeneous) contact that skews the I-V plots.

No major improvement in the ideality factor was seen. All the diodes (except N_2O and P_2O_5 treated Ti-SBDs) had a very low ideality factor value, confirming that thermionic emission is the dominant current transport mechanism [207] as predicted by the diode equation of Equation 5-1. It can also be seen that the O_2 oxidation treatment seems to have degraded the electrical characteristics of all diodes, resulting in a higher average SBH.

The doping extracted from post-anneal C-V data varies from the Ni diodes, at the expected value of 4×10^{15} cm^{-3}, to the Ti (~3×10^{15} cm^{-3}) and Mo diode (~2×10^{15} cm^{-3}). This occurs due to bending in the C^{-2}-V plot used to extract the value which is most pronounced in the Mo, and the result of charge at the interface that skews the measurement. This is shown in Figure 8-1 for N_2O treated Mo, Ni, and Ti-SiC SBDS before contact annealing. Doping concentration extraction using capacitance-voltage method is explained in Appendix B. According to C-V test results, Ni-SBDs do not have as much trapped charge at the metal/semiconductor interface, but they show the expected doping concentration. Figure 8-2 shows the forward characteristics of Mo/SiC, Ni/SiC Ti/SiC SBDs after annealing with different surface treatments.

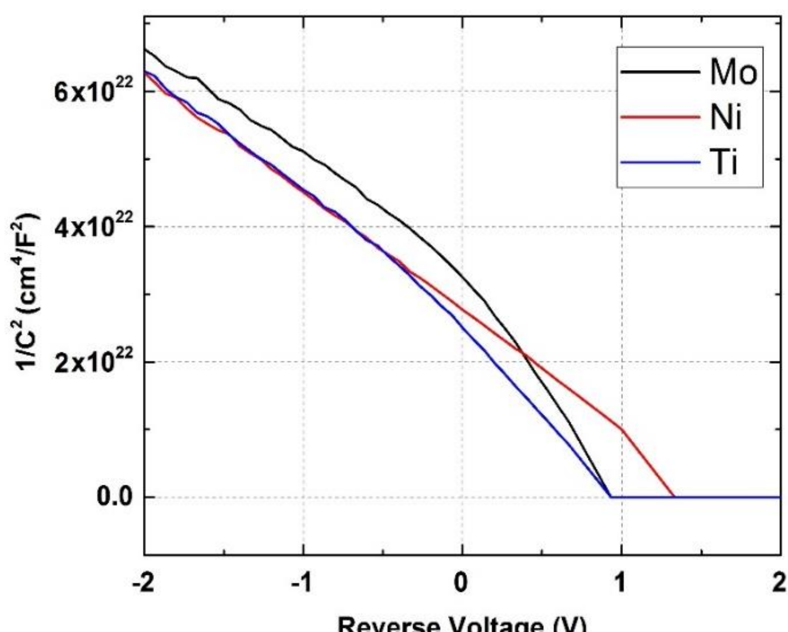


Figure 8-1: The C^{-2}-V used to extract the doping value (N_2O treated diodes before contact annealing).

The most significant outcome of this work was the performance of P_2O_5 treated Mo diodes. These appear to break the trade-off between turn-on voltage and leakage current by having a low barrier height (consistent with all the Mo and Ti diodes), but also the lowest leakage of any device (4.44×10^{-5} A/cm^2). This is contrary to the expectations that lower Schottky barrier height and hence lower turn-on voltage will result in an increase leakage current, as happened for Infineon devices when they moved from Ti to Mo [198, 208].

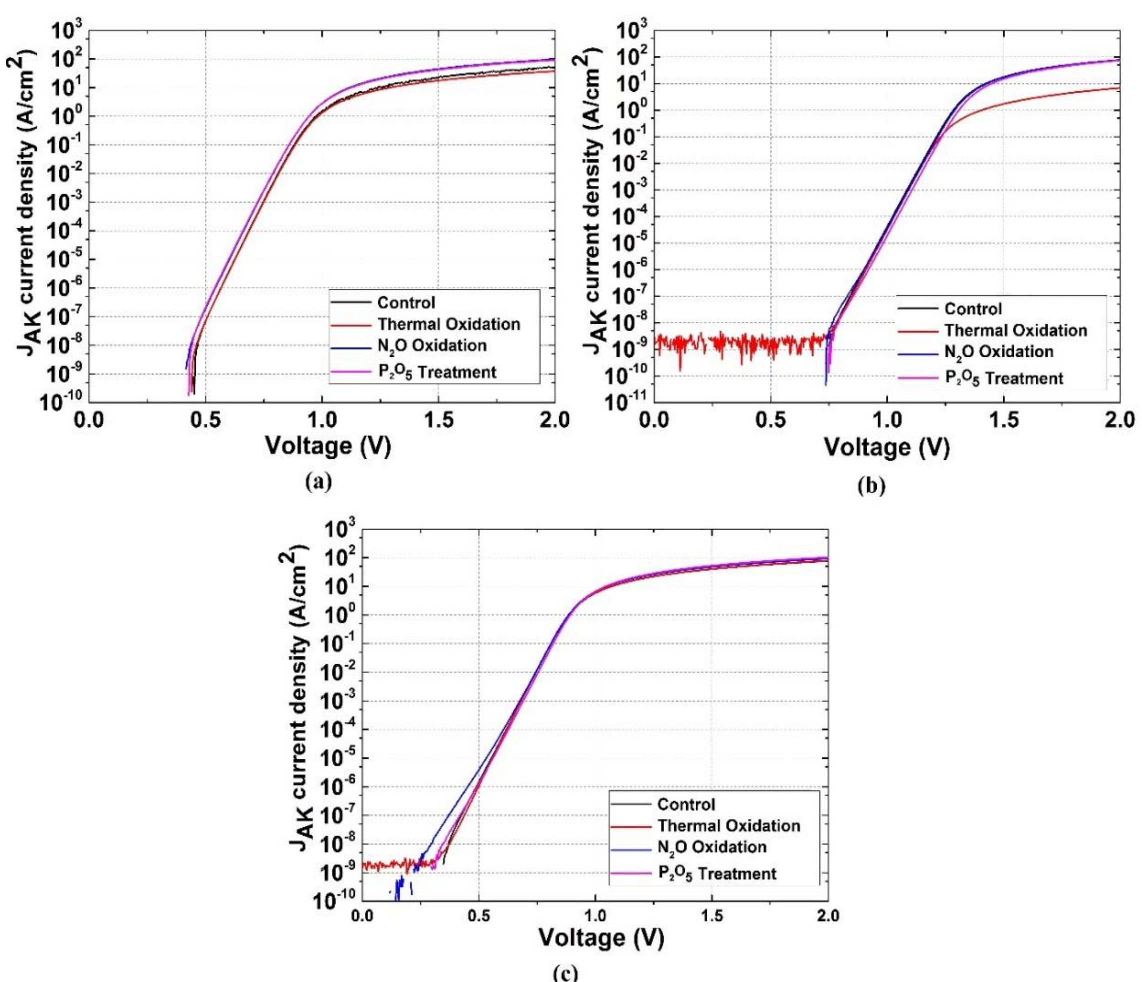


Figure 8-2: Forward characteristics of (a) Mo/SiC, (b) Ni/SiC and (c) Ti/SiC SBDs using different surface passivation treatments.

Figure 8-3 compares the reverse I-V characteristics of Mo/SBDs and Ni/SBDs with various surface treatments. It can be seen that the P_2O_5 treatment in Schottkey diodes with Mo contact improves the leakage current by 3 orders of magnitude. P_2O_5 treatment on Ni/SBDs does not seem to have improved the reverse characteristics. In fact, the control samples appear to have slightly better reverse characteristics compared to the other Ni/SBDs with various metal-semiconductor interface treatments.

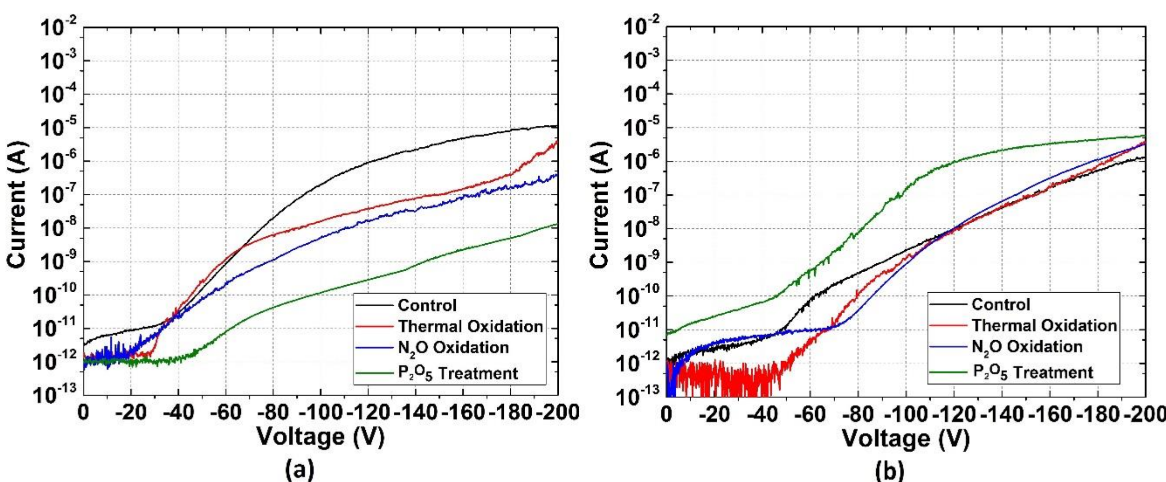


Figure 8-3: Reverse I-V characteristics of (a) Mo/SBD diodes and (b) Ni/SBD diodes

The electrical characteristics obtained from current-voltage analysis of Mo/SiC SBDs are presented in Figure 8-4 using box and whisker plots to represent at least 30 different Mo SBDs of each type. Figure 8-4 (a) suggests little variation in SBH, which ranges from 1.26 for the P_2O_5 treated diodes to 1.29 for the thermal oxidation treated diodes. Similarly Figure 8-10 (c) shows little variation in ideality factor, with all devices having $n<1.1$, with the thermal oxidation treated diodes fractionally higher, and less consistent than the others.

The significant outcome of this study is again shown in Figure 8-4 (b), which represents the leakage current of the diodes at -200 V. Here, the P_2O_5 treated Mo diodes are seen to consistently achieve a leakage current averaging of two orders of magnitude lower than the N_2O or thermal oxidation treated diodes and three orders of magnitude lower than the untreated control diodes. To investigate the mechanisms by which the P_2O_5 treatment improves the diode characteristics, a series of physical analyses were carried out.

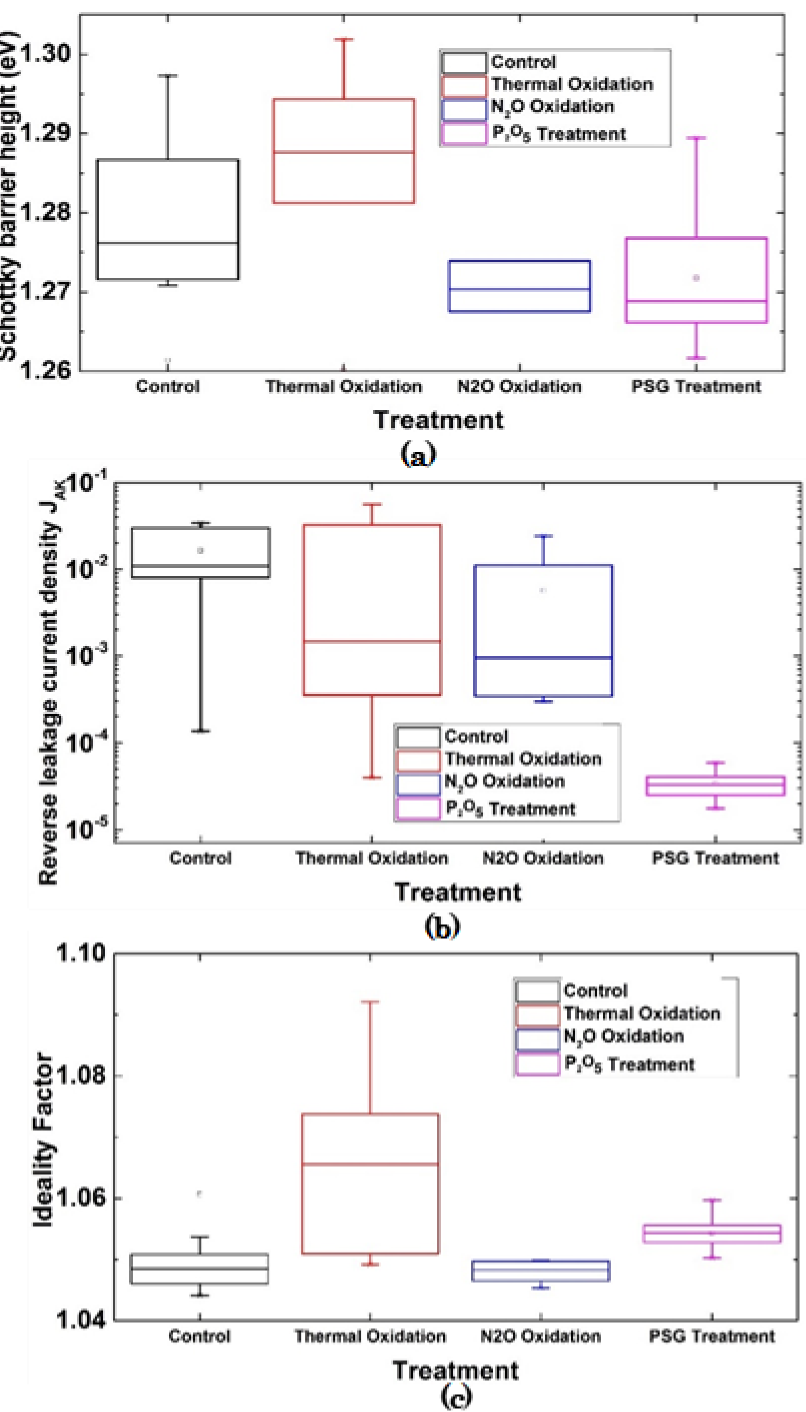


Figure 8-4: (a) Schottky Barrier Height (SBH), (b) reverse leakage current density measured at 200 V and (c) ideality factor, all derived from I-V measurements on Mo/SiC diodes, post-anneal. Each dataset contains at least 30 of each diode tested.

The reverse breakdown characteristics of the fabricated Mo/SiC Schottky diodes were previously shown in Section 5.1.3, Figure 5-6.

8.3.2 Inhomogeneity of the Diodes

Even when the P_2O_5 treated Mo-SBDs were tested at 300°C, a leakage of 7.26×10^{-4} A/cm^2 is much lower than any of the other devices at room temperature. The results of I-V-T testing of the P_2O_5 treated and N_2O treated diodes can be seen in Figure 8-5 and Figure 8-6 respectively. I-V-T testing was carried out using the science city clean room variable temperature probe station as shown in Figure 8-7. Figure 8-6 (a) shows the temperature dependant I-V plot of N_2O treated Mo/SiC Schottky diode. The temperature is shown to directly affect the plot where carrier mobility decreases considerably with increasing temperature due to the increased lattice vibrations and hence more scattering events. This results in the increase in resistance seen above 1 V. Moreover, an increase in temperature also increases thermionic emission current, but the built-in potential drops. This causes the variations in reverse leakage current and turn-on voltage.

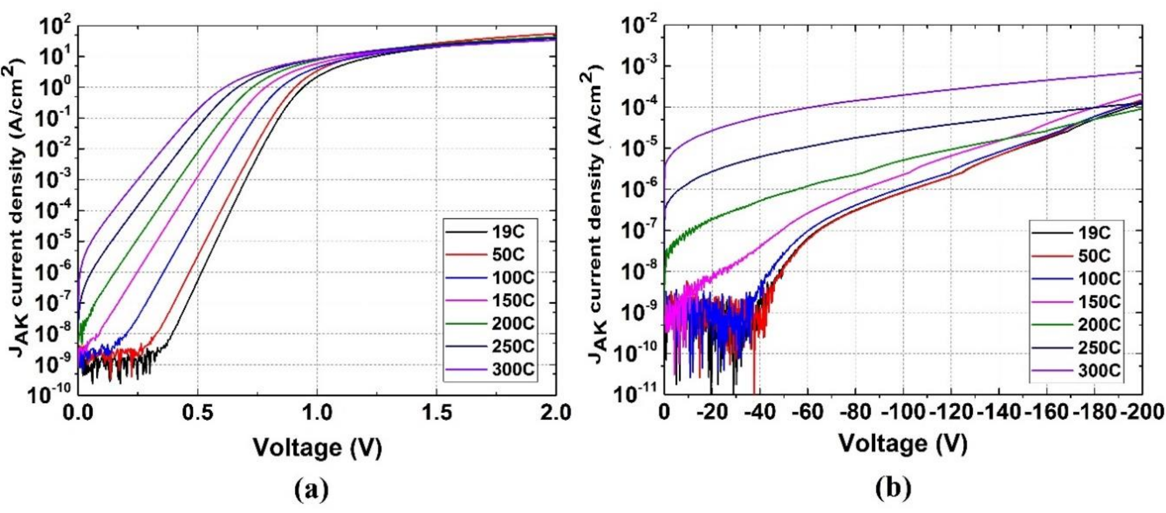


Figure 8-5: (a) Forward and (b) Reverse I-V-T characteristics of P_2O_5 treated Mo/SiC at different temperatures.

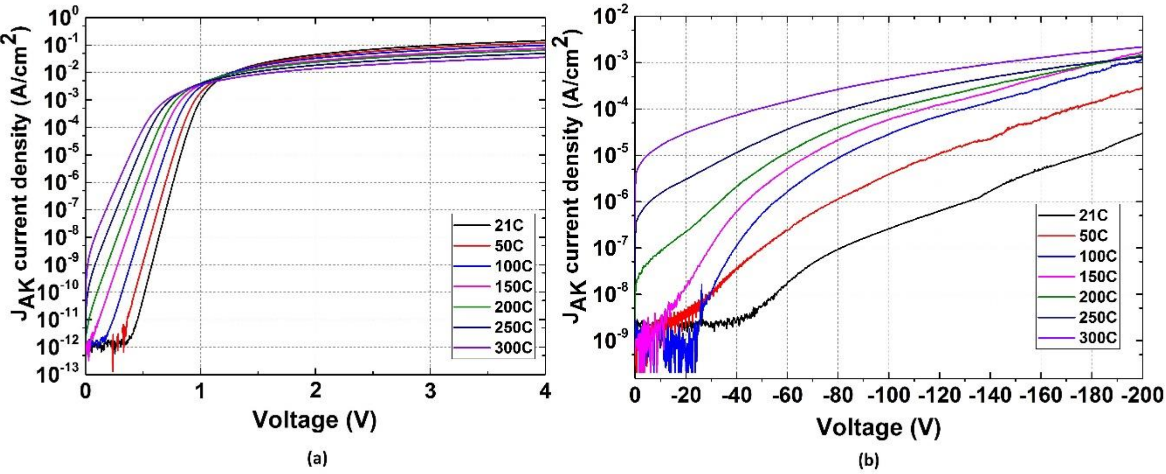


Figure 8-6: (a) Forward and (b) Reverse I-V-T characteristics of N_2O treated Mo/SiC at different temperatures.

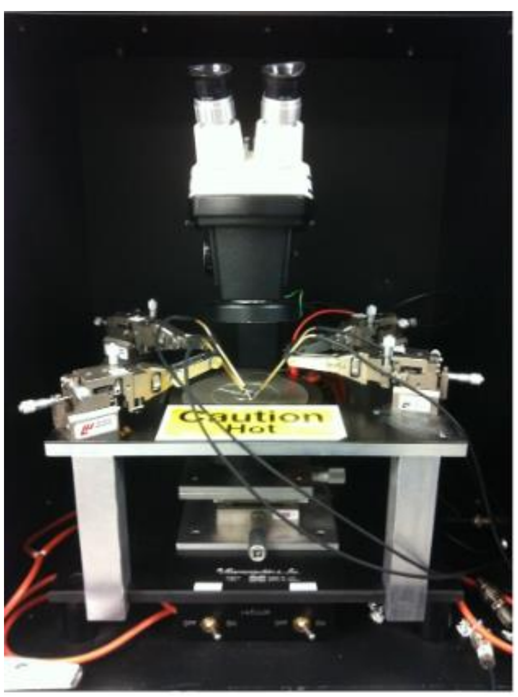


Figure 8-7: Variable temperature probe station set up in the clean room.

I-V measurements were taken on the Mo/SiC diodes across a wide range of temperature. The I-V results taken at room temperature demonstrate comparative consistency across the fabricated batch. Focusing on one typical diode, a barrier height of 1.26 eV, an ideality factor of 1.021 and leakage current of 4×10^{-5} A/cm^2 at 200 V, propose that the contacts are of good quality at 300 K. Additionally, as shown in Figure 8-8 (a), I-V results taken down to 40 K, illustrate a consistent set of characteristics across a wide range of temperatures. Though, as shown in Figure 8-8 (c), by plotting the ideality factor and SBH against temperature, it can be seen that below 100 K, the ideality factor will gradually rise to values far beyond 2, whereas the SBH mirrors this

by falling at lower temperature. According to the fundamental theory in [42], such high values of ideality factor propose that the recombination current transport is dominant. However, according to Schottky barrier height inhomogeneity theory, this is the inherent breakdown of the ideality factor concept. Moreover, the positive SBH-temperature relationship is counterintuitive given that a negative temperature dependence exists for the bandgap, while any freeze-out of the dopant should also result in a negative SBH-temperature relationship.

The typical non-linearity of a log(I)-V plot is shown in Figure 8-8 (b) where the dependency of ideality factor to voltage is demonstrated. Figure 8-8 (b) zooms into the exponential area of the temperature responses of three devices and a dotted line has been fitted to the first two decades of these responses. This confirms there is constantly some voltage dependence of the ideality factor, even at room temperature, which increases at lower temperatures. This is due to the parallel conduction paths arising through area of variable barrier height. As in [209], the ideality factor can be plotted against the current density at which it is extracted to better show this effect.

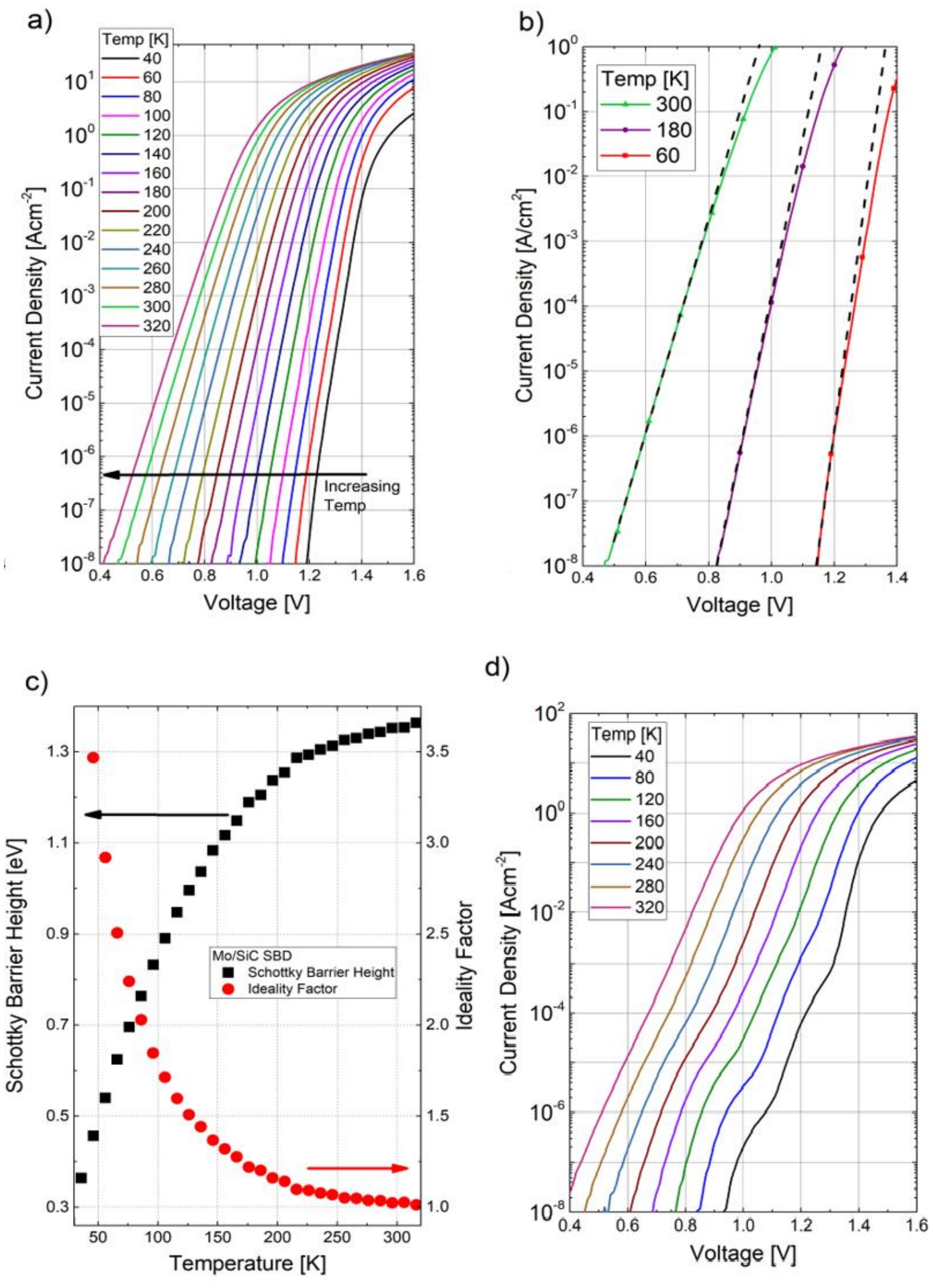


Figure 8-8: The effects of SBH inhomogeneity shown on a Mo/SiC Schottky diode. (a) IVT characteristics of a single device. (b) Zooms in on three of the temperatures showing increasing voltage dependency at low temperature. (c) Extracted SBH and ideality factor across the temperature range, d) is a second device showing chip to chip variability and characteristic double bumps.

Figure 8-8 (d) shows another Mo/SiC diode, an outlier in the batch of fabricated devices, showing chip to chip variability and characteristic multiple bumps with poor turn-on characteristics. The diode's I-V characteristics show three turn on regions at low temperature and two turn on at high temperature, signifying the existence of multiple macroscopic areas with different barrier height. This can occur when the Schottky contact covers a defective or dirty area of the wafer and can be represented as having two or more diodes with different metals in parallel between areas with double bumps. First, the diode with the lowest barrier conducts then it becomes resistive, before the second lowest barrier conducts and becomes resistive, and so on.

Figure 8-9 shows the Low temperature I-V-T characteristics of P_2O_5 treated Mo/SiC in a temperature range from 320 to 25 K. At low temperatures, the effect of carrier freeze-out is seen in 4H-SiC. Electrons move more slowly, and lattice vibrations are low as well; therefore, the ion impurity forces which have a slight effect on high-energy particles become the governing limit to mobility. Hence, lowering the temperature prolongs the amount of time electrons spend passing an impurity ion, decreasing the mobility as temperature declines (μ_{cb}/T). Thus, in Figure 8-9, as the temperature drops, the resistance increases.

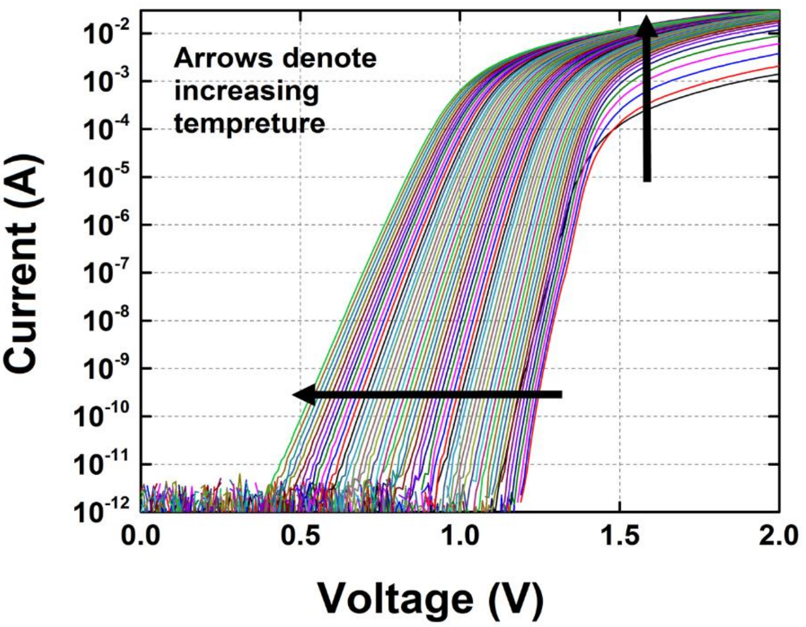


Figure 8-9 Low temperature I-V-T characteristics of P2O5 treated Mo/SiC at different temperatures, from 320K at the left to 25K (black line).

8.3.3 Physical Characterisation

To further understand the mechanisms by which the P_2O_5 treatment improves the Mo diode characteristics, a series of physical and electrical analyses were performed.

8.3.3.1 X-Ray Photoelectron Spectroscopy (XPS) & Secondary Ion Mass Spectroscopy (SIMS)

X-ray photoelectron spectroscopy characterisation was performed in order to investigate the physical and chemical properties of the Mo/SiC interface. Separate

samples were prepared using the same fabrication procedure described in Section 8.2.1, omitting the patterning of device structures and instead thinning the Mo to allow the metal-semiconductor interface to be studied by XPS. A SF_6 dry etch process was performed using a Coriel 200IL to reduce metal thickness and the samples were loaded into a Kratos Axis Ultra DLD XPS system. Once loaded, an argon sputter process was used to further thin the metal until the bulk SiC could be detected alongside the Mo metal.

High-resolution core spectra were taken for Si 2p, C 1s, Mo 3d, P 2p and N 1s and data was analysed using CasaXPS software package, employing linear backgrounds and Voigt (Gaussian-Lorentzian) lineshapes. The P 2p and N 1s spectra showed no photoemission within the detection limits of the instrument, indicating that the oxide removal, metallisation and/or sputter thinning processes removed the treatment elements. The Si 2p and C 1s spectra of untreated sample are shown in Figure 8-10. The x-axis is binding energy, shown in reverse direction (i.e. higher binding energy to the left, lower to the right). Low binding energy is characteristic of bonding to a metal or an electropositive element. High binding energy is characteristic of bonding to oxygen or an electronegative element. In Figure 8-10 (a), the component shown using a red dashed trace represents carbon atoms bonded to silicon (i.e. SiC).

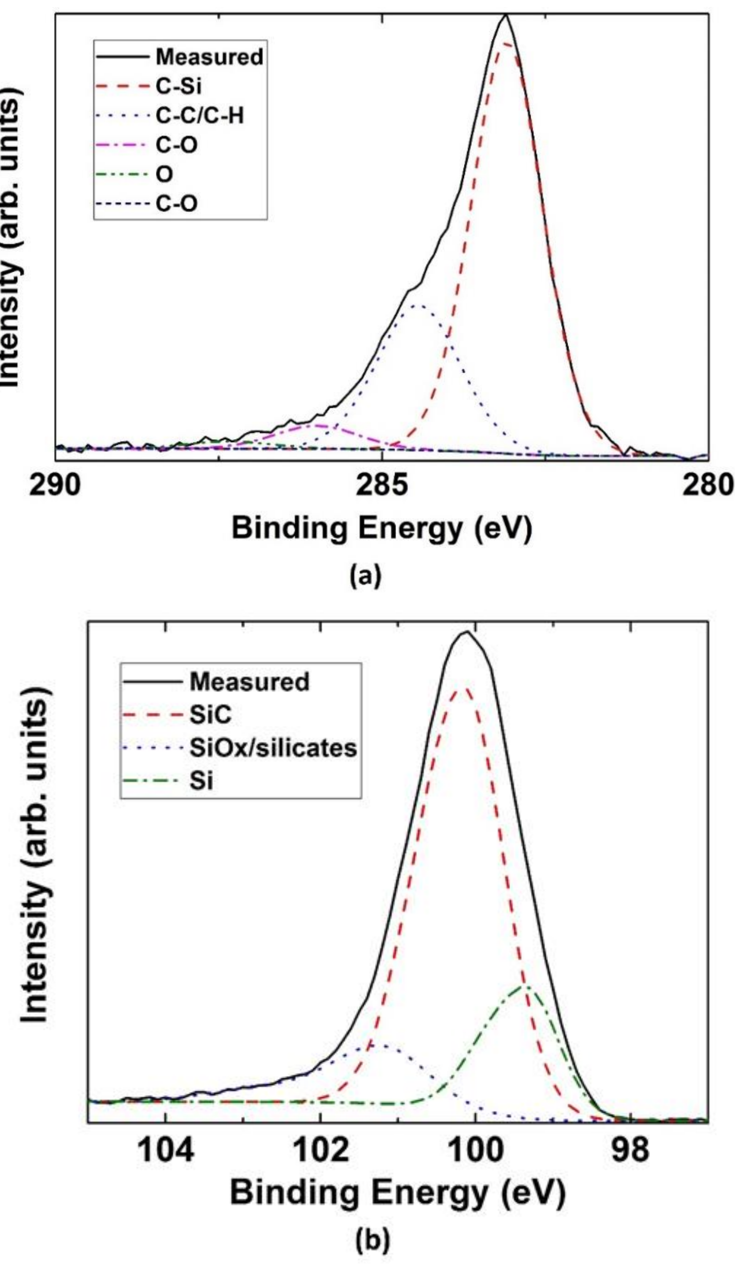


Figure 8-10: XPS data for the (a) C 1s region and (b) Si 2p region without surface treatment.

In Figure 8-10 (b), the red dashed trace represents the corresponding silicon atoms bonded to carbon. For an ideal surface, the C:Si ratio should be close to 1 implying that there are few carbon clusters and/or that the surface is clean, orderly and close to an ideal surface. As elemental carbon from the oxidation process could not be distinguished from atmospheric carbon, the stoichiometry of the interface was investigated quantitatively using the relative atomic concentration of SiC components in the C 1s and Si 2p spectra, shown in Table 8-3. This was found using CasaXPS software which calculates the area under each peak to show the relative atomic percentage of SiC in the C 1s and Si 2p spectra. The XPS results show that the devices that have undergone the P_2O_5 treatment improve the Si:C ratio, reaching stoichiometry value of 0.99, hence there is less C enrichment compared to the untreated sample and other treatments. Therefore, this suggests that the P_2O_5 treatment improves the metal-semiconductor interface of the devices by getting rid of carbon clusters.

The poorest stoichiometry was observed for the oxidation treatment. Only the N_2O and P_2O_5 treatments improved on the control sample, with the P_2O_5 treatment offering a significant improvement on the control sample. The XPS data shows that, consistent with the carbon cluster model, the oxidation treatment increased the concentration of carbon at the metal-semiconductor interface. The data also shows that performing a phosphorus diffusion process in N_2 ambient reduces carbon enrichment at the interface and that this effect, may be responsible for improved device performance and its lower reverse leakage currents.

Table 8-3: Ratio of SiC atomic percentage from the C 1s spectrum to SiC atomic percentage from the Si 2p spectrum for each surface treatment

Surface Treatment	SiC in Si 2p / SiC in C 1s
Control	0.95
O_2	0.93
N_2O	0.96
P_2O_5	0.99

During XPS analysis of the Mo/SiC interface, no phosphorous photoemission was seen from any of the treated samples except the P_2O_5 treated sample. The P 2p spectrum of the P_2O_5 treated sample is shown in Figure 8-11 (top) where photoemission from phosphorous was seen at the Schottky interface (Mo-SiC interface) confirming the presence of phosphorous pentoxide following P_2O_5 treatment. This shows that traces of P_2O_5 can be found near the surface even after the removal of oxide by HF.

Figure 8-11 (bottom) shows the secondary ion mass spectroscopy (SIMS) spectra on the P_2O_5 treated sample to further confirm the existence of phosphorus after P_2O_5 treatment and Mo contact metallisation and understand its depth distribution. To perform SIMS analysis, a sample was prepared using the same P_2O_5 treatment and Mo deposition as discussed in Section 8.2.1. SIMS was performed using Si, C and P^+ matrix markers at a high resolution (<1 nm) near the Mo/SiC interface (100 nm- 200nm). The P quantification is based on the SiC. Phosphorus concentrations of up to $1.5 \times 10^{19} cm^{-3}$ could be detected at the Mo/SiC interface.

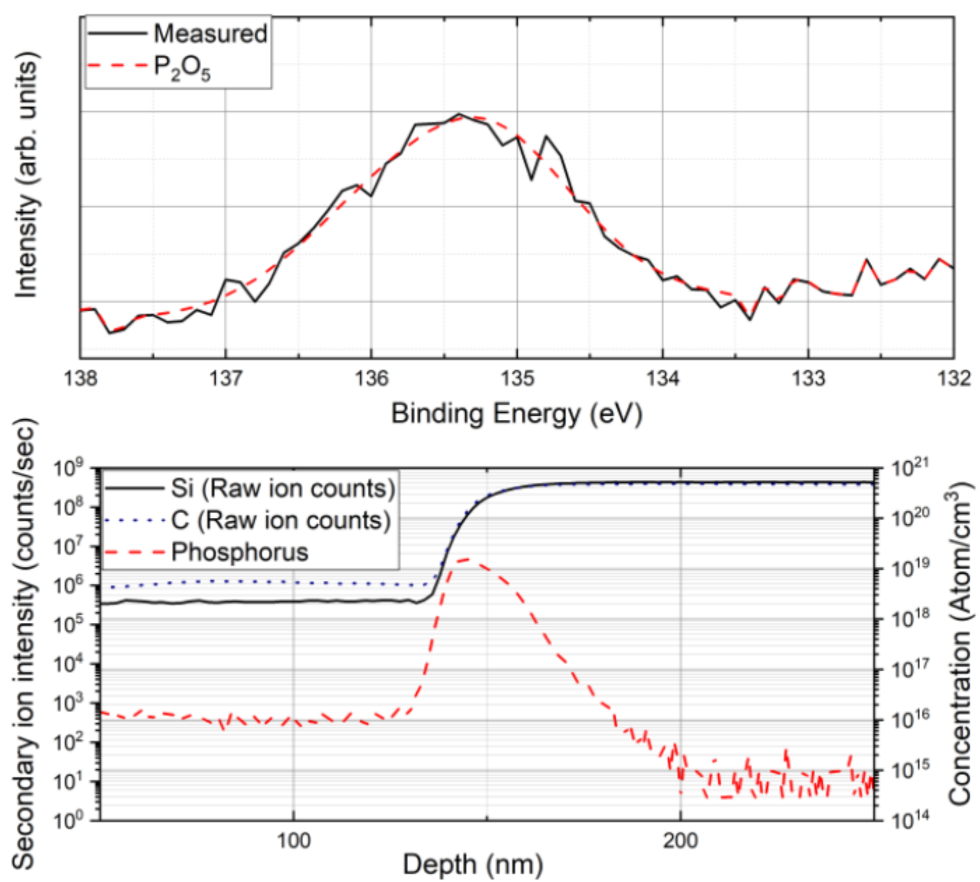


Figure 8-11: (top) XPS data for P 2p region showing a P2O5 peak for P2O5 treated Mo/SBD sample and (bottom) SIMS result for the P2O5 treated sample.

This surface chemistry study using XPS has shown that a phosphorous deposition (P_2O_5) treatment process in N_2 ambient reduces carbon enrichment at the interface. Furthermore, both XPS and SIMS results show that traces of phosphorus pentoxide are found after wet etching in HF and post-treatment metallisation. It is possible that the improved stoichiometry, and/or the residual P_2O_5 could be contributing to the SBDs improved electrical characteristics following metallisation.

8.3.3.2 Scanning Transmission Electron Microscopy (STEM)

In order to analyse the physical characteristic of Mo-semiconductor interface of the untreated and P_2O_5 treated samples, STEM analysis was performed. Additional samples were fabricated using the same fabrication procedure as used for XPS analysis, omitting the patterning of device structures. The STEM specimens were then prepared using the same preparation technique discussed in Section 5.2.2.1. Figure 8-12 shows the high-resolution STEM images of the interface between Mo and the semiconductor for untreated 4H-SiC Mo Schottky diode and Figure 8-13 shows the STEM images for P_2O_5 treated Mo Schottky diode. The atomic resolution can be seen at images with 1 nm resolution. As seen in Figure 8-13, Mo-4H-SiC interface is very sharp and uniform on the P_2O_5 treated Mo Schottky diode compared to the untreated sample where metal-semiconductor interface looks uneven and cloudy. Mo-silicide could not be seen on the metal semiconductor interface on any of the samples.

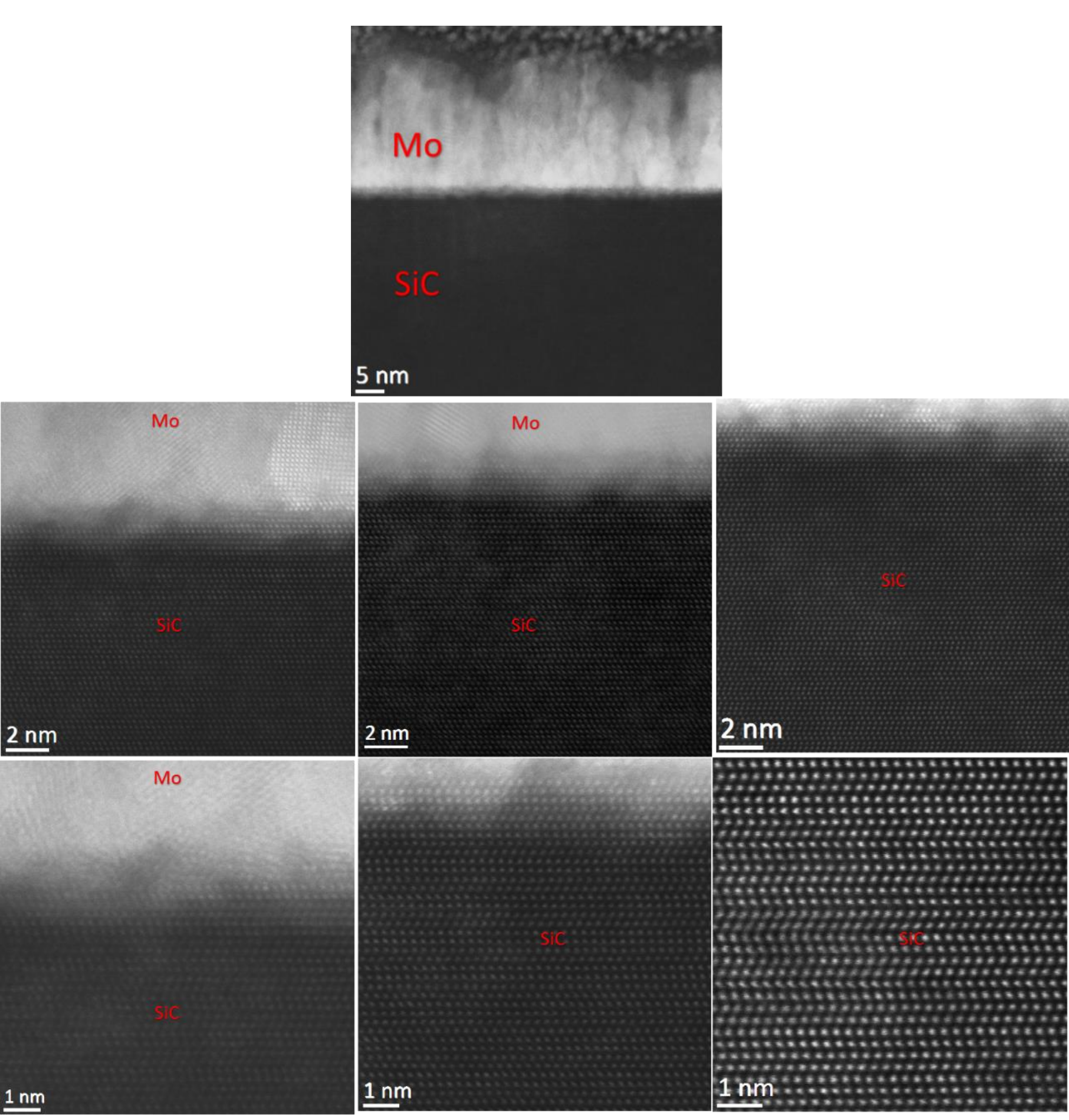


Figure 8-12: STEM images of metal-semiconductor interface for untreated (control sample) 4H-SiC Mo Schottky diode.

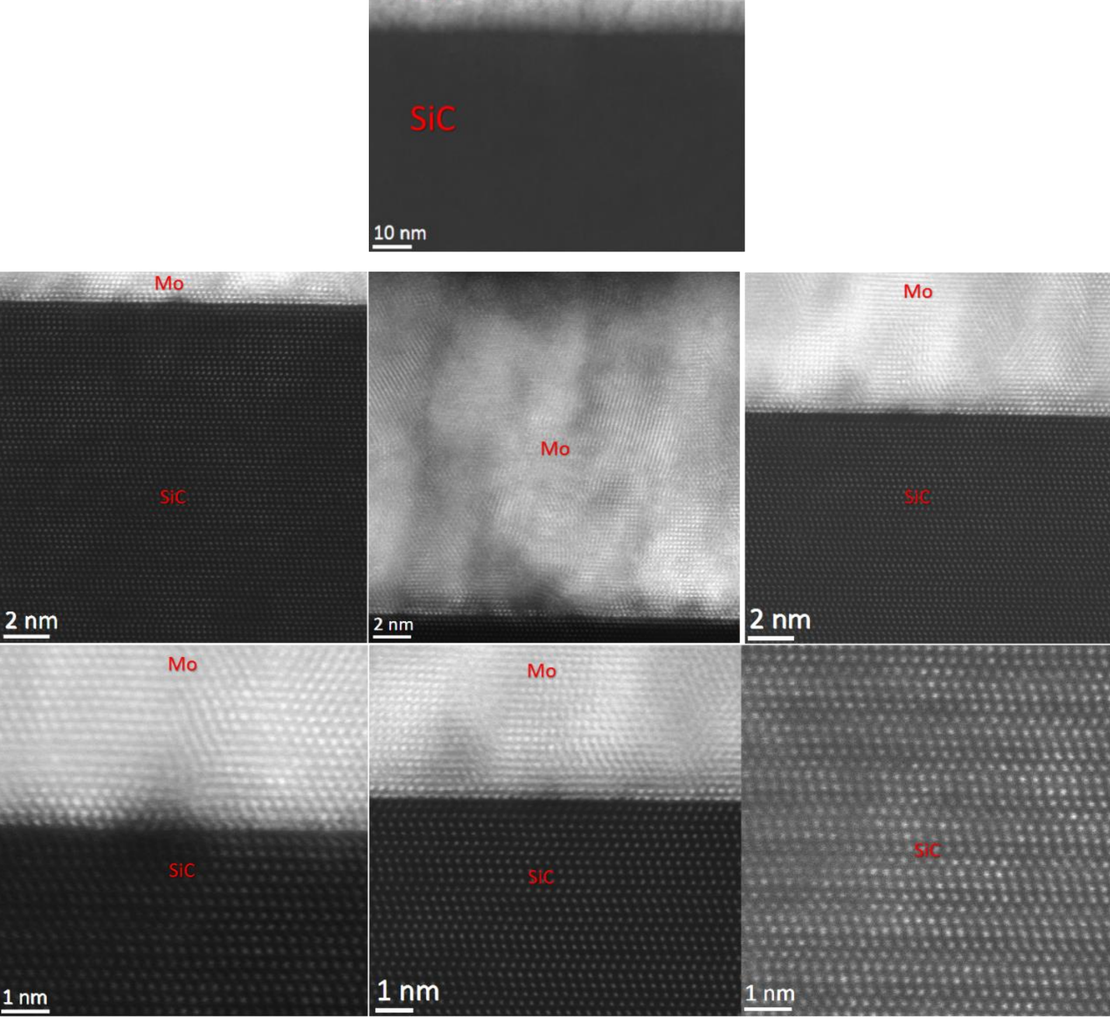


Figure 8-13: STEM images of metal-semiconductor interface for P2O5 treated 4H-SiC Mo Schottky diode.

8.3.3.3 Electron Energy Loss Spectroscopy (EELS)

Electron energy loss spectroscopy (EELS) uses the energy scattering of electrons that pass through a transparent sample to evaluate the content of the sample and generate images with distinctive contrast effects [167].

EELS technique was used in this study to determine the atomic structure and chemical properties of both samples, including: the type of atoms present at the interface, chemical state of atoms and the collective interactions of atoms with their neighbours. The results of EELS analysis of the Mo and 4H-SiC interface is presented in Figure 8-14 for an untreated Mo/SiC SBD sample and Figure 8-15 shows the EELS analysis results for a P_2O_5 treated sample. Spectra 1 and 2 in the in the STEM images for both Figures 8-14 and 8-15 are obtained from areas 1 and 2 shown with red boxes. The green box shows the region where the maps of Si and Mo was generated. RGB Overlay combines waveforms of different colours, for example (and in this case), it combines the red (Mo), green (Si) components in one display. The presence of very weak Si peak in waveform 1 of Figure 8-15 could either be due to the presence of Mo Silicide near the interface, or caused by beam broadening effect, meaning that the Si substrate was touched with the beam during the EELS analysis. As shown in the EELS spectrum, Mo was mapped around 2500 eV (energy-loss) and phosphorous can be mapped around 2100 eV. However, after point analyses, line scan and mapping were done on this sample, no phosphorous was seen in the EELS spectra of the interface for P_2O_5 treated Mo/SBDs. This result of EELS analysis is in contrast with the findings of XPS and

SIMS analysis where phosphorous could be seen at the metal-semiconductor interface. This could be due to the resolution limit of the EELS system.

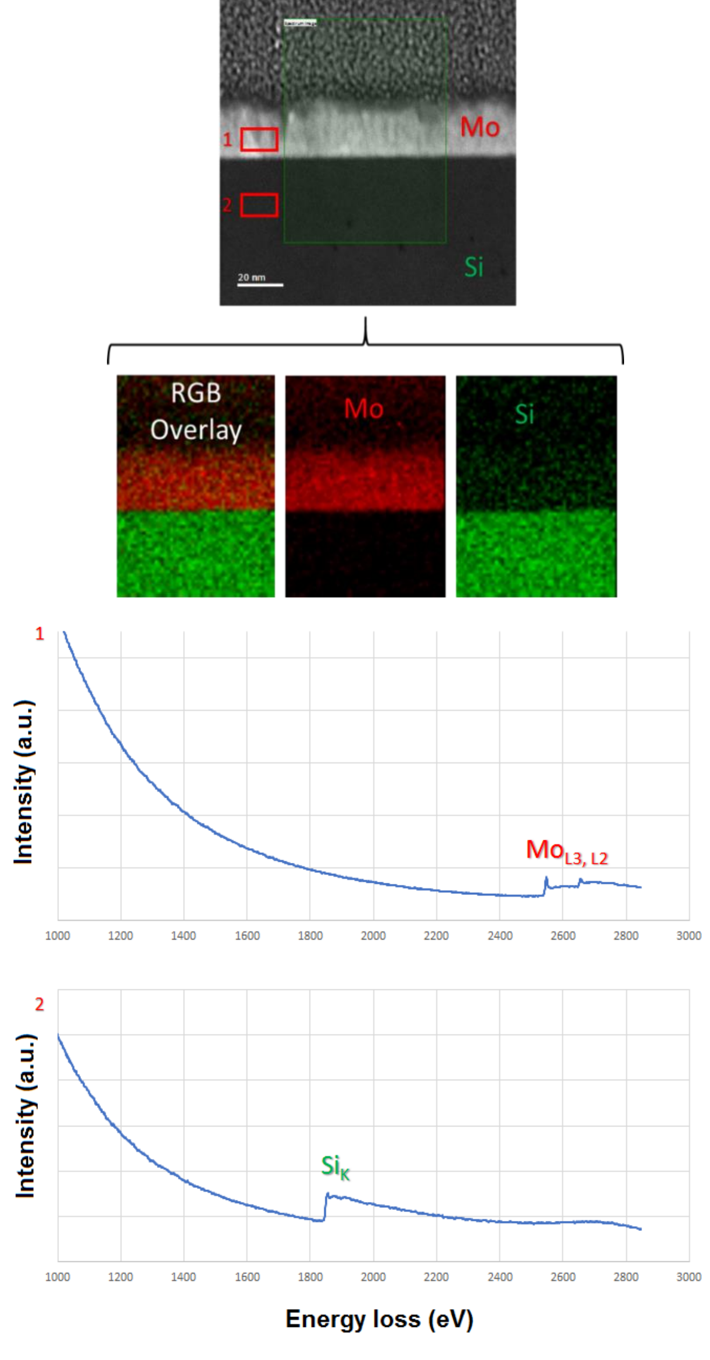


Figure 8-14: EELS results of untreated 4H-SiC Mo/SBD sample

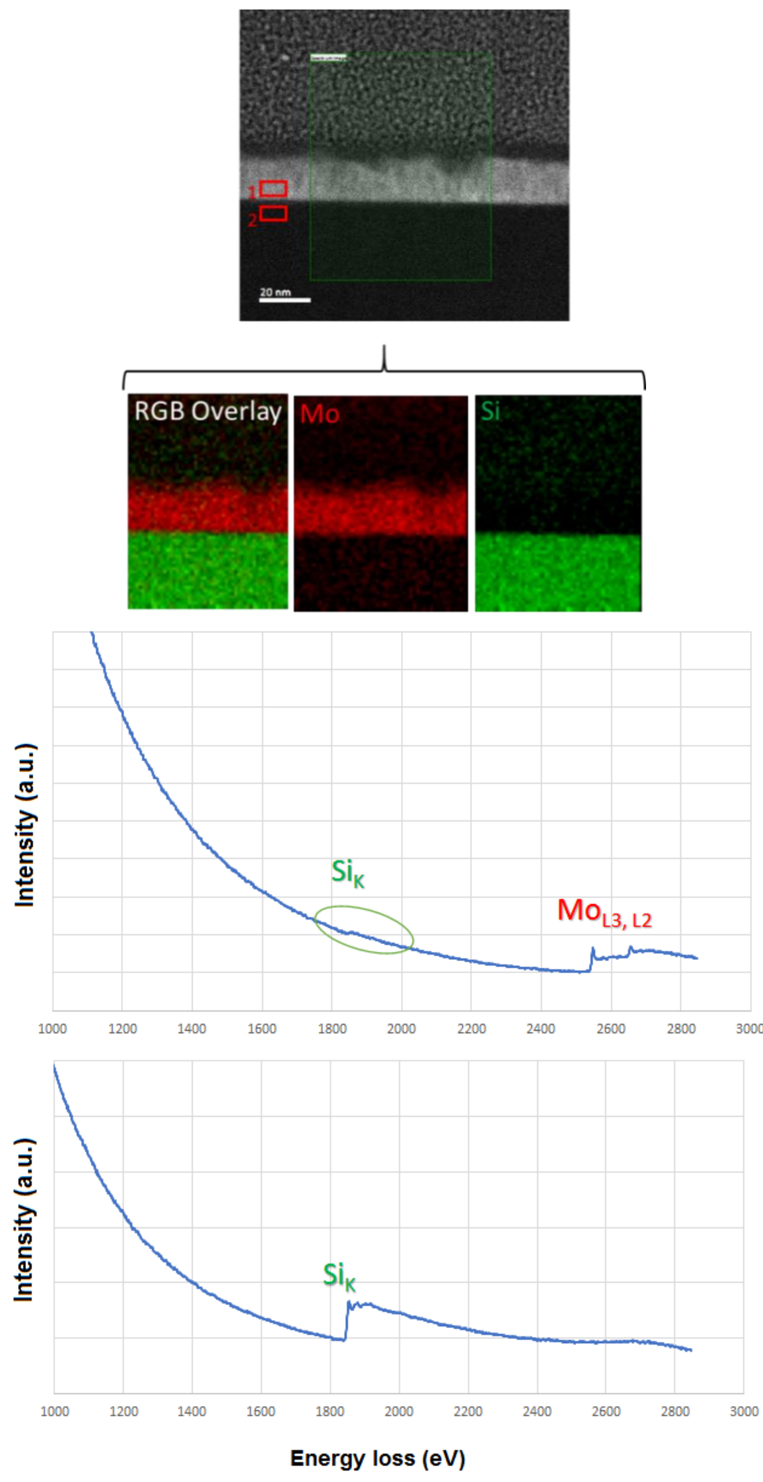


Figure 8-15: EELS results of P_2O_5 treated Mo/SBD sample.

Due to the resolution limit of the system it was not possible to confirm whether there was any Mo silicide at the interface. In another attempt, EELS analysis was performed on 3 regions on the untreated Mo/SBD sample with higher resolution to look for any Mo silicide at the interface. This is shown in Figure 8-16 (a) where area 1 looks at the Mo/SiC interface, area 2 at SiC and area 3 at Mo contact metal. The EELS spectra is illustrated in Figure 8-16 (b) which still could not confirm the presence of Mo Silicide at the interface. Therefore, it can be concluded that the apparent absence of a Mo-silicide is the result of the very high melting point of Mo. This explains why the surface treatments have little impact on the fabricated Ni or Ti/SiC-SBDs where the silicide consumes the treated semiconductor material.

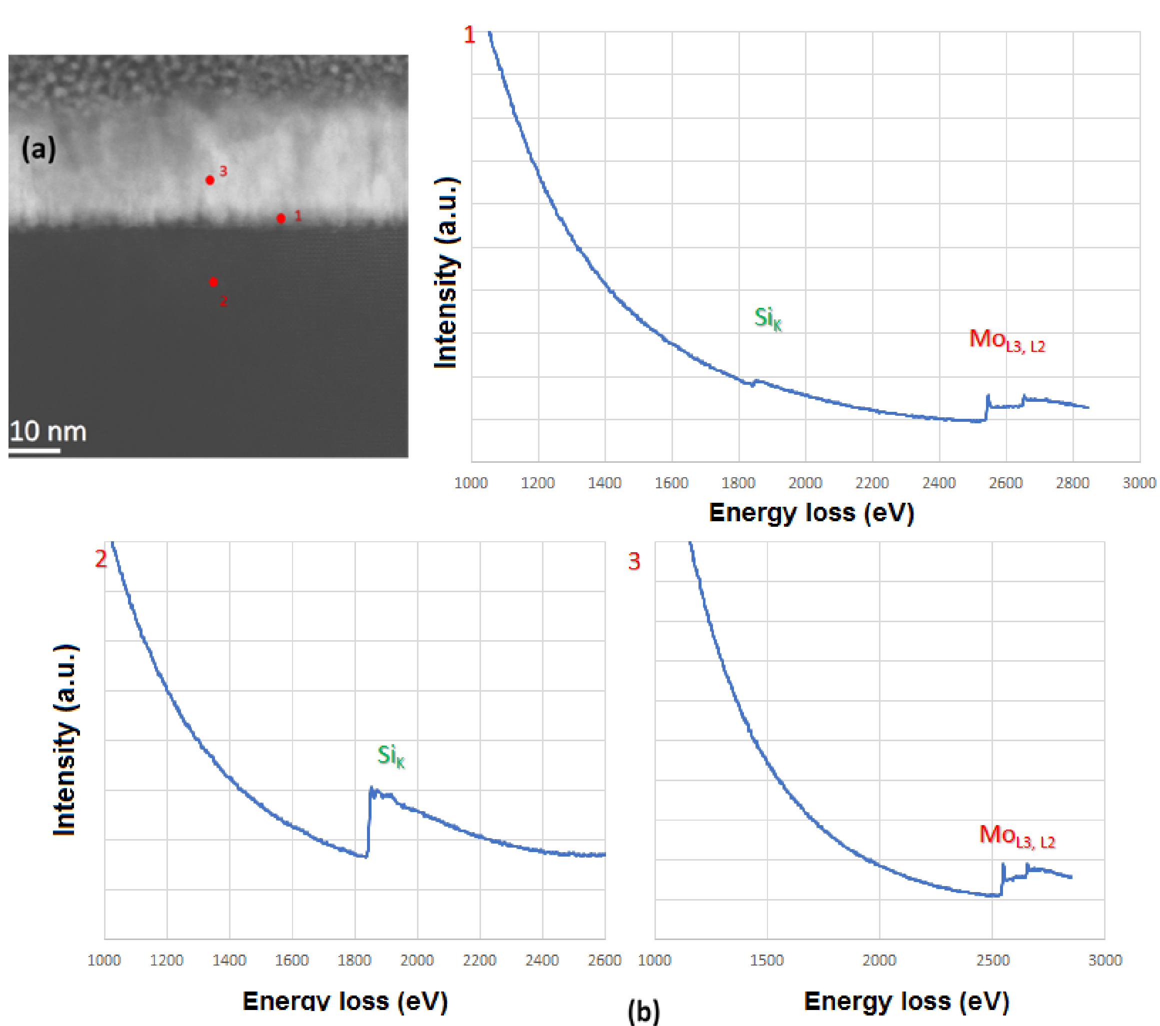


Figure 8-16: EELS analysis of untreated Mo/SBDs at 3 different regions

8.3.3.4 Energy-Dispersive X-Ray Spectroscopy (EDX)

EDX analysis was performed on the control sample and P_2O_5 treated sample shown in Figure 8-17 and Figure 8-18 respectively. Looking at the EDX results, the atomic percentage of C (shown in tables in Figure 17 and Figure 8-18) is quite high

compared to what was seen in XPS analysis of the interface. When studying a SiC interface using XPS, you would expect the Si-C peak in the Si spectrum and the C-Si peak in the C spectrum to have the same atomic percentage. In practice this is not the case, indicating the surface is enriched in one element or the other. In the XPS results presented earlier, the stoichiometry correlated with the electrical measurements for all samples: confirming that the closer you get to 50:50 ratio, the better the interfaces and hence the superior the device performance. A larger SiC peak was seen in the C spectrum than in the Si spectrum in XPS analysis. Looking at the atomic percentage of C in EDX results for both untreated and treat samples, there is much more carbon which correlates with the XPS result. As expected, if you oxidise SiC, the carbon is left over. The leading explanation is that, carbon is missing from Si-C bonds, implying it is in clusters at the interface. XPS has a higher detection limit (especially for light elements, C, N and O) compared to EDX and it is found that the reliability of the latter for low atomic number elements is generally low. This is due to various parameters such as absorption, fluorescence, collection solid angle, etc. Hence, XPS is a favourable technique for quantification of very low atomic number elements.

Regarding carbon ratios, in microscopy, there is a lot of uncertainties while measuring the contents of C and O on everything. In many instruments there appears to be an unavoidable contamination due to beam effects and oxidation. Hence, typically C and O peaks are disregarded in EDX due to unavoidable organic contaminations.

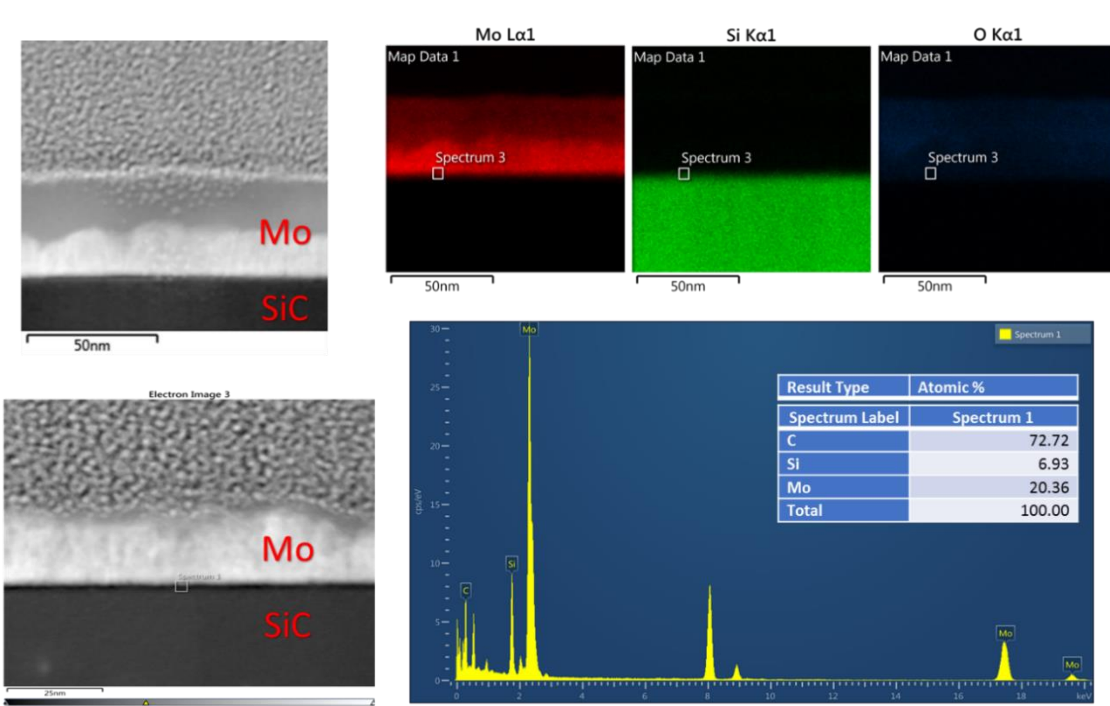


Figure 8-17: : EDX results for as deposited Mo/SiC Schottky diode sample.

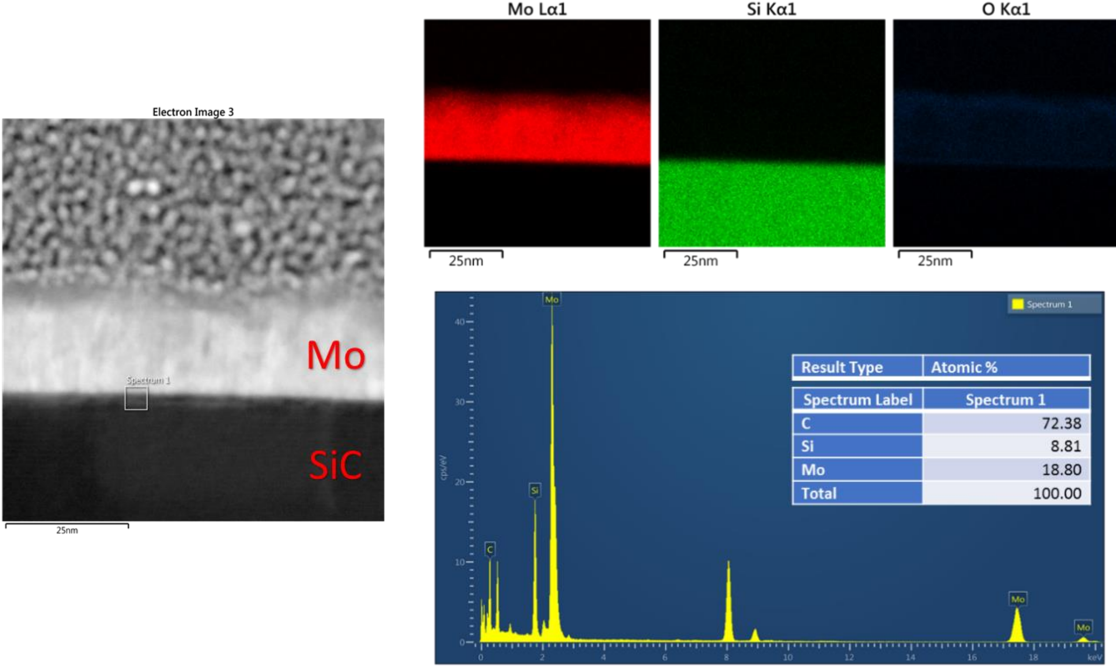


Figure 8-18: EDX results for results for P_2O_5 treated Mo/SiC Schottky diode sample.

8.4 Summary

The investigation into the impact of surface passivation techniques was carried out by fabricating SBDs on SiC surfaces that had been treated with different surface passivation techniques. It was shown that the P_2O_5 treated Mo/SiC diode retained a barrier height equivalent to that of titanium, but with a leakage current lower than any Ni diode, seemingly combining the benefits of both a low- and high-SBH metal. Furthermore, Mo diodes formed on a surface after P_2O_5 treatment were the only diodes to undergo any significant leakage current reduction after any of the pre-treatments. They displayed exceptionally low leakage (4.44×10^{-5} A/cm^2 at 19°C). Even when tested at 300°C, a leakage of 7.26×10^{-4} A/cm^2 is lower than any of the other devices at room temperature given a low barrier height (1.27 eV). Hence, it was shown that pre-treatments have the potential to overcome the major weakness of using low SBH metals such as Mo. Electrical characterisation results showed that a P_2O_5 treatment improved the homogeneity of the diodes, with the ideality factor reducing to 1.05. Furthermore, the range of all P_2O_5 treated Schottky characteristics over the batch improved. Moreover, X-ray photoelectron spectroscopy characterisation showed that the stoichiometry of the SiC underneath the contact was enhanced using P_2O_5 treatment, with the Si:C ratio increasing to 0.99. This surface chemistry study using XPS has shown that a phosphorous deposition (P_2O_5) treatment process in N_2 ambient reduces carbon enrichment at the interface. Moreover, both XPS and SIMS results on P_2O_5 treated Mo-SBD show that traces of phosphorus pentoxide were found after wet etching

the samples in HF and post-treatment metallisation (Mo). It is possible that the improved stoichiometry, and/or the residual P_2O_5 could be contributing to the Mo-SBDs improved electrical characteristics following metallisation.

STEM analysis was also performed on Mo-4H-SiC interface for both untreated Mo/SBDs and P_2O_5 treated Mo Schottky diode. It was found that the Mo-4H-SiC interface is very sharp and uniform on the P_2O_5 treated Mo Schottky diode compared to the untreated sample where metal-semiconductor interface looks uneven and cloudy. Mo-silicide could not be seen on the metal semiconductor interface on any of the samples. This was also confirmed by performing EELS analysis on the same samples. Therefore, it can be concluded that the apparent absence of a Mo-silicide is the result of the very high melting point of Mo. This explains why the surface treatments have little impact on the fabricated Ni or Ti/SiC-SBDs where the silicide consumes the treated semiconductor material.

EDX analysis was also performed on Mo-4H-SiC SBDs. It was found that the atomic percentage of C is quite high compared to what was seen in XPS analysis of the interface. Looking at the atomic percentage of C in EDX results for both untreated and treat samples, there is much more carbon compared to what was seen in XPS results. This could be because a lot of carbon is missing from Si-C bonds, suggesting it is in clusters at the interface. XPS analysis has higher detection limit compared to EDX and it is found that the reliability of the latter for low atomic number elements is generally low due to various parameters such as absorption, fluorescence, collection solid angle,

etc. Hence, it was found that XPS is a favourable technique for quantification of very low atomic number elements.

In summary, the electrical and physical characteristics of P_2O_5 treated Mo/SBDs fabricated in this Chapter are superior to what is reported in the literature and other SBDs fabricated in this work. For example, Infineon reported the characteristics of their new Mo/SiC Schottky diode in [198], but, the leakage current of the diode's fabricated in this research is significantly improved in comparison to Infineon's while the Schottky barrier height is stable and exceptionally low offering improved electrical performance. In high voltage applications such as modular multi-level converters where the power switching devices are connected in series, low leakage characteristic of a power device is desirable as this determines the distribution of the electro-thermal stress between the series connected devices. The device with lower leakage current, shares less voltage during off-state and is less stressed. However, if the leakage current is significantly small and more stable, this results in a stable voltage sharing during the off-state.

Chapter 9 Conclusion and Further Work

In this final Chapter, the conclusions that have arisen from this research is presented. Hence, upon drawing the conclusions, several key areas that could benefit from further work have been outlined with the intention to further enhance the technological capability of high voltage 4H-SiC power electronic devices and to provide a pathway for further studies.

9.1 Conclusion

The overall aim of this thesis was to enhance the performance of 4H-SiC power diodes for high voltage applications with particular focus on improving the performance of 4H-SiC SBDs using a novel metal-semiconductor interface treatment and 4H-SiC PiN diodes using high temperature processing techniques. The findings of the study on 4H-SiC PiN diodes could be potentially used for other 4H-SiC bipolar devices such as IGBTs, BJTs and thyristors. And the developed novel metal-semiconductor interface

treatment on 4H-SiC SBDs can be potentially employed for MOS interface improvements.

As discussed in earlier chapters, Si power devices are at their practical limit due to increasing demand for high voltage, high power devices. 4H-SiC is the most promising candidate for high voltage applications. However, despite the advancements in the field of 4H-SiC epitaxial growth, the existence of defects in the material can considerably reduce the electrical performance of the power diodes, such as low carrier lifetimes and increased reverse leakage current. Hence, another key focus of this research was understanding the impact of a commonly found surface morphological defect, the triangular defect, on the performance of the fabricated 4H-SiC diodes.

The research on the impact of triangular defects in this thesis shows that the existence of these macroscopic defects severely limits the active area of the fabricated PiN diodes and creates a short path through the drift region, which ultimately increases the leakage current almost 10^8 times higher than the devices fabricated on the areas with no visible defects. This investigation was performed by intentionally fabricating PiN diode on-and off-defects on three wafers with 35 μm (PiN1), 30 μm (PiN2), and 100 μm (PiN3) epilayer thicknesses and was presented in Chapter 6. The defects were successfully characterised on all three substrates before device fabrication using methods including AFM, SEM, Photoluminescence and HRTEM. HRTEM, SEM and PL analysis were used to understand the formation mechanism of the triangular defect. SEM analysis revealed that triangular defects originate from the downfall of a foreign particle at the initial stage of the epitaxial growth. HRTEM and Photoluminescence

techniques proved that the triangular defects are actually a thick layer of 3C-SiC which is sandwiched between two 4H-SiC layers on top and bottom. Other complex structures were also observed on the triangular defect using HRTEM called DPBs which resulted in a leakage path through the drift region of the devices and therefore confirming the cause of increased leakage currents seen in all samples fabricated on-defect.

In addition to the above, it was shown for the first time the impact of triangular defects on switching characteristics of SiC PiN diodes fabricated on- and off-defects. The switching characteristics of the devices on- and off-defects on PiN1 and PiN2 revealed that the amount of stored charge in the devices on-defect is not decreased, suggesting that either there are not many extra stacking faults around the defect, or that their impact on triangular defects on recombination rate is minor. However, this behaviour was not seen for PiN3, where the switching behaviour of devices on PiN3 revealed a 60% reduction in the amount of charge stored in the devices on-defect compared to the devices off-defect. This is due to the fact that as triangular defects on PiN3 on-defect diodes propagate through the complete width of the drift region, carriers that enter the drift region leak out from the device rather than forming the charge storage region and creating conductivity modulation. Hence, the likelihood of electrons and holes getting recombined in the drift region increases by increasing the drift region thickness, resulting in smaller charge getting formed in the charge storage region. Hence, the on-state resistance of the device on-defect on PiN3 increases. As a result, a significantly lower forward current passes through the device compared to the device off-defect.

The developed PiN diode fabrication process discussed in Chapter 6 was used for the fabrication of the PiN diodes in Chapter 7 with the aim to improve the forward characteristics by enhancing the carrier lifetime. Three samples with 35 μm epilayer thickness were fabricated. This enabled a comparison of control sample devices against devices that had undergone thermal oxidation and subsequent annealing process at 1450°C and 1550°C for 1 hour. The analysis of the I-V characteristics of the first generation control sample diodes revealed that the poor I-V characteristics in the low-level injection conditions was due to the existence of conduction paths in parallel with the pn junction at the mesa sidewall exists. This was resolved by increasing the thickness of the passivation TEOS SiO_2 layer to higher than the mesa etch depth and fully coating the mesa sidewalls. The small-area diodes on the control sample showed a forward voltage drop of around 3.12 V at 100 A/cm^2 and 25°C with a corresponding differential on-resistance of approximately 2.07 mΩ-cm^2. The samples that had undergone the thermal oxidation process were found to improve on this, with the 1450°C oxidised/annealed sample having a forward voltage drop of 3.09 V and $R_{on,diff}$ of around 2.04 mΩ-cm^2 at 100 A/cm^2 and 25°C compared to forward voltage drop of 3.06 V and $R_{on,diff}$ of 1.9 mΩ-cm^2 for the 1550°C oxidised PiN diodes.

The transient characteristics of the fabricated PiN diodes on all three samples were analysed and compared under clamped inductive switching conditions. From the reverse recovery characteristics, an increase of 44% of the reverse recovery current was seen for the 1550°C annealed sample compared to the control sample. This is due to the increase of excessive minority carriers in the drift region. The 1450°C oxidised sample

also exhibited a 14% increase of the reverse recovery current compared to the untreated sample. Moreover, from the reverse recovery characteristics it was found that the carrier lifetime had increased from 400 ns in the control sample to 440 ns for the 1450˚C thermally oxidised/annealed sample and 542 ns for the 1550˚C thermally oxidised/annealed sample. This shows an increase of around 40% in the carrier lifetime. Therefore, it can be concluded that the developed thermal oxidation and successive Ar annealing process at 1550°C is highly effective in enhancing the carrier lifetime. However, it is important to note that, to some extent, the quality of the starting material has an impact on the electrical performance of the fabricated device. Moreover, it was shown that increasing the oxidation temperature reduces the overall carrier lifetime enhancement process time and further repairs the lifetime-killing defects in the material. The developed high temperature oxidation and subsequent annealing process is a cost effective and time saving process which is beneficial for commercial device fabrication processes

In addition, it was shown that the peak of the reverse recovery current of 4H-SiC PiN diodes increase with temperature due to the positive temperature coefficient of the minority carrier lifetime which results in higher reverse recovery charge during turn-off. As expected, the reverse charge of the PiN diode was shown to increase with increasing the forward current, since the stored charge during the on-state of the device increases with the forward current. The reverse recovery characteristics were also found to become snappier as the supply voltage increases. This is because increasing the supply voltage increases the extent in which the depletion width spreads into the

PiN diode, consequently resulting in faster charge extraction and recombination. As anticipated, the reverse recovery characteristics of the PiN diode becomes snappier by increasing the switching rate. The peak reverse recovery current increases with increasing the switching rate and the recovery current has a higher *dI/dt*.

The aim of the study in Chapter 8 was to further enhance the performance of SBDs by investigating the impact of various surface passivation treatments on both the 4H-SiC surface, and the metal-semiconductor interface prior to the device fabrication. Moreover, the findings of this Chapter have the potential to be employed for MOS interface improvements. To do so, SBDs were fabricated on treated SiC surfaces, so that metal-semiconductor junctions could be used to evaluate the quality of this surface, using a range of metals including Mo, Ni, and Ti. Various surface passivation treatments were performed on 4H-SiC surface, including the growth then removal of oxide layers formed in O_2, via direct N_2O growth and a novel surface passivation process using phosphorus pentoxide (P_2O_5) deposition. SBDs developed after the removal of these passivating layers were compared to those on untreated (control) surfaces and characterised. The on-state and reverse-leakage characteristics for the fabricated SBDs of each type were compared, as well as the barrier height and ideality factor. Almost all the diodes had very low values of ideality factor, confirming that thermionic emission is the dominant current transport mechanism. Without any surface treatment, the control samples had a relatively wide spread of SBH and ideality factor. It was also found that the O_2 oxidation treatment had degraded the electrical characteristics of all

diodes, resulting in a higher average SBH. In contrast, the SBH was significantly lowered by using the N_2O and P_2O_5 surface treatments.

The most significant outcome of this work was the performance of P_2O_5 treated Mo/SiC Schottky diodes. These retained a barrier height equivalent to that of titanium, but with a leakage current lower than any Ni diode, seemingly combining the benefits of both a low- and high-SBH metal. Moreover, the P_2O_5 treated Mo/SiC Schottky diodes were the only diodes that exhibited significant leakage current reduction compared to any of the other pre-treatments (4.44×10^{-5} A/cm^2). Even when tested at 300°C, a leakage of 7.26×10^{-4} A/cm^2 is lower than any of the other devices at room temperature given a low barrier height (1.27 eV). This is contrary to the expectations that lower Schottky barrier height and hence lower turn-on voltage will result in an increase leakage current, as happened for Infineon devices when they moved from Ti to Mo [198, 208]. Hence, it was shown that pre-treatments have the potential to overcome the major weakness of using low SBH metals such as Mo. Electrical characterisation results showed that a P_2O_5 treatment improved the homogeneity of the diodes, with the ideality factor reducing to 1.05. Furthermore, the range of all P_2O_5 treated Schottky characteristics over the batch improved.

Moreover, by performing XPS characterisation technique on all Mo-based samples it was found that the stoichiometry of the SiC underneath the contact was enhanced using P_2O_5 treatment, with the Si:C ratio increasing to 0.99. This surface chemistry study using XPS has shown that P_2O_5 deposition process in N_2 ambient reduces carbon enrichment at the interface. Moreover, both XPS and SIMS results

showed that traces of phosphorus pentoxide were found after wet etching the P_2O_5 treated samples in HF and post-treatment metallisation (Mo). Therefore, it is possible that the improved electrical characteristics of Mo-SBDs following metallisation could be due to enhanced stoichiometry, and/or the residual P_2O_5.

Mo-4H-SiC interface for both untreated Mo/SBDs and P_2O_5 treated Mo Schottky diodes were characterised using STEM analysis. It was found that the Mo-4H-SiC interface on the P_2O_5 treated sample was very sharp and uniform as opposed to the control sample where the Mo/SiC interface looked uneven and cloudy. Mo-silicide could not be seen on the metal-semiconductor interface on any of the samples using STEM and EELS analysis as a result of the very high melting point of Mo. This explains why the surface treatments have little impact on the fabricated Ni or Ti/SiC-SBDs where the silicide consumes the treated semiconductor material. It was also found that XPS is a favourable technique for quantification of very low atomic number elements over EDX analysis due to its higher detection limit compared to EDX.

In summary, it was shown that the electrical and physical characteristics of P_2O_5 treated Mo/SBDs fabricated in this thesis are superior to what is reported in the literature [198, 208] and other 4H-SiC SBDs fabricated in this thesis. For instance, the leakage current of the diode's fabricated in this research is significantly improved in comparison to Infineon's [198], while the Schottky barrier height is stable and exceptionally low offering improved electrical performance. In high voltage applications such as modular multi-level converters where the power switching devices are connected in series, low leakage characteristic of a power device is desirable as this

determines the distribution of the electro-thermal stress between the series connected devices. The device with lower leakage current, shares less voltage during off-state and is less stressed. However, if the leakage current is significantly small and more stable, this results in a stable voltage sharing during the off-state.

9.2 Suggestions for Future Work

In this Section, areas of future work have been outlined. One of the key areas that would benefit from further work is reverse breakdown simulations for both 4H-SiC Schottky diode and PiN diodes using Silvaco Athena software in order to design and develop a simple yet high performance edge terminations structure for blocking high reverse voltages. This would require experimentation with implantation dose to achieve the desired breakdown voltages.

Another area that would benefit from further development is in the device fabrication processes, such as formation of ohmic contacts and Schottky contacts. In the fabrication processes presented in this thesis, the RTA furnace was dependant on the manual control of the furnace. This resulted in variable ramp rates and temperature overshoot and undershoot and could have an impact on the physical and electrical characteristics of the fabricated metal contacts. This area would benefit from having a more accurate control of the RTA furnace to obtain more reproducible results.

It was shown in Chapter 7 that the combined high temperature and Ar annealing process was highly effective in increasing the carrier lifetime in the

fabricated 4H-SiC PiN diodes and enhancing their on-state characteristics. However, this study would benefit from studying the oxidation rate at various oxidation temperatures to understand how much of the 4H-SiC is consumed during oxidation treatment. This would allow high temperature process durations to increase and further enhance the carrier lifetime. This is especially crucial for 4H-SiC wafers with thicker drift region than 35 μm, as the risk of all the 4H-SiC p-type layer being consumed increases with increasing the oxidation duration and oxidation rate to completely repair the carbon vacancy defects in the bulk.

In the study in Chapter 8, it was shown that the electrical and physical characteristics of P_2O_5 treated Mo/SBDs fabricated are superior to what is reported in the literature. Various physical characterisation techniques revealed that Mo-silicide could not be seen at the metal-semiconductor interface of any of the samples. However, traces of phosphorus pentoxide were found on after wet etching the P_2O_5 treated samples and post-treatment metallisation (Mo) which could have contributed to these superior characteristics and the enhanced stoichiometry. A suggestion for further investigation in this subject would be to use a range of metal contacts such as platinum (Pt), niobium (Nb) and tantalum (Ta) with different melting points to fabricate P_2O_5 treated 4H-SiC SBDs. The melting point of Pt is lower than Mo, but higher than Ni, which is interesting to see if the formation of Pt-silicide would have an impact on the resulting P_2O_5 treated 4H-SiC SBDs. Moreover, the melting point and presumably diffusion behaviour of Nb is similar to Mo, but it has a different chemistry compared to Mo. Ta has similar chemistry to Nb, but higher melting point that Pt, Nb and Mo.

Therefore, 4H-SiC surface can be treated using the passivation techniques discussed in Chapter 8 and Schottky diodes can be formed on the treated surface. The contact annealing temperatures, durations and the resulting SBDs can be compared and benchmarked.

Appendix A

Alternative SiC Schottky Devices

Both Rohm [113] and Cree (Wolfspeed, now Cree owned) [210] have explored the use of SiC trench JBS structures where the p-type implant surrounds a trench filled with the anode metal, as seen in Figure A-1. This drops the electric field at the Schottky surface even further and decreases the device leakage current. The trench JBS structure has a lower leakage current (by 1 order of magnitude) at rated voltage compared to a typical JBS structure [210]. The space-charge areas spreading from the pn junctions at the bottom of the trench play a significant role and can increase the on-resistance if not optimised.

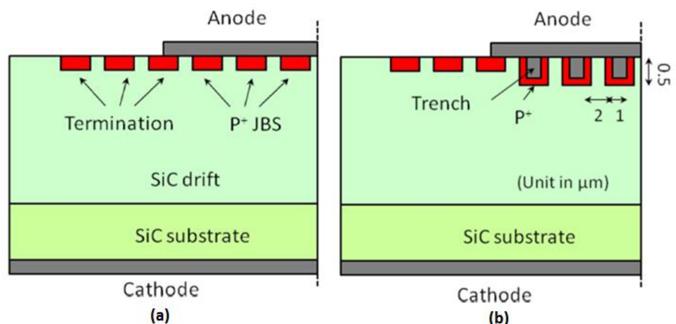


Figure A-1: (a) Planar JBS structure, (b) Trench JBS structure used in simulations [118]

Figure A-2 shows the schematic cross section of SiC trench structure Schotttky diodes by Rohm [211]. In 2014, Rohm reported that their 1200V ultra-low VF trench SBDs with lower barrier height (while keeping the same leakage current) have about 0.3V smaller V_F compared to conventional SBDs. They also showed that trench structure enables the reduction of the on-resistance by about 50% throughout temperature range of 25°C to 150°C [211].

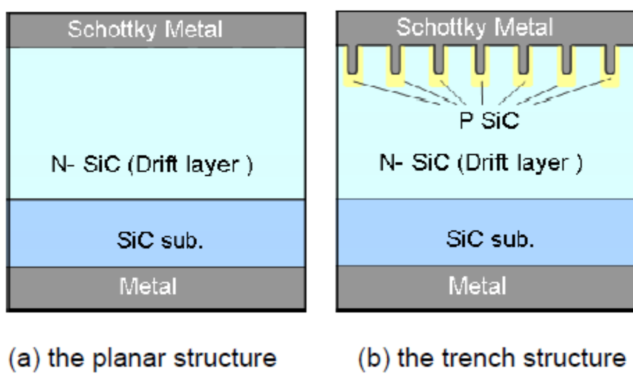


Figure A-2: Schematic cross section of the planar and trench structure Schottky diodes [119]

Even beyond this, several other alternative device structures exist, including: 4H-SiC Dual-Metal-Trench (DMT) Schottky Pinch-Rectifier [212] involving a trench with different metals on the surface, than that on the side and bottom of the trench, Trench MOS barrier Schottky diodes [213]; and heterojunction diodes, that use Si or Ge as a contact [214, 215].

A pinch rectifier uses a high barrier region to pinch-off or electrically shield a low barrier region. Numerous pinch-rectifier device structures have been employed and established in Si. The work in [212] reports on the fabricated 4H-SiC pinch-rectifiers

using a small/large barrier height (Ti/Ni). The Ti/Ni DMT device structure is shown in Figure A-3, where w_m is the mesa width, w_t is the trench width, t_m is the mesa thickness, and t_{Epi} is the epilayer thickness [212]. As reported in [212] at a reverse bias of 300 V, the reverse leakage current of the SiC DMT device is 75 times lower compared to a planar device, but the forward bias characteristics stay similar to those of a planar device. The DMT structure is particularly intended to facilitate simple fabrication in SiC. Therefore, it is a favourable technology for enhancing the performance of power SiC Schottky rectifiers.

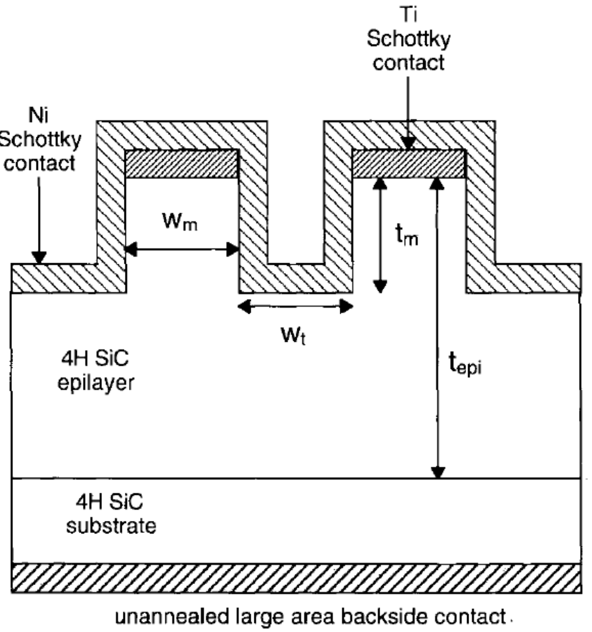


Figure A-3: Device structure of Ti/Ni dual-metal-trench pinch rectifier [120]

To realise good reverse blocking while sustaining a Schottky-like forward conduction level, the trench MOS barrier Schottky (TMBS) rectifier has been proposed

and developed in silicon [213, 216]. However, regardless of these structural benefits, the 4H-SiC TMBS rectifiers experience a great risk of premature breakdown due to their poor oxide quality [26, 217, 218]. Numerous studies have been reported on the enhancement of the forward and reverse characteristics of the 4H-SiC TMBS rectifier on counter doped TMBS or dual-material (DM) TMBS rectifiers [219, 220]. The trench MOS barrier Schottky diode structure shown in Figure A-4 has a high doping concentration at the trench sidewall [213]. This high doping concentration improves both the reverse blocking and forward characteristics of the structure.

The enhanced sidewall layer Trench (ESL–TMBS) rectifier has a 7.4% lower forward voltage drop, a 24% higher breakdown voltage and an oxide shielding effect as it mitigates the electric field crowding at the trench corner. However, this structure has a reverse leakage current that is approximately three times higher than that of a conventional TMBS rectifier owing to the reduction in energy barrier height. This problem is solved when ESL is used partially, since its use provides a reverse leakage current that is comparable to that of a conventional TMBS rectifier. Thus, the forward voltage drop and breakdown voltage improve without any loss in static and dynamic characteristics in the ESL–TMBS rectifier compared with the performance of a conventional TMBS rectifier.

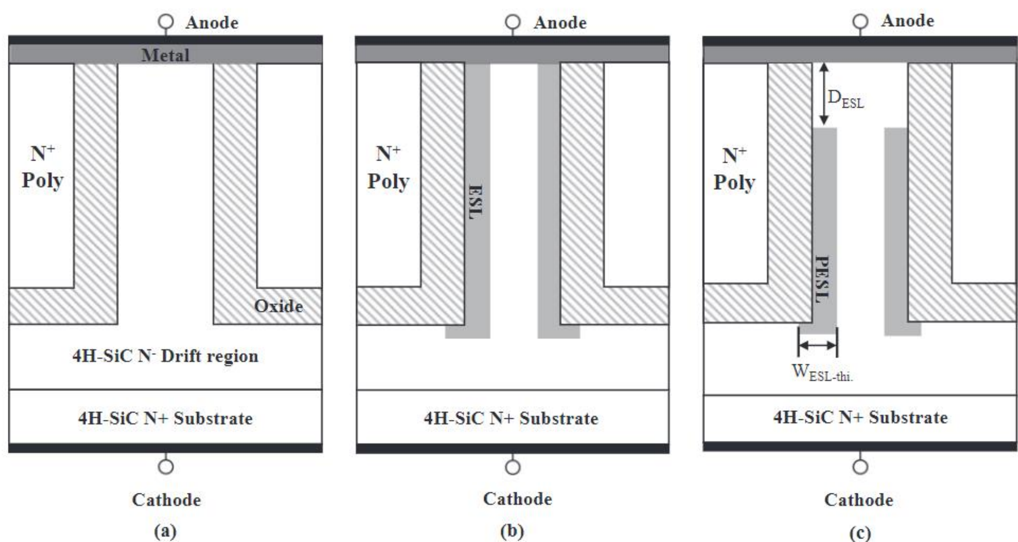


Figure A-4: Cross sections of the (a) conventional 4H-SiC TMBS, (b) ESL–TMBS, and (c) partial–ESL–TMBS rectifiers [121]

The super junction (SJ) principle is expected in SiC power devices to improve its trade-off between the breakdown voltage (BV) and specific on-resistance ($R_{ON,SP}$). A SiC SJ structure has been recently demonstrated with the high energy implantation method [221]. Figure A-5 shows the SiC super junction (SJ) Schottky diode structure reported by Zhong et al. in [222] as the first functional SiC SJ Schottky diode which substantially improved the trade-off between the breakdown voltage and on-resistance in SiC power devices.

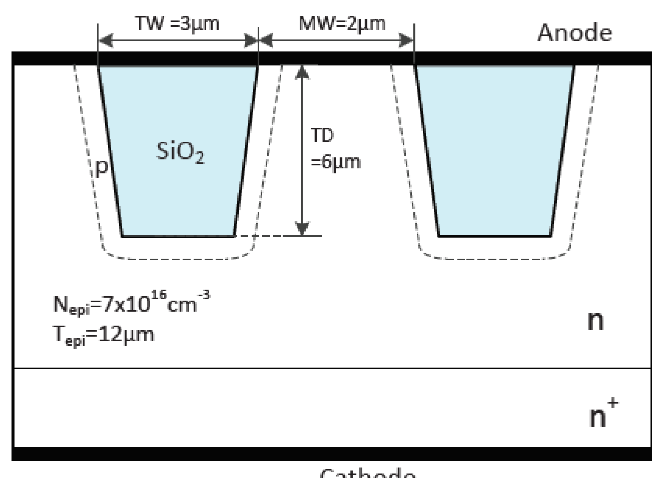


Figure A-5: SiC SJ Schottky diode cell structure and basic dimension information [129]

They used a trench-etching-and-sidewall implant method to develop this device as shown in Figure A-6. The trench sidewall is designed to have an 86° angle to facilitate tilted ion implantation and trench refill process. The measured blocking voltage was 1350V which is 95% of simulated blocking voltage for the ideally-charge balanced SJ structure. The measured device specific on resistance was 0.92mΩ.cm^2. The SJ drift region specific on-resistance as low as 0.32mΩ.cm^2 obtained.

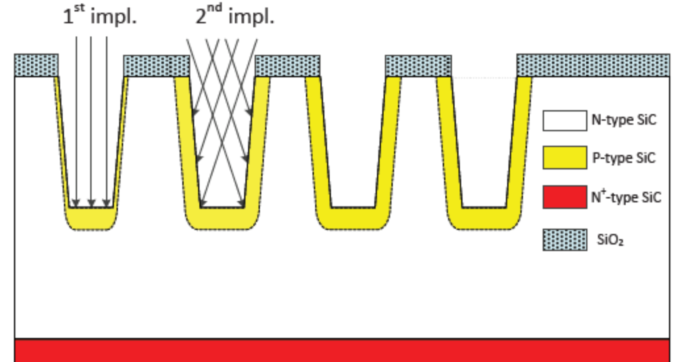


Figure A-6: Key process step of the SiC SJ Schottky diode [129]

Appendix B

Derivation of Capacitance-Voltage Equations

According to the theory of the C-V analysis [123, 223], for an abrupt junction, a linear relationship exists between an applied voltage and the inverse square of the capacitance. This relationship is derived here.

The capacitance-voltage method is dependent on the fact that the applied voltage affects the width of a reverse-biased space-charge region (scr) of a semiconductor junction device. The reliance of scr width on voltage is the basis of C–V measurement technique. The C–V characterisation technique has been used with Schottky barrier diodes, p-n junctions, MOS capacitors, MOSFETs, and metal-air-semiconductor structures [123]. Consider a Schottky barrier diode of a n-type semiconductor material with doping density of N_D.

A space-charge region of width W is created by applying a DC bias voltage V_A. The equation below defines the differential or small signal capacitance where Q_m and Q_s represent the charge density in the metal and semiconductor sides of the diode respectively:

$$C = -\frac{dQ_m}{dV_A} = -\frac{dQ_s}{dV_A} \qquad \text{B-1}$$

The negative sign in Equation B-1 is due to the presence of negative charge in the semiconductor scr (negatively charged ionized acceptors) for positive voltage on the metal for reverse bias [123]. The capacitance is found by means of superimposing an AC voltage with a small-amplitude of v on the DC voltage V_A. The frequency of the aforementioned ac voltage frequency normally in the range of 10 kHz to 1 MHz with 10 to 20 mV amplitude, however other frequencies and voltages can also be employed [123].

The semiconductor charge is given by the approximation presented in Equation B-2 for $N_D = 0$ and P ≈ n ≈ 0 in the depletion estimate and also it is assumed that all acceptors are ionised.

$$Q_S = qA \int_0^W (p - n + N_D^+ - N_A^-)\, dx \approx qA \int_0^W N_D dx \quad \text{B-2}$$

The charge increase dQ_S is due to the small increase in scr width. Assuming that N_A is constant over the space charge region, then Equation B-3 can be rewritten as,

$$Q_S = qAN_D dW \quad \text{B-3}$$

We can combine Equations Equation's B-1 and B-3 to derive

$$C = qAN_D \frac{dW}{dV_A} \quad \text{B-4}$$

The width of the depletion region (W) constantly changes due to the AC signal given than,

$$W = \sqrt{\frac{2K_S\varepsilon_0 dV_A}{qN_D}}$$ B-5

As W changes, so does the capacitance, since the capacitance in the space charge region corresponds to that across the parallel plates of the capacitor,

$$C = -\frac{\varepsilon A}{d} = \frac{K_S\varepsilon_0 A}{W}$$ B-6

where the distance between the plates (d) can be substituted with the width of the semiconductor region (W) and the permittivity of the dielectric (ε) can be replaced by the permittivity of the semiconductor ($K_S\varepsilon_0$). Equation B-7 is the result of differentiating Equation B-6 with respect to voltage,

$$\frac{dW}{dV_A} = \frac{dCK_S\varepsilon_0 A}{C^2 dV_A}$$ B-7

Substituting Equation B-7 into Equation B-4 gives,

$$-\frac{2}{N_D K_S\varepsilon_0 A^2} = -2C^3\frac{dC}{dV_A}$$ B-8

Integrating $-(2/C^{-3})\ dC/dV_A$ results in dC^{-2}/dV_A. This can be substituted into Equation B-8 to give,

$$\frac{dC^{-2}}{dV_A} = -\frac{2}{N_D K_S\varepsilon_0 A^2}$$ B-9

The above derivation can be done for p-type material resulting in the equation below:

$$\frac{dC^{-2}}{dV_A} = \frac{2}{N_A K_S \varepsilon_0 A^2} \quad \text{B-10}$$

Hence, considering Equations B-9 and B-10, for a Schottky diode, the capacitance per unit area can be calculated using the equation below [223],

$$\frac{C}{A} = \sqrt{\frac{\pm q K_S \varepsilon_O (N_A - N_D)}{2(\pm V_{bi} \pm V_A - kT/q)}} \quad \text{B-11}$$

where the "+" sign is used for p-type substrates ($N_A > N_D$), the "–" sign for n-type ($N_D > N_A$) substrates, and V_A is the reverse-bias voltage. For p-type substrates $N_D < N_A$, $V_{bi} > 0$, and $V > 0$, while for n-type substrates $N_D > N_A$, $V_{bi} < 0$, and $V < 0$. The kT/q expression in the denominator represents the majority carrier tail in the scr which is eliminated in the depletion approximation. Equation B-12 shows the relationship between the built-in potential and the Schottky barrier height,

$$\emptyset_{BN} = V_{bi} + V_o \quad \text{B-12}$$

Where V_o is the potential of the semiconductor Fermi level with respect to the conduction band and equals: $V_O = (kT/q) ln(N_C/N_D)$, and N_C is the effective density of states in the conduction band. The slope of the curve when plotting $1/(C/A)^2$ against V is defined by

$$2/[q K_S \varepsilon_O (N_A - N_D)] \quad \text{B-13}$$

and it's the intercept on the V-axis is

$$V_i = -V_{bi} + kT/q \qquad \text{B-14}$$

The barrier height is calculated from the intercept voltage by

$$\emptyset_{BN} = -V_i + V_o + kT/q \qquad \text{B-15}$$

And the doping density can also be calculated as discussed earlier in this section. $\emptyset_{BN}$(C–V) is roughly the flat-band barrier height as it is can be found using the $1/C^2$ –V curve for $1/C^2 \rightarrow 0$ or $C \rightarrow \infty$ demonstrating adequate forward bias to result in flatband conditions in the semiconductor.

An example of reverse-biased $1/C^2$ against V plot of a "No Anneal" Schottky diode is shown in Figure B-1 where the intercept voltage on the x-axis is found.

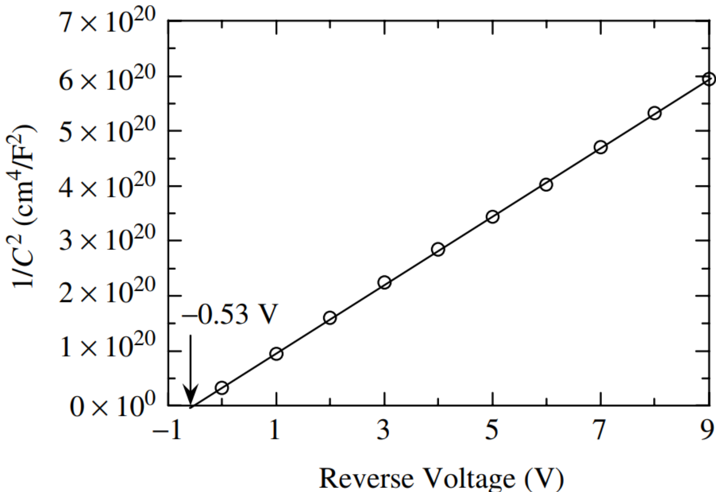


Figure B-1: Reverse-bias $1/C^2$ against V of the "No Anneal" diode measured at room temperature [97]

Appendix C

Carrier Recombination and Generation

Three types of carrier recombination exist where excessive electron/hole pairs stabilise in the valance layer and they annihilate each other during the recombination process:

- Auger recombination
- Radiative recombination
- Schockley-Read-Hall recombination

During Auger recombination, when an electron and hole recombine, their energy is transmitted to a different electron in the band edge of the conduction band in the shape of kinetic energy, resulting in its movement to a higher energy in the conduction band. This electron then steadily releases the extra energy in form of heat and travels down to the band edge of the conduction layer. Auger recombination normally occurs in the heavily doped semiconductor and during high level injection, when the number of excessive minority carriers that are injected into the semiconductor becomes similar to the background doping of the semiconductor. Figure C-1 shows the two steps of Auger recombination process.

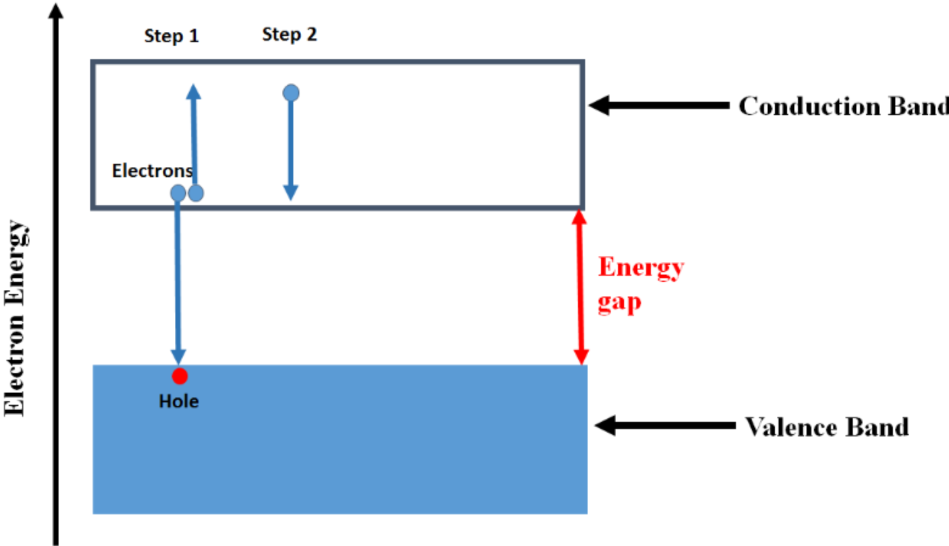


Figure C-1: Auger recombination process, where an electron and hole recombine, the electron release its energy to another electron (third electron) in the conduction band. This causes the third electron to move to a higher energy. It then releases its additional energy and moves back down to the edge of the conduction band.

Radiative recombination is also known as band-to-band recombination or electroluminescence and is shown in Figure C-2. In this phenomenon, when an electron and a hole recombine and the valance band of the semiconductor atom stabilises, the carriers release their energies in the form of photons (the emission of photons). Band-to-band recombination is the basic operation of Light Emitting Diodes (LED) where the wavelength of the emitted photon and therefore the colour of the emitted light depends on the bandgap of the semiconductor and the amount of released energy.

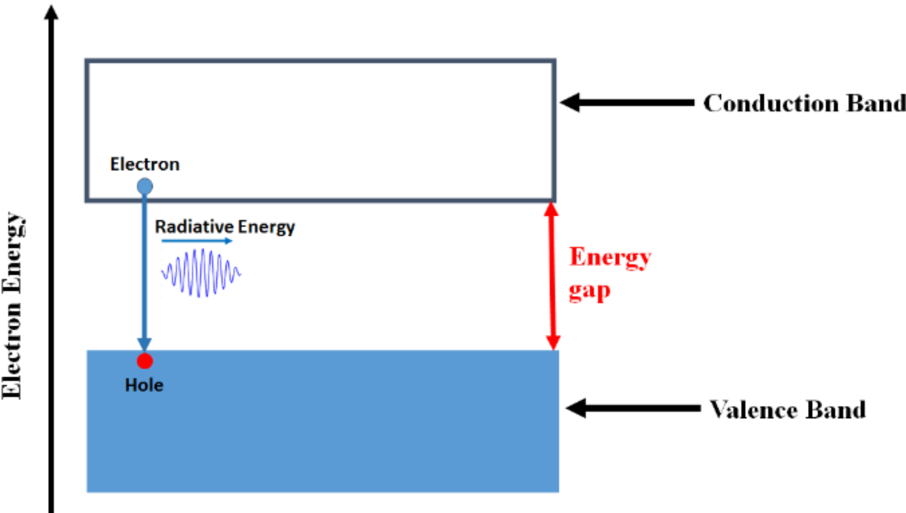


Figure C-2: Band-to-band recombination process.

Schockley-Read-Hall (SRH) recombination is a two-step process which occurs when an electron falls into a trap, an energy level in the bandgap due to the existence of a foreign particle (atom) or a defect. These defects could be an uncontrolled defect in the crystal lattice of the semiconductor such as presence of defects in SiC (as discussed in chapter 2) or an intentional added material due to doping of the semiconductor. This trap cannot accept another electron. In the second step, the electron that is residing in the trap can fall into an empty state in the valance band and hence ending the recombination process. Another explanation of this process is that the electron and hole annihilate in the trap band as they encounter in the trap. The trap band can either be located near the valance band or the conduction band and the SRH recombination rate relies on where the trap band is placed in relation to the conduction band or the valance band. If the trap band is close to the conduction band, the rate of SRH recombination is low due to the fact that the electrons or holes trapped in this band can easily receive

enough energy to jump up to the conduction band again. The most effective trap band to maximise the SRH recombination is the mid-point of the band-gap. Figure C-3 shows the SRH recombination process.

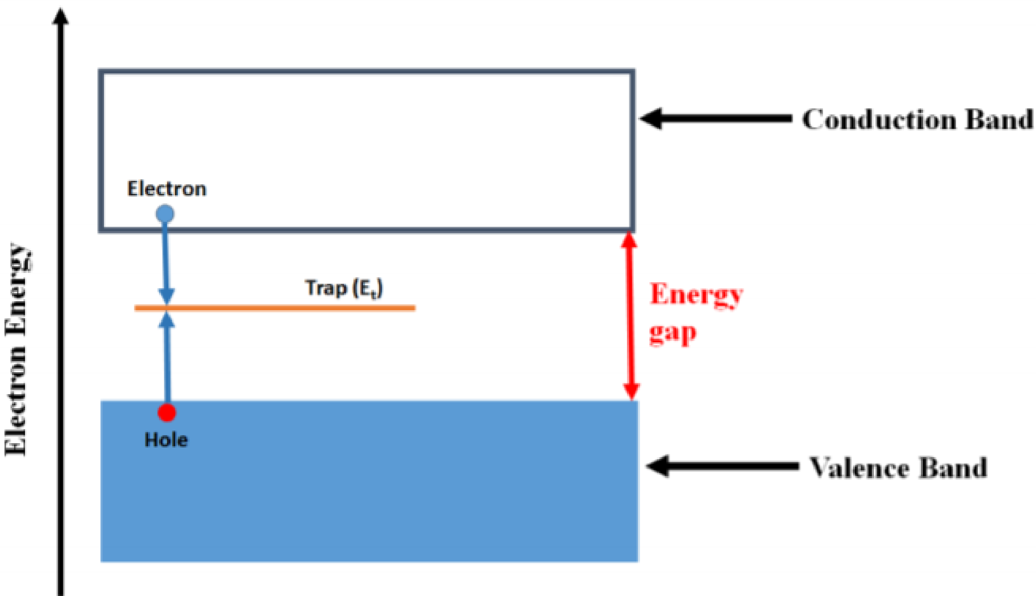


Figure C-3:Schockley-Read-Hall recombination process.

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