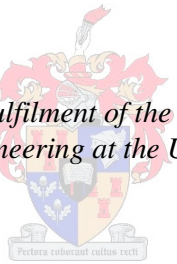
Shunt reactive compensation of voltage dips and unbalance

by
Frans Marx Welgemoed



Thesis presented in partial fulfilment of the requirements for the degree Master of Science in Engineering at the University of Stellenbosch

Supervisor: Dr. H.J. Beukes
Department of Electrical Engineering

December 2010

Declaration

By submitting this thesis electronically, I declare that the entirety of the work contained therein is my own, original work, and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

December 2010

Opsomming

Drywings elektroniese omsetters wat gebruik word vir newe reaktiewe kompensasie lewer meer effektiewe, akkurate en dinamiese resultate. In hierdie tesis word die toepassing van drywings elektroniese omsetters vir newe reaktiewe kompensasie bespreek. Daar word meer spesifiek na spannings duike en spannings wanbalans gekyk aangesien albei met newe reaktiewe kompensasie verminder kan word.

'n Bestaande nood kragbron is aangepas om as n newe reaktiewe kompenseerder te funksioneer. Die nood kragbron bestaan hoofsaaklik uit 'n 250 kVA drie fase omsetter spanningsbron. Die aanpassings is beperk tot sagteware en beheer algoritmes wat nie die oorspronklike funksionaliteit van die nood krag bron beinvloed nie. Beheer algoritmes word ontwerp en deeglik bespreek. 'n Tipiese dubbel lus beheer strategie word op die drywings elektroniese omsetter toegepas. Die binne-lus bestaan uit 'n voorspellende stroom beheerder. Die buite-lus bestaan uit drie proportioneel en integraal beheerders wat onderskeidelik die GS-bus spanning, WS spanning en spanning wanbalans reguleer.

Spannings duike en wanbalans is verminder deur slegs reaktiewe drywing te gebruik. Die doel was ook om 'n prakties bruikbare resultaat te lewer.

Abstract

The use of power electronic converters provides a more efficient, accurate and dynamic solution to reactive compensation. In this thesis the application of power electronic converters to shunt reactive compensation will be discussed. In particular voltage dips and voltage unbalance are considered as both can be mitigated by means of shunt reactive compensation.

A pre-existing uninterruptible power supply is adapted to operate as a shunt reactive compensator. The uninterruptible power supply consists of a 250 kVA three phase voltage source inverter. The modifications are limited to software and control algorithms that do not alter the normal operation of the uninterruptible power supply. Control algorithms are designed and discussed in detail. A typical double loop control strategy is implemented on the power electronic converter. The inner loop consists of a dead-beat current controller. The outer loop consists of three proportional and integral controllers controlling the DC-bus voltage, AC voltage and voltage unbalance respectively.

Voltage dips and unbalance are compensated for using only reactive power. Focus is placed on producing a result can be used easily in practice.

Acknowledgements

I would like to thank the following people....

My study leader, Dr HJ Beukes, for his assistance throughout my postgraduate studies.

My fiancé, Marelize Joubert, for her support, understanding and motivation throughout my studies.

My father, Frans Welgemoed, for his support and motivation and for making my studies possible.

The Lord for making it possible for me to complete this degree.

Contents

Declaration i

Opsomming ii

Abstract iii

Acknowledgements iv

List of Figures x

List of Tables xv

Nomenclature xvi

Abbreviations xvi

Circuit symbols xvi

Units xvi

Other xvii

Chapter 1: Introduction 1

1.1. Motivation 1

1.2. Background 2

1.3. Aim and outline of the Thesis 2

1.4. Contributions 3

1.5. Overview 4

Chapter 2: Voltage Dips and Unbalance 5

2.1. Introduction 5

2.2. Voltage Dips 5

2.2.1. Definition 5

2.2.2. Causes 6

2.2.3. Effects 6

2.2.4. Specifications 7

2.3. Unbalance 8

2.3.1. Definition 8

2.3.2. Causes 9
2.3.3. Effects 10
2.3.4. Specifications 11
2.4. Dip Mitigation Methods 11
2.4.1. Soft-starting 11
2.4.2. Constant Voltage Transformer 12
2.4.3. Step Regulator 12
2.4.4. Switching Converter Series Compensator 13
2.4.5. Fixed and Variable Impedance Static Compensators 13
2.4.6. Switching Converter Shunt Compensator 14
2.5. Unbalance Mitigation Methods 15
Chapter 3: The Voltage Source Inverter 16
3.1. Introduction 16
3.2. Control 18
3.2.1. Clarke-Transform 18
3.2.2. Park-Transform 22
3.2.3. Space Vector Modulation 23
3.3 Dead-Time Compensation 25
3.3.1. Introduction 25
3.3.2. Quantification 28
3.3.3. Effects 29
3.3.4. Dynamic Compensation 30
3.3.5. Implementing Methods 32
3.3.6. Performance 34
3.4. Dead-Beat Current Control 34
3.4.1. Introduction 35
3.4.2. Design and Theory 35
3.4.3. Implementation 38

3.4.4. Delay Compensation 39
3.5. DC-bus Controller 40
3.5.1. Introduction 40
3.5.2. Design and Theory 40
3.5.3. Implementation 47
3.5.4. Performance 51
3.6. Conclusion 52
Chapter 4: Shunt Connected VSI for Dip Mitigation 53
4.1. Introduction 53
4.2. VSI (VAR Generation) 54
4.3. System Overview 55
4.4. Controller Overview 57
4.5. Controller Design 60
4.6. Controller Implementation 69
4.7. Performance 71
Chapter 5: Shunt Connected VSI for Unbalance Mitigation 73
5.1. Introduction 73
5.2. VSI (Unbalanced Conditions) 74
5.3. System Overview 75
5.4. Unbalanced Voltage 77
5.4.1. Sequence Decomposition 78
5.4.2. Delayed Signal Cancellation 79
5.4.3. Weighted-Mean Error Reduction 82
5.5. Controller Overview 83
5.6. Controller Design 85
5.7. Controller Implementation 87
5.8. Performance 88
Chapter 6: Results 89

6.1. Introduction 89
6.2. Practical Measurements 89
6.3. Dead-time Compensation 90
6.4. Dead-Beat Current Controller 93
6.5. Dip Mitigation 94
6.5.1. Regulation 96
6.5.2. Dips 101
6.5.3. Unbalanced Conditions 104
6.5.4. Dynamic Performance 106
6.6. Unbalance Mitigation 108
6.6.1. Regulation 110
6.6.2. Unbalanced Dips 111
6.6.3. Dynamic Performance 113
6.7. Performance 113
Chapter 7: Conclusions 114
7.1 General 114
7.2 Dead-Time Compensation 115
7.3 Dead-Beat Current Controller 115
7.4 Dip Mitigation 116
7.5 Unbalance Mitigation 117
Bibliography 118
Appendix A 122
Dead-Time Compensation 122
Appendix B 128
Reactive Compensator *[C-code]* 128
Appendix C 129
Sequence Decomposition *[C-code]* 129
Appendix D 130

Unbalance Compensator *[C-code]*.. 130

List of Figures

Figure 2.1 - The three sequences into which an unbalanced system can be decomposed..... 8

Figure 2.2 - The basic circuit of a ferro-resonant regulator or CVT. 12

Figure 2.3 - Step regulator or tap-changer..... 13

Figure 2.4 - A transmission-line and load showing a static series compensator..... 13

Figure 2.5 - Shunt reactive compensation techniques. From left: Thyristor switched reactor, thyristor switched capacitor, fixed reactor and fixed capacitor. 14

Figure 3.1 - A basic half-bridge configuration showing the two IGBTs making up a single phase-arm and their individual anti-parallel diodes..... 16

Figure 3.2 - The three-phase VSI. 17

Figure 3.3 - The three-phase VSI as used in the specific UPS. 18

Figure 3.4 - A graphical representation of the Clarke-Transformation..... 20

Figure 3.5 - The direction and path of the space-vector in the stationary reference frame..... 21

Figure 3.6 - A graphical representation of the synchronous reference frame in relation with the stationary reference frame. 22

Figure 3.7 - A simplified model of the VSI showing the reference point on the bottom rail of the DC-bus. 23

Figure 3.8 - The eight different switch states that the three phase inverter can assume. 24

Figure 3.9 - The space-vector in sector I. 25

Figure 3.10 - The model of a single phase VSI as used to derive expressions for dead-time. 26

Figure 3.11 - Switching patterns. 27

Figure 3.12 - The effect of dead-time on the inverter's output voltage is shown..... 30

Figure 3.13 - The various times associated with an IGBT versus the current through the IGBT [19]..... 31

Figure 3.14 - TOP: The various times associated with an IGBT versus the current through the IGBT. BOTTOM: The duty cycle error caused as a result of the non-ideal switching times shown above. 32

Figure 3.15 - A typical switched current. 33

Figure 3.16 - A single phase-arm of the VSI used to derive the dead-beat controller. 36

Figure 3.17 - The currents involved with the dead-beat current controller. 39

Figure 3.18 - The DC-bus connected to the VSI. 41

Figure 3.19 – LEFT: The equivalent circuit of the DC-bus. RIGHT: The s-domain equivalent circuit of the DC-bus. 42

Figure 3.20 - The control-loop of the DC-bus controller. 43

Figure 3.21 - The known poles and zeros of the system are placed and the root locus constructed. 44

Figure 3.22 - The poles and zeros are placed and the root locus constructed after pole-zero cancellation. 45

Figure 3.23 - The response of the system to a unit step change. 46

Figure 3.24 – The response of the system to a unit step change. 47

Figure 3.25 - The digital control-loop depicted as two parallel branches. The top showing the proportional branch and the bottom the integral branch. 48

Figure 3.26 - The DC-bus voltage during a step change in the reference voltage. ... 51

Figure 4.1 - A feeder from the grid, V_s, to the load. 53

Figure 4.2 - The inductor in the output filter of the VSI. 54

Figure 4.3 - The converter voltage, V_c, with respect to the output voltage, V_f. LEFT: The inverter generating a lagging current. RIGHT: The inverter generating a leading current. 54

Figure 4.4 - A single-phase diagram of the system showing the directions and names of currents and components. 56

Figure 4.5 - A control diagram showing the system with a maximum impedance. ... 56

Figure 4.6 - The control diagram of the VSI showing the relation of the various control-loops and controllers. 57

Figure 4.7 - A control diagram showing the voltage-loop. 57

Figure 4.8 - The relationship of the voltage and reactive current space vectors depicted in the stationary reference frame. 58

Figure 4.9 - The V-I curve of the static compensator. 60

Figure 4.10 - The control diagram of the shunt reactive compensator. 60

Figure 4.11 - The control diagram after the reference voltage is set to zero. 61

Figure 4.12 - A very simplified version of the control diagram. The filter capacitance and regulation slope are neglected. 62

Figure 4.13 - Root locus for the known poles and zeros. 63

Figure 4.14 - The bode-plot of the known poles and zeros in the transfer function. . 63

Figure 4.15 - The bode-plot after the zero at 2500 rad/sec is inserted. 64

Figure 4.16 - The bode-plot with all the calculated values substituted. 65

Figure 4.17 - The control diagram with the regulation slope taken into consideration. 65

Figure 4.18 - The bode-plot of the system with the approximation made and the previously designed controller. 67

Figure 4.19 - The control diagram with all factors taken into consideration as intitally derived from the system. 68

Figure 4.20 - The bode-plot of the system with the intially designed controller. 69

Figure 4.21 - The implementation of the PI-controller. 70

Figure 5.1 - The feeder showing the shunt connected VSI at the point of regulation.76

Figure 5.2 - Single phase diagrams for the positive (TOP) and negative (BOTTOM) sequence systems 76

Figure 5.3 - A control diagram showing the relation of the inverter current to the measured voltage for the negative sequence. 77

Figure 5.4 - The interconnection of various external control-loops with the current controller. 84

Figure 5.5 - The closed-loop control diagram for the negative sequence voltage. ... 84

Figure 5.6 - The control diagram derived from the system analysis. 86

Figure 6.1 - The inverter current with no dead-time compensation implemented. The reference current is set at 100 A peak. 91

Figure 6.2 - The inverter current with dead-zone dead-time compensation implemented. The reference current is set at 100 A peak. 92

Figure 6.3 - The inverter current with slope dead-time compensation implemented. The reference current is 100 A peak. 92

Figure 6.4 - The response of the current controller to a step change in the reference current. 94

Figure 6.5 - The sytem used to test the shunt voltage-dip compensator as used in experiments and in simulations. 95

Figure 6.6 - RMS voltage of the three phases before compensation. 97

Figure 6.7 - Voltage and current plots during the first test. 97

Figure 6.8 - The RMS voltage of each phase during the first test. 98

Figure 6.9 - The RMS voltage of each phase during the second test. 99

Figure 6.10 - The RMS voltage of each phase during the third test. 99

Figure 6.11 - Voltage and current plots during the fourth test. 100

Figure 6.12 - The RMS voltage of each phase during the fourth test. 101

Figure 6.13 - The RMS voltage without compensation. 102

Figure 6.14 - The RMS voltage during compensation for the generated dip. 103

Figure 6.15 - Voltage and current plot for the dip with compensation. 103

Figure 6.16 - The RMS current generated by the inverter during the dip. 104

Figure 6.17 - A voltage and current plot of the reactive compensator under unbalanced conditions. 105

Figure 6.18 - The RMS voltage for each phase during an unbalanced dip. 105

Figure 6.19 – The step response of the inverter current space-vector magnitude for the maximum system impedance. 106

Figure 6.20 - The step response of the inverter current space-vector magnitude for a lower system impedance. 107

Figure 6.21 Response of the controller as a function of the system impedance... 108

Figure 6.22 - The system used to test the unbalance voltage compensator as used in simulations and practically 109

Figure 6.23 - The percentage voltage unbalance before unbalance compensation. 110

Figure 6.24 - The percentage voltage unbalance after unbalance compensation. . 110

Figure 6.25 - The percentage voltage unbalance, before compensation, during the generated dip. 111

Figure 6.26 - The percentage voltage unbalance, with compensation, during the dip of the third test. 112

Figure 6.27 - The percentage voltage unbalance during steady state conditions with compensation. 112

List of Tables

Table 2.1 - Voltage dip classifications according to NRS-048. 6

Table 2.2 - RMS voltage specifications for 400 V three phase systems. 7

Table 4.1 - System specifications for the designed controller. 65

Table 4.2 - System specifications for the designed controller. 67

Table 4.3 - System specifications for the designed controller. 69

Table 4.4 - System specifications for the designed controller with a variation in the system impedance. 71

Table 6.1 - The THD of the current for each dead-time compensation method. 93

Table 6.2 - Component values used in dip mitigation tests. 95

Table 6.3 - The reference voltages used in the various tests. 96

Table 6.4 - Component values used in unbalance mitigation tests. 109

Table 6.5 - The delta load resistances for the unbalance compensation test. 111

Table A.1 - Dead-time compensation summarized. 127

Nomenclature

Abbreviations

AC	Alternating Current
DC	Direct Current
DPS	Digital Signal Processor
DSC	Delayed Signal Cancellation
NRS	National Regulatory Services
PEC	Power Electronic Converter
PI	Proportional and Integral
SSC	Static Series Compensator
THD	Total Harmonic Distortion
TSC	Thyristor-switched Capacitor
TSR	Thyristor-switched Reactor
UPS	Uninterruptible Power Supply
VAR	Volt-Ampere Reactive
VSD	Variable Speed Drive
VSI	Voltage Source Inverter

Circuit symbols

C	Capacitor
D	Diode
L	Inductor
S	Switch

Units

A	Ampere
dB	Decibel

Hz	Hertz
s	Seconds
V	Volt

Other

f_s	Sample frequency [Hz]
f_{ac}	Line voltage frequency [Hz]
I_c	Capacitor current [A]
I_{dc}	Inverter DC-bus current [A]
I_f	Inverter output filter current [A]
I_s	Supply current [A]
K_i	Integrator gain
K_p	Proportional gain
K_r	Regulation slope constant $\left[\frac{V}{A}\right]$
UB_v	Voltage unbalance [%]
V_c	Converter output voltage [V]
V_{dc}	Inverter DC-bus voltage [V]
V_f	Inverter output filter voltage [V]
V_s	Supply voltage [V]

Chapter 1: Introduction

This chapter serves as an introduction to this thesis. A motivation for the study is given followed by background information, objectives and contributions. Finally an overview of the study and the content is given.

1.1. Motivation

The main motivation behind this study is the improvement of power quality.

The power quality phenomena focussed on are voltage dips and voltage unbalance. Although there are many methods of improving these phenomena the methodology used is dictated by a prerequisite of using a shunt connected three-phase uninterruptible power supply (UPS).

The trend is to use power electronic converters (PECs) to mitigate power quality issues. Using a UPS to improve power quality is a suitable solution because UPSs incorporate PECs and may already be installed at a customer who is sensitive to poor power quality. No hardware costs are involved and only software needs to be implemented.

The idea is then to use an existing UPS and simply implement control algorithms in its software that will not influence its normal working while improving the power quality. Using an existing UPS and simply upgrading software will not only reduce the effect that poor power quality has on the customer; it will greatly reduce the cost involved with the added functionality.

The control algorithms and methods for the mitigation of dips and unbalance are not exclusively for UPS application and may be used on similar PECs.

1.2. Background

Power quality is an important issue that requires attention in any power system. Phenomena such as harmonics, interruptions, voltage dips and swells, surges, flicker and unbalance are considered when measuring power quality. Poor power quality reduces the overall efficiency of the power system and may cause other issues at user level. The trend is to use power electronic based solutions and more specifically PECs to improve the power quality.

Two phenomena related to power quality have been identified for consideration throughout this study. These are voltage dips and voltage unbalance that have a serious influence on the quality of power received by customers of the electricity supplier. The specific power quality condition may have serious consequences for these customers.

Customers making use of voltage sensitive equipment may be vulnerable to voltage dips. Dips may cause voltage sensitive equipment to detect an under voltage event and switch off. The consequences are interruptions in the processes of such a customer that may cause large amounts of downtime.

1.3. Aim and outline of the Thesis

The main objectives are listed below.

- *Mitigation of balanced voltage dips*. One of the main objectives of this study is to mitigate voltage dips. Only reactive power is to be used. The transient depth of the dip is to be reduced so that voltage sensitive equipment will not experience the dip.

- *Regulation of balanced voltage to within 3 % of the nominal value.* As a secondary objective to the one above it was decided to set a specification on the maximum deviation from the nominal voltage. The RMS voltage of each phase will therefore not deviate from the nominal value by more than 3 % at any time.

- *Mitigation of unbalanced voltage dips*. The other main objective of this study is to mitigate unbalanced voltage. The aim is to reduce the voltage unbalance to below 2 %.

- *Specifications*. A specification for the depths of voltage dips and unbalance was chosen before the onset of the study. The 3 % specification chosen for the voltage regulation is far less than specified by the NRS-048 while the specification of 2 % for voltage unbalance is the nominal specification of the NRS-048. These specifications were decided on for purely idealistic reasons. The results achieved are shown in the results section.

1.4. Contributions

As can be expected a thorough understanding of the working of PECs is necessary before any modification can be made to an existing device. The working of voltage source inverters (VSIs) was researched and issues that may impact on the performance and working of the converter as it is meant to be used, were identified.

The identified components and issues were the dc-bus voltage controller, current controller and dead-time effects. These were identified as components and issues that would impede the performance of the converter or are critical to the application.

It was found that dead-time not only reduced the operational range of the converter but also impedes dynamic response. Existing dead-time compensation methods were analysed and considered. Expanding on an existing dead-time compensation method produced a significant result and improved the converter's operational range.

A current controller is essential to ensure easy interconnection and design of external control-loops. The performance of the current controller is also important to maximize the response of the converter to system changes. A wide-band predictive controller was derived and implemented allowing easy interconnection of various external control-loops.

The design procedure of a reactive compensator is evaluated. Suggestions about the practical implementation of the controllers, especially the unbalance compensator, are also made.

1.5. Overview

Although the compensation of voltage dips and unbalance will be incorporated to function simultaneously on a single VSI the discussion of each is handled separately.

Understanding the causes and effects of dips and unbalance will provide a basis for understanding the overall problem better. It also aids the testing phase of the study. Understanding how these phenomena occur in practice help the researcher to choose the most suitable testing methodologies. Dips and unbalance are discussed in chapter 2 where the definitions, causes and effects of each are discussed. Looking at other methods of compensating for dips and unbalance will allow for a more objective look at test results and also lead to the best solution being chosen.

In chapter 3 the basic operation of VSIs is discussed and the focus is more specifically on the VSI used in this thesis, from here on referred to as the test VSI. Control techniques are discussed briefly and the commonly used transformations are shown. This is followed by a discussion on dead-time, the effect that it has and how it can be compensated for follows. A dead-beat current controller is discussed and designed to control the converter. A proportional integral (PI) controller is also designed to regulate the DC-bus voltage.

In chapter 4 the focus is on shunt reactive compensation by means of a VSI. The system is analysed and VAR generation is discussed. The controller and the design thereof are discussed in detail.

In chapter 5 the focus is on the shunt compensation of voltage unbalance by means of a VSI. The system is analysed and sequence decomposition is discussed in detail. The controller and its implementation are also discussed in detail.

In chapter 6 all results that were obtained throughout the thesis and that are relevant, provide insight or confirm design specifications. In some cases comparisons are made between different methods or implementation methods.

In chapter 7 what has been done and achieved is summarised.

Chapter 2: Voltage Dips and Unbalance

In this chapter an overview of voltage dips and unbalance is presented. The cause, classification, effects and mitigation methods of each are discussed.

2.1. Introduction

To be able to resolve a problem adequately the causes and effects of the problem need to be investigated. For this reason it makes sense to determine what causes voltage dips and unbalance. Knowledge of the causes of voltage dips and unbalance will aid in setting up suitable experiments to test the designed mitigation methods.

It is also important to investigate the effects arising from these phenomena. Not only will the effects highlight the importance of the mitigation but will also give an indication of what effect requires priority above another.

The above is discussed in the following sections. An overview of other mitigation methods is also given.

2.2. Voltage Dips

2.2.1. Definition

Voltage dips are defined differently by different institutions. Generally voltage dips are specified in terms of their duration and the retained or residual voltage [1]. Voltage dips differ from under voltage events in that under voltage events generally last much longer than dips. The definition assumed is that of the NRS-048 standard. According to the NRS-048 standard voltage dips are defined as sudden reductions in the RMS voltage to a level below 0.9 per unit of the declared voltage for a period between 20 ms and 3 s [2]. The reduction may occur at any or all of the phases. Table 2.1 shows the classification of various dips according to the NRS-048 standard.

<table>
<tr><th rowspan="2">Range of residual voltage
U_r (% of $V_{nominal}$)</th><th colspan="3">Duration (t)</th></tr>
<tr><th>20 < t ≤ 150 ms</th><th>150 < t ≤ 600 ms</th><th>600 < t ≤ 3000 ms</th></tr>
<tr><td>90 > U_r ≥ 85</td><td colspan="2" rowspan="3">Y</td><td></td></tr>
<tr><td>85 > U_r ≥ 80</td><td rowspan="2">Z_1</td></tr>
<tr><td>80 > U_r ≥ 70</td><td rowspan="3">S</td></tr>
<tr><td>70 > U_r ≥ 60</td><td>X_1</td><td rowspan="3">Z_2</td></tr>
<tr><td>60 > U_r ≥ 40</td><td>X_2</td></tr>
<tr><td>40 > U_r ≥ 0</td><td colspan="2">T</td></tr>
</table>

Table 2.1 - Voltage dip classifications according to NRS-048.

2.2.2. Causes

There are two main causes of voltage dips. These are the connection and starting of large loads or faults on the network [1].

The large current drawn by a load during start-up flows through the transmission-line and causes a voltage drop across the transmission-line which is proportional to the transmission-line impedance. The effect that the voltage drop has on other points of the network is dependent on the network topology.

For a feeder, as focussed on in this thesis, the switching on of a large load on the transmission-line will affect the voltage at all points on the feeder transmission-line. This means that an industrial plant, such as a sawmill, may influence the voltage of another customer connected to the same feeder transmission-line.

Faults on other parts of the network may cause fluctuations in the voltage at different points on the network. These fluctuations may or may not be detected as a voltage dip at a specific point as they are dependent on the network topology and the relation of the fault to the reference site [1] [2].

2.2.3. Effects

Most equipment is designed to withstand small voltage dips, however some equipment does not allow for voltage dips, because manufacturers feel that there is

no need for this or that the cost to make the equipment resilient to a voltage dip is too high. While the voltage dip may not have a serious effect on the customer causing the dip, it may have adverse effects on other customers with voltage sensitive equipment. Some examples are discussed in the following paragraphs.

Something as simple as a sodium discharge lamp may experience problems if a voltage dip is present. These lamps may have a much higher striking voltage when they are hot [1]. The striking voltage may become so high that a lamp may not restart after a dip that caused it to turn off. These lamps may turn off as a result of as little as a 2 % voltage drop [1].

Contactors are also susceptible to voltage dips. The actual point on the voltage waveform where the dip occurs may cause a contactor to fall out [1].

Induction motors that lose too much speed during a dip may draw close to their entire start-up current when they try to re-accelerate [1]. If there are multiple motors experiencing a dip and re-accelerating at the same time the total current drawn may cause further problems.

2.2.4. Specifications

The specifications which determine the allowed deviation from the nominal voltage are shown in the table below, as specified by NRS-048:2 for all systems below 500 V. The matching phase to phase and phase to neutral voltages are shown as well as the ±3 % specification as chosen in this thesis.

Voltage specifications for 400 V systems		
Range	**Phase - Phase Voltage**	**Phase-Neutral Voltage**
±10 % NRS Compatibility Level	360 V – 440 V	207 V – 254 V
±15 % NRS Limit	340 V – 460 V	196 V – 265 V
±3 % Specification Limit	388 V – 412 V	224 V – 237 V

Table 2.2 - RMS voltage specifications for 400 V three phase systems.

2.3. Unbalance

A three-phase system is balanced if the three-phase voltages and currents have the same magnitude and are phase shifted by 120° with respect to each other [3] [4]. An unbalanced system can be decomposed into a positive-, negative- and zero-sequence system. These sequence or Fortescue components, denoted by the subscripts (+, - , 0), are calculated from the three-phase phasor values, denoted by subscripts (a, b, c) as shown by equation 2.1.

$$\begin{bmatrix} V_+ \\ V_- \\ V_0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad 2.1$$

where a is the rotational operator and is given by: $a = e^{-j120^\circ}$.

The three-phase voltages in equation 2.1 may also be replaced by the three-phase currents if the current sequence components are to be calculated.

The positive and negative sequence systems are both balanced three-phase systems with a frequency of 50 Hz. With the negative sequence system the phase order has been reversed. The zero sequence system consists of three components that are identical in magnitude and phase and only occurs in a system with a neutral point. If the system is balanced, the zero and negative sequences do not exist. Figure 2.1 shows the phasor diagrams for the three sequence systems.

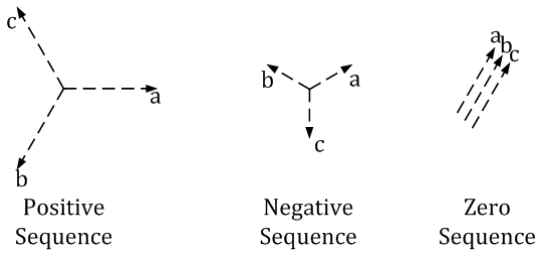


Figure 2.1 - The three sequences into which an unbalanced system can be decomposed.

2.3.1. Definition

To measure the “amount” of unbalance that exists in a system, the sequence components are used. The two definitions used are: negative sequence voltage unbalance and the zero sequence voltage unbalance. They are calculated using the

magnitudes of the positive, negative and zero sequences as shown by equation 2.2 and 2.3.

$$\text{Negative Sequence Voltage Unbalance} = \frac{V_-}{V_+} \cdot 100 \qquad 2.2$$

$$\text{Zero Sequence Voltage Unbalance} = \frac{V_0}{V_+} \cdot 100 \qquad 2.3$$

where V_- is the magnitude of the negative sequence voltage,

V_+ is the magnitude of the positive sequence voltage and

V_0 is the magnitude of the zero sequence voltage.

Zero sequence current cannot flow in three wire systems and is therefore often not used [4]. The ratio between the magnitude of the negative and positive sequence, or the negative sequence unbalance is commonly used as a measure of unbalance. Although many other definitions of unbalance exist in literature [3] [4] [5] [6], the definition given by equation 2.2 is mostly used. Equation 2.2 shows the equation used to calculate voltage unbalance, denoted by UB_v. Replacing the positive and negative sequence voltage components with the respective positive and negative sequence current components gives the current unbalance, UB_i.

2.3.2. Causes

The system voltages at the point of generation are generally highly balanced due to the physical construction and operation of synchronous generators [3]. The cause of an unbalanced system generally does not lie at the point of generation. Variations in the impedance of transmission-lines for each phase and single-phase loads could cause unbalance. The effect is that different voltage drops across each phase will occur even if the current flowing in each phase is the same. With the voltage balanced at the point of generation the unbalanced voltage drop across the phases will cause an unbalanced voltage to be experienced at the end of the transmission-line. The variation in the impedances of transmission-lines is very often negligible due to precautions such as transposition of lines that are taken into consideration during the construction of a transmission network [3].

In most cases unbalanced and single-phase loads cause unbalance in three-phase systems [3] [4]. These loads cause unbalanced current to flow in the transmission-line causing the voltage drop across each phase to be different. The voltage experienced at a point further down the line may then be unbalanced.

Unbalanced voltage has various effects and can be compensated for. Some of the effects of voltage unbalance are discussed in the following section.

2.3.3. Effects

The greatest effect of voltage unbalance is the effect that it has on three-phase induction motors. The main reason is the fact that they are found in large numbers on the network [4]. A three-phase induction motor connected to an unbalanced supply voltage results in current unbalance that is much greater than the voltage unbalance [4]. The negative sequence current then causes an inversely rotating magnetic field which causes a braking torque in the motor. The result is a reduction in the maximum deliverable torque and the excessive current draw causes heating and faster thermal ageing [3] [7] [8]. Unbalance also causes these machines to be noisy due to torque and speed pulsations [4].

The capacities of transformers, cables, and transmission-lines are reduced in unbalanced systems [8]. The reason is that the rating of such equipment is determined by the RMS current flowing in the conductor [4]. If the current consists of a large negative sequence component, that is unusable to the consumer, the maximum amount of positive sequence current that is transmittable through the conductor is reduced. Depending on the configuration of the transformer, zero sequence currents can cause heating of the transformer.

If the voltage of a single or multiple phases falls to below a certain value the same effects as with voltage dips may be experienced by loads connected to the specific phases.

2.3.4. Specifications

A compatibility level of 2 % is set by the NRS-048 standard. Although no limit is set on unbalance a limit of 3 % for all three phase networks is under consideration [2]. In this thesis a maximum of 2 % is chosen for voltage unbalance. The aim will be to reduce the voltage unbalance to below 2 %.

2.4. Dip Mitigation Methods

The methods used to mitigate or compensate for voltage dips differ in level of complexity, accuracy and response time. Although the main focus here is on shunt reactive compensation some other methods are briefly discussed here for background purposes. The approach followed is to reduce the interruptions that voltage dips cause in industry processes. Some methods only stop processes in the event of a voltage dip so that the process should be restarted in a structured way. This is purely a safety factor and does not mitigate or compensate for voltage dips.

The specific application determines which method is most suitable. The factors taken into consideration would usually be the required level of dip immunity in terms of accuracy and response time, the cost of the solution and the size of the installation. Some methods may not be suitable for fast voltage dip mitigation but are rather used for regulation purposes.

2.4.1. Soft-starting

Since the main cause of voltage dips is the connection of large loads, the most obvious solution when mitigating voltage dips is to make the connection more gradual. Soft-starting is an effective way to achieve this and is a suitable solution for devices such as motors and furnaces. Auto-transformers or variable speed drives (VSDs) are used for soft-starting. If the load cannot be soft-started or other factors cause the voltage dips then other methods are available to mitigate voltage dips.

2.4.2. Constant Voltage Transformer

As the name dictates this method makes use of a transformer. The ferro-resonant or constant voltage transformer (CVT) is shown in figure 2.2. The transformer has a 1:1 turns ratio and is operated at a point above the knee-point on its saturation curve [9] meaning that the output voltage remains constant no matter how the input voltage varies [9]. The operating region of the transformer is ensured by selecting the capacitor appropriately. There are several disadvantages to this method and only some are noted here. The first is the limiting of the output current that makes the CVT unsuitable for loads requiring large start-up currents [10]. The CVT is therefore more suitable for constant loads. The CVT produces very high magnetic fields due to the core saturation which may pose a problem to sensitive equipment in the immediate vicinity.

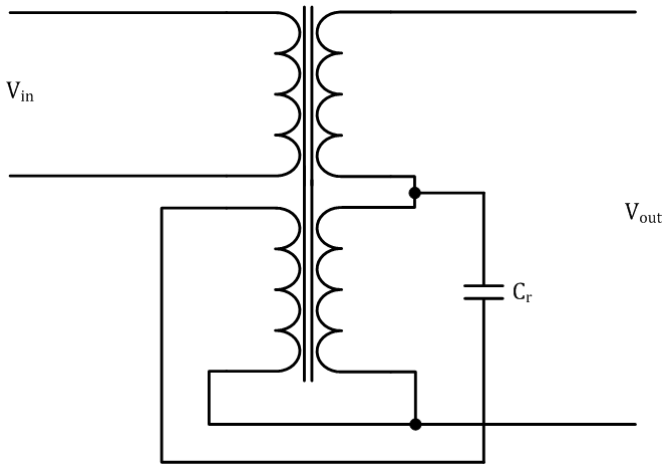


Figure 2.2 - The basic circuit of a ferro-resonant regulator or CVT.

2.4.3. Step Regulator

Another method making use of a transformer is the method which makes use of a step-regulator or a tap-changer. The transformer used here has multiple taps on its secondary side as shown by figure 2.3. The load may be connected to a tap that will realize a voltage closest to the required voltage. The step-regulator is a low cost solution and may have very high efficiency [10]. The major disadvantage is that the voltage regulation can only be done in steps and may not always be very accurate. A limited number of taps on the secondary side is the cause of this step-like regulation.

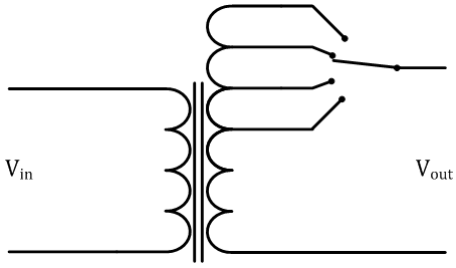


Figure 2.3 - Step regulator or tap-changer.

2.4.4. Switching Converter Series Compensator

The methods mentioned so far require some series connected device between the supply and the point of regulation. A major disadvantage is the one related to faults or outages and means that these devices cannot be used to mitigate interruptions [11]. Another method that also requires such a series connection is shown in figure 2.4 and is referred to as static series compensation (SSC).

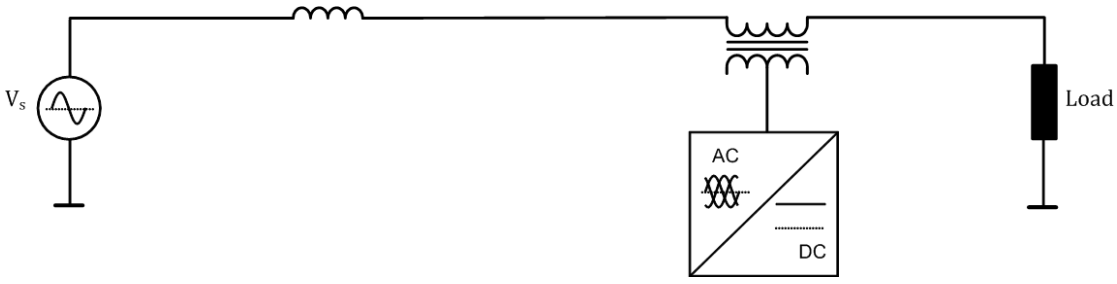


Figure 2.4 - A transmission-line and load showing a static series compensator.

The SSC requires the series connection of a transformer with the secondary in series with the load and the primary connected to a VSI. The voltage required to regulate the load voltage is simply added by means of the inverter and transformer. The SSC produces more dynamic and accurate compensation than the tap-changer but still requires an unwanted series connection.

2.4.5. Fixed and Variable Impedance Static Compensators

Capacitor or reactor banks are used to load a transmission-line to regulate the voltage with varying loads. This method either requires the calculation of the exact

reactive load for the operating condition or switching in multiple smaller reactive loads that reduces the accuracy and response time of this compensation technique.

A slight variation on this method is switching the reactive load in by means of thyristors while adjusting the firing angle to achieve the correct reactive current. This is commonly referred to as thyristor-switched reactor (TSR) or thyristor-switched capacitor (TSC). Switching the load in and out makes the reactive load appear to be variable for better dynamic compensation and improved accuracy. Various combinations of these four methods are sometimes implemented. Figure 2.5 shows the four most common methods connected in shunt with the transmission-line.

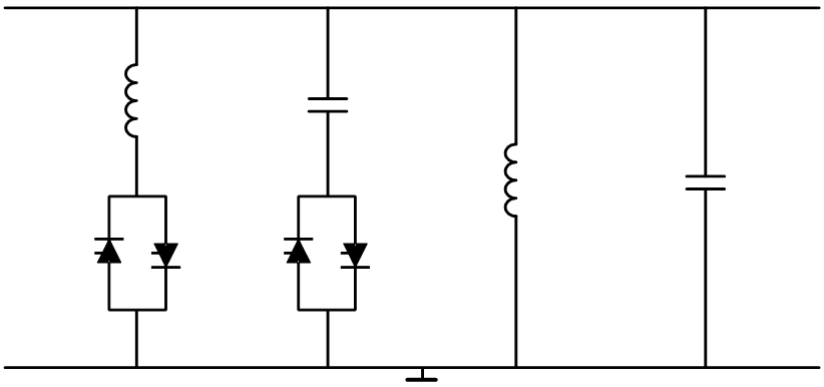


Figure 2.5 - Shunt reactive compensation techniques. From left: Thyristor switched reactor, thyristor switched capacitor, fixed reactor and fixed capacitor.

2.4.6. Switching Converter Shunt Compensator

Using a PEC to supply the reactive power to the transmission line allows for fast, dynamic and accurate compensation of voltage dips. The converter based VAR generators generally have a much faster response than a TSC or TSR [12]. A PEC also has no inertia compared to synchronous generators that are also used for shunt reactive compensation.

The converter is controlled to draw either a leading or lagging current, allowing the converter to appear as a variable reactive load to the transmission-line.

Converter based solutions reduce the overall size of the installations by up to 40 % [13].

2.5. Unbalance Mitigation Methods

With the causes of unbalance known it is possible to apply appropriate techniques to minimize the amount of unbalance in a three-phase system. These can range from utility level to plant level techniques.

Utility level techniques entail the following practices. The most obvious method is the redistribution of loads across the three phases. Redistribution can be done in a system where there is already an unwanted level of unbalance due to unbalanced loading of the three phases. Another solution that can be implemented at utility level is the reduction in unbalance between phase impedances. These include transmission lines and transformers. The voltage drop across each phase will be the same with balanced loads if the impedance of each phase is the same.

Plant level techniques usually require the customer to take some action to limit the unbalance at its plant. As with the utility level techniques the balancing of single-phase loads across the three phases is a simple and effective method to reduce unbalance. Another method requires the use of static VAR compensators. These compensators can be configured to reduce voltage unbalance by means of reactive power as discussed in this thesis.

Other methods that aid in the balancing of a three-phase system, where single-phase loads are used, require special transformers. These are the Scott and Steinmetz transformers [3]. Both these transformers allow for the connection of single-phase loads to a three-phase system while the three-phase system sees a balanced three-phase load. In the case of the Steinmetz transformer the load should be constant at the designed value for the load balancing to be effective.

The use of static compensators, as noted above, is preferable due to the method's dynamic compensation capabilities. The additional cost of these compensators make them unsuitable for most users who do not require very low levels of unbalance or who can reduce the unbalance by means of another method. Static compensators are mainly used in large industries and where other methods are insufficient.

Chapter 3: The Voltage Source Inverter

In this chapter an overview of voltage source inverters in general as well as the test VSI is presented. First the general control schemes used are shown where after a detailed discussion on dead-time compensation and the design of a dead-beat current controller is presented. The design of a suitable DC-bus controller is also discussed as this is almost always used in VSIs.

3.1. Introduction

Voltage source inverters are used in many applications in industry; these include uninterruptable power supplies, variable speed drives, active filters, flicker compensators and dynamic voltage restorers [14].

The basic single-phase VSI has a conventional half bridge topological structure as shown in figure 3.1. An extension of this inverter leads to the three-phase VSI shown in figure 3.2. Figure 3.2 shows the three parallel half-bridge structures that form the three phase arms of the VSI.

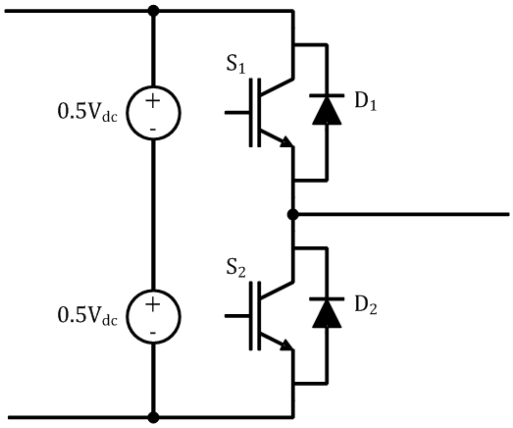


Figure 3.1 - A basic half-bridge configuration showing the two IGBTs making up a single phase-arm and their individual anti-parallel diodes.

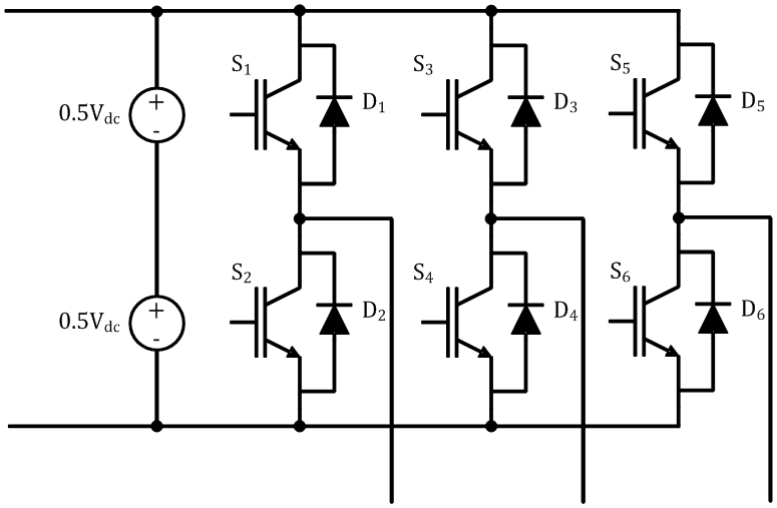


Figure 3.2 - The three-phase VSI.

A VSI is fed from a DC voltage source. Depending on the application this may be anything such as capacitors, batteries, flywheels, active and passive rectifiers etc.

The power switches shown are conventional IGBTs however in some applications power MOSFETs, thyristors or GTOs can be used. As shown in figures 3.1 and 3.2 each switch is paralleled with a free-wheeling diode the purpose of which is to make the switch bidirectional. Current is therefore able to flow in both directions through each part of the phase-arm and therefore makes the VSI a four-quadrant converter [15]. Subsequently the VSI is able to deliver and absorb power.

The test VSI is shown in figure 3.3. The VSI is connected to a battery and is mainly used as a UPS. The VSI is rated to 250 kVA at 400 V. It is also advantageous to use a UPS for dip and unbalance mitigation since it would normally be connected in shunt with the load as required for these applications.

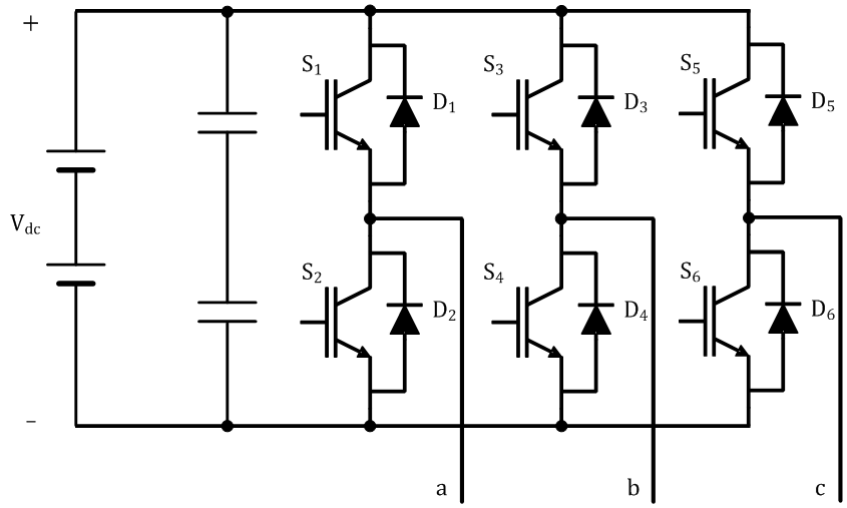


Figure 3.3 - The three-phase VSI as used in the specific UPS.

3.2. Control

Various control methods and implementations are used to control VSIs depending on their implementation and application. Control is often done only in the (α, β) reference frame due to its simplicity. Some applications require the use of the (d, q) reference frame and sometimes even variations thereof. The advantages and disadvantages of each are explained in this section. The conditions under which each should be used are also noted.

3.2.1. Clarke-Transform

The Clarke-transformation is used to transform the three dimensional (a, b, c) system to an equivalent two dimensional (α, β) system, also known as the stationary reference frame. For the transformation to hold it is assumed that the system is balanced. Under balanced conditions the transformation does not lead to any loss of information. For unbalanced systems the transformation makes provision for a zero sequence component, V_γ. The transformation is given in full by equation 3.1.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad 3.1$$

where, $T_{\alpha\beta}$ is the αβ coordinate transformation and is given by equation 3.2.

$$T_{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad 3.2$$

In a balanced system the V_γ term equates to zero and may be neglected. The inverse transformation is given by equation 3.3.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = T_{\alpha\beta}^T \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} \quad 3.3$$

A graphical representation of the Clarke-transformation, showing the relation of the αβ-axes to the three-phase vectors, is shown in figure 3.4.

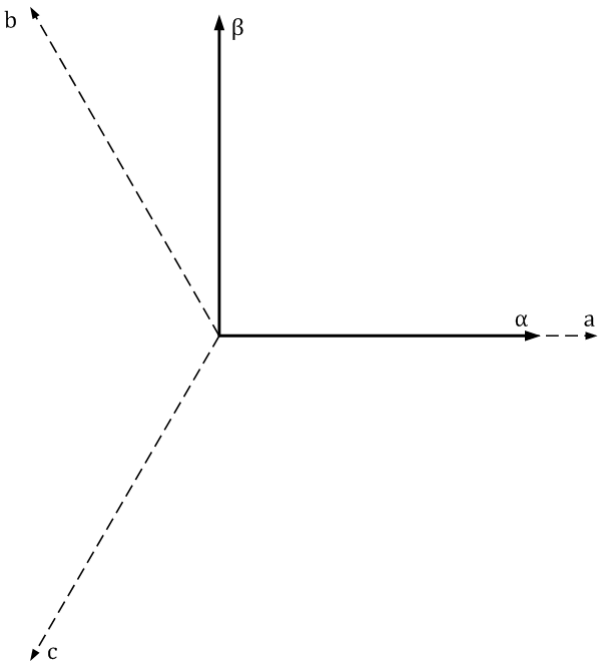


Figure 3.4 - A graphical representation of the Clarke-Transformation.

If the three instantaneous voltage values, in equation 3.4, are subjected to the transform, shown in equation 3.1, the corresponding αβ-voltages are given by equations 3.5 and 3.6.

$$\begin{aligned} V_a &= V_M \sin(\omega t) \\ V_b &= V_M \sin(\omega t - 120°) \\ V_c &= V_M \sin(\omega t + 120°) \end{aligned} \qquad 3.4$$

$$V_\alpha = \sqrt{\frac{3}{2}} V_M \sin(\omega t) \qquad 3.5$$

$$V_\beta = -\sqrt{\frac{3}{2}} V_M \cos(\omega t) \qquad 3.6$$

Under balanced conditions three-phase vectors are transformed to a single vector consisting of a real, α, and imaginary, β, components. The vector rotates counter-clockwise in the αβ-plane at the fundamental system frequency. One full revolution in the stationary reference frame equates to one cycle at the fundamental system

frequency. The magnitude of the αβ-vector is $\sqrt{3/2}\,V_M$. Figure 3.5 shows the rotating vector in the stationary reference frame.

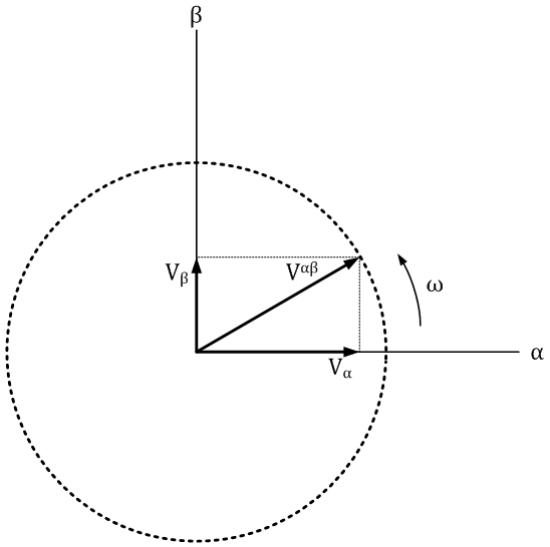


Figure 3.5 - The direction and path of the space-vector in the stationary reference frame.

The advantage of using the (α, β) reference frame to implement control in a VSI is that the three-dimensional space is transformed to a simpler two-dimensional space. This transformation also requires less computation effort than other transformations.

The disadvantage of using this reference frame is that the α and β components are sinusoidal causing PI-controllers to have a tracking error. The tracking error may have a non-negligible effect. [15].

Under balanced and low harmonic conditions the magnitude of the space-vector is not sinusoidal but rather a constant value. Under these conditions a PI-controller can be implemented to regulate the magnitude of the space-vector. The successful implementation of such a controller is shown in chapter 4.

Under unbalanced conditions the magnitude of the space vector becomes irregular and the path that it follows in the αβ-plane becomes elliptical. In a following section it is shown that this is due to the presence of a non-zero negative sequence voltage. The negative sequence space-vector essentially rotates in the opposite direction to that of the positive sequence space-vector in the αβ-plane. The summation of these two oppositely rotating components causes the tip of the resultant space-vector to

follow an elliptical path. Under such conditions the use of another transformation is required.

3.2.2. Park-Transform

The Park-transformation transforms the three dimensional, (a, b, c), system to a two-axis synchronous rotating reference frame. The implication is that the transformation is a dynamic one rather than a static one as with the Clarke-transformation. The Park-transformation defines a new set of axes, (d, q), that rotate around the αβ-axes at the fundamental system frequency as depicted in figure 3.6.

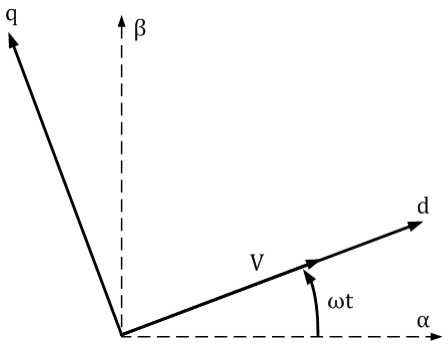


Figure 3.6 - A graphical representation of the synchronous reference frame in relation with the stationary reference frame.

If the frequency at which the dq-plane rotates is equal to the fundamental system frequency, the angle θ will be equal to ωt, where ω is the fundamental system frequency. The implication is that the vector V does not rotate with respect to the newly defined axes. This means that the projections of V onto the dq-axes is constant and can be viewed as DC-voltages. The d-axis is in phase with the space-vector.

This transformation is done mathematically as shown in equation 3.7.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{dq} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \qquad 3.7$$

where, $T_{\alpha\beta}$ is the dq coordinate transformation given by equation 3.8.

$$T_{dq} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad 3.8$$

The inverse transformation is given by equation 3.9.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T_{dq}^T \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad 3.9$$

The general advantage of using the synchronous reference frame is that the non-negligible tracking error of a PI-controller with respect to sinusoidal reference signals can be eliminated. The reason is that a PI-controller can ensure a zero tracking error with respect to a constant reference signal.

3.2.3. Space Vector Modulation

Space-vector modulation is a method used to implement PWM in three-phase inverters. It entails transforming the three-phase inverter output voltage, V_c, to the αβ-plane and comparing the vector with the available switching states of the inverter.

Space-vector modulation is discussed in great detail by many other authors and only a brief overview follows. As shown in figure 3.7 the inverter is fed with a single DC voltage source and the neutral point is isolated from the DC-bus. The bottom rail of the DC-bus is used as reference for the calculation of the inverter output voltages.

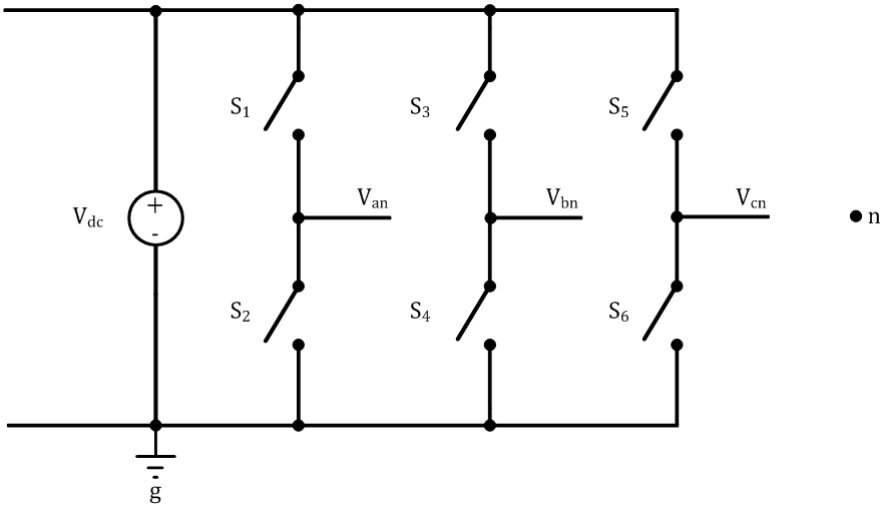


Figure 3.7 - A simplified model of the VSI showing the reference point on the bottom rail of the DC-bus.

The inverter is able to assume eight different switch states. These are depicted in figure 3.8. The figure also shows the equivalent output voltage vector realized by each switch state.

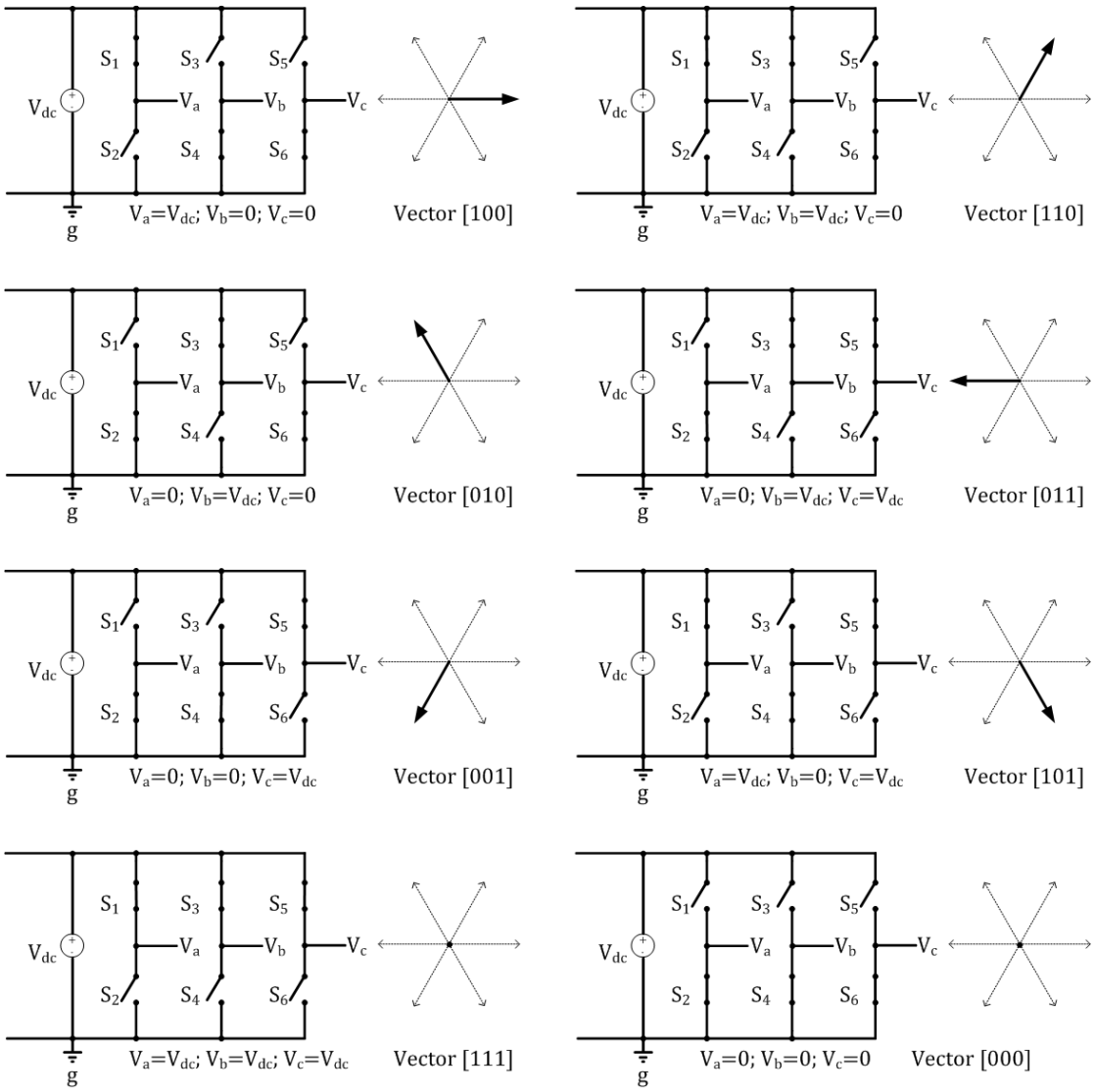


Figure 3.8 - The eight different switch states that the three phase inverter can assume.

It is clear that the reference voltage, $V_c^{\alpha\beta*}$, will fall in any of the six sectors shown in figure 3.8. Once it is known in which sector this vector falls, the projection of the vector onto the two closest realizable vectors can be calculated. In figure 3.9 the vector falls in sector 1.

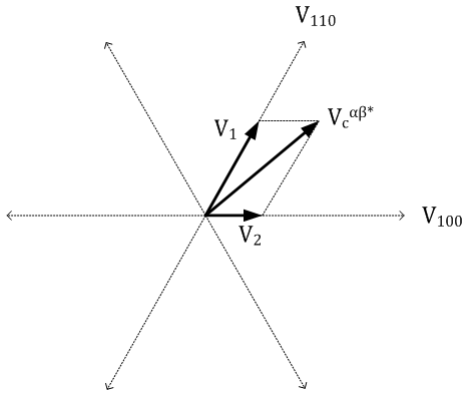


Figure 3.9 - The space-vector in sector I.

The fraction of the modulation period that is occupied by the two projections of the vector can be calculated as follows:

$$\delta_1 = \frac{|V_1|}{|V_{100}|} \qquad 3.10$$

$$\delta_2 = \frac{|V_2|}{|V_{110}|} \qquad 3.11$$

The sum of the fractions should be equal or less than one. Consequently the fraction of the modulation period that the zero-vector occupies is added. The sum of the fractions is shown by equation 3.12 where δ_3 is the fraction of the modulation period associated with the zero-vector.

$$\delta_1 + \delta_2 + \delta_3 = 1 \qquad 3.12$$

The exact same reasoning is applicable for other vector positions.

3.3 Dead-Time Compensation

3.3.1. Introduction

Dead time is associated with all switching inverters that incorporate some sort of half bridge configuration, as shown in figure 3.10, and it is simply unavoidable. Blanking time is inserted in the gating signals of switches S_1 and S_2 to ensure that

simultaneous conduction does not occur. The blanking time allows for the non-instantaneous turn-on and turn-off times of the switches.

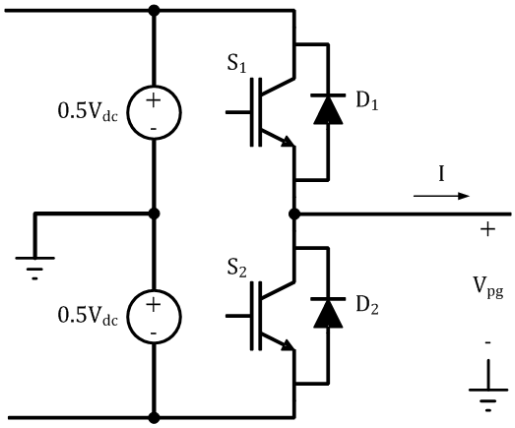


Figure 3.10 - The model of a single phase VSI as used to derive expressions for dead-time.

If both switches in a phase arm are on at the same time the DC-bus will be short circuited and a destructive current will flow through the switches causing them to fail. The amount of blanking time that will ensure safe operation is calculated from the specific switch parameters. These parameters include: turn-on delay time ($t_{d(on)}$), rise time (t_r), turn-off delay time ($t_{d(off)}$) and fall time (t_f). T_{on} is the sum of $t_{d(on)}$ and t_r and T_{off} is the sum of $t_{d(off)}$ and t_f. In figure 3.10 only a single phase arm is shown and the voltage, V_{pg}, refers to the phase to ground voltage, where p can be a, b or c.

Dead time refers to the combination of the above mentioned parameters and the blanking time. Figure 3.11 shows the ideal switching pattern and how the actual on and off times of each switch are affected by dead time. S_1^* and S_2^* are the ideal reference gate signals for switches S_1 and S_2. S_1 and S_2, in figure 3.11, are the gate signals for switches S_1 and S_2 with the required blanking time inserted.

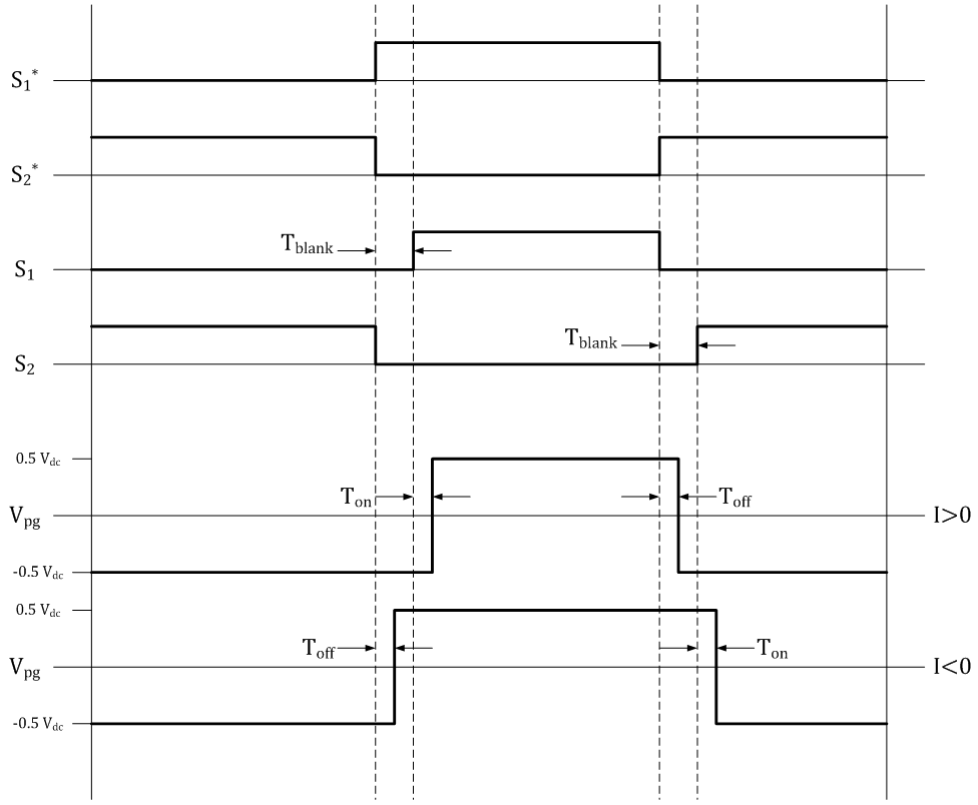


Figure 3.11 - Switching patterns.

Ideally the output voltage, V_{pg}, should be equal to +0.5 V_{dc} when switch S_1 is on and equal to -0.5 V_{dc} when switch S_2 is on. In practice this is not the case as the switches have finite turn-on and turn-off times. If only the output voltage is considered over a switching cycle and the transition voltages of the switches and diodes are ignored the output voltage can be calculated using figure 3.11.

When the output current is positive the switched output voltage, V_{pg}, is derived as follows. If S_2 is on the output voltage is -0.5 V_{dc}. S_2 is then commanded to turn off and is fully off after a certain turn-off time, T_{off}. The output current does not fall to zero instantaneously and continues to flow causing diode, D_2 to turn on and the output voltage to stay at -0.5 V_{dc}. S_1 is commanded to turn on and is fully on after a certain turn-on time, T_{on}. The output voltage then changes to +0.5 V_{dc}. S_1 is then commanded to turn off and is fully off after T_{off}. The output current continues to flow, causing D_2 to turn on and the output voltage to change to -0.5 V_{dc}.

The same approach is followed for conditions of negative output current. Once again, when S_2 is on, the output voltage is -0.5V_{dc}. When S_2 is commanded to turn off and is fully off after T_{off}, the current continues to flow, causing D_1 to turn on and

the output voltage to change to +0.5 V_{dc}. S_1 is commanded to turn on and is fully on after T_{on}.

The output voltage remains +0.5 V_{dc}. S_1 is then commanded to turn off and is fully off after T_{off}. The output current continues to flow, causing D_1 to turn on and the output voltage remains +0.5 V_{dc}.

When the current is positive, the time that S_1 is on is less than the ideal reference. Consequently a smaller output voltage is realized than the reference would suggest and therefore an error is made. A similar error is experienced when a negative current is flowing [16]. The effects and consequences of these errors are discussed in a following section.

This non-ideal dead-time does impede the performance of the inverter and should be quantified and compensated for to ensure an efficient and optimally functioning inverter.

3.3.2. Quantification

The error made during each switching period can be calculated for the two directions of output current. These are shown in equation 3.13 and 3.14, as calculated from the discussion in the previous section. The time that the switch is fully on compared to the ideal reference will give the dead time.

If I > 0:

$$t_{s1} = t_{s1}^{*} - (T_{blank} + T_{on} - T_{off}) \qquad 3.13$$

If I < 0:

$$t_{s1} = t_{s1}^{*} + (T_{blank} + T_{on} - T_{off}) \qquad 3.14$$

The term dead-time then refers to the error made in terms of the time that each switch is on. This error, defined as T_e, is shown in the above two equations and is given by equation 3.15.

$$T_e = T_{blank} + T_{on} - T_{off} \quad 3.15$$

The duty cycle error made due to dead-time is expressed as:

$$D_e = \text{sign}(I) \cdot \frac{T_e}{T_s} \quad 3.16$$

where, T_s is the switching period.

From the above it should be apparent that due to dead-time there is a bound on the range of switchable duty cycle. The implication is that when the duty cycle is above or below a certain level the switches will be unable to switch. These levels are given by the following equation 3.17.

$$\begin{aligned} D_{max} &= 1 - D_e \\ D_{min} &= D_e \end{aligned} \quad 3.17$$

When the duty cycle is within these constraints the type of compensation method is referred to as mode 1 and when it falls outside of these constraints the compensation method is referred to as mode 2. The precise compensating terms and their derivation are shown in appendix A for mode 2.

The error made during each switching period appears to be small or even negligible. However, the effect of the accumulated errors over a period of the fundamental system frequency is very noticeable. Some of the important issues arising from dead time are discussed in the following section.

3.3.3. Effects

The error in the output voltage as discussed above, directly leads to an error in the output current of the inverter. The maximum output voltage and current of the inverter is subsequently reduced. The implication is that a current reference set at the maximum converter current will not be realized, therefore reducing the converter's operating range.

The other less intuitive effect that dead time has is that of poor output waveform quality. Dead-time leads to the distortion of the output waveforms of the voltage and

consequently the output current, therefore introducing unwanted harmonic content which reduces the efficiency of the system [16] [17].

The above mentioned effects of dead-time are shown by the waveforms in figure 3.12.

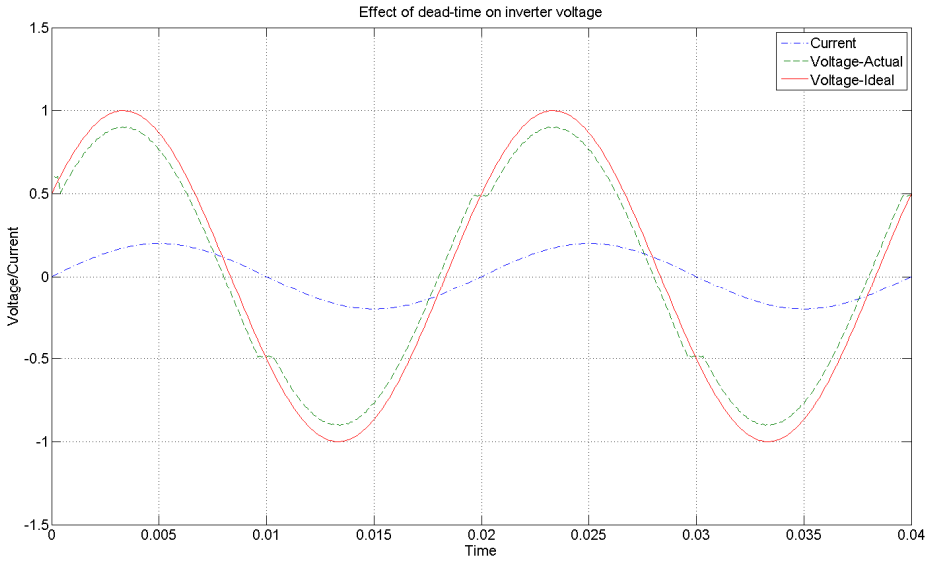


Figure 3.12 - The effect of dead-time on the inverter's output voltage is shown.

Depending on the application and operating conditions dead-time can lead to instability [18].

3.3.4. Dynamic Compensation

The turn-on and turn-off times are related to the specific IGBTs used in the inverter. On closer inspection of the specific IGBT datasheet it can be seen that these times are also dependent on the current being conducted by the device. Figure 3.13, which is extracted from the datasheet of the specific IGBT used in the inverter, shows that the switch times are dependent on the current through the switch [19].

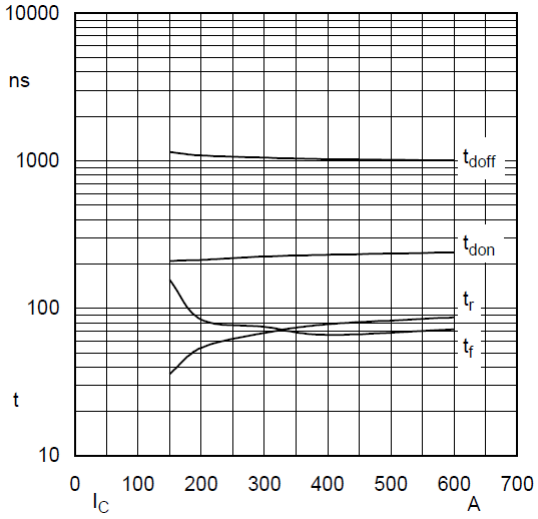


Figure 3.13 - The various times associated with an IGBT versus the current through the IGBT [19].

The IGBT modules used in higher power inverters are able to conduct large currents. These inverters are inevitably operated over the entire range and by simply assuming an average working point in a large operating range, will not deliver best results. This is especially true when the inverter is operating away from this average point and is verifiable when implemented. An attempt was subsequently made to incorporate this variation into the compensation method.

The inverter referred to in this thesis is able to generate current of 360 A_{RMS}. The graph shown in figure 3.13 does not show the various times of the switch for currents below 150 A. An attempt has been made to extrapolate these curves for the unspecified area. The extrapolation together with the matching compensating term is shown in figure 3.14. The compensation term, D_e, is the duty cycle error made due to dead-time as shown by equation 3.16.

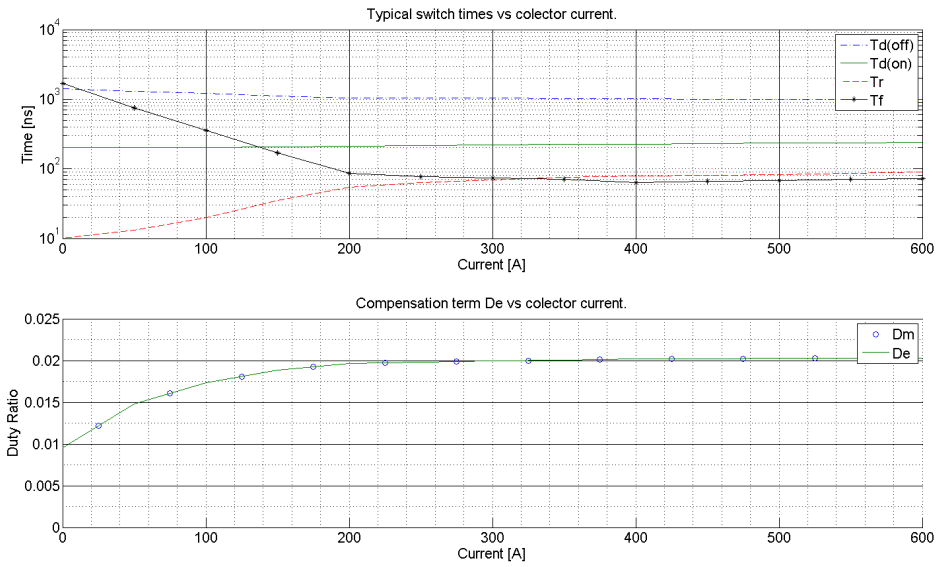


Figure 3.14 - TOP: The various times associated with an IGBT versus the current through the IGBT. BOTTOM: The duty cycle error caused as a result of the non-ideal switching times shown above.

The current range of the switch has been divided into 50 A intervals and the average D_e value is used to compensate. This reduces the effort necessary to determine the mathematical function of the D_e curve shown in figure 3.14 above. Figure 3.14 shows these averaged points denoted as D_m.

Using these averaged points over the operating range of the inverter instead of a single average value results in better performance over the entire operating range.

3.3.5. Implementing Methods

The literature suggests various methods to compensate for dead-time. Some methods require different functioning hardware to what was already available in the laboratory.

The selected method only requires the implementation of an algorithm in software. Another method that compensates using only a software algorithm calculates the error made in the converter output voltage and adds it to the reference before the duty cycles of each phase arm are calculated [15]. This method only reduces the amplitude error of the fundamental frequency component and does not attempt to reduce the dead-time induced harmonics.

From section 3.3.2 it is evident that the sign of the error term and therefore also that of the compensation term changes, based on the direction or sign of the output current. Figure 3.15 shows the typical switched output current of an inverter. The ripple on the current may cause multiple zero-crossings to be detected. The times at which these multiple crossings occur depend on the current ripple and the amplitude of the output current.

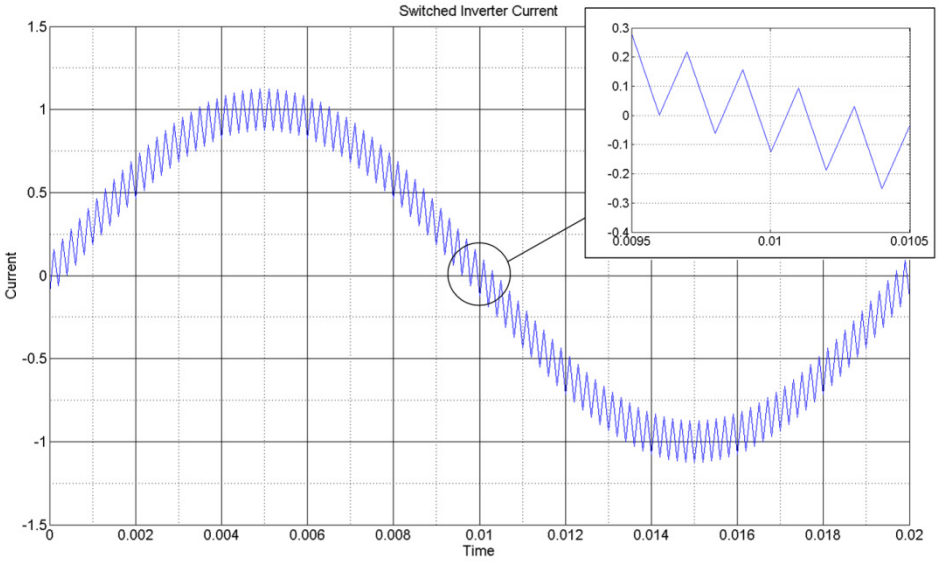


Figure 3.15 - A typical switched current.

In the case of compensation being done by using a fixed compensating term, the sign of the compensating term may change rapidly within the zero-crossing region. One method to resolve this problem is simply to implement no compensation in this region and is known as dead-zone dead-time compensation. Dead-zone dead-time compensation however causes unwanted harmonics on the voltage. Another method suggests using a slope or linearly scaled value in this region that reduces the effect of the sign change while still compensating [17].

The method implemented in this thesis is the one using a linear slope in the zero-crossing zone together with the dynamic compensation discussed in the previous section. The threshold that determines the linear compensating region is chosen based on the current ripple on the inverter's output current. The inverter with a LC output filter, with inductance value of L_f, has a ripple current given by equation 3.18 [20].

$$\Delta I_L \cong \frac{1}{8} \cdot \frac{V_{dc}}{L_f f_s} \qquad 3.18$$

The specific inverter's current ripple is calculated to be 50 A peak-peak and the threshold, I_{th}, on the average inverter current is set to 25 A. This means that if the average inverter current is below 25 A, compensation will be done with a linearly scaled value, D_{comp}, which is calculated as follows.

$$D_{comp} = D_e \cdot \frac{I}{I_{th}} \qquad 3.19$$

3.3.6. Performance

The two most important issues that are focussed on during the analysis of the dead-time compensation technique are firstly the correlation between the reference signal and the fundamental frequency component and secondly the harmonic content and THD.

The compensation methodology is verified using simulation software and ultimately by conducting experiments. As noted in a previous section the compensation method used in this thesis is the one incorporating a linear slope in the zero-crossing region of the current. A discussion of each method leading to the specific choice is given in chapter 6. The tabulated results of the various dead-time compensation methods are also shown and discussed in chapter 6.

3.4. Dead-Beat Current Control

The current controller discussed here is aimed at controlling the inverter such that any reference current will be realized at the output of the inverter. The necessity for this controller is discussed here, as well as the design and implementation thereof.

3.4.1. Introduction

The dead-beat, also referred to as predictive, current controller is derived using a very physical approach. The control algorithm is based on the voltage across and the current through the filter inductor. The relationship between the voltage and current together with the digital implementation of the controller form part of the derivation process. This process is discussed later in this section.

This controller essentially controls the inverter voltage such that a certain reference current is realized at the output. This is done by calculating the average inverter voltage at each control iteration that will realize the reference converter current at some time thereafter.

The digital implementation is also important. In the specific inverter the signals are measured at the beginning of the sample period. The control algorithm is then evaluated. The duty cycles are updated right at the end of the sample period after which the cycle is repeated.

The controller controls the inverter such that the reference current is realized at the inverter output. Outer control-loops that simply generate a reference current can easily be implemented with this current controller.

3.4.2. Design and Theory

The design of the dead-beat controller is done by examining a single-phase inverter and then expanding the result to the three-phase inverter by means of the Clarke transformation.

Figure 3.16 shows the single-phase VSI with output filter inductor and the series resistance of the filter inductor. In most designs the series resistance of the inductor is neglected due to its small resistance. Here it is used in the design and shown that it does not greatly affect the computing effort of the controller. Another reason for taking it into consideration is that it may have a significant impact on the output current in high power inverters. Since the current controller controls the current flowing in the inverters output filter inductor the filter capacitors are neglected and only the voltage at each end and the current through the inductor is considered.

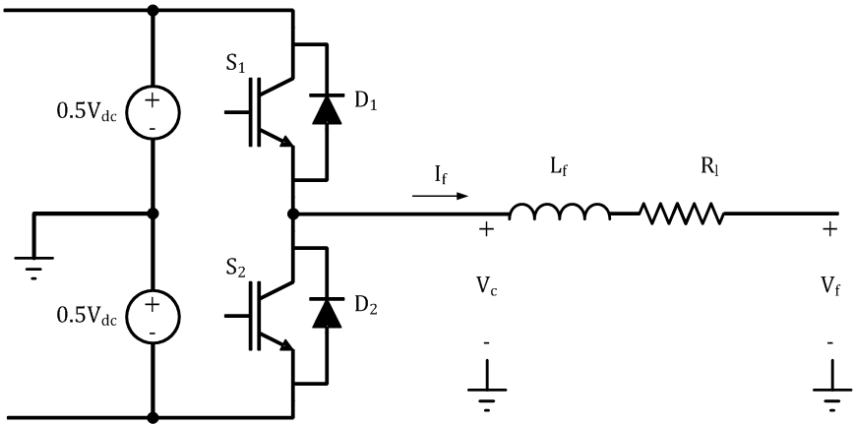


Figure 3.16 - A single phase-arm of the VSI used to derive the dead-beat controller.

The filter current is denoted by I_f, the filter voltage by V_f and the converter voltage by V_c. Considering Kirchhoff's voltage law leads to the following equation.

$$V_c(t) - V_f(t) = L_f \frac{dI_f(t)}{dt} + R_l I_f(t) \qquad 3.20$$

Taking the Laplace transform and rewriting the equation gives:

$$V_c(s) - V_f(s) - R_l I_f(s) = sL_f I_f(s) \qquad 3.21$$

Discretization is necessary to implement the controller digitally. Using the forward Euler method, where $s \rightarrow \frac{z-1}{T_s}$, and rewriting the equation in discrete time, by making use of z-transform properties, gives the following equations:

$$V_c(z) - V_f(z) - R_l I_f(z) = \frac{z-1}{T_s} L_f I_f(z) \qquad 3.22$$

$$V_c[k] - V_f[k] - R_l I_f[k] = \frac{L_f}{T_s}(I_f[k+1] - I_f[k]) \qquad 3.23$$

From equation 3.23 it can be seen that the inverter will generate a voltage, V_c, during period k that will realize the reference current at instant k+1. However the calculation of the voltage to be generated during this period is done during the same period and the duty cycles only updated at the end of the same period. The digital implementation of the controller and the finite computation time causes this delay. Essentially this means that calculations done in the current sample period will only take effect in the following sample period. Advancing equation 3.23 forward by one

sample period (k→k+1) will give an entire sample period to complete all computations. This advanced equation is shown below.

$$V_c[k+1] - V_f[k+1] - R_l I_f[k+1] = \frac{L_f}{T_s}(I_f[k+2] - I_f[k+1]) \qquad 3.24$$

From this equation it can be seen that the voltage to be generated by the inverter during the next period is calculated in the current period. The advanced equation solves the previous timing issue associated with the digital implementation and finite computation time. However now values such as $V_f[k+1]$ and $I_f[k+1]$ appear in the algorithm. These are obviously not known at instant k and some method of prediction might be needed to find the values.

$I_f[k+1]$ can be extracted from equation 3.23 and substituted into equation 3.24 to give equation 3.25.

$$\begin{aligned} V_c[k+1] = \frac{L_f}{T_s}\left(I_f[k+2] - \left(1 - \frac{R_l T_s}{L_f}\right)^2 I_f[k]\right) - \left(1 - \frac{R_l T_s}{L_f}\right) V_c[k] \\ + \left(1 - \frac{R_l T_s}{L_f}\right) V_f[k] + V_f[k+1] \end{aligned} \qquad 3.25$$

The only unknown value is the filter voltage at the following sample instant. A number of methods can be used to predict or estimate this value. A simple way, and the way it has been done in this thesis, is as follows. The filter voltage can be approximated by assuming that it varies slowly compared to the sampling rate. The phase can be predicted by knowing the sample frequency and simply rotating the filter voltage vector forward by 3.6° (one sample period). Another method suggests simply assuming that the filter voltage does not change much and using the current value as the predicted value ($V_f[k+1] \cong V_f[k]$) [15]. Both these methods require much less computational time and design effort than the estimators suggested by others [11]. Furthermore, estimators increase the order of the system and generally make the dead-beat controller's properties and the controlled system's stability more sensitive to parameter mismatches [15]. The value of $V_c[k+1]$, calculated in the previous control iteration, is used for $V_c[k]$ in the current control iteration.

The prediction makes the algorithm in equation 3.25 causal and all values are now known. $I_f[k+2]$ is the reference current at instant k, i.e. $I_f^*[k]$. At the beginning of the current sample period the control system samples the values required in equation

3.25 and calculates the voltage, $V_c[k+1]$, that the inverter needs to generate during the following sample period to make the inductor current error go to zero at instant k+2. The control algorithm implies a two-period delay.

The exact implementation of this controller is discussed in the following section.

3.4.3. Implementation

The dead-beat controller is implemented in the stationary reference frame. Using the αβ-notation, equation 3.25 is simply rewritten to give the following equation. The equation below is actually two separate equations, identical for α and β respectively, and is only shown in this compact form to minimize repetition.

$$\begin{aligned} V_c^{\alpha\beta}[k+1] = \frac{L_f}{T_s}\left(I_f^{\alpha\beta}[k+2] - \left(1 - \frac{R_l T_s}{L_f}\right)^2 I_f^{\alpha\beta}[k]\right) \\ - \left(1 - \frac{R_l T_s}{L_f}\right) V_c^{\alpha\beta}[k] + \left(1 - \frac{R_l T_s}{L_f}\right) V_f^{\alpha\beta}[k] + V_f^{\alpha\beta}[k+1] \end{aligned} \quad 3.26$$

The converter reference voltage, $V_c^{\alpha\beta*}[k] = V_c^{\alpha\beta}[k+1]$, is used in the SVPWM algorithm to generate the duty cycles of each phase-arm as discussed in section 3.2.3.

The robustness of the controller is something that needs to be known. The most obvious component that could influence the performance and stability of the controller is the system parameters. For this dead-beat controller these will be the filter inductance and the filter inductor's series resistance. As mentioned in the previous section the use of an estimator will result in the controller being more sensitive to parameter mismatches. It has been determined that the predictive controller is not very sensitive to a variation in the filter inductance. The controller is able to keep the system stable with mismatches of up to 100% in the filter inductance [15]. Parameter mismatches degrade the performance of the controller substantially, however stability is maintained. The variation in the series resistance is considered negligible as this is usually very small and is often completely omitted from the algorithm.

3.4.4. Delay Compensation

The single period delay caused by the finite computation time required to evaluate the control algorithm has been taken care of during the design of the control algorithm. Instead of the single period delay that is theoretically possible as given by equation 3.23, an additional single period delay is added to the controller during this compensating action. The result is a controller that has a two period delay. This means that the reference current at instant k will only be realized at instant k+2. Essentially this means that the current will lag the reference by two sample periods, which is 7.2° in the specific controller. By rotating the reference current-vector forward by 7.2° (two sample periods) the realized current will be exactly in phase with the initial reference current. This effectively takes care of the phase error made by the controller due to its double period delay.

Figure 3.17 shows the advanced reference, initial reference and the measured current from a Simplorer v8 simulation. Note that the measured current follows the initial reference very closely and that it lags the advanced reference by two sample periods.

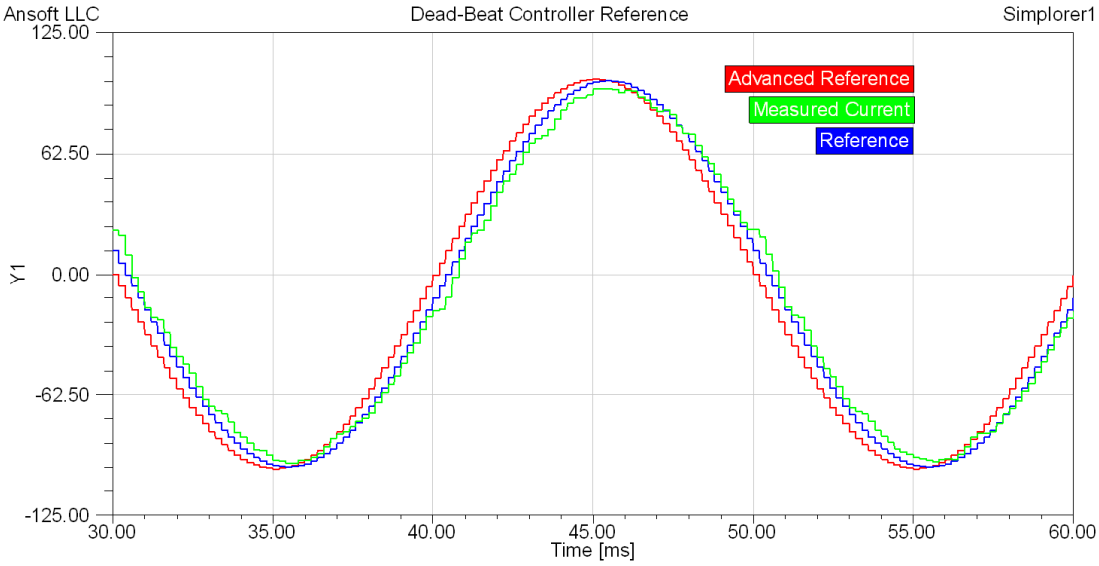


Figure 3.17 - The currents involved with the dead-beat current controller.

3.5. DC-bus Controller

The DC-bus controller discussed here is aimed at regulating the DC-bus voltage at a specific voltage level. The reason is discussed and a suitable PI-controller is designed.

3.5.1. Introduction

For the specific VSI, used primarily as an UPS, the battery should be kept fully charged at all times. This requires operating the inverter as an active rectifier and means that active power is drawn from the AC network.

When a VSI is used only for reactive compensation (only absorbing or supplying reactive power) it is advisable to draw a small amount of active power from the electricity network to compensate for the losses of the inverter [13].

The two abovementioned needs for drawing active power from the electricity network necessitate the design and implementation of a DC-bus controller.

3.5.2. Design and Theory

An outer voltage control-loop is used to regulate the DC-bus. The aim of this controller is simply to adjust the amplitude of the inverter current so that the required voltage level is maintained. To prevent input-current distortion, the DC voltage-ripple needs to be filtered by the controller [15]. Limiting the controller bandwidth to typically one-tenth of the fundamental system frequency solves this problem [15]. Usually this is achieved by means of a PI-controller that is easily designed due to the non-stringent design specifications. A model of the DC-bus is needed for this design and is derived by considering the components of the DC-bus. The DC-bus can consist of various components, depending on the application. The VSI considered in this thesis is shown in figure 3.3 where a DC-bus consisting of capacitors and a battery is presented. The capacitors are permanently connected and the battery is connected by means of a contactor. A transfer function for this DC-bus, shown in figure 3.18, is derived in the following section.

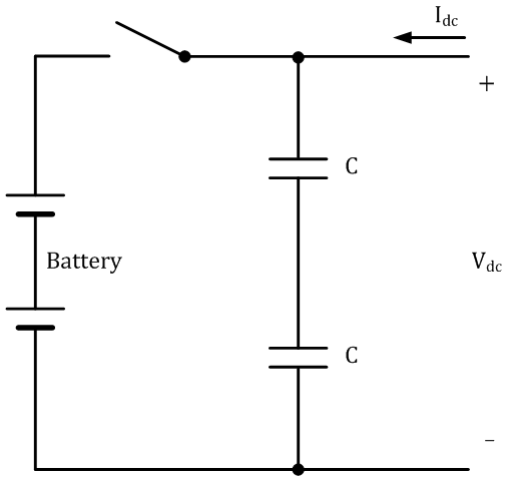


Figure 3.18 - The DC-bus connected to the VSI.

An important issue to take into consideration from the start is the physical functioning of the system as a whole. When the inverter initially starts up, the battery will be disconnected from the inverter. Once the three-phase supply is connected the capacitors will be passively charged through the diodes incorporated in the IGBTs. The inverter then starts to boost the DC-bus voltage to the same level as the battery voltage before connecting the battery to the inverter. The inverter is then allowed to charge the DC-bus further to the desired level.

To reduce the design and implementation effort the use of a single controller for both these cases would be ideal. A single controller that is stable for two different DC-bus configurations is therefore required.

An equivalent circuit diagram of the DC-bus can be drawn and then transformed to the s-domain to find the transfer function for the two different situations. This is shown in figure 3.19.

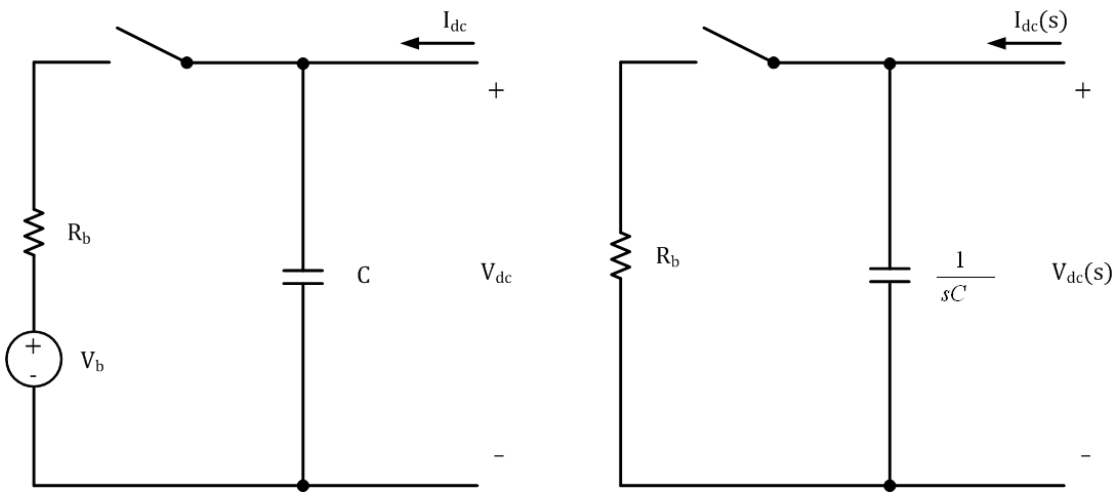


Figure 3.19 – LEFT: The equivalent circuit of the DC-bus. RIGHT: The s-domain equivalent circuit of the DC-bus.

The battery, consisting of 66, 12 V Deltec-1250 lead-acid batteries connected in series, is modelled as an ideal voltage source with an equivalent internal resistance. The average internal resistance is determined from the battery datasheet. This average resistance and battery potential is multiplied by the number of batteries to get the total series resistance of the battery, R_b, and the total battery voltage, V_b. The bus capacitance is 23.5 mF and the battery resistance is 0.37 Ω.

The transfer function defining the DC-bus for the two cases can be determined as follows. When the battery is disconnected from the DC-bus of the inverter the transfer function is:

$$H_{case_1}(s) = \frac{V_{dc}(s)}{I_{dc}(s)} = \frac{1}{sC} \tag{3.27}$$

When the battery is connected to the inverter the transfer function is:

$$H_{case_2}(s) = \frac{V_{dc}(s)}{I_{dc}(s)} = R_b || \frac{1}{sC} = \frac{R_b}{1 + sCR_b} \tag{3.28}$$

The inverter is used mostly with the battery connected and for this reason the design is first done and optimized for the second case. The designed controller will then be tested for stability and functionality for the first case. The control-loop is shown in figure 3.20.

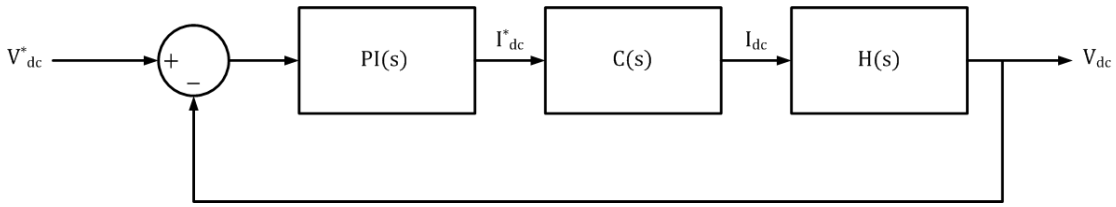


Figure 3.20 - The control-loop of the DC-bus controller.

The PI-controller transfer function is shown in equation 3.29 below.

$$\mathrm{PI(s)} = \mathrm{K_p} + \frac{\mathrm{K_i}}{\mathrm{s}} \tag{3.29}$$

The output of the PI-controller is a DC current. This current is used as a reference current for the current controller, which in turn will control the inverter such that it generates the required current. The exact implementation of this loop is discussed later in this section. The design of this PI-controller is done by only considering the DC side of the inverter.

The current controller is modelled as a pure two sample period delay with unity gain. This is done by using a first-order Padé approximation. The first-order Padé approximation of the current controller is shown in equation 3.30 [15].

$$\mathrm{C(s)} = \frac{\mathrm{I_{dc}(s)}}{\mathrm{I^*_{dc}(s)}} = \frac{1 - \mathrm{sT_s}}{1 + \mathrm{sT_s}} \tag{3.30}$$

The closed-loop transfer function of the controller, as depicted in figure 3.20, is calculated and shown in the following equation.

$$\frac{\mathrm{V_{dc}(s)}}{\mathrm{V^*_{dc}(s)}} = \frac{\mathrm{PI(s)C(s)H(s)}}{1 + \mathrm{PI(s)C(s)H(s)}} \tag{3.31}$$

The DC-bus transfer function, H(s), can be changed for either of the two cases discussed above. For reasons discussed above the initial design is done for the second case. To draw the root-locus and design the controller, PI(s), the characteristic equation, shown in equation 3.32, needs to be evaluated.

$$1 + \mathrm{PI(s)C(s)H(s)} = 0 \tag{3.32}$$

Substituting in the different transfer functions and simplifying the characteristic equation to the standard form gives equation 3.33.

$$\frac{-\frac{K_p}{C}\left(s+\frac{K_i}{K_p}\right)\left(s-\frac{1}{T_s}\right)}{s\left(s+\frac{1}{T_s}\right)\left(s+\frac{1}{CR_b}\right)}=-1 \qquad 3.33$$

The known poles and zeros can be plotted in the s-plane and the root-locus constructed. This is shown in figure 3.21.

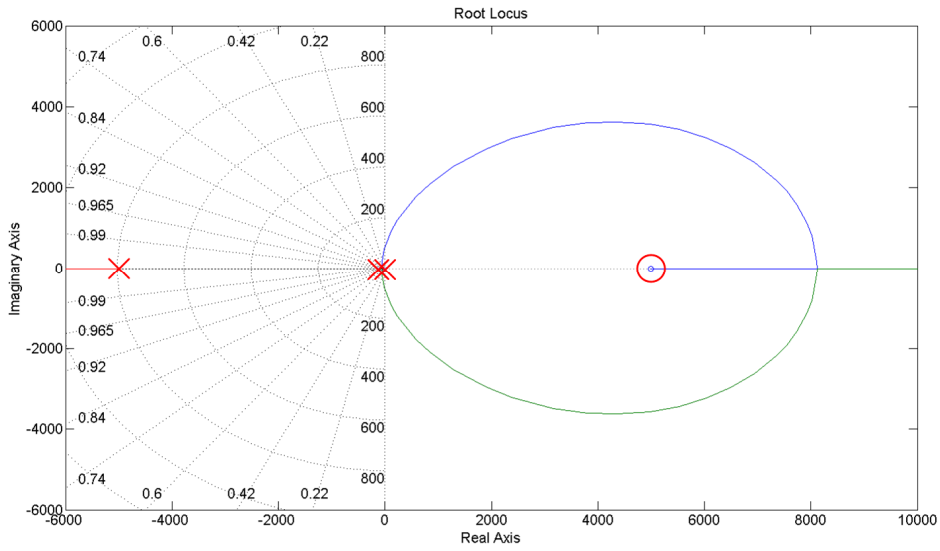


Figure 3.21 - The known poles and zeros of the system are placed and the root locus constructed.

The zero located at $-\frac{K_i}{K_p}$ can be placed anywhere on the real axis. Taking the general root-locus rules into consideration it can be seen that by placing the zero on the pole at $\frac{-1}{CR_b}$ the root locus can be brought further to the left side of the s-plane. This means a more stable system can be achieved by choosing the gain appropriately. The root-locus after pole-zero cancellation is shown in figure 3.22 below.

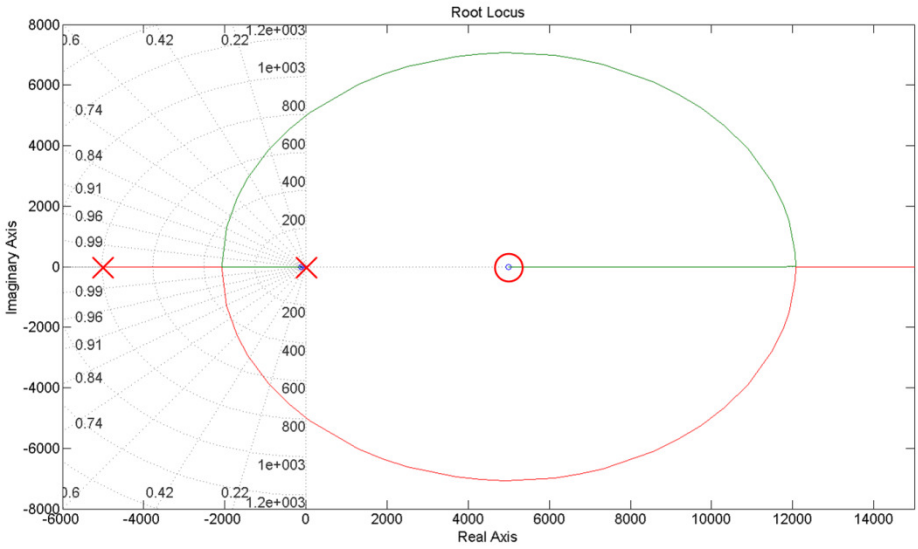


Figure 3.22 - The poles and zeros are placed and the root locus constructed after pole-zero cancellation.

The simplified characteristic equation after the pole-zero cancellation is shown in equation 3.34.

$$\frac{-\frac{K_p}{C}\left(s-\frac{1}{T_s}\right)}{s\left(s+\frac{1}{T_s}\right)}=-1 \qquad 3.34$$

The gain of the loop is then determined by evaluating the magnitude of equation 3.34 at the desired frequency. This is done by substituting $s \rightarrow j\omega$ and setting ω to $2\pi f_{cl}$, where f_{cl} is the desired closed-loop frequency, the unknown parameter, K_p, can be calculated. This is shown in equation 3.35.

$$\frac{K_p}{C}\cdot\frac{\sqrt{(2\pi f_{cl})^2+\left(-\frac{1}{T_s}\right)^2}}{\sqrt{(2\pi f_{cl})^2+\left(\frac{1}{T_s}\right)^2}\cdot\sqrt{(2\pi f_{cl})^2}}=1 \qquad 3.35$$

Evaluating this equation results in a value for $K_p = 0.74$. Substituting this value into the equation for the zero, $-\frac{K_i}{K_p}=\frac{-1}{CR_b}$, the value for K_i is found to be 84.9. The response of the system to a step input is determined with MATLAB and shown in

figure 3.23. The 90% rise-time is 69 ms and the bandwidth of the system is confirmed to be 5 Hz.

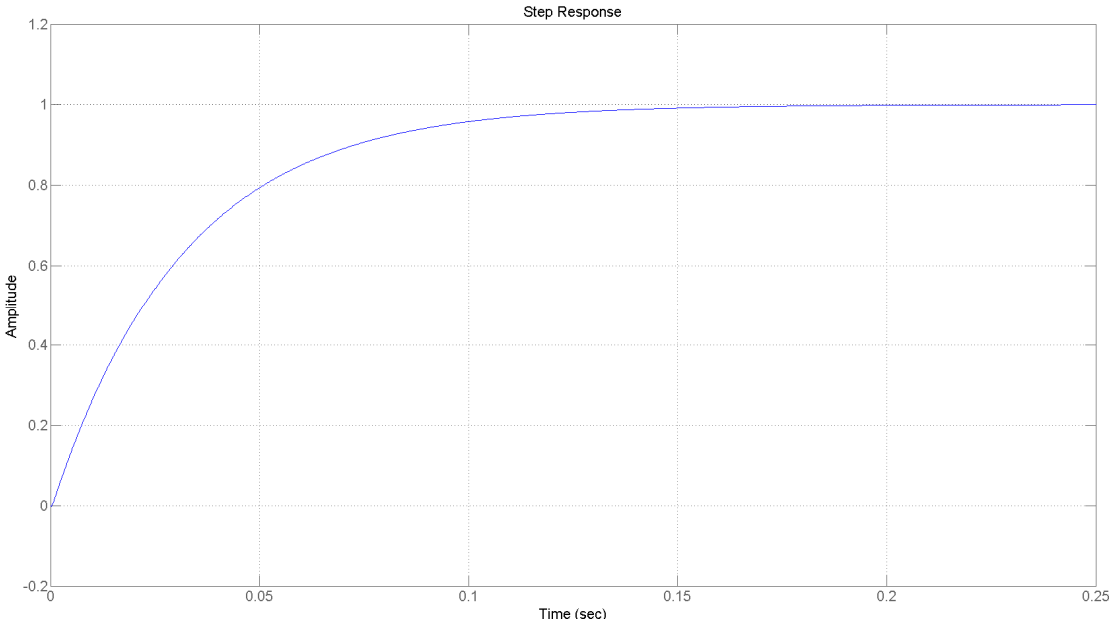


Figure 3.23 - The response of the system to a unit step change.

The stability of the designed controller should also be determined for the first case. This is done by determining the characteristic equation and constructing the root-locus for this case and examining the positions of the closed-loop poles. If all the poles are on the left side of the s-plane the system will be stable. The step response should also be examined to ensure that it has a satisfactory response. The characteristic equation for the system resulting from the first case is shown in equation 3.36.

$$\frac{-\frac{K_p}{C}\left(s+\frac{K_i}{K_p}\right)\left(s-\frac{1}{T_s}\right)}{s^2\left(s+\frac{1}{T_s}\right)}=-1 \qquad 3.36$$

Constructing the root-locus yields closed-loop poles in the left half of the s-plane. The system is therefore stable during this operating state. The step-response of the system, for the first case, is shown in figure 3.24. The designed step-response would not be acceptable for continuous use due to the large overshoot.

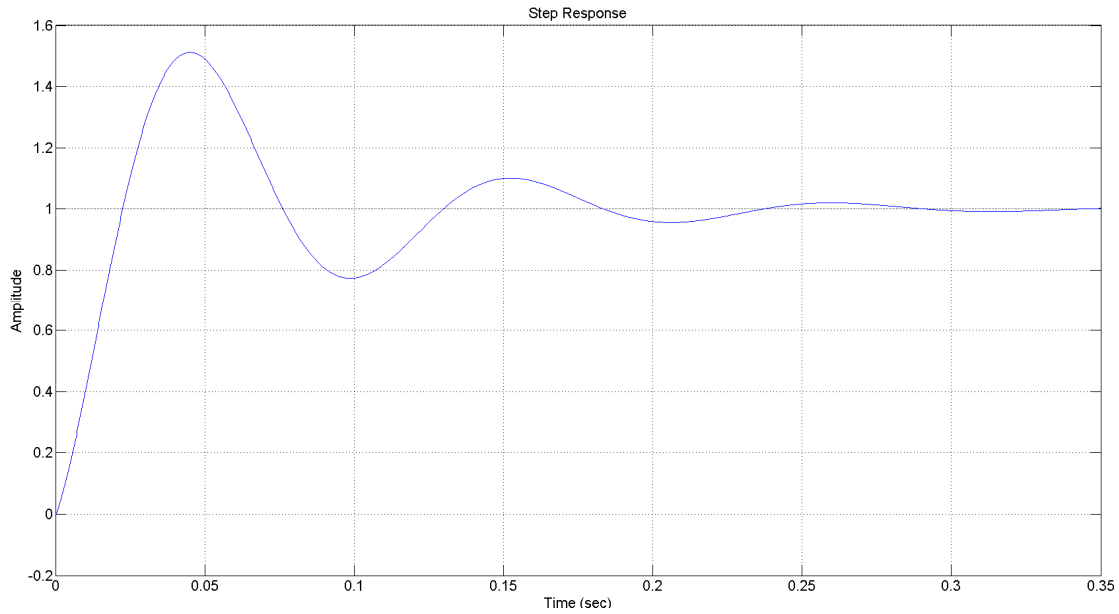


Figure 3.24 – The response of the system to a unit step change.

The implementation of various other necessary safety measures will prevent the overshoot to a value that is safe for the inverter. These aspects are discussed in the next section.

3.5.3. Implementation

The design of the controller is done in the s-domain, considering only the DC-bus, and needs to be implemented digitally. The various issues regarding the implementation of this controller are discussed in this section.

To implement the s-domain PI-controller, PI(s) as shown in equation 3.37, digitally, it needs to be discretisized. This is done using the backward Euler method.

$$\mathrm{PI}(s) = \frac{I_{dc}(s)}{V_{dc\,e}(s)} = K_p + \frac{K_i}{s} \qquad 3.37$$

The proportional and integral terms can be divided into two separate algorithms as shown in equations 3.38 and 3.39. This is also graphically shown as two parallel branches by figure 3.25.

$$I_{dc\,p}(s) = K_p V_{dc\,e}(s) \qquad 3.38$$

$$I_{dc\,i}(s) = \frac{K_i}{s} V_{dc\,e}(s) \qquad 3.39$$

where, $I_{dc\,p}$ and $I_{dc\,i}$ are the proportional and integral terms as generated by the controller.

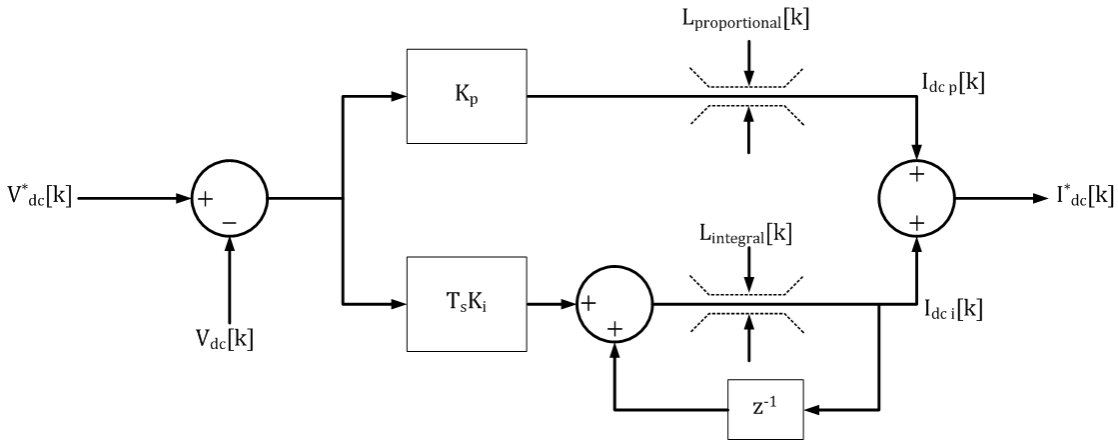


Figure 3.25 - The digital control-loop depicted as two parallel branches. The top showing the proportional branch and the bottom the integral branch.

Using the backward Euler method, where $s \rightarrow \frac{z-1}{zT_s}$, and rewriting the equation in discrete time, by making use of z-transform properties, leads to the following two equations.

$$I_{dc\,p}[k] = K_p V_{dc\,e}[k] \qquad 3.40$$

$$I_{dc\,i}[k+1] = I_{dc\,i}[k] + K_i T_s V_{dc\,e}[k+1] \qquad 3.41$$

Writing equation 3.41 back one sample period eliminates the unknown values and gives an expression for the correct integral term.

$$I_{dc\,i}[k] = I_{dc\,i}[k-1] + K_i T_s V_{dc\,e}[k] \qquad 3.42$$

Equations 3.40 and 3.42 can be implemented directly in code on the DSP. Adding the proportional and integral terms gives the total DC reference current.

As discussed in section 3.3 the current controller controls the AC current of the inverter. The relationship between the DC and AC current is required to transform the DC reference current to an equivalent AC reference current.

This relationship can easily be obtained by considering the power at the AC and DC sides of the inverter. Assuming that losses in the inverter are negligible the power at the DC side must equal the power at the AC side, as shown in equation 3.43. To get the AC power in the stationary reference frame the $\sqrt{\frac{2}{3}}$ relationship between the space-vector magnitude and the three-phase quantity is used.

$$P_{ac} = V_{3\varphi} I_{3\varphi} = \left(\frac{1}{\sqrt{\frac{2}{3}}}\right)^2 V^{\alpha\beta} I^{\alpha\beta} = V_{dc} I_{dc} = P_{dc} \qquad 3.43$$

Manipulating this equation yields the ratio between the DC current and the AC current in the stationary reference frame.

$$\frac{I^{\alpha\beta}}{I_{dc}} = \left(\sqrt{\frac{2}{3}}\right)^2 \frac{V_{dc}}{V^{\alpha\beta}} \qquad 3.44$$

By using the relationship in equation 3.44 the output of the DC-bus PI-controller is transformed to the equivalent space-vector AC current.

To reduce computations the relationship can be approximated to be constant. This is done by assuming the ratio between the three-phase voltage and the DC voltage is constant. For the specific case this ratio is $\frac{800}{400} = 2$. The relationship is then reduced to the constant value shown in equation 3.45.

$$\frac{I^{\alpha\beta}}{I_{dc}} = 2 \cdot \sqrt{\frac{2}{3}} \qquad 3.45$$

The integral action of the PI-controller successfully takes care of the error caused when the ratio between the three-phase voltage and DC-bus voltage is not exactly equal to 2.

As shown by figure 3.25 the output of each of the branches of the controller is clamped at a certain value. The reason for this is firstly to limit the maximum reference current generated by the controller, and secondly to implement an integral anti-windup function. The integral anti-windup functionality prevents the integral term

from becoming infinitely large and subsequently prevents the problems associated with this windup from occurring.

The most common issue associated with the integral term becoming very large is that is takes a lot of time to change to a different value if a step change in the input occurs. When a new set point is reached a transient can be generated by the controller being very far from steady state [15].

If the integral branch's output limit is determined based on the difference between the maximum current limit and the output of the proportional branch a dynamically limited integral output is achieved. Slightly more computation time is required for this method, but it will ensure that the integral component is always much closer to steady-state.

For this method to work correctly the proportional term should be limited to the maximum allowed DC reference current before the integral limit is calculated.

The integration limit is calculated as shown in equation 3.46.

$$\left|L_{integral}[k]\right| = I^{*}_{dc(max)} - \left|I_{dc\,p}[k]\right| \qquad 3.46$$

where, $L_{integral}$ is the integral limit,

$I^{*}_{dc(max)}$ is the maximum allowed DC reference current and

$I_{dc\,p}$ is the proportional output term.

The total reference current is calculated by the summation of the proportional and integral terms. With this anti-windup algorithm the final output of the controller does not need not be limited as the sum of both terms will always be less than or equal to the maximum allowed reference.

When the inverter is switched on initially the current limit is ramped up linearly over 100 ms to limit any start-up over-voltage transients.

The variation of the current limit, the implementation of an integral anti-windup function and the non-zero initial DC-bus voltage are the reasons that the PI-

controller, designed in section 3.5.2, works well despite it showing a large overshoot with a step input.

3.5.4. Performance

The only result that is important to discuss is the response of the controller to a step change in reference voltage for the case when the battery is connected to the inverter's DC-bus. A step-change in the reference voltage from 790 V to 800 V at 80 ms is shown in figure 3.26. Only a small step is considered as the controller easily reaches the predefined current limit. Once this limit is reached the controller remains at this maximum current until the voltage starts to change.

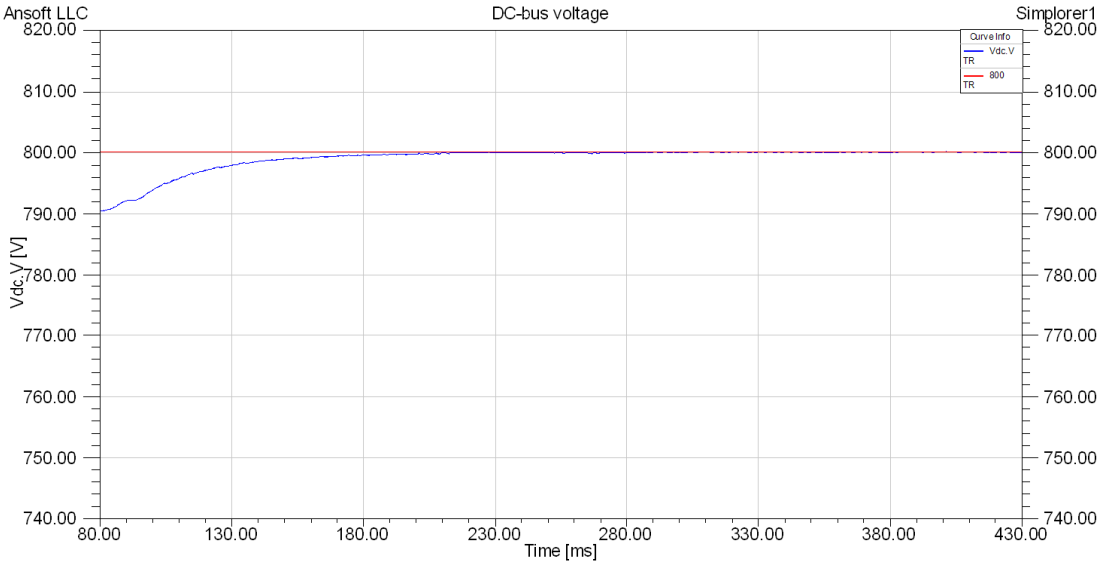


Figure 3.26 - The DC-bus voltage during a step change in the reference voltage.

As discussed previously the system is expected to show an overshoot when the battery is disconnected. The battery is only disconnected during the start-up procedure of the inverter and various other necessary measures ensure that the system does not experience an overshoot which may have disastrous consequences for the DC-bus capacitors.

When the inverter starts the bus charges passively through the diodes that are parallel to the IGBTs. After that the inverter is allowed to start switching and the reference voltage is gradually increased until the battery voltage is reached. When this level is reached the battery is connected and the reference voltage is set to the

desired level. During this start-up procedure the current limit on the controller is also gradually increased to the maximum.

The system will only be in this state during the start-up procedure. The existing controller satisfies all requirements since, together with all other measures, it ensures the safe operation of the inverter.

3.6. Conclusion

The basic operation of the VSI has been discussed. The various reference frames that can be used to implement control for the three-phase VSI were shown and discussed. Dead-time was discussed and the effect thereof shown. A suitable compensation technique was chosen and implemented to adequately compensate for the dead-time.

A suitable current controller was designed and implemented on the VSI. The current controller forms the inner control-loop of the inverter. Other outer or external control-loops can interface with this current controller.

A controller has also been designed and implemented to regulate the DC-bus at a certain reference voltage.

The basic operation of the VSI is now known and the basis set for the additional control that is to be implemented. This is discussed in chapters 4 and 5.

Chapter 4: Shunt Connected VSI for Dip Mitigation

In this chapter the application of a VSI for the mitigation of voltage dips is discussed. A brief introduction to the operation of the VSI and the conditions under which it operates are given and the design and implementation of a suitable control algorithm are discussed in detail.

4.1. Introduction

The aim in this chapter is to design and implement a control algorithm that will enable the VSI to compensate for voltage dips by means of reactive power only. A shunt connected VSI is used. The VSI, connected in shunt to a feeder, is shown in figure 4.1. The figure shows the feeder from the point where it connects to the grid to the point at which the load is connected. The VSI is connected in shunt with the load.

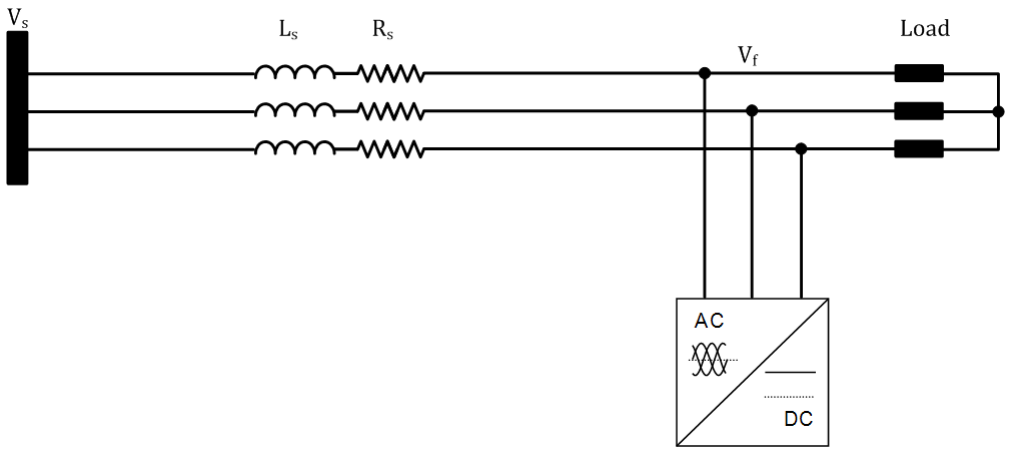


Figure 4.1 - A feeder from the grid, V_s, to the load.

As discussed in detail in section 2.4, the shunt VSI is used to load the transmission-line with the appropriate reactive load that will correct the voltage magnitude. The "load" is not an actual load but rather a simulated load meaning that the inverter is supplying or absorbing reactive power to or from the transmission-line. For this to happen the inverter must be able to generate reactive power and as will be seen in the next section, this is achieved by generating a reactive current.

4.2. VSI (VAR Generation)

The VSI can be controlled in such a way that it can generate a leading or lagging current with respect to the voltage at its output. Consider the inductor from the output filter shown in figure 4.2. Note that the direction of current flow is out of the inverter.

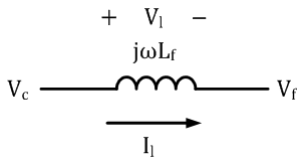


Figure 4.2 - The inductor in the output filter of the VSI.

If the generated voltage, V_c, is kept in phase with the voltage, V_f, and only its magnitude is varied then the result is a voltage, V_l, across the inductor that is either in phase with V_f and V_c or 180° out of phase with V_f and V_c. The current I_l will be lagging the voltage V_l by 90° and will either lead or lag V_f by 90° depending on the phase relationship of V_l and V_f. This is depicted in figure 4.3 below. If V_c is larger than V_f then I_l lags V_f and when V_c is smaller that V_f then I_l leads V_f.

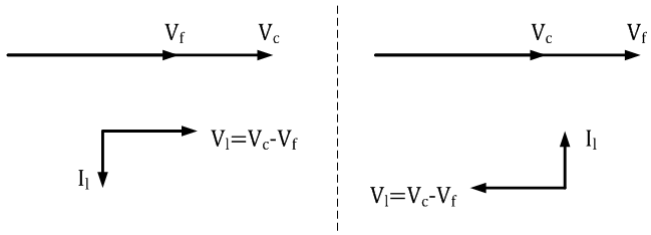


Figure 4.3 - The converter voltage, V_c, with respect to the output voltage, V_f. LEFT: The inverter generating a lagging current. RIGHT: The inverter generating a leading current.

When the inverter generates a current leading V_f the VSI can be seen as an inductive load on the line and when it generates a current lagging V_f it can be seen as a capacitive load. This is the opposite of what is expected but is only due to the chosen direction of current flow. In terms of the direction chosen to be positive for the inverter current a capacitive current has a positive sign and an inductive current has a negative sign.

By varying the amplitude of V_c with respect to the amplitude of V_f a variable amount of reactive power can be generated by the VSI. The ability of a VSI to generate a variable amount of reactive power makes it ideal for regulating voltage accurately.

It is recommended that a small amount of real power be drawn by the inverter to counter the losses in the inverter [21] [13]. The implementation of this algorithm is discussed in section 3.5. If the amount of active power drawn by the inverter is negligible compared to the total power rating of the inverter, as it is in many cases, the maximum reactive power available from the inverter is equal to the maximum inverter rating.

4.3. System Overview

In this chapter the impedance of each phase of the three-phase transmission-line is considered to be identical. Due to the routing of the lines they will generally be the same length. The transmission-line considered is a relatively short feeder and is modelled by a series combination of inductance and resistance. The inductance and series resistance of each line is considered to be the same. The capacitance of short transmission-lines is generally not taken into account [22].

Only balanced voltage dips are considered. This, together with the balanced transmission-line, means that the reactive load that will correct the voltage amplitude needs to be balanced as well. Since the inverter is a reactive load it means that the reactive current produced should be balanced.

A single-phase diagram of the system is shown in figure 4.4. Only reactive components are shown in this diagram because only reactive current will be controlled by the voltage controller. The figure shows the feeder from the point where it connects to the grid, denoted by V_s. It shows the total line inductance, denoted by L_s. The point at which the load is connected and also the voltage that will be regulated is denoted by V_f. The capacitors C_f form part of the inverter's output filter. These capacitors are there to absorb the high frequency switching currents and prevent them from being injected into the system.

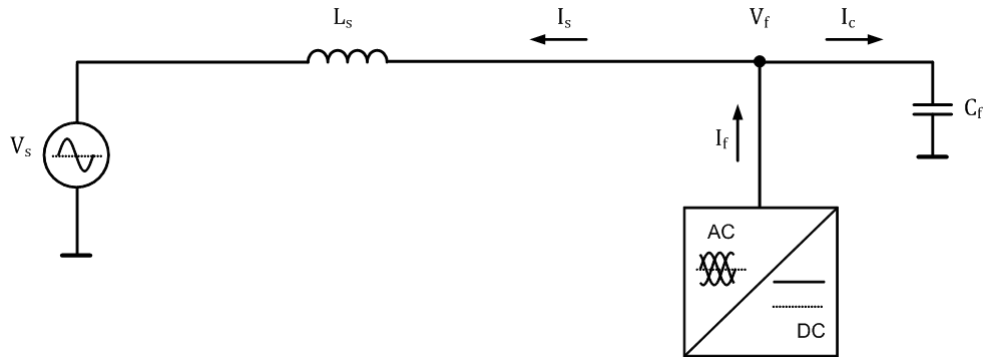


Figure 4.4 - A single-phase diagram of the system showing the directions and names of currents and components.

The system impedance may vary greatly due to load variation and will have an influence on the controller. For this reason the controller is designed for the maximum system impedance. This essentially means neglecting all components that are not permanently connected to the transmission-line and that only the transmission-line impedance is considered. The grid is assumed to have zero-impedance.

On closer inspection it is seen that the filter capacitors of the inverter are also permanently connected to the transmission-line and can therefore also be taken into consideration when determining the system impedance. Figure 4.5 shows the system for the maximum impedance calculation and is depicted as a control diagram. Note that the load does not form part of the diagram as it may not be constant. The maximum line inductance is used to calculate the impedance X_s. X_c is the filter capacitor impedance calculated as $\frac{1}{2\pi f C_f}$.

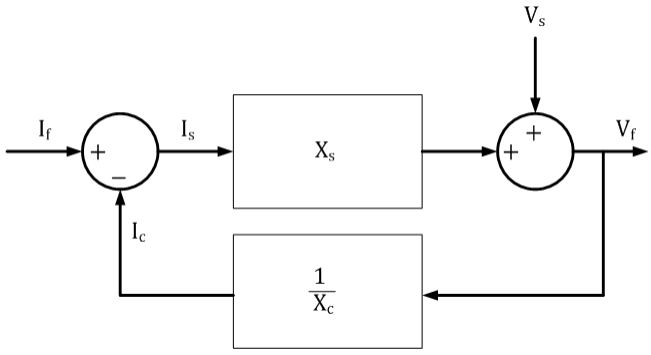


Figure 4.5 - A control diagram showing the system with a maximum impedance.

4.4. Controller Overview

The controller that will regulate the filter voltage is implemented in an outer voltage control-loop with the current control-loop still forming the inner loop. Figure 4.6 depicts this basic control diagram.

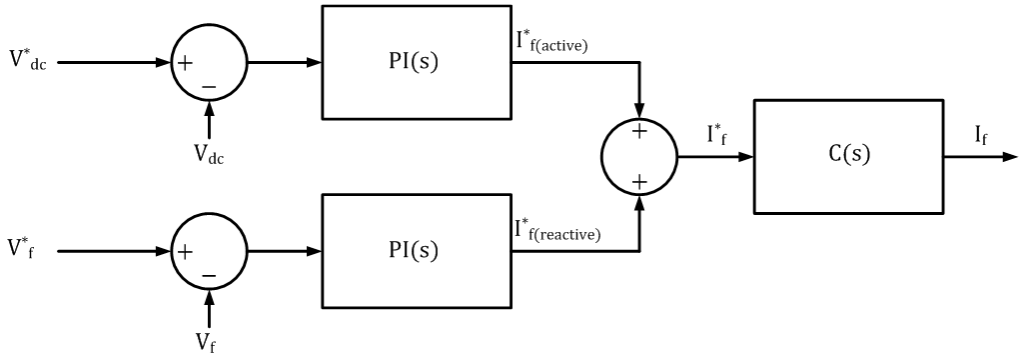


Figure 4.6 - The control diagram of the VSI showing the relation of the various control-loops and controllers.

The basic form of the voltage-loop is shown in figure 4.7.

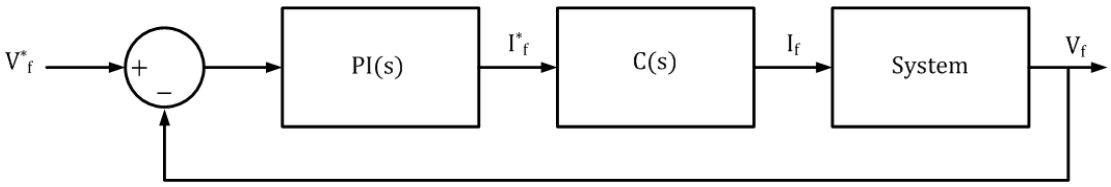


Figure 4.7 - A control diagram showing the voltage-loop.

The design of the controller in the outer voltage loop is described in a later section in this chapter and only the basic functioning of the control loop is discussed here. Only reactive components and currents are considered for control, analysis and design. Therefore, I_f denotes the reactive filter current.

From the control diagram it can be seen that the voltage controller generates a reference current based on the voltage error. The current loop ensures that the reference current is realized at the inverter output so that the voltage error can be eliminated. As noted in a previous section the reactive current should be balanced between the three phases. The balanced reactive current that the inverter generates can be represented by a space vector as shown in figure 4.8. This space vector has a constant magnitude, is 90° out of phase with the voltage and rotates at the

fundamental system frequency. The tip of the vector forms a circular path as it rotates in the αβ-plane.

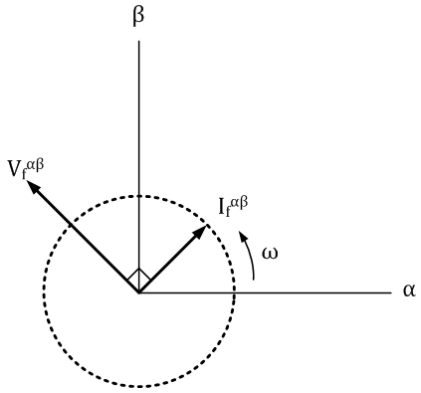


Figure 4.8 - The relationship of the voltage and reactive current space vectors depicted in the stationary reference frame.

The phase of the reference current is known since it is always 90° out of phase with the voltage. The current depicted in figure 4.8 realizes a capacitive load on the transmission line. The counterintuitive representation is due to the chosen current direction in the specific inverter. The capacitive current is associated with the filter voltage being lower than the reference and vice versa. With the phase of the reference current known only the magnitude is required to generate a suitable reference current. This is easily done by considering the space-vector representation of the three-phase filter voltage.

The voltage error is simply calculated by calculating the space-vector magnitude and comparing it to the reference magnitude. The reference magnitude for the filter voltage space-vector is as shown in equation 4.1. This is derived from the relationship shown in section 3.2.1.

$$\left|V_f^{\alpha\beta*}\right| = 400 \qquad 4.1$$

The error voltage is defined as the difference between this reference magnitude and the measured magnitude. The voltage error can be either positive or negative and the sign of the error is used to determine whether the reactive current should be leading or lagging the voltage by 90°.

The voltage controller consists of a PI-controller, shown by equation 4.2. This controller determines the sign and magnitude of the reactive current based on the voltage error input.

$$\mathrm{PI}(s) = \mathrm{K_p} + \frac{\mathrm{K_i}}{s} \qquad 4.2$$

Using a unit space-vector and simply multiplying it with the output of the PI-controller, which may be positive or negative, will give the correct current space-vector.

The current-controller and the inverter form part of the loop. These components are depicted as the current-loop in the control diagram. The current-loop is modelled as a pure delay with unity gain based on the discussion of dead-time and delay compensation in sections 3.3 and 3.4. This is done using the same method as with the DC-bus controller in section 3.5 and is shown in equation 4.3.

$$\mathrm{C}(s) = \frac{\mathrm{I_f}(s)}{\mathrm{I_f^*}(s)} = \frac{1 - s\mathrm{T_s}}{1 + s\mathrm{T_s}} \qquad 4.3$$

A regulation slope is introduced that varies the reference voltage, as the inverter's output current varies, lowering the reference voltage as the capacitive current increases and raising the reference as the inductive current increases. A regulation slope ensures an extended linear operating range and a better defined operating point for the inverter [13]. The regulation slope also enforces automatic load sharing between static-compensators and other voltage regulating devices employed on the transmission-line [13].

A typical VI-curve of a VSI is shown in figure 4.9. The slope induced by the regulation slope is also shown. This regulation slope is generally chosen to be in the range of 1 % to 5 % [13]. The current is limited by the maximum current rating of the VSI, while the minimum voltage is limited by the minimum synchronisation voltage of the controller.

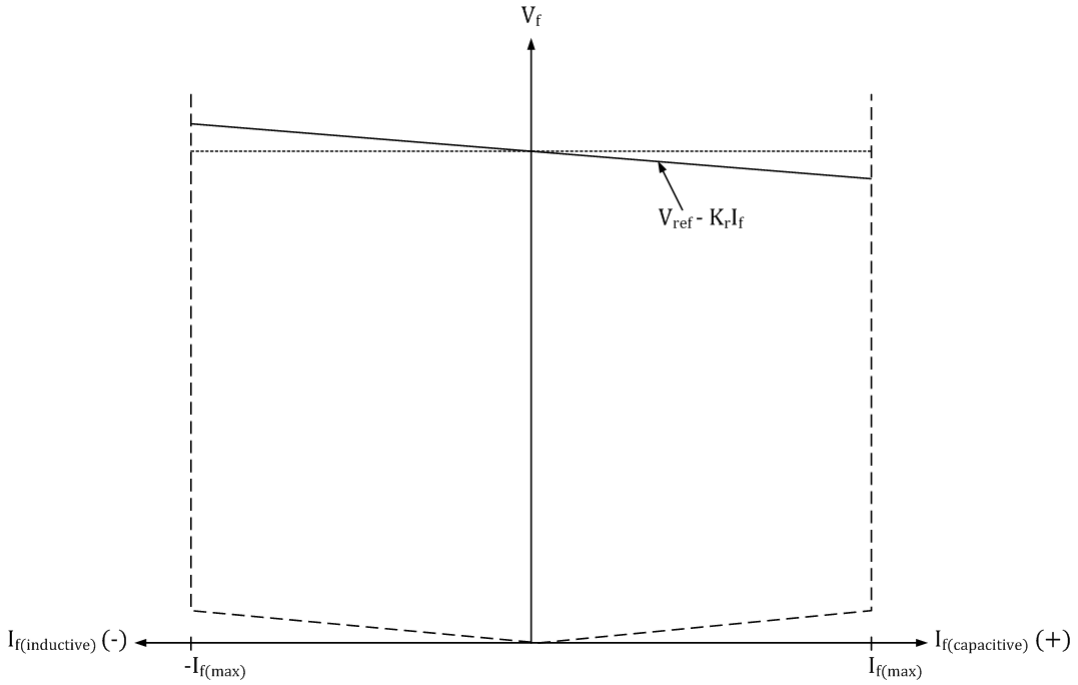


Figure 4.9 - The V-I curve of the static compensator.

The basic working of the controller is now clear and a detailed system model is needed to design the PI-controller gains. This is done in the next section.

4.5. Controller Design

To design the voltage-loop a control diagram is drawn up after considering the system and the discussion in the previous section. This is shown in figure 4.10.

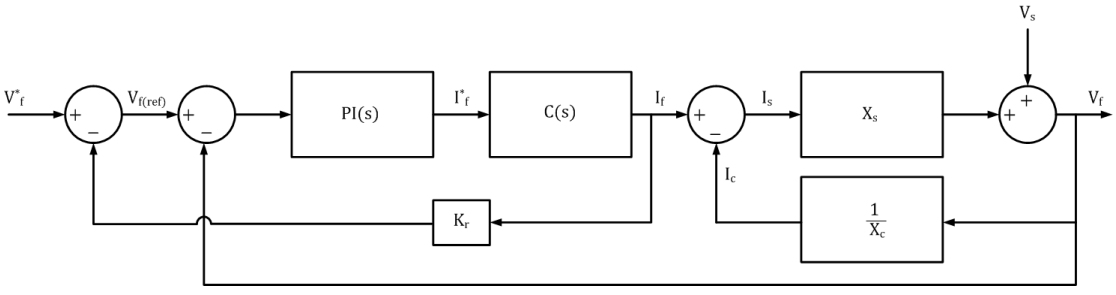


Figure 4.10 - The control diagram of the shunt reactive compensator.

To coincide with the specifications of the project this regulation slope is chosen to allow a 3 % deviation in the nominal voltage at the maximum inverter current. The

regulation slope constant, K_r, is calculated as shown in equation 4.4. K_r is a positive value as a capacitive current is chosen to be positive in the specific inverter.

$$K_r = \frac{\Delta V_{f(max)}}{I_{f(max)}} \qquad 4.4$$

The first step in designing the controller is to note that the system should respond optimally to a change in the voltage V_s rather than to a change in the reference voltage. The reference voltage, V^*_f, is then set to zero and the control diagram redrawn to represent the closed-loop transfer function shown in equation 4.5. The control diagram is shown in figure 4.11.

$$G_{cl}(s) = \frac{V_f(s)}{V_s(s)} \qquad 4.5$$

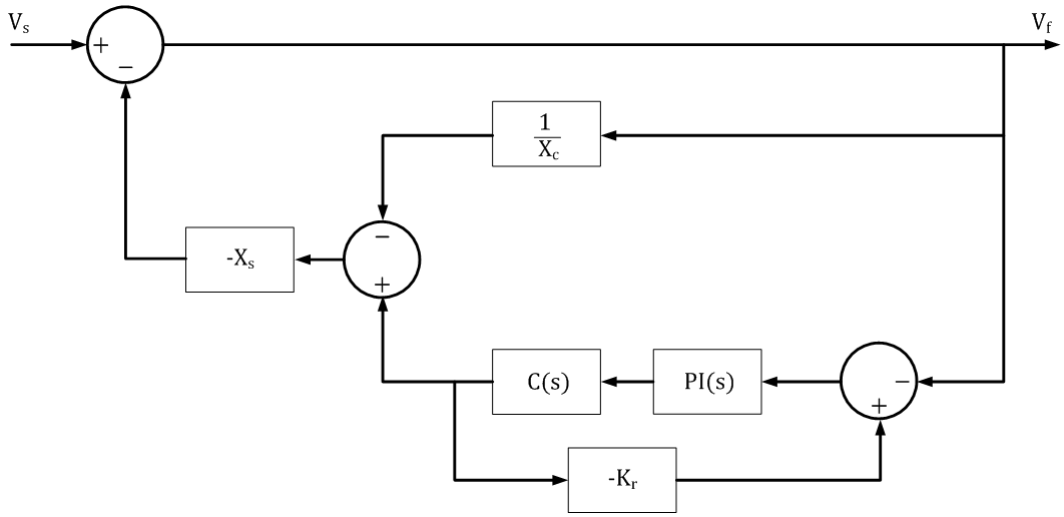


Figure 4.11 - The control diagram after the reference voltage is set to zero.

To simplify the design of the PI-controller it is done in steps making assumptions and approximations. The systematic approach aids in understanding the working of the system and the effects of various parts on the system.

The initial design of the controller is done with a very simplified version of the control loop. The regulation slope and filter capacitance are neglected. The control diagram for this case is shown in figure 4.12.

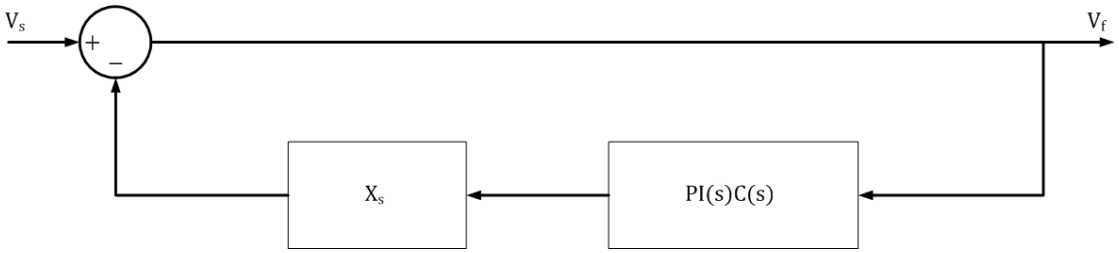


Figure 4.12 - A very simplified version of the control diagram. The filter capacitance and regulation slope are neglected.

The closed-loop transfer function for the simplified case is given by:

$$G_{cl}(s) = \frac{1}{1 + X_s C(s) PI(s)} \qquad 4.6$$

To draw the root locus and the bode plot of the system the characteristic equation, Δ, is needed and can be obtained from the closed loop transfer function. The characteristic equation is shown in equation 4.7.

$$\Delta = 1 + X_s C(s) PI(s) \qquad 4.7$$

Substituting the transfer functions for C(s) and PI(s) and simplifying the result leads to the following equation in the standard form, making it possible to plot the poles and zeros in the s-domain.

$$\frac{-X_s K_p \left(s + \frac{K_i}{K_p}\right)\left(s - \frac{1}{T_s}\right)}{s\left(s + \frac{1}{T_s}\right)} = -1 \qquad 4.8$$

Drawing the root-locus for the system shown in figure 4.13, does not yield much information except that the zero at $\omega = -\frac{K_i}{K_p}$ should be placed in the left side of the s-plane.

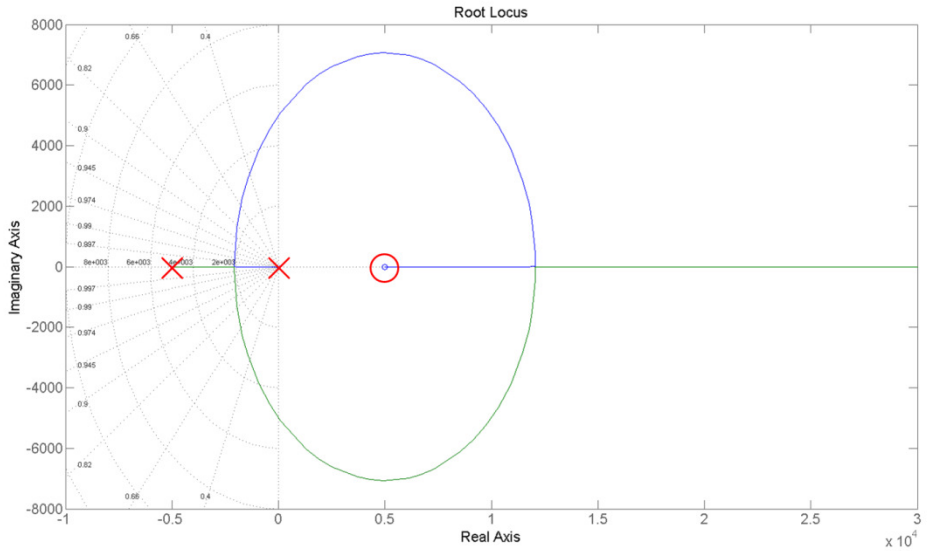


Figure 4.13 - Root locus for the known poles and zeros.

The bode-plot is drawn by neglecting the unknown values as shown in figure 4.14.

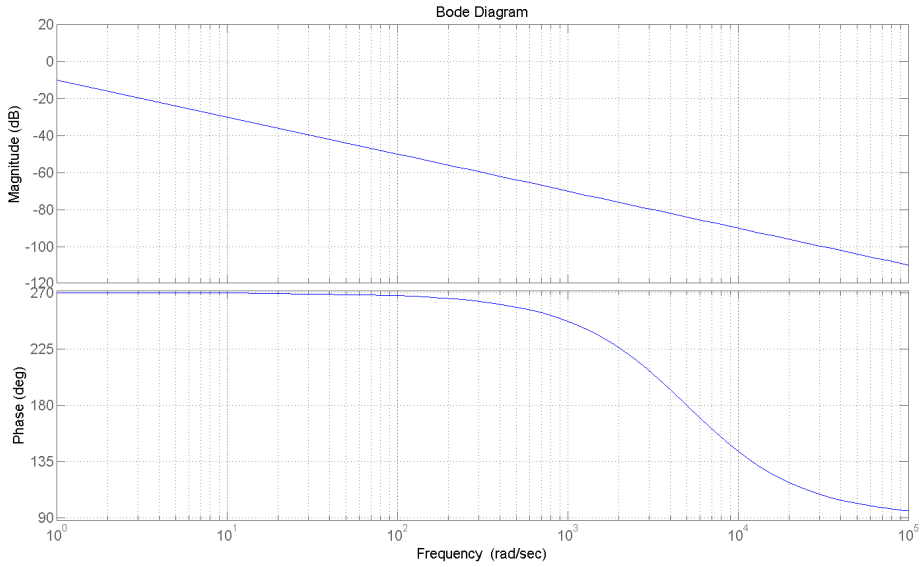


Figure 4.14 - The bode-plot of the known poles and zeros in the transfer function.

The zero at $\omega = -\frac{K_i}{K_p}$ should be placed so that the phase margin is increased. Increasing the phase margin is not critically necessary from a stability point of view as the phase margin is already sufficiently large. The sharp drop in phase angle around $\frac{1}{T_s}$ rad/sec is due to the pole-zero pair of the current controller and can be

countered by placing the zero somewhere between 1 and $\frac{1}{T_s}$ rad/sec. The zero is placed at 2500 rad/sec. And the new bode-plot is drawn as shown in figure 4.15.

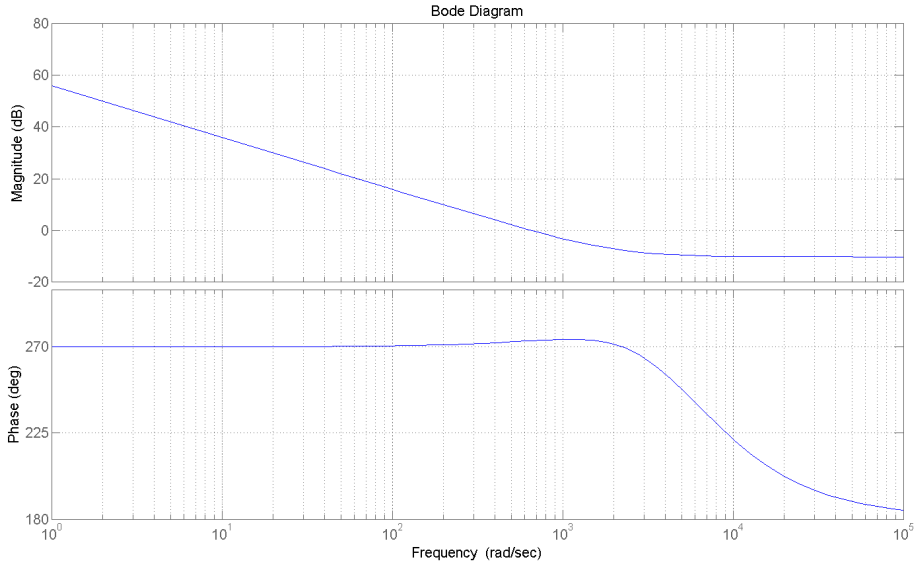


Figure 4.15 - The bode-plot after the zero at 2500 rad/sec is inserted.

The gain, K_p, is free to be calculated and is determined by enforcing a gain margin. Suggesting a gain margin of roughly 20 dB, means that K_p should provide the needed gain to achieve this specification. From the bode-plot in figure 4.15 it can be seen that an extra 10 dB gain is required. Choosing this slightly higher to ensure at least an 20 dB gain margin leads to the calculation of K_p as shown in equation 4.9.

$$20\log(K_p) = -12$$
$$K_p \cong 0.25 \qquad 4.9$$

Knowing the value of K_p and substituting it into the equation for the chosen zero yields a value of 500 for K_i.

After substituting all values and drawing the resulting bode-plot, shown in figure 4.16, the results in table 4.1 can be obtained.

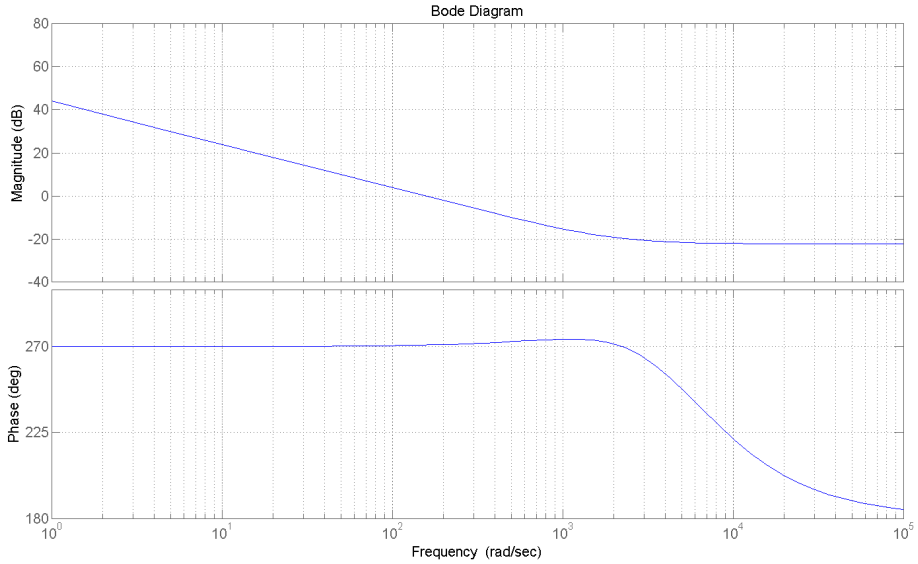


Figure 4.16 - The bode-plot with all the calculated values substituted.

Specification	Value
Phase margin	90.9°
Gain margin	22.1 dB
f_{0dB}	25.15 Hz

Table 4.1 - System specifications for the designed controller.

For the second case the regulation slope is now taken into consideration. The corresponding control diagram is shown in figure 4.17.

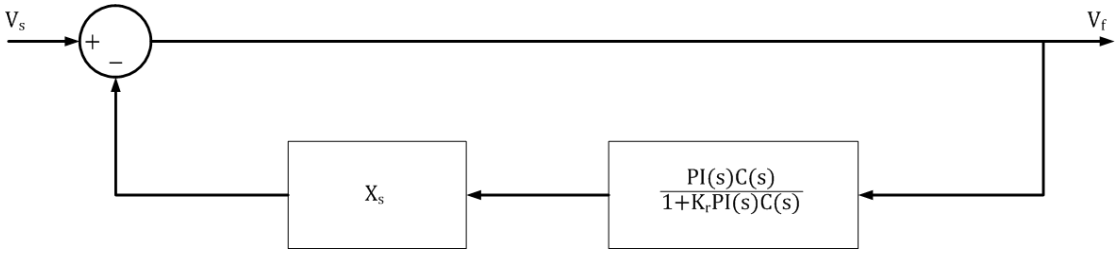


Figure 4.17 - The control diagram with the regulation slope taken into consideration.

The closed-loop transfer function for this case is given by equation 4.10.

$$G_{cl}(s) = \frac{1}{1 + X_s \frac{C(s)PI(s)}{1 + K_r C(s)PI(s)}} \qquad 4.10$$

The characteristic equation is obtained from the closed-loop transfer function, as shown in equation 4.11.

$$\Delta = 1 + X_s \frac{C(s)PI(s)}{1 + K_r C(s)PI(s)} \qquad 4.11$$

Substituting the transfer functions for C(s) and PI(s) and simplifying as far as possible gives the following equation.

$$\frac{X_s K_p}{(K_r K_p - 1)} \cdot \frac{\left(s + \frac{K_i}{K_p}\right)\left(s - \frac{1}{T_s}\right)}{\left(s^2 + s\left(\frac{K_r K_i - \frac{1}{T_s}(K_r K_p + 1)}{(K_r K_p - 1)}\right) - \frac{\frac{K_r K_i}{T_s}}{(K_r K_p - 1)}\right)} = -1 \qquad 4.12$$

Simplifying this equation further will not give an easy and clear indication of the placement of the poles and zeros. An approximation is made by assuming that K_rK_p is much smaller than 1 and can be approximated by 0. If this is true then the term K_rK_i will be even smaller and can also be approximated by 0. Setting these terms equal to 0 yields the exact same equation as in equation 4.8.

To establish that the approximation made here is valid, the controller designed in the case above is substituted into equation 4.12, and the bode-plot is drawn. The corresponding bode-plot is shown in figure 4.18.

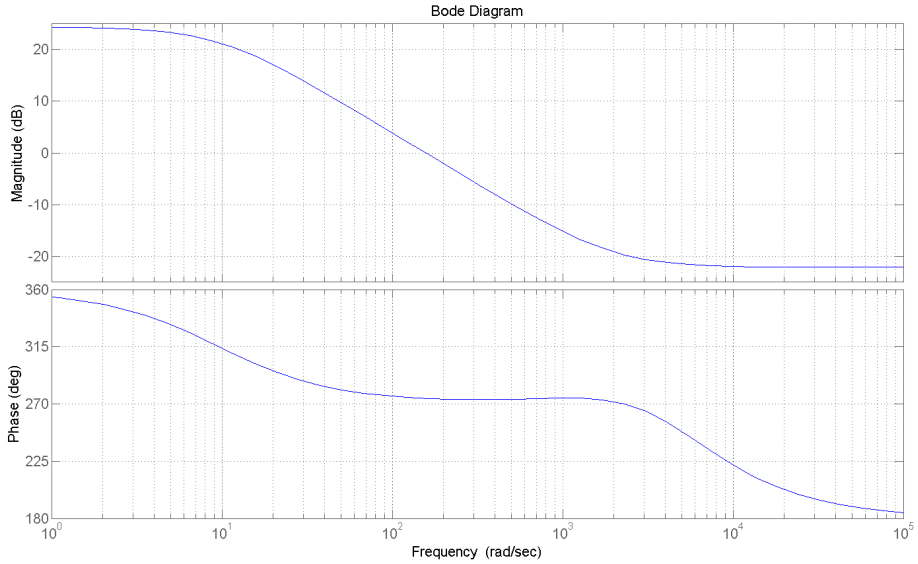


Figure 4.18 - The bode-plot of the system with the approximation made and the previously designed controller.

The result shows that there is a difference in the magnitude and phase at lower frequencies but the phase and gain margins are very close to the previous design as shown in the table below.

Specification	Value
Phase margin	94.4°
Gain margin	22.1 dB
f_{0dB}	24.99 Hz

Table 4.2 - System specifications for the designed controller.

The approximation is therefore considered valid and it shows that the design done with the simplified case yields a very usable result.

For the last case the filter capacitance is also taken into consideration. The control diagram for this case is shown in figure 4.19.

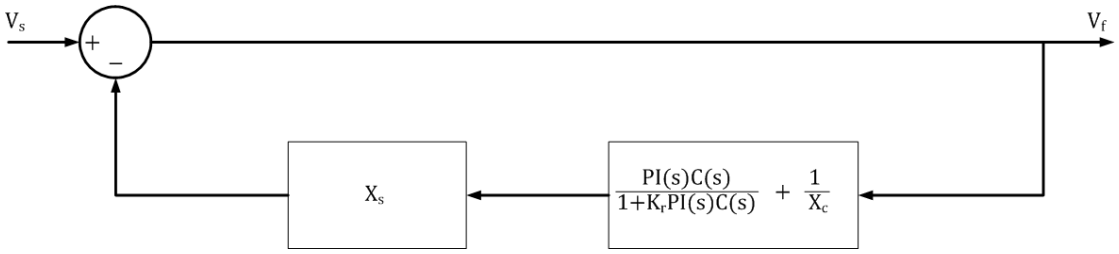


Figure 4.19 - The control diagram with all factors taken into consideration as intitally derived from the system.

The closed-loop transfer function for this case is given by equation 4.13.

$$G_{cl}(s) = \frac{1}{1 + X_s\left(\frac{C(s)PI(s)}{1 + K_r C(s)PI(s)} + \frac{1}{X_c}\right)} \qquad 4.13$$

The characteristic equation is derived from the closed-loop transfer function and is shown in equation 4.14.

$$\Delta = 1 + X_s\left(\frac{C(s)PI(s)}{1 + K_r C(s)PI(s)} + \frac{1}{X_c}\right) \qquad 4.14$$

Simply substituting the initially designed controller into this characteristic equation and by drawing the resulting bode-plot, it is evident that there is almost no difference between this and the previous bode-plot. Only a small variation in the gain margin is seen. A slight variation is however expected as the filter capacitance essentially reduces the system impedance seen by the inverter. The change in the gain margin is so small that it is simply neglected, however, it can be compensated for by simply enforcing a smaller gain margin during the design done for the simplified case.

The bode-plot is shown in figure 4.20 and the resulting specifications are listed in table 4.3 below.

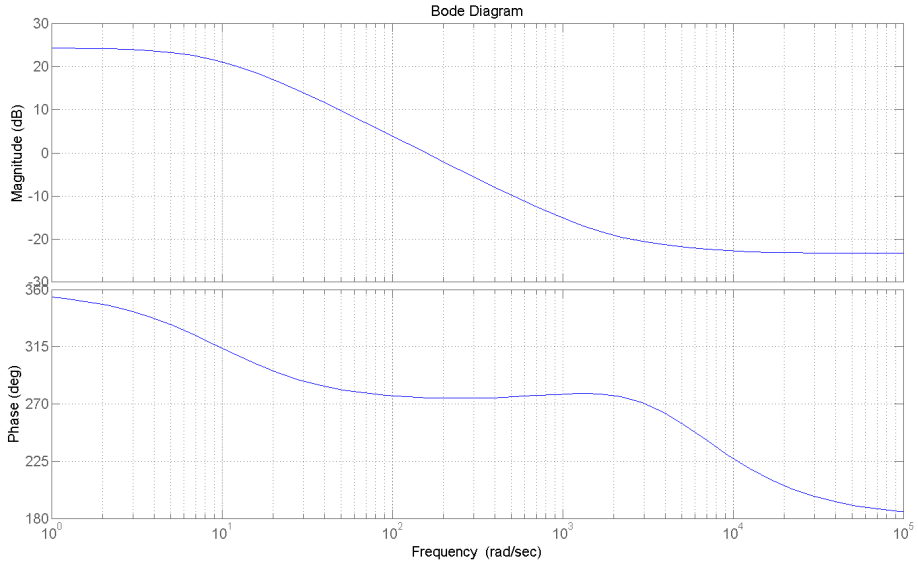


Figure 4.20 - The bode-plot of the system with the intially designed controller.

Specification	Value
Phase margin	95°
Gain margin	23.2 dB
f_{0dB}	24.99 Hz

Table 4.3 - System specifications for the designed controller.

It is concluded that the design is sufficient and that the acquired PI-controller can be used for the voltage controller. If it is noted that this is indeed a second order system the specifications of the controller can be determined from some standard equations.

All the closed-loop poles are located on the real axis and therefore the damping ratio is equal to one, resulting in a system that is over damped and no overshoot is expected.

4.6. Controller Implementation

The controller for the design discussed above is implemented in the stationary reference frame. The controller is designed in the continuous-time domain and needs to be discretisized for it to be implemented digitally. Equation 4.15 descries the PI-controller and is shown below.

$$PI(s) = \frac{I_f^*(s)}{V_{fe}(s)} = K_p + \frac{K_i}{s} \qquad 4.15$$

where, I_f^* is the reference reactive current and

V_{fe} is the difference between the reference space-vector magnitude and the measured space-vector magnitude.

The proportional and integral terms can be divided into two separate algorithms as shown in section 3.5.3. Discretization is done using the backward Euler method. Using this method, where $s \rightarrow \frac{z-1}{zT_s}$, and rewriting the equations in discrete time, by making use of z-transform properties, leads to the following two equations.

$$I_{fp}^*[k] = K_p V_{fe}[k] \qquad 4.16$$

$$I_{fi}^*[k+1] = I_{fi}^*[k] + K_i T_s V_{fe}[k+1] \qquad 4.17$$

Equations 4.16 and 4.17 can be implemented exactly as shown in C-code on the DSP. The values of K_i and K_p are known from section 4.5.

The exact implementation of the controller is depicted in figure 4.21 below. The figure shows the integral anti-windup and current limit as implemented in section 3.5.3.

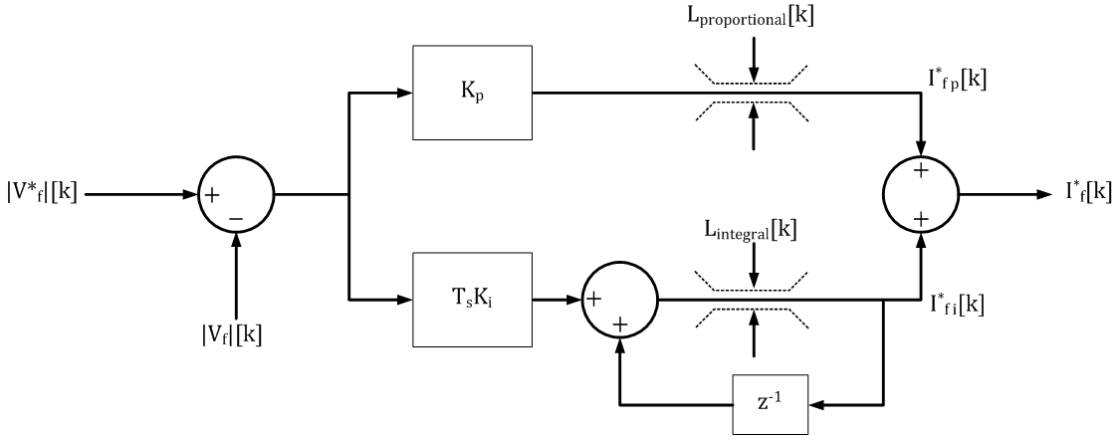


Figure 4.21 - The implementation of the PI-controller.

The current needs to be exactly 90° out of phase with the voltage and this is realized by using the voltage space vector and a rotational transformation. The voltage space-

vector is normalized and used to represent the phase of the voltage space vector. The unit vector is calculated by dividing the α and β components of the voltage space vector by the magnitude of the voltage space vector. Rotating this unit vector through 90° and multiplying the α and β components with the determined reference current will ensure that the current is always 90° out of phase with the voltage. The rotational operation is shown mathematically by equation 4.18.

$$\begin{bmatrix} u_{\alpha}^{current} \\ u_{\beta}^{current} \end{bmatrix} = \begin{bmatrix} \cos(90°) & -\sin(90°) \\ \sin(90°) & \cos(90°) \end{bmatrix} \begin{bmatrix} u_{\alpha}^{voltage} \\ u_{\beta}^{voltage} \end{bmatrix} \quad 4.18$$

where, $\begin{bmatrix} u_{\alpha}^{current} \\ u_{\beta}^{current} \end{bmatrix}$ are the components of the unit vector for the current and

$\begin{bmatrix} u_{\alpha}^{voltage} \\ u_{\beta}^{voltage} \end{bmatrix}$ are the components of the voltage unit vector.

The C-code showing the implementation of this specific controller is shown in appendix B of this thesis.

4.7. Performance

As noted in a previous section the impedance of the system may vary greatly due to load variation. To quantify the effect that this variation has on the controller the line impedance is varied and the bode-plot drawn. The change does not result in the controller becoming unstable. The 0 dB crossing of the bode plot is lowered as the system impedance is reduced essentially resulting in a slower response. The phase margins, gain margins and 0 dB crossing frequencies are shown in table 4.4.

System Impedance	0.0628 Ω	0.1256 Ω	0.1885 Ω	0.2513 Ω	0.3142 Ω
Phase Margin	108°	99.4°	96.7°	95.5°	95.0°
Gain Margin	37.2 dB	31.2 dB	27.7 dB	25.2 dB	23.2 dB
$\mathbf{f_{0dB}}$	4.76 Hz	9.88 Hz	14.9 Hz	20.05 Hz	24.99 Hz

Table 4.4 - System specifications for the designed controller with a variation in the system impedance.

A slower controller is expected as the impedance decreases. The controller should therefore always be designed for the maximum system impedance, but an over estimation will lead to an unnecessarily poor performance.

Chapter 5: Shunt Connected VSI for Unbalance Mitigation

In this chapter the application of a VSI for the mitigation of voltage unbalance in a three-phase system is discussed. The condition under which the VSI operates and how the unbalance is mitigated is discussed in detail. A discussion on the practical implementation of the control algorithm is also included.

5.1. Introduction

The aim is to design and implement a control algorithm that will enable a shunt connected VSI to compensate for voltage unbalance and to reduce the voltage unbalance at the point of coupling to zero by means of reactive power.

The same approach is followed as in chapter 4 where the VSI is used to load the transmission line with the appropriate reactive load to restore the voltage to the correct level. The main difference here being that the average voltage level of the three phases are now different and the reactive load required by each phase to restore the voltage is different. The inverter is required to generate unbalanced reactive current.

As discussed in section 2.3.1 the unbalanced system can be represented by two balanced three-phase systems. The controller's objective here will be to reduce the negative sequence voltage to zero. Injecting an additional current that either leads or lags the negative sequence voltage by 90° will achieve this. The inverter will generate an unbalanced reactive current if a negative sequence reactive current is added to the positive sequence reactive current.

It is important to note that the zero-sequence is not controlled, as this requires the use of a VSI with an additional phase-arm. This means that zero-sequence voltages cannot be compensated for. The implication is that the load at the point of regulation must be balanced when connected in a wye configuration or be reconnected in delta. This will ensure low levels of zero-sequence voltage or none at all. Any unbalance

originating from the supply side can be successfully mitigated at the point of regulation.

Emphasis is placed on voltage unbalance compensation in this section. The goal is to ensure that a balanced voltage is experienced by the load at the point of regulation. No attempt is made to compensate for unbalanced current due to unbalanced loads. These types of compensation methods may require absorbing or supplying active power [23] and is not ideal considering the specific UPS application of the VSI under discussion here.

The implementation of reactive compensation is also discussed throughout this chapter as it may be implemented together with unbalance compensation.

There are two major issues regarding the practical implementation of the control strategy that become evident early in the design process. These involve the negative sequence voltage error and the phase of the injected negative sequence current and are subsequently discussed.

5.2. VSI (Unbalanced Conditions)

In section 4.2 it was shown that the VSI is able to generate reactive currents. In order for this same VSI to be used to compensate for voltage unbalance, it should be possible to unbalance this reactive current.

As discussed in section 2.3.1 the unbalanced system can be represented by two balanced three-phase systems. The addition of a negative sequence reference current to a positive sequence reference current will realize an unbalanced reference current. Feeding the current controller with this unbalanced reference current allows the VSI to generate the unbalanced current consisting of positive and negative sequence components.

To be able to control the zero sequence voltage and thus the zero sequence current, the neutral phase must also be switched. Consequently a VSI with four phase-arms, with the fourth one being connected to the neutral phase, will be needed. The current controller should be designed to control zero sequence currents as well.

Since the negative sequence reference current that will mitigate the voltage unbalance is a reactive current, it either leads or lags the negative sequence voltage by 90°.

To draw an active negative sequence current from the electricity network is not desired in the case of the test inverter. It is useful to do this in the case of multi-level inverters where this current is used to control individual DC-bus capacitor voltages [24]. The active negative sequence reference current is therefore set to zero.

The small amount of active power drawn by the inverter in chapter 4 is still required and is implemented in exactly the same way as before. The amount of unbalance in the current generated by the inverter is variable making the VSI very suitable for compensating for varying amounts of unbalance.

5.3. System Overview

The same approach is used as in chapter 4 where the transmission-line impedance is assumed to be equal in each phase. The transmission line is the same relatively short feeder and is modelled by a series combination of inductance and resistance. The capacitance of this short transmission-line is again neglected.

The unbalanced voltage is assumed to originate at the point where the feeder connects to the grid or at some point between the grid and the point of regulation. The reason for this, considering the balanced transmission-line, is the use of unbalanced loads at various places along the transmission-line. The system is shown in figure 5.1.

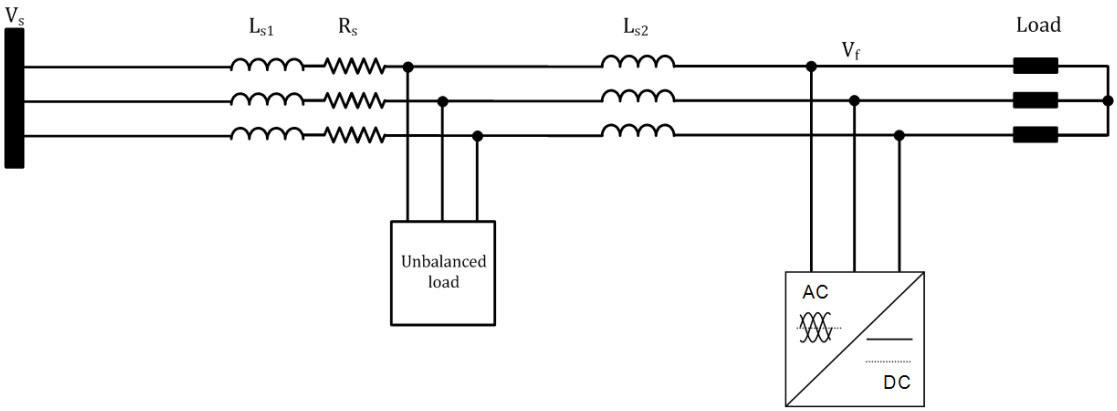


Figure 5.1 - The feeder showing the shunt connected VSI at the point of regulation.

A single-phase diagram of the system is shown in figure 5.1 for the positive and negative sequence. Only reactive components are shown in these diagrams because, as for the reactive compensation in chapter 4, only reactive current will be controlled by the positive and negative sequence voltage controllers. The transmission-line is exactly the same for the negative and positive sequences. The figure shows the feeder from the point where it connects to the grid, denoted by V_{s+} and V_{s-}. It shows the total line inductance, denoted by L_s.

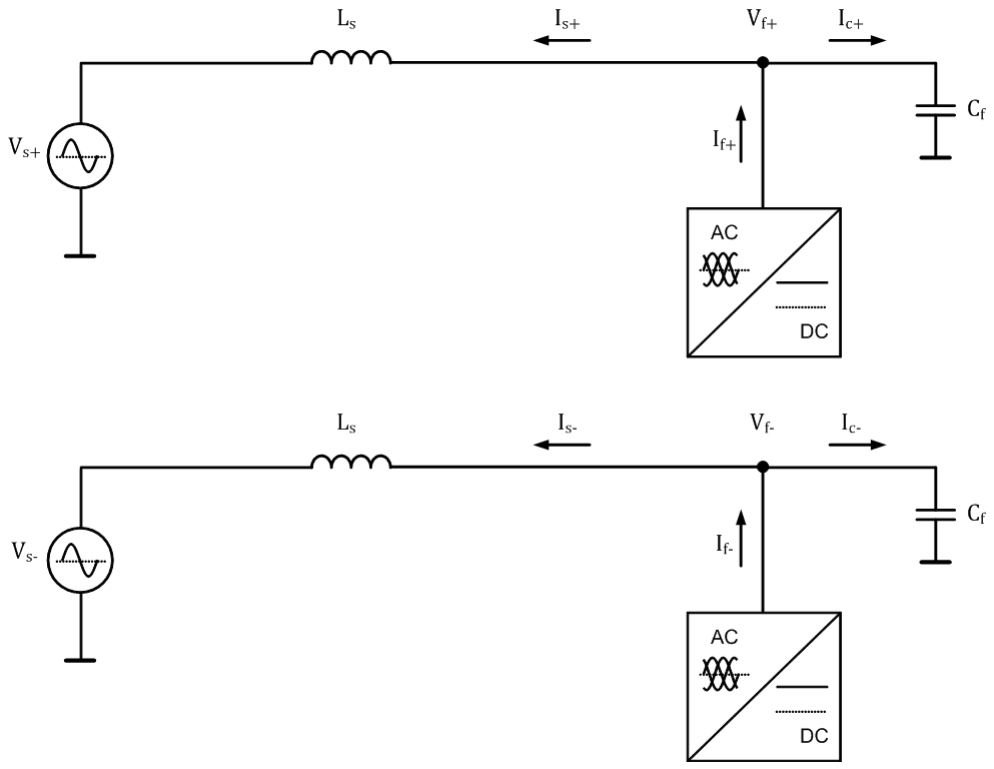


Figure 5.2 - Single phase diagrams for the positive (TOP) and negative (BOTTOM) sequence systems.

The point at which the load is connected and also where the voltage will be regulated, is denoted by V_{f+} and V_{f-}. The capacitors C_f form part of the inverter's output filter.

The system impedance may vary greatly due to load variation and will have an influence on the controller. For this reason this controller is again designed for the maximum system impedance. Here all components that are not permanently connected to the transmission-line are neglected and only the transmission-line impedance is considered. The grid is assumed to have zero-impedance.

The filter capacitors of the inverter are permanently connected to the transmission line and can therefore be taken into consideration when determining the system impedance. Figure 5.3 shows the system for the maximum impedance calculation and is depicted as a control diagram. Note that the load does not feature at all and that the system is the same for the negative sequence as it was for the positive sequence. The maximum line inductance is used to calculate the impedance X_s. X_c is the filter capacitor impedance calculated as $\frac{1}{2\pi f C_f}$.

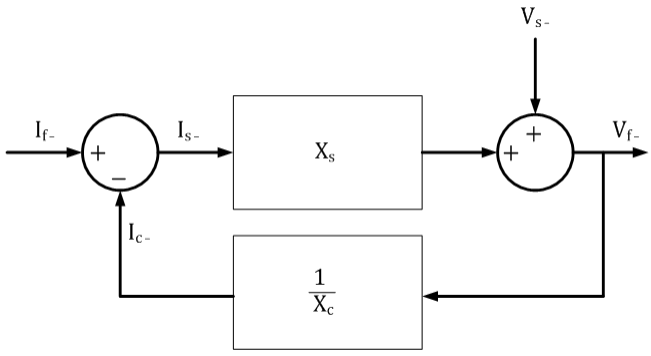


Figure 5.3 - A control diagram showing the relation of the inverter current to the measured voltage for the negative sequence.

5.4. Unbalanced Voltage

In this chapter the unbalanced voltage is considered to consist of a positive and negative sequence only. Accurate knowledge of these two sequences is required to control the positive sequence to its desired level and the negative sequence to zero. This entails measuring the positive and negative sequences as accurately as possible.

5.4.1. Sequence Decomposition

There are several methods of measuring the negative sequence from an unbalanced system. Some methods are not desired especially when it comes to mitigating the unbalance. A distinction needs to be made between purely measuring the negative sequence and measuring it to be able to control it. The reason for this will be discussed in a following section.

The three phase voltages are measured and transformed to their equivalent αβ-components by means of the Clarke-transformation. A method to extract the positive and negative sequences from the measured αβ-components is desired as control is already implemented in this stationary reference frame in the inverter.

Another obvious method is to make use of the inverse Park-transformation that essentially inverts the axes and rotates in the direction of the negative sequence vector. This method is used because the negative sequence is seen as an oscillating signal in the positive sequence synchronous reference frame [15] [25]. The negative sequence signal oscillates at twice the system frequency. Applying the inverse Park-transformation where ω is negative yields the negative sequence in its own dq-plane where the d and q components of the negative sequence (V_{d-} and V_{q-}) are constant values. This transformation is shown in equation 5.1.

$$\begin{bmatrix} V_{d-} \\ V_{q-} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V_{\alpha} \\ V_{\beta} \end{bmatrix} \quad 5.1$$

The positive sequence is obtained by applying the forward Park-transformation on the measured αβ-components as follows:

$$\begin{bmatrix} V_{d+} \\ V_{q+} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V_{\alpha} \\ V_{\beta} \end{bmatrix} \quad 5.2$$

With this method filtering of the signals are essential. Low-pass filters with cut-off frequencies as low as the system frequency are required to eliminate the oscillating AC signals [26] [27]. These filters will have an inherent phase lag and certainly affect the system response [26] [27] and the method is therefore considered undesirable. In addition to this the control of both sequences will have to be implemented in the dq-frame and the result transformed back to the αβ-plane.

Another method that does not require the additional Park-transformation is referred to as delayed signal cancellation (DSC) [28]. Making use of delays, DSC extracts the positive and negative sequence αβ-components from the measured αβ-components. Due to control already being implemented in this reference frame this method is more desirable than the previous one. DSC is derived and explained in the following section.

5.4.2. Delayed Signal Cancellation

Consider an unbalanced grid voltage $V^{\alpha\beta}(t)$ in the fixed reference frame. From previous discussions it is known that this is equal to the sum of the positive and negative sequences:

$$V^{\alpha\beta}(t) = V^{\alpha\beta-}(t) + V^{\alpha\beta+}(t) \qquad 5.3$$

where, $V^{\alpha\beta-}(t)$ is the negative sequence space-vector and $V^{\alpha\beta+}(t)$ is the positive sequence space-vector.

From the definition of the fixed reference frame transformation the positive and negative sequences can be expressed as:

$$V^{\alpha\beta}(t) = V^{\alpha\beta-}(t) + V^{\alpha\beta+}(t) = V^{-}e^{-j(\omega t+\theta^{-})} + V^{+}e^{j(\omega t+\theta^{+})} \qquad 5.4$$

where ω is the fundamental system frequency, θ^{-} and θ^{+} are the phase displacements of the negative and positive sequences and V^{-} and V^{+} are the amplitudes of the negative and positive sequence space-vectors.

If a time delay T_d is added to the measured voltage, equation 5.4 becomes

$$V^{\alpha\beta}(t - T_d) = V^{-}e^{-j[\omega(t-T_d)+\theta^{-}]} + V^{+}e^{j[\omega(t-T_d)+\theta^{+}]} \qquad 5.5$$

Setting the time delay, T_d, equal to a quarter cycle delay at the fundamental system frequency and substituting it into equation 5.5 yields an interesting result:

$$V^{\alpha\beta}\left(t-\frac{T}{4}\right)=V^{-}e^{-j\left[\omega\left(t-\frac{2\pi}{4\omega}\right)+\theta^{-}\right]}+V^{+}e^{j\left[\omega\left(t-\frac{2\pi}{4\omega}\right)+\theta^{+}\right]} \quad 5.6$$

where T_d in equation 5.5 was set to $\frac{T}{4}$ which is equal to $\frac{2\pi}{4\omega}$.

Simplifying equation 5.6 leads to the following result:

$$V^{\alpha\beta}\left(t-\frac{T}{4}\right)=V^{-}e^{-j\left(\omega t-\frac{\pi}{2}+\theta^{-}\right)}+V^{+}e^{j\left(\omega t-\frac{\pi}{2}+\theta^{+}\right)} \quad 5.7$$

Identifying that $e^{-j\frac{\pi}{2}}=-j$ and substituting it into equation 5.7 leads to:

$$V^{\alpha\beta}\left(t-\frac{T}{4}\right)=-j\left(-V^{-}e^{-j(\omega t+\theta^{-})}+V^{+}e^{j(\omega t+\theta^{+})}\right) \quad 5.8$$

Manipulating equation 5.8 and substituting the known equations from equation 5.4 gives:

$$jV^{\alpha\beta}\left(t-\frac{T}{4}\right)=V^{\alpha\beta+}(t)-V^{\alpha\beta-}(t) \quad 5.9$$

Making $V^{\alpha\beta+}(t)$ and $V^{\alpha\beta-}(t)$ the subjects in equation 5.9 and substituting them into equation 5.3 yields expressions for the positive and negative space-vectors consisting of only the measured space-vector and a delayed space-vector.

$$V^{\alpha\beta}(t)=V^{\alpha\beta+}(t)+V^{\alpha\beta+}(t)-jV^{\alpha\beta}\left(t-\frac{T}{4}\right) \quad 5.10$$

$$V^{\alpha\beta}(t)=V^{\alpha\beta-}(t)+V^{\alpha\beta-}(t)+jV^{\alpha\beta}\left(t-\frac{T}{4}\right) \quad 5.11$$

Simplifying these equations and making $V^{\alpha\beta+}(t)$ and $V^{\alpha\beta-}(t)$ the subjects yield the final result.

$$V^{\alpha\beta+}(t) = \frac{1}{2}\left[V^{\alpha\beta}(t) + jV^{\alpha\beta}\left(t - \frac{T}{4}\right)\right] \quad 5.12$$

$$V^{\alpha\beta-}(t) = \frac{1}{2}\left[V^{\alpha\beta}(t) - jV^{\alpha\beta}\left(t - \frac{T}{4}\right)\right] \quad 5.13$$

The sequence decomposition algorithm is digitally applied as follows:

$$V^{\alpha\beta+}(k) = \frac{1}{2}\left[V^{\alpha\beta}(k) + jV^{\alpha\beta}(k - n_d)\right] \quad 5.14$$

$$V^{\alpha\beta-}(k) = \frac{1}{2}\left[V^{\alpha\beta}(k) - jV^{\alpha\beta}(k - n_d)\right] \quad 5.15$$

where, k is the instant at which the current sample period takes place. n_d is the number of samples that make up a quarter cycle delay and can be calculated as:

$$n_d = \frac{f_s}{4f_{ac}} \quad 5.16$$

where f_s is the sampling frequency and f_{ac} is the line voltage frequency.

From equations 5.14 and 5.15 the measured space-vector is decomposed into the positive and negative sequence space-vectors. The αβ-components of each sequence are now available to be used in any way necessary.

From a digital implementation point of view the value of n_d should be an integer. It is obvious from equation 5.16 that this may not always be the case, since the ratio between the sampling and system frequency may not always be constant due to a variation in either. Normally in a digital system the sampling frequency is fixed. A variation in the system frequency is however very possible and almost always deviates from the nominal frequency. The variation may be small but can have a significant effect on the decomposed signals [27] [28]. It is shown that the error made with the decomposition is the same for a variation in sampling frequency and a variation in system frequency [27] [28].

Methods are available to reduce the error made due to this variation in frequency. The two main methods are averaging and the weighted mean method. The second method is identified as the best solution to reduce the decomposition error [27] and is discussed in the next section.

5.4.3. Weighted-Mean Error Reduction

The weighted mean method essentially involves rounding the calculated delay shown in equation 5.16. This calculated delay is rounded up and down to the nearest integers as shown by equations 5.17 and 5.18. The sequence decomposition is calculated, as shown by equations 5.14 and 5.15, for both these delays. A weight is assigned to each calculation and the sum calculated. This is shown in equation 5.19 and 5.20.

$$n_{d1} = \text{floor}\left(\frac{f_s}{4f_{ac\,m}}\right) \tag{5.17}$$

$$n_{d2} = \text{ceil}\left(\frac{f_s}{4f_{ac\,m}}\right) \tag{5.18}$$

where, floor() rounds the value to the closest integer smaller than the value,

ceil() rounds the value to the closest integer bigger than the value and

$f_{ac\,m}$ is the measured line voltage frequency.

$$V^{\alpha\beta+}(k) = aV^{\alpha\beta+}_{(n_{d1})}(k) + (1-a)V^{\alpha\beta+}_{(n_{d2})}(k) \tag{5.19}$$

$$V^{\alpha\beta-}(k) = aV^{\alpha\beta-}_{(n_{d1})}(k) + (1-a)V^{\alpha\beta-}_{(n_{d2})}(k) \tag{5.20}$$

where the subscripts n_{d1} and n_{d2} denote the sequence decomposition using the delay n_{d1} and n_{d2} respectively and a is a value used to weigh the contribution of each term.

The weight, a, that will minimize the decomposition error should be chosen to be equal to [27] [28]

$$a = 1 - \Delta n_d \qquad 5.21$$

where, Δn_d is the deviation in the calculated number of samples delay from the ideal number of samples delay and can be calculated as shown in equation 5.22.

$$\Delta n_d = \left(\frac{f_s}{4f_{ac\,i}}\right) - \left(\frac{f_s}{4f_{ac\,m}}\right) \qquad 5.22$$

where, $f_{ac\,i}$ is the ideal line voltage frequency.

The weighted-mean values of the positive and negative space-vectors can therefore be calculated from the equations shown above. The only additional requirement is that the frequency of the voltage be measured. Various methods exist to do this and only a simple method is explained below for completeness.

A simple method to measure frequency is to evaluate the voltage measurement at every sample instant. A counter is set to zero at every zero crossing and incremented at every sample instant until another zero crossing is detected. With the sample frequency and the value of the counter known, the frequency can be calculated as follows:

$$f_{ac\,m} = \frac{f_s}{2 \times \text{counter}} \qquad 5.23$$

With this method the frequency measurement is calculated every half-cycle or 10 ms for a 50 Hz system. The discrete implementation of this method means that the measurement may deviate due to non-exact zero-crossing detections. A simple low-pass filter solves this problem by averaging the measured values.

The implementation of this simple method delivers acceptable results.

5.5. Controller Overview

The controller that will mitigate the voltage unbalance consists of an external voltage-loop incorporating the current-loop. The controller controls the negative sequence voltage to its reference magnitude of zero by injecting a negative sequence reactive

current. The voltage-loop can be implemented in parallel with the positive sequence voltage controller which is a similar control-loop as designed in chapter 4. Figure 5.4 shows how the various control-loops interconnect in the inverter's controller.

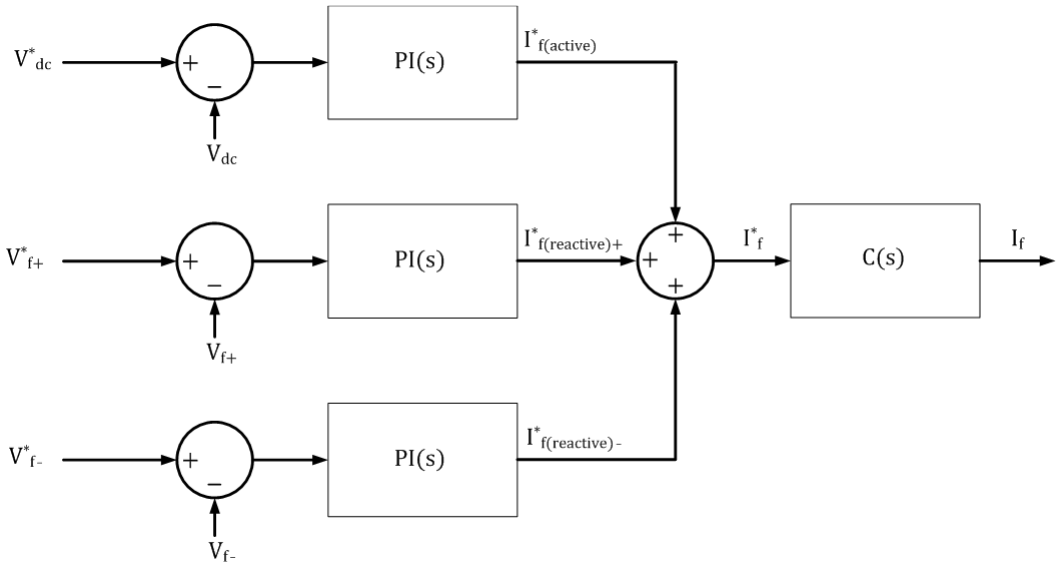


Figure 5.4 - The interconnection of various external control-loops with the current controller.

The basic control diagram of the negative sequence voltage-loop is shown in figure 5.5.

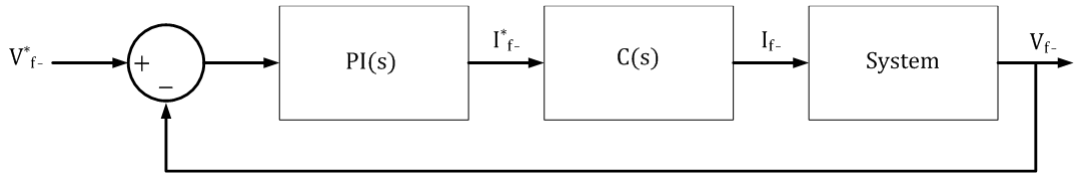


Figure 5.5 - The closed-loop control diagram for the negative sequence voltage.

The negative sequence voltage is handled in the same manner as the positive sequence voltage as the only difference is the direction of the rotating space-vector. As with the controller in chapter 4 only reactive components are considered in the design of the controller because only reactive current is to be controlled.

The voltage controller generates a reference current that will be realized by the dead-beat current controller. This is similar to the control discussed in chapter 4.

The exact same implementation as for the voltage dip compensation, as shown in chapter 4, is not possible. The method used in chapter 4 required the calculation of the space-vector magnitude and comparing it with the reference voltage of 400 V that

meant that the error could be either positive or negative. However, this is not the case for the negative sequence. The space-vector magnitude will always be a positive value and with the reference set to 0 V the error will always remain negative. Consequently the space-vector magnitude calculated from the αβ-components cannot be used for this purpose.

Another issue requiring attention is the phase of the injected negative sequence current. Assume that a negative sequence current of a certain magnitude is required to reduce the unbalance, and therefore the negative sequence voltage to zero. The measured negative sequence voltage will then become zero. The measured voltage is used to determine the required phase of the injected current. The measured negative sequence will become zero making it impossible to inject the required current with the correct phase angle accurately. This problem does not exist with the positive sequence implementation as its voltage remains at some well defined value making accurate determination of the phase possible. Consequently the negative sequence will have to be projected into another reference frame that will make it possible to control it even when it becomes very small or zero.

The solution to these issues is to project the negative sequence into a synchronous reference frame that rotates anti-clockwise but is defined by the positive sequence voltage. The derivation and implementation of this is discussed in detail in section 5.7.

5.6. Controller Design

To design a controller that will mitigate the negative sequence voltage, the same approach is taken as with the dip compensator. The system is analysed and a control diagram drawn as shown in figure 5.6. This diagram shows the measurement of the negative sequence voltage and compares it to the reference. Here the reference is zero as the negative sequence voltage should be controlled to zero. The error is then fed to the PI-controller which generates a reference current and this is then fed into the current controller.

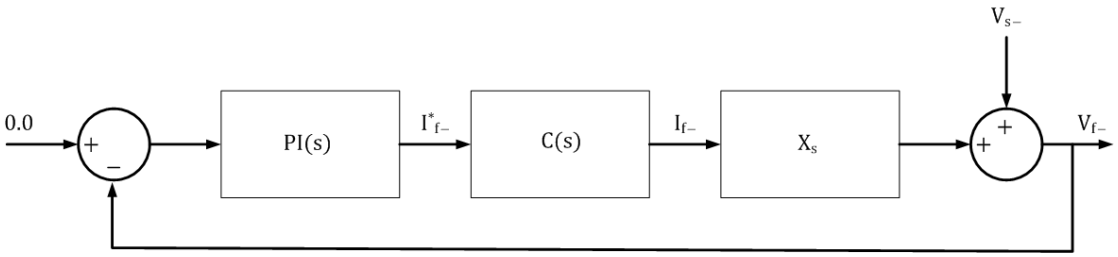


Figure 5.6 - The control diagram derived from the system analysis.

The system is similar to the one for the dip mitigation. This is because with dip mitigation the system was modelled from a positive sequence point of view. The system is now modelled by looking at it from a negative sequence point of view. The impedances are the same for both cases. The only difference is that negative sequence voltages and currents are considered. The current controller is again modelled as a pure delay with unity gain.

The control diagram is simplified here because no regulation slope is introduced as with dip mitigation. This control diagram is exactly as for the initial case considered in section 5.4. The controller that will control this system sufficiently and in a stable way can therefore be designed exactly the same way. The design is only briefly discussed here as it is exactly the same as the initial design in chapter 4.

The closed-loop transfer function for this case is given by:

$$G_{cl}(s) = \frac{1}{1 + X_s C(s) PI(s)} \qquad 5.24$$

To draw the root-locus and the bode-plot of the system the characteristic equation is needed and is easily obtained from the closed-loop transfer function.

$$\Delta = 1 + X_s C(s) PI(s) \qquad 5.25$$

The transfer functions of the current controller, C(s), and the PI-controller, PI(s), are given by equations 4.2 and 4.3 in chapter 4. Substituting the transfer functions C(s) and PI(s) into equation 5.24 and simplifying the result leads to the following equation.

$$\frac{-X_s K_p \left(s + \frac{K_i}{K_p}\right)\left(s - \frac{1}{T_s}\right)}{s\left(s + \frac{1}{T_s}\right)} = -1 \qquad 5.26$$

As before, the bode-plot can be used to determine a suitable position for the zero given by $\omega = -\frac{K_i}{K_p}$ and the gain determined by K_p.

There is no difference between this transfer function and the one in chapter 4 therefore the PI-controller is designed to be exactly the same and is given by equation 5.27.

$$PI(s) = 0.25 + \frac{500}{s} \qquad 5.27$$

5.7. Controller Implementation

For the reasons discussed in section 5.5 the controller needs to be implemented slightly differently. Many methods were considered and ultimately the following one was chosen.

Applying the inverse Park-transformation to the negative sequence αβ-components by making use of the positive sequence unit-vector will place the negative sequence space-vector in a reference frame that rotates oppositely from the positive sequence reference frame. The advantage of this method is that the reference frame is well defined and will not disappear when the negative sequence disappears. A certain current that will reduce the negative sequence voltage can now be injected without the phase becoming an issue. The phase relationship of the negative sequence space-vector and the new reference frame is not predictable and two controllers are needed to control the d and q components respectively. The reference of both, d and q, are set to zero.

Good results have been achieved by implementing this method that adequately resolves the pre-existing issue.

5.8. Performance

A major disadvantage of this method of unbalance compensation is that unbalanced currents are generated. In cases where a coupling transformer is used to interface with the transmission-line this poses a problem. Unbalanced currents may lead to heating of this coupling transformer. In this specific case the inverter is connected directly to the transmission-line and a coupling transformer is not used, therefore eliminating this issue.

The d and q components of the negative sequence voltage are filtered with low-pass filters to ensure that no harmonics and noise disturbs the control algorithm. As a result a slightly longer response time can be expected. This is, however, acceptable as it is considered more important to reduce the unbalance voltage to a low as possible level rather than reducing it as fast as possible.

Chapter 6: Results

In this chapter the information from various simulations and practical experiments that were conducted while carrying out the research for this thesis is given. The reason for each simulation and experiment is stated, the results are shown and their significance explained.

6.1. Introduction

Various tests and simulations were carried out to analyse, evaluate and confirm various phenomena, theories and methodologies.

The details of the specific tests and simulations are discussed in detail in the preceding chapters. Here the specific details of the tests and simulations are discussed, as well as the reasoning behind all of them. In all cases simulations as well as practical experiments have been done. Results throughout were very similar between simulations and practical experiments. Paying attention to creating a simulation environment that reflects the practical environment ensured accurate simulation results. This involved not only the controller setup but also component values and supply voltage harmonics. The results are presented and discussed here.

Due to limited interfacing with the implemented controller hardware in the inverter all control signals are generated in MATLAB or Simplorer v8.

6.2. Practical Measurements

All measurements were made with oscilloscopes using either voltage or current probes. The measurements were saved and processed by MATLAB scripts. This is essential to calculate certain values.

The RMS voltages and currents were calculated using the method specified by the NRS, unless otherwise stated. This method uses a 20 ms window moving across the

time signal in 10 ms intervals. The RMS value for each such window is calculated and plotted.

Voltages and currents were measured on separate oscilloscopes using a common trigger. The voltage and current plots were added to be able to plot the voltage and current on the same plot. This was also done using MATLAB scripts.

Frequency spectrums were also calculated using MATLAB.

6.3. Dead-time Compensation

The two most important issues that were focussed on during the analysis of the dead-time compensation technique were firstly the correlation between the reference signal and the fundamental frequency component of the current and secondly the harmonic content and THD in the current.

To evaluate the tracking error the current delivered by the inverter is evaluated. This is a suitable analysis as the current controller forms the inner control-loop in the inverter. Any tracking error in the current will limit the operational range or the dynamic performance of the inverter.

Evaluating harmonics usually necessitates the consideration of the voltage waveforms. This is because harmonic specifications are usually specified for voltage. Here only the THD of the current is analysed and the different compensation techniques compared. This gives an indication of the distortion of the current waveform due to harmonics.

The tracking error made by the inverter due to dead-time was investigated first. A Simplorer v8 simulation was used for this analysis. Here the inverter is set to deliver power to a resistive load and only a fixed reference current is fed into the predictive current controller. The current is then measured and the error between the reference and the measured current calculated. A good indication of the error made by the dead-time as well as the best method to compensate for this can be made by looking at this error. The current flowing in the inductor of the output filter is measured as this is the current being controlled by the controller.

For the Simplorer v8 simulation a blanking time of 5 µs is inserted and the compensation term is calculated according to equation 3.16. The inverter is set up to deliver power from the DC-bus to a resistive load on the AC side.

The following three figures show the simulation results of the measured current with the reference set to 100 A (peak) in each case.

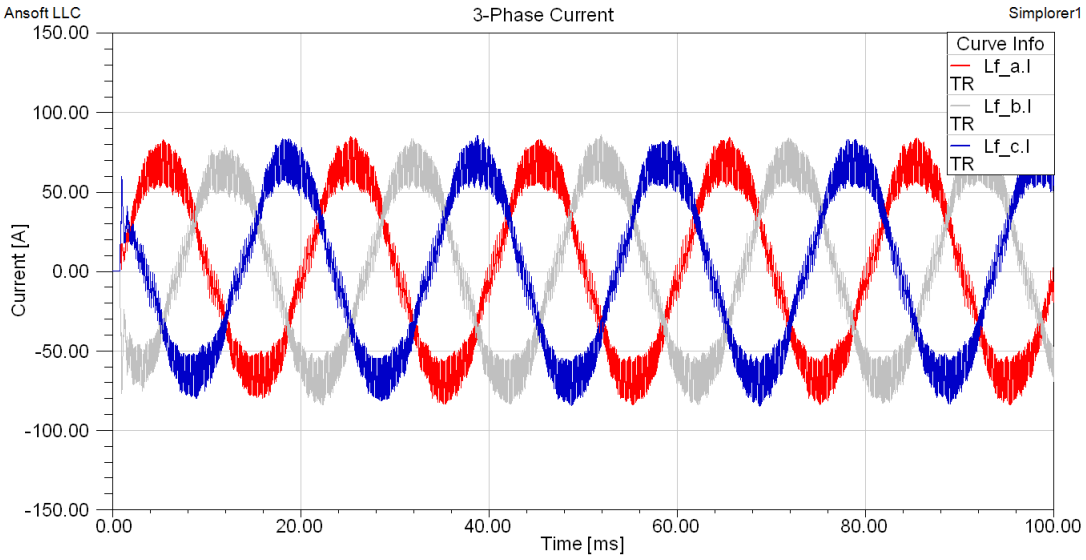


Figure 6.1 - The inverter current with no dead-time compensation implemented. The reference current is set at 100 A peak.

Figure 6.1 shows the inverter output current for the case where no dead-time compensation is implemented. From this figure it is very obvious that there is a large tracking error. The peak current measured 69.3 A. Compared to the reference of 100 A there is a 30.7 % tracking error.

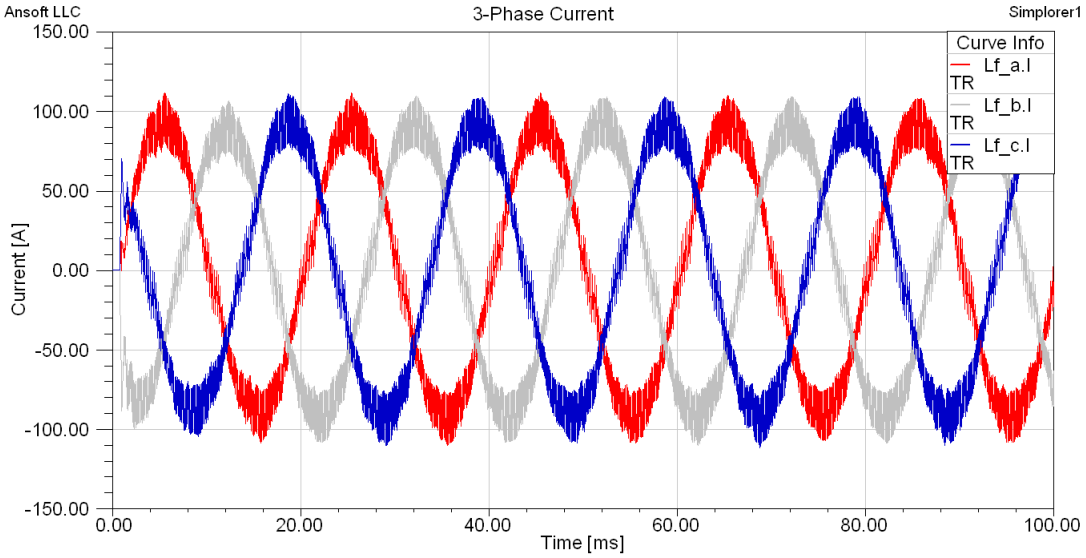


Figure 6.2 - The inverter current with dead-zone dead-time compensation implemented. The reference current is set at 100 A peak.

Figure 6.2 shows the inverter output current for the case where the so called dead-zone dead-time compensation is implemented. It can immediately be seen that there is a substantial improvement. The peak current measured 91.8 A. This equates to a tracking error of 8.2 %. This result shows a great improvement in the tracking error.

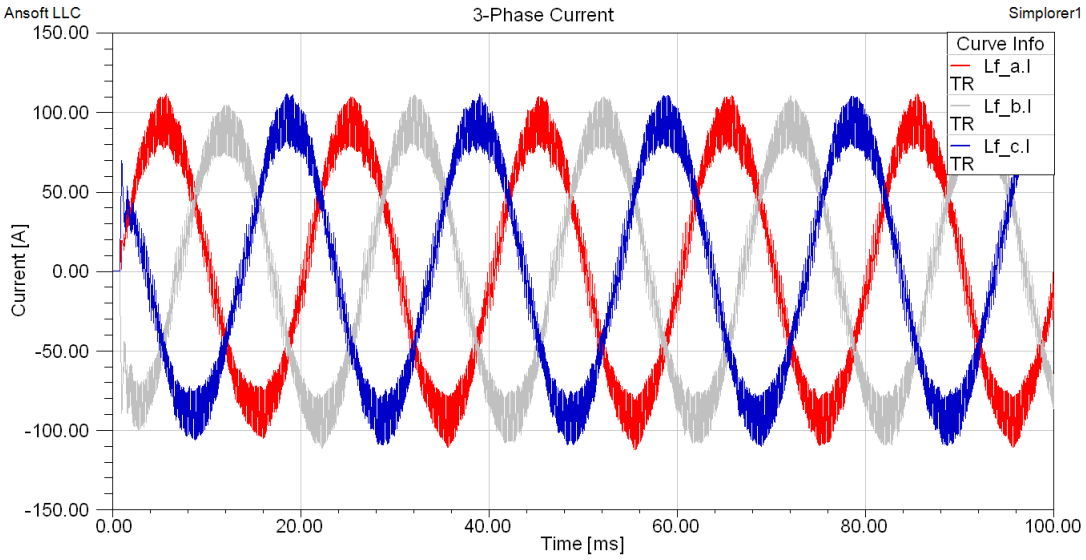


Figure 6.3 - The inverter current with slope dead-time compensation implemented. The reference current is 100 A peak.

Figure 6.3 shows the inverter output current for the case where the linear slope is implemented in the zero crossing of the current. The tracking error also seems to be much smaller. The peak current measured 93.8 A, which equates to a tracking error of 6.2 %. This is a significant improvement in the tracking error.

The difference in tracking error between the dead-zone and the slope methods is small and another measure was needed to determine which is best. Consequently the THD was calculated for each case. The THD will give an indication of which compensation method induces the least amount of harmonics. Considering the first 40 harmonics, the THD was calculated for each case and tabulated in table 6.1.

Compensation method	**Percentage THD_{40}**			
	Phase A	**Phase B**	**Phase C**	**Average**
No	2.78	3.23	3.34	3.12
Dead-zone	3.36	3.56	3.62	3.51
Slope	2.48	3.13	2.85	2.82

Table 6.1 - The THD of the current for each dead-time compensation method.

The percentage THD is lower for the slope method than for the dead-zone method. Any distortion of the current waveform can cause a distortion in the voltage and for this reason the slope method is more desirable than the dead-zone method. This is also the method that performed the best when the tracking error was analysed.

The dead-time compensation not only reduces the error between the reference current and the measured value but, also reduces unwanted harmonics.

The residual tracking error can be attributed to either the dead-beat current controller or more likely an error in the measured current. An error in the measured current is likely due to sampling of signals taking place at the start of the modulation period. This causes the controller to sample the peak inductor current and not the average inductor current. Another modulation technique where sampling takes place in the middle of the modulation period may produce a better result. A faster DSP is required to implement this modulation technique. The DSP used in the test converter has limited computation time and could not be used to practically verify this.

6.4. Dead-Beat Current Controller

The dead-beat controller designed in chapter 3 was implemented and performed exactly as the design methodology predicted. The controller adequately controlled

the converter to realize the reference currents that it was given. The tracking error that was initially experienced was due to dead-time and was sufficiently resolved by implementing dead-time compensation. The two modulation period delay is demonstrated by a step change in the reference current. Figure 6.4 shows the current reference step and the measured current reaching the reference two modulation periods later. The figure shows the reference current after delay compensation was done.

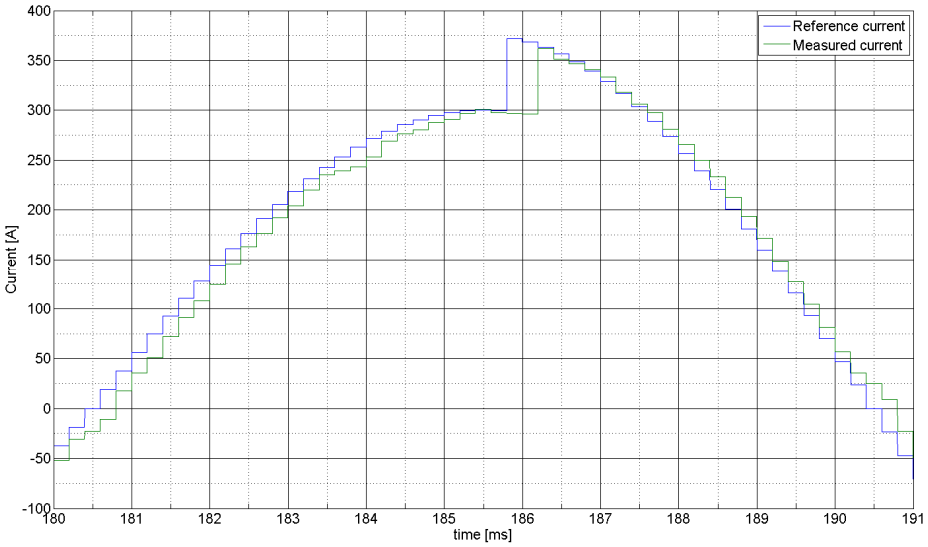


Figure 6.4 - The response of the current controller to a step change in the reference current.

There is no need to discuss the current controller further as the response is known and the controller is used in every test throughout this thesis.

6.5. Dip Mitigation

To test the reactive compensator the feeder in chapter 4 was reconstructed by inductors and resistors. A dip was simulated by connecting a load to the transmission-line. The same approach was followed for the practical experiments as well as the Simplorer v8 simulations. The transmission-line, consisting of inductors and resistors, is shown in figure 6.5.

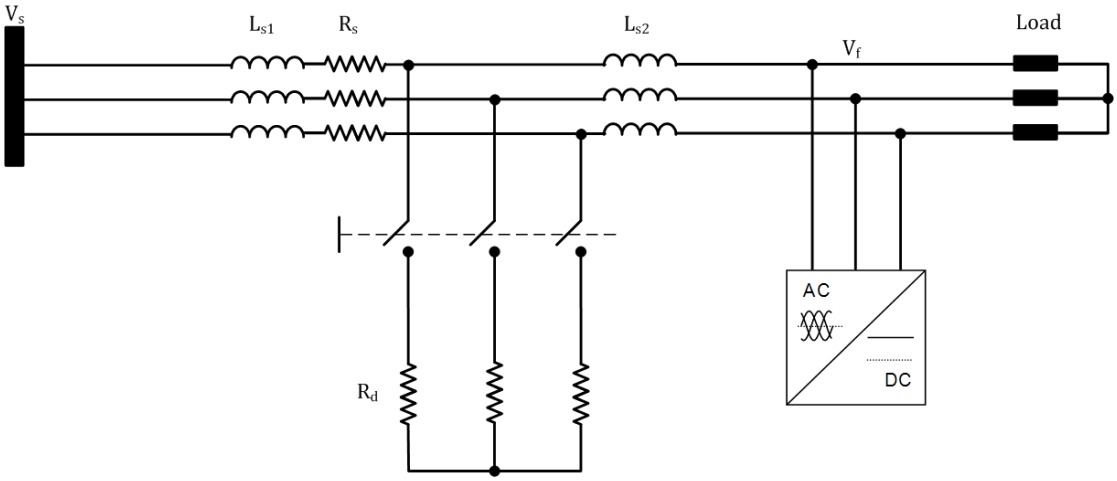


Figure 6.5 - The sytem used to test the shunt voltage-dip compensator as used in experiments and in simulations.

The load was first connected by means of a contactor, in an attempt to simulate a step response in the voltage and to determine the response of the controller. By varying the connected load the depth of the dip could be adjusted. As was noted in chapter 4 the performance is expected to deteriorate as the system impedance drops. To simulate this, a load was connected to the VSI and the transmission-line inductance reduced.

The VSI was set to regulate the DC-bus voltage at 790 V during all of these tests. This is due to reasons discussed before and done by means of the PI-controller designed in section 3.5. A small amount of active current can therefore be expected in all of the current measurements.

Component	**Value**
L_{s1}	200 µH
R_s	0.16 Ω
L_{s1}	800 µH
R_d	1.25 Ω

Table 6.2 - Component values used in dip mitigation tests.

6.5.1. Regulation

The first tests were conducted to determine if the controller was able to regulate the voltage at a specific level. For these tests the reference voltage was set at different levels. These levels varied between 95 % and 102.5 % of the nominal voltage. The supply voltage was also measured without any reactive compensation being done. This indicated that the voltage was already below the ideal nominal value.

With no reactive compensation being done the RMS value of the voltage, V_f, was below the ideal nominal value of 400 V. This value varied in the range of 385 V to 393 V. The table below shows the reference voltages for the various cases tested. Each test is numbered for future reference.

Test #	Reference Voltage [% of nominal voltage]	Reference Voltage Line-Line [V_{RMS}]	Reference Voltage Line-Neutral [V_{RMS}]
1	95.0	380 V	219.4 V
2	97.5	390 V	225.2 V
3	100.0	400 V	230.9 V
4	102.5	410 V	236.7 V

Table 6.3 - The reference voltages used in the various tests.

The voltage levels before any compensation was done are shown in figure 6.6. This shows the voltage at a level of 224 V_{RMS}. The tests in table 6.2 were chosen to allow for regulation above and below this value. The results of these tests are given below.

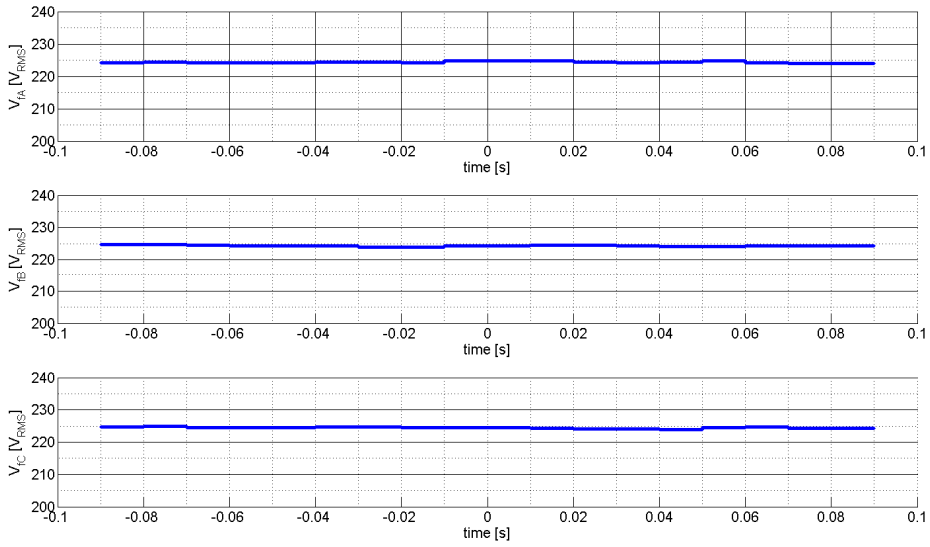


Figure 6.6 - RMS voltage of the three phases before compensation.

Figure 6.7 shows the voltage and current for each phase during the first test. Here the reference voltage is set to 219.4 V_{RMS} which is lower than the voltage before compensation. Figure 6.7 shows a leading current for each phase. This is equivalent to an inductive load on the transmission-line due to the inverted current direction chosen in the inverter. The current measured roughly 15 A_{RMS}.

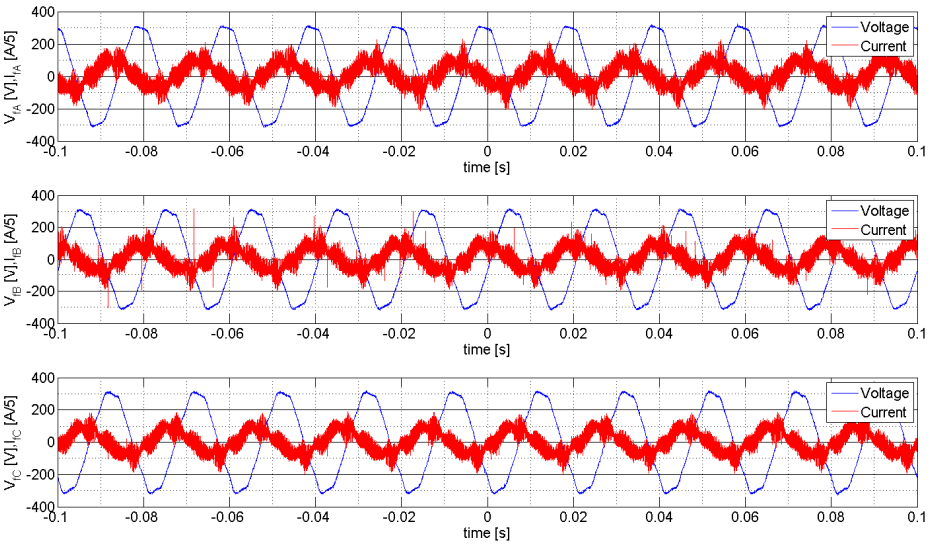


Figure 6.7 - Voltage and current plots during the first test.

Figure 6.8 shows the RMS voltage for each phase during this compensation. From the graph it is evident that the voltage follows the reference very well.

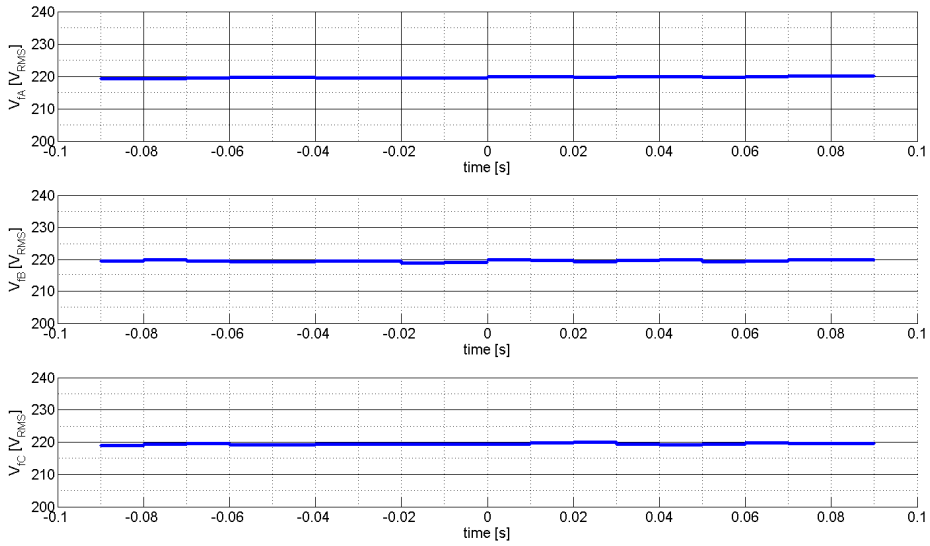


Figure 6.8 - The RMS voltage of each phase during the first test.

The first test distinctly showed that the inverter is able to generate a leading current that simulates an inductive load on the transmission-line. An inductive load is required when the measured voltage is higher than the reference voltage.

During the second test the reference voltage was set to 225.2 V_{RMS} which is very close to the voltage level before compensation. A small reactive current was thus expected to change the voltage to the specific reference. The current was measured and found to be in the region of 9 A_{RMS}. The RMS voltage for each phase is shown in figure 6.9. The voltage follows the reference closely with a negligible error.

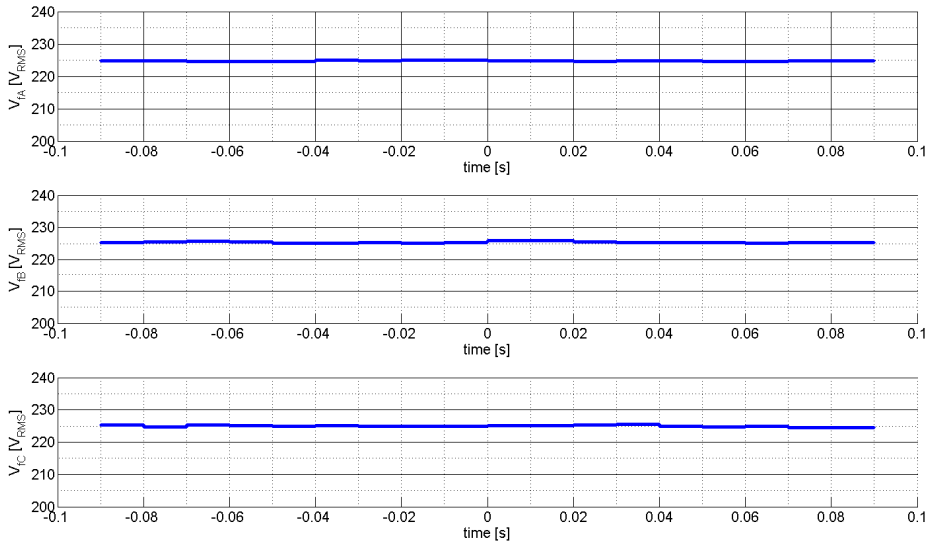


Figure 6.9 - The RMS voltage of each phase during the second test.

The reference voltage was set to 230.9 V_{RMS} during the third test. The reference is slightly higher than the voltage before compensation and is also the level at which the inverter will be used in the field. The inverter was expected to react as a capacitive load on the network. A current corresponding to a capacitive load was generated and measured approximately 14 A_{RMS}. Figure 6.10 shows the RMS voltage for each phase during this test. The voltage follows the reference closely with a negligible error.

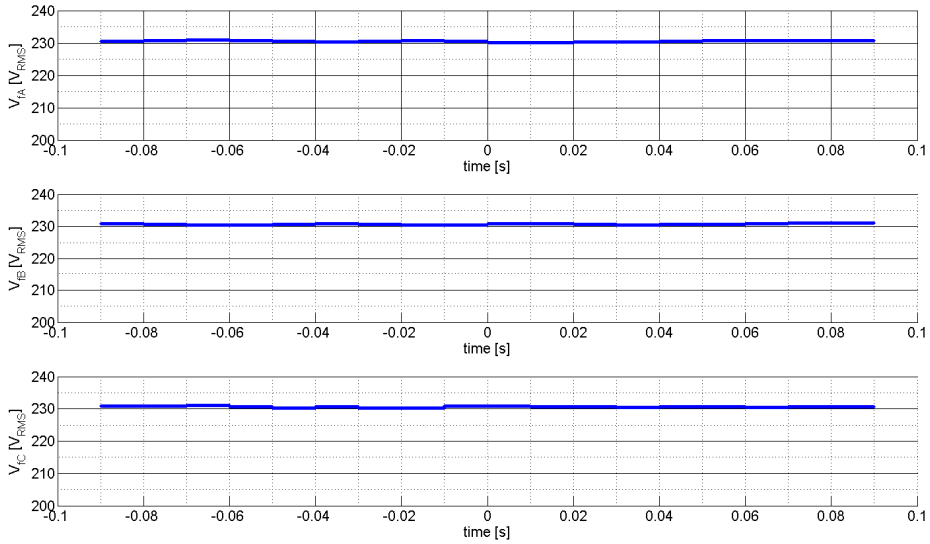


Figure 6.10 - The RMS voltage of each phase during the third test.

Figure 6.11 shows the voltage and current for each phase during the fourth test. For this test the reference voltage was set much higher than the specified voltage. The reference was set to 236.7 V_{RMS}. Figure 6.11 shows a lagging current measuring almost 32 A_{RMS}. The higher current, compared to the third test, was expected as the reference voltage was higher.

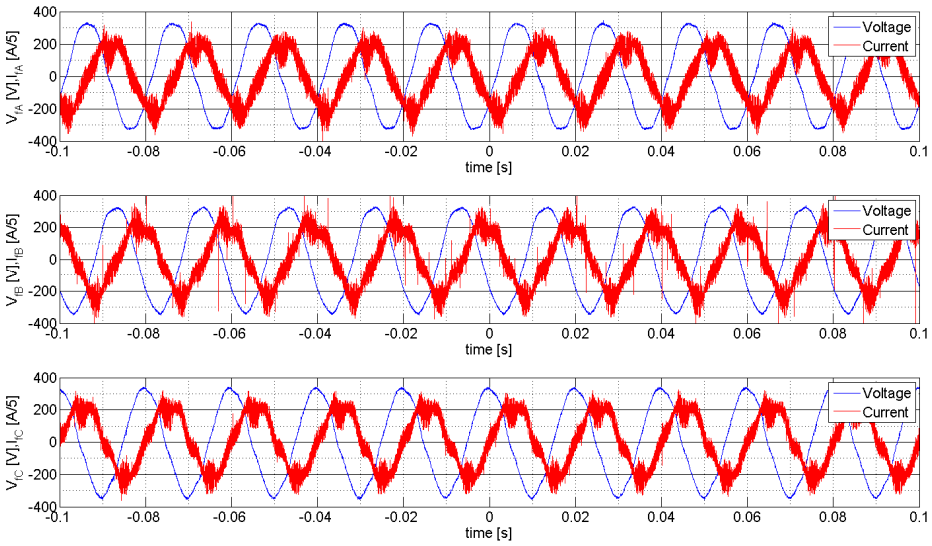


Figure 6.11 - Voltage and current plots during the fourth test.

Figure 6.12 shows the RMS voltage for each phase during the fourth test. The voltage follows the reference closely with a negligible error.

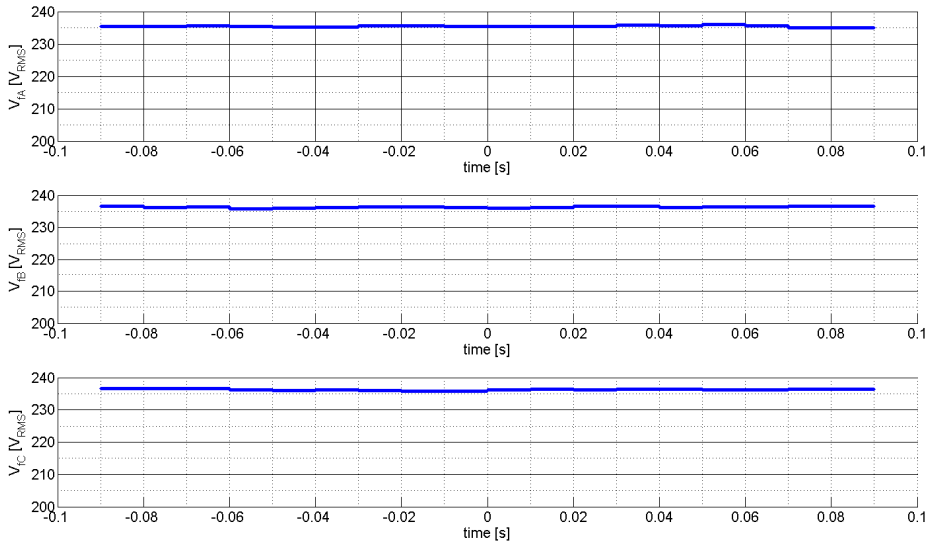


Figure 6.12 - The RMS voltage of each phase during the fourth test.

The fourth test distinctly showed that the inverter is able to generate a lagging current that simulates a capacitive load on the transmission-line. A capacitive load is required when the measured voltage is lower that the reference voltage.

The series of tests above and their results proved that the control algorithm is able to regulate the voltage at levels higher or lower that the transmission-line voltage before compensation. The voltage and current plots show that this is done by means of reactive power. The current is either leading or lagging by 90 degrees depending on the relation of the reference voltage and the supply voltage. The voltage tracks the reference with no error and was expected as the controller consists of an integrator working with constant signals.

6.5.2. Dips

After concluding that the inverter is able to regulate the voltage at a steady level the next step was to determine its response to voltage dips. Voltage dips of various depths were generated. The dips were measured before and after compensation to show the accuracy of compensation.

Apart from the dynamic compensation the effect of the regulation slope was expected to become visible in these tests. With the tests discussed here a reduction in the reference voltage was expected as the current increased.

The voltage controller controls the magnitude of the voltage space-vector and therefore the average value of the three-phase voltage. In all of the presented data the three-phase voltages are shown separately. The voltage and current values discussed refer to the three-phase average values.

A single dip is considered here to illustrate the dip compensation controller. The dip generating resistance, R_d, was chosen to be 1.25 Ω and generated a dip with a depth of 40.9 V_{RMS}. Figure 6.13 shows that the voltage was reduced to 190 V_{RMS} when no compensation was done.

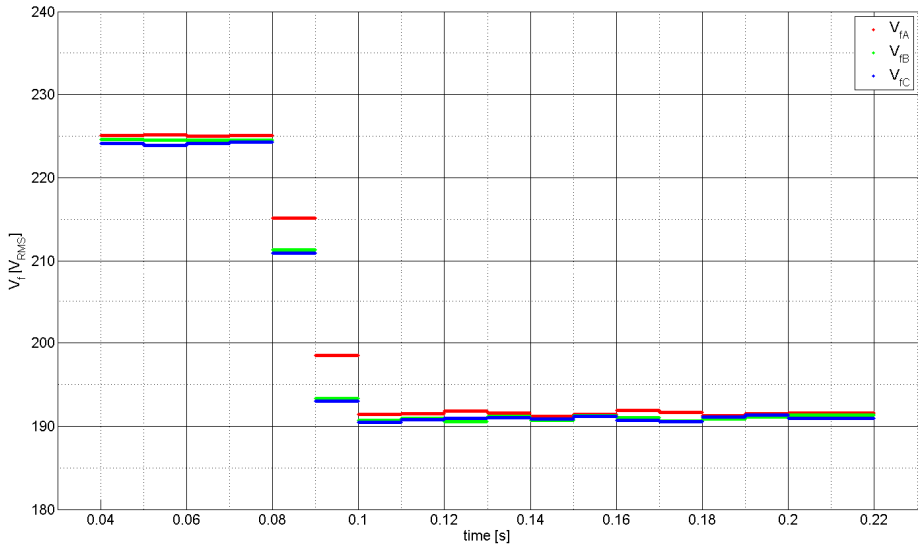


Figure 6.13 - The RMS voltage without compensation.

The corresponding voltage is shown in figure 6.14 for compensation being done. A significant reduction in the depth of the dip can be seen.

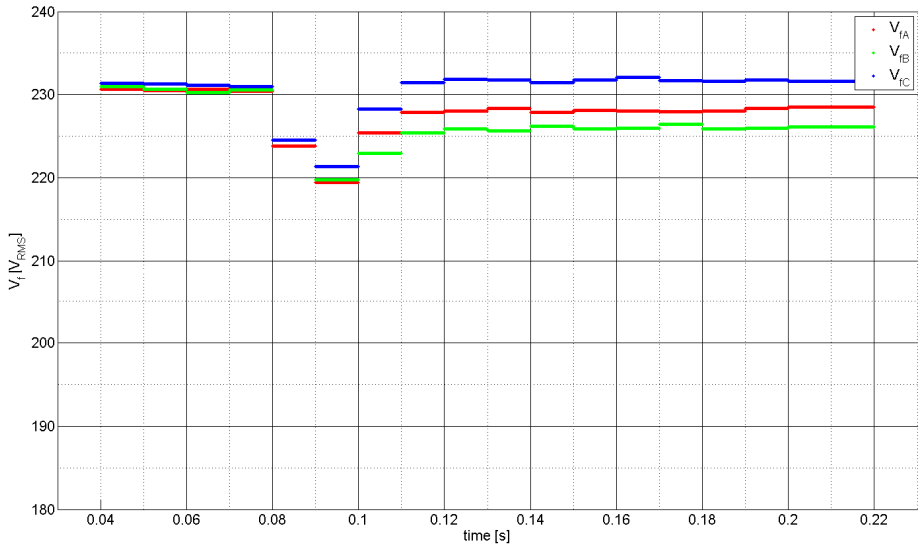


Figure 6.14 - The RMS voltage during compensation for the generated dip.

The voltage and current plots showing compensation are shown in figure 6.15. An increase in current amplitude is seen at the time that the dip is generated.

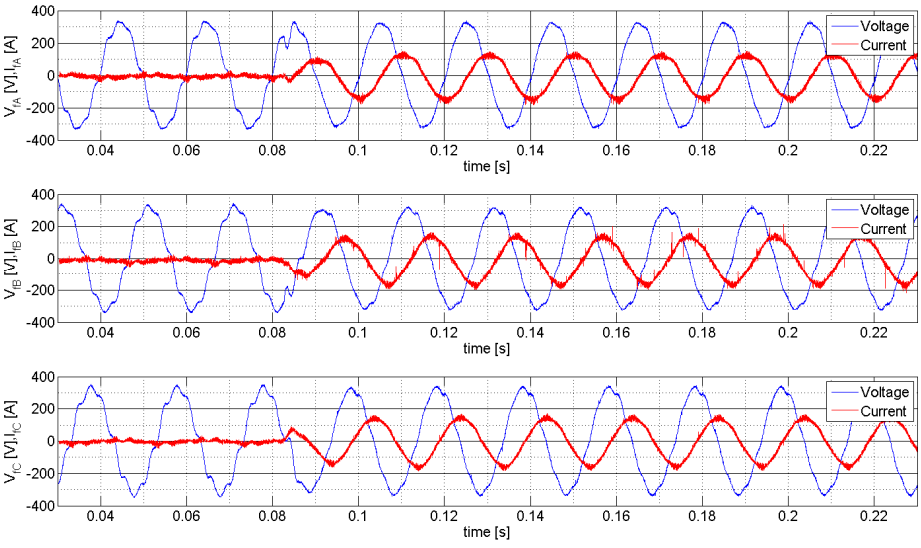


Figure 6.15 - Voltage and current plot for the dip with compensation.

The lowest level of RMS voltage, shown in figure 6.14, is at 220.1 V. The dip experienced is much shallower that the 190 V experienced without compensation.

The current corresponding to the dip increases from roughly 13 A_{RMS} to about 102.9 A_{RMS}.

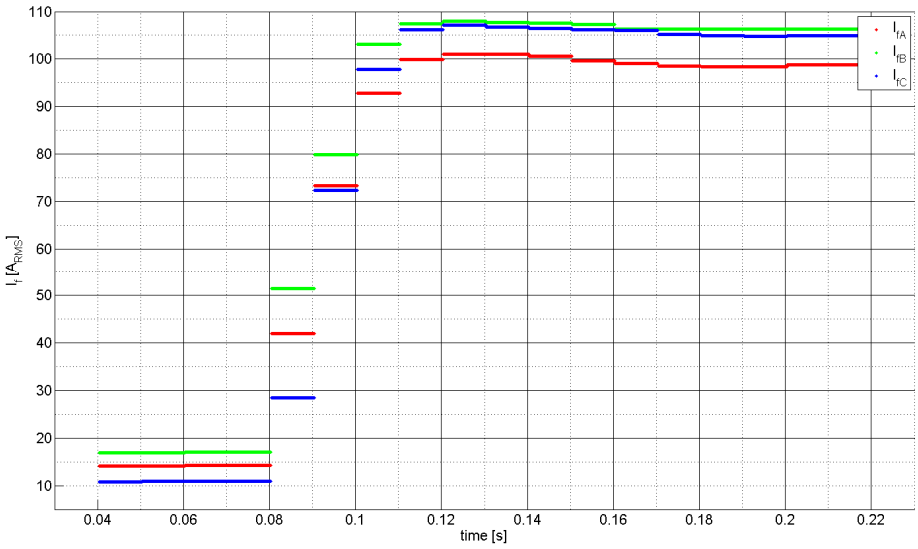


Figure 6.16 - The RMS current generated by the inverter during the dip.

The above test showed that the controller is able to respond to a step change in the voltage. Stability is maintained and the depths of the voltage dips are substantially reduced. The regulation slope also has the desired effect and reduces the voltage reference as the current increases.

From some of the above measurements it is evident that there is some unbalance between the three phases. Mismatches in the values of components and measurement offsets, in the case of currents, cause the slight unbalance.

6.5.3. Unbalanced Conditions

The voltage and current plots for a deliberate unbalanced dip are shown in figure 6.17. Figure 6.17 shows the three phase voltages at different levels while the current in each phase is the same. The controller is designed with only balanced systems in mind and the reference current is configured such that it will be balanced, therefore the result is to be expected.

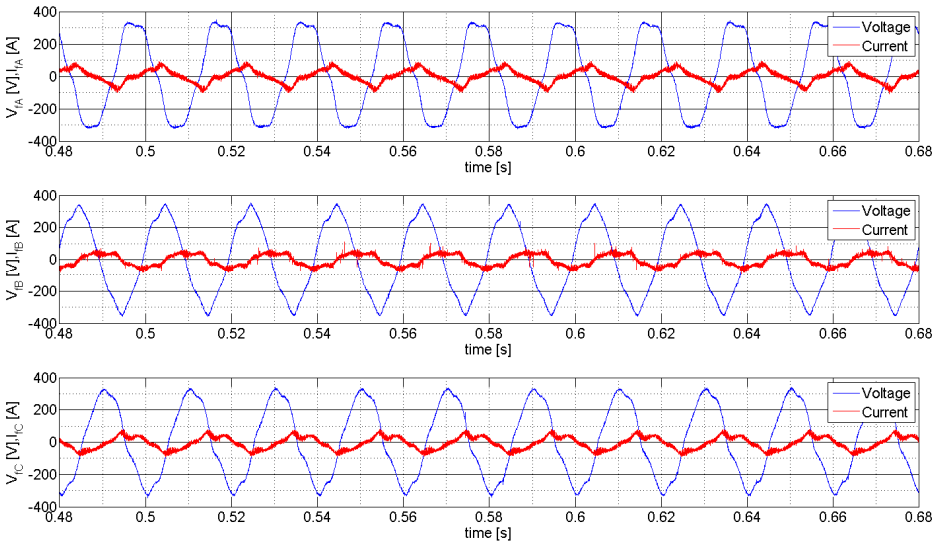


Figure 6.17 - A voltage and current plot of the reactive compensator under unbalanced conditions.

The result of this is that the compensating current is identical in each phase and that the voltage is at different levels as shown in figure 6.18.

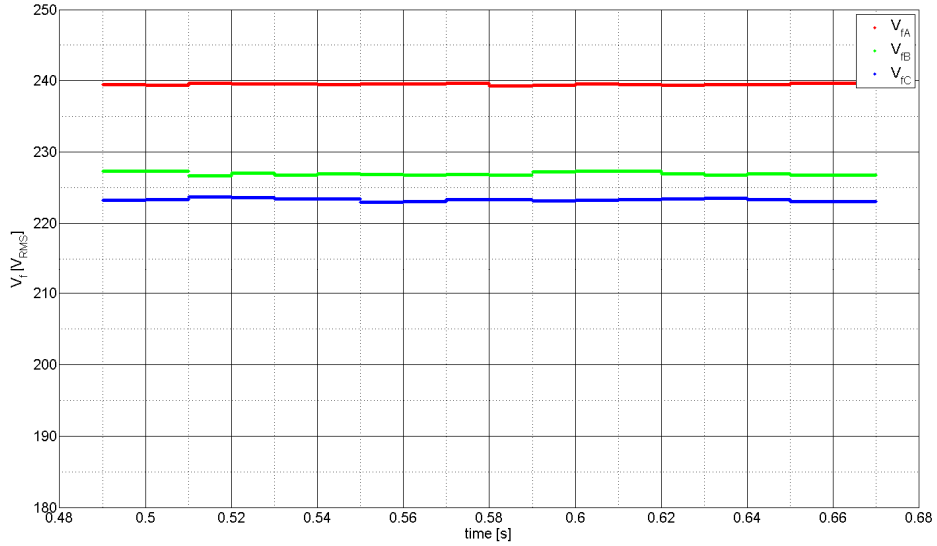


Figure 6.18 - The RMS voltage for each phase during an unbalanced dip.

The average value of the three phase voltages is 229.9 V_{RMS} and the current is 40 A_{RMS} in each phase. The average voltage is controlled to the correct level although the individual phase voltages are not at the correct level. The reason is that an unbalanced current is required to re-balance the voltage.

6.5.4. Dynamic Performance

The important result of the above experiments was that the controller is able to remain stable during all of the step changes. The response time was measured by considering the current generated by the converter. The reference current was generated by the voltage controller and directly controls the voltage. The current space-vector magnitude was measured from the point where the dip starts to the point when the current reaches the required level. Figure 6.19 shows this for the maximum system impedance.

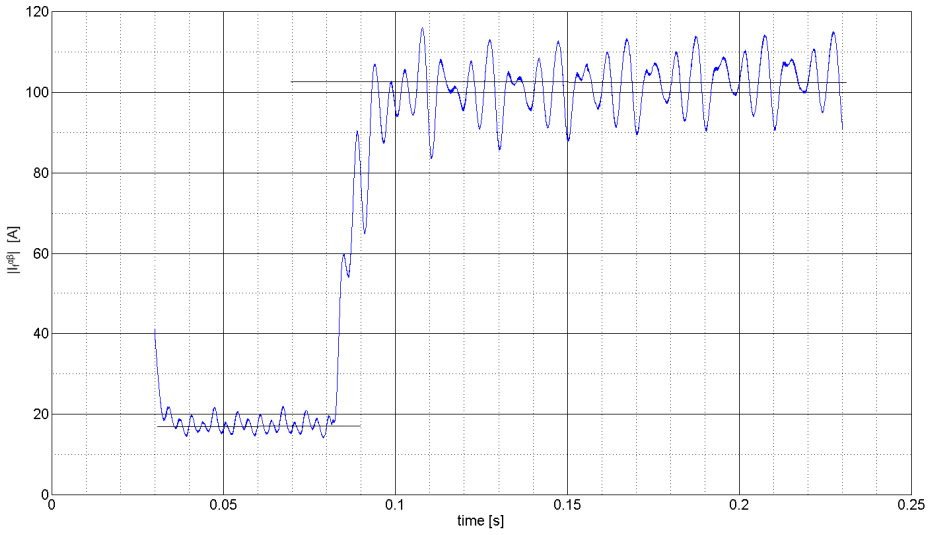


Figure 6.19 – The step response of the inverter current space-vector magnitude for the maximum system impedance.

The time required for the current to reach the required level was 10.9 ms. Connecting a load to the transmission-line at the point of regulation and generating the same dip shows what effect a reduction on the system impedance has. Figure 6.20 shows the corresponding magnitude of the current space-vector.

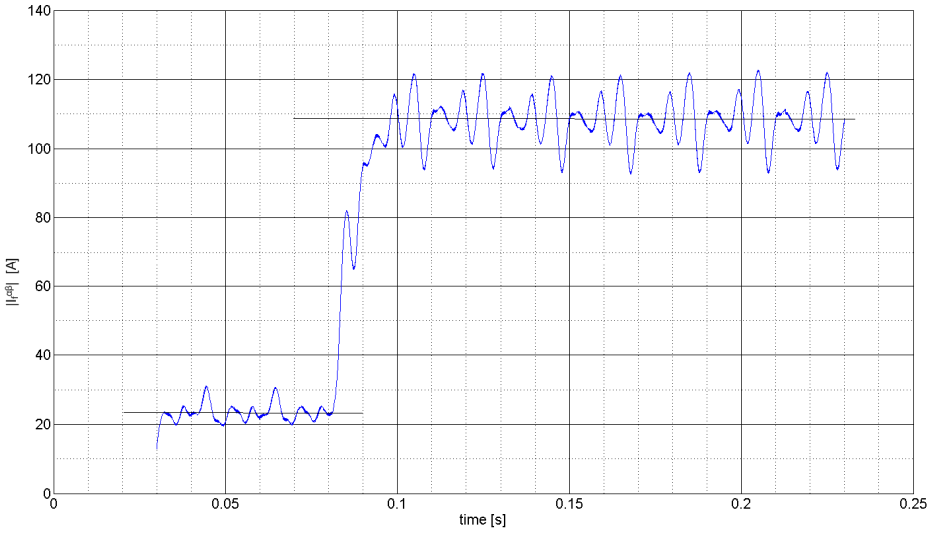


Figure 6.20 - The step response of the inverter current space-vector magnitude for a lower system impedance.

In this case the time required for the current to reach the required level was 16.8 ms. As expected the rise time is longer than for the maximum system impedance case.

Due to the method of generating dips in these experiments the impedance of the system is decreased while the dip generating load is connected. Consequently the response time is reduced. The above two tests were chosen to illustrate this. In both cases the dip generating load is the same. In the second case an additional load is connected to the point where the voltage is being regulated, and this reduces the system impedance.

In these and all other experiments conducted the current reached the required level in a time less than or equal to 21.2 ms. The corresponding voltage is corrected to within the 3 % level in a slightly shorter time. Even though the peak depth of the dip may have been more than 3 % the voltage is corrected to within this range within 20 ms. The conclusion is that these dips were mitigated to such a level that they fall within the NRS specifications.

Simulations confirmed that the response time of the controller is slowed down as the system impedance is decreased. The average of the three-phase currents RMS values was measured to evaluate this. These average values are plotted in figure 6.21. A dip is generated each time by connecting a 10 Ω load to the transmission-line while the inductance, L_{s2}, of the line was varied. The dip is generated at time

300 ms and the rise time is considered in each case. From figure 6.21 it is evident that the response becomes slower as the system impedance is reduced. The importance of estimating the system impedance as accurately as possible is illustrated by this.

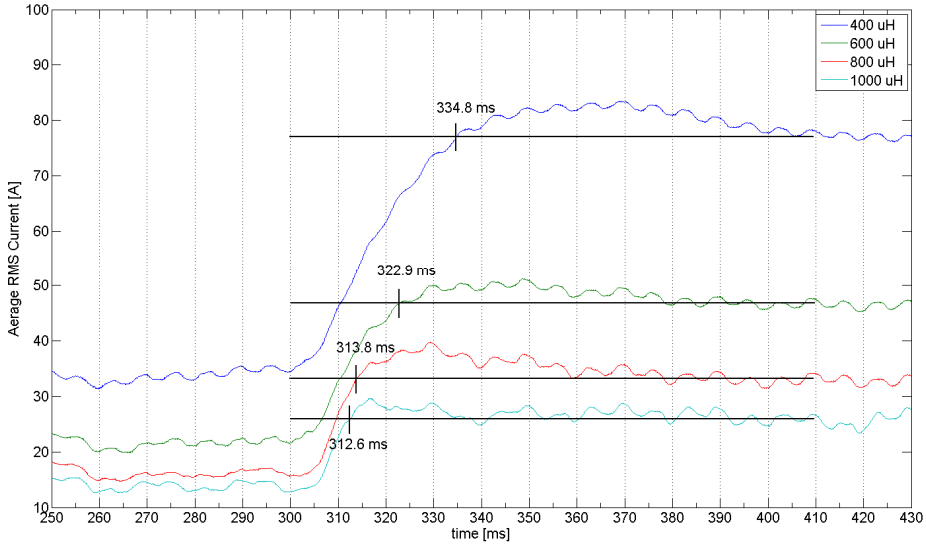


Figure 6.21 Response of the controller as a function of the system impedance.

6.6. Unbalance Mitigation

The unbalance controller was tested by using the same transmission-line in the experiments of the reactive compensator. The voltage unbalance is usually low in any normal network and unbalance had to be created. Unbalance was created by connecting a load to the line, similarly as what was done in the reactive compensator experiments. The main difference here was that the load was connected in a delta configuration and it was unbalanced. It was necessary to use a delta configuration as this would not cause neutral currents to flow. Figure 6.22 shows the schematic of the experimental setup for these experiments. The unbalanced load then caused an unbalanced voltage drop across the line impedance causing the inverter to experience an unbalanced voltage.

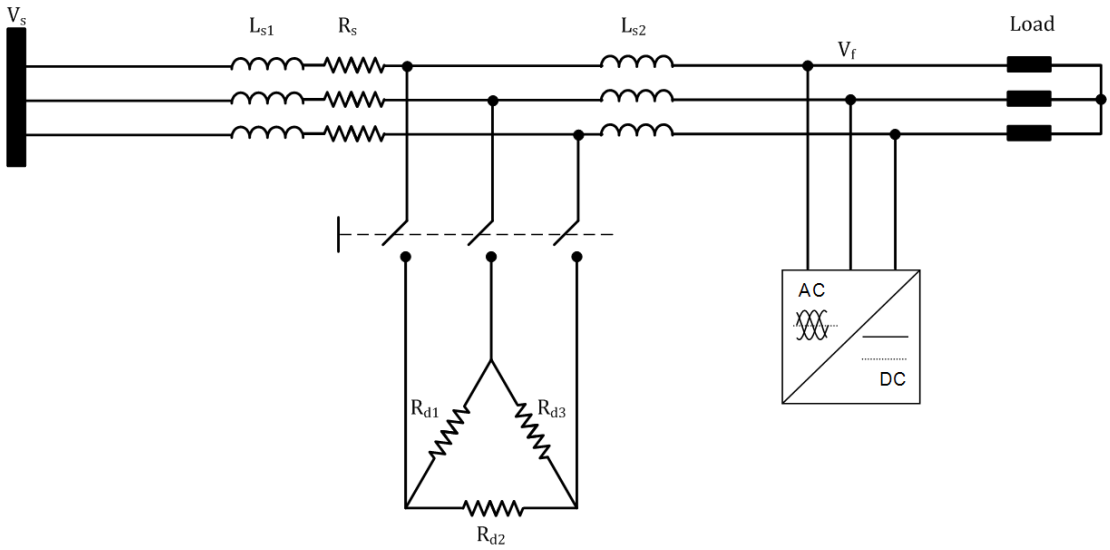


Figure 6.22 - The system used to test the unbalance voltage compensator as used in simulations and practically.

The inverter was expected to generate unbalanced reactive current such that the three-phase voltages are balanced and the negative sequence voltage will become zero. The average value of the voltage was expected to be at the reference value as for the reactive compensation experiments. This was because the positive and negative sequence controllers were both implemented and set to function in parallel.

In the experiment that follows the values of the components shown in figure 6.22 were as follows: L_{s1} = 200 µH, L_{s2} = 800 µH and R_s = 0.16 Ω. The resistance values used to generate the unbalanced dips are given in section 6.6.2.

Component	**Value**
L_{s1}	200 µH
R_s	0.16 Ω
L_{s1}	800 µH

Table 6.4 - Component values used in unbalance mitigation tests.

6.6.1. Regulation

The first test was done by allowing the inverter to control both sequences while no additional unbalance was created. The percentage voltage unbalance is shown before and after compensation in figures 6.23 and 6.24 respectively.

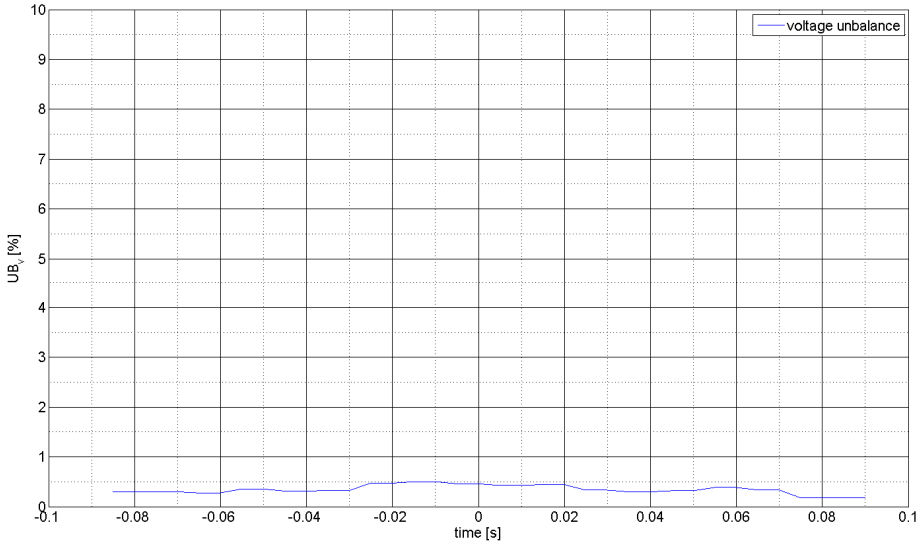


Figure 6.23 - The percentage voltage unbalance before unbalance compensation.

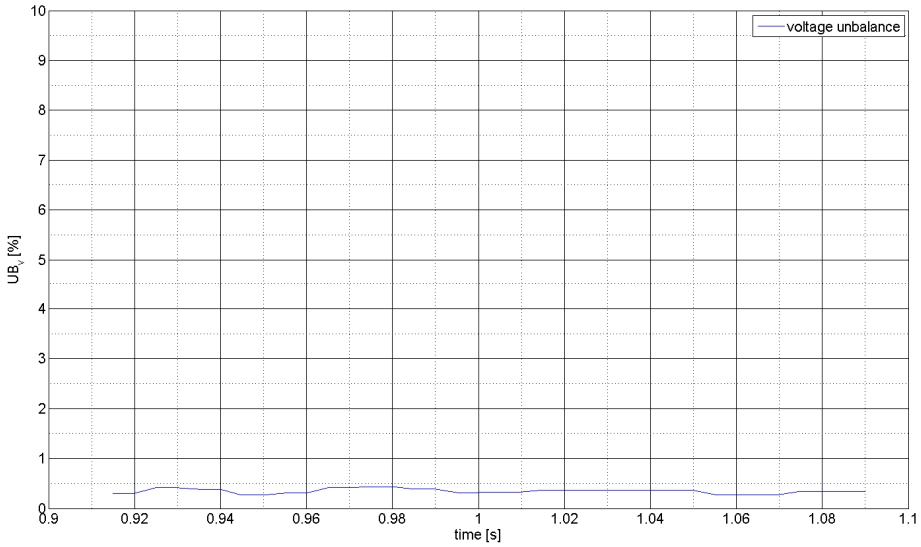


Figure 6.24 - The percentage voltage unbalance after unbalance compensation.

In both cases no unbalance was created and the voltage unbalance was found to be less than 0.5 % before and after compensation. Generating large unbalance showed that the inverter can reduce voltage unbalance at the point of regulation to this level by generating unbalanced reactive current. This is shown in the next section.

6.6.2. Unbalanced Dips

Different levels of unbalance, well outside the regulatory specifications, were generated and compensated for. One unbalanced dip used to illustrate the working of the unbalance compensator and was generated by choosing the dip generating load, in figure 6.22, as shown in table 6.3.

Resistor	R_{d1}	R_{d2}	R_{d3}
Value	∞	∞	5 Ω

Table 6.5 - The delta load resistances for the unbalance compensation test.

The percentage voltage unbalance, before compensation, is shown in figure 6.25 and shows the unbalance increase to 7.75 % when the load was connected.

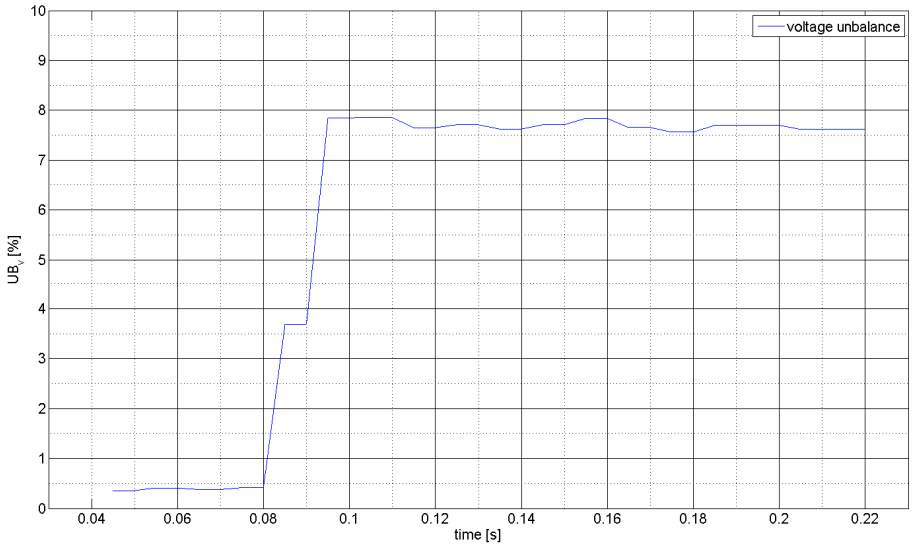


Figure 6.25 - The percentage voltage unbalance, before compensation, during the generated dip.

The voltage unbalance with the controller enabled is shown in figure 6.26. This figure shows the unbalance peak at 2.5 %. Further in time the voltage unbalance was reduced to 0.5 % as shown by figure 6.27. At this stage the inverter's three phase currents were: I_a = 57.5 A_{RMS}, I_b = 103.4 and A_{RMS} I_c = 50.4 A_{RMS}.

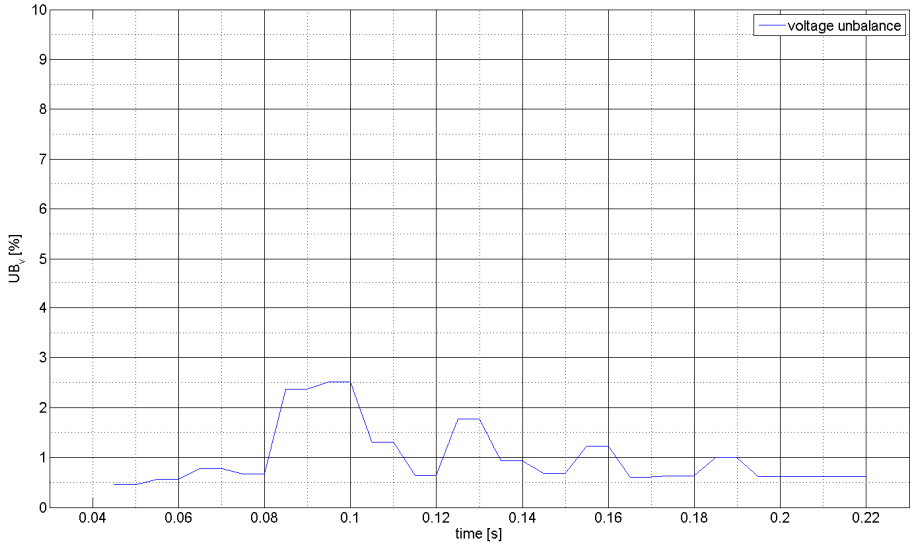


Figure 6.26 - The percentage voltage unbalance, with compensation, during the dip of the third test.

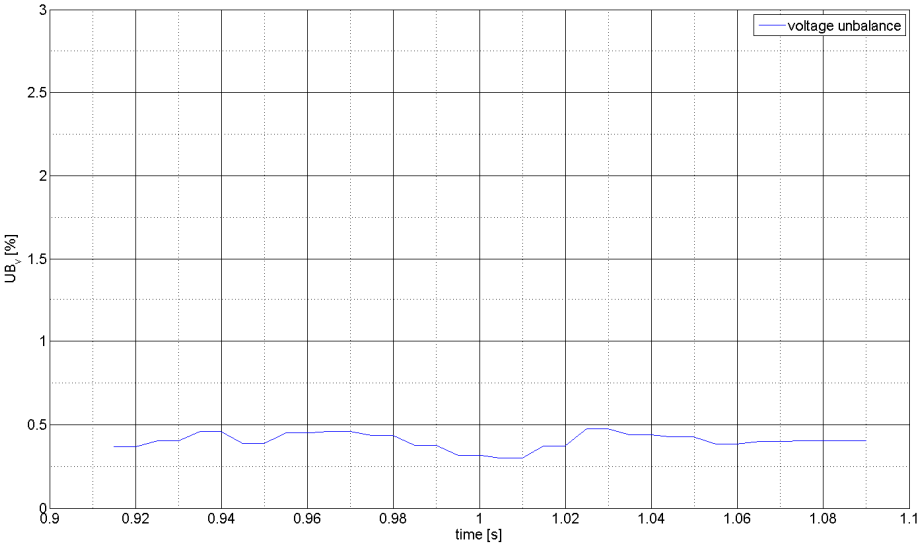


Figure 6.27 - The percentage voltage unbalance during steady state conditions with compensation.

The controller was able to reduce the voltage unbalance to well within the specifications of the NRS-048, which is 2 %. In all cases the steady state unbalance was reduced to 0.5 % or less.

6.6.3. Dynamic Performance

All the tests or experiments above were done by subjecting the controller to a step change. Step changes in voltage of the magnitude done here may not be the norm in practice. In practice the changes are either more gradual or smaller in magnitude. These tests prove that the controller is able to compensate sufficiently for these step changes. More importantly these tests prove that the controller remains stable during such changes.

6.7. Performance

The overall performance of the system, compensating for the average voltage as well as the voltage unbalance, conforms to the initial design specifications. The two compensation controllers are implemented in parallel. The two were able to function independently and the option exists to implement either the reactive compensator or the unbalance compensator separately. In the experiments described in section 6.6 both these controllers were implemented and enabled showing that parallel implementation is indeed possible.

Chapter 7: Conclusions

This chapter concludes the thesis and all activities performed in the process of carrying out this project are described. The major activities and their implications are discussed here.

Throughout this thesis many observations were made and conclusions reached. Most of the conclusions are related to the functioning of the VSI and implementation of the control algorithms on the controller of the VSI. Here follows the activities, observations and conclusions.

7.1 General

Some research needed to be done on the general operation of the VSI. The various reference frame transformations and specific PWM techniques were examined. Once the operation principles were known the design and implementation of the various controllers could be done. The knowledge gained could be applied to the rest of the project that followed.

Literature suggested that static VAR generators compensate for losses in the inverter by regulating the DC-bus at a specific level. It was necessary to design and implement a DC-bus controller to do this. This could be effectively incorporated into the functioning of the UPS as the same controller was used to condition its battery bank.

Some thought went into designing the tests and simulations as to generate scenarios similar to what would be expected in practical situations.

Ultimately a UPS was equipped with the ability to compensate for voltage dips and voltage unbalance simultaneously while still maintaining its original functionality.

In the sections that follow a summary can be found of what was done, accomplished and concluded during the research.

7.2 Dead-Time Compensation

Literature suggested that dead-time affects the operation of an inverter. The consequences of dead-time were identified and quantified. By using existing dead-time compensation methods and expanding them a very distinct improvement in the converter's performance could be seen. The current reference is tracked with a substantially smaller error showing an almost 25 % decrease in the tracking error. An improvement in the THD of the current could also be measured. It was decided to do the following to effectively improve the dead-time in the inverter:

- Mathematically derive and quantify the effect of dead-time on the VSI. Extend the derivation to areas not considered by other literature.
- Implement an existing compensation method using a linear slope in the zero crossing region of the inverter current.
- Determine the relationship between dead-time and the specific IGBT current.
- Derive and implement a new technique to compensate dynamically for different levels of IGBT current.
- Verify the effect and results of the compensation technique with simulation and practical experiments.

The result is a VSI that can be operated over a much wider range. The dynamic compensation technique ensures the correct amount of compensation is done over the entire operating range of the VSI. An improved THD means that the quality of the power generated by a VSI with this dead-time compensation is improved. The conclusion reached here is that dead-time compensation should be done to every inverter to increase efficiency.

7.3 Dead-Beat Current Controller

A current controller was needed to control the inverter so that whatever the reference current was, it would be generated at the output of the inverter. A dead-beat current

controller was decided on as it shows superior performance and can be fairly easily designed. The decision was to do the following:

- Derive, design and implement a control algorithm for a dead-beat current controller.
- Derive and implement a suitable compensation method for the inherent period delay and the computation delay.
- Verify the operation of the controller with simulations and practical experiments.

The current controller controls the inverter such that any reference current is realized by the inverter. Together with dead-time compensation the current controller can be modelled as a pure delay with unity gain making the design of external control-loops easier.

7.4 Dip Mitigation

Dip mitigation required the design of an external control-loop that would command the inverter to generate the correct amount of reactive power in order to correct the voltage level. The main activities here were as listed below.

- Studying the origin and effect of voltage dips.
- Studying different voltage dip compensation methods.
- Studying different shunt reactive compensators.
- Analysing the environment in which the compensator is to be implemented.
- Designing and implement a suitable voltage controller, incorporating a regulation slope.
- Setting up suitable simulation and practical environments.
- Verifying the working of the compensator with simulations and practical experiments.

Voltage dips were successfully mitigated using the UPS and the reactive compensation algorithm. Regulation to various levels was also tested and found to be successful. It can also be concluded that optimal response is only possible trough accurate knowledge of the system impedance.

7.5 Unbalance Mitigation

A thorough understanding of the dip compensator made the extension to the unbalance compensator easier. Some implementation issues required a careful approach to ensure safe and correct functioning of the control algorithm. The major activities consisted of:

- Studying the origin and effect of voltage unbalance.
- Studying conventional unbalance compensation techniques.
- Studying the application of static compensators on unbalanced systems.
- Studying sequence decomposition techniques.
- Evaluating delayed signal cancellation sequence detection algorithm.
- Analysing the unbalanced system in which the compensator is to be implemented.
- Setting up suitable simulation and practical environments.
- Designing and implementing a suitable voltage controller to mitigate voltage unbalance.
- Implementing a modified reference frame to ensure good operation.
- Verifying the working of the compensator with simulations and practical experiments.

Unbalanced voltage was compensated for successfully. The steady state levels were below 0.5 % which is well below 2 % specified by NRS. Very fast response to voltage unbalance is not essential but may depend on the specific application and environment.

Bibliography

[1] European Copper Institute. (2001, Mar.) Voltage Dips Introduction (5.1). Power Quality Application Guide.

[2] Eskom, "Electicity Supply - Quality of Supply Part 2: Voltage characteristics, compatibility (NRS 048-2)," Standards South Africa Rationalized User Specification ISBN 0-626-15823-0, 2004.

[3] European Copper Institute. (2002, May) Voltage Disturbances Introduction to Unbalance. Power Quality Application Guide.

[4] V. Gosbell, S. Perera, and V. Smith, "Voltage Unbalance," University of Wollongong Technical Note, Oct. 2002.

[5] P. Pillay and M. Manyage, "Definitions of Voltage Unbalance," *IEEE Power Engineering Review*, pp. 50-51, May 2001.

[6] J. A. Ghijselen and A. P. Van den Bossche, "Exact Voltage Unbalance Assessment Without Phase Measurements," *IEEE Transactions on Power Systems*, vol. 20, no. 1, pp. 519-520, Feb. 2005.

[7] P. Gnacinski, "Effect of unbalanced voltage on windings temperature, operational life and load carrying capacity of induction machine," *Science Direct Energy Conversion and Management*, vol. 49, pp. 761-770, 2008.

[8] M. Chindris, A. Cziker, A. Miron, and H. Balan, "Propogation of Unbalance in Electric Power Systems," *Electrical Power Quality and Utilisation*, vol. 9, Oct. 2007.

[9] C. Rong, "Analysis of STATCOM for Voltage Dip Mitigation," M.Sc.Eng Thesis, Chalmers University of Technology, Göteborg, 2004.

[10] European Copper Institute. (2001, Mar.) Voltage Dips Voltage Dip Mitigation. Power Quality Application Guide.

[11] M. Bongiorno, "On Control of Grid-connected Voltage Source Converters," PhD Thesis, Chalmers University of Technology, Goteborg, 2007.

[12] Y. Deng, "Reactive Power Compensation of Transmission Lines," Concordia University MASc.

[13] N. G. Hingorani and L. Gyugyi, *Understanding FACTS: concepts and technology of flexible AC transmission systems*. New York, United States of America: Wiley-IEEE Press, 1999.

[14] S. A. Larrinaga, "Predictive Control of the 2L-VSI and 3L-NPC VSI," PhD Thesis, University of Mondragon, 2007.

[15] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, 1st ed., J. Hudgins, Ed. United States of America: Morgan & Claypool, 2006.

[16] L. De Wit, "Flicker Mitigation in Industrial Systems," MSc Thesis, Stellenbosch University, Stellenbosch, 2006.

[17] I. Hobbs, H. J. Beukes, and F. Koeslag, "Analytical Characterization of Dead Time in the Zero-Crossing Region of the Inductor Current," in *IEEE Africon*, Nairobi, 2009, pp. 1-7.

[18] D. Leggate and R. J. Kerkman, "Pulsed Based Dead Time Compensator for PWM Voltage Inverters," Allen-Bradley Co Paper.

[19] Semikron. SKiM400GD128D. Datasheet.

[20] K. H. Ahmed, S. J. Finney, and B. W. Williams, "Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation," *Electrical Power Quality and Utilisation*, vol. XIII, no. 2, pp. 49-58, 2007.

[21] S. Buso, S. Fasolo, and P. Mattavelli, "Uninterruptible Power Supply Multiloop Control Employing Digital Predictive Voltage and Current Regulators," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1846-1854, Nov. 2001.

[22] J. D. Glover and M. S. Sarma, *Power System Analysis and Design*. California, United States of America: Thomson Learning, 2002.

[23] Y. Xu and J. D. Kueck, "Voltage and Current Unbalance Compensation Using a Parallel Active Filter," *IEEE*, pp. 2919-2925, 2007.

[24] C. Hochgraf and R. H. Lasseter, "StatCom Controls for Operation with Unbalanced Voltages," *IEEE*, 1997.

[25] R. Cutri and L. Matakas, "Reference Currents Determination Techniques for Load Unbalance Compensation," in *COBEP*, 2003, pp. 864-869.

[26] A. Akdag, S. Tadakuma, and H. Minakata, "Load Balancing Control by Symmetrical Coordinates Frame for PWM Inverter Based Reactive Power Compensators," *T.IEE Japan*, vol. 121-D, no. 1, pp. 43-51, 2001.

[27] J. Svensson, M. Bongiorno, and A. Sannino, "Practical Implementation of Delayed Signal Cancellation Method for Phase-Sequence Seperation," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 18-26, Jan. 2007.

[28] M. Bongiorno, J. Svensson, and A. Sannino, "Effect of Sampling Frequency and Harmonics on Delay-Based Phase-Sequence Estimation Method," *IEEE*

Transactions on Power Delivery, vol. 23, no. 3, pp. 1644-1672, Jul. 2008.

Appendix A

Dead-Time Compensation

This appendix shows the derivation of the compensation algorithms for dead-time when a short pulse is experienced. This would mean that the switches in a phase-arm are unable to change their state. A switch is unable to change its state if the pulse on its gate is too short. In terms of the duty cycle this means that if the duty cycle is too low the top switch cannot turn-on and if the duty cycle is too high the bottom switch cannot turn on. Based on the discussion in chapter 3 the minimum duty cycle is D_e and the maximum is $1 - D_e$. D_e is the error in duty cycle due to dead-time.

The four possible states of a phase experiencing such a short pulse are discussed below.

First consider the ideal phase-phase voltages shown below. These are calculated assuming that the switches are ideal and can be turned on and off for the exact times. The reference times refer to the time that the top switch in a phase-arm is on.

$$V_{ab}^{*} = V_d\left(\frac{t_a^{*}}{T_s} - \frac{t_b^{*}}{T_s}\right) \quad \text{A.1}$$

$$V_{bc}^{*} = V_d\left(\frac{t_b^{*}}{T_s} - \frac{t_c^{*}}{T_s}\right) \quad \text{A.2}$$

$$V_{ca}^{*} = V_d\left(\frac{t_c^{*}}{T_s} - \frac{t_a^{*}}{T_s}\right) \quad \text{A.3}$$

Assume the current in phase A and B is positive and negative in phase C. Also assume that the reference time for phase A is as shown below.

$$t_a^{*} \leq T_e \quad \text{A.4}$$

Taking dead-time into consideration the on-time for each phase is as shown below.

$$t_a \leq T_e - T_e \rightarrow 0 \quad \text{A.5}$$

$$t_b = t_b^* - T_e \quad \text{A.6}$$

$$t_c \leq t_c^* + T_e \quad \text{A.7}$$

Using these times the various phase-phase voltages can be calculated as shown below.

$$V_{ab} = V_d\left(\frac{-t_b^*}{T_s} + \frac{T_e}{T_s}\right) \quad \text{A.8}$$

$$V_{bc} = V_d\left(\frac{t_b^*}{T_s} - \frac{t_c^*}{T_s} - \frac{2T_e}{T_s}\right) \quad \text{A.9}$$

$$V_{ca} = V_d\left(\frac{t_c^*}{T_s} + \frac{T_e}{T_s}\right) \quad \text{A.10}$$

The difference between these equations and the ideal equations will yield the appropriate compensation.

In the case of voltage V_{ab} it is evident that the compensation should be done in phase B since phase A is un-switchable. This means that the time t_b should be altered in order for the realized voltage to be the same as the ideal reference. Similarly for voltage V_{ca} the compensation needs to be done in phase C and t_c should be compensated.

Substituting t_b^* with t_b^{comp} and comparing the times from equations A.1 and A.8 give the following equality. Making the compensated time, t_b^{comp}, the subject gives the appropriate compensation algorithm.

$$\begin{aligned} -t_b^{comp} + T_e &= t_a^* - t_b^* \\ t_b^{comp} &= t_b^* - (t_a^* - T_e) \end{aligned} \quad \text{A.11}$$

A similar procedure with equations A.2 and A.9 yield the following result for phase C.

$$\begin{aligned} t_c^{comp} + T_e &= t_c^* - t_a^* \\ t_c^{comp} &= t_c^* - (t_a^* + T_e) \end{aligned} \quad \text{A.12}$$

Therefore if the duty cycle is too low in a phase conducting a positive current then the compensation in the other two phases should be as follows, depending on the current in these other phases.

If $I_p > 0$:

$$t_p^{comp} = t_p^* - (t_{short}^* - T_e) \quad \text{A.13}$$

If $I_p < 0$:

$$t_p^{comp} = t_p^* - (t_{short}^* + T_e) \quad \text{A.14}$$

If the same approach as above is followed the compensation algorithms can be derived for other cases. These are for when the low duty cycle is in a phase with a negative current and when the duty cycle is too high in a phase with positive or negative current.

Consider the case where the system is in the same state as the one above except for phase A that has a negative current. This means that the low duty cycle is in a phase with a negative current. This means that the on-time for phase A is now calculated as shown below.

$$t_a \leq T_e + T_e \rightarrow 2T_e \quad \text{A.15}$$

Calculating the phase-phase voltages from the various on-times gives equations A.16, A.17 and A.18.

$$V_{ab} = V_d\left(\frac{-t_b^*}{T_s} + \frac{3T_e}{T_s}\right) \quad \text{A.16}$$

$$V_{bc} = V_d\left(\frac{t_b^*}{T_s} - \frac{t_c^*}{T_s} - \frac{2T_e}{T_s}\right) \quad \text{A.17}$$

$$V_{ca} = V_d\left(\frac{t_c^*}{T_s} - \frac{T_e}{T_s}\right) \quad \text{A.18}$$

Comparing the on-times with those of the ideal voltages gives the compensation terms.

$$-t_b^{comp} + 3T_e = t_a^* - t_b^*$$
$$t_b^{comp} = t_b^* - (t_a^* - 3T_e) \quad \text{A.19}$$

$$t_c^{comp} - T_e = t_c^* - t_a^*$$
$$t_c^{comp} = t_c^* - (t_a^* - T_e) \quad \text{A.20}$$

Therefore if the duty cycle is too low in a phase conducting a negative current then the compensation in the other two phases should be as follows, depending on the current in these other phases.

If $I_p > 0$:

$$t_p^{comp} = t_p^* - (t_{short}^* - 3T_e) \quad \text{A.21}$$

If $I_p < 0$:

$$t_p^{comp} = t_p^* - (t_{short}^* - T_e) \quad \text{A.22}$$

Consider the case where the duty cycle in phase A is too high and this phase is conducting a positive current. The other currents are assumed to be as in the first case. The on-time for phase A is then calculated as follows.

$$t_a \geq T_s - T_e - T_e \rightarrow T_s - 2T_e \quad \text{A.23}$$

Calculating the phase-phase voltages yield the following.

$$V_{ab} = V_d\left(\frac{-t_b^*}{T_s} - \frac{T_e}{T_s} + \frac{T_s}{T_s}\right) \quad \text{A.24}$$

$$V_{bc} = V_d\left(\frac{t_b^*}{T_s} - \frac{t_c^*}{T_s} - \frac{2T_e}{T_s}\right) \quad \text{A.25}$$

$$V_{ca} = V_d\left(\frac{t_c^*}{T_s} + \frac{3T_e}{T_s} - \frac{T_s}{T_s}\right) \quad \text{A.26}$$

Comparing the on-times with those of the ideal voltages gives the compensation terms.

$$-t_b^{comp} - T_e + T_s = t_a^* - t_b^*$$
$$t_b^{comp} = t_b^* - (t_a^* - T_s + T_e) \quad \text{A.27}$$

$$t_c^{comp} + 3T_e - T_s = t_c^* - t_a^*$$
$$t_c^{comp} = t_c^* - (t_a^* - T_s + 3T_e) \quad \text{A.28}$$

Therefore if the duty cycle is too high in a phase conducting a positive current then the compensation in the other two phases should be as follows, depending on the current in these other phases.

If $I_p > 0$:

$$t_p^{comp} = t_p^* - \left(t_{long}^* - T_s + T_e\right) \quad \text{A.29}$$

If $I_p < 0$:

$$t_p^{comp} = t_p^* - \left(t_{long}^* - T_s + 3T_e\right) \quad \text{A.30}$$

The only remaining case is for when the duty cycle is too high in a phase and the current in that phase is negative. Assume this phase to be phase A again and the other phases are as in all the cases above. The on-time for phase A is then calculated as follows.

$$t_a \geq T_s - T_e + T_e \rightarrow T_s \quad \text{A.31}$$

Calculating the phase-phase voltages yield the following.

$$V_{ab} = V_d \left(\frac{-t_b^*}{T_s} + \frac{T_e}{T_s} + \frac{T_s}{T_s}\right) \quad \text{A.32}$$

$$V_{bc} = V_d \left(\frac{t_b^*}{T_s} - \frac{t_c^*}{T_s} - \frac{2T_e}{T_s}\right) \quad \text{A.33}$$

$$V_{ca} = V_d\left(\frac{t_c^*}{T_s} + \frac{T_e}{T_s} - \frac{T_s}{T_s}\right) \quad \text{A.34}$$

Comparing the on-times with those of the ideal voltages gives the compensation terms.

$$\begin{aligned} -t_b^{comp} + T_e + T_s &= t_a^* - t_b^* \\ t_b^{comp} &= t_b^* - (t_a^* - T_s - T_e) \end{aligned} \quad \text{A.35}$$

$$\begin{aligned} t_c^{comp} + T_e - T_s &= t_c^* - t_a^* \\ t_c^{comp} &= t_c^* - (t_a^* - T_s + T_e) \end{aligned} \quad \text{A.36}$$

Therefore if the duty cycle is too high in a phase conducting a positive current, then the compensation in the other two phases should be as follows depending on the current in these other phases.

If $I_p > 0$:

$$t_p^{comp} = t_p^* - \left(t_{long}^* - T_s - T_e\right) \quad \text{A.37}$$

If $I_p < 0$:

$$t_p^{comp} = t_p^* - \left(t_{long}^* - T_s + T_e\right) \quad \text{A.38}$$

To summarize assume that the I_k denotes a phase, k, that experiences an un-switchable time. It may be either too high or too low to be switched. The compensation algorithms are summarized in the table below where p denotes any phase except phase k.

		$I_p > 0$	$I_p < 0$
$I_k > 0$	D_k low	$t_p^{comp} = t_p^* - (t_k^* - T_e)$	$t_p^{comp} = t_p^* - (t_k^* + T_e)$
	D_k high	$t_p^{comp} = t_p^* - (t_k^* - T_s + T_e)$	$t_p^{comp} = t_p^* - (t_k^* - T_s + 3T_e)$
$I_k < 0$	D_k low	$t_p^{comp} = t_p^* - (t_k^* - 3T_e)$	$t_p^{comp} = t_p^* - (t_k^* - T_e)$
	D_k high	$t_p^{comp} = t_p^* - (t_k^* - T_s - T_e)$	$t_p^{comp} = t_p^* - (t_k^* - T_s + T_e)$

Table A.1 - Dead-time compensation summarized.

Appendix B

Reactive Compensator *[C-code]*

```
/* Reactive Compensation */

r_Vac = 400.0*1.0*cp_Vac - cRS*mIfQ;

/* Reference voltage with regulation slope */


Irc_p = cAp*cID*cDV*(r_Vac - f_mVf);

                  /* Proportional term    */

Irc_p = min( (cRCSS*360.0*cAD*cRMSA*cID),
      max((-360.0*cRCSS*cAD*cRMSA*cID),Irc_p));

Irc_i += cAi*cID*cDV*(r_Vac - f_mVf);

                  /* Integral term        */

Irc_i = min( (360.0*cRCSS*cAD*cRMSA*cID-fabs(Irc_p)),
      max((-360.0*cRCSS*cAD*cRMSA*cID+fabs(Irc_p)),Irc_i));

                  /* Integral anti-windup */

r_outp_Ifp = Irc_p + Irc_i;
r_outp_Ifp = max(-360.0*cRCSS*cAD*cRMSA*cID,r_outp_Ifp);
r_outp_Ifp = min( 360.0*cRCSS*cAD*cRMSA*cID,r_outp_Ifp);

/* Set alpha-beta components for positive reactive current */
r_outp_Ifpd =      r_outp_Ifp*sinwtf;
r_outp_Ifpq = -1.0*r_outp_Ifp*coswtf;


/* Reactive Compensation - Done */
```

Appendix C

Sequence Decomposition *[C-code]*

```
/* DSC with Reduction of Detection Error by Weighted Mean Value */

weight  = 1250.0/(freq_dsc);
n_delay = (int)floor(weight);

delay_1 = (30 + (delay_count - n_delay))%30;

delay_2 = (30 + (delay_count - (n_delay+1)))%30;

weight = 1.0 - (25.0 - weight);
weight = (weight>1.0?weight:1.0);
weight = (weight<0.0?weight:0.0);

mVfd_p = weight*0.5*(mVfd - mVfq_array[delay_1])
       + (1.0 - weight)*0.5*(mVfd - mVfq_array[delay_2]);

mVfq_p = weight*0.5*(mVfq + mVfd_array[delay_1])
       + (1.0 - weight)*0.5*(mVfq + mVfd_array[delay_2]);

mVfd_n = weight*0.5*(mVfd + mVfq_array[delay_1])
       + (1.0 - weight)*0.5*(mVfd + mVfq_array[delay_2]);

mVfq_n = weight*0.5*(mVfq - mVfd_array[delay_1])
       + (1.0 - weight)*0.5*(mVfq - mVfd_array[delay_2]);

mVfd_array[delay_count] = mVfd;
mVfq_array[delay_count] = mVfq;

delay_count  = (delay_count + 1)%30;

/* Positive sequence */

mVfp   = sqrt(mVfd_p*mVfd_p + mVfq_p*mVfq_p);
f_mVfp += 0.0715390456*(mVfp - f_mVfp);
f_mVfp = max(1.0,f_mVfp);

coswtp = mVfd_p/f_mVfp;
sinwtp = mVfq_p/f_mVfp;

/* DSC - Done */
```

Appendix D

Unbalance Compensator *[C-code]*

```
/* Unbalance Compensation */

fmVfn_D += 0.0715390456*((mVfd_n*coswtp - mVfq_n*sinwtp) - fmVfn_D);

Iubc_pD = cAp*cID*cDV*(0.0 - fmVfn_D);

                  /* Proportional term    */

Iubc_pD = min( (cRCSS*360.0*cAD*cRMSA*cID),
        max((-360.0*cRCSS*cAD*cRMSA*cID),Iubc_pD));

Iubc_iD += cAi*cID*cDV*(0.0 - fmVfn_D);

                  /* Integral term        */

Iubc_iD = min( (360.0*cRCSS*cAD*cRMSA*cID-fabs(Iubc_pD)),
        max((-360.0*cRCSS*cAD*cRMSA*cID+fabs(Iubc_pD)),Iubc_iD));

                  /* Integral anti-windup */

r_outp_IfnD = Iubc_pD + Iubc_iD;
r_outp_IfnD = max(-360.0*cRCSS*cAD*cRMSA*cID,r_outp_IfnD);
r_outp_IfnD = min( 360.0*cRCSS*cAD*cRMSA*cID,r_outp_IfnD);


fmVfn_Q += 0.0715390456*((mVfd_n*sinwtp + mVfq_n*coswtp) - fmVfn_Q);

Iubc_pQ = cAp*cID*cDV*(0.0 - fmVfn_Q);

                  /* Proportional term    */

Iubc_pQ = min( (cRCSS*360.0*cAD*cRMSA*cID),
        max((-360.0*cRCSS*cAD*cRMSA*cID),Iubc_pQ));

Iubc_iQ += cAi*cID*cDV*(0.0 - fmVfn_Q);

                  /* Integral term        */

Iubc_iQ = min( (360.0*cRCSS*cAD*cRMSA*cID-fabs(Iubc_pQ)),
        max((-360.0*cRCSS*cAD*cRMSA*cID+fabs(Iubc_pQ)),Iubc_iQ));

                  /* Integral anti-windup */

r_outp_IfnQ = Iubc_pQ + Iubc_iQ;
r_outp_IfnQ = max(-360.0*cRCSS*cAD*cRMSA*cID,r_outp_IfnQ);
r_outp_IfnQ = min( 360.0*cRCSS*cAD*cRMSA*cID,r_outp_IfnQ);


/* Transform from d-q to alpha-beta and add 90 degree phase shift */

r_outp_Ifnd = -1.0*(-1.0*r_outp_IfnD*sinwtp + r_outp_IfnQ*coswtp);
r_outp_Ifnq =      (     r_outp_IfnD*coswtp + r_outp_IfnQ*sinwtp);

/* Unbalance Compensation - Done */
```