Study on the Connection Between the Set Transient in RRAMs and the Progressive Breakdown of Thin Oxides

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Abstract— In this paper, the transition rate (TR) from the high-resistance state to the low-resistance state of a HfO$_2$-based resistive random access memory (RRAM) is investigated. The TR is statistically characterized by applying constant voltage stresses in the range from 0.45 to 0.65 V. It is found that TR follows a voltage dependence which closely resembles the one exhibited by metal-insulator-semiconductor / metal-insulator-metal structures when subjected to constant voltage stress, but with remarkably different fitting parameters. This result suggests a common underlying mechanism in both evolutionary behaviors. Furthermore, the investigation provides additional evidence supporting the micro-structural changes in the oxide after the forming step as well as the role played by the atomic species during the SET event.

Index Terms— High-*k*, progressive oxide breakdown, resistive random access memory (RRAM), resistive switching (RS).

I. Introduction

RESISTIVE random access memory (RRAM) is attracting considerable interest as a promising future technology for scalable memory [1] and neuromorphic computing systems [2]. RRAM relies on the formation and dissolution of a nanoscale conductive filament (CF) spanning an insulating layer, typically a binary transition-metal oxide, such as NiO [3], TiO$_x$ [4], HfO$_x$ [5], and TaO$_x$ [6], among others. The CF is initially generated by a forming operation, namely, a controlled dielectric breakdown (BD) of the insulating layer using an appropriate current compliance level [7]. A small gap in the localized CF, which is responsible for the low-resistance state (LRS) in the memory device, is then opened through a RESET operation causing the transition from the LRS to the high-resistance state (HRS) and closed with a SET operation (HRS to LRS transition). SET/RESET operations can be achieved via electrical pulses of the same or opposite polarities (unipolar/bipolar switching modes, respectively). The resistive switching (RS) mechanism has been widely studied in the last years [1]–[12], and many authors claim that the SET/RESET processes are described through ion migration induced by the local electric field and the temperature increase associated with Joule heating [10]. Ion migration is modeled by diffusion and drift components, where both rely on hopping mechanisms. Ions move along an energy landscape of potential wells, which provide states for ion localization [11], [12].

On the other hand, the main physical mechanism behind the BD dynamics of ultra-thin dielectrics (Al$_2$O$_3$, HfO$_2$, SiO$_2$, and Si$_3$N$_4$) used in a CMOS technology was recently identified [13], [14]. Briefly, the energy transfer from the CF to its surroundings promotes the diffusion of the fastest atomic species, which gradually enlarges the CF connecting the electrodes of the stack causing a progressive increase in the leakage current. Remarkably, SET and BD events show the same statistical behavior [9] and similar micro-structural changes in the dielectric [15]–[19]. Several authors [15]–[17] showed that the BD spot is characterized by the formation of a Si-rich region (for poly-Si/SiO$_x$N$_y$/Si stacks) or a metal-rich region (for metal gate/high-K/Si stacks) in the gate dielectric. In this regard, Privitera *et al.* [18] have shown the presence of metallic species in the oxide for the case of HfO$_2$-based RRAM MIM devices after forming.

In particular, a huge amount of research has been carried out regarding the static *I–V* characteristics of the RRAMs. However, the time evolution of the switching phenomenon
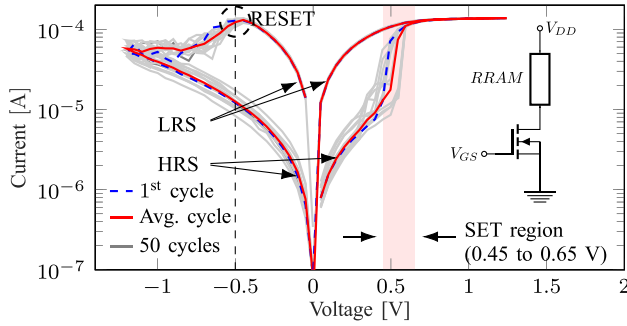
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Fig. 1. *I–V* characteristics for the samples under test (50 curves). The red solid line is the average curve, and the blue dashed one stands for the first cycle. The inset in the right side shows the 1T1R assembly, comprising the RRAM structure and its driving nMOS transistor.

is not completely understood yet. In this context, it is clear that despite the recent advances regarding the modeling of the current–voltage behavior of the RS devices [9], [20], more information about the SET event in RRAM devices is needed. Detailed knowledge of the evolution of the CF morphology during forming and SET transitions, as well as the corresponding shape of the I–V curves, is needed to accurately model the switching phenomena and to make reliability predictions. Ultimately, the study of the voltage–time dependence of RS is needed to estimate the minimum time required for writing a bit in an RRAM cell [21]. In this paper, the HRS to LRS transition is studied as a function of time and switching voltage using a large number of measurements. Based on a physical description of the BD dynamics in the dielectrics of common use in the CMOS processes and the aforementioned similarities to the SET event in RRAM, a model for the time evolution of the resistive state of the RRAM as a function of the switching voltage is proposed.

II. EXPERIMENT

Experimental data were obtained from HfO_2-based RRAM cells. The MIM structure consists of a 10-nm-thick atomic-layer-deposited HfO_2 film sandwiched between Ti and TiN electrodes. The cell is connected in series with an n-type MOSFET, embedding a one-transistor–one-resistor (1T1R) structure, as shown in Fig. 1 (inset). The transistor controls the maximum current that can flow through the memory cell, which in turn determines the resistance window of the device [7], [22]. All the measurements were performed by applying a gate–source voltage (V_{GS}) of 1.2 V. Quasi-static I–V–t measurements were performed using a Keithley 4200-SCS equipped with a fast measurement and pulse generator unit (4225-RPM) capable of providing an appropriate time resolution (down to 200 ns in Fig. 2(b). As reported in a previous work considering similar samples [20], the forming event takes place at ≈3.8 V, and the devices exhibit bipolar switching characteristics. Notice that the average SET and RESET voltages are almost symmetric (approximately ±0.5 V). This indicates the voltage-controlled processes for HfO_2 in agreement with the previously reported results [23]. Further details about the devices and the experimental setup can be found in [9].
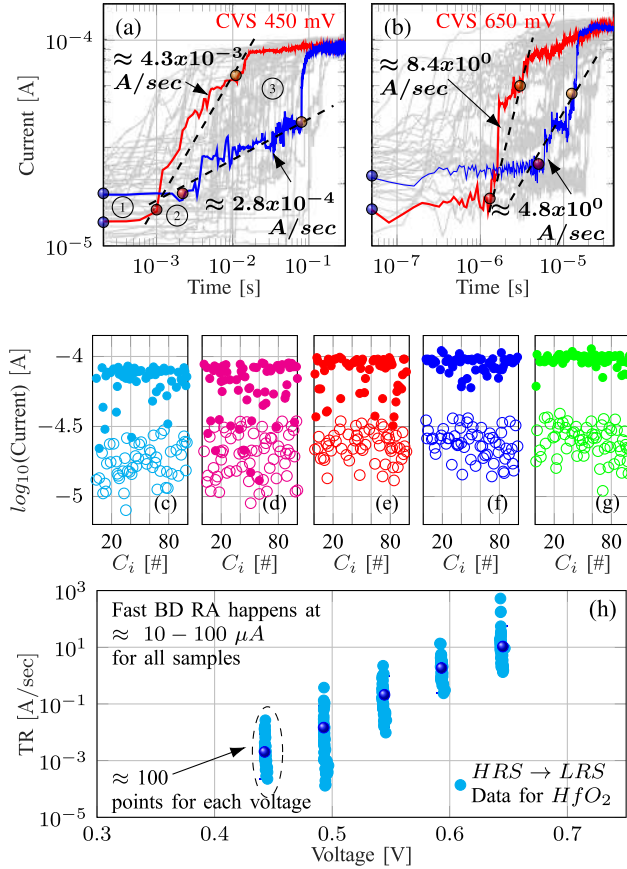

Fig. 2. Current transient of the device under tests under CVS. For clarity, only the lowest -450 mV- and highest -650 mV- voltages are shown. Ball markers 1–3 point out the initial current (I_{init}), the onset of the progressive increase of current (I_{on}), and the final jump to the compliance level (I_{end}), respectively. Initial currents (I_{init}) (empty markers) and end currents (I_{end}) (filled markers) at (c) 450, (d) 500, (e) 550, (f) 600, and (g) 650 mV. C_i in (c)–(g) stands for the cycle number. (h) TR (dI_{Tr}/dt) of the samples under test. Approximately, 100 transients and the mean value are reported for each voltage condition (450, 500, 550, 600, and 650 mV). The mean value increases roughly one order of magnitude for every 50 mV.

III. RESULTS

In order to study the SET event, the whole process, including the wear-out phase and the transition from HRS to LRS, must be explored. Therefore, current–time (I–t) measurements at constant bias were performed using the high-bandwidth setup mentioned in Section II until the fast HRS to LRS transition occurred or in other words, until the current through the device reaches the compliance limit (∼100 μA). I–t measurements were performed under a constant voltage stress (CVS) of 450, 500, 550, 600, and 650 mV. For clarity, only the transients corresponding to the 450 - and 650-mV stresses are shown in Fig. 2(a) and (b). Such stress voltages were applied in the HRS state and were chosen after the I–V curves shown in Fig. 1, where the HRS to LRS transition occurs for voltages ranging from 0.45 to 0.65 V.

Current through the MIM stack during the HRS to LRS transition (I_{Tr}) increases gradually with time [24], evidencing the progressive nature of the SET event [see Fig. 2(a) and (b)]. It is a noisy and progressive process well in agreement with the literature [7], [9], [10], [25] whose duration shows a strong

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voltage dependence and dispersion. Such dispersion will be discussed in Section IV-A. The maximal current growth rate is limited by the bandwidth of the equipment. Fig. 2(c)–(g) shows the initial (I_{init}, empty symbols) and end (I_{end}, filled symbols) currents of the acquired transients, including those shown in Fig. 2(a) and (b). It is worth mentioning that the initial current matches the I–V data shown in Fig. 1, where the SET region shows initial currents around 10 μA. I_{end} current represents the level from which the acquired transient exhibits a jump to the compliance level (see Fig. 2), leaving the sample in LRS. The time evolution of the HRS to LRS transition is quantified by the slope dI_{Tr}/dt, as defined in [13], [26], and [27]. Such a metric will be subsequently referred to as the transition rate (TR) [A/s]. The TR values were experimentally evaluated through measurements such as those of Fig. 2(a) and (b), and it is reported for approximately 100 measurements for each voltage value [see Fig. 2(h)]. The comparison between the TR in Fig. 2(a) and (b) and the trend in Fig. 2(h) suggests a strong voltage dependence, as the TR increases almost four orders of magnitude in between these two cases. Similar measurements of the HRS–LRS transition have been previously reported [25], showing a comparable voltage dependence (TR increases as the applied voltage increases).

IV. ANALYSIS AND DISCUSSION

It has been experimentally shown that both the SET and forming events in RRAM devices [9], [25] and the dielectric BD of gate oxides [13], [14] share some common aspects. Aside from the noisy and progressive increase of the leakage current, whose increase rate depends on the stressing voltage, further insight into these events reveals a few other common points. Previously reported current compliance studies have shown a clear dependence of the CF characteristics on the maximal current flowing through the device, both for the BD of gate oxides [7] and the SET event in RRAM devices [22]. In addition, transmission electron microscopy imaging of Si-based MOS capacitors prior to and post dielectric BD [15]–[17] and HfO$_2$-based RRAM cells after forming and cycling [18], [19] shows comparable micro-structural changes in the oxide, suggesting the diffusion of the anodic atomic species into the oxide layer during both events.

Thus, there are not only similar electrical characteristics between the SET event and the gate-oxide BD but also the comparable micro-structural changes and the combination of both points toward a common underlying physical mechanism. In such a scenario, we propose to model the results for the SET event in RRAM devices similar to the gate-oxide BD in MOSFETs. In this regard, Palumbo *et al.* have presented in [13] a model describing the gate-oxide BD phenomenon in ultra-thin, bulk dielectrics considering SiO$_2$ and various high-k dielectrics with different thermal conductivities deposited on II I–V and Si substrates as well as in 2-D layered materials [28], providing good understanding of the experimental data. Such a model accounts for the progressive nature of the BD event and quantifies it in terms of dI_{BD}/dt [namely the degradation rate (DR), where I_{BD} is the current through the device during the progressive BD (PBD). Regarding the physics behind this evolution, the model assumes that the BD process is closely linked to the energy transfer from the CF itself to its surrounding atomic network. According to this idea, the high temperature associated with the localized current flow (current density of a few MA/cm^2 through a BD spot area of 1–50 nm^2 [13], [15], [16]) would promote the electromigration of the fastest available atomic species, thus contributing to the enlargement of the BD filament connecting the electrodes of the stack. Such electromigration phenomena have been shown to exist in RRAM by Tang *et al.* [29]. This interpretation of the BD phenomena accounts for the dependence of the CF features on the current compliance and the presence of the anodic species in the oxide layer after BD, and therefore, it could be used to model the SET event in RRAMs.

It is worth pointing out that the TR shows an evident voltage dependence (four orders of magnitude in 200 mV) much stronger than the DR reported for the BD event (dI_{BD}/dt, 3–5 orders of magnitude per volt) [13]. To understand such a big difference, a detailed explanation of the proposed model will be given in the following sections, as well as an explanation about the parameters' change from the gate-oxide BD to the SET event case.

A. Model of the Transition Rate for HRS to LRS as Function of Voltage

Based on the experimental results and the common underlying physical mechanism that seems to govern both SET and oxide BD, a diffusion phenomenon driven by the energy transfer from the CF to its surroundings is proposed, including the voltage and oxide thickness dependence. In this context and considering the model reported in [13] for the BD transient, it is possible to express the TR for the HRS to LRS transition as follows:

$$TR = \frac{dI_{\text{Tr}}}{dt} = \frac{qVf_1}{k_B T t_{\text{ox}}^2} D I_{\text{SET}} \tag{1}$$

where t_{ox} is the oxide thickness, T is the temperature at the gap in the CF [see Fig. 3(c)], k_B is Boltzmann's constant, D is the diffusion constant of the atomic species responsible for the HRS to LRS transition, V is the applied voltage, I_{SET} is the current level at the onset of the HRS to LRS transition (SET event) as expressed in (2), and $f_1 = n_e \lambda_e \sigma_e$, with being n_e the electron density, λ_e the electron mean free path, and σ_e the cross section for the electron–atom collision (responsible for the momentum transfer). f_1 is around the unity value since the defect concentration in the CF is most likely very high [18].

From (1), dI_{Tr}/dt is proportional to $D \times I_{\text{SET}}$. This means that the CF growth rate increases either by increasing I_{SET}, the electron current, or the dominant diffusivity D. There is also a dependence on t_{ox}, V, and T. Therefore, to use (1), we need to model I_{SET} and D. In addition, the effective value of t_{ox} as well as the atomic species involved in the HRS to LRS transition will be further discussed in Sections IV-B and IV-C, respectively.

SET processes were shown to be controlled by the device I–V characteristics, which dictates the local temperature [13], [22] and drives the completion and rupture of a

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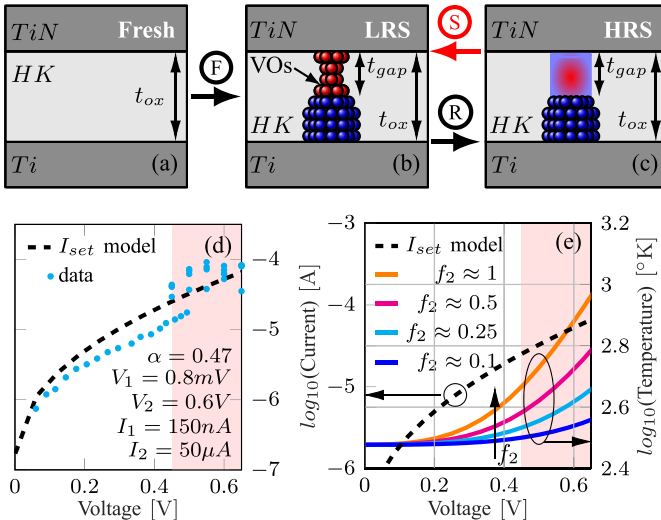

Fig. 3. Representation of the t_{ox} reduction due to the appearance of a gap in the CF. (a) before forming step. (b) LRS. (c) HRS. Blue balls represent the electrode's atomic species, and the red balls stand for the oxygen vacancies (VOs). (d) I_{SET} model described by (2) versus measurements. (e) Temperature calculations as a function of voltage and the energy loss in the CF constriction. In both (d) and (e) plots, the red shaded zone indicates the voltages employed for the CVS (0.45–0.65 V).

nanoscale CF through the insulating layer [10] [see Fig. 3(b) and (c)]. This accounts for the compliance current used to control the resistance in the SET state [10]. I_{SET} can be described by modeling the discontinuous CF [see Fig. 3(c)] as a quantum size filament with a constriction, according to the Landauer–Buttiker formalism [8], as we have previously reported [7]. However, for simplicity, we have preferred to model the $I_{SET}-V$ characteristic of the CF in HRS by assuming an interpolation equation [see (2)] [13], [28]. This avoids the use of more parameters. The fitting of our experimental data is shown in Fig. 3(d). I_1, V_1 and I_2, V_2 represent two points in the experimental $I_{SET}-V$ curve (see HRS curves in Fig. 1) at low and high voltages, respectively, while α is a fitting constant

$$I_{SET} = I_1 \exp\left(\log\left(\frac{I_2}{I_1}\right)\left(\frac{V - V_1}{V_2 - V_1}\right)^{\alpha}\right). \tag{2}$$

To model D, we first need to model the temperature T in the constriction/discontinuity of the CF. To do so, the heat diffusion equation was solved. We assumed a simplification of spherical symmetry around the CF constriction and considered the source power density to be constant over the inner surface of the sphere. The result is (3), where f_2 is the fraction of the energy qV per electron lost at the constriction, the dissipated power at the CF constriction is proportional to $I_{SET} \times V$, T_{amb} is the room temperature, and k is the thermal conductivity of the dielectric

$$T = \frac{f_2 V I_{SET}}{2\pi t_{ox} k} + T_{amb}. \tag{3}$$

The assumption of power dissipation taking place inside the dielectric layer is reasonable. It has been shown by Takagi et al. [30] for the case of gate-oxide BD in MOSFETs that electrons tunneling through defects responsible for stress-induced leakage current (SILC) in thin oxynitrides do

lose a large fraction of their energy in the oxide, which suggests an inelastic process. This behavior has been explained to be a consequence of defect relaxation [31] and was recently confirmed by Lombardo et al. [32] for ultra-thin MOS devices.

f_2 represents the fraction of energy qV lost by the carriers injected into the dielectric, which ranges from 0 to 1. While at a large applied voltage, f_2 tends to 1 in agreement with the electron's high energy loss, and for low voltages, f_2 decreases, tending to zero for $V = 0$. f_2 also depends on the temperature mainly because of phonon–electron scattering [32]. Therefore, f_2 is a function of voltage and temperature whose behavior is found by the best fit procedure. The influence of f_2 on the temperature is shown in Fig. 3(e) for different f_2 values.

Once T at the CF constriction is estimated, then the diffusivity D can be modeled by the exponential law given by (4), where D_0 is a pre-exponential term and E_{act} is the diffusion activation energy. It is worth noting that as shown by Lombardo et al. [32], substituting (4) and (3) into (1), an exponential dependence of TR on f_2 shows off. This may be helpful to explain the remarkable dispersion shown in Fig. 2(a) and (b). If, for example, f_2 has a 20% dispersion, then the TR may present a standard deviation of up to two orders of magnitude

$$D = D_0 e^{\frac{-E_{act}}{k_B T}}. \tag{4}$$

B. Effect of the t_{ox} Reduction After the Forming Step

To implement this model for the SET event, the thickness of the dielectric needs to be considered in detail. In a first step, the CF is created through the fresh insulating layer [HfO$_2$ in Fig. 3(a)] by a forming operation [a controlled dielectric BD, see Fig. 3(b)]. Then, the switching mechanism relies on the creation of a gap (RESET) and the restoration of the CF (SET). The width (t_{gap}) of such a gap is independent of the oxide layer thickness (t_{ox}) [see Fig. 3(c)] but dependent on the current compliance used during the SET event [11], [12], [15].

In a dielectric layer, BD is attributed to the formation of a percolative path between anode and cathode due to the generation of defects of size of ~1 nm [15], and it is statistically described using the Weibull distribution, an extreme-value distribution appropriate for a weakest-link problem, such as dielectric BD . Being the probability of forming such a path throughout the oxide bulk dependent of the oxide thickness [34], it is possible to use the statistics of the SET switching time (t_s) (i.e., the time to complete the HRS to LRS transition) under constant bias to estimate the effective thickness of the oxide layer after the forming event (t_{gap}). Fig. 4(a) shows the Weibull plots for t_s, where the slope (marked as β and constant throughout all the voltages considered) is ~1.2. This suggests a HfO$_2$ film of ~2 nm from its comparison with the literature [34], [35]. From the model viewpoint, this can be regarded in (1) as a reduction in the physical thickness t_{ox}, as shown in Fig. 3(a) and 3(c). From (3), it is clear that such t_{ox} reduction causes a significant increase in the temperature at the CF constriction, as shown in Fig. 4(b) by the dashed and solid lines for the case of $t_{ox} \approx 10$ nm (fresh device) and $t_{ox} \approx t_{gap} \approx 2$ nm. It is worth
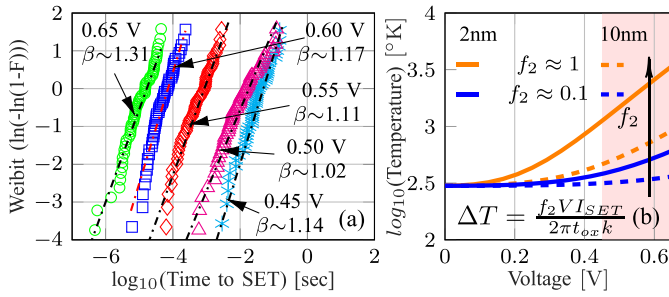
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Fig. 4. (a) t_s distributions for CVS experiments for ~100 transitions for each voltage. Symbols are experimental data. Dashed-dotted lines are Weibull fitting results. (b) Temperature in the CF constriction versus the stressing voltage, the resulting t_{ox}, and the energy loss; the red shaded zone indicates the stressing voltage range (0.45–0.65 V).

mentioning that the local reduction of the thickness caused by the creation of a metal-rich region in the oxide has been observed using cross-sectional high resolution transmission electron microscopy [17], [18], [36].

C. Increase in the Diffusivity of the Species Involved

In the model proposed by Palumbo *et al.* in [13], the creation and growth of the CF connecting anode and cathode (PBD) are due to the diffusion of the anode/cathode atomic species into the gate dielectric, creating a metallic filamentary path. This has been shown [13] by fitting the DR observed in both SiO_2- and high-k stacks with (1) and evaluating the required diffusivity D as a function of temperature with (4), as shown in Fig. 5 (see curves A, B, and C). Although quite large (of the order of 10^{-13} cm^2/s at 1000 °K, with low activation energies ranging from 0.7 to 0.3 eV), such values are in a range compatible with the diffusivity of metals in dielectrics for conditions similar to those adopted here (e.g., the case of Cu diffusion into SiO_2 layers [33]).

In the same way, the diffusivity required to fit the TR versus voltage data has been calculated with (1)–(4) assuming the same values for the fitting parameters [13] (E_{act} ranging from 0.3 to 0.7 eV, $f_2 \sim 0.1$, and $f_1 \sim 1$) and is also plotted against the temperature in Fig. 5 (curve D). The obtained value for D is quite larger ($\sim 10^{-6}$ cm^2/s at 1000 °K) than the fit diffusivities for the case of gate-oxide BD. It should be mentioned that even in an unlikely scenario in which 100% of the electron's energy is lost at the BD spot (i.e., $f_2 = 1$), the required diffusivity to fit the TR data is significantly higher than the diffusivity obtained from fitting the PBD of gate oxides (for clarity, such fitting results are not shown).

At this point, it is worth recalling that the transition from HRS to LRS has been explained as the vanishing of the gap in the filamentary path. During the forming operation, the CF is jointly created by the migration of the conductive species from the electrodes (blue balls) into the dielectric and the dissociation of oxygen ions (O^{2-}), which drift to the top electrode (TE) generating positively charged VOs (red balls) in the oxide layer and a reservoir of O^{2-} ions in the TE [see Fig. 3(a) and (b)] [12], [38]. Then, the RESET process opens a gap in the CF due to the recombination of the VOs in the CF with the O^{2-} ions, which diffuses back from the TE into the oxide [see Fig. 3(c)]. The sample is then in
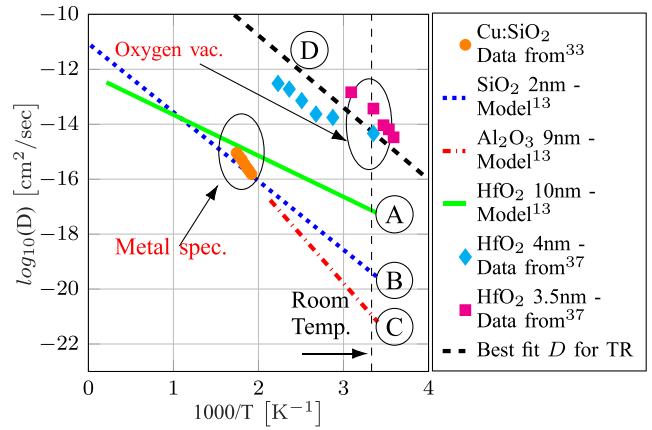

Fig. 5. Diffusivity of the dominant atomic species in the CF versus the reciprocal of temperature. VOs diffusivity [37] is $\sim 10^4$ times higher than for the metallic species [13]. E_{act} ranges from 0.3 to 0.7 eV. The diffusivity D required for fitting the TR results is shown to be in the same range as the VOs diffusivity.
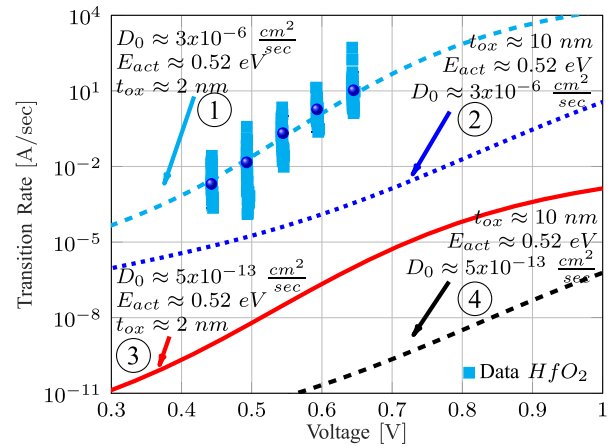

Fig. 6. TR data (square markers–ball markers stand for the mean value-) fit assuming VOs and $t_{gap} = t_{ox}$ (cyan dashed line—curve n°1). In addition, the TR assuming the values reported in the literature for t_{ox} and D is plotted—curves n° 2, 3, and 4. The TR increases almost one order of magnitude for every 50-mV step, with a mean value of 2×10^{-3}, 1.4×10^{-2}, 2.1×10^{-1}, 1.8×10^{0}, and 1×10^{1} A/sec for 450, 500, 550, 600, and 650 mV, respectively.

HRS, with a ruptured CF that consists mainly of the anodic atomic species (blue balls) that diffused during the forming. Under such a scheme, the SET event is explained as the completion of the gap due to the migration of O^{2-} ions toward the TE through a field-assisted and thermally activated effect, which creates the VOs that fill the gap within the CF [see Fig. 3(b)] [20], [38], [39]. This is quite a relevant point to notice, as the diffusivity of VOs, or equivalently the O^{2-} ions, in a HfO_2 layer of thickness similar to t_{gap} spreads over a range similar to the fit diffusivity for the TR [37] (see curve D in Fig. 5). Therefore, it might, altogether with the mentioned "reduction" of t_{ox}, explain the higher TR for these samples.

D. Fitting Results

The fitting results for the TR as a function of the applied voltage obtained with the proposed model in (1)–(4) are shown in Fig. 6 (see curve n°1). These results have been superimposed to the scatter plot of the experimental TR data (see the

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square symbols), showing good agreement with the mean value for each voltage (indicated by the ball markers). The proposed fit accounts for both the t_{ox} reduction (t_{ox} considered is equal to $t_{gap} \sim 2$ nm) and the increase in diffusivity (D_0 is in the order of $\sim 10^{-6}$ cm^2/s, as other species are considered to complete the CF, i.e., VOs). The rest of the parameters involved remain as previously mentioned ($E_{act} \sim 0.3$–0.7 eV, $f_2 \sim 0.1$, and $f_1 \sim 1$).

In order to make clear the impact of both the t_{ox} reduction and the diffusivity increase (D_0), alternative fitting values are used to plot curves n°2, n°3, and n°4. Curve n°2 shows the TR as a function of voltage assuming fixed t_{ox} to the nominal oxide thickness ($t_{ox} \sim 10$ nm) but an increase in the atomic species diffusivity ($D_0 \sim 10^{-6}$ cm^2/s). Curve n°3 presents the resulting curve when only the t_{ox} reduction is considered (i.e., $t_{ox} \sim t_{gap} \sim 2$ nm and D_0 corresponding to the metal diffusion in oxides $\sim 10^{-13}$ cm^2/s). Finally, curve n°4 presents the TR as a function of the applied voltage considering the same parameter values as in the gate-oxide BD transients, i.e., the diffusivity of metals in oxide layers ($D_0 \sim 10^{-13}$ cm^2/s) and no t_{ox} reduction ($t_{ox} \approx 10$ nm). This coincides with the DR for gate-oxide BD.

The comparison of curves n°1 and n°4 evidences that the TR is significantly higher than the DR expected for the voltage range considered. It is also worth noticing that the TR calculated considering only a t_{ox} reduction or an increase in diffusivity (D_0) cannot meet the experimental data (see curve n°1 versus curve n°3 and curve n°1 versus curve n°2, respectively). This suggests that the TR as a function of voltage is jointly determined by a combination of both effects, as none of them can fit the results independently.

V. Conclusion

In this paper, we showed that the HRS to LRS transition (SET) in HfO$_2$-based MIM stacks acting as resistive random access memories (RRAMs) is a progressive phenomenon whose voltage dependence can be modeled in a similar fashion to the PBD of thin oxides [13] by considering a proper adjustment of parameters. In this regard, the time required for the SET transition is studied as a function of the switching voltage considering CVS. As well as in the case of PBD, we propose that the HRS to LRS transition is due to the energy transfer from a CF to its surroundings, which promotes the electromigration of the fastest available atomic species, enlarging the CF. Although the magnitude and voltage acceleration of DR during PBD (forming process) and TR during the SET event are different, in the framework of the model proposed in this paper, such differences are explained as a consequence of an increase in the diffusivity and a reduction of the effective oxide thickness. Diffusivity increases, as the HRS to LRS transition (caused by the completion of the CF) is due to the migration of VOs, whose diffusion coefficient is higher than that from electrode's atoms that diffuse during PBD. Second, the reduction in the effective value of t_{ox} should be considered, as the SET event takes place in a previously degraded oxide layer, and this increases the speed of the transition. The model presented here accounts for such effects and is in agreement

with the previous results reported [18], [20], [38], which presented experimental evidence of both the t_{ox} reduction and the influence of the VOs.

Finally, it is worth mentioning that, by relating the TR with the temperature and thermal conductivity of the dielectric considered, the TR could be potentially sped up by increasing the temperature at the CF, whether by increasing the SET voltage or by using a material with lower thermal conductivity [40]. As the reduction in the supply voltage is common in current CMOS processes, the second option could eventually lead to shorter writing times for the RRAM devices, which have been proposed as future non-volatile memories.

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