Steep-slope Devices for Power Efficient Adiabatic Logic Circuits

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***Abstract*— Reducing supply voltage is an effective way to reduce power consumption, however, it greatly reduces CMOS circuits speed. This translates in limitations on how low the supply voltage can be reduced in many applications due to frequency constraints. In particular, in the context of low voltage adiabatic circuits, another well-known technique to save power, it is not possible to obtain satisfactory power-speed trade-offs. Tunnel field-effect transistors (TFETs) have been shown to outperforms CMOS at low supply voltage in static logic implementations, operation due to their steep subthreshold slope (*SS*), and have potential for combining low voltage and adiabatic. To the best of our knowledge, the adiabatic circuit topologies reported with TFETs do not take into account the problems associated with their inverse current due to their intrinsic p-i-n diode. In this paper, we propose a solution to this problem, demonstrating that the proposed modification allows to significantly improving the performance in terms of power/energy savings compared to the original ones, especially at medium and low frequencies. In addition, we have evaluated the relative advantages of the proposed TFET adiabatic circuits, both at gate and architecture levels, with respect to their static implementations, demonstrating that these are greater than for FinFET transistor designs.**

***Index Terms*—Adiabatic logic, Tunnel field-effect transistors, Steep subthreshold slope, Low power.**

I. Introduction

Very intensive research targeting the reduction of power and energy consumption of complementary metal-oxide-semiconductor (CMOS) electronics circuits and systems has been being conducted during the last decade. The need for ultra-low-power and energy-efficient circuits is due to different reasons. The impossibility of further increasing the system complexity because of power density problem of CMOS and the boom of portable devices working from batteries are the main ones [1]. More recently, the arising of IoT or implantable medical devices which eventually use energy harvesting has boosted the activity in the area [2],[3].

The reduction of power and energy has been addressed from different domains, including both software and hardware approximations. Concerning the latter, methodologies and techniques at distinct abstraction levels are possible. At the circuit level, it is well known that reducing the supply voltage is a very powerful way of reducing power. In fact, supply voltage reduction enabled by the scaling of CMOS technologies has significantly reduced power consumption in the past. However, the further scaling of supply voltages to reduce dynamic power while maintaining adequate speed is counterbalanced by the exponential growth of leakage currents. Keeping speed with lower voltage supply requires lowering the threshold voltage of the transistors, which, because of the 60 mV/decade minimum subthreshold slope (*SS*) of CMOS devices, produces unacceptable off-state leakage currents. This has motivated intensive research into devices with *SS* below the physical limit of CMOS, known as steep slope devices, to achieve better transistor performance at reduced supply voltages [4].

Among them, Tunnel field-effect transistors (TFETs) have been extensively explored [5]-[11]. Several works have shown power benefits for iso-performance or higher performance at iso-power up to moderate operating frequencies [12]-[17]. This is because current TFETs do not reach the high on current values exhibited by CMOS transistors at their nominal supply voltage. Difficulties encountered to simultaneously achieve high I_{ON} current and reduced I_{OFF} current in TFETs are being investigated to be solved using different approaches [16]-[22].

A completely different approach for low power circuits is quasi-adiabatic logic. Adiabatic circuits are operated such that power dissipation in transistor´s resistance is almost eliminated and energy stored in circuit capacitances is recovered. The former requires very slow charging and discharging of capacitances and so the speed of adiabatic gates is significantly smaller than in conventional complementary logic gates. However, in order to take advantage of adiabatic operation, power must be dominated by its dynamic component. In other words, power savings are not obtained for very low frequencies. Because of this, the amount by which the supply voltage can be reduced in adiabatic logic is more limited than in their conventional counterparts. In fact, there are very few works on low voltage adiabatic CMOS circuits. In [23] it is shown that they cannot achieve a satisfactory trade-off between energy and operating frequency.

The better performance of TFETs for low voltage suggests it is interesting exploring TFET adiabatic circuits. We believe that combining the adiabatic operating principle and TFETs can lead to ultra-low-power and energy-efficient circuits. Up to our knowledge, just a few papers have addressed this issue. In this paper, we present a comprehensive study that not only investigates suitable circuit topologies for TFETs quasi-adiabatic logic gates and provides design guidelines for them but also evaluates power and energy savings achieved. It will also be shown that the use of adiabatic gates in complex circuits provides significant advantages in terms of power consumption compared to conventional static implementations as they do not need to increase the supply voltage to operate at high frequencies.

The rest of the paper is structured as follows. Section II introduces background for this work on both the adiabatic logic style and the TFET devices characteristics. Section III describes the implementation of a widely used adiabatic gate topology with TFETs and proposes novel circuit topologies that solve drawbacks of other previously reported. In Section IV simulation results are discussed at gate level. The design and

evaluation of a complex circuit are presented as a case study in Section V. Finally, some conclusions are given in Section VI.

II. Background

A. Adiabatic logic

Adiabatic logic has been used as a technique to design circuits with low power consumption by reducing the exchange of energy between the circuit and the environment. In real circuits, due to the presence of power dissipating elements, such as resistors, this exchange cannot be reduced to zero, although it can be minimized by using ramped power supplies through which energy is stored and recovered from the output node of the circuits. That is, unlike CMOS design styles, in adiabatic logic transitions between 0 and V_{DD} do not occur abruptly.

To illustrate the operation of an adiabatic gate, we consider the Positive Feedback Adiabatic Logic (PFAL) [24] buffer in Fig 1a. This topology has been selected since it exhibits the best performance in terms of energy compared to other families of adiabatic circuits [24]. It consists of an adiabatic amplifier, that is, a latch composed of the pair of transistors P_A-N_{A2} and P_B-N_{B2}. Logic functionality is implemented by transistors N_{A1} and N_{B1}. Other logic functionalities can be obtained by replacing these transistors by the corresponding network and its complement. Note that both the positive and negative outputs are obtained. A ramped power supply (φ_i) is applied, with the same rising, falling, hold and reset times (see Fig 1b). The cascade connection of this type of gates requires a successive offset of 90º in φ_i for each of the interconnected levels (φ_{i+1} in dashed line in Fig 1b).

When φ_i switches from 0 to V_{DD}, the output is evaluated according to the inputs (IN and its complement $\overline{IN}$), which are stabilized previously, as shown in Fig 1b. Note that in the first pulse of φ_i IN is at a high logic level, driving current through transistor N_{A1} to charge the output capacitance C_{LA} (I_φ>0 in Fig 1b). The node $\overline{OUT}$ remains at a low level because, on the one hand, $\overline{IN}$ is low, cutting the N_{B1} transistor and, on the other hand, OUT is rising together with the power supply, making the V_{GS} seen by transistor P_{B2} transistor practically 0 and, hence, cutting the transistor. For the second cycle of φ, where the inputs have different values (IN='0', $\overline{IN}$='1'), the scenario is the opposite. When φ_i is high the outputs keep their value in order to be evaluated by the next stage with φ_{i+1}. Note that in this scenario I_φ=0. Transistors P_{A1} (P_{B1}) and N_{B2} (N_{A2}) take care of storing the information when OUT='1'/$\overline{OUT}$='0' (OUT='0'/$\overline{OUT}$='1'). Finally, φ_i descends from V_{DD} to 0. As long as its value remains above the threshold voltage of the P transistor ($V_{TH,P}$), the output will discharge overlapped with φ_i, restoring the energy stored in the output capacitance (I_φ<0 in Fig 1). When that value is reached, the P transistor is cut off and with it, the remaining energy in the capacitor is dissipated or reused in the next cycle depending on the value of the inputs.

The total energy dissipated is the sum of three terms: active losses (E_{ADL}), those associated with the remaining voltage at the output (E_{VT}) and those of leakage (E_{LEAK}). In static designs, there is an energy component that decreases with frequency, that of leakage, while the dynamic part (see (1)) is independent of frequency. However, this dynamic energy increases when the switching activity does. In adiabatic circuits, the leakage energy also decreases with frequency and there is remnant energy that

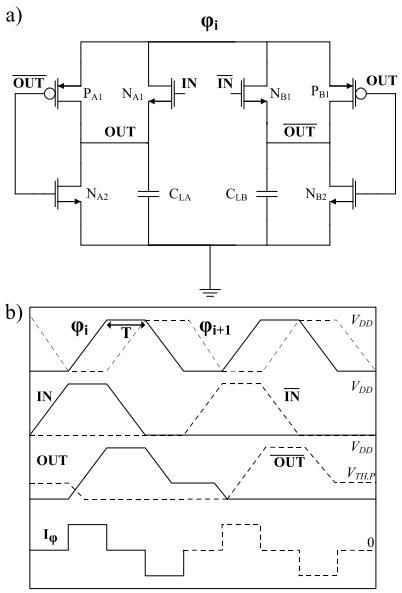

Fig 1. (a) Schematic of a PFAL buffer (b) Waveforms illustrating its operation.

does not vary with frequency, but adiabatic energy losses (dynamic component) do increase with frequency. On one hand, for low frequencies, where the leakage is dominant, there is no reason to expect advantages of adiabatic circuits. On the other hand, for very high frequencies, where the dynamic component dominates, static circuits would be more efficient than adiabatic ones. Thus, it is in an intermediate frequency range that the adiabatic design style can present advantages in terms of efficiency, given that, in those scenarios, its dynamic energy component is below that of the static designs

B. Tunnel field-effect transistors

TFETs are one of the most attractive steep *SS* devices [1]- [7]. Subthreshold swing under 60mV/dec has been experimentally obtained in different material systems [25], [26]. TFETs exhibit several distinguishing characteristics with respect to MOSFETs, including super-linear onset, ambipolarity, enhanced Miller capacitance effect due to the dominance of gate to drain capacitance or asymmetric conduction which are being addressed [27]-[30]. Let us focus on the asymmetric conduction which is relevant for this work. Fig 2 depicts output I-V curves for an N-type TFET device. Differences are evident compared with a MOSFET transistor. TFET behavior is very much unlike for positive and negatives drain to source voltages. It is usual to define the TFET as a unidirectional device, although this is not completely true as it can be observed in the figure. The asymmetric conduction can be more precisely defined as:

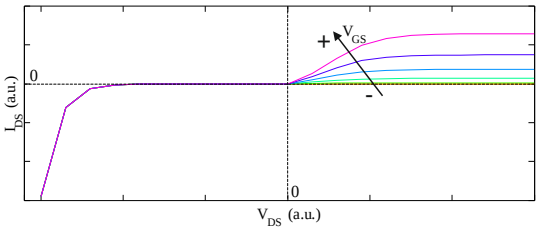

Fig 2. *I-V* characteristic of an *N*-type TFET.

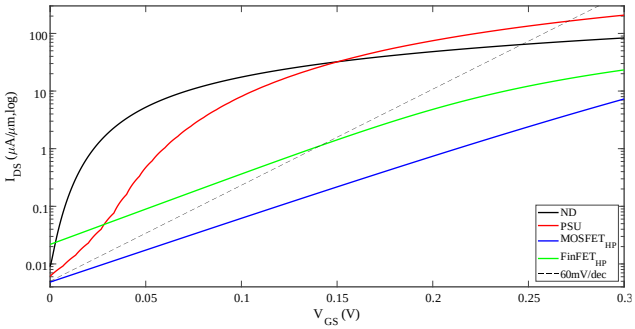

Fig 3. I_{DS}-V_{GS} characteristics of simulated transistors for V_{DS}=0.3V.

- Low conduction of the *n*-type (*p*-type) TFET transistors with a moderate negative (positive) drain to source voltage.
- Large current of the *n*-type (*p*-type) TFET transistors for high enough negative (positive) V_{DS}, due to the forward biasing of the intrinsic *p-i-n* diode.

Additionally, this behavior is almost independent of V_{GS}. It occurs both for positive and negative values and for V_{GS} = 0. The design of circuits using TFETs requires considering, among other non-ideal effects, the impact of p-i-n leakage current. [31]-[33]. As in conventional CMOS technologies, a given TFET device is not competitive for all possible applications. For example, in terms of power, depending on the required operating frequency, different TFETs are more suitable. In this work two predictive TFET models have been used. The first are 20nm AlGaSbInAs heterojunction transistors, which have been developed by Notre Dame University (ND) [33], exhibits ultra-low off current but limitations in terms of speed. The second are 20nm GaSb-InAs heterojunction transistors, which have derived by Pennsylvania State University (PSU) [35], and are advantageous when the operating frequency is the primary concern.

Fig 3 shows drain-source current (I_{DS}) versus gate-source voltage, V_{GS}, (with V_{DS}=0.3V) for both TFETs and the HP MOSFET and FinFET transistors. Currents have been normalized with respect to the transistor width and have been calculated using minimum length transistors. Clearly, TFETs exhibit larger currents at reduced supply voltage.

III. Implementation of Adiabatic Circuits Using TFETs

This section deals with the design of PFAL adiabatic circuits with TFETs, highlighting the problems that arise when using these devices and proposing a modification of this topology that solves them.

The main difference between the implementation of PFAL circuits in CMOS and tunnel technologies lies in the fact that, given the asymmetrical conduction of TFETs, it is necessary to enable a return path for charge recovery, different from that of injection [38]. Fig 4 shows the modified PFAL TFET-based topology, in which flipped P transistors P_{A2} and P_{B2} have been added in each branch for that purpose [38].

A. Reverse conduction currents in TFET-based PFAL circuits

Fig 5 illustrates the operation of branch A of the PFAL buffer in Fig 4 designed with ND transistors, operating at a frequency of 1MHz and with a high voltage level of 0.3V. The figure

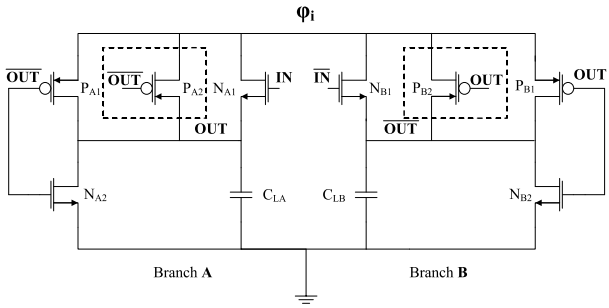

Fig 4. Schematic of a TFET-based PFAL buffer [38].

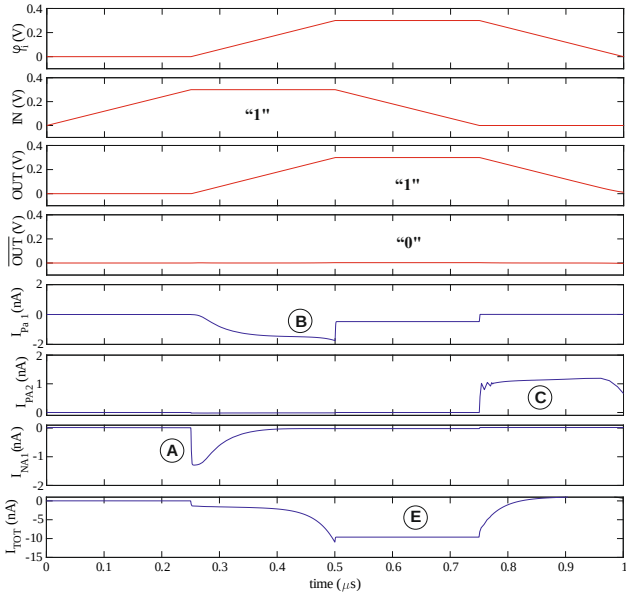

Fig 5. Descriptive waveforms of the PFAL buffer operation for IN='1'.

shows the power supply, the input, the outputs, as well as the currents flowing through transistors P_{A1}, P_{A2}, N_{A1} and the total current (I_{TOT}) supplied by φ_i. To ease the interpretation of the figures, voltages are depicted in red and currents in blue. Note that for these simulations negative currents are drained from the power source whereas positive are recovered.

In Fig 5, the input is at a high level at the rising edge of φ_i, so transistors P_{A1} and N_{A1} drive current to the load capacitance C_{LA} Note that N_{A1} transistor starts to drive before P_{A1} because, at the beginning of the rising edge of φ_i, OUT=0 and its V_{GS} voltage is maximum (mark "A" in Fig 5). As OUT rises, the V_{GS} voltage of N_{A1} begins to decrease, while that of P_{A1} (V_{GS}= $\overline{OUT}$- φ_i) becomes larger and, thus, this transistor is the one that provides most of the current to charge C_{LA} in the final part of the rising edge of φ_i (mark "B" in Fig 5).

As expected, once the output is stabilized at a high level, the current circulating through branch A (I_{PA1}+I_{PA2}+I_{NA1}) becomes practically zero. When φ_i starts to fall and triggers the discharge of OUT, the current is recovered mainly through P_{A2} transistor (mark "C" in Fig 5).

However, reverse conduction currents from a certain negative V_{DS} value (shown in Fig 2), cause the appearance of a conduction path between φ_i and ground through P_{A2} and N_{A2} transistors which spoils the adiabatic operation of the circuit.

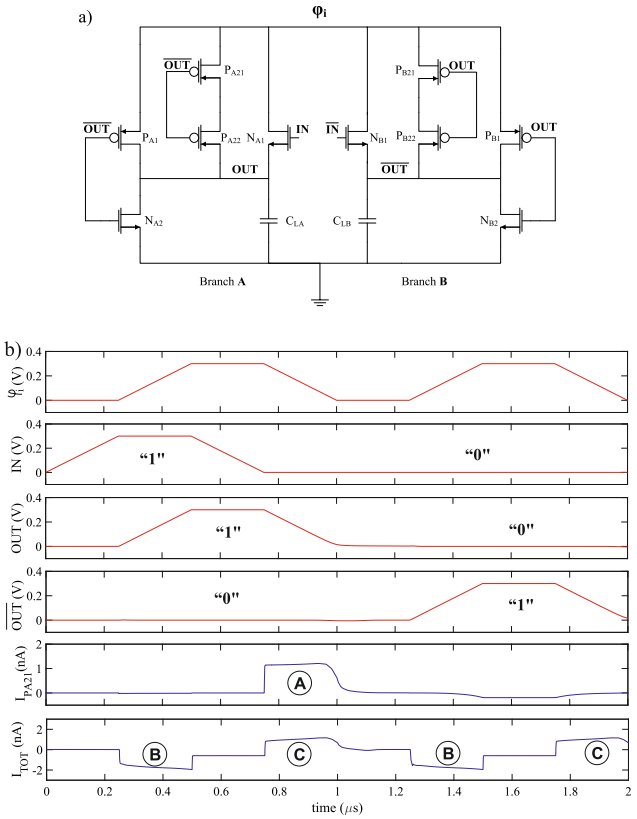

Fig 6.(a) Schematic of the proposed PFAL buffer topology to avoid reverse currents. (b) Waveforms showing the correct operation of the modified topology.

B. Proposed PFAL topology

The origin of the reverse currents appearing on P_{A2} (and P_{B2}) transistor is an excessive negative V_{DS} voltage when the output OUT ($\overline{OUT}$) is at zero and the power supply is high. To avoid these currents, we propose a modification of the PFAL topology in which this transistor is replaced by two identical ones connected in series. Fig 6a shows this modification, in which P_{A2} transistor (and P_{B2} in the other branch) has been replaced by the series connection of transistors P_{A21} and P_{A22}. In this way, the total V_{DS} voltage is distributed among each of the new transistors, so that the reverse current remains within the zone of practically zero currents, avoiding the incorrect operation described above. The proposed solution implies increasing the number of transistors from 8 to 10 (25% of area penalty).

Fig 6b shows waveforms of the operation of the proposed topology. In this case, the evaluation of consecutive logical zero and one in the input is shown. Note that now the current through the two new transistors in series (I_{PA21} in Fig 6b) exhibits the expected behavior, recovering charge from C_{LA} on the falling edge of the supply voltage when the output is high (mark "A"). It is now evident that the total current of the power supply (I_{TOT}) exhibits an expected behavior, with one part being consumed during charging the output capacitance (I_{TOT}<0, marks "B") and another part being recovered during the discharge (I_{TOT}>0, marks "C").

IV. Evaluation of the Performance of TFET-based Adiabatic Gates

This section compares power consumption and frequency trade-offs for simple logic gates implemented with adiabatic logic and conventional static logic. Specifically, for adiabatic design, the buffer/inverter described above will be used (Fig 6a), while for static logic an inverter is selected. In these experiments, we consider voltage levels between 0V and 0.3V and a load capacitance at the output of 1fF. This study includes different models of TFETs (ND and PSU described in section II.B), as well as FinFET HP transistors. FinFET HP has been selected at the conventional reference transistor since it achieves the best results among the conventional studied ones, as expected from the data in Table I. Minimum-size transistors for each technology have been considered.

Fig 7a depicts the results obtained for power consumption versus frequency assuming a train of pulses at the input of the adiabatic buffer. The figure shows that the designs based on the proposed topology (ND_{PROP} and PSU_{PROP}) exhibit power performance around 40 times lower for the lower frequencies (up to 100KHz) than the conventional ones (ND and PSU), due to the elimination of the current flowing through the flipped recovery P transistor. Note that, at low frequencies, the modified design with PSU transistors consumes less power than the original with ND TFETs. This evidences that the proposed topology is necessary to exploit the advantages of ND transistors at low frequencies. However, increasing the frequency will reduce the differences between the results of the original and proposed designs, since current levels of the flipped transistors will be negligible compared to those associated to the charging and discharging of the output capacitance. In addition, the frequency from which PSU transistor design becomes more efficient than ND transistors is reduced from 50MHz to 5MHz.

On the other hand, as shown in Fig 7b, the proposed solutions also offer better performance in terms of energy per operation compared to FinFET HP. Specifically, the proposed design with ND transistors is more efficient up to 30MHz, while the one using PSU transistors exhibits less energy across the entire explored frequency range.

Finally, a comparison has been carried out between the power consumption of adiabatic and conventional static design styles. The results are shown in Fig 7c, which represents the ratio between adiabatic and static circuit consumption (i.e. a ratio less than 1 implies advantages of adiabatic versus static). On the one hand, the advantages of the ND tunnel design are given for low/medium frequencies (between 0.3MHz and 15MHz), exhibiting maximum savings of around 70% at 2MHz. On the other hand, advantages for the PSU tunnel designs are obtained from 0.2MHz, achieving power savings of more than 50% from 5MHz to 100MHz, with a maximum of around 75% at 40MHz. Finally, it should be noted that quite smaller savings are obtained with adiabatic FinFETs (from 10MHz to 100MHz with a maximum around 20% at 50MHz). These results suggest the potential of TFETs for the design of efficient low-voltage adiabatic circuits.

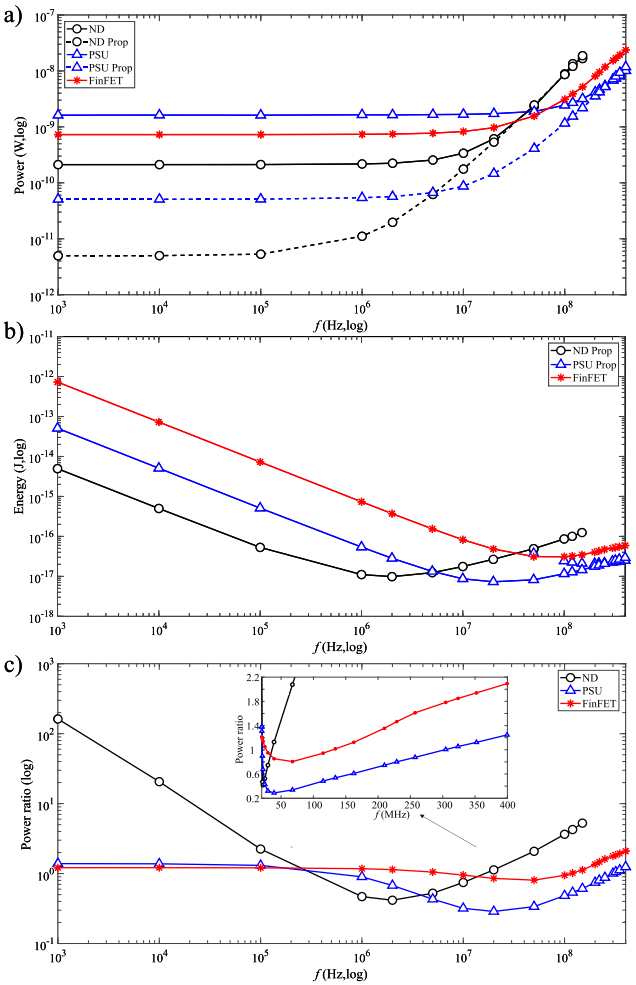

Fig 7. Evaluation of the performance of the original and proposed implementations of the TFET-based adiabatic buffer. Results for a FinFET HP have been also included. (a) Power versus frequency. (b) Energy per operation versus frequency. (c) Power ratio (with respect to static inverters implemented in the same technologies) versus frequency.

V. Case Study: Kogge-Stone Adders

The power consumption results shown in the previous section considering a pulse train at the gate input, although they provide a starting point for our study, do not correspond to a realistic scenario in which the circuit nodes switch at different frequencies depending on the combination of inputs applied. Thus, as a case study we have evaluated and compared a more complex circuit, an 8-bit Kogge-Stone (KS) adder [40] for both the static and the proposed adiabatic implementations using PSU transistors. Fig 8a shows power consumption of the evaluated adders with V_{DD}=0.3V considering random sequences at the inputs of the adder (in black). Additionally, to assess if the adiabatic design is more efficient than the static one, power ratio is depicted (red). A ratio less than one means that the adiabatic design consumes less power than the static one. Note that adiabatic implementation is more efficient than static for the entire explored frequency range. The power ratio shows some correspondence with the one obtained at gate level (Fig 7c) in that it presents a minimum around 20MHz, although it is observed that for higher frequency values the adiabatic buffer consumption is higher than that of the static inverter. This is due to the fact that the static implementation of the adder uses more than half as many gates as the adiabatic one. Furthermore, unlike adiabatic circuits, the implementation of complex static gates implies the use of additional P-type transistors, thus increasing capacitances (and power consumption).

One of the main advantages of adiabatic designs over static designs is that there is no need to increase the supply voltage when the logic depth of the circuit increases, which allows significant power savings. This is due to the natural operation of adiabatic logic in a gate-level pipelined fashion. In this sense we have evaluated the connection of three KS adders in series. Fig 8b shows power consumption and power ratio for this architecture. For lower frequencies the behavior is similar to that of isolated adders since the adder network operates with V_{DD}=0.3V. However, around 800MHz it is observed that the static designs need to increase their supply voltage to 0.4V, so the advantages of adiabatic designs against static ones become even more evident.

VI. Conclusions

The potential of TFETs for low-voltage adiabatic circuits has been explored. A modification of a previously reported TFET adiabatic topology has been proposed. It eliminates a phenomenon associated with the current of the intrinsic p-i-n diode of this type of transistors which limits its performance. Our results show that the proposed topology improves power savings, especially for low operating frequencies. Experiments with two TFETs predictive technologies show significantly larger power savings of TFETs adiabatic gates with respect to conventional MOS technologies ones. The steep slope characteristics of these transistors can be exploited to reduce leakage power without degrading too much current at low voltage and so enabling power savings of adiabatic operation, as it is the case of the ND transistor. Also, it can be exploited to increase the on current at low voltages so that adiabatic losses

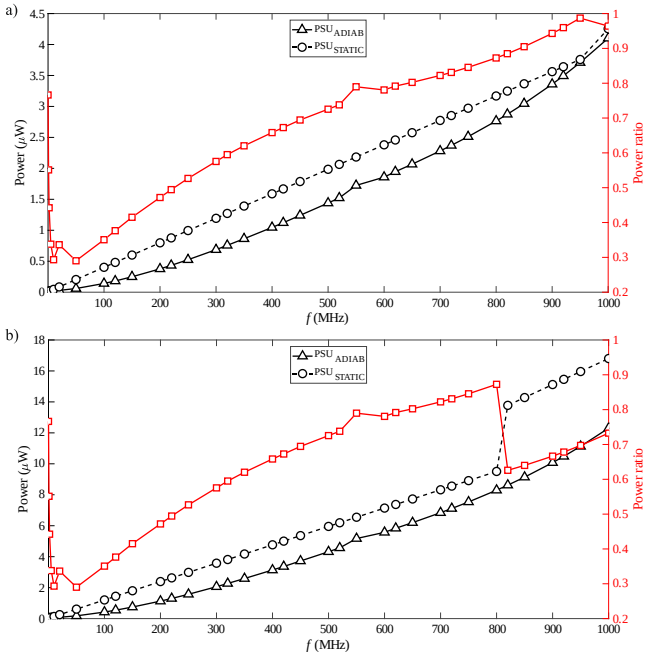

Fig 8. Power versus frequency (black) and power ratio (red) for (a) single 8-bits Kogge-Stone adder and (b) interconnection of three Kogge-Stone adders.

are reduced which translates in larger power savings even at larger frequencies, as it is the case of the PSU transistor. We have also shown, through the design of a KS adder and a network of KS adders, that the implementation of complex circuits using adiabatic gates can take advantage of the fact that operating frequency at a given supply voltage is independent of logic depth, contrary to static designs.

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