# MODELING OF GALLIUM NITRIDE TRANSISTORS FOR HIGH POWER AND HIGH TEMPERATURE APPLICATIONS

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Doctor of Philosophy

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The undersigned, appointed by the dean of the Graduate School, have examined the dissertation entitled

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presented by Samira Shamsir, a candidate for the degree of Doctor of Philosophy,

and hereby certify that, in their opinion, it is worthy of acceptance.

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This dissertation is dedicated to my parents,

Md. Shamsir and Hosne Ara

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# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# ABSTRACT

Wide bandgap (WBG) semiconductors such as GaN and SiC are emerging as promising alternatives to Si for new generation of high efficiency power devices. GaN has attracted a lot of attention recently because of its superior material properties leading to potential realization of power transistors for high power, high frequency, and high temperature applications. In order to utilize the full potential of GaN-based power transistors, proper device modeling is essential to verify its operation and improve the design efficiency. In this view, this research work presents modeling and characterization of GaN transistors for high power and high temperature applications.

The objective of this research work includes three key areas of GaN device modeling such as physics-based analytical modeling, device simulation with numerical simulator and electrothermal SPICE model for circuit simulation. The analytical model presented in this dissertation enables understanding of the fundamental physics of this newly emerged GaN device technology to improve the operation of existing device structures and to optimize the device configuration in the future. The numerical device simulation allows to verify the analytical model and study the impact of different device parameters. An empirical SPICE model for standard circuit simulator has been developed and presented in the dissertation which allows simulation of power electronic circuits employing GaN power devices. The empirical model provides a good approximation of the device behavior and creates a link between the physics-based analytical model and the actual device testing data. Furthermore, it includes an electrothermal model which can predict the device behavior at elevated temperatures as required for high temperature applications.

# Chapter 1

# Introduction

## 1.1. Motivation

During the past few years, research efforts in power semiconductor devices have been focused on the search for new materials as the successor of Si as it approaches its theoretical bound to keep pace with the growing technological needs. Wide bandgap (WBG) semiconductors are emerging as promising technologies for new generation of high frequency and high efficiency power devices. In fact, the material properties of WBG semiconductors yield devices with lower on-resistance and switching losses compared to Si devices with comparable voltage and current capabilities. Among the potential WBG materials for device applications, GaN and SiC are emerging as the leading contenders. Extensive research works on GaN device technology during the past decade have resulted in the realization of power devices with superior on-resistance, higher breakdown voltage and smaller footprints compared to the conventional power devices realized in Si.

As GaN power devices are intended to be used in high power application, a rigorous investigation of the device physics will provide insight into the behavior of the device in electronic circuits for the targeted applications. A proper modeling is also very important to simulate the device in a circuit simulator in order to verify its operation and improve the design efficiency for particular power electronic application. Although there have been several works on various types of GaN transistors and circuit topologies for power electronic applications reported in literature, modeling and device characterization efforts are relatively inadequate. In view of these issues, this research effort outlines some aspects of modeling

and characterization of GaN transistors for power electronic applications. The outcome of this work will serve as the foundation for GaN-based power electronic devices and circuits for high power and high temperature applications.

## 1.2. Research Objectives

The main objectives of this research are as follows-

***i) Development of a Physics-Based Analytical Model***

As GaN transistor technology is very new, it is important to study the underlining physical properties of the material and the device structures. Thus, one of the research tasks involves analysis of the device physics and representation of the device operation with analytical expressions with appropriate assumptions to adopt the analytical model for circuit and system level applications.

***ii) Device Characterization***

Device characterization is one of the important steps in order to validate any device or circuit model. At present, there are only a few commercially available GaN power devices and this work employs characterization of some of these GaN power devices.

***iii) Numerical Device Simulation***

In many cases, actual device testing and characterization can be very complicated, time consuming and expensive. In addition, for many commercially available devices, the details of device geometry and many device parameters can be unknown. A numerical device simulator can help overcome this by providing a virtual environment where the device can

be simulated under various conditions. However, it is important to develop a benchmark for the newly developed GaN transistors validated with actual measurement data. In this work, a numerical device simulation platform for GaN transistors is developed that can be used as a template for various device geometries and parameters.

***iv) Electrothermal SPICE Model***

This task includes development of an electrothermal model of GaN HEMT in order to predict the device performance at high temperature due to high power dissipation. To find the temperature limit of a designed system, this model can be used to achieve a quick solution to predict the device performances for the power dissipation for a specific application and thus can optimize the design.

Figure 1.1 summarizes the main research tasks that have been performed in this research effort.

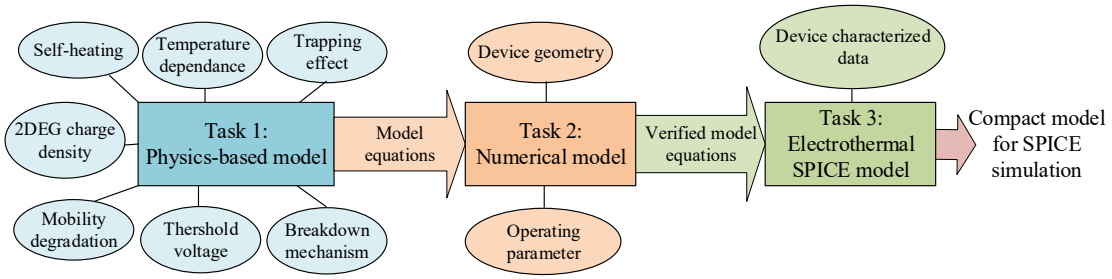



Figure 1.1: Summary of the research tasks.

## 1.3. Dissertation Overview

This dissertation is divided into seven chapters. Chapters 2 presents a literature review of GaN as a wide bandgap semiconductor demonstrating its capability to overcome the present

limitations of Si-based power electronics. In addition, it describes the main types of GaN power device configurations developed for high power applications. Chapter 3 includes different types of device models including GaN device models reported in the literature. It also includes the key properties of GaN-based transistor which need to be considered to develop a proper device model. Chapter 4 presents an analytical model developed for GaN Gate-Injection-Transistor (GIT) and compares the model with measured data. Chapter 5 describes the development of TCAD simulation for the device that allows study of the device performance for various device parameters. Chapter 6 introduces an approach to develop an electrothermal model for the GaN transistors that can be included in a SPICE simulator to simulate the device operation for a specific power electronic module. Chapter 7 summarizes the dissertation and presents future research directions.

# Chapter 2

# Wide Bandgap Power Semiconductor Device

## 2.1. Challenges of Silicon Semiconductor Technology

Power semiconductor devices are the key components of all power electronic systems that enable conversion of electrical power from one form to another (AC or DC) and control the magnitude of currents and voltages. The function of power processing or conversion includes rectification (AC to DC), inversion (DC to AC), bucking or boosting (DC to DC) and frequency conversion (AC to AC). A typical power conversion system (PCS) also includes other essential hardware such as control systems, semiconductor switches, passive components, thermal management systems, protection devices and enclosures. Power semiconductor devices are the modern replacement for electromechanical devices and all electric power generated today requires power electronic modules in several points between generation and consumption. Figure 2.1 shows different fields of operation of power devices with the required voltage and current ratings [1].

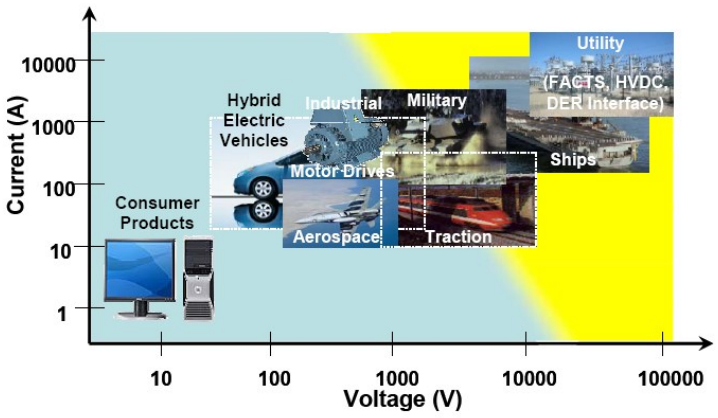



Figure 2.1: Applications for power semiconductor devices [1].

At present, the power electronic device technologies are still dominated by Si because of the continuous breakthrough of Si-based device physics and processing technologies. The invention of bipolar junction transistor (BJT) and gate turn-off thyristor (GTO) initiated the early stage of power electronics and the evolution reached the second stage with the invention of power metal-oxide-semiconductor field-effect transistors (MOSFET) [2]. Subsequent modification of transistor design such as double-diffused MOS (DMOS) process and trench gate technologies are adopted to have better performance. Insulated gate bipolar transistor (IGBT) is an emerging technology that combines MOS device physics with bipolar transistor technology. Although Si-based power devices are the most matured and widely used in power electronics, there are several factors which limit the use of Si and demand for the search for new alternative materials [3], [4].

### 2.1.1. Voltage Blocking Capability

The relatively narrow bandgap of Si (1.1 eV) leads to a low intrinsic critical electric field and low voltage blocking capability. For high voltage applications, stacking of packaged devices are used which increases the cost and complexity of the system. Thus, the devices with greater voltage blocking capability are required for smaller device packages. In addition, the active layers of the Si power devices are made very thick to achieve a high blocking voltage which results in high on-state resistance with a large amount of power loss [5].

### 2.1.2. Thermal Conductivity

The normal operating temperature of Si is less than $150^0$ C primarily due to low thermal conductivity of the material [6]. To maintain the junction temperature of Si devices below

this limit, several thermal management options for cooling are used such as natural air, forced air or water-cooled heat sinks, etc. A thermal management module typically occupies one third of the total volume of the overall system [6], [7].

### 2.1.3. Temperature Limits

Despite having low thermal conductivity, the operation of Si-based devices is degraded at elevated temperatures due to high intrinsic carrier concentration resulting from the narrow bandgap energy, which further increases with higher operating temperature. Beyond $150^0$ C, Si devices are undesirably dominated by intrinsic carriers rather than the dopant concentrations causing failure in device operation. The increase in the intrinsic carrier concentrations at high temperature also increases the reverse-bias junction leakage current and a low $I_{ON}/I_{OFF}$ ratio which is unacceptable for high power applications [8], [9].

### 2.1.4. Switching Frequency

The heat generated from the switching losses of the device further limits the operation of Si-based devices in high frequency switching applications. Typically, the switching frequency is limited to less than 20 kHz for a few kilowatts of power level. High frequency operation of the converters is preferable as it reduces the filter requirement with less audible noise and provides an exact control with smaller passive elements for high performance.

## 2.2. Wide Bandgap Semiconductors for Power Devices

Due to the several limitations of Si-based power devices and increased demand for improved performance, new semiconductor materials are brought into light for next

generation power electronic devices. With superior electrical characteristics, wide bandgap (WBG) semiconductors such as SiC and GaN, have emerged as the front-runners for power electronic applications. As many of the limitations for Si-based devices are attributed to the narrow bandgap of the material, power devices based on wide bandgap materials result in improved performance with higher blocking voltage, reliability, and efficiency with reduced thermal limitations [10]-[13].

### 2.2.1. High Critical Electric Breakdown Field

The critical electric breakdown field directly depends on the bandgap energy of a semiconductor material and thus the WBG semiconductors have much higher value of critical electric field compared to Si which in turns enables the power device to sustain higher blocking voltage.

### 2.2.2. Maximum Operating Temperature

The intrinsic carrier concentration of a semiconductor material is dependent on its bandgap energy and for wide bandgap semiconductor this value is significantly lower. Thus, when the junction temperature of the device is increased, the intrinsic carrier concentration remains much lower than the doping concentration and the device can operate at a much higher temperature. For most WBG semiconductors, the ambient operating temperature can be maximized above $400^0$ C.

### 2.2.3. High Switching Speed

The switching speed of semiconductor devices is directly proportional to drift velocity of the carrier. Si has a lower value of saturated drift velocity compared to that of the wide bandgap semiconductors. Therefore, for a device based on WBG semiconductors, it is

expected to have a much higher switching speed due to this high saturated drift velocity. In addition, this type of device can have lower reverse recovery current and shorter recovery time.

Key material properties of Si are compared with those of WBG semiconductors: SiC and GaN in Table 2.1 [11]. The table contains two figure-of-merits often used to compare performance of a semiconductor for power electronic applications:

$$\text{Baliga's figure-of-merit,} BFM = \varepsilon \mu E_C^2 \tag{2.1}$$

$$\text{Johnson's figure-of-merit, } JFM = \frac{E_c v_s}{2\pi} \tag{2.2}$$

where $E_c$ is the critical electric field, $\mu$ is the mobility, $v_s$ is the saturation velocity, and $\varepsilon$ is the dielectric constant. These material properties need to have high values so that the device can sustain high blocking voltage and high current density. This implies that the higher figure-of-merit allows the semiconductor to be more suitable for high power electronic applications. For wide bandgap semiconductors such as SiC and GaN, both figure-of-merits have higher values than Si.

TABLE 2.1
COMPARISON OF WIDE BANDGAP MATERIALS WITH SI

| Material | Mobility, $\mu$ $cm^2/V\text{-}s$ | Saturation Velocity, $v_s$ cm/s | Dielectric Constant, $\varepsilon_r$ | Energy Bandgap, $E_g$ eV | BFM Ratio | JFM Ratio | Maximum Temperature, $T_{max}$ °C |
|---|---|---|---|---|---|---|---|
| Si | 1300 | $1\times10^7$ | 11.4 | 1.1 | 1.0 | 1.0 | 300 |
| SiC | 260 | $2\times10^7$ | 9.7 | 2.9 | 3.1 | 60 | 600 |
| GaN | 1500 | $2.2\times10^7$ | 9.5 | 3.4 | 24.6 | 80 | 700 |

Although it has been established beyond doubt that WBG semiconductors demonstrate superiority in terms of several device characteristics, there are still disputes regarding the most optimal choice of WBG semiconductor for power device applications. SiC, GaN and diamond are the three most widely considered WBG materials. Despite having superior intrinsic material properties, diamond significantly lags behind other two contenders in terms of material synthesis and processing and thus is saved for remote future choice. On the other hand, most of the intrinsic material properties of GaN and SiC are very similar except for a few in which one excels the other. Due to having better thermal conductivity than GaN, SiC has been chosen more frequently for high temperature applications [14], [15]. On the other hand, most of the GaN devices are employed in radio frequency (RF) applications due to high carrier mobility of GaN. However, in recent years, GaN-based devices have been attracting attention for the application in power electronics [16]. As shown in the Table 2.1, the bandgap for GaN is slightly higher than that of SiC. This may result in a significantly higher critical electric field and blocking voltage as well as lower on-resistance for GaN-based devices due to high order dependence of these parameters on the bandgap energy [11], [12]. High breakdown voltage further enables better trade-off in achieving low on-resistance, which can be even lower due to the availability of heterostructure (AlGaN/GaN) for GaN-based system. Moreover, the ongoing development of GaN-based devices for RF applications offers natural indication of high speed switching in power device operation due to the inherent high carrier drift velocity. Although the higher thermal conductivity of SiC is often argued to be an advantage for high temperature operation over GaN, some researches are now indicating that the advantage brought by the

high thermal conductivity of SiC is more than the offset by the theoretical junction temperature of the WBG. In addition, another thermal property called coefficient of thermal expansion has higher value for GaN than SiC [12], which makes it more promising in a well-matched packaging technology. However, it is not only the device physics but also the maturity and the cost consideration of material processing technology that play important role in determining near-future optimal choice. In this term, both materials are emerging and facing their individual challenges along with the continuous research efforts.

## 2.3. GaN Power Device

Due to the inherent formation of two-dimensional electron gas (2DEG) created by polarization of AlGaN/GaN heterojunction, most GaN-based transistors are lateral heterojunction field-effect transistors (HFET) or high electron mobility transistors (HEMT) which demonstrate the basic principle of operation of most GaN-based devices

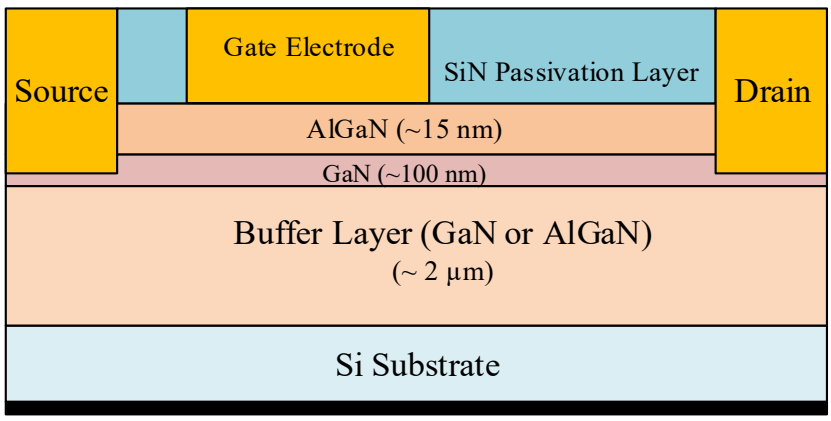



Figure 2.2: Basic structure of AlGaN/GaN HEMT or HFET [19].

[17], [18]. This 2DEG is formed by spontaneous polarization in GaN due to its crystal structure which is further augmented by piezoelectric polarization due to the lattice mismatch between AlGaN and GaN. The basic structure of a depletion-mode lateral GaN HFET is shown in Figure 2.2 [19]. The substrates are mainly SiC or sapphire and a buffer layer is deposited to provide strain relief due to the lattice mismatch with foreign substrate. A native channel between the source and the drain of the device is formed by the 2DEG. In most of the initial transistors based on AlGaN/GaN, a Schottky gate electrode is created by Ni/Au or Pt metal deposition on top of the AlGaN layer [11].

### 2.3.1. Two-Dimensional Electron Gas (2DEG) in AlGaN/GaN Heterojunction

The native channel present in GaN HEMTs is formed by the two-dimensional electron gas (2DEG) in the AlGaN/GaN heterojunction. When two semiconducting materials with different energy bandgap form an interface, electrons from the conduction band of the wider bandgap material try to flow to the conduction band of narrower bandgap energy. This creates a band bending near the interface and the electrons become confined to a potential well where they can move only in two dimensions [20]-[22]. Thus, these electrons are called two-dimensional electron gas (2DEG) and this confinement of the 2DEG increases its electron mobility from about 1000 $cm^2$/V-s in unstrained bulk GaN to 1500–2000 $cm^2$/V-s [22]. The high concentration of electrons with very high mobility is the basis for the high electron mobility transistor (HEMT).

Figure 2.3 shows the energy band diagram of two different types of heterojunction such as the AlGaAs/GaAs and AlGaN/GaN. The major difference between these two heterostructures is that for AlGaAs/GaAs structure, an *n*-doped AlGaAs layer is used to

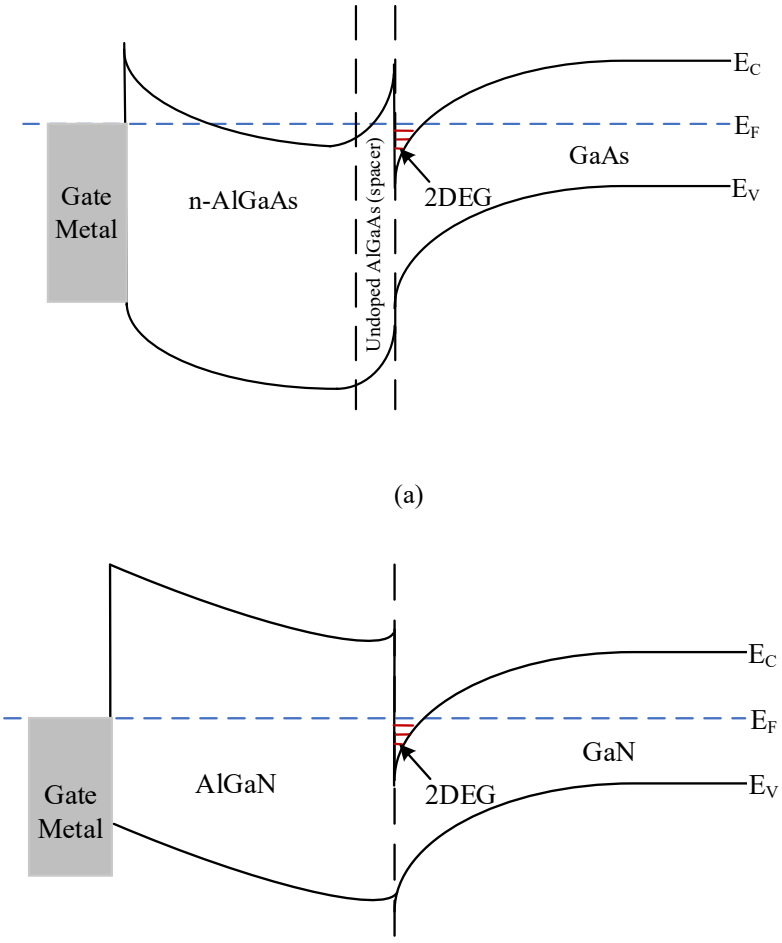
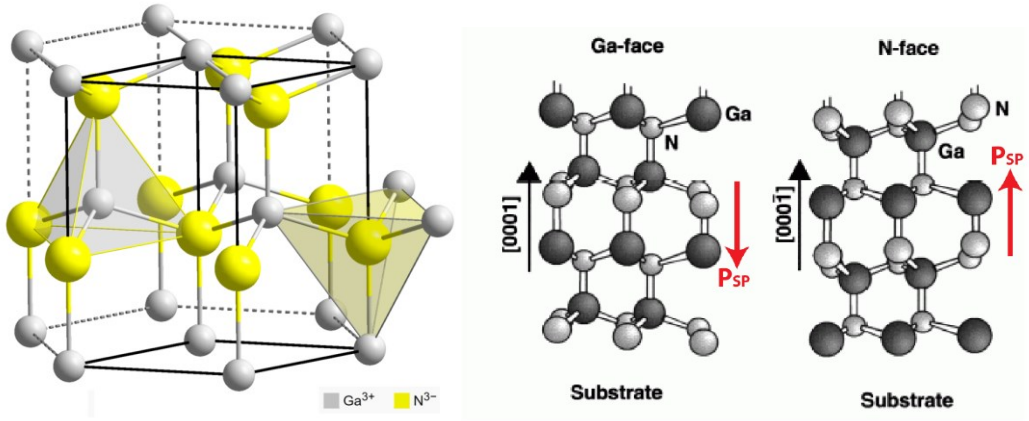



Figure 2.3: Equilibrium energy band diagram of two different heterojunctions: (a) AlGaAs/GaAs heterojunction and (b) AlGaN/GaN heterojunction.

supply the excess electron for the 2DEG. However, the electrostatic force due to Coulombic attraction between the ionized dopant atoms and electrons degrades the mobilty of the 2DEG. To minimize this effect, an undoped AlGaAs spacer layer is used in this heterostructure. Unlike the modulation-doped AlGaAs/GaAs heterostructures, no intentional doping is required to generate two-dimensional electron gas (2DEG) at the

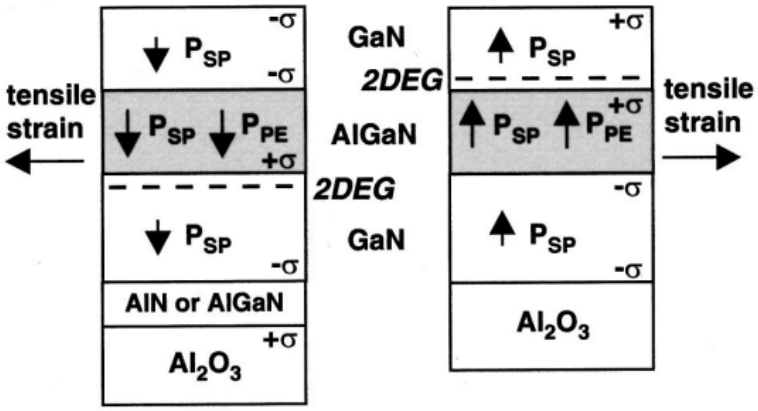
AlGaN/GaN interface. This 2DEG is formed as a result of spontaneous and piezoelectric polarization of AlGaN and GaN materials.

The natural structure of crystalline gallium nitride is a hexagonal structure named "wurtzite" as shown in Figure 2.4(a) [23]. In the crystal, Ga and N differ in electronegativity and therefore every Ga--N bond is partly ionic and has a certain dipole moment. For a completely symmetric arrangement of the bonds (as in the cubic variant 3C-GaN) these dipole moments cancel each other on a macroscopic scale. However, in wurtzite 2H-GaN, the bonds along the c-axis have a different length than the bonds nearly perpendicular to the c-axis, so the cancellation is incomplete resultinhg in a net dipole moment along the c-axis. Figure 2.4(b) shows the atomic planes consisting of successive stacking layers along the six-fold symmetry axis which includes only cations or anions [24]. As shown in this figure, there exists a non-overlap center of gravity of reticular cation




(a) (b)

Figure 2.4: (a) Wurtzite crystal structure of GaN. (b) Atomic arrangement of Ga-face and N-face in GaN crystal [23].




Lattice constants for $Al_mGa_{1-m}N$

$a_0\,(m) = (-0.077m+3.189)\times10^{-10}$ m,

$c_0\,(m) = (-0.203m+5.189)\times 10^{-10}$ m,

$m$: Al mole fraction

Figure 2.5: Polarization charges in an AlGaN/GaN structure [23].

and anion planes which creates an electric dipole along the c-direction of the crystal. This creation of the dipole inside the wurtzite crystal results in spontaneous polarization.

The formation of the 2DEG is enhanced by the piezoelectric polarization present in the AlGaN/GaN interface. This piezoelectric polarization is predominantly caused by the displacement of charged elements in the crystal lattice due to tensile strain. By growing a thin layer of AlGaN on top of a GaN crystal, a strain is created at the interface due to the lattice mismatch between these two materials. Lattice mismatch induces mechanical stress due to the elastic behavior of the materials (stress-strain coupling, described by the elastic stiffness constants). A thin film on a substrate usually experiences biaxial strain, since its in-plane lattice parameters are clamped and are equal to the substrate values (since this results in the smallest deformation energy, a much higher energy would be needed to

deform the thick substrate) and elastic relaxation can take place only perpendicular to the surface. Figure 2.5 illustrates the piezoelectric polarization and the formation of 2DEG in GaN/AlGaN/GaN heterostructures with Ga-face or N-face polarity [23].

Because of the confinement of the electrons in two-dimension, the 2DEG is very conductive with very high electron mobility. However, the main disadvantage of the HEMT structure is that the device is inherently normally-on or depletion-mode type due to the native 2DEG channel, which is unacceptable for many high power applications. In order to achieve a normally-off or enhancement-mode device, different types of mechanisms are incorporated by many researchers as discussed in the following sections.

### 2.3.2. Enhancement-Mode AlGaN/GaN HEMT for High Power Application

***i) Cascode Hybrid Enhancement-Mode Structure***

An enhancement-mode device can be made by cascoding a depletion-mode GaN HEMT with enhancement-mode Si MOSFET as shown in Figure 2.6 [25], [26]. In this configuration, the gate of the enhancement-mode Si MOSFET controls the turning on and

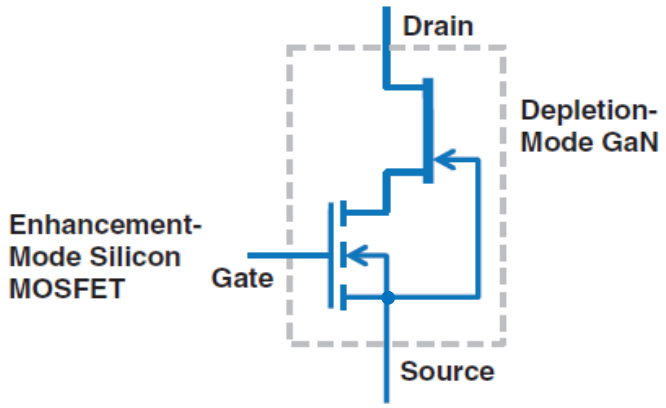



Figure 2.6: Cascode hybrid enhancement-mode structure [25].

off of the overall channel of the cascode device. However, in this configuration the on-resistance of the two devices are combined and thus it is not suitable for use in power electronic switching circuits. In addition, the packaging of the two die results in a significant increase in parasitic inductance [27].

***ii) Recessed-Gate Structure***

Recessed-gate structure is a very effective way to obtain a moderate value of threshold voltage for enhancement-mode operation of AlGaN/GaN HEMTs [28]-[31]. One such approach is presented by Saito *et al.* [28]. The device structure for this work is shown in Figure 2.7 which shows that the thickness of 2DEG density under the gate electrode has been selectively reduced to form a recessed-gate structure. The threshold voltage depends on the AlGaN thickness, $t_{RA}$ as shown in Figure 2.8(a) and an increase in the threshold voltage results with a decrease of $t_{RA}$. But the decrease in 2DEG density will further increase the on-resistance. Figure 2.8 (b) shows the dependence of the on-resistance with the threshold voltage [28].

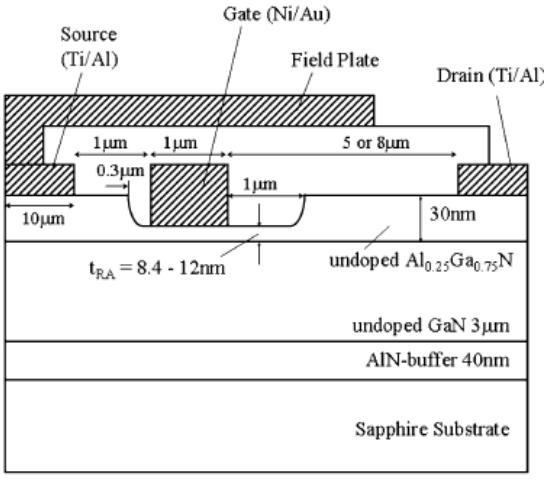



Figure 2.7: Recessed-gate structure of the AlGaN/GaN HEMT [28].

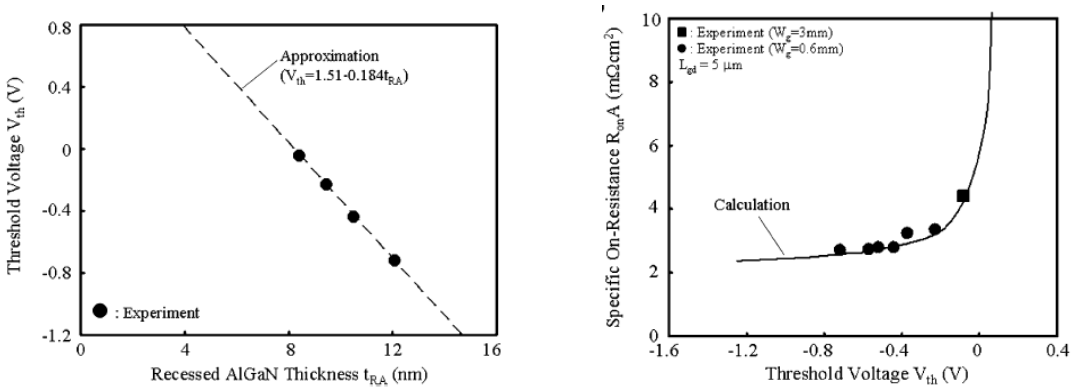



Figure 2.8: (a) Relationship between the gate threshold voltage and the AlGaN layer thickness. (b) Relationship between the specific on-resistance and the threshold voltage [28].

Another important feature of this device structure is the use of field plate to obtain a current-collapse-free operation. Current-collapse has been a widely reported phenomenon for GaN-based devices that results in a trade-off between the on-resistance and the breakdown voltage [31]-[34]. Because of the lateral structure, the gate-drain electric field is stronger at this edge causing the charges to be trapped temporally in the impurities due to surface passivation and interface states. While the device is turned on, these trapped charges weaken the 2DEG acting like a 'virtual gate' until they are released thereby increasing the on-resistance. Another mechanism for current collapse is the 'hot electron' injection in the deeper traps from carbon doping in the buffer layer. This also weakens the 2DEG and effectively increases the on-resistance. Both of the mechanisms are proportional to the blocking voltage which causes a high on-resistance. The trade-off between the breakdown voltage and the on-resistance is improved by design optimizations by using field plates. By inserting the source-gate field plate, the electric field at the gate-drain edge is redistributed. The substrate can act as a bottom field plate by connecting with the source.

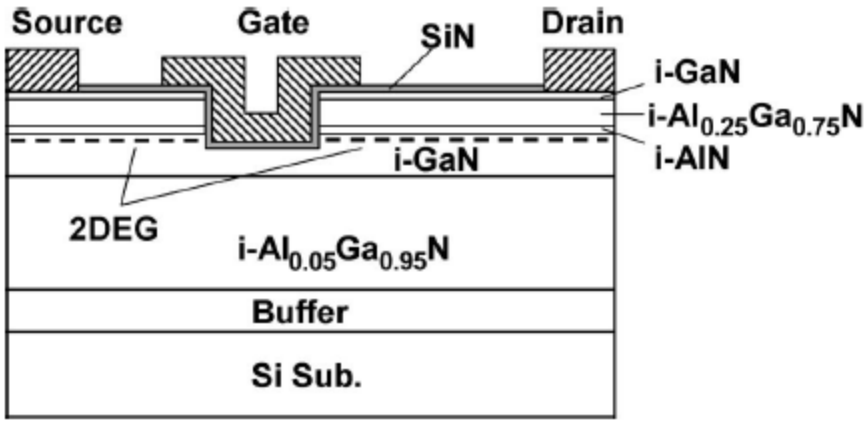
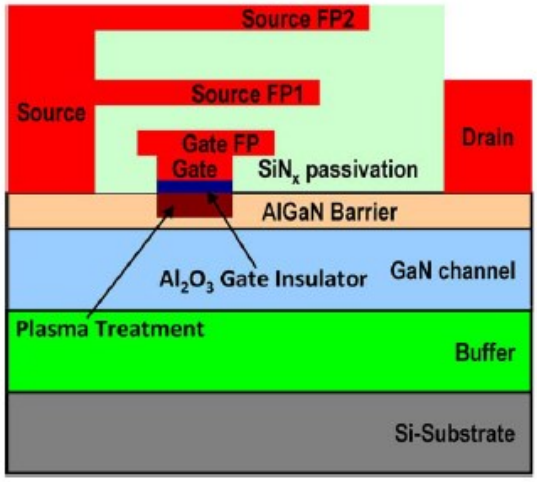



Figure 2.9: Schematic of the AlGaN/GaN recessed MIS-gate HFET [35].

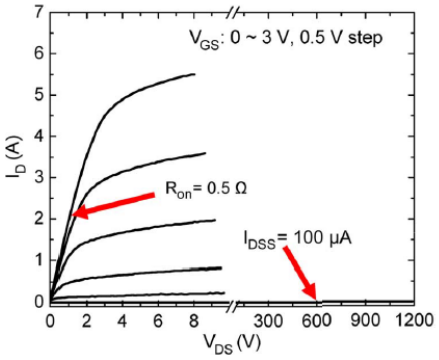
Due to the requirements of the precise control of the gate etching depth, positive threshold voltage is obtained in some device configurations by a full removal of the AlGaN layer beneath the gate regions of metal-insulator-semiconductor (MIS)-HFET type GaN device structure. The threshold voltage of this device is less sensitive to the exact etching depth. A high threshold voltage of this type of GaN MIS-HFET ($V_{th}$ > 5 V) was reported by Oka *et al.* [35] as shown in Figure 2.9. The main disadvantage of the complete removal of the 2DEG channel beneath the gate compared to partial removal as the recessed gate HEMT is that it increases the on-resistance of the device. Recently, Ikeda *et al.* [36] demonstrated a hybrid MIS-HFET device in which the on-resistance was reduced to 7.1 mΩ.cm$^2$ with 1.21 kV breakdown voltage.

***iii) Plasma Implanted Gate Enhancement-Mode Operation***

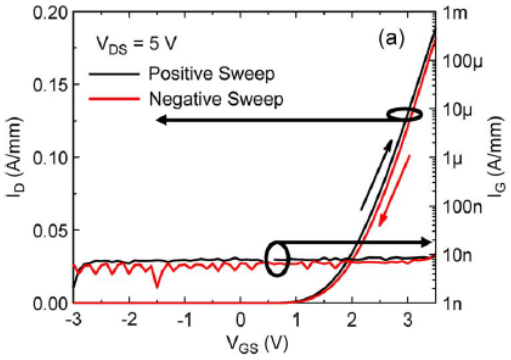
A normally-off operation of AlGaN/GaN HEMT can be obtained by implanting a plasma treated buried layer on AlGaN layer [37]-[40]. This type of GaN device, which incorporates




(a)




(b)




(c)

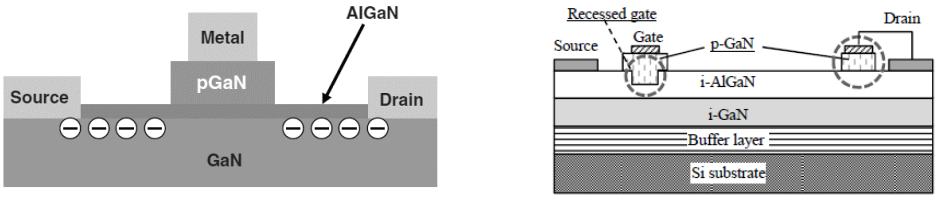
Figure 2.10: (a) Schematic of plasma implanted gate GaN HFET. (b) DC output characteristics and (c) DC transfer characteristics of the device [40].

a halide-based plasma treatment to obtain enhancement-mode operation, has been reported by R. Chu *et al*. from HRL laboratories [40]. The fluorine plasma treatment effectively creates some trapped negative charges and depletes the 2DEG charges beneath the gate and thus results in positive threshold voltage. An additional Cl-based plasma helps improve the transconductance and the threshold hysteresis. The threshold voltage defined by the gate

voltage to achieve a drain current of 1 μA/mm is obtained to be 0.64 V. The device structure is shown in Figure 2.10(a) where the atomic layer deposition of $Al_2O_3$ gate insulator is adapted to reduce the gate leakage current. Field plates are connected to the gate and the drain regions to achieve a current collapse-free operation. This device includes multiple field plate operation with one field plate above the gate and two field plates connected to the source electrode achieving a high breakdown voltage of 1.2 kV. The on-resistance of this device is reported to be 9 $m\Omega.cm^2$. The DC output characteristics and the transfer characteristics of this device are shown in Figure 2.10(b) and 2.10(c), respectively.

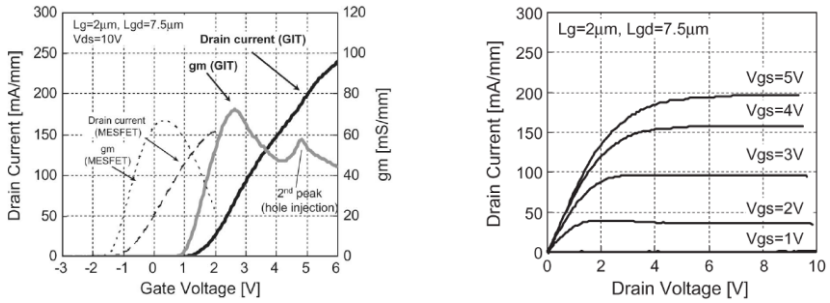
***iv) GaN Gate-Injection Transistor (GIT)***

Another approach to obtain enhancement-mode operation for AlGaN/GaN HEMT is to use a *p*-doped GaN layer beneath the gate [41], as shown in Figure 2.11(a). This type of configuration is often termed as gate-injection transistor (GIT). The *p*-doped GaN layer above the intrinsic AlGaN layer lifts up the potential barrier by forming a diode-like depletion layer without any gate voltage. With a sufficiently low thickness of AlGaN layer, all the 2DEG charges beneath the gate can be depleted from the channel to enable normally-off operation. At a positive gate voltage above the built-in potential between the *p*-doped GaN layer and the AlGaN layer removes the depletion charges and the drain current begins to flow due to the 2DEG channel charges. The threshold voltage obtained in this configuration is around 1~3 V. Further increase in gate voltage results in injection of hole in the GaN layer beneath the AlGaN layer and these injected holes accumulate more electrons enhancing the conductivity of the 2DEG channel. The lower mobility of hole ensures that the injected holes stay around the gate while the electrons are moved by the




(a) (b)

Figure 2.11: Schematic cross section of (a) a conventional GIT [41] and (b) HD-GIT by Panasonic™ [42].




(a) (b)

Figure 2.12: DC characteristics of GaN-GIT: (a) Transfer characteristics and (b) output characteristics [41].

drain bias. Thus, this configuration implements the advantage of conductivity modulation as observed in insulated gate bipolar transistors (IGBTs). A recent work by Kaneko *et al.* [42] of Panasonic group involves modification of the GaN-GIT structure to hybrid drain-embedded GIT (HD-GIT) which includes a *p*-doped GaN region next to the ohmic drain. This layer is electrically connected to the drain as shown in Figure 2.11(b). This modified configuration helps mitigate current-collapse as the trapped electrons at the drain edge at the off-state are released by the injected holes from the *p*-GaN layer. In order to maintain sufficient 2DEG sheet carrier concentration beneath the drain region, the thickness of

AlGaN layer is increased. However, to maintain enhancement-mode operation at the same time the thickness of AlGaN layer is reduced by selective etching forming a recessed gate structure. This new modification increases the breakdown voltage up to 850 V with a small increase in the leakage current compared to the conventional GIT structure. The DC transfer characteristics of this device are shown in Figure 2.12(a), which compare the drain current and the transconductance of this device with conventional Schottky gate MESFET. The drain current is higher due to the conductivity modulation and there is a second peak in the transconductance ($g_m$) characteristics due to the hole injection and the electron accumulation at increased gate voltage. The specific on-resistance of the device is reported to be 2.6 mΩ.cm$^2$. Figure 2.12(b) shows the $I_{ds}$-$V_{ds}$ characteristics of this device in both the on-state and the off-state [41].

# Chapter 3

# Modeling of GaN Device

## 3.1. Different Types of Device Model

The main objective of semiconductor device modeling is to achieve a predictive description of the device performance at some specific conditions such as bias (e.g. applied voltages and currents), environment (e.g. temperature, radiation), and physical characteristics (e.g. geometry, doping levels). Formulation of a valid model involves trade-off between accuracy and computational speed to analyze the particular device operation in a circuit and in a system [43]. In general, semiconductor device models can be categorized as the following types:

***i) Physics-Based or Analytical Model***

This model is developed by studying the physical phenomena that occur during the device operation based on the specific device parameters. This type of model is also called analytical model and includes physics-based equations to describe a particular operation. The model is very accurate in predicting device behavior but includes very complex equations and is very time consuming for simulation. However, for new semiconductor devices, it is very important to study this type of model to achieve a proper insight into the device behavior.

***ii) Behavioral or Empirical Model***

This type of model predicts device operation by implementing mathematically fitted equations without considering the actual physical mechanism. This provides a very fast

simulation, but the accuracy is often compromised when the operating condition goes beyond the fitting conditions.

***iii) Semi-Physics or Semi-Empirical Model***

This type of model attempts to establish a balance between the accuracy obtained from physics-based model and the simulation speed from empirical model. This model often implies practical assumptions to simplify the physics-based equations and then mathematically fit the simplified equations for a wide range of conditions. For most practical operations such as for SPICE-based circuit simulators, this type of model is preferred.

***iv) Numerical Model***

This type of model involves numerical simulation of the device to predict the device performance under different operating conditions. Numerical simulation is often performed by using various computer-based tools such as SILVACO, Sentaurus TCAD, MEDICI, etc. In general, numerical models are used as virtual environment for device optimization under different conditions and the results can be used to validate the simulation model for other operating conditions which are otherwise very expensive and time consuming to achieve by actual measurement.

## 3.2. Properties of GaN HEMTs for High Power Applications

In the previous chapter, it has been discussed that GaN as a wide bandgap material has its own unique material properties and the device developed for power electronic applications

has its own unique characteristics. Therefore, to achieve the device model, it is very important to study the impact of the material properties and device structures of GaN HEMTs which results in some specific device operating conditions for the particular application. In this research, the following physical phenomena related to GaN HEMT for high power and high temperature application will mainly be considered.

***i) Charge Control and Transport Characteristics***

Due to the availability of two-dimensional electron gas (2DEG) between the interface of AlGaN and GaN, the basic principle of operation of most GaN-based HEMT devices is determined by this 2DEG charge density [44], [45]. The substrates for GaN HEMT are mainly SiC or sapphire and a native channel between the source and the drain of the device is formed by the 2DEG. Unlike Si, GaN does not have a native insulating oxide and thus a Schottky gate electrode is usually implemented for this device [46]. In order to achieve a normally-off or an enhancement-mode device, different schemes have been adopted by many researchers. Among these approaches cascode structure, recessed-gate configuration, plasma implanted enhancement-mode operation and *p*-doped GaN gate-injection transistor (GIT) are the most common [25]- [42]. The device characteristics can be further improved by incorporating a thin insulating layer under the gate. Presence of the insulating layer under the gate reduces the gate leakage currents by several orders of magnitude [47], [48]. With so many different configurations of the device, it is very important to predict the impact of the variation of any particular modification on the device parameters. The charge control and the carrier transport models are typically used to determine *I-V* and *C-V* characteristics of the devices. In addition, the carrier transport model considers carrier-

impurity ion scattering, carrier-carrier scattering, alloy composition, interface roughness, polar optical phonon, acoustic phonon, piezoelectric polarization, intervalley scatterings, carrier generation due to impact ionization as well as gate leakage [49]-[51].

***ii) Self-Heating and Charge Trapping Model***

The temperature response of GaN HEMT device to instantaneous power dissipation has been shown to be significant in high frequency switching operations even though the self-heating process has a very slow time constant [52]. The performances of GaN-based devices are also limited by trapping effects. The presence of traps not only results in current collapse in the current-voltage characteristics but also makes the electrical characteristics to be dependent on frequency. Trapping effects will affect the power handling capability as well as harmonic contents of the power electronic circuits [53], [54]. Self-heating effect of the devices needs to be modeled by considering temperature dependent variation of the device behavior due to dynamic power dissipation. The effect of charge trapping can be modeled by considering the concentration of acceptor and donor type 'trapping centers' at a particular energy level. These models are very helpful in determining the parasitic losses of the device for high power applications.

***iii) Breakdown Voltage Model***

Achieving high breakdown voltages with a minimum on-resistance is another major challenge for power transistor design [55], [56]. For this reason, single or multiple field plates have been implemented to increase the breakdown voltages in AlGaN/GaN HFETs [31], [32], [57]. Another approach to achieve high breakdown voltage in AlGaN/GaN heterostructure field-effect transistors (HFETs) is by suppressing the surface flashover

using solid encapsulation material or by immersing the device in high dielectric strength liquids (e.g. Fluorinert®) [58]. Current collapse is another phenomenon that has been widely reported for lateral GaN devices which causes a temporary increase in on-resistance and is proportional to the blocking voltage [59], [60]. In order to mitigate these issues, it is important to model physical mechanisms of these effects and incorporate them in the device model resulting in a more accurate prediction of the device performance.

***iv) High Temperature Model***

GaN transistor as a wide bandgap semiconductor device is one of the suitable choices for the next generation high power applications [55], [61]. However, high power operation of the device is often associated with high temperature operation as the increase in the output power causes heat dissipation. This elevated temperature degrades the performance of the device as many of the device operating parameters are significantly dependent on temperature. Some of such physical phenomena include generation of leakage currents, mobility degradation, and change in the threshold voltage at higher temperatures. Analytical model can be used to predict the high temperature performances of a device by considering the device temperature-dependent parameters.

## 3.3. GaN Device Models in Literature

Due to the inherent ability of GaN devices to operate in high frequency, most GaN transistors and the models were initially developed for RF applications. However, there have been some research works on GaN transistors which exhibited significant potential in

high power application [62]- [64]. During last few decades different configurations of GaN transistors have been developed to adopt their applications in power electronics with low on-resistance, enhancement-mode operation and high breakdown voltage. Although there have been several works on various types of GaN transistors and circuit topologies for power electronic applications reported in literature, modeling and device characterization efforts are relatively inadequate.

In general, the existing device models for GaN transistors can be categorized in four types such as empirical or behavioral model, semi-physics-based model, analytical or physics-based model and numerical model. An empirical SPICE model for GaN transistor has been developed by Okamoto *et al.* [65] in which the model is used to simulate AC-AC direct converter to calculate power loss. Although this research demonstrates an improvement in power loss by 30% by using GaN transistor over Si power device, the empirical model is developed using some fitting equations without providing any physical insight of the actual device operation. To address this issue, a few semi-physics-based models are developed for SPICE simulation [66], [67]. Most of these models are developed based on the Staz model which is originally developed for short channel gallium arsenide (GaAs) MESFETs. Although most of the GaN devices are also high electron mobility transistors (HEMT) or heterojunction field effect transistors (HFET), their device structures are significantly different from the GaAs-based HEMTs or HFETs.

A number of physics-based models or analytical models have been developed to explain the physical operation of these devices incorporating many unique properties present in GaN material systems [68], [69]. However, most of these models are developed

considering the basic GaN HEMT structure rather than considering the device modification adopted for high power applications.

Numerical simulation is performed to verify the physics-based models which allows simulation of the device in a virtual environment with various operating conditions. A few numerical models have already been developed for GaN HEMT devices [70], [71] which incorporate the sheet polarization charge model for group III-V materials. These models are tested and verified with experimental device measurement data and thus can be used to study the device performance for various device geometries and parameters. Table 3.1 summarizes the published GaN device models and their main contributions.

TABLE 3.1
CONTRIBUTIONS OF DIFFERENT PUBLISHED MODELS FOR GAN TRANSISTOR

| Model | Model type | Contributions |
|---|---|---|
| Okamoto *et al.* (2011) [65] | Empirical | • SPICE simulation to calculate power loss in AC-AC converter module<br>• implemented using general fitting equations |
| Waldron *et al.* (2013) [66] and Hoffmann *et al.* (2014) [67] | Semi-physics | • implement static and switching characteristics<br>• based on Statz model developed for GaAs MESFET |
| Yigletu *et al.* (2013) [68] and Khandelwal *et al.* (2012) [69] | Physics | • implement 2DEG charge density model<br>• include physical phenomena such as carrier velocity saturation, mobility degradation, self-heating etc. |
| Huang *et al.* (2012) [70] and Strauss *et al.* (2014) [71] | Numerical | • TCAD model for GaN HEMT including polarization sheet charge data, numerical mobility model etc. |

# Chapter 4

# Analytical Modeling of GaN Transistor

In this chapter, an analytical model is presented for GaN HEMT with an additional *p*-doped GaN layer beneath the metal gate electrode to enable normally-off operation [41],[72],[73]. This enhancement-mode device structure, called the gate-injection transistor (GIT), has been recently commercialized by Panasonic™. The model presented in this chapter considers the impact of the additional *p*-type gate on achieving a positive threshold voltage for the *n*-channel device. It also includes the impact of carrier spill-over on 2DEG charge density and the reduction in mobility at high gate voltage to derive the current-voltage characteristics for the device. In addition, the model addresses high temperature operation by considering the physical parameters which are significantly impacted by the change in temperature.

## 4.1. Device Structure

Figure 4.1 shows the cross-sectional schematic of the *n*-channel GaN-GIT device used in this work which is based on the device reported in [74]. The basic device structure of GIT is typically a lateral heterojunction field-effect transistor (HFET) or high electron mobility transistor (HEMT). The two-dimensional electron gas (2DEG) creates the channel of the transistor which is formed by spontaneous polarization due to the crystal polarity of wurtzite GaN material. This 2DEG is augmented by piezoelectric polarization due to the lattice mismatch between AlGaN and GaN [75]. In GaN HEMT, this inherently formed

channel along with a Schottky gate electrode achieves a normally-on *n*-channel device with a negative threshold voltage. However, to reduce the overall power loss for high power applications, it is important to have the transistor turned off in the absence of any applied gate bias. To achieve this normally-off operation, a Mg-doped *p*-type GaN layer is inserted beneath the metal electrode to achieve a GIT structure. The *p*-GaN gate helps deplete the 2DEG charge from the channel to turn-off the current conduction under no applied gate bias. Unlike the recessed gate or plasmonically achieved enhancement-mode operation, the GIT structure does not compromise the electron density in the 2DEG at positive gate bias and thus the on-resistance, $R_{on}$ remains small [41]. The AlGaN buffer layer with low Al content underneath the *p*-GaN gate layer facilitates further increase in the threshold voltage of the device. The AlGaN barrier layer with high Al content helps improve $R_{on}$ which is

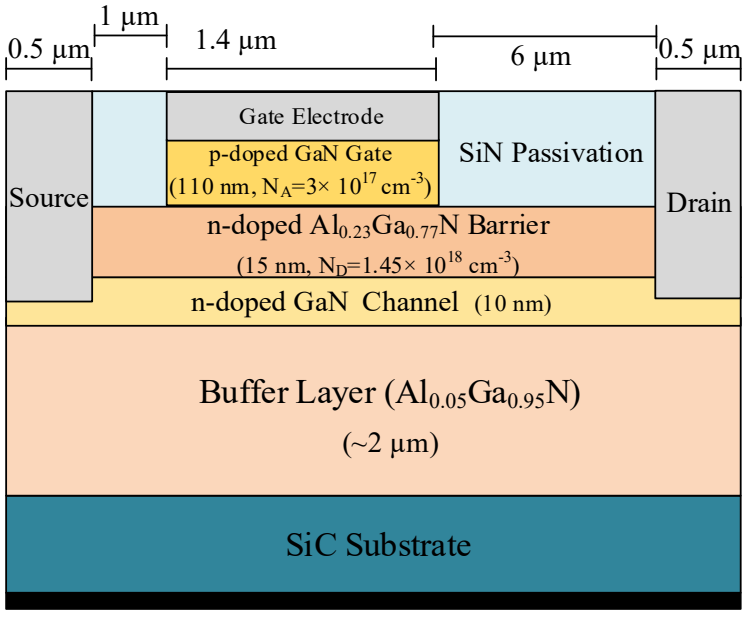



Figure 4.1: Cross-sectional schematic of the GaN-GIT device used in the model showing different layers, major dimensions and doping concentrations [74].

compromised due to the low Al content of the buffer layer while suppressing the punch-through effect of the device.

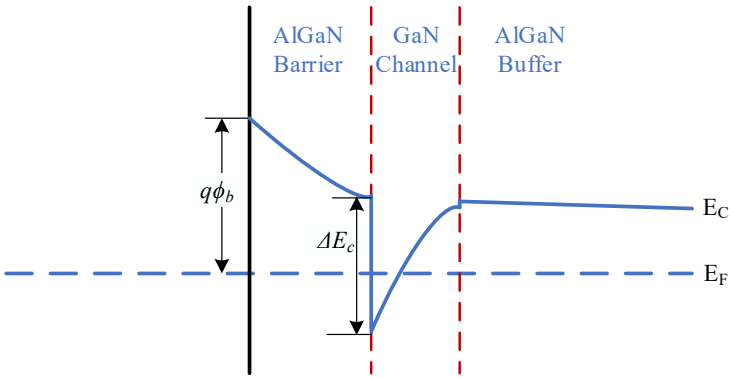
## 4.2. Model Description

Table 4.1 lists all the major parameters used in this model [76]. The principle of operation of the GaN HEMT device depends on the formation of the 2DEG channel layer and modeling of this 2DEG carrier density forms the foundation of the analytical model of the device. Recently, several works on analytical model for the 2DEG charge density in the AlGaN/GaN heterostructure have been reported in the literature [77]- [79]. However, these models only consider the basic HEMT structure and the impact of the insertion of *p*-gate layer under the metal gate and other modifications for practical high power application is not considered. Figure 4.2 shows the impact of a *p*-GaN gate on the conduction band with respect to the Fermi energy level [76]. Without the *p*-GaN gate the inherently formed

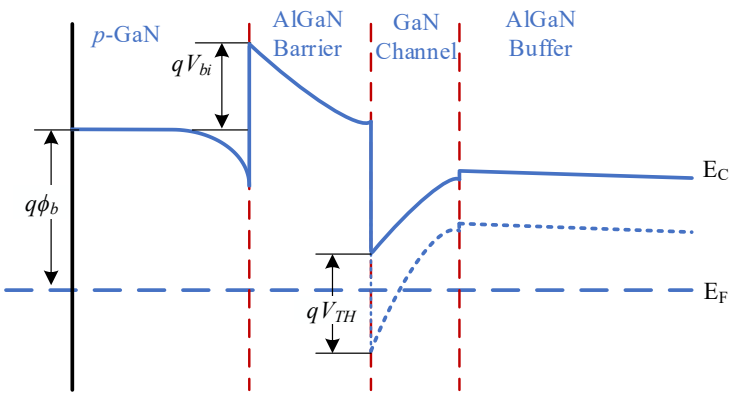
TABLE 4.1
LIST OF MODEL PARAMETERS [76]

| | |
|---|---|
| $\varepsilon$: Dielectric constant | $d$: AlGaN barrier layer thickness |
| $N_A$: Doping concentration of *p*-GaN | $N_D$: Doping concentration of AlGaN barrier |
| $\phi_b$: Schottky barrier height | $\sigma$: Polarization charge density |
| $E_g$: Energy bandgap | $\Delta E_C$: Conduction band offset |
| $\mu_{2DEG}$: 2DEG Mobility | $\mu_b$: AlGaN bulk Mobility |
| $\gamma_0$, $\gamma_1$: Constants obtained from cyclotron resonance experiment | |
| $N_C$: effective density of state at the conduction band | |
| $k$: Boltzmann constant | $E_{crit}$: Critical electric field |

2DEG carrier concentration at the heterojunction between the AlGaN barrier and the GaN channel layers causes the conduction band to dip below the Fermi level (Figure 4.2(a)). This results in a depletion-mode *n*-channel device with a negative threshold voltage which needs to be applied to remove the 2DEG concentration to turn off the device. However, when an additional *p*-GaN gate is inserted, it adds to the built-in potential at the heterojunction diode between the *p*-doped GaN and the *n*-doped AlGaN barrier layers. This




(a)




(b)

Figure 4.2: Schematic diagram of the conduction band, $E_C$ with respect to the Fermi level: (a) Without any *p*-GaN gate and (b) with a *p*-GaN gate (dotted line shows the formation of 2DEG while the device is turned on) [76].

additional built-in potential depletes the 2DEG carriers and pulls up the conduction band above the Fermi level. Thus, an enhancement-mode operation is achieved with the insertion of *p*-GaN gate in a GIT device. To turn on the device, a gate voltage greater than the positive threshold voltage needs to be applied that overcomes the built-in potential and regenerates the 2DEG carriers which form the channel of the device as shown by the dashed line in Figure 4.2(b). The 2DEG carrier concentration and thus the positive threshold voltage for the GIT can be modeled by considering the impact of *p*-doped GaN gate on the device operation.

In this model, the impact of *p*-GaN gate on the positive threshold voltage is considered by taking into account the built-in potential of the *p*-GaN and the *n*-AlGaN heterojunction diode. This built-in potential depends on sheet carrier concentration, band energy levels, and doping concentrations of these two layers. The sheet carrier concentration model is further modified by considering the carrier spill-over phenomenon at high gate potential. Parallel conduction due to this phenomenon also influences the effective channel mobility which is considered in the proposed model to obtain a better match with the experimental data. The room temperature analytical model includes the impact of temperature on different device parameters. The updated values of these parameters at the elevated temperatures are used to obtain the high temperature performance of the device. To model the impact of self-heating effect on the operation of the device, the increase in temperature is calculated using the thermal resistance and the power dissipation at a specific current density and is fed back to the temperature dependent model. The following subsections describe each model step in details and include the corresponding analytical expressions.

### 4.2.1. 2DEG Charge Density and Threshold Voltage

Considering all the potential drops the 2DEG sheet carrier density, $n_s$ can be expressed as [80],

$$n_s = \frac{\varepsilon}{qd}\left(V_G - V_{TH} - \frac{E_F}{q}\right) \tag{4.1}$$

where $d$ is the thickness of AlGaN barrier layer, $V_G$ is the applied gate voltage, $V_{TH}$ is the threshold voltage, and $E_F$ is the Fermi energy level.

The threshold voltage, $V_{TH}$ of the device includes the impact of Schottky barrier height, bandgap offset of the heterostructure, built-in potential along the *p*-GaN gate and the potential due to the polarization charges. The analytical expression for $V_{TH}$ can be written as,

$$V_{TH} = \phi_b - \frac{\Delta E_C}{q} - \frac{qd^2}{\varepsilon} N_D + \frac{qd}{\varepsilon} \sigma + V_{bi} \tag{4.2}$$

where $\phi_b$ is the Schottky barrier height, $\Delta E_C$ is the conduction band offset in the AlGaN/GaN heterostructure, $N_D$ is the doping concentration of the AlGaN barrier layer, $\sigma$ is the polarization charge and $V_{bi}$ is the built-in potential of the *p*-GaN/*n*-AlGaN layer.

The *p*-GaN gate and the *n*-type AlGaN barrier layer form a *p*-*n* heterojunction diode that results in a built-in potential. This built-in potential at the *p*-GaN gate with the AlGaN barrier layer heterojunction diode helps deplete any polarization charge in the channel achieving the normally-off operation. The built-in potential depends on the characteristics of AlGaN/GaN heterostructure as shown in (4.3), where $n_{sp}$ is the 2DEG sheet carrier concentration in the gate diode [81].

$$V_{bi} = \frac{E_g(GaN)}{q} - \frac{E_F - \Delta E_C}{q} - \frac{qn_{sp}^2}{2\varepsilon(N_A + N_D)} \quad (4.3)$$

where $n_{sp}$ is the 2DEG sheet carrier concentration in the gate diode and $N_A$ is the doping concentration of *p*-GaN.

When the device turns on, the polarization charge, $\sigma$ reappears similar to the depletion-mode devices [82]. The polarization charge density can be modeled by using spontaneous and piezoelectric polarization models for AlGaN/GaN heterostructure [75]. The polarization charge density is a function of the mole fraction and the thickness of AlGaN as well as the lattice parameters of the wurtzite crystal structure of GaN material. The net polarization charge can be expressed as a function of Al mole fraction, *m*,

$$|\sigma(m)| = \left| 2\frac{a(0) - a(m)}{a(m)} \left\{ e_{31}(m) - e_{33}(m)\frac{C_{13}(m)}{C_{33}(m)} \right\} + P_{sp}(m) - P_{sp}(0) \right| \quad (4.4)$$

where $a$ is equilibrium value of the lattice constant, $e_{31}$ and $e_{33}$ are piezoelectric coefficients, $C_{13}$ and $C_{33}$ are elastic constants and $P_{sp}$ is the spontaneous polarization induced sheet charge. All these parameters are functions of Al mole fraction, *m* of $Al_mGaN_{1-m}N$ layer and the experimentally derived expressions are listed in Table 4.2.

The energy band offset, $\Delta E_C$ can be calculated from the bandgap energy of AlGaN and GaN as shown in (4.5).

$$\Delta E_C = 0.7(E_g(m) - E_g(0)) \quad (4.5)$$

where the bandgap energy, $E_g$ is also function of mole fraction, *m* as shown in Table 4.2.

TABLE 4.2
MOLE FRACTION DEPENDENT PARAMETERS OF ALGAN/GAN HETEROSTRUCTURE [75]

| Symbol | Quantity | Expression |
|---|---|---|
| $a$ | Lattice constant | $(-0.077m + 3.189) \times 10^{-10}$ m |
| $e_{31}$ | Piezoelectric coefficient | $(-0.11m - 0.49)$ C/m$^2$ |
| $e_{33}$ | Piezoelectric coefficient | $(0.73m + 0.73)$ C/m$^2$ |
| $C_{13}$ | Elastic constant | $(5m + 103)$ GPa |
| $C_{33}$ | Elastic constant | $(-32m + 405)$ GPa |
| $P_{sp}$ | Spontaneous polarization induced sheet charge | $(-0.052m - 0.029)$ C/m$^2$ |
| $E_g$ | Bandgap energy | $mE_g(AlN) + (1 - m) - m(1 - m)$ eV |
| $\epsilon$ | Dielectric constant | $-0.5m + 9.5$ |
| $q\phi_b$ | Schottky barrier height | $1.3m + 0.84$ eV |

One of the challenges encountered in analytical modeling of the 2DEG sheet carrier concentration, $n_s$ is that the Fermi level, $E_F$ itself is a non-linear function of $n_s$. $E_F$ is derived from the solution of the Schrodinger equation for the two lowest sub-band energies as shown below [75].

$$E_F = E_0 + \frac{\pi\hbar^2}{m^*} n_s = \gamma_0 n_s^{2/3} + \gamma_1 n_s \tag{4.6}$$

$$E_0 = \left\{ \frac{9\pi\hbar q^2}{8\epsilon_0\sqrt{8m^*}} . \frac{n_s}{\epsilon} \right\}^{2/3} = \gamma_0 n_s^{2/3} \text{ and } \gamma_1 = \frac{\pi\hbar^2}{m^*} \tag{4.7}$$

where $m^*$ is the effective electron mass and approximately equal to 0.22 times of electron rest mass [75].

### 4.2.2. Carrier Spill-Over at Higher Gate Bias

For most depletion-mode GaN HEMTs the applied gate bias does not exceed 1 V. However, for the recently developed enhancement-mode GaN power HEMTs the gate bias

can be as high as 5 V. When the applied gate voltage is high, the conduction band near the AlGaN barrier layer will drop below the Fermi level which will significantly increase the carrier concentration of the AlGaN barrier layer. This phenomenon is also known as carrier spill-over and is reported in experimental work on the measurement of drift mobility and gate charge on AlGaN/GaN devices [83], [84].

In order to model the carrier concentration of the AlGaN barrier layer, $n_b$, the effective electric field in the AlGaN layer is used in a simplified Fermi-Dirac statistic by considering $E_F > \Delta E_C$ [85].

$$n_b = \frac{N_C}{bc}\left[\frac{E_F - \Delta E_C}{kT} + \ln(c)\right] \tag{4.8}$$

$$b = \frac{q^2(\sigma - n_{s.eff} - n_b)}{kT}, \text{ c=0.27} \tag{4.9}$$

The effective 2DEG carrier concentration at any point can be then modified from (4.1) as,

$$n_{s.eff}(V_x) = \frac{\varepsilon}{qd}\left(V_{GS} - V_{TH} - V_x - \frac{E_F}{q}\right) - n_b \tag{4.10}$$

where $V_x$ is the lateral potential at that point due to the applied drain-to-source voltage.

The carriers in the barrier layer create a parallel conduction path along with the 2DEG channel which degrades the effective mobility because the bulk mobility at AlGaN layer is much lower than the 2DEG mobility. For this reason, the effective mobility for the channel current conduction of the device is modeled by,

$$\mu_{eff} = \frac{n_{s.eff}\mu_{2DEG} + n_b\mu_b}{n_{s.eff} + n_b} \tag{4.11}$$

where, $\mu_{2DEG}$ is the 2DEG mobility and $\mu_b$ is the bulk mobility of electron in the AlGaN barrier layer.

### 4.2.3. Drain-Current Model

The drain current of the device is calculated by integrating the drift equation over the channel length and the drain-to-source potential with the drift velocity model adopted from [86].

$$I_{DS} = \frac{-q\mu}{L+K_1 V_{DS}} \left[ \left( \frac{qd}{2\varepsilon} + \gamma_1 \right) \left\{ \left( n_{s.eff}(V_D) \right)^2 - \left( n_{s.eff}(V_S) \right)^2 \right\} + \frac{2}{5} \left\{ \left( n_{s.eff}(V_D) \right)^{\frac{5}{3}} - \left( n_{s.eff}(V_S) \right)^{\frac{5}{3}} \right\} \right] \tag{4.12}$$

where $K_1 = \frac{n_2}{\epsilon_{crit}}$ and $n_2 = 4.1$ which are determined from the mobility model of wurtzite GaN [86].

### 4.2.4. Self-Heating and High Temperature Model

One of the characteristics of GaN device is the self-heating present at high current density which tends to reduce the current in the saturation region. To model the self-heating effect the change in the temperature due to a specific power dissipation is calculated from the thermal conductivity of the device using (4.13) and (4.14) and the drain current is recalculated using the temperature dependent model.

$$\Delta T = P_D R_{th} \tag{4.13}$$

$$T_{operating} = T_{ambient} + \Delta T \tag{4.14}$$

where, $P_D$ is the dissipated power calculated from the biasing operation and the device current and $R_{th}$ is the thermal resistance of GaN.

In order to model the device for high temperature applications, the parameters which significantly vary with temperature is considered. In general, mobility, thermal conductivity, effective carrier concentration and bandgap energy are the parameters which have the most significant impact due to temperature variation. At higher temperature the bandgap energy of a semiconductor tends to decrease. The temperature dependence of the bandgap energy is usually described by the empirical Varshni formula [87] as shown in (4.15).

$$E_g(T) = E_{g.0} - \frac{\alpha_g T^2}{\beta_g T} \tag{4.15}$$

where $E_{g.0}$ is the bandgap energy at 0 K and $\alpha_g$ and $\beta_g$ are empirically determined parameters for III-V compound semiconductors. For bandgap energy of AlGaN, similar expression shown in Table 4.2 is used for a particular value of Al mole fraction. On the other hand, the spontaneous and piezoelectric polarization coefficients for AlGaN/GaN system do not have any significant impact due to the increase in temperature [88].

Mobility, thermal conductivity, and carrier concentration tend to decrease with elevated temperature and are usually modeled using power exponent of temperature along the measured value of these parameters at 300 K.

$$\mu\,(T) = \mu_{300K}\left(\frac{T}{300K}\right)^{-\alpha_\mu} \tag{4.16}$$

$$\kappa(T) = \kappa_{300K}\left(\frac{T}{300K}\right)^{-\alpha_\kappa} \tag{4.17}$$

$$n_{s.eff}(T) = n_{s.eff.300K}\left(\frac{T}{300K}\right)^{-\alpha_n} \tag{4.18}$$

where $\alpha_\mu$, $\alpha_\kappa$ and $\alpha_n$ are empirically determined values.

The Schottky barrier height shows a linear dependence on temperature [89], [90] and is thus modeled using (4.19).

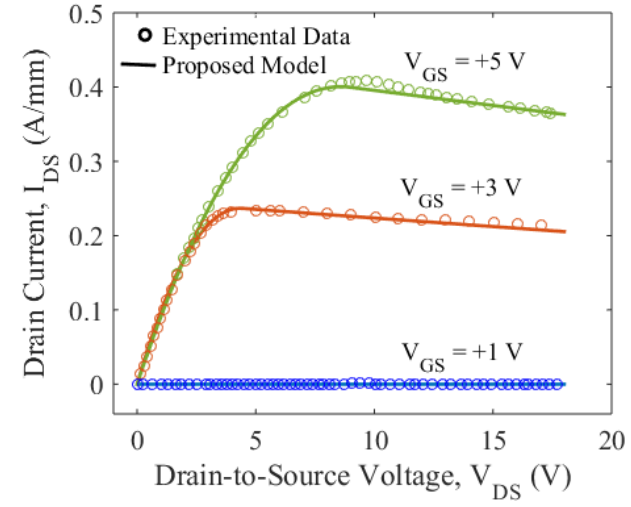
$$\phi_b(T) = \phi_{b.300K} + \alpha_\phi T \tag{4.19}$$

where $\alpha_\phi$ is an empirically determined value.

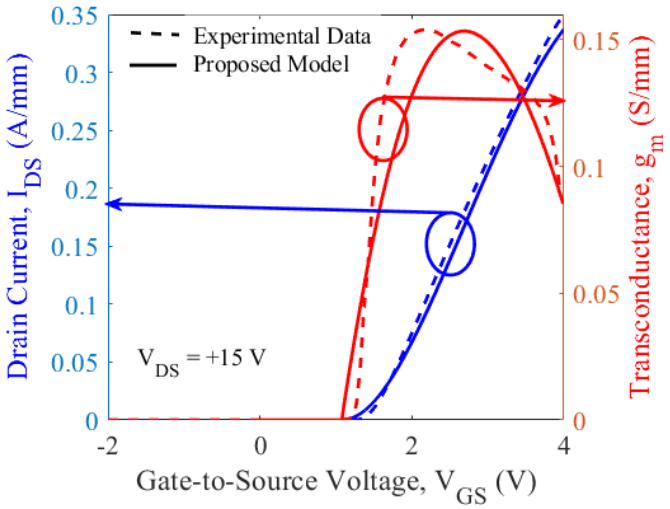
## 4.3. Results and Discussion

The output and the transfer characteristics of the device obtained from the model are compared with the measured data [74] at room temperature as shown in Figure 4.3. It can be seen from the figure that the experimental measurement data and the model show good matching. As shown in Figure 4.3 (a), there is a significant self-heating at high current density which is well-predicted by the model. However, the model considers a long channel device and ignores pinch-off and channel length modulation effects. In practice, the channel length modulation tends to compensate the self-heating effect by increasing the drain current in the saturation region. For a gate voltage of 3 V, the self-heating effect slightly underestimates the drain current at high drain-to-source voltage which can be attributed to the ignored pinch-off condition. However, for a gate voltage of 5 V, the self-heating effect completely dominates over these two phenomena and the model shows a better match. In addition, the transconductance curve shows discrepancies at high gate

voltage as shown in Figure 4.3 (b) [76]. This can be attributed to the fact that at high gate potential, there will be hole injection through the *p-n* heterojunction diode that can further accumulate electrons in the channel. However, this phenomenon known as conductivity modulation [41] is difficult to model analytically due to the presence of impurities, trapping effects and recombination of injected holes.



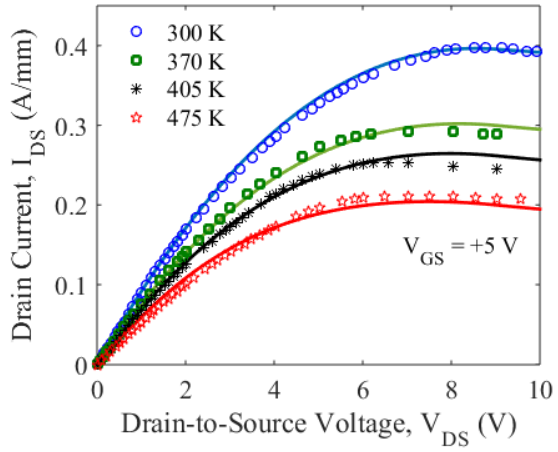

(a)



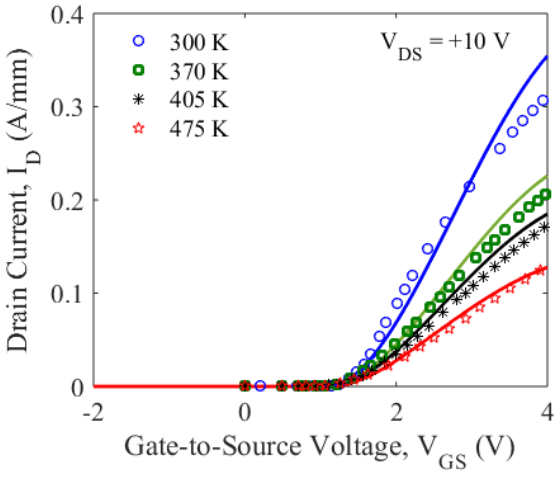

(b)

Figure 4.3: (a) DC output characteristics with different gate bias and (b) transfer characteristics [76].

The output and the transfer characteristics of the device with higher temperature are shown in Figure 4.4 with experimentally measured results from [74]. The plots clearly show that the drain current decreases at higher temperature due to the reduction in mobility and sheet carrier concentration at elevated temperatures. The transfer characteristics of the device also show deviation from the experimentally measured data. This can also be attributed to the gate voltage dependent phenomena such as the carrier injection at high bias.




(a)




(b)

Figure 4.4: (a) Output characteristic at different temperatures and (b) Transfer characteristics at different temperatures (symbol: experimental data; solid-line: proposed model) [76].

# Chapter 5

# TCAD Simulation of the GaN Transistor

In many cases, actual device testing and characterization can be very complicated, time-consuming, and expensive. In addition, for many commercially available devices, the details of device geometry and many device parameters can be unknown. A numerical device simulator can be useful by providing a virtual environment where the device can be simulated under various conditions. For this reason, numerical device simulation has been performed for the GaN-GIT devices so that the physics-based model developed in Chapter 4 can be verified for various device geometries and parameters.

## 5.1. Technology Computer Aided Design (TCAD)

Technology computer-aided design (TCAD) tools implement the numerical simulation of the device which enables prediction of the device behavior by varying different process and operating parameters. In order to achieve this, the overall package of the TCAD includes several tools specifically designed to implement various steps in device processing for simulation of device performance. Figure 5.1 shows some of the major tools inside a TCAD package such as device structure editor, device processing, device simulation, and data visualization which can be combined in a common virtual environment to analyze device performances based on various input parameters [91]. Commercial standard TCAD package such as Synopsys Sentaurus$^{TM}$ TCAD has been used in this work and the following section describes the operation of the principal tools of TCAD used to simulate the GaN transistor.

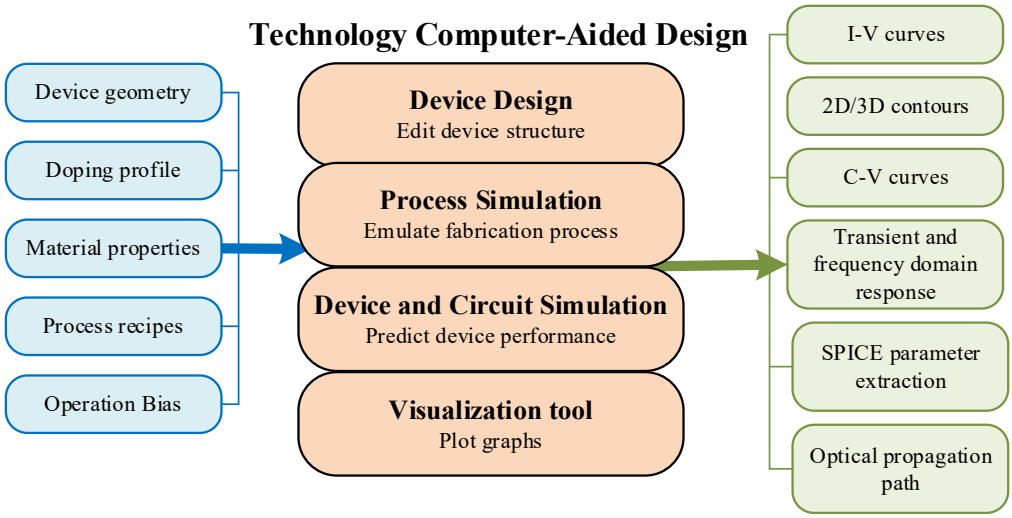



Figure 5.1: Combination of different tools inside a TCAD device simulator with input and output files.

### *i) Device Design Tool*

Device design tool is used to construct the geometrical structure of the device either by a graphical user interface (GUI) or by the scripting language. This tool allows the designer to select materials for different device layers, doping profiles, and other device geometrical parameters. Synopsys Sentaurus™ includes Sentaurus Structure Editor (SSE) [92] to perform this particular task.

### *ii) Device Process Tool*

Device process tool emulates different fabrication steps of the device processing. This tool allows the designer to choose different process parameters and analyze the impact of these parameters on device performance. For Synopsys Sentaurus™ TCAD this task is performed by Sentaurus Process [93].

***iii) Device Simulation Tool***

Device simulation tool allows the simulation of electrical, optical, and thermal characteristics of the device on a set of applied operating conditions. It also includes the impact of the device structure and process parameters on device performance so that the result can be used as an alternative to original device testing data with an experimental setup. Synopsys Sentaurus$^{TM}$ TCAD includes Sentaurus Device for this task [94].

***iv) Data Visualization Tool***

Data visualization tool allows the designer to plot the simulated data obtained from the device simulation tool. Synopsys Sentaurus$^{TM}$ TCAD includes Sentaurus Visual and Inspect for performing this task.

For a complete device simulation all the required tools are combined in a common environment such as Sentaurus Workbench which allows the designer to control, organize and analyze all the required steps.

## 5.2. GaN Material Physics Modeling

Most TCAD tools are initially developed for Si-based device simulation and in order to implement the wide bandgap semiconductor device such as the GaN, some of the material properties need to be modeled numerically to simulate the device. Most GaN transistors include GaN and AlN materials and their alloy $Al_mGa_{1-m}N$ with a specific mole fractions, represented by *m*. Thus, the material properties of GaN and AlN need to be included in the TCAD model and $Al_mGa_{1-m}N$ material properties are implemented by considering the mole

fraction dependence on the parameter values. The main parameters which need to be included in the TCAD simulator are band parameters, doping and ionization parameters, and mobility.

### 5.2.1. Band Parameters

GaN and AlN are group III-V nitride semiconductors which are direct bandgap semiconductors. Similar to most semiconductors, the energy bandgap, $E_g$ is a strong function of doping profile and temperature [95]. The effective energy bandgap is modeled by (5.1) and the parameters are listed in Table 5.1 [96]. The numerical temperature dependent intrinsic carrier concentration, $n_i$ and the density of states (DoS) of electrons in the conduction band, $N_c$ and the density of states of holes in the valence band, $N_v$ for GaN are modeled as shown below in (5.2) -(5.4) [95].

$$E_g(T) = E_g(0) - \alpha T^2/(T + \beta) \tag{5.1}$$

$$n_i = (N_C.N_V)^{1/2}\exp\left(-E_g/(2k_BT)\right) \tag{5.2}$$

$$N_C = 4.82 \times 10^{15}.(m_\Gamma/m_0)^{3/2}T^{3/2}\ cm^{-3} = 4.3 \times 10^{14} \times T^{3/2}\ cm^{-3} \tag{5.3}$$

$$N_V = 8.9 \times 10^{15} \times T^{3/2}\ cm^{-3} \tag{5.4}$$

TABLE 5.1
ENERGY BANDGAP PARAMETERS FOR GAN AND ALN [96]

| Parameter | AlN | GaN |
|---|---|---|
| $\alpha$ | $1.79\times10^{-3}$ eV/K | $9.1\times10^{-4}$ eV/K |
| $\beta$ | $1.462\times10^{3}$ K | 836 K |
| $E_g$ (0) | 6.23 eV | 3.507 eV |

### 5.2.2. Mobility

The carrier mobilities of GaN and AlN are adopted from the Masetti model for low-field operation as shown in (5.5) [91]. The temperature dependence is modeled using (5.6) and (5.7) and the fitting parameters are listed in Table 5.2. For high-field operation, the Canali model [91] is implemented with the fitting parameters shown in Table 5.3.

$$\mu_{dop} = \mu_{min1} exp\left(\frac{P_C}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{const}-\mu_{min2}}{1+\left(\frac{N_{A,0}+N_{D,0}}{C_r}\right)^{\alpha}} - \frac{\mu_I}{1+\left(\frac{C_S}{N_{A,0}+N_{D,0}}\right)^{\beta}} \tag{5.5}$$

$$\mu_0(E) = \frac{(\alpha+1)\mu_{low}}{\alpha+\left[1+\left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{5.6}$$

$$v_{sat} = v_{sat,0}\left(\frac{300\ K}{T}\right)^{v_{sat,exp}} \tag{5.7}$$

TABLE 5.2
COEFFICIENTS FOR THE MASETTI MODEL OF LOW-FIELD MOBILITY [91]

| Parameter | AlN | | GaN | |
|---|---|---|---|---|
| | Electrons | Holes | Electrons | Holes |
| $\alpha$ | 0.88 | 1.05 | 0.55 | 0.55 |
| $\beta$ | 0.75 | 0.75 | 0.75 | 0.7 |
| $\gamma_{\mu max}$ | 1 | 2.1 | 1 | 2.1 |
| $\mu_{const}$ | 300 $cm^2/(V.s)$ | 14 $cm^2/(V.s)$ | 1800 $cm^2/(V.s)$ | 20 $cm^2/(V.s)$ |
| $\mu_{min1}$ | 20 $cm^2/(V.s)$ | 11 $cm^2/(V.s)$ | 85 $cm^2/(V.s)$ | 33 $cm^2/(V.s)$ |
| $\mu_{min2}$ | 65 $cm^2/(V.s)$ | 0 $cm^2/(V.s)$ | 75 $cm^2/(V.s)$ | 0 $cm^2/(V.s)$ |
| $\mu_1$ | 20 $cm^2/(V.s)$ | 10 $cm^2/(V.s)$ | 50 $cm^2/(V.s)$ | 20 $cm^2/(V.s)$ |
| $P_C$ | $8\times10^{17}$ $cm^{-3}$ | $5\times10^{18}$ $cm^{-3}$ | $6.5\times10^{15}$ $cm^{-3}$ | $5\times10^{15}$ $cm^{-3}$ |
| $C_R$ | $7\times10^{16}$ $cm^{-3}$ | $8\times10^{17}$ $cm^{-3}$ | $9.5\times10^{16}$ $cm^{-3}$ | $8\times10^{16}$ $cm^{-3}$ |
| $C_S$ | $5.2\times10^{17}$ $cm^{-3}$ | $8\times10^{18}$ $cm^{-3}$ | $7.2\times10^{19}$ $cm^{-3}$ | $8\times10^{20}$ $cm^{-3}$ |

TABLE 5.3
COEFFICIENTS FOR THE CANALI MODEL OF HIGH-FIELD MOBILITY [91]

| Parameter | AlN | | GaN | |
|---|---|---|---|---|
| | Electrons | Holes | Electrons | Holes |
| $\alpha$ | 0.8554 | 0 | 0.7857 | 0 |
| $\beta$ | 17.3681 | 4 | 7.2044 | 4 |
| $\gamma_{beta}$ | 8.7253 | 0 | 6.1973 | 0 |
| $v_{sat,0}$ | $1.5\times10^7$ cm/s | $1.25\times10^7$ cm/s | $1.3\times10^7$ cm/s | $1.7\times10^7$ cm/s |
| $v_{sat,exp}$ | 2 | 2 | 0.7 | 0.725 |

### 5.2.3. Doping and Ionization

The impurities in most WBG semiconductors including GaN form deep energy level and thus would not be fully ionized even at high temperature [97]. The effective doping concentration is modeled using (5.8) -(5.10) where $N_{A,D}$ is the effective doping concentration, $N_{A,D0}$ is the implanted doping concentration, $E_f$ is the Fermi level, $E_{A,D}$ is the activation energy, $G_{A,D}$ is the degeneracy factor, and $N_{crit}$ is the maximum doping concentration beyond which the material loses its semiconducting properties. For the degeneracy factor for acceptor, $g_A$ a value of 4 is used for shallow acceptors and for donor degeneracy, $g_D$ a value of 2 is used for shallow donors [98].

$$N_{A,D} = \frac{N_{A,D0}}{\left(1+G_A\frac{E_{A,D}-E_F}{kT}\right)}, N_{A,D0} < N_{crit} \tag{5.8}$$

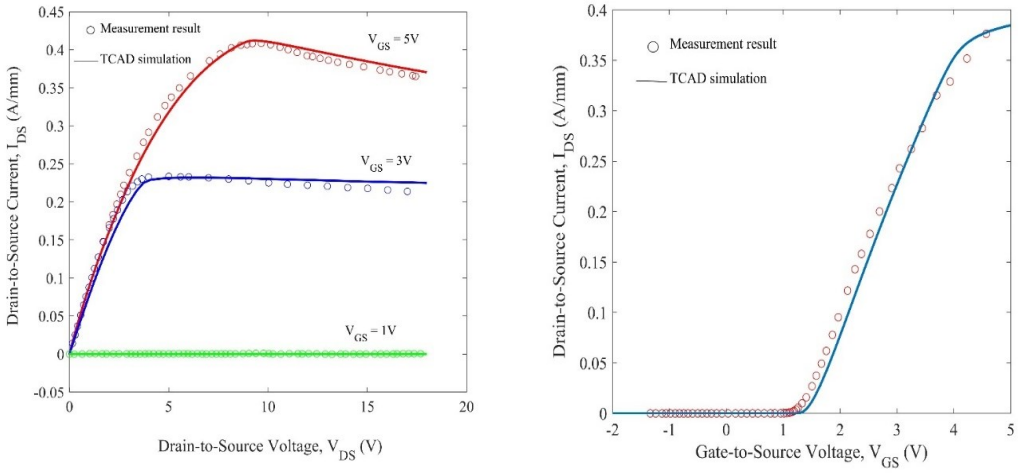
$$N_{A,D} = N_{A,D0}, N_{A,D0} > N_{crit} \tag{5.9}$$

$$G_{A,D}(T) = g_{A,D}exp\left(\frac{\Delta E_{A,D}}{kT}\right) \tag{5.10}$$

## 5.3. Device Simulation of the GaN GIT

An enhancement-mode AlGaN/GaN GIT device with *p*-type GaN gate and AlGaN buffer has been simulated using TCAD Sentaurus in which the same device structure as the analytical model has been used. Polarization charges at interfaces due to divergence of polarization vectors are computed automatically using the built-in strain piezoelectric polarization model. The simulated DC characteristics curves are compared with the actual measurement data in order to validate the numerical model. Figure 5.2 shows the TCAD simulation results along with the actual measurement results showing a very good match.

Once a general benchmark model is developed and validated, it can be adopted for further simulation with varying device parameters. The performance of any transistor depends on many parameters related to material, geometry and dopant concentration. Using a numerical

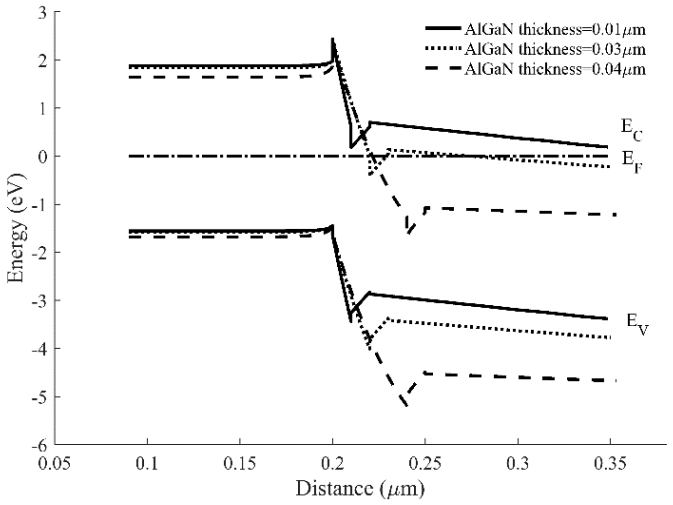



(a) (b)

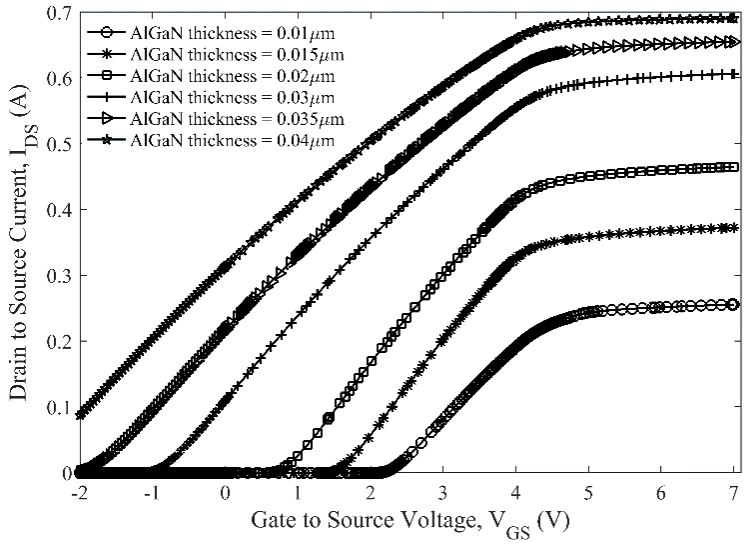
Figure 5.2: TCAD simulation results with the actual measurement result. (a) DC output characteristics with various gate biases and (b) transfer characteristics [99].

simulator, it is possible to predict the variation of the device behavior by varying these parameters. For example, the thickness and the doping concentration of AlGaN barrier layer have significant impact on the 2DEG electron concentration and on the channel transport characteristics of the GaN HEMT device [99]. TCAD Sentaurus simulation is performed by varying the thickness of the AlGaN layer from 10 nm to 40 nm and the band diagram and the device transfer characteristics for different thicknesses are shown in Figure 5.3. As the thickness of AlGaN is increased, the piezoelectric polarization is also increased resulting in an increase in the concentration of 2DEG. As shown in Figure 5.3 (a), the increase in 2DEG will pull the conduction band below the Fermi energy level. It will make the device operate in depletion-mode and as shown in Figure 5.3 (b) the threshold voltage becomes negative for AlGaN layer thickness higher than 30 nm.

TCAD Sentaurus simulation has also been performed by varying the doping concentration of the AlGaN layer from $10^{14}$ $cm^{-3}$ to $5\times10^{18}$ $cm^{-3}$ and the band diagram and the device transfer characteristics are shown in Figure 5.4. As the doping concentration of AlGaN is increased, the piezoelectric polarization is also increased which in turn increases the concentration of 2DEG. As shown in Figure 5.4 (a), the increase in 2DEG will pull the conduction band below the Fermi energy level. It will make the device to operate in depletion mode and as shown in Figure 5.4 (b) the threshold voltage becomes negative at AlGaN layer doping greater than $4\times10^{18}$ $cm^{-3}$.

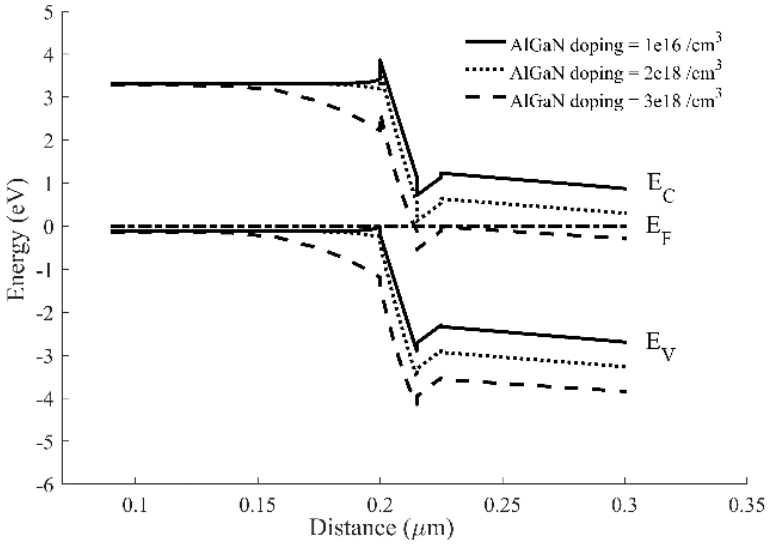



(a)

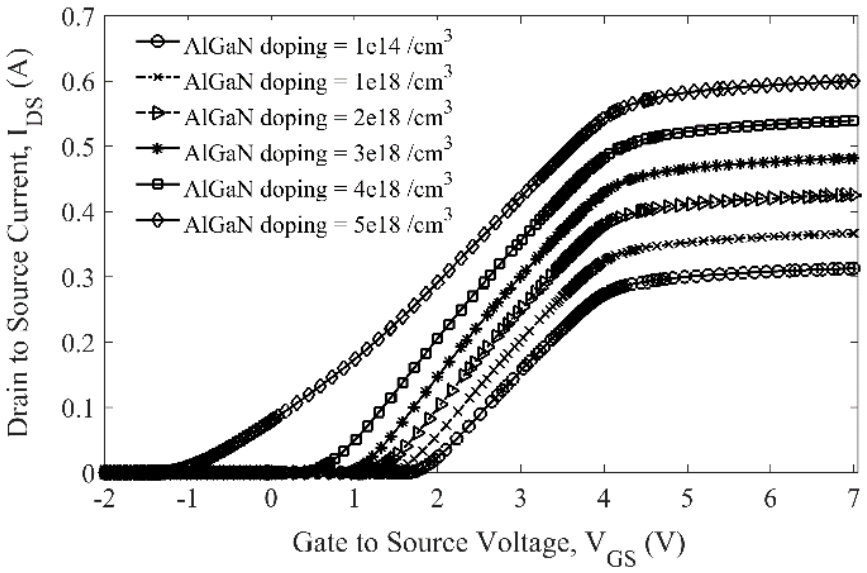



(b)

Figure 5.3: Impact of AlGaN thickness. (a) Band diagrams for different AlGaN thicknesses and (b) transfer characteristics for different AlGaN thicknesses [99].




(a)




(b)

Figure 5.4: Impact of AlGaN doping concentration. (a) Band diagrams for different AlGaN doping concentrations and (b) transfer characteristics for different AlGaN doping concentrations [99].

# Chapter 6

# Electrothermal SPICE Model

As high power density leads to the increased junction temperature, proper electrothermal modeling of the device is very important to simulate the device in a circuit simulator in order to verify its operation and improve the design efficiency for a specific power electronic application. In addition, it also allows a good estimation of power losses enabling the optimization of the system design such as thermal management and maximum allowable switching frequency. In this chapter, an electrothermal modeling approach for GaN HEMT is presented which can be implemented in the large signal SPICE simulation for any power electronic system.

## 6.1. Modeling Approach

Figure 6.1 shows the basic approach of the electrothermal model proposed in this work. It involves developing a temperature-dependent empirical device model for GaN power device. Commercially available GaN power transistors have been used to validate this model [100], [101]. The device characterization data at different temperatures are fitted to a MESFET-based empirical model to extract the model parameters. Next, a power loss model is developed to estimate the system power loss under a specific control strategy. This power consumed by the system is dissipated as heat thereby increasing the junction temperature of the device. Thus, the next step is to build a thermal model to obtain real-time junction temperatures of the device corresponding to the power losses. The equivalent thermal model

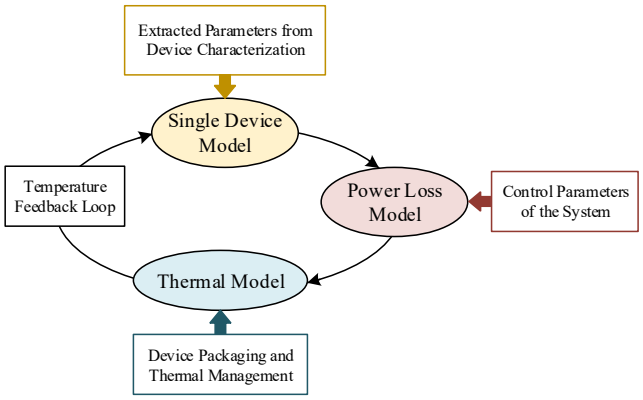



Figure 6.1: Electrothermal modeling approach for the GaN power HEMT.

parameters are significantly dependent on the packaging of the device and the thermal management of the designed system. Most common approach to achieve this is to use electrothermal analogy so that the model can be easily incorporated in electrical behavior of the device using electrical circuit components. This will allow the implementation of this model in common circuit simulators such as SPICE. For this purpose, RC thermal network can be used in which the resistances comprise the thermal resistance of the material and the capacitors contribute to the transient heat dissipation. From this description of the RC circuit it is possible to generate the temperature change as a function of time for a power loss model. This temperature is fed back to the single device models in order to update the device characteristics at elevated temperatures.

In addition, to achieve a device level temperature dependent model, it is also important to develop a model that can predict the power loss from a particular power electronic module depending on the system and the application. For high power system applications such as HEVs, the operating temperature depends on the overall power dissipation of the system. For

this reason, in this task, a power loss model will be developed to estimate the system power loss under a specific control strategy. This power loss model can be developed by analyzing the static and the dynamic characterization which will be performed in order to investigate the switching performance of the transistors to estimate the overall conduction and switching losses of the device. The lost power will be dissipated as heat thereby increasing the junction temperature of the device.

## 6.2. Thermal Model

The value of the corresponding resistors and capacitors in the RC thermal model can be determined by two approaches namely Cauer and Foster networks. Figure 6.2 shows these two RC networks generally used for the electrothermal model of power transistor [102]. The first approach or the Cauer RC network model involves simulating 3-D heat diffusion through different layers of device packaging with varying cross-sectional areas. This involves numerical simulation using solution techniques such as Finite Element Methods (FEM) or Finite Difference Methods (FDM). However, these approaches require intensive knowledge of the device structures with all the layers and material properties to perform thermal simulation by considering dense discretization meshes. Thus, to develop the Cauer model it is essential to know all the material properties and the exact device dimensions which are usually not available to the end users or for the commercialized device that the circuit designers use to develop the module. Therefore, for practical circuit and system design processes, model using Foster RC network is more effective and convenient. It is because Foster model is an empirically fitted model that considers the thermal characterization of the

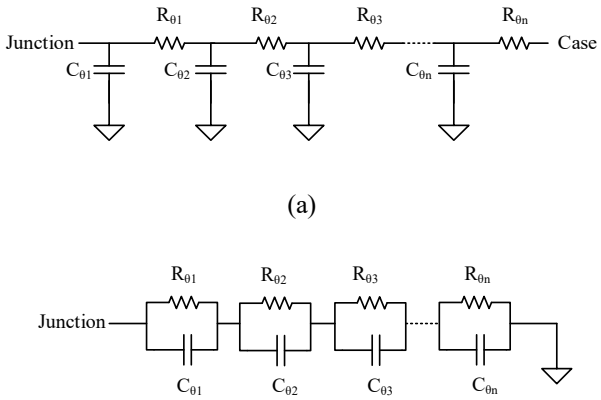



Figure 6.2: Two types of RC thermal model: (a) Cauer model and (b) Foster model.

device to generate the value of the circuit components. For this reason, in this work, Foster RC thermal network is developed from the device characterization data of thermal impedance.

For developing the Foster model, the first step is to obtain the transient characterization of the thermal impedance of the device. The transient thermal response of the power device is characterized by measuring the heat dissipation with time from the device junction to the case and from the case to the heat sink as shown in Figure 6.3. The basic principle of measuring the thermal impedance of a power device is described in [103]. For this purpose, a constant current flow is provided that generates a constant power to heat up the device to a steady-state temperature after a transient period of time. The device is then cooled down by turning off the current source and the transient cooling response is measured. The thermal impedance, $Z_{th}$ (t) as a function of time can be calculated by dividing the change in temperature between two time periods by the total applied power. As shown in Figure 6.3, the case and the heatsink temperatures can be measured conventionally by using

thermocouples. However, the junction of the device is not physically accessible to measure the junction temperature. For this reason, temperature dependent electrical characteristic of the device is used to measure the junction temperature. For most semiconductor devices, the current-voltage characteristic is a strong function of the operating temperature and by measuring the saturation voltage due to a specific reference current, the junction temperature of the device can be measured. Figure 6.4(a) shows the thermal impedance of the GaN device from Infineon$^{TM}$ and Figure 6.4(b) shows the thermal impedance of the GaN device from GaN System$^{TM}$ as a function of pulse width. The thermal impedance of power transistor is usually characterized by pulse power operation because the device is intended to be used as a switch subjected to a pulsed load. The transient response of the thermal impedance depends on the duration of the turn-on time or on the duty cycle of the applied pulse source. As shown in Figure 6.4, when the pulse duration is shorter for a specific duty cycle, the thermal impedance is lower due to low junction temperature for a short pulse period. As the pulse duration is increased, the transient thermal impedance tends to be equal to the steady state thermal resistance. As the duty cycle of the pulse power is increased, the slope of the transient response from the lowest thermal impedance to the maximum steady state value decreases.

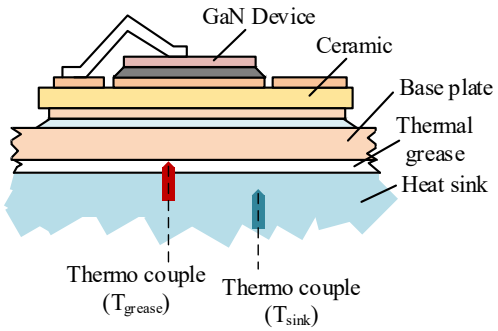
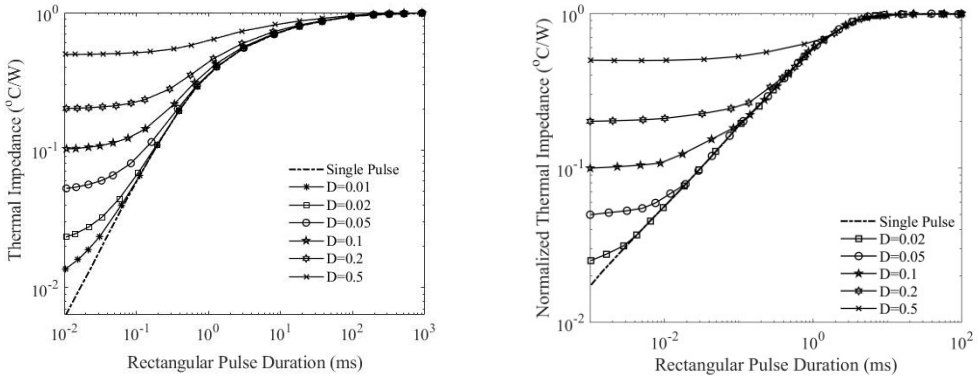



Figure 6.3: Cross-section of the GaN power device with thermal grease and heat sink [102].




(a) (b)

Figure 6.4: Transient thermal impedance as a function of duty cycle, D and pulse duration: (a) Infineon™ [100] and (b) GaN System™ [101].

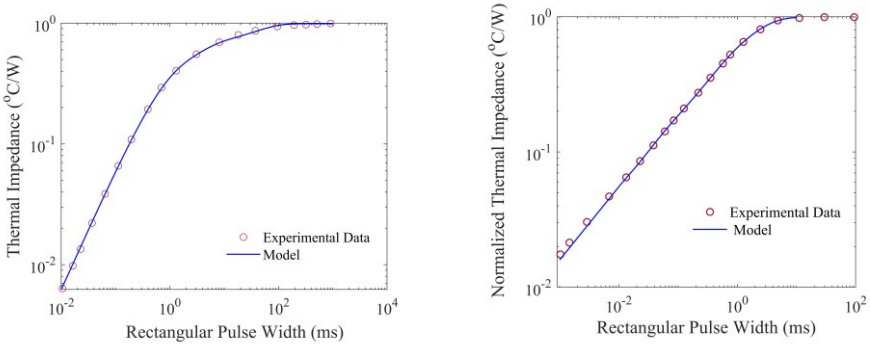
This is due to the fact that with higher duty cycle the pulse source is turned on for longer period of time providing less time to dissipate the heat compared to a short pulse.

The values of the resistors and the capacitors present in the RC Foster network are determined from the empirically fitting parameters. For the fitting parameter, the measured result for single short pulse is used because this provides the lowest duty factor allowing the junction to cool down completely between two consecutive pulse periods. In addition, for the proposed model three to four segments of RC network are used which provide very good approximation of the measured results. The steady state thermal impedance depends on the total resistance of the RC network considering all the capacitors to be open circuited when the period is high and the frequency is low. On the other hand, the value of the capacitors depends on the heat capacity or the time constant of the transient response. Thus, the transient thermal impedance is expressed by the following equation-

$$Z_{th}(t) = R_1\left(1 - e^{-\frac{t}{\tau_1}}\right) + R_2\left(1 - e^{-\frac{t}{\tau_2}}\right) + \cdots + R_n\left(1 - e^{-\frac{t}{\tau_n}}\right) \quad (6.1)$$

and thermal capacitance, $C_i = \frac{\tau_i}{R_i}$.

Figure 6.5 shows the fitted curves from the thermal model along with measurement data and Table 6.1 shows the determined resistor and capacitor values for the Infineon™ and GaN System™ GaN power devices.




(a) (b)

Figure 6.5: Transient thermal impedance curves from the model for single pulse: (a) Infineon™ [100] and (b) GaN System™ [101].

TABLE 6.1
THERMAL RESISTANCE AND CAPACITANCE VALUE FOR THE FOSTER THERMAL MODEL

| | Infineon™ | | GaN System™ | |
|---|---|---|---|---|
| Thermal Resistance (°C/W) | Parameter | Value | Parameter | Value |
| | R1 | 0.33 | R1 | 0.028 |
| | R2 | 0.33 | R2 | 0.607 |
| | R3 | 0.33 | R3 | 0.273 |
| | - | - | R4 | 0.079 |
| Thermal Capacitance (J/°C) | C1 | 0.1289 | C1 | $5.78\times10^{-5}$ |
| | C2 | 0.0103 | C2 | $3.29\times10^{-3}$ |
| | C3 | $1.917\times10^{-3}$ | C3 | $1.68\times10^{-3}$ |
| | - | - | C4 | $4.83\times10^{-4}$ |

## 6.3. Empirical SPICE Model

In order to simulate the GaN device in a power electronic module, it is important to develop a SPICE model for the transistor. The equivalent circuit model of the device is shown in

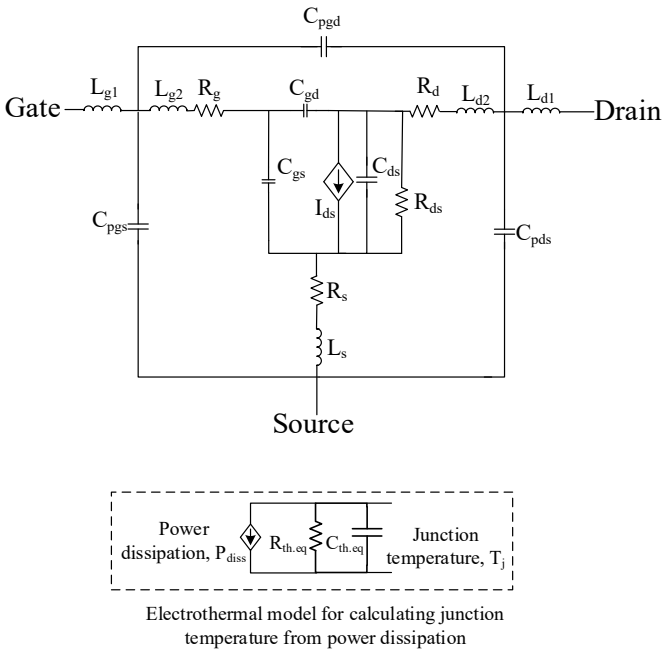



Figure 6.6: Empirical large signal model topology of the GaN HEMT with the electrothermal RC network.

Figure 6.6 which is based on Cree GaN HEMT model adopted from Fager-Statz's 13-Element MESFET model developed for high frequency application [104]. The core current-voltage model for the power transistor is developed from the analytical model described in Chapter 4. Other elements used in the model are derived from non-linear device characteristics as found in recent literatures [105], [106]. The parameters in the model equations are empirically fitted with the characterized data obtained for the particular transistor. In general, the SPICE model includes the following circuit components:

### *i) Drain-to-Source Current, $I_{ds}$*

The drain-to-source current of the device is implemented using a voltage dependent current source which is a function of the gate-to-source voltage, $V_{GS}$ and drain-to-source voltage,

$V_{DS}$. The drain current equation obtained from the analytical model has been implemented for this component.

***ii) Drain-to-Source Resistance, $R_{ds}$***

The drain-to-source resistance, $R_{ds}$ is also called the output resistance of the transistor which is obtained from the output characteristics ($I_{DS}$ vs $V_{DS}$) of the device. It is the reciprocal of the output conductance, $g_{ds}$ which is defined as the incremental change in the drain-to-source current with an incremental change in the drain-to-source voltage, as shown in (6.2).

$$\frac{1}{R_{ds}} = g_{ds} = \frac{I_{DS}}{V_{DS}}|_{V_{GS}} \tag{6.2}$$

***iii) Parasitic Resistances ($R_g$, $R_d$, $R_s$)***

The parasitic resistances $R_g$, $R_d$, $R_s$ are connected to each terminal such as the gate, the drain and the source, respectively, which account for the contact resistance due to the ohmic contacts at each terminal.

***iv) Parasitic Inductances ($L_g$, $L_d$, $L_s$)***

The parasitic inductances account for any inductance developed between the metal contact pads to the device surface. The parasitic inductance at each terminal is divided in two parts. The first part accounts for the inductances present inside the device between the metal contact pads and the second part accounts for the inductances present in the bonding wires and other parasitic package inductances.

***v) Capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$***

The capacitances $C_{gs}$ and $C_{gd}$ account for the change in the depletion charge with respect to the gate-to-source and gate-to-drain voltages, respectively. The drain-to-source capacitance,

$C_{ds}$ is included in the equivalent circuit to account for geometric capacitance effects between the source and the drain electrodes. These capacitors play a very important role to determine the switching performance of the device and are also dependent on the bias voltages. Besides there are three more parasitic capacitances such as the $C_{pgd}$, $C_{pds}$ and $C_{pgs}$ which account for any parasitic capacitance present in the device packages.

***vi) Thermal Model***

In addition, the SPICE model includes the electrothermal model and the temperature dependent device characteristics to obtain the operating temperature of the device for a specific operating condition.

## 6.4. Device Characterization

In order to extract different model parameters of the empirical SPICE model, the model equation needs to be fitted to the device characterization data. Thus, device characterization is an important part of the development of the empirical model. In this work, three different types of device characterization efforts have been performed such as the current-voltage (*I-V*) characterization, capacitance-voltage (*C-V*) characterization, and dynamic double pulse testing for switching parameters. The device used for the characterization is the commercially available GaN transistor GS66508B-E01-MR produced by GaN system [101].

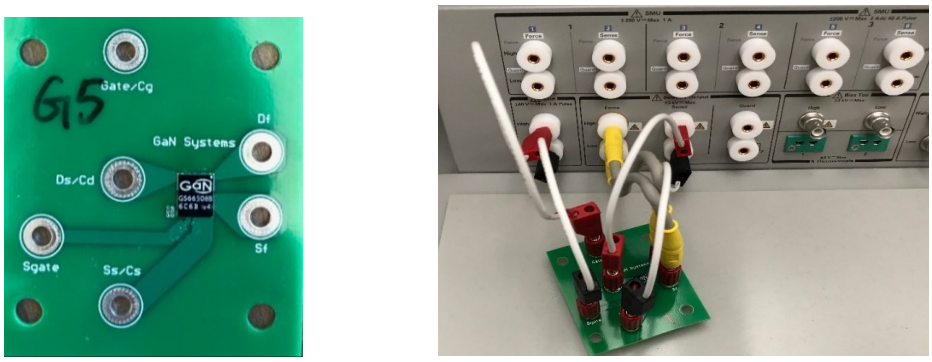
### 6.4.1. Current-Voltage (*I-V*) Characterization

The device used for the characterization is a surface mounted device which is adapted to PCB board for characterization as shown in Figure 6.7 and the *I-V* characterization is

performed using Keysight B1505A curve tracer. The *I-V* characterization includes measurement of the device drain-to-source current, $I_{DS}$ either by sweeping the gate-to-source voltage, $V_{GS}$ or by sweeping the drain-to-source voltage, $V_{DS}$ while keeping other bias to a constant value. In addition, the reverse conduction characteristic is obtained by measuring the drain current of the device with varying drain voltage in the negative polarity. This characterization is important because the GaN HEMT under study is a lateral device where the source and the drain terminals are not symmetric with respect to the gate unlike conventional MOSFETs. In addition, the leakage characterization is performed by measuring $I_{DS}$ as a function of $V_{DS}$ when $V_{GS}$ is set below the threshold voltage so that the device is in the off state. Therefore, the characterization operation provides the following sets of characteristics such as-

i) Transfer characteristic which provides $I_{DS}$ as a function of $V_{GS}$ at a constant $V_{DS}$.

Figure 6.8 shows the transfer characteristic of the device where the gate-to-source voltage, $V_{GS}$ is swept from 0 to 5 V with a linear step of 200 mV. The drain voltage is selected to be




(a) (b)

Figure 6.7: Experimental setup for the current-voltage characterizations. (a) Adaptor board for surface mounted device and (b) *I-V* test connections.

6 V which is sufficient to keep the device in saturation for the range of the gate voltage sweep. It can be concluded from the transfer characteristic that the enhancement-mode device has a threshold voltage of about 1.3 V.

ii) Output characteristics which provide $I_{DS}$ as a function of $V_{DS}$ at different set of $V_{GS}$.

The output characteristics of the GaN transistor are shown in Figure 6.9 where the drain-to-source voltage, $V_{DS}$ is swept from 0 to 15 V with a linear step of 200 mV for different values of the gate-to-source voltage, $V_{GS}$ from 0 to 5 V with a linear step of 1 V.

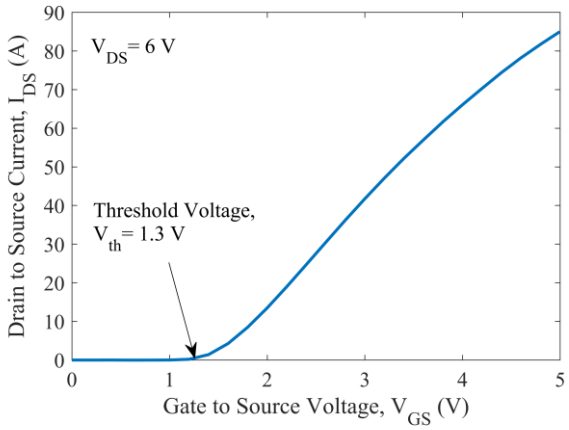



Figure 6.8: Transfer characteristic of the GaN transistor with $V_{DS}$ = 6 V.

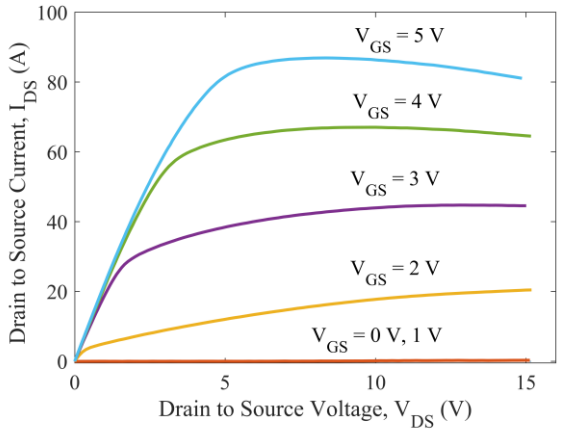



Figure 6.9: Output characteristics of the GaN transistor.

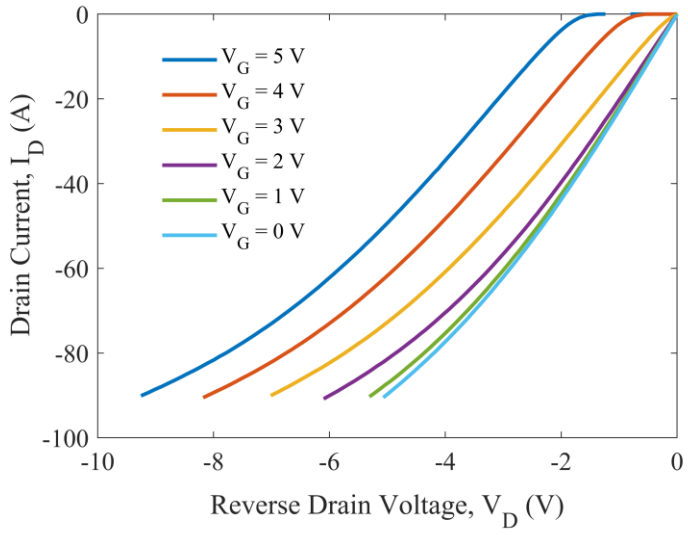



Figure 6.10: Reverse conduction characteristics of the GaN transistor.

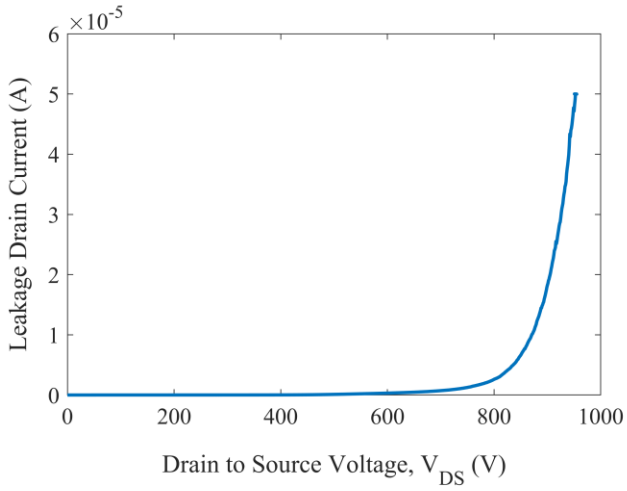



Figure 6.11: Leakage current characteristic of the GaN transistor with $V_{GS}$ = 0 V.

iii) Reverse conduction characteristics which provides $I_{ds}$ as a function of reverse drain-to-source voltage or $V_{SD}$ at different set of $V_G$.

Figure 6.10 shows the reverse conduction characteristics of the transistor where the drain-to-source voltage, $V_{DS}$ is swept from -15 to 0 V with a linear step of 200 mV for different values of the gate-to-source voltage, $V_{GS}$ from 0 to 5 V with a linear step of 1 V.

iv) Leakage characteristic which provides $I_{DS}$ as a function of $V_{DS}$ when $V_{GS} < V_{th}$.

To determine the leakage current of the device, the gate voltage is kept at 0 V to turn the device off and the drain voltage was swept until the leakage current threshold of 50 µA was reached. Figure 6.11 shows the leakage characterization of the device.

### 6.4.2. Capacitance-Voltage (*C-V*) Characterization

The capacitance-voltage characterization is performed to determine the junction capacitances such as the $C_{gs}$, $C_{ds}$ and $C_{gd}$. However, these capacitances are obtained in terms of input capacitance, $C_{iss}$, output capacitance, $C_{oss}$ and reverse transfer capacitance, $C_{rss}$. The input capacitance, $C_{iss}$ is measured by shorting the drain terminal to the ground where output capacitance, $C_{oss}$ is measured by shorting the gate terminal to the ground. The reverse transfer capacitance, $C_{rss}$ is measured in between the gate and the drain terminals.

$$C_{iss} = C_{gd} + C_{gs} \tag{6.3}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{6.4}$$

$$C_{rss} = C_{gd} \tag{6.5}$$

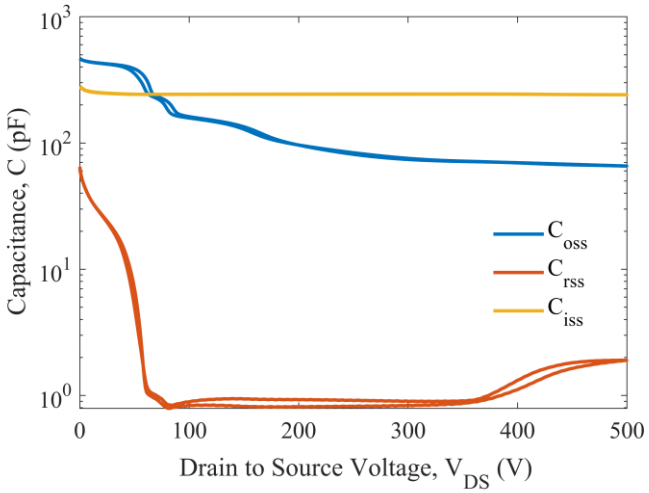



Figure 6.12: $C_{oss}$, $C_{iss}$ and $C_{rss}$ as functions of $V_{DS}$.

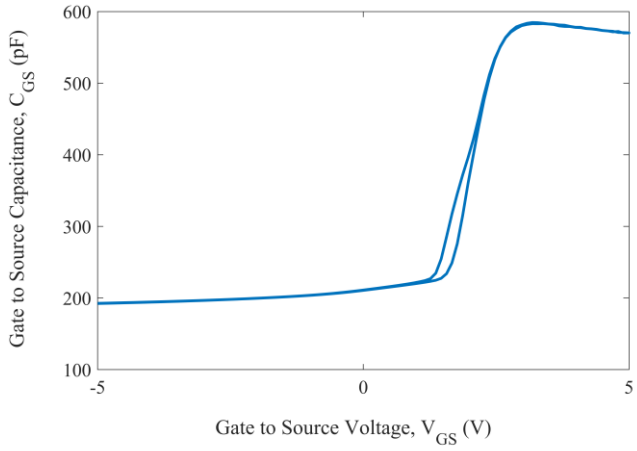



Figure 6.13: Gate-to-source capacitance, $C_{GS}$ as a function of $V_{GS}$.

Figure 6.12 shows the three capacitances $C_{oss}$, $C_{iss}$ and $C_{rss}$ as function of $V_{DS}$ where $C_{oss}$ and $C_{rss}$ vary significantly with $V_{DS}$. However, the input capacitance $C_{iss}$ includes the gate-to-source capacitance which does not change significantly with $V_{DS}$ but is a strong function of $V_{GS}$ as shown in Figure 6.13.

### 6.4.3. Dynamic Characterization by Double Pulse Testing

The static *I-V* and *C-V* characterizations provide some of the key components present in the device model. In addition, dynamic characterization needs to be performed to study the switching characteristics such as the turn-on and turn-off time and *dV/dt* capabilities. The standard method of determining these parameters is to perform a double pulse testing (DPT) in which a two consecutive pulse is used to observe the turn-on and turn-off mechanisms of the device under test. In this testing, an inductor is used to replicate the circuit conditions in a converter design. An arbitrary function generator is used to output pulses that trigger the gate of the transistor and the turn-off characteristics are measured at the end of the first pulse and the turn-on characteristics are measured in the beginning of the second pulse.

The methodology for the dynamic characterization of wide bandgap devices has been developed by Zhang *et al.* at the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT) in the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville [107]. Figure 6.14 shows the DPT board which includes the DC bus power supply, bulky capacitors for energy storage, solid-state circuit breaker (SSCB) board for protection, load inductor, gate drive circuits, devices under test, auxiliary power supply, and the measurement probes like coaxial shunt [107]. Figure 6.15 shows the output voltage of the gate driver integrated circuit (IC) which

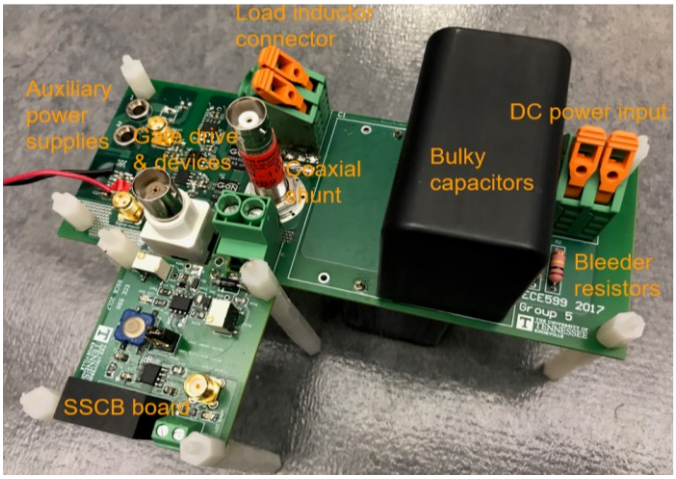



Figure 6.14: Double pulse test board [107].

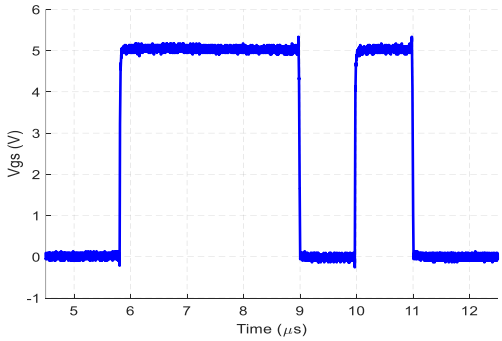
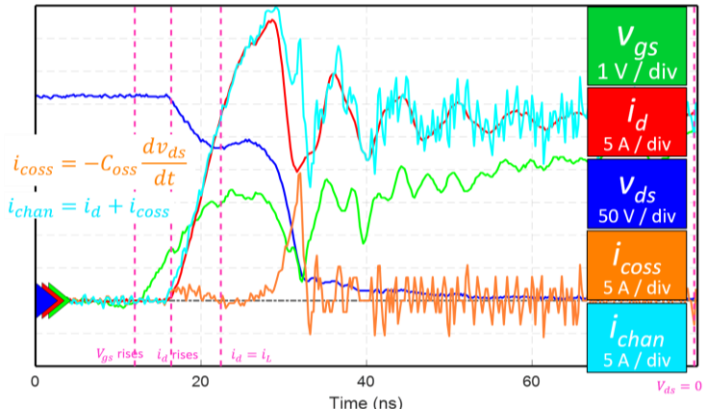
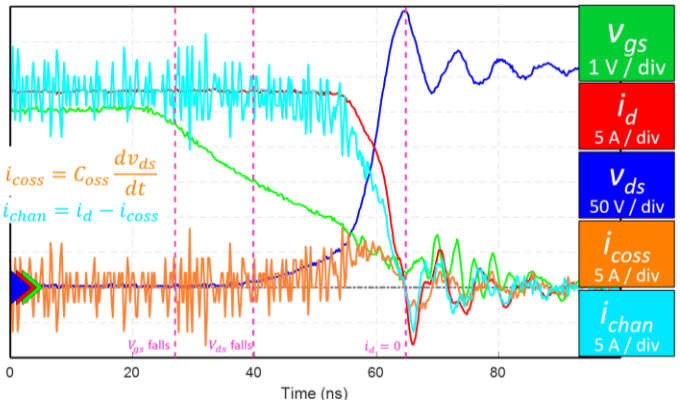



Figure 6.15: Complete double pulse of the gate driver output.

generates the two consecutive pulses for this test. Figure 6.16 shows the turn-on and turn-off waveforms for the condition of $V_{DC}$ = 300 V, $I_L$ = 30 A, and $R_{on} = R_{off}$ = 20 Ω. This figure includes the gate-to-source voltage, the drain current, and the drain-to-source voltage. In addition, the channel current and the current flowing through the output capacitance are estimated and pink vertical lines are labeled to separate different periods during turn-on and turn-off switching conditions. Table 6.2 lists the key switching parameters extracted from the DPT of the GaN transistor.




(a)




(b)

Figure 6.16: Turn-on and turn-off waveforms at $V_{DC}$ = 300 V, $I_L$ = 30 A, $R_{on} = R_{off}$ = 20 Ω. (a) Turn-on transient and (b) turn-off transient.

TABLE 6.2
KEY SWITCHING PARAMETERS EXTRACTED FROM THE DPT OF THE GAN TRANSISTOR

| Key Parameters | Measurement |
|---|---|
| Turn-on time, $t_{on}$ | 20 ns |
| Turn-off time, $t_{off}$ | 15.2 ns |
| Turn-on Energy Loss, $E_{on}$ | 66.5 µJ |
| Turn-off Energy Loss, $E_{off}$ | 19.3 µJ |
| Total Energy Loss, $E_{tot}$ | 85.8 µJ |
| Peak dv/dt during turn-on | -121.6 V/ns |
| Peak dv/dt during turn-off | 110 V/ns |

## 6.5. Simulation of a DC-DC Boost Converter

The empirical SPICE model developed in this work is used to simulate a DC-DC boost converter with an input of 200 V to a boosted output of 400 V. Figure 6.17 shows the circuit diagram of the DC-DC boost converter in which operating switching frequency at the gate pulse is 50 kHz. As shown in this figure, the device model also provides two additional terminals, TJ and TC for the junction and case temperatures, respectively. The case temperature is fixed to the ambient temperature of $25^0$C which is implemented by adding a 25 V voltage source at the TC node. The $R_{THCA}$ is the thermal capacitance of the case and a value of 10 $^0$C/W is used for this parameter. Figure 6.18 shows the output of the converter for 60 ms and the junction and the case temperatures are shown in Figure 6.19. The turn-on and the turn-off switching transients are shown in Figure 6.20, which also shows the junction and the case temperatures during the switching transients.

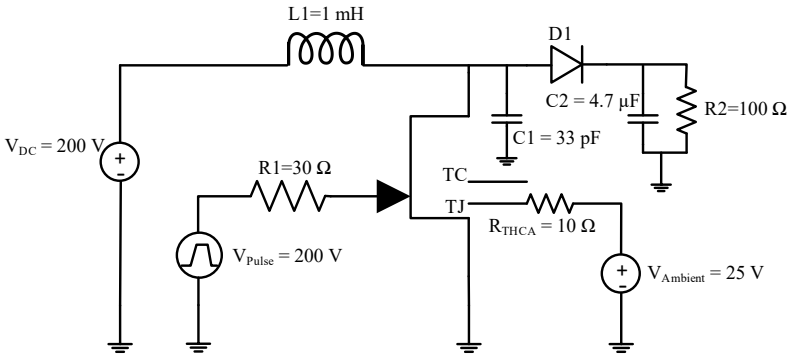



Figure 6.17: Circuit diagram of the DC-DC boost converter.

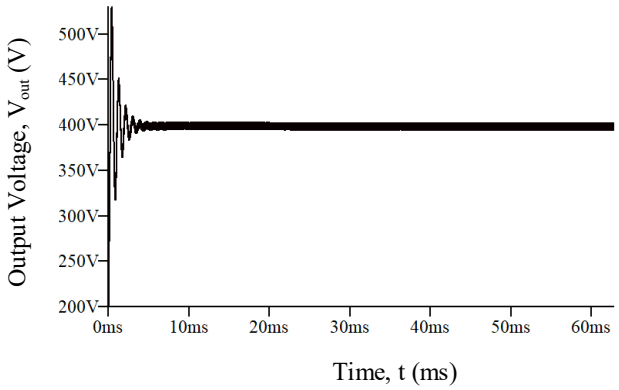



Figure 6.18: Output voltage of the DC-DC boost converter.

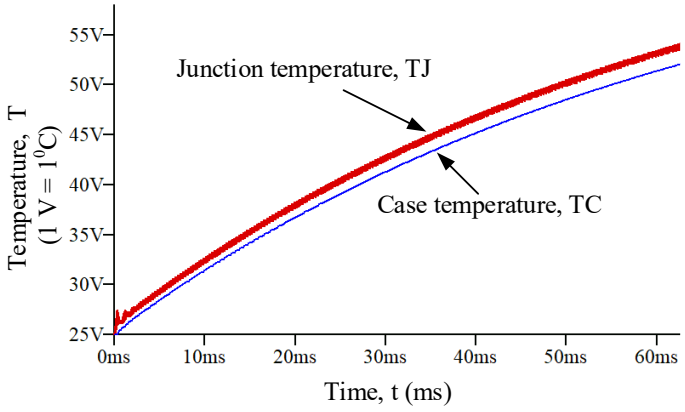
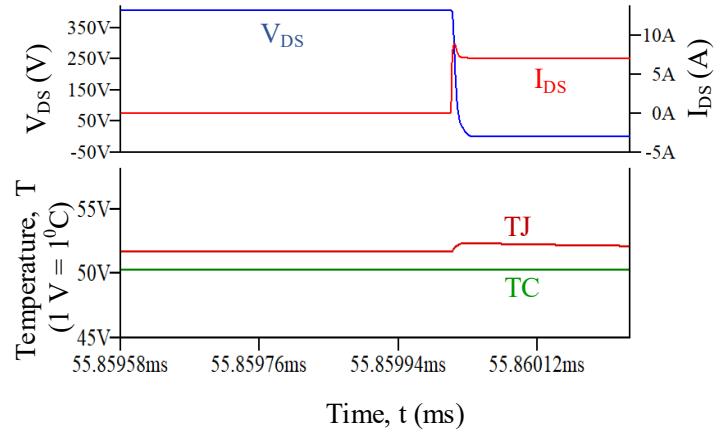
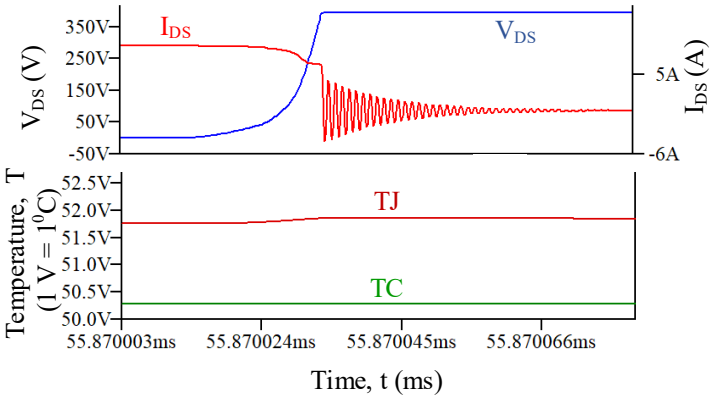



Figure 6.19: Junction (TJ) and case (TC) temperature from the thermal simulation of the DC-DC boost converter.




(a)




(b)

Figure 6.20: Switching transients with the junction and case temperature. (a) Turn-on transient and (b) turn-off transient.

# Chapter 7

# Conclusion

## 7.1. Summary

This research project is focused on modeling of GaN HEMT has been performed for high power and high temperature applications. The main research tasks include study of the device physics underlining the operation of the GaN transistors, development of an analytical model and validation of the model with numerical simulation and experimental measurement results. In addition, TCAD simulation platform for this new type of devices has been developed. With the help of the numerical device simulators such as TCAD Sentaurus, the performance of the device was studied more extensively by varying the device parameters. As the application for this work is associated with high power electronic modules, it is also very important to study the device performance at elevated temperatures. In this regard, this research also includes an approach to build an electrothermal model for GaN power devices that enables estimation of the increase in junction temperature based on the power dissipation of the electronic modules employing the GaN power devices. The proposed electrothermal model is built for standard SPICE simulators which will allow the circuit designer to optimize the system level design based on the device performance at high temperature.

## 7.2. Original Contributions

The original contribution can be summarized as follows:

1) A physics-based model for an enhancement-mode *n*-channel GaN-GIT device for high power and high temperature application has been developed. The positive threshold voltage obtained by the *p*-doped gate is modeled by considering the impact of the built-in potential on the 2DEG channel of the transistor. In addition, parallel conduction on the barrier layer of the device due to the carrier spill-over at higher gate bias has been considered. As the power devices are expected to operate at elevated temperatures, high temperature performance of the transistor is also modeled in this work. The model shows an excellent match with the experimentally measured data.

2) The simulation of the GaN-GIT device has been performed using TCAD Sentaurus. Device characteristics predicted from the analytical model have been verified by comparing with the TCAD simulated data. In addition, using the TCAD Sentaurus, impact of different parameters such as the doping concentration and layer thickness on the device characteristics has also been studied.

3) An electrothermal SPICE model of GaN HEMT is developed to simulate the device for power electronic applications. This model can predict the operating temperature due to the power dissipation of a power electronic module. This model can be used to achieve a quick solution to achieve a good estimation of power losses enabling the optimization of the system design such as the thermal management and control parameters.

## 7.3. Future Research Direction

Modeling Scopes:

- The proposed analytical model only considers one particular type of GaN transistor which is an *n*-channel GaN-GIT. In future, other types of device structures can be studied following the same procedure. In particular, the recessed-gate GaN HEMT structure is also a popular structure for enhancement-mode GaN power device and a combination of recessed and a *p*-doped gates for better performance has been studied by a few research works predicting better device performance [42].

Simulation Scopes:

- COMSOL Multiphysics simulation can be performed to model the heat dissipation through the device and to model the channel temperature of the transistor.
- Sentaurus device simulator can be used further to vary other device parameters and geometries and can be linked with the analytical model.

Experimental and System Level Scopes:

- Additional device testing can be performed to validate the model, particularly at elevated temperatures.
- The proposed model can be adopted in design of a power system module such as a converter or inverter module. Test result from this power electronic module employing commercial GaN transistor can be used to validate the results obtained from SPICE circuit simulation using the proposed model.

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