# Thermal and electrical stability assessment of AlGaN/GaN Metal-Oxide-Semiconductor High Electron Mobility Transistors (MOS-HEMT) with $HfO_2$ gate dielectric

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***Abstract*—AlGaN/GaN HEMTs and MOS-HEMTs using $HfO_2$ as gate dielectric have been analyzed at room temperature, after STA and TC test, during off-state electrical step stress, HTRB and PBTI tests. Results showed that the leakage current in as-fabricated MOS-HEMTs decreased by $10^6$ and the on/off ratio increased by over $10^4$ than the HEMTs. Moreover, it was even higher after a STA test, up to $10^8$, in the MOS-HEMTs, and the surface trapping effects were mitigated, especially if a KOH cleaning was used before $HfO_2$ deposition. The MOS-HEMTs also showed higher electrical stability after off-state step electrical stress, HTRB and PBTI tests.**

***Index Terms*—AlGaN/GaN, HEMTs, $HfO_2$, MOS-HEMTs, surface cleaning, electrical stress.**

## I. Motivation and Objectives

GaN based high electron mobility transistors (HEMTs) have drawn great attention due to their potential in high temperature (HT), high power and high frequency applications [1]. However, high gate leakage current and current collapse are still some of the most critical problems limiting the performance and reliability of the devices [2, 3]. MOS-HEMTs using gate insulators such as, $SiO_2$, $Al_2O_3$, $HfO_2$, $Gd_2O_3$, $Y_2O_3$ have been studied to solve this problem [3, 4]. In particular, $HfO_2$, with electron affinity of 1.75-2.0 eV [5], band gap of 5.3 eV [6], was proven to be effective in reducing leakage current in Si, GaAs and GaN based MOS devices [7]. Although some authors do not use any particular treatment before dielectric deposition [8, 9], the use of a surface treatment, such as KOH, was shown to be effective in reducing the gate leakage in different GaN-based devices [10, 11]. However, further investigation on electrical stability and interface properties of high-$\kappa$/GaN structures is still needed to achieve reliable and competitive AlGaN/GaN-based devices for RF and power applications.

In this work, AlGaN/GaN MOS-HEMTs and MOS diodes (MOSD) with $HfO_2$ as gate dielectric and an optimized KOH-based surface treatment was assessed at room temperature (RT) and after various thermal and electrical stress tests, in order to compare their degradation mechanisms with the HEMTs and those MOS-HEMTs with only organics cleaning prior to $HfO_2$ deposition.

## II. Experimental Details

The devices were fabricated on AlGaN/GaN heterostructures with a GaN cap (2 nm) grown on Si(111) by metal-organic chemical vapor deposition. The Al content and the thickness of the AlGaN layer is 31% and 22 nm, respectively. The GaN layer (0.6 µm) is unintentionally doped. A schematic cross section of the devices is shown in Fig. 1. Both HEMTs and diodes were processed simultaneously on the wafer as follows.

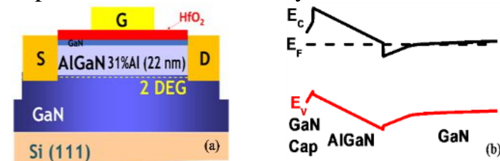


Fig. 1. (a) Schematic cross-section and (b) the corresponding energy band diagram of the heterostructure.

First, ohmic contacts were defined using a Ti/Al/Ni/Au (20/120/40/50 nm) metal stack, evaporated by e-beam and rapid-annealed at 850ºC for 30 s in $N_2$ ambient. Afterwards, mesa etching device isolation (100 nm depth) was carried out by inductively coupled plasma etching using $Cl_2$/Ar based process. The contact resistance ($R_c$) of the ohmic contacts was 0.75 Ω·mm and the sheet resistance ($R_{sheet}$) of the 2-dimensional electron gas was 420 Ω/□, as calculated by means of the transmission line method. The sheet carrier density ($n_s$) and the electron mobility (μ) of the devices calculated from Hall measurements were $0.7\times10^{13}$ $cm^{-2}$ and 1016 $cm^2$/V·s, respectively.

The wafer was divided into three pieces, one of them (named “Control”) was used as a reference for HEMTs processing. The other two pieces were used to process

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MOS-HEMTs with $HfO_2$ films (5 nm thickness).

Prior to $HfO_2$ deposition, one sample (named "Org") was cleaned only with organics solvents: acetone (5 min), methanol (5 min) and rinsed with deionized water, and the other (named "KOH") was cleaned with an optimized cleaning with KOH (0.5 M) for 20 s after organics. $HfO_2$ was deposited in an ALD reactor at 200°C using Hf based precursors and $H_2O$, by Ctechnano Coating Technologies [12].

Subsequently, all the samples were gate patterned using standard photolithography. Metallization of the gate contact Ni/Au (20/200 nm) and lift-off were performed. The gates (G) of the HEMTs are 1.2 µm in length and 50 µm in width, and the distance between source (S) and drain (D) is 5 µm, with the same S-G and G-D distances. The diodes have square shapes with a side length of 100 µm.

Finally, the Ti/Au feed metallization was defined with the dielectric layer on top of ohmic metal previously etched using diluted HF:$H_2O$ (1:10) for 5 minutes.

Some of the HEMTs and MOS-HEMTs were used to analyze the thermal stability after a short thermal annealing (STA) at 400ºC for 10 min and a thermal cycle (TC) test from 25ºC to 325ºC with a step of 100ºC. Current-voltage (I-V) measurements at RT before and after STA, and at each step during TC test were taken.

Another set of devices was used to test the device robustness after electrical stresses including: an off-state electrical stress, a HT reverse bias (HTRB) test and a positive bias temperature instability (PBTI) test. The off-state electrical stress consisted of a long-term drain-bias step stress at RT, keeping the gate source voltage ($V_{GS}$) at -7 V (off-state), and sweeping the drain source voltage ($V_{DS}$) from 13 V to 39 V, with a 2 V step for 1800 s at each step. The HTRB test was taken with $V_{DS}$= 23 V and $V_{GS}$ = -7 V during 120 hours with a base plate T of 125ºC. The PBTI test was series of stress sections with increasing stress time from 200 s to 1000 s. During stress, the devices were subject to a positive gate stress from 0.6 V to 1.4 V while the S and D grounded. The same electrical measurements were systematically monitored before and right after each stress step, in order to assess the devices stabilities.

## III. RESULTS AND DISCUSSION

### A. As fabricated devices

I-V characteristics of the AlGaN/GaN Schottky diodes (SD) and $HfO_2$ MOSD are shown in Fig. 2(a). Results show that the reverse gate current ($I_{rev}$) of MOSD is about $10^4$ lower than the SD, regardless of cleaning procedure. However, the lowest forward current ($I_{for}$) is observed in the MOSD (KOH), about $10^6$ lower than SD, and 10 times lower than MOSD (Org). Schottky barrier height was close to 1.0 eV for the SD, and the ideality factor was about 2.0±0.6, extracted from the forward I-V curve, close to the results shown in the literatures [13], [14].

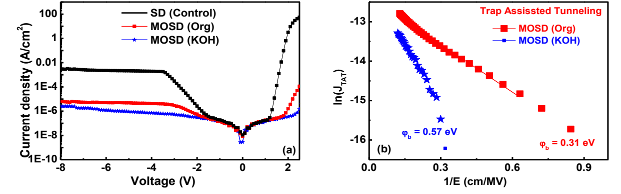


Fig. 2. (a) Gate leakage current and (b) TAT fitting plots of $HfO_2$ based MOSD and SD.

In addition, the electron transport mechanisms were analyzed in both devices using the techniques discussed in [15], [16]. For the SD, Schottky emission (SE) fit well with the experimental I-V curves, which means the dominant electron transport mechanism was SE, and for the MOSDs (Org and KOH), trap assisted tunneling (TAT) fit well with the experimental results, indicating TAT in the oxide layer is the dominate electron transport mechanism, and the activation energy was calculated to be 0.31 eV (at $V_G$ = 1 V to 2.8 V) and 0.57 eV (at $V_G$ = 1.2 V to 2.5 V), respectively, as shown in Fig. 2(b).

The energy level at 0.31 eV is likely due to carbon substituting N($C_N$) [17]. The deep traps with activation energy level of 0.57 eV are often observed at GaN side of the AlGaN/GaN interface [18–20]. Interestingly, the carbon related traps were not observed in the MOSD (KOH), proving that the KOH cleaning could remove the C on the GaN surface effectively [21].

The capacitance-voltage (C-V) curves and the carrier density ($n_s$) of the diodes are shown in Fig. 3(a). From the MOSD, the dielectric constant of the $HfO_2$ is about 15, in agreement with the literature [22]. Neither hysteresis nor frequency dispersion were observed in SD or MOSDs. No threshold voltage shift ($\Delta V_{th}$) was observed in MOSD (KOH) with respect to the SD, however, $\Delta V_{th}$ about +0.4 V was observed in MOSD (Org), possibly due to negative fixed oxide charges at the oxide/heterostructure interface [23, 24].

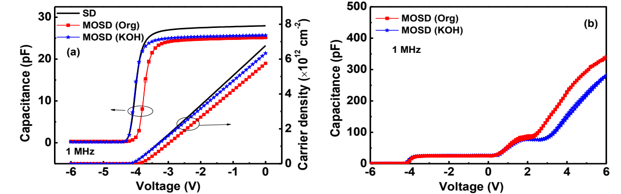


Fig. 3. (a) C-V and carrier density characteristics of SD and MOSDs and (b) C-V curves the MOSDs at the -6 V to 6 V range.

In order to further study the $HfO_2$ dielectric and $HfO_2$/GaN interface, MOSDs were swept from -6 to 6 V (Fig. 3(b)). When positive gate bias was applied, electrons accumulated at the AlGaN layer, leading to dielectric capacitance ($C_{HfO2}$). An extra step (at ~1 V) is observed in this region, which could be related to trapping centers at the $HfO_2$/GaN interface, possibly due to lack of post-deposition annealing [25]. The interface state density ($D_{it}$) as a function of energy level can be

calculated using conductance method [26]. The equivalent parallel conductance ($\frac{G_p}{\omega}$) can be calculated from the experimental measurements:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_b^2}{G_m^2+\omega^2(C_b-C_m)^2}, \qquad (1)$$

where $\omega = 2\pi f$, $f$, $G_m$ and $C_m$ are measurement frequency, measured conductance and capacitance and $C_b$ is the static state capacitance.

On the other hand, $\frac{G_p}{\omega}$ is given as:

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it} D_{it}}{1+(\omega\tau_{it})^2} \qquad (2)$$

where $\tau_{it}$ is the trap time constant. By fitting the experimental $\frac{G_p}{\omega}$ curves with Eq. 2, $D_{it}$ can be achieved. The results are shown in Fig. 4 (a). The traps located at energy level of 0.56±0.01 eV in MOSD (KOH), 0.31±0.02 eV in MOSD (Org), in the range of 0.31-0.45 eV in SD.

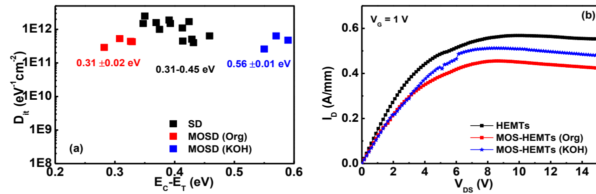


Fig. 4. (a) $D_{it}$ as a function of energy level for the diodes and (b) $I_D$-$V_{DS}$ curves of HEMTs and MOS-HEMTs.

I-V characteristics of the (MOS-)HEMTs are shown in Fig. 4(b). The MOS-HEMTs showed decreased maximum drain current ($I_{D,max}$): by -10% (Org) and -16% (KOH), and increased ON resistance ($R_{ON}$): by 11% (Org) and 9% (KOH), compared with the HEMTs. Also, the maximum transconductance ($g_{m,max}$) decreased by -3% in the MOS-HEMTs (Org and KOH) (Fig. 5(a)). Similar to MOSDs, no $V_{th}$ shift ($\Delta V_{th}$) was observed in MOS-HEMTs (KOH), and +0.1 V shift in MOS-HEMTs (Org).

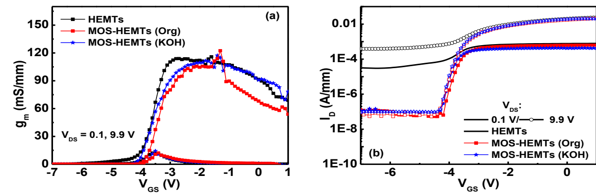


Fig. 5. (a) $g_m$-$V_{GS}$ and (b) $I_D$-$V_{GS}$ curves of the MOS-HEMTs and HEMTs at $V_{DS}$ = 0.1 V, 9.9 V.

In addition, regardless of cleaning technique, the MOS-HEMTs showed $I_{D,OFF}$ ($V_G$=-7 V) smaller than 0.1 μA/mm and on/off ratio $10^7$, $10^4$ times higher than the HEMTs (Fig. 5(b)). These results show that MOS-HEMTs using $HfO_2$ can reduce both drain and gate leakage currents.

### *B. Thermal Stability*

#### *1) Short Thermal Annealing Test (STA)*

I-V characteristics of the SDs and MOSDs before and after the STA are shown in Fig. 6(a). After the STA, MOSD (KOH) showed the lowest $I_{rev}$ and $I_{for}$, about 1 μA/cm² ($V_G$ = -8 V) and 1 mA/cm² ($V_G$ = 3 V). $I_{rev}$ decreased after STA, by $10^2$ in SD, and by 10 times in MOSDs, regardless of cleaning procedure. $I_{for}$ increased slightly in the diodes.

The main electron transport mechanism in the MOSD (KOH) is still TAT after the STA, but with shallow vacancies with activation energy of 0.18 eV (at $V_G$ = 0.8 V to 2 V) (Fig. 6(b)). According to literature, this trap center at energy level in the range 0.17-0.24 eV could be related to linear line defects due to the dangling bonds along dislocation cores [27]. In the case of the MOSD (Org), the activation energy is about 0.38 eV (at $V_G$ = 1 V to 2.5 V) and it is likely due to $HfO_2$/GaN interface traps on the oxide side [28].

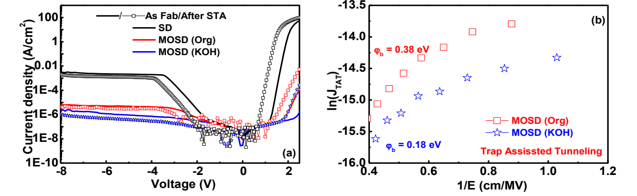


Fig. 6. (a) Gate leakage current of SD and MOSDs and (b) TAT fitting plots of MOSDs after STA.

The C-V characteristics and the $n_s$ of the diodes before and after the STA are shown in Fig. 7(a). SD and MOSD (KOH) showed a more positive $V_{th}$ shift (+0.2 V) than the MOSD (Org) (+0.02 V). This could be explained by the traps at AlGaN/GaN interface with activation energy of 0.57 eV, which were de-trapped after the STA, causing the positive $V_{th}$ shift.

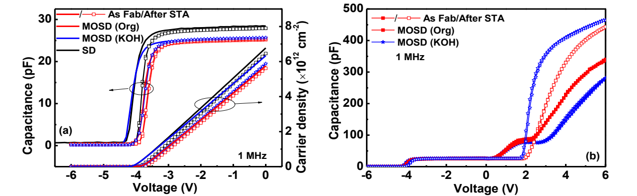


Fig. 7. (a) C-V and $n_s$ characteristics of SD and MOSDs and (b) positive sweep of the MOSDs before and after STA.

The C-V curves of the MOSDs (KOH) during positive sweep in Fig. 7(b) showed that the extra step, assigning to trapping centers at the $HfO_2$/GaN interface, is vanished after the STA, as expected. Interface density as a function of energy level calculated using the conductance method are shown in Fig. 8(a). After STA, the traps in the SD and in the MOSD (Org) are located in the same energy level (around 0.35 eV), but in the case of MOSD (KOH) are located at an energy level of 0.45 eV, similar traps were observed in $Al_2O_3$/AlGaN interface [29]. The energy level of the trapping centers was further summarized in Table 1.

Table 1 Energy level of the trapping centers calculated from I-V and C-f characteristics in the SD and MOSDs before and after STA.

| $E_C$-$E_T$ (eV) | | SD | MOSD (Org) | MOSD (KOH) |
|---|---|---|---|---|
| I-V | Before | -- | 0.31 | 0.57 |
| | After | -- | 0.38 | 0.18 |
| $G_p$/w-f | Before | 0.31~ 0.45 | 0.31 | 0.56 |
| | After | 0.35 | 0.35 | 0.45 |

I-V characteristics of the HEMTs and MOS-HEMTs before and after the STA are shown in Fig. 8(b). After STA, $I_{D,max}$ decreased and $R_{ON}$ increased in all the devices, which is consistent with the $n_s$ decrease shown in Fig. 7(a). The magnitude of $I_{D,max}$ and $g_{m,max}$ were close among all three kinds of devices, 0.47±0.1 A/mm and 115 mS/mm, respectively. $R_{ON}$ of the MOS-HEMTs was 8.2 Ω·mm, 15% smaller than the HEMTs.

Transfer characterization showed that $\Delta V_{th}$ was about +0.2 V for HEMTs and MOS-HEMTs (KOH), +0.1 V for MOS-HEMTs (Org). This is similar to the results of SD and MOSD, which can be caused by the detrapped interface traps at the AlGaN/GaN interface after STA.

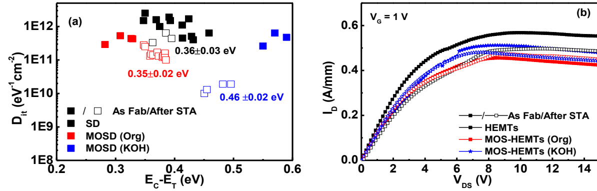


Fig. 8. (a) $D_{it}$ as a function of energy level for the diodes and (b) $I_D$-$V_{DS}$ curves of HEMTs and $HfO_2$ MOS-HEMTs before and after STA.

$I_{OFF}$ decreased by 10 to $10^2$ times in the MOS-HEMTs (Org and KOH) (Fig. 9(b)), in good agreement with the MOSDs. The highest on/off ratio after the STA (~ $10^7$) corresponded to MOS-HEMTs (KOH), which is about $10^4$ higher than the HEMTs, similar to that before STA. Therefore, MOS-HEMTs using $HfO_2$ with a KOH cleaning are suitable for high speed switch applications working at HT.

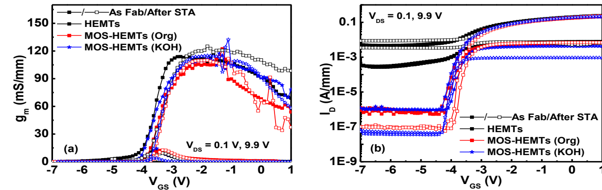


Fig. 9. (a) $g_m$-$V_{GS}$ and (b) $I_D$-$V_{GS}$ curves of $HfO_2$ MOS-HEMTs and HEMTs before and after STA.

Besides, pulsed measurements were taken in the MOS-HEMTs (KOH and Org) before and after STA (Fig. 10). The results showed that GLR increased by 25% in the MOS-HEMTs (KOH), indicating less surface trapping effects after STA. This is caused by Ga vacancies or oxygen complex reduction after annealing. Therefore, the STA is helpful to reduce the trapping effects in the MOS devices. Moreover, KOH cleaning can help reduce the C-related defects on the surface of the devices, further improve the devices characteristics.

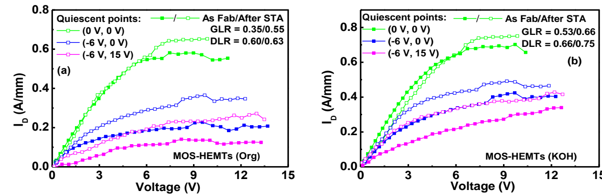


Fig. 10. Pulsed $I_D$-$V_{DS}$ curves of $HfO_2$ based (a) MOS-HEMTs (Org) and (b) MOS-HEMTs (KOH) before and after STA.

*2) Thermal Cycle Test (TC)*

Schottky and MOS-devices were subjected to a TC test from RT to 325ºC with increment of 100ºC. The $I_{rev}$ (at $V_G$ = -8 V) and $I_{for}$ (at $V_G$ = 3 V) evolution of the diodes with T are shown in Fig. 11. Results showed that $I_{rev}$ increased gradually with T in all devices. $I_{rev}$ and $I_{for}$ of MOSDs (Org and KOH) at 325°C were about $10^3$ lower than that of the SDs, demonstrating the effectiveness of the $HfO_2$ gate dielectric in the suppression of gate leakage current at HT. In addition, $I_{rev}$ and $I_{for}$ exhibited smaller than 10 times increase after TC test, showing that the increase of $I_{rev}$ caused by HT is not permanent.

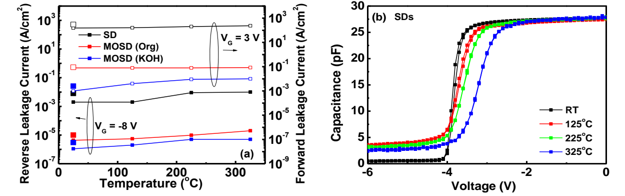


Fig. 11. (a) $I_{rev}$ and $I_{for}$ evolution of SDs and MOSDs and (b) C-V curves of SD during TC test.

No hysteresis was observed in the CV curves of SDs or MOSDs (Org and KOH) during the TC test, indicating that very few traps in the oxide near the semiconductor interface are activated by T. However, midgap-to-flatband stretchout was observed in the SDs and MOSDs (Org and KOH) with rising T, as shown in Fig. 11(b). The interface trap density was estimation with a rough calculation using the Eq. 2. The $D_{it}$ density was calculated to be $5.5\times10^{11}$ cm$^{-2}$eV$^{-1}$ for HEMTs, $2.8\times10^{11}$ cm$^{-2}$eV$^{-1}$ for MOSDs (Org) and $1.9\times10^{11}$ cm$^{-2}$eV$^{-1}$ for MOSDs (KOH). The stretch out observed here are most possibly due to the thermal inducted hot electrons at the AlGaN/GaN interface.

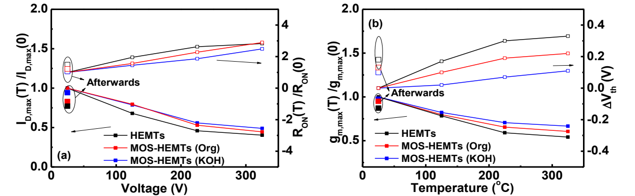


Fig. 12. (a) Evolution of $I_{D,max}$, $R_{ON}$ and (b) $g_{m,max}$, $V_{th}$ during TC test.

The electrical parameters ($I_{D,max}$, $g_{m,max}$, $R_{ON}$, $V_{th}$) evolutions of the devices (Fig. 12) show that $I_{D,max}$ and $g_{m,max}$ decrease with increasing T, and the decrease rate of MOS-HEMTs are smaller than HEMTs, and they are similar between the two devices. $I_{D,max}$ decrease of MOS-HEMTs (KOH) at 325°C was ~50%, smaller than MOS-HEMTs (Org) and HEMTs. Also it is smaller compared with the results in previous studies, where $I_{D,max}$ showed ~70% decrease at 425°C in $Al_2O_3$/AlGaN/GaN MOS-HFETs [30], $I_{D,max}$ decreased by ~40% at 200°C in $SiO_2$/AlGaN/GaN grown on sapphire [31], and $I_{D,max}$ decreased by ~60% at 425°C in $Gd_2O_3$/AlGaN/GaN MOS-HEMTs [32]. In addition, $g_{m,max}$ decreased 45% in MOS-HEMTs (KOH) at 325°C,

which is slightly lower than the $Al_2O_3$/AlGaN/GaN MOS-HFETs, where $g_{m,max}$ dropped by ~55% at 200°C [30]. These results showed that the MOS-HEMTs using $HfO_2$ with KOH cleaning have better thermal stability compared with previous studies [29-31].

$V_{th}$ shift was due to the thermal activated hot electrons, in agreement with the C-V measurements. After TC test, MOS-HEMTs (KOH) showed recovery over 95%, MOS-HEMTs (Org) over 90% and HEMTs 85%, proving that the electrical properties decrease during TC test is not permanent. Results showed that $HfO_2$ MOS-HEMTs would be a good choice for HT operation, particularly those with a KOH cleaning.

*C.Electrical stress*

*1) Step Stress*

The devices were subjected to a step stress test, as described in section II. The evolutions of the electrical parameters as a function of the stress step in the three kinds of devices are shown in Fig. 13. All devices showed $I_{D,\ max}$ decrease, but the MOS-HEMTs (KOH) showed the smallest change (~ 17%). $I_{G,\ off}$ increase of the MOS-HEMTs are negligible regardless of cleaning procedures. However, HEMTs showed dramatical $I_{G,OFF}$ increase after $V_{DG}$ = 30 V, leading to devices degradation [33]. This critical voltage phenomena can be explained by the inverse piezo effects together with the hot electrons in the devices [33–35].

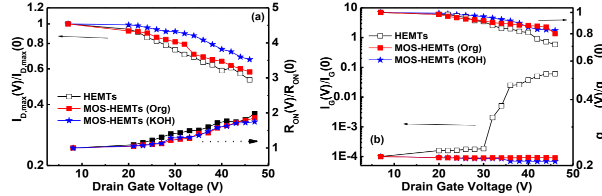

Fig. 13 (a) Evolution of $I_{D,max}$, $R_{ON}$ and (b) $I_G$, $g_{m,max}$ in the step stress test.

Crystallographic defects could be induced by the inverse piezoelectric effect caused by high vertical electric field, and acting as trapping centers at the G-D edge of the HEMTs [24, 25, 27, 28]. Also, the electron diffusion could be accelerated due to the presence of hot electrons during stress, which may accelerate the piezoelectric strain effects, enhancing the device degradation [29, 30]. This behavior was not observed in the MOS-HEMTs up to 47 V, proving that the $HfO_2$ dielectric can inhibit early degradation of the devices.

*2) High Temperature Reverse Bias (HTRB)*

Also, the devices were subjected to HTRB test, as described in section II. The devices electrical parameters variations over stress time in Fig. 14 (a) showed that after 120 h of HTRB test, the HEMTs showed 48% $I_{D.max}$ decrease, 40% $g_{m,max}$ decease and 1.5 times $R_{ON}$ increase. However, the MOS-HEMTs showed much smaller change, especially the MOS-HEMTs(KOH), $I_{D.max}$ and $g_{m,max}$ decreased by 28% and 18%, respectively, and $R_{ON}$ increased by 70%. $I_{G,OFF}$ increased by over 10 times in the HEMTs, but not in the MOS-HEMTs (KOH and Org). $V_{th}$ shifts were -0.6 V in HEMTs, -0.1 V ~ -0.3 V in MOS-HEMTs (Org), and -0.02 V ~ -0.15 V in MOS-HEMTs (KOH).

The $V_{th}$ shift as well as the electrical degradation during HTRB test are due to oxygen diffusion and field driven oxidation [41] or the structural defects caused by the electrical stress [42].

In the HEMTs, oxygen would diffuse to the GaN cap, leading to oxidation of the surface, forming grooves on the device surface [41], which might develop to pits and cracks and introduce trapping center, leading to leakage increase and electrical degradation in the devices. Another possibility is inter-diffusion between the Au in the gate metal and Ga [43], together with the existence of holes, unbounded $Ga^{3+}$ or/and $Al^{3+}$ ions may occur [44]. With the injected oxygen, $Ga_2O_3$ or/and $Al_2O_3$ could be created, bringing about pits and cracks, and causing device failure.

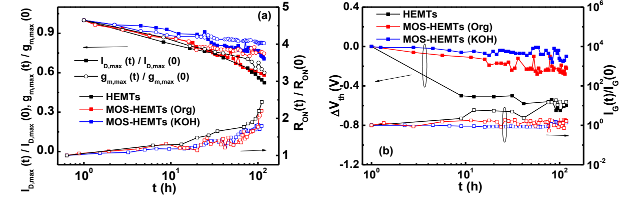

Fig. 14 (a) Evolution of $I_{D,max}$, $g_{m,max}$, $R_{ON}$ and (b) $V_{th}$, $I_G$ during HTRB test.

In the MOS-HEMTs, $HfO_2$ layer can prevent the infusion of oxygen or oxidation of the GaN, thus mitigate the structural degradation, especially in the case of the MOS-HEMTs with KOH cleaning.

After the HTRB tests, all the MOS-HEMTs showed over 98% recovery ($I_{D,max}$, $R_{ON}$, $g_{m,max}$, $V_{th}$), the HEMTs showed 85% recovery, indicating that the $HfO_2$ layer helped protect the device from possible structure damage during electrical stress.

*3) Positive bias temperature instability (PBTI)*

PBTI tests were performed on the MOS-HEMTs, as described in section II. $g_{m,max}$ decreases and $V_{th}$ shifts were observed on both kinds of MOS-HEMTs. $g_{m,max}$ decrease is due to the channel mobility decrease by ways of Coulomb scattering during PBTI stress. Dependent of $V_{th}$ shift on stress time and stress voltage follows up a power law relationship [45]:

$$\Delta V_{th} \sim (V_{GS,srtess} - V_{th0})^{\gamma} t_{stress}^{n} \quad (3)$$

where $V_{th0}$ is the initial $V_{th}$ value, $n$ and $\gamma$ are stress time and stress voltage exponent, respectively. $\gamma$ indicates the accessibility of defects in the gate dielectric, where the lower γ, the wider distribution of dielectric defects centered around the channel Fermi level. [45] By fitting the $\Delta V_{th}$ with Eq. 3, n and γ can be extracted. γ is fitted to be 1.0 for MOS-HEMTs (Org) and 2.5 for MOS-HEMTs (KOH), indicating that the MOS-HEMTs (KOH) is much more promising for reliability improvement.

## IV. CONCLUSIONS

In summary, this work has showed the improvement of electrical and thermal stability of GaN based MOS-HEMTs with $HfO_2$ compared with standard HEMTs, and the effects of KOH cleaning before dielectric deposition. Results proved that an optimized KOH treatment prior to $HfO_2$ deposition can enhance the beneficial effects of $HfO_2$/AlGaN/GaN MOS-HEMTs with respect to standard HEMTs: lower leakage current and fixed interface traps, higher drain current than the standard design. Also, this work has proven that STA can improve the interface properties of all the devices, especially in the MOS devices using KOH cleaning. Three kinds of electrical stress were carried out on the devices: step stress, HTRB and PBTI tests. $HfO_2$ MOS-HEMTs help improve the device reliability after step stress and HTRB test and MOS-HEMTs (KOH) are more reliable than MOS-HEMTs (Org) after PBTI test.

In general, this work showed that $HfO_2$ MOS-HEMTs (KOH) can help mitigate the degradation effects caused by thermal or electrical stress, and it will be a good candidate for high temperature and extensive life-time operations in the future.

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